CMOS
DATABOOK

including the latest products in microCMOS technology

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Introduction

National Semiconductor Corporation's CMOS Databook contains the industry's most comprehensive collection of high-performance CMOS products available today. Our early commitment to microCMOS technology has made possible the development of a broad spectrum of advanced devices that will simplify your design and ensure state-of-the-art systems.

microCMOS technology describes National's array of small-geometry, silicon-gate, oxide-isolated processes used to build the high-performance products found in this book. Using N- or P-well substrates and multiple-layer metal or polysilicon-interconnect structures, microCMOS processes produce feature sizes of 3.0, 2.0, or 1.5 microns, with submicron feature sizes in development. (For more detailed information, specific device family introductions are provided at the beginning of each section.) microCMOS accounts for nearly half of National's current research and development effort, and this commitment will increase through the '80s.

New microCMOS products are being introduced constantly. If you don't find what you need in this book, please contact your local National Semiconductor sales office or distributor.

Introduction

National Semiconductor Corporation a réuni dans son CMOS Databook la plus complète collection de l'industrie de circuits CMOS hautes performances actuellement disponible. National, en s'engageant depuis un certain temps dans la technologie microCMOS, a rendu possible le développement d'une large gamme de circuits performants qui simplifieront la conception de vos circuits tout en les faisant bénéficier des meilleures performances.

Les circuits performants décrits dans cet ouvrage mettent en oeuvre la technologie microCMOS National (cellules de faible géométrie MOS). Le procédé microCMOS, dispose de substrats N ou P, de structures multi-couches métalliques et interconnexions multiples, il permet d'obtenir des canaux de 3, 2 or 1,5 microns. National travaille actuellement sur des cellules inférieures au micron. (Pour une information plus detaillée, consulter au début de chaque chapitrê, les instructions particulières à chaque famille de circuits.) National consacre pratiquement la moitié de ses efforts en recherche et developpement à la technologie microCMOS. Cet effort ira sans cesse en s'accroissant au cours des années 1980.

De nouveaux produits microCMOS sortent sans cesse. Si vous ne trouvez pas dans cet ouvrage ce dont vous avez besoin, veuillez contacter votre ingénieur commercial ou votre distributeur National Semiconductor.

Einführung

Das CMOS-Datenbuch von National Semiconductor enthält in seiner neuesten Ausgabe (1984) das umfangreichste Typenspektrum an Hochleistungs-CMOS-Produkten, die derzeit in der Industrie erhältlich sind. Die frühzeitige Entscheidung von National Semiconductor für die sogenannte "microCMOS"-Technologie ermöglichte die Entwicklung eines breiten Spektrums fortschrittlicher Bauelemente, die den Entwurf moderner Systeme sehr erleichtern.

microCMOS-Technologie ist ein Oxid-isolierter Herstellungs-prozeß für Silizium-Gate-CMOS-Strukturen mit kleinen Geometrien, der die Produktion der im Datenbuch beschriebenen Hochleistungs-Bauelemente ermöglicht. Auf P- oder N-Wannen-Substraten erzeugt der microCMOS-Prozeß Strukturen mit Abmessungen von 3,0, 2,0 oder 1,5 μm und mit Polysilizium-oder Metallverbindungen. (Detailinformationen enthalten die technischen Angaben zu einer speziellen Bauelemetefamilie, die zu Reginn eines jeden Abschnittes zu finden sind.) Submikrometer-Strukturen befinden sich derzeit in Entwicklung.

Für die microCMOS-Technologie wendet National Semiconductor derzeit etwa die Hälfte der Forschungs— und Entwicklungs—Mittel auf. Dieser Anteil wird in den nächsten Jahren noch zunehmen.

Neue microCMOS-Produkte werden laufend auf den Markt gebracht. Sollten spezielle Bauelementetypen, die noch nicht im Katalog enthalten sind, benötigt werden, erteilen der örtliche Distributor oder das nächstgelegene Verkaufsburo von National Semiconductor gerne Auskunft.

Introduzione

Il databook sui dispositivi CMOS Della National Semiconductor Corporation contiene una tra le piu vaste gamme di prodotti CMOS ad alta tecnologia attualmente disponibili per l'industria.

Il nostro recente impegno verso la tecnologia CMOS. Ha reso posibile lo sviluppo di una vastissima gamma di dispositivi avanzati che semplificheranno i vostri progetti e garantiranno ai vostri sistemi una tra le piu avanzate tecnologie. La tecnologia CMOS della National comprende gli array a canale stretto, i silicon gate ed i processi con isolamento ad ossido usati per la fabbricazione di prodotti per applicazioni ad alto livello che trovere in questo calalogo.

Usando substrati drogati n oppure p e stratificazioni di alluminio a diversi livelli, oppure connessioni a polysilicio, i processi CMOS hanno in produzione canali di dimensioni da 3.0-2.0-1,5 microns, con dimensioni di submicron in sviluppo. (Per informazione pio dettagliate, indicazione specifiche per ogni famiglia sono fornito all'inizio di ciascun paragrafo).

La National dedica la meta dei propri sforzi per la ricerca e lo sviluppo della tecnologia CMOS, e questo impegno crescera senza dubbio nel corso degli anni 80.

I nuovi dispositivi CMOS vengono introdotti constantemente; nel caso in cui non trovaste cio di cui avete bisogno in questo catalogo, mettetevi in contatto con l'ufficio di zona della National oppure con il distributore di zona.

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Parts Listing

National manufactures a complete line of metal gate CMOS logic products (CD4000, 54C/74C, and 74PC). A list of these products follows. Our 54HC/74HC products offer improved performance and appear in Section 1 in datasheet form for your information and convenience.

METAL GATE CMOS

CD4000 LOGIC

Device	Description
CD4000	Dual 3-Input NOR Gate
CD4001	Buffered Quad 2-Input NOR Gate
CD4002	Buffered Dual 4-Input NOR Gate
CD4006	13-Bit Static Shift Register
CD4007	Dual Complementary Pair Plus Inverter
CD4008	4-Bit Full Adder
CD4009	Hex Buffer (Inverting)
CD4010	Hex Buffer (Non-Inverting)
CD4011	Buffered Quad 2-Input NAND Gate
CD4012	Buffered Dual 4-Input NAND Gate
CD4013	Dual D Flip-Flop
CD4014	8-Bit Static Shift Register
CD4015	Dual 4-Bit Static Shift Register
CD4016	Quad Bilateral Switch
CD4017	Decade Counter/Divider
CD4018	Presettable Divide-by-N Counter
CD4019	Dual AND/OR Select Gate
CD4020	14-Stage Ripple-Carry Binary Counter/Divider
CD4021	8-Bit Static Shift Register
CD4022	Divide-by-8 Counter/Divider with 8 Decoded Outputs
CD4023	Buffered Triple 3-Input NAND Gate
CD4024	7-Stage Ripple-Carry Binary Counter/Divider
CD4025	Buffered Triple 3-Input NOR Gate
CD4027	Dual J-K Flip-Flop
CD4028	BCD-to-Decimal Decoder
CD4029	Presettable Binary/Decade Up/Down Counter
CD4030	Quad Exclusive-OR Gate
CD4031	64-Bit Static Shift Register
CD4034	8-Bit Bi-Directional Shift Register
CD4035	4-Bit Shift Register
CD4040	12-Stage Ripple-Carry Binary Counter
CD4041	Quad True/Complement Buffer
CD4042	Quad D Latch
CD4043	Quad TRI-STATE® NOR R/S Latch
CD4044	Quad TRI-STATE NAND R/S Latch
CD4046	Phase Locked Loop
CD4047	Monostable/Astable Multivibrator
CD4048	Expandable 8-Input Gate
CD4049	Hex Inverting Buffer
CD4050	Hex Buffer
CD4051	Single 8-Channel Multiplexer
CD4052	Differential 4-Channel Multiplexer
CD4053	Triple 2-Channel Multiplexer
CD4060	14-Stage Ripple-Carry Binary Counter
CD4066	Quad Bilateral Switch
CD4069	Hex Inverter
CD4070	Quad 2-Input Exclusive OR Gate
CD4071	Buffered Quad 2-Input OR Gate
CD4072	Buffered Dual 4-Input OR Gate
CD4073	Triple 3-Input AND Gate
CD4075	Triple 3-Input OR Gate
CD4076	TRI-STATE Quad D Flip-Flop
CD4081	Buffered Quad 2-Input AND Gate
CD4082	Buffered Dual 4-Input AND Gate
CD4089	Binary Rate Multiplier
CD4093	Quad 2-Input NAND Schmitt Trigger
CD4094	8-Bit Shift Register with Latch
CD4099	8-Bit Addressable Latch
CD4503	TRI-STATE Hex Buffer
CD4507	Quad 2-Input Exclusive OR Gate
CD4510	BCD Up/Down Counter
CD4511	BCD-to-7 Segment Decoder Driver
CD4512	8-Channel Data Selector
CD4512/B	8-Channel Data Selector with Buffer
CD4514	4-Bit Latch 4-to-16 Line Decoder
CD4515	4-Bit Latch 4-to-16 Line Decoder
CD4516	Binary Up/Down Counter
CD4518	Dual Synchronous Up Counter
CD4519	4-Bit AND/OR Selector
CD4520	Dual Synchronous Up Counter
CD4522	Divide-by-N Counter (BCD)
CD4526	Divide-by-N Counter (Binary)
CD4527	Binary Rate Multiplier
CD4528	Dual Monostable Multivibrator
CD4529	Dual 4-Channel or Single 8-Channel Analog Data Selector
CD4538	Dual Monostable Multivibrator
CD4541	Programmable Timer with Oscillator
CD4543	BCD-to-7-Segment Decoder
CD4584	Hex Schmitt Trigger
CD4723	Dual 4-Bit Addressable Latch
CD4724	8-Bit Addressable Latch
CD40106	Hex Schmitt Trigger
CD40160	Synchronous Decade Counter
CD40161	Synchronous Binary Counter
CD40162	Full Synchronous Decade Counter

CD4000 LOGIC (Continued)

Device	Description
CD40163	Full Synchronous Binary Counter
CD40174	Hex D Flip-Flop
CD40175	Quad D Flip-Flop
CD40192	Decade Up/Down Counter
CD40193	Binary Up/Down Counter
CD40195	4-Bit Parallel Access Shift Register

MM54C/74C LOGIC

Device	Description
MM54C/74C00	Quad 2-Input NAND Gate
MM54C/74C02	Quad 2-Input NOR Gate
MM54C/74C04	Hex Inverter
MM54C/74C08	Quad 2-Input AND Gate
MM54C/74C10	Triple 3-Input NAND Gate
MM54C/74C14	Hex Schmitt Trigger
MM54C/74C20	Dual 4-Input NAND Gate
MM54C/74C30	8-Input AND Gate
MM54C/74C32	Quad 2-Input OR Gate
MM54C/74C42	BCD-to-Decimal Decoder
MM54C/74C48	BCD-to-7 Segment Decoder Driver
MM54C/74C73	Dual J-K Flip-Flop with Clear
MM54C/74C74	Dual D Flip-Flop
MM54C/74C76	Dual J-K Flip-Flop with Clear and Preset
MM54C/74C83	4-Bit Binary Full Adder
MM54C/74C85	4-Bit Comparator
MM54C/74C86	Quad 2-Input Exclusive OR Gate
MM54C/74C89	65-Bit (16 × 4) RAM TRI-STATE
MM54C/74C90	4-Bit Decade Counter
MM54C/74C93	4-Bit Binary Counter
MM54C/74C95	4-Bit Right-Shift/Left-Shift Register
MM54C/74C107	Dual J-K Flip-Flop
MM54C/74C150	1-of-16 Data Selector
MM54C/74C151	4-Bit Data Select/Multiplexer with Strobe
MM54C/74C154	4-to-16 Line Decoder
MM54C/74C157	Quad 2-Input Multiplexer
MM54C/74C160	Decade Counter with Asynchronous Clear
MM54C/74C161	Binary Counter with Asynchronous Clear
MM54C/74C162	Synchronous Decade Counter
MM54C/74C163	Synchronous Binary Counter
MM54C/74C164	8-Bit Serial-In/Parallel-Out Shift Register
MM54C/74C165	8-Bit Parallel-In/Serial-Out Shift Register
MM54C/74C173	TRI-STATE Quad Flip-Flop
MM54C/74C174	Hex D Flip-Flop
MM54C/74C175	Quad D Flip-Flop
MM54C/74C192	Decade Up/Down Counter
MM54C/74C193	Binary Up/Down Counter
MM54C/74C195	4-Bit Parallel Access Shift Register
MM54C/74C200	256-Bit RAM TRI-STATE
MM54C/74C221	Dual Monostable Multivibrator
MM54C/74C240	TRI-STATE Octal Buffer (Inverting Outputs)
MM54C/74C244	TRI-STATE Octal Buffer
MM54C/74C373	Octal Flow-Thru Latch TRI-STATE
MM54C/74C374	Octal D Type Flip-Flop TRI-STATE
MM54C/74C901	Hex Inverting Buffer (TTL Interface)
MM54C/74C902	Hex Non-Inverting Buffer (TTL Interface)
MM54C/74C903	Hex Inverting Buffer (TTL Interface)
MM54C/74C904	Hex Non-Inverting Buffer (TTL Interface)
MM54C/74C905	12-Bit Successive Approximation Register
MM54C/74C906	Open Drain Buffer (Active Pull Down)
MM54C/74C907	Open Drain Buffer (Active Pull Down)
MM54C/74C908	Dual High-Voltage Driver
MM54C/74C909	Quad Comparator
MM54C/74C910	256-Bit (64 × 4) RAM TRI-STATE
MM54C/74C911	4-Digit LED Display Controller
MM54C/74C912	6-Digit LED Display Controller
MM54C/74C914	Hex Schmitt Trigger with Extended Input Voltage
MM54C/74C915	7-Segment-to-BCD Decoder
MM54C/74C922	16-Key Keyboard Encoder
MM54C/74C923	16-Key Keyboard Encoder
MM54C/74C929/30	1024-Bit Static RAM
MM54C/74C932	Phase Comparator
MM54C/74C933	Address Bus Comparator
MM54C/74C941	TRI-STATE Octal Buffer
MM54C/74C945/47	4-Digit Up/Down Counter/Latch/Decoder Driver
MM54C/74C946	4 1/2-Digit Counter Decoder Driver
MM54C/74C949	8-Bit Microprocessor Compatible A/D Converter
MM54C/74C989	64-Bit (16 × 4) RAM TRI-STATE 5V

microCMOS

MM74PC LOGIC

Device	Description
MM74PC00	Quad 2-Input NAND Gate
MM74PC02	NOR Gate
MM74PC04	Hex Inverter
MM74PC08	AND Gate
MM74PC32	OR Gate
MM74PC74	Dual D Flip-Flop
MM74PC138	3-to-8 Decoder

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Section 1

54HC/74HC High Speed CMOS

1

Introduction

National has been a supplier of CMOS logic since 1970, starting with the CD4000 family. National next introduced the 54/74C Series—replicating, in CMOS, the "footprints" (pinouts) and functions of the standard TTL bipolar 7400 Logic Family.

Until recently, however, high-speed CMOS systems had to include some bipolar logic ICs as well because CMOS logic was not fast enough. The use of bipolar logic meant that system designers had interface and power dissipation problems.

AN ADVANCED, HIGH-SPEED CMOS LOGIC FAMILY

National has introduced a new, high-speed CMOS Logic Family—the 54/74HC Series.* Many industry watchers are calling it the most significant development in logic since TTL.

This new series is the first broad-based CMOS logic family to attain true bipolar (74LS) speed performance, while maintaining the many advantages of CMOS: high noise immunity, wide power supply range, wide range of operating temperature, and low power dissipation. In addition, this CMOS family offers 74LS equivalent pinouts and output drive (4 mA sink and source).

National is also supplying some of the most popular CD4000 devices in this new high-speed technology. As an example, the CD4060 will be offered as the MM74HC4060. Some new functions not currently available in any logic family (MM74HC9XX parts) will also be offered and the MM74HCTXXX designation is used for a group of special TTL buffers. (The inputs of these buffers meet TTL logic voltage level specs.)

HOW SPEED HAS BEEN IMPROVED

National uses self-aligned silicon-gate CMOS with oxide isolation to obtain speed and density advantages in these logic circuits.

To understand how this works, look at a cross-section of a logic inverter in metal-gate CMOS, as shown in *Figure 1-1*. Notice that all the key parasitics have been drawn on this diagram. The extra P^+ diffusion necessary around the N-channel device and the extra N^+ diffusion around the P-channel device are the guard rings (channel stoppers) that are necessary to prevent parasitic MOS transistors between devices. The length indicated for laying out a logic inverter (one N-channel and one P-channel device) is about 125 microns for a typical metal-gate process.

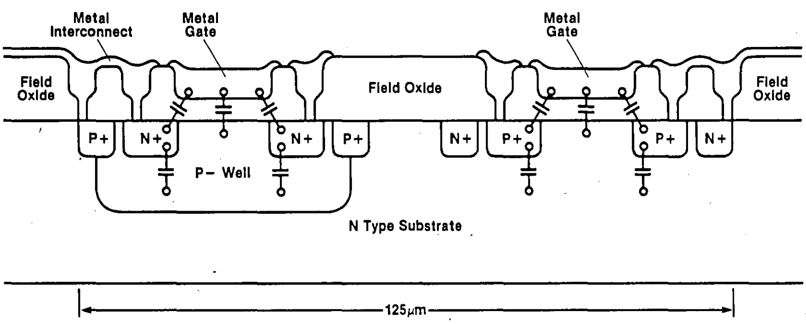


FIGURE 1-1. A Cross-Section of a Logic Inverter In Metal-Gate CMOS

*This MM54/74HC family is alternately sourced by Motorola Inc.

Now, look at the Si-gate CMOS inverter shown in *Figure 1-2*. The 125-micron distance noted previously for a simple logic inverter is reduced to only 64 microns.

With the oxide isolation performing the channel stop function:

- The need for extra channel stop diffusions is eliminated.
- The P^+ and N^+ diffusions can now butt directly against the oxide (no space is required).
- The geometries and spacings overall can be made smaller because of shallower junction depths.

Therefore, a 2:1 reduction in the parasitic capacitances can be obtained with this new CMOS process. Since the gate is self-aligned to the source and drain (i.e., the gate actually defines the separation between the source and drain regions), the gate overlap capacitance is also significantly reduced.

This decreased capacitance, combined with the 4:1 increase in the gain of the silicon-gate transistors (the silicon-gate devices have better gain due to the shorter channel length, thinner gate oxide, and lower threshold voltage), explains the speed improvement of eight to ten times over the earlier metal-gate CMOS logic.

SPECIFICATIONS FOR THE 54/74HC LOGIC FAMILY

A 2V to 6V operating range was chosen for the new 54/74HC family. The 6V maximum limit results because of transistor drain-to-source punchthrough with the short channel lengths (further reductions in channel length will bring about the new 2V to 3V power supply voltage standard for VLSI products).

There are specifications on the maximum allowable DC output current for all of the outputs as well as for the V_{CC} and ground pins. These limits exist because of the potential for metal migration...a phenomenon that occurs if DC current limits are exceeded for long time intervals. Limiting the maximum DC current flow increases the reliability of the circuit.

The input logic levels for this family are similar to standard CD4000 and 54/74C CMOS: 1.0V and 3.5V, using a 5V power supply. Over the complete supply voltage range the worst-case V_{IH} and V_{IL} input levels are typically 70% and 20% of V_{CC}, respectively. In addition, to facilitate interfacing from TTL and TTL compatible circuits to 54/74HC, a sub-family of devices (designated MM54HCT/MM74HCT) is also offered. These devices are designed and specified for TTL input logic voltage levels.

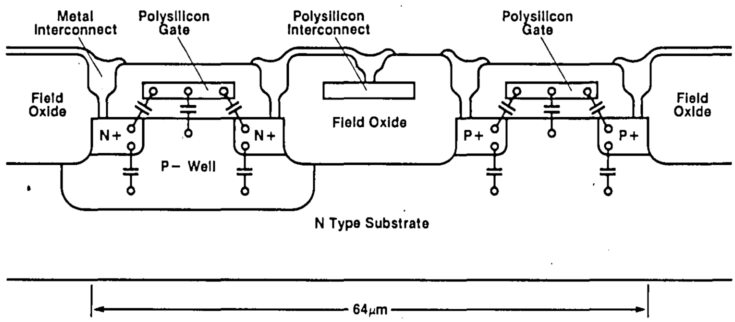


FIGURE 1-2. A Cross-Section of a Logic Inverter in microCMOS

COMPARING OUTPUT CURRENT SINK AND SOURCE

These new 74HC products can drive capacitive loads with the same response times as the 74LS products. The reasons for this can be seen by looking at the comparisons of the output current sink and source capabilities of these logic families as shown in *Figures 1-3 and 1-4.*

Here the new CMOS output stages can be seen to compare favorably with those of the 74LS bipolar logic family. It is these large output currents that provide the ability to rapidly drive load capacitance. This also requires the same attention as 74LS to PC board layouts and power supply bypass capacitors.

For complete details and characteristics of the 54/74HC family, see National's 1983 High-Speed CMOS Databook, which also contains numerous application notes.

CMOS AND BIPOLAR DESIGN

Bipolar designers who have never used CMOS must remember one important rule: never leave an input pin floating. Unused inputs must be tied to V_{CC}, ground, or an output. If left floating, an input can charge up (due to leakage current flow) to the threshold voltage level and turn ON both the N-channel and P-channel transistors at the same time. This will cause the IC to draw potentially destructive DC currents from V_{CC} to ground. This problem is aggravated by the large current capability of this new logic family.

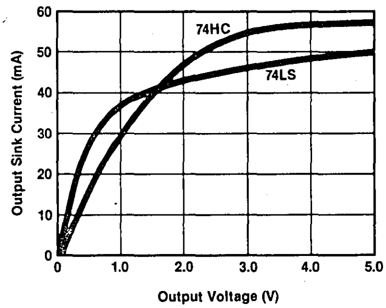


FIGURE 1-3. Comparing the Output Sink Current Capabilities of 74HC and 74LS

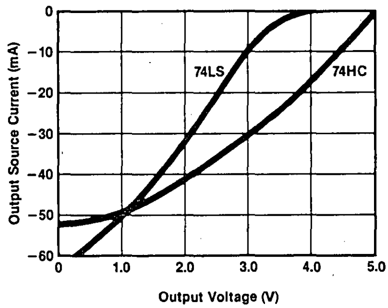


FIGURE 1-4. Comparing the Output Source Current Capabilities of 74HC and 74LS

National Semiconductor

microCMOS

MM54HC00/MM74HC00 Quad 2-Input NAND Gate

General Description

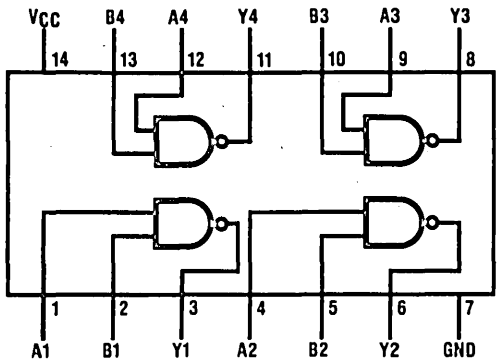
These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



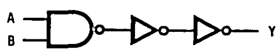
TOP VIEW

TL/F/5295-1

MM54HC00/MM74HC00

54HC00 (J) 74HC00 (J,N)

Logic Diagram



TL/F/5292-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC02/MM74HC02 Quad 2-Input NOR Gate

General Description

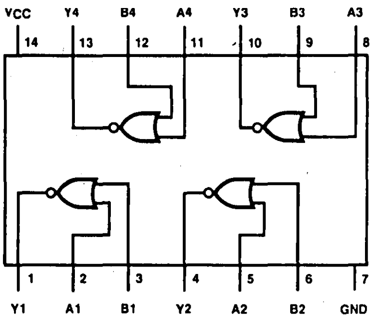
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection Diagram

Dual-In-Line Package



TL/F/5294–1

TOP VIEW

MM54HC02/MM74HC02

54HC02 (J)   74HC02 (J,N)

Logic Diagram

TL/F/5294–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IL}$ $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	45 9 8	90 18 15	113 23 19	134 27 23	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC03/MM74HC03 Quad 2-Input Open Drain NAND Gate

General Description

These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

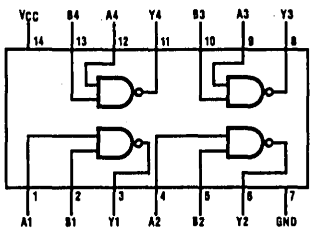
As with standard 54HC/74HC push-pull outputs there are diodes to both V_{CC} and ground. Therefore the output should not be pulled above V_{CC} as it would be clamped to one diode voltage above V_{CC}. This diode is added to enhance electrostatic protection.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



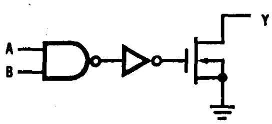
TL/F/5295-1

TOP VIEW

MM54HC03/MM74HC03

54HC03 (J) 74HC03 (J,N)

Logic Diagram



TL/F/5295-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
		R_L=1 kΩ	4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN}=V_{IH}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
		R_L=∞	4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{LKG}	Maximum High Level Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, V_{OUT}=V_{CC}	6.0V		0.5	5	10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$R_L=1$ KΩ	10	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$R_L=1$ KΩ	2.0V 4.5V 6.0V	63 13 11	125 25 21	158 32 27	186 37 32	ns ns ns
t_{THL}	Maximum Output Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$. The power dissipated by R_L is not included.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC04/MM74HC04 Hex Inverter

General Description

These Inverters utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

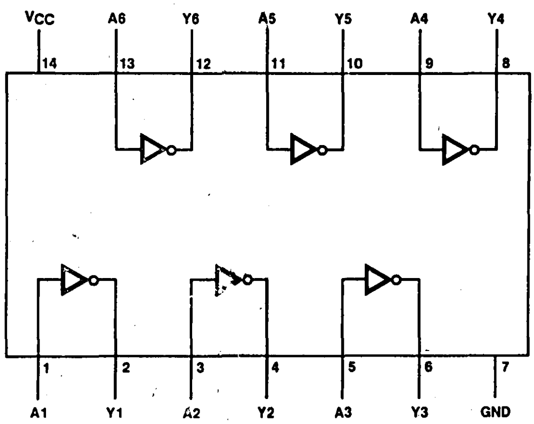
The MM54HC04/MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10 μW maximum at room temperature
- Typical input current: 10^{-5} μA

Connection Diagram

Dual-In-Line Package



TL/F/5069-1

TOP VIEW
MM54HC04/MM74HC04

54HC04 (J)   74HC04 (J,N)

Logic Diagram

TL/F/5069-2

1 of 6 Inverters

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IL}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	55 11 9	95 19 16	120 24 20	145 29 24	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC08/MM74HC08 Quad 2-Input AND Gate

General Description

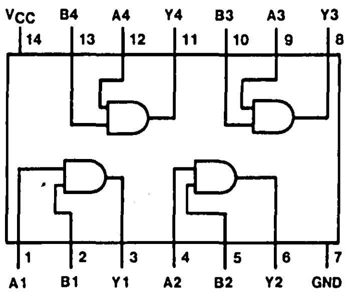
These AND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns (t_{PHL}), 12 ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2 μA maximum at room temperature
- Typical input current: 10^{-5} μA

Connection Diagram

Dual-In-Line Package



TL/F/5297-1

TOP VIEW
MM54HC08/MM74HC08

54HC08 (J) 74HC08 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, Output High to Low		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		7	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay Output High to Low		2.0V	77	121	151	175	ns
			4.5V	15	24	30	35	ns
			6.0V	13	20	25	30	ns
t_{PLH}	Maximum Propagation Delay Output Low to High		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		38				pF
C_{IN}	Maximum Input Capacitance			4	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC10/MM74HC10 Triple 3-Input NAND Gate

General Description

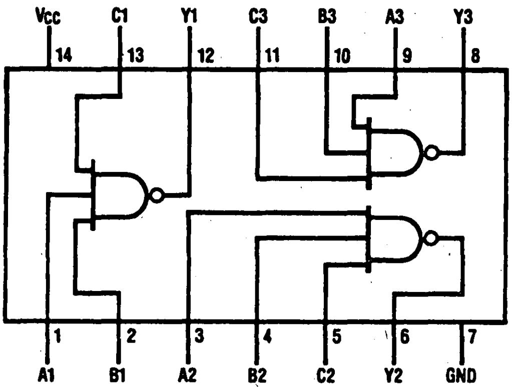
These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

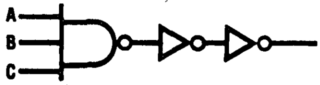


TL/F/5153-1

MM54HC10/MM74HC10

54HC10 (J) 74HC10 (J,N)

Logic Diagram



$Y = \overline{ABC}$

TL/F/5153-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	µA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	48	90	113	134	ns
			4.5V	10	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC11/MM74HC11 Triple 3-Input AND Gate

General Description

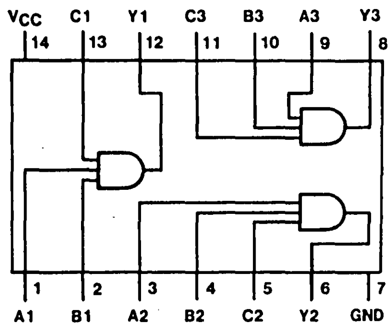
These AND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

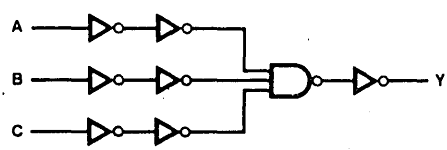


TOP VIEW
MM54HC11/MM74HC11

TL/F/5298-1

54HC11 (J)   74HC11 (J,N)

Logic Diagram



TL/F/5298-2

(1 OF 3 GATES)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	48 18 15	125 25 21	156 31 27	190 38 31	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		35				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC14/MM74HC14 Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

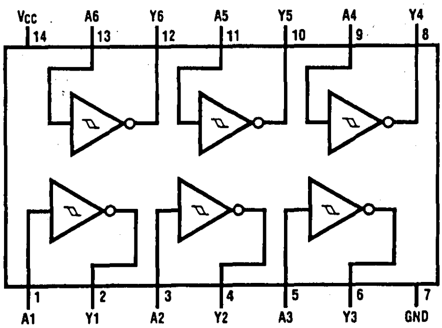
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V

Connection Diagram

Dual-In-Line Package



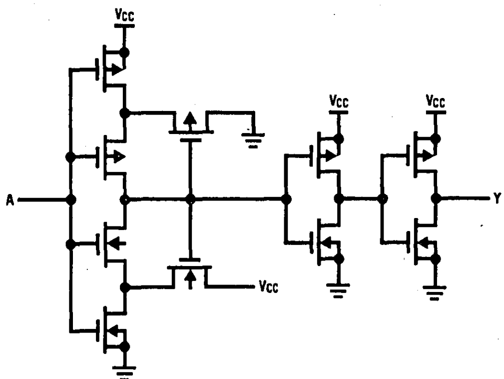
TOP VIEW

TL/F/5105-1

MM54HC14/MM74HC14

54HC14(J) 74HC14(J,N)

Schematic Diagram



TL/F/5105-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_T+	Maximum Positive Going Threshold Voltage		2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_T-	Minimum Negative Going Threshold Voltage		2.0V	0.7	0.3	0.3	0.3	V
			4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
V_H	Hysterisis Voltage	Min	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.6	0.6	0.6	V
		Max	2.0V	0.5	1.2	1.2	1.2	V
			4.5V	0.9	2.25	2.25	2.25	V
			6.0V	1.0	3.0	3.0	3.0	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IL}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

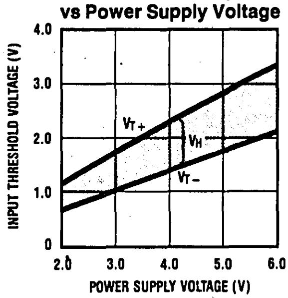
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	60 13 11	125 25 21	156 31 26	188 38 32	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

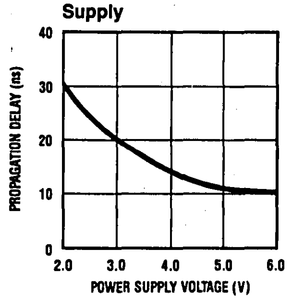
Typical Performance Characteristics

Input Threshold, V_{T+}, V_{T-}, vs Power Supply Voltage



TL/F/5105-3

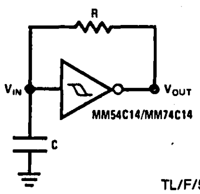
Propagation Delay vs Power Supply



TL/F/5105-4

Typical Applications

Low Power Oscillator



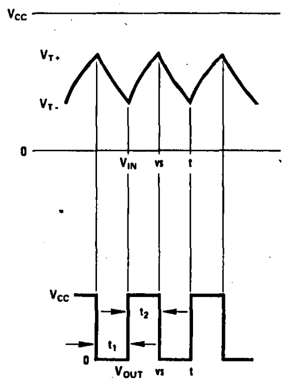
TL/F/5105-5

$t_1 \approx RC \ln \frac{V_{T+}}{V_{-T}}$

$t_2 \approx RC \ln \frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC}-V_{T-})}{V_{T-}(V_{CC}-V_{T+})}}$$

Note: The equations assume $t_1+t_2 \gg t_{pd0}+t_{pd1}$



TL/F/5105-6

National Semiconductor

microCMOS

MM54HC20/MM74HC20 Dual 4-Input NAND Gate

General Description

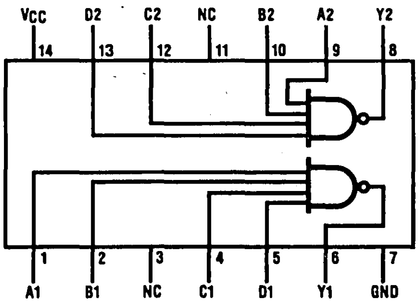
These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-Well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



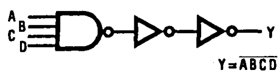
TOP VIEW

TL/F/5299–1

MM54HC20/MM74HC20

54HC20 (J) 74HC20 (J,N)

Logic Diagram



TL/F/5299–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	45 9 8	90 18 15	113 23 19	134 27 23	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC27/MM74HC27 Triple 3-Input NOR Gate

General Description

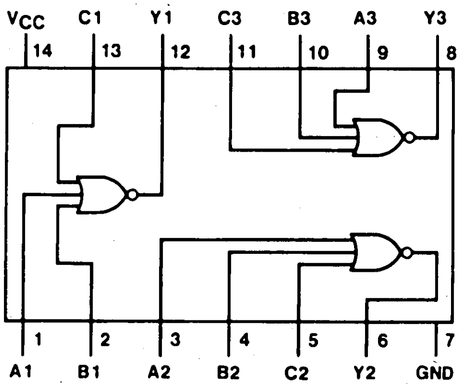
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 8 ns
- Wide Operating Supply Voltage Range: 2–6V
- Low Input Current: $< 1\ \mu A$
- Low Quiescent Supply Current: 20 μA maximum (74HC series)
- Fanout of 10 LS-TTL Loads

Connection and Logic Diagrams

Dual-In-Line Package



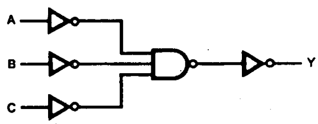
TOP VIEW

TL/F/5300-1

MM54HC27/MM74HC27

54HC27 (J) 74HC27 (J,N)

$$Y = \overline{A + B + C}$$



TL/F/5300-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	45 9 8	90 18 15	113 23 19	134 27 23	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		36				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC30/MM74HC30 8-Input NAND Gate

General Description

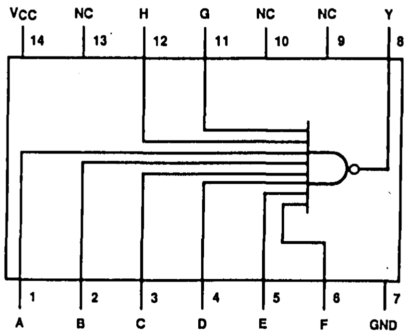
This NAND gate utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. This device has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

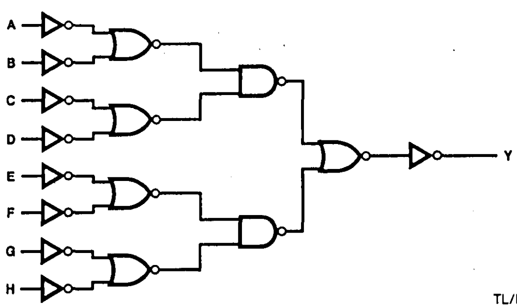
Dual-In-Line Package



TL/F/5133-1

TOP VIEW
MM54HC30/MM74HC30

54HC30 (J) 74HC30 (J,N)



Y = ABCDEFGH

TL/F/5133-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
DC Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC32/MM74HC32 Quad 2-Input OR Gate

General Description

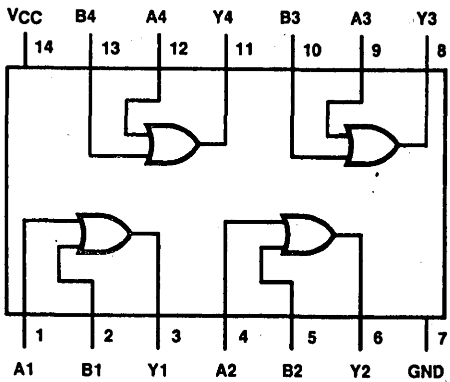
These OR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



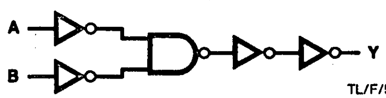
TOP VIEW

TL/F/5132-1

M54HC32/MM74HC32

54HC32 (J) **74HC32 (J,N)**

Logic Diagram



Y=A+B

TL/F/5132-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.7	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC42/MM74HC42 BCD-to-Decimal Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Data on the four input pins select one of the 10 outputs corresponding to the value of the BCD number on the inputs. An output will go low when selected, otherwise it remains high. If the input data is not a valid BCD number all outputs will remain high. The circuit has high noise immunity and low power consumption usually associated with CMOS circuitry, yet also has speeds comparable to low power Schottky TTL (LS-TTL) circuits, and is capable of driving 10 LS-TTL equivalent loads.

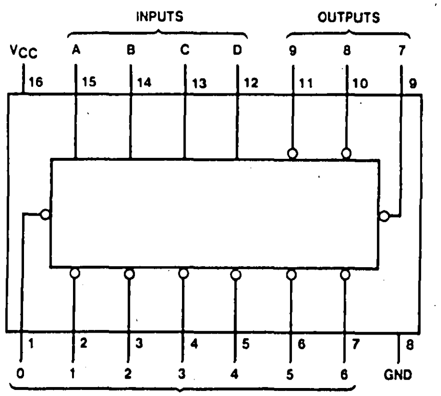
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide supply range: 2V–6V
- Low quiescent current: 80 μA (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-line Package



TOP VIEW
MM54HC42/MM74HC42

TL/F/5301-1

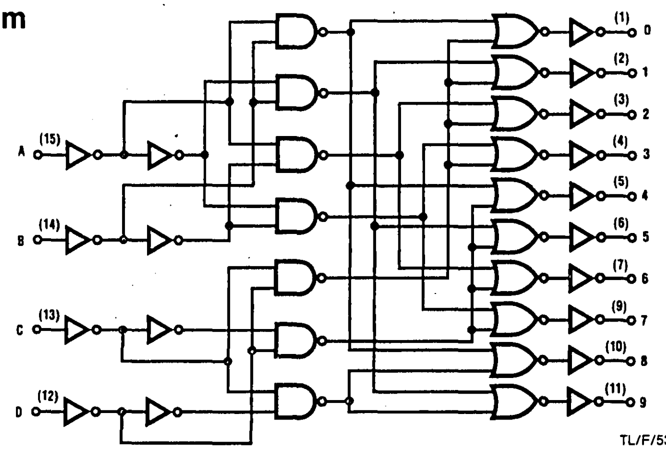
54HC42(J) 74HC42(J,N)

Truth Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level

Logic Diagram



TL/F/5301-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Minimum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		15	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	75 17 15	150 30 26	189 38 32	224 45 38	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC51/MM74HC51 Dual AND-OR-Invert Gate
MM54HC58/MM74HC58 Dual AND-OR Gate

General Description

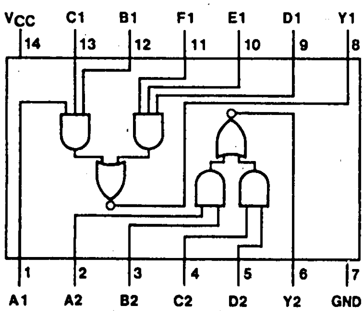
These gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74 series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection Diagrams

Dual-In-Line Package

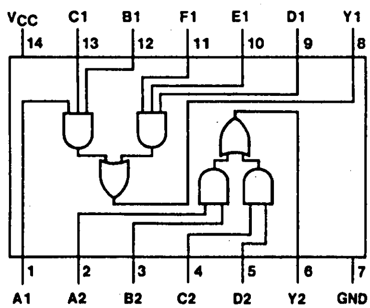


TOP VIEW TL/F/5302-1

MM54HC51/MM74HC51

54HC51 (J) 74HC51 (J,N)

Dual-In-Line Package



TOP VIEW TL/F/5302-2

MM54HC58/MM74HC58

54HC58 (J) 74HC58 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	63 13 11	125 25 21	158 32 27	186 37 32	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per AND-OR-Gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

microCMOS

MM54HC73/MM74HC73 Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent, J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family.

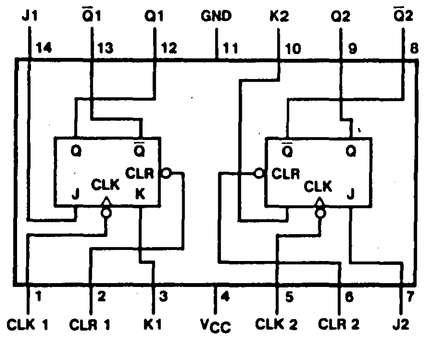
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5072-1

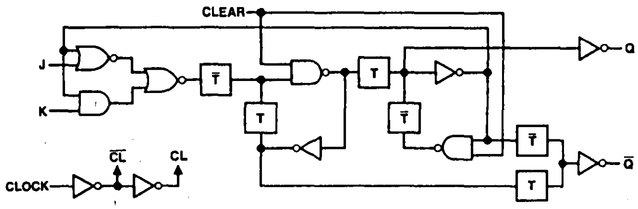
MM54HC73/MM74HC73

54HC73 (J) 74HC73 (J,N)

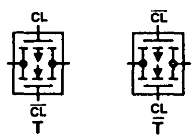
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q0}$

Logic Diagrams



TL/F/5304-2



TL/F/5304-3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

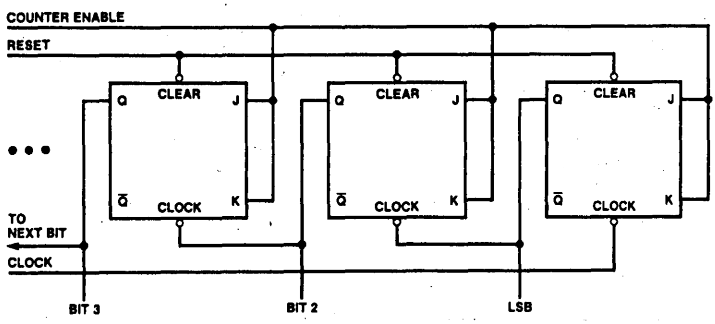
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 32	4 21 25	3 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	70 18 15	126 25 21	160 32 27	185 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	126 25 21	155 31 26	194 39 32	250 47 40	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	55 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time J or K to Clock		2.0V 4.5V 6.0V	77 15.4 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K from Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clock or Clear		2.0V 4.5V 6.0V	55 11 9	80 16 14	100 20 18	120 24 21	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

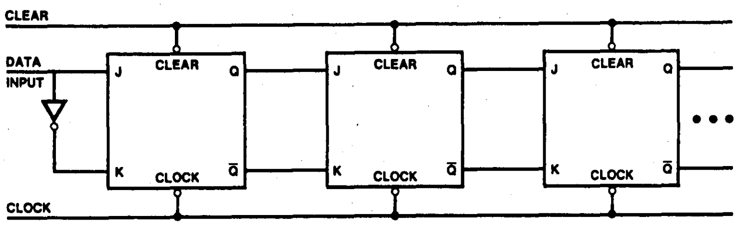
Typical Applications

N Bit binary ripple counter with enable and reset



TL/F/5072-4

N Bit shift register with clear



TL/F/5072-5

microCMOS

MM54HC74/MM74HC74 Dual D Flip-Flop with Preset and Clear

General Description

The MM54HC74/MM74HC74 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

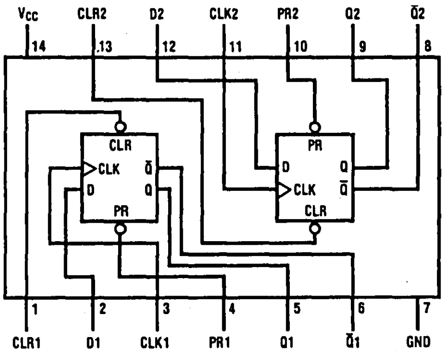
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5106-1

MM54HC74/MM74HC74

54HC74 (J) 74HC74 (J,N)

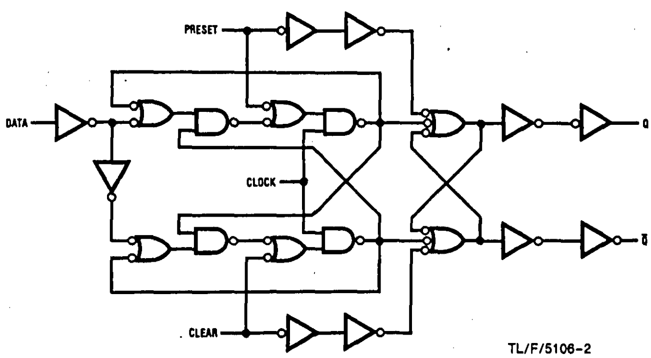
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Logic Diagram



TL/F/5106-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.3	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		25	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Set Up Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data			0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V 4.5V 6.0V	98 30 28	230 46 39	290 58 49	343 69 58	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V 4.5V 6.0V		25 5 4	32 6 5	37 7 6	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V		100 20 17	126 25 21	149 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum, Pulse Width Clock, Preset or Clear		2.0V 4.5V 6.0V	30 9 8	80 16 14	101 20 17	119 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC75/MM74HC75 4-Bit Bistable Latch with Q and $\overline{Q}$ Output

General Description

This 4-Bit Latch utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. To achieve the high noise immunity and low power consumption normally associated with standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

This latch is ideally suited for use as temporary storage for binary information processing, input/output, and indicator units. Information present at the data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information that was present at the data input at the time the transition occurred is retained at the Q output until the enable is permitted to go high again.

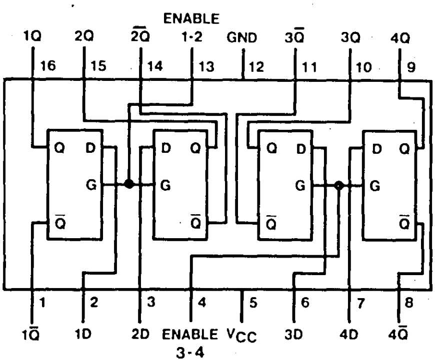
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 12 ns
- Wide operating supply voltage range: 2–6V
- Low input current: < 1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5303-1

TOP VIEW

MM54HC75/MM54HC75

54HC75 (J) 74HC75 (J,N)

Truth Table

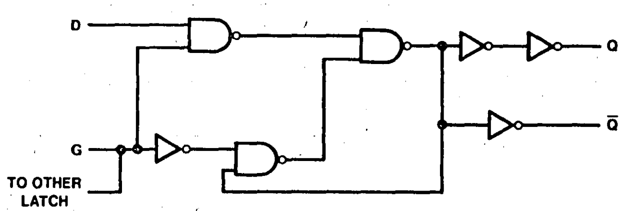
Inputs		Outputs	
D	**G**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level: L = Low Level

X = Don't Care:

Q_0 = The level of Q before the transition of G

Logic Diagram



TL/F/5303-2

(1 of 4 latches)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		14	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		10	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		16	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		11	23	ns
t_S	Minimum Set Up Time			20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		2.0V 4.5V 6.0V	37 15 14	125 25 24	156 32 27	188 38 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		2.0V 4.5V 6.0V	29 12 11	110 22 19	138 28 24	165 33 29	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		2.0V 4.5V 6.0V	40 18 16	145 29 25	181 36 31	218 44 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		2.0V 4.5V 6.0V	36 15 14	125 25 22	156 31 28	188 38 33	ns ns ns
t_S	Minimum Set Up Time Data to Enable		2.0V 4.5V 6.0V	40 10 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Enable to Data		2.0V 4.5V 6.0V	−10 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Enable Pulse Width		2.0V 4.5V 6.0V	40 11 9	80 16 14	100 20 18	120 24 21	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		40				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC76/MM74HC76 Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon P-well CMOS, to achieve, the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

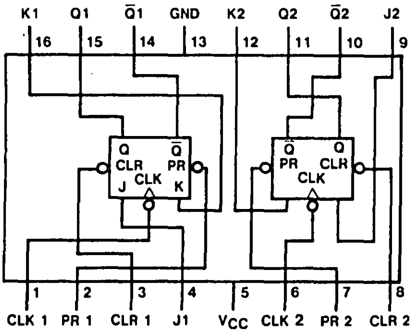
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5074-1

MM54HC76/MM74HC76

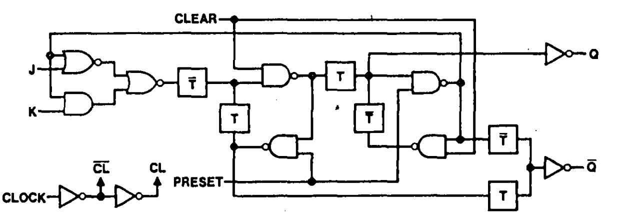
54HC76 (J) 74HC76 (J,N)

Truth Table

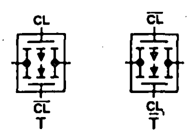
Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed

Logic Diagrams



TL/F/5307-2



TL/F/5307-3

MM54HC76/MM74HC76

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time,		10	20	ns
t_S	Minimum Set Up Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

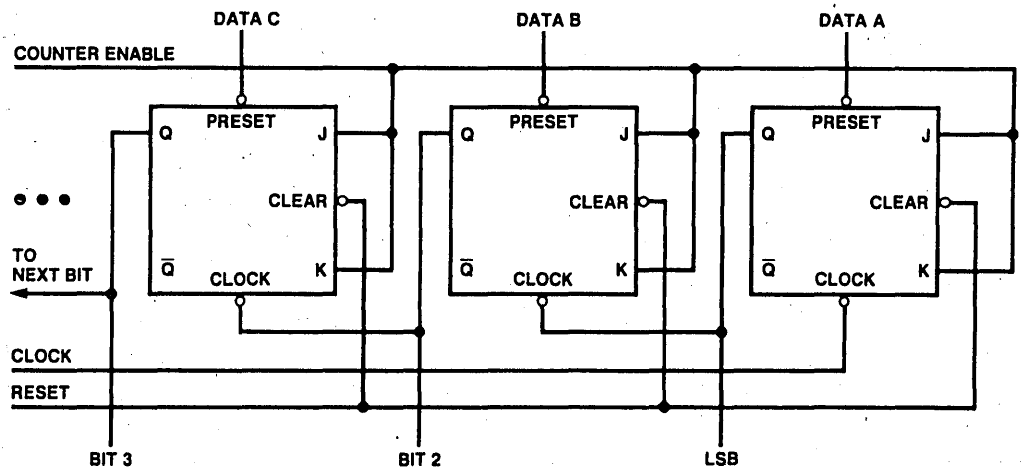
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	100 20 17	126 25 21	160 31 27	183 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	126 25 21	155 31 26	191 39 33	250 47 40	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	137 27 23	165 33 28	210 41 35	240 50 40	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V	55 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Time J or K to Clock		2.0V 4.5V 6.0V	77 15 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K from Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum, Pulse Width, Preset, Clear or Clock		2.0V 4.5V 6.0V	55 11 9	80 16 14	100 20 18	120 24 21	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

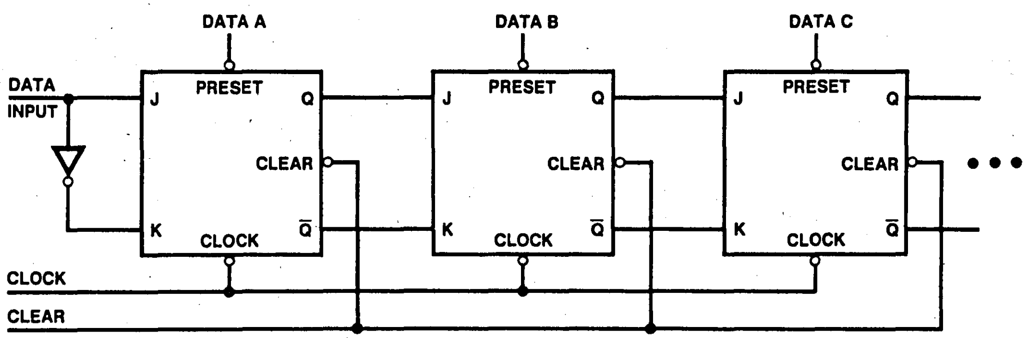
Typical Applications

N Bit presettable ripple counter with enable and reset



TL/F/5074-4

N Bit parallel load/serial load shift register with clear



TL/F/5074-5

National Semiconductor

microCMOS

MM54HC85/MM74HC85 4-Bit Magnitude Comparator

General Description

The MM54HC85/MM74HC85 is a 4-bit magnitude comparator that utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It is designed for high speed comparison of two four bit words. This circuit has eight comparison inputs, 4 for each word; three cascade inputs (A < B, A > B, A = B); and three decision outputs (A < B, A > B, A = B). The result of a comparison is indicated by a high level on one of the decision outputs. Thus it may be determined whether one word is "greater than," "less than," or "equal to" the other word. By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than four bits can be compared. In addition the least significant stage must have a high level applied to the A = B input, and a low level to the A < B, and A > B inputs.

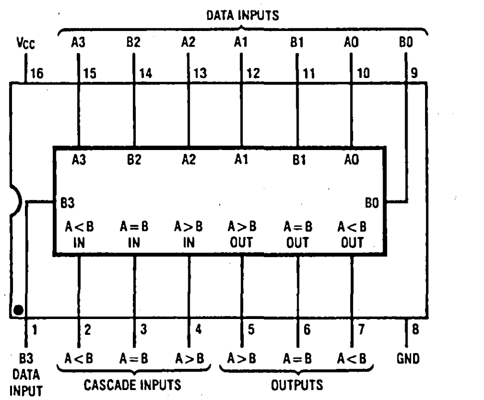
The comparator's outputs can drive 10 low power Schottky TTL (LS-TTL) equivalent loads, and is functionally, and pin equivalent to the 54LS85/74LS85. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 27 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5205-1

MM54HC85/MM74HC85

54HC85 (J) 74HC85 (J,N)

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC Vcc or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A<B or A>B		20	36	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A=B Input to A=B Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output		13	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A=B		20	30	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

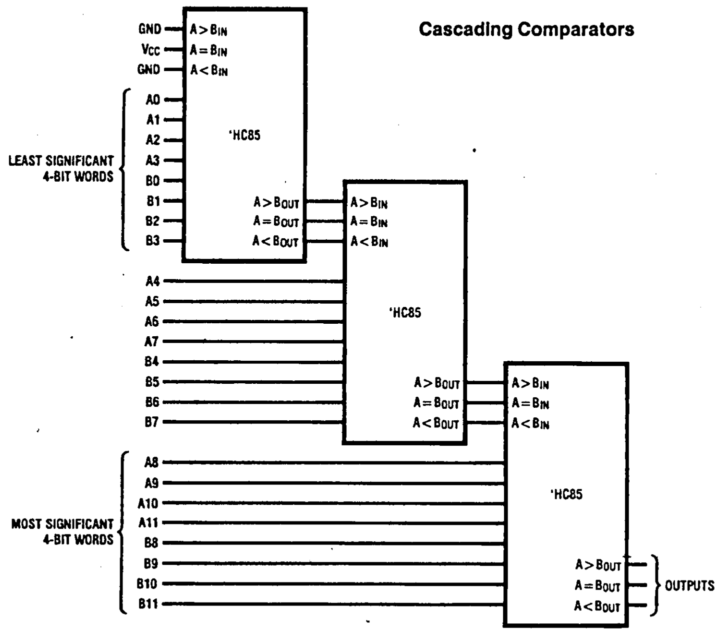
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to Output		2.0V 4.5V 6.0V	100 21 18	210 42 36	265 53 45	313 63 53	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A=B Output		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A=B Input to A=B Output		2.0V 4.5V 6.0V	63 13 11	125 25 21	158 32 27	186 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output (except A=B)		2.0V 4.5V 6.0V	70 16 13	155 31 26	195 39 33	231 46 39	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\,V_{CC}^2\,f + I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\,V_{CC}\,f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

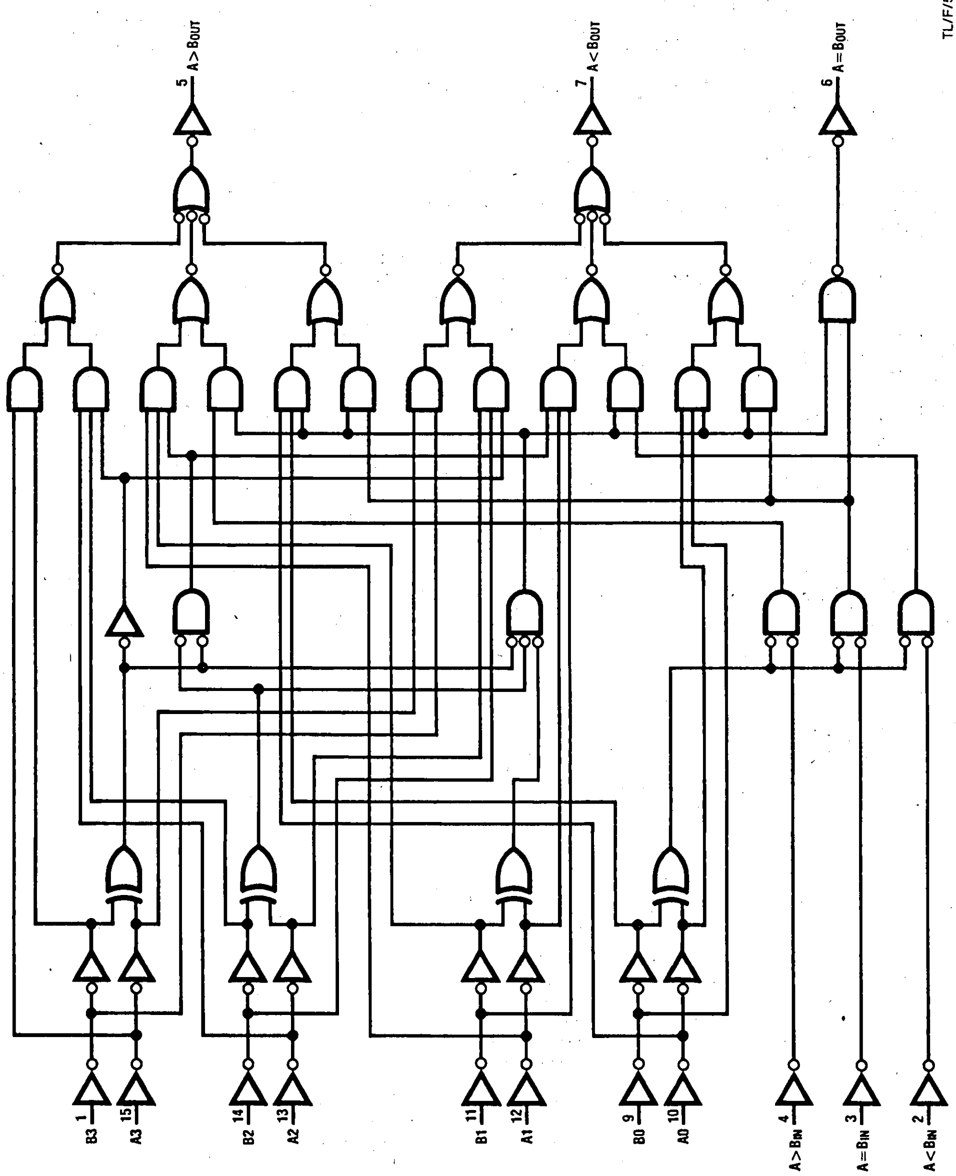
Typical Application

Cascading Comparators



TL/F/5205-4

Logic Diagram



TL/F/5205-3

National Semiconductor

microCMOS

MM54HC86/MM74HC86 Quad 2-Input Exclusive OR Gate

General Description

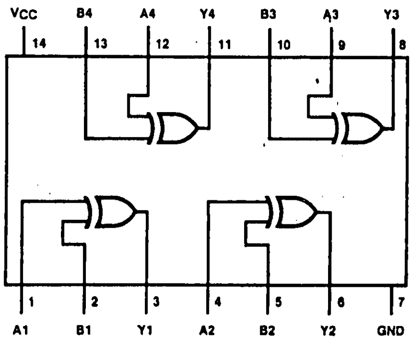
This EXCLUSIVE OR gate utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5305-1

TOP VIEW

MM54HC86/MM54HC86

54HC86 (J) **74HC86 (J,N)**

Truth Table

Inputs		Outputs
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA $|I_{OUT}|\leq$5.2 mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA $|I_{OUT}|\leq$5.2 mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC107/MM74HC107 Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

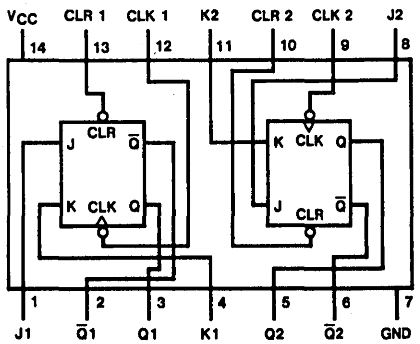
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5304-1

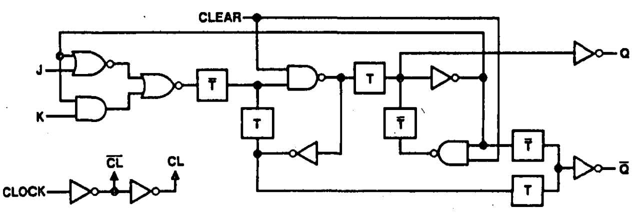
MM54HC107/MM74HC107

54HC107 (J) 74HC107 (J,N)

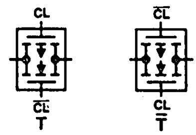
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q0}$

Logic Diagrams



TL/F/5304-2



TL/F/5304-3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

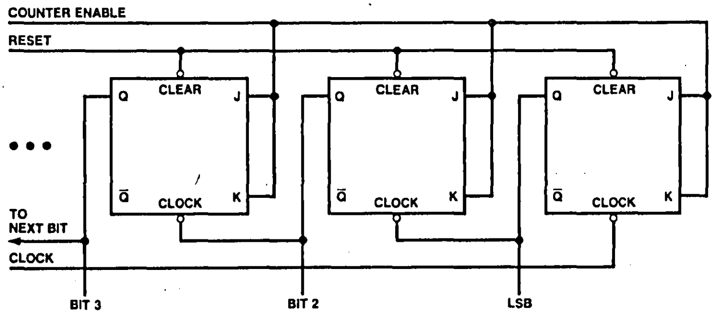
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	70 18 16	126 25 21	160 32 27	185 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	126 25 21	155 31 26	194 39 32	250 47 40	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	55 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time J or K to Clock		2.0V 4.5V 6.0V	77 15 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K to Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clear or Clock		2.0V 4.5V 6.0V	55 11 10	80 16 14	100 20 18	120 24 21	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

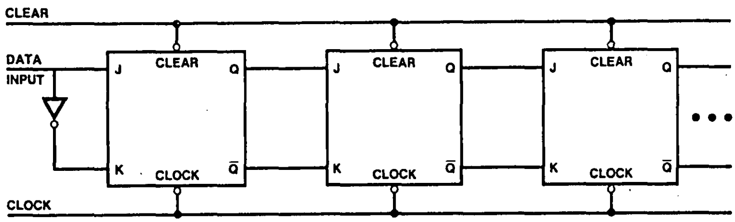
Typical Applications

N Bit binary ripple counter with enable and reset



TL/F/5072-4

N bit shift register with clear



TL/F/5072-5

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC109/MM74HC109 Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These J-$\overline{K}$ FLIP-FLOPS utilize microCMOS Technology, 3.5 micron silicon gate P-Well CMOS to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$ PRESET, CLEAR and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

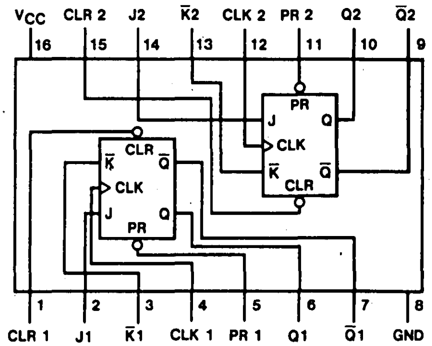
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5306-1

MM54HC109/MM74HC109

54HC109 (J)   74HC109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		21	42	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Set Up Time, J or $\overline{K}$ to Clock			20	ns
t_H	Minimum Hold Time, J or $\overline{K}$ to Clock			0	ns
t_W	Minimum Pulse Width: Preset, Clear or Clock		9	16	ns

AC Electrical Characteristics

$C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	4 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	115 23 20	230 46 39	290 58 49	343 69 58	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V	−10 5 3	25 5 4	32 6 5	37 7 6	ns ns ns
t_S	Minimum Set Time J or $\overline{K}$ to Clock		2.0V 4.5V 6.0V		100 20 17	126 25 21	119 30 20	ns ns ns
t_H	Minimum Hold Time Clock to J or K		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clock, Preset or Clear		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC112/MM74HC112 Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

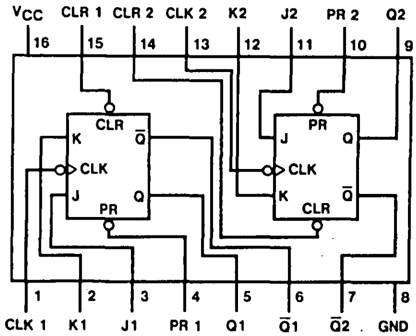
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5307-1

MM54HC112/MM74HC112

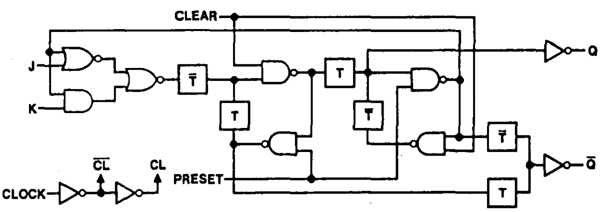
54HC112 (J) 74HC112 (J,N)

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

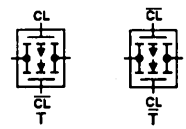
*This is an unstable condition, and is not guaranteed

Logic Diagrams



TL/F/5307-2

MM54HC112/MM74HC112



TL/F/5307-3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		10	20	ns
t_S	Minimum Set Up Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width Clock Preset or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

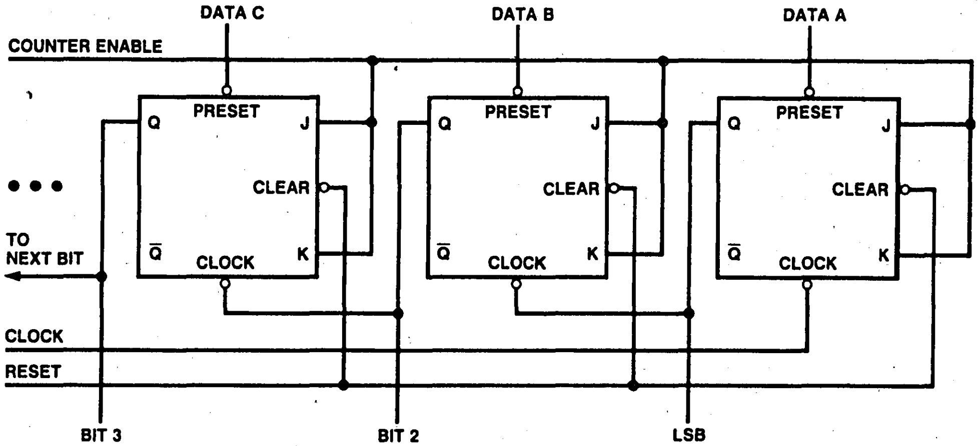
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	100	126	160	183	ns
			4.5V	20	25	32	37	ns
			6.0V	17	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		2.0V	126	155	191	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	33	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	210	240	ns
			4.5V	27	33	41	50	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9.4	17	21	25	ns
t_S	Minimum Set Up Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

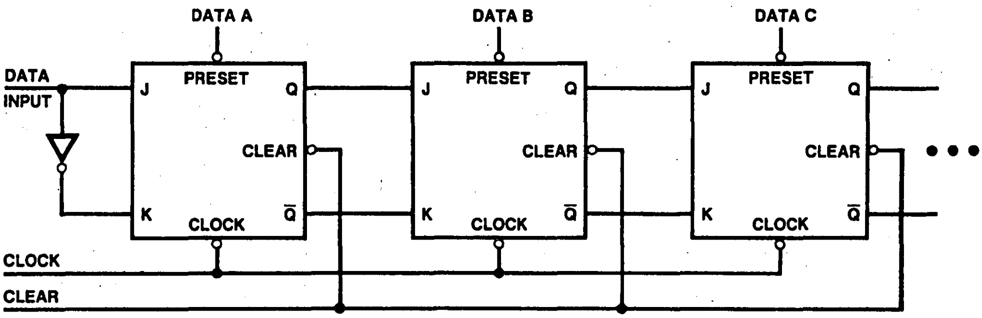
Typical Applications

N Bit presettable ripple counter with enable and reset



TL/F/5074-4

N Bit parallel load/serial load shift register with clear



TL/F/5074-5

National Semiconductor

microCMOS

MM54HC113/MM74HC113 Dual J-K Flip-Flops with Preset

General Description

These high speed J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and PRESET inputs and Q and $\overline{Q}$ inputs. PRESET is independent of the clock and accomplished by a low level on the input.

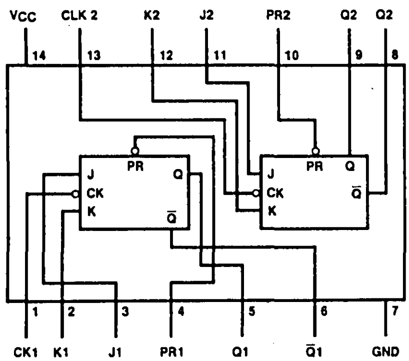
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5073-1

TOP VIEW

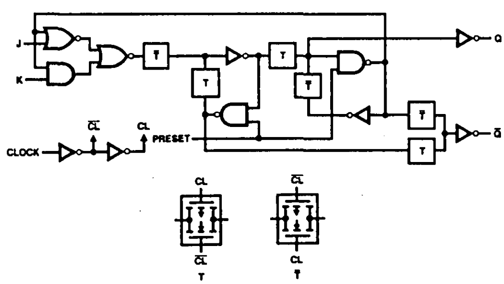
MM54HC113/MM74HC113

54HC113 (J) 74HC113 (J,N)

Inputs				Outputs	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q0}$

Logic Diagram

MM54HC113/MM74HC113



TL/F/5073-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset to Clock		10	20	ns
t_S	Minimum Set Up Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time, J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

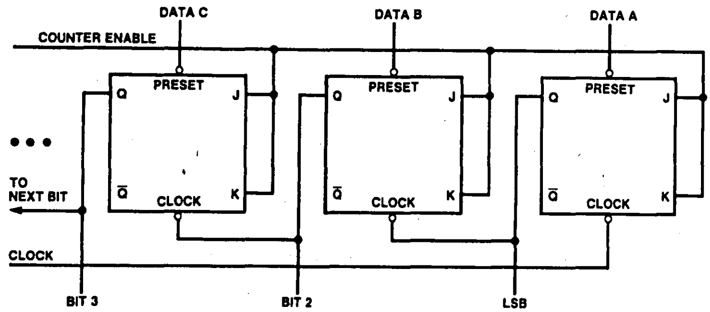
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	100 20 17	125 25 33	160 32 27	183 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	137 27 23	165 33 28	206 41 35	239 47 40	ns ns ns
t_{REM}	Minimum Removal Time Preset to Clock		2.0V 4.5V 6.0V	55 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time J or K to Clock		2.0V 4.5V 6.0V	77 15 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K from Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		2.0V 4.5V 6.0V	55 11 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

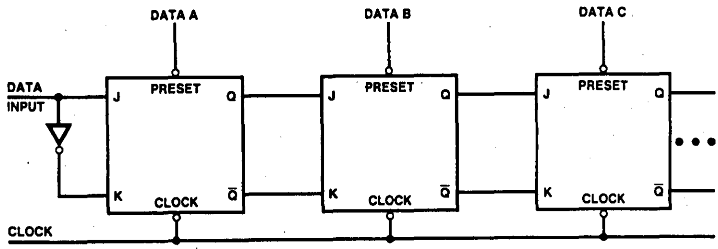
Typical Applications

N Bit presettable binary ripple counter with enable



TL/F/5073-3

N Bit parallel load/serial load shift register



TL/F/5073-4

National Semiconductor

microCMOS

MM54HC123A/MM74HC123A Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC123A high speed monostable multivibrators (one shots) utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC123 can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC123A is retriggerable. That is it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

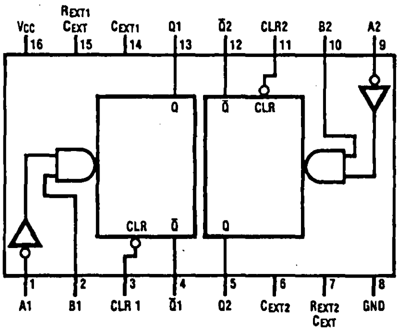
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise and fall times.

Connection Diagram

Dual-In-Line Package

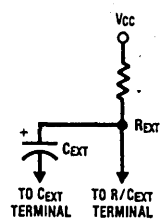


TOP VIEW TL/F/5206–1

MM54HC123A/MM74HC123A

54HC123A (J) 74HC123A (J,N)

Timing Component



TL/F/5206–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔
↑	L	H	⎍	⊔

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Clear Input)			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\lvert I_{OUT}\rvert \le$ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\lvert I_{OUT}\rvert \le$ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le$ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\lvert I_{OUT}\rvert \le$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\lvert I_{OUT}\rvert \le$4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN}=V_{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (All other pins)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Standby)	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN}=V_{CC} or GND	2.0V	36	80	110	130	μA
		R/C_{EXT}=0.5V_{CC}	4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating:

Plastic "N" Package: −12mW/°C from 65°C to 85°C

Ceramic "J" Package: −12mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

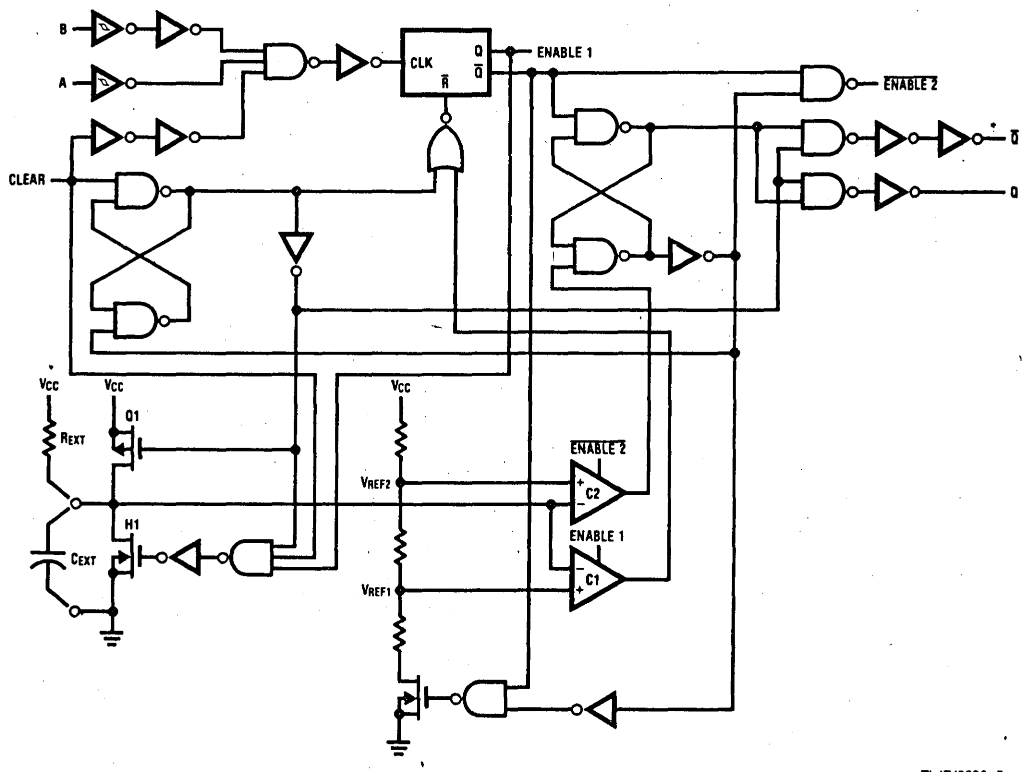
Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits			
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V 4.5V 6.0V	77 26 21	169 42 32	194 51 39	210 57 44	ns ns ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V 4.5V 6.0V	88 29 24	197 48 38	229 60 46	250 67 51	ns ns ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V 4.5V 6.0V	54 23 19	114 34 28	132 41 33	143 45 36	ns ns ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V 4.5V 6.0V	56 25 20	116 36 29	135 42 34	147 46 37	ns ns ns
t_W	Minimum Pulse Width A, B, Clear			2.0V 4.5V 6.0V	57 17 12	123 30 21	144 37 27	157 42 30	ns ns ns
t_{REM}	Minimum Clear Removal Time			2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ $R_{EXT}=6$ kΩ ($V_{CC}=2V$)		2.0V 4.5V 6.0V	1.5 450 380				μs ns ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9			ms
			Max	4.5V	1	1.1			ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				6	10	10	10	pF

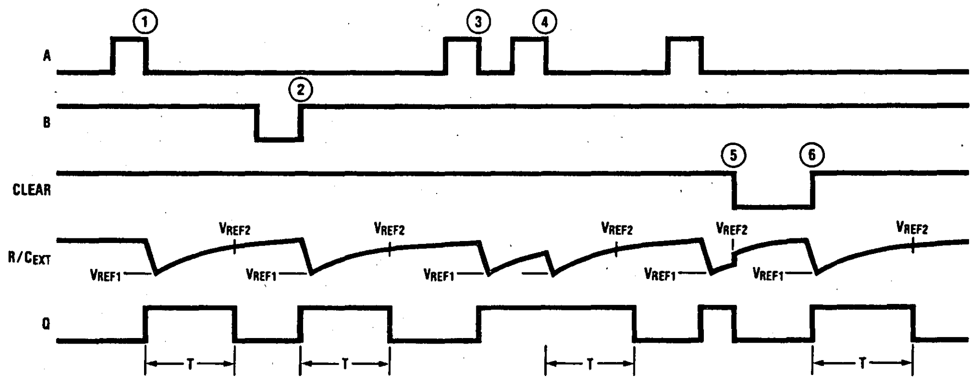
Note 5: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5206–5

Theory of Operation



TL/F/5206–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER ('HC123, 'HC221 ONLY)

FIGURE 1

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}②.) The 'HC123 can also be triggered when clear goes from GND to V_{CC} (while A is at GND and B is at V_{CC}⑥.)

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC123 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

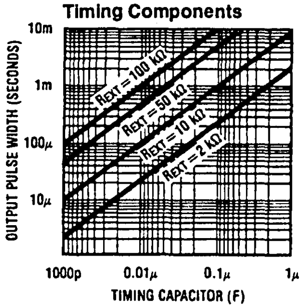
RETRIGGER OPERATION

The 'HC123 is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

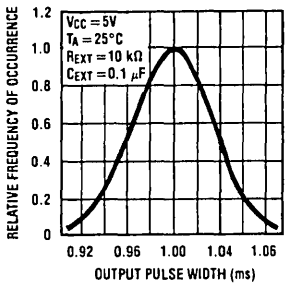
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



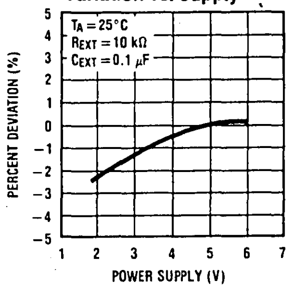
TL/F/5206-7

Typical Distribution of Output Pulse Width, Part to Part



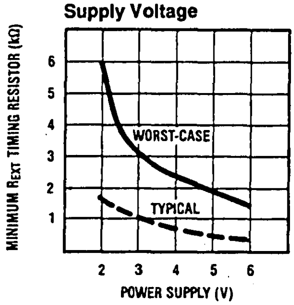
TL/F/5206-8

Typical 1ms Pulse Width Variation vs. Supply



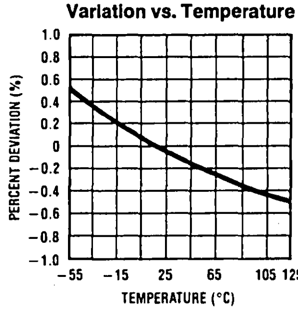
TL/F/5206-9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5206-10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5206-11

Note: R and C are not subjected to temperature. The C is polypropolyne.

National Semiconductor

microCMOS

MM54HC125/MM74HC125 MM54HC126/MM74HC126 TRI-STATE® QUAD BUFFERS

General Description

These are general purpose TRI-STATE high speed non-inverting buffers utilizing microCMOS technology, 3.5 micron silicon gate P-well CMOS. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM54HC125/MM74HC125 require the TRI-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM54HC126/MM74HC126 requires the control input to be low to put the output into high impedance.

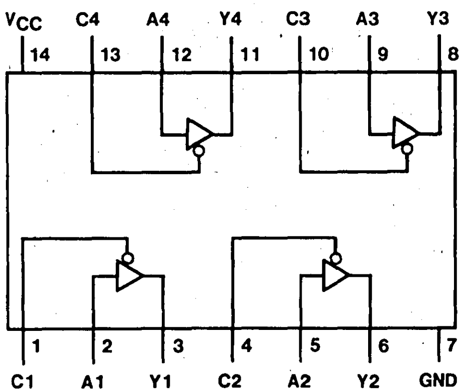
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC)
- Fanout of 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

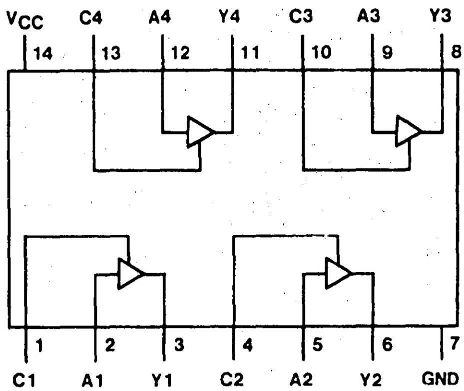


TOP VIEW TL/F/5308-1

MM54HC125/MM74HC125

54HC125 (J) 54HC125 (J,N)

Dual-In-Line Package



TOP VIEW TL/F/5308-2

MM54HC126/MM74HC126

54HC126 (J) 54HC126 (J,N)

Truth Tables

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	5.7	5.74	5.48	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND C_n=Disabled	6.0V		±0.5	±5	±10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to High Level	$R_L=1$ kΩ	13	25	ns
t_{PHZ}	Maximum Output Disable Time from High Level	$R_L=1$ kΩ, $C_L=5$ pF	17	25	ns
t_{PZL}	Maximum Output Enable Time to Low Level	$R_L=1$ kΩ	18	25	ns
t_{PLZ}	Maximum Output Disable Time from Low Level	$R_L=1$ kΩ, $C_L=5$ pF	13	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	54HC/74HC $T_A=25°C$ Typ	54HC/74HC $T_A=25°C$ Guaranteed Limits	74HC −40 to 85°C Guaranteed Limits	54HC −55 to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	8	17	21	25	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	$C_L=150$ pF	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=150$ pF, $R_L=1$ kΩ	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) Enabled		45				pF
		Disabled		6				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC132/MM74HC132 Quad 2-Input NAND Schmitt Trigger

General Description

The MM54HC132/MM74HC132 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

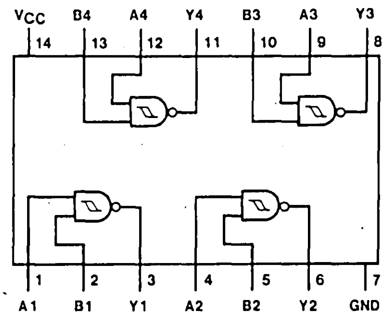
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V.

Connection Diagram

Dual-In-Line Package



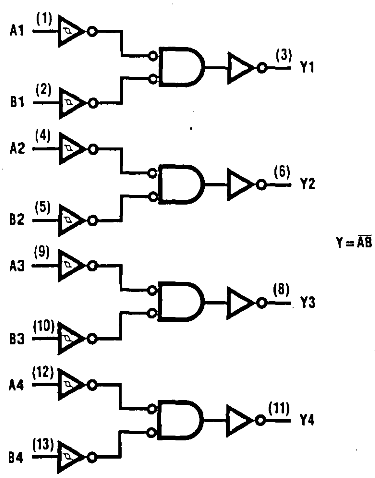
TOP VIEW

TL/F/5309-1

MM54HC132/MM74HC132

54HC132 (J)   74HC132 (J,N)

Logic Diagram



TL/F/5309-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
						Guaranteed Limits			
V_{T+}	Positive Going Threshold Voltage		Min	2.0V		1.0	0.95	0.95	V
			Max			1.5	1.5	1.5	V
			Min	4.5V		2.30	2.25	2.25	V
			Max			3.15	3.15	3.15	V
			Min	6.0V		3.0	2.95	2.95	V
			Max			4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage		Min	2.0V		0.3	0.3	0.3	V
			Max			0.8	0.85	0.85	V
			Min	4.5V		0.9	0.9	0.9	V
			Max			2.0	2.05	2.05	V
			Min	6.0V		1.2	1.2	1.2	V
			Max			2.3	2.35	2.35	V
V_H	Hysteresis Voltage		Min	2.0V		0.2	0.2	0.2	V
			Max	2.0V		1.2	1.2	1.2	V
			Min	4.5V		0.4	0.4	0.4	V
			Max	4.5V		2.25	2.25	2.25	V
			Min	6.0V		0.6	0.6	0.6	V
			Max	6.0V		3.0	3.0	3.0	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$		2.0V	2.0	1.9	1.9	1.9	V
				4.5V	4.5	4.4	4.4	4.4	V
				6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA		4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA		6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$		2.0V	0	0.1	0.1	0.1	V
				4.5V	0	0.1	0.1	0.1	V
				6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA		4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA		6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$		6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	63 13 11	125 25 21	158 32 27	186 37 32	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						pF
C_{IN}	Maximum Input Capacitance				5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC133/MM74HC133 13-Input NAND Gate

General Description

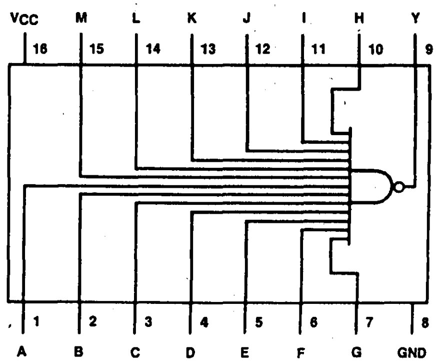
This NAND gate utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

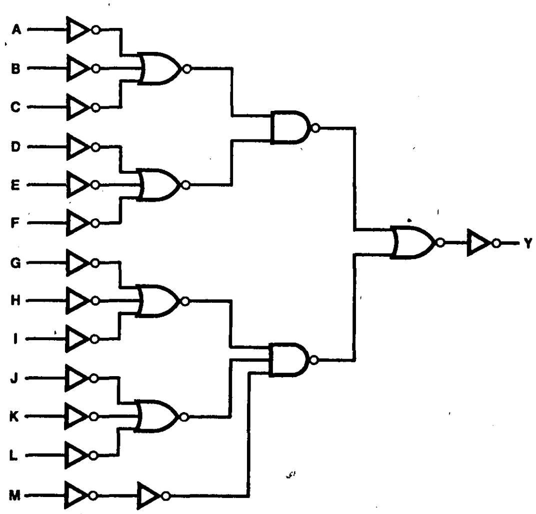
Dual-In-Line Package



TL/F/5134-1

MM54HC133/MM74HC133
54HC133 (J) 74HC133 (J,N)

Logic Diagram



TL/F/5134-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC137/MM74HC137 3-to-8 Line Decoder With Address Latches (Inverted Output)

General Description

This device utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

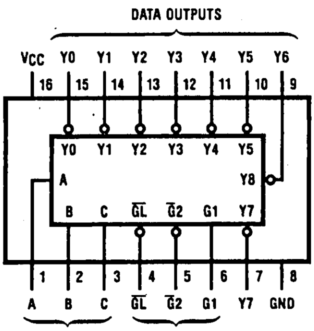
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

Connection Diagram

Dual-In-Line Package

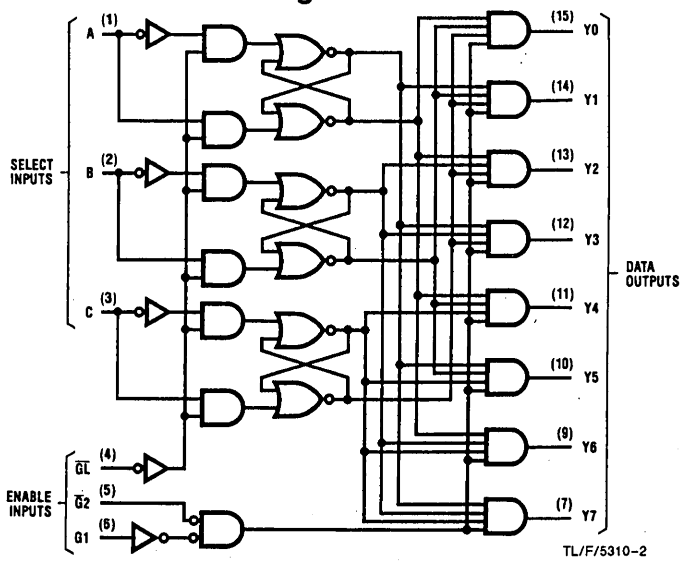


TOP VIEW TL/F/5310-1

MM54HC137/MM74HC137

54HC137 (J) 74HC137 (J,N)

Functional Block Diagram



TL/F/5310-2

Truth Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L; all others, H							

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		14	29	ns
t_{PHL}	Maximum Propagation Delay, A, B or C to any Y Output		20	42	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		12	22	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		15	34	ns
t_{PLH}	Maximum Propagation Delay G1 to any Output		13	25	ns
t_{PHL}	Maximum Propagation Delay GL to any Output		17	34	ns
t_{PLH}	Maximum Propagation GL to Output		15	30	ns
t_{PHL}	Maximum Propagation Delay GL to Output		22	34	ns
t_S	Minimum Setup Time at A, B and C Inputs			20	ns
t_H	Minimum Hold Time at A, B and C Inputs			0	ns
t_W	Minimum Pulse Width of Enabling Pulse at GL			16	ns

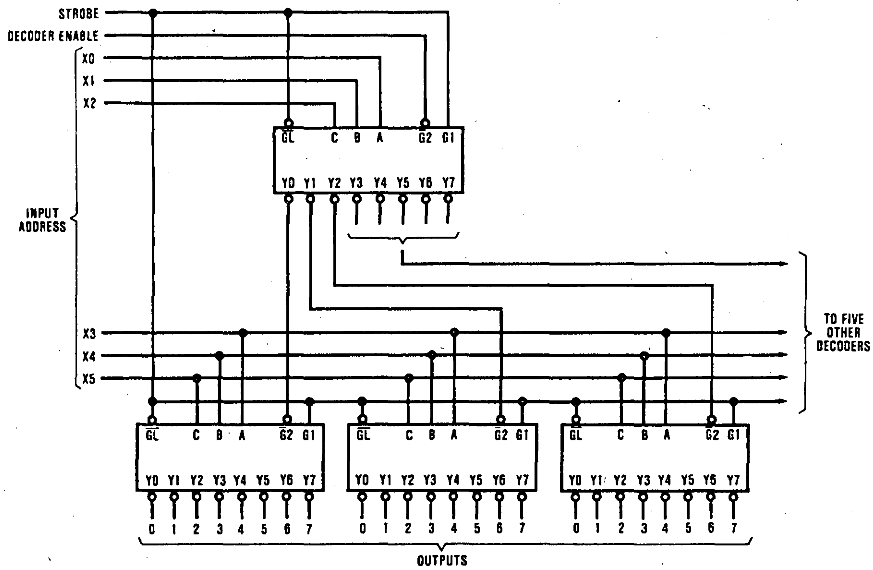
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		2.0V 4.5V 6.0V	85 17 14	170 34 29	214 43 36	253 51 43	ns ns ns
t_{PHL}	Maximum Propagation Delay A, B or C to any Y Output		2.0V 4.5V 6.0V	120 24 20	240 48 41	302 60 51	358 72 61	ns ns ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		2.0V 4.5V 6.0V	65 13 11	130 26 22	164 33 28	194 39 33	ns ns ns
t_{PLH}	Maximum Propagation Delay G1 to Output		2.0V 4.5V 6.0V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}	Maximum Propagation Delay G1 to Output		2.0V 4.5V 6.0V	98 20 17	195 39 33	246 49 42	291 58 49	ns ns ns
t_{PLH}	Maximum Propagation Delay GL to Output		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}	Maximum Propagation Delay GL to Output		2.0V 4.5V 6.0V	125 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$, to any Y Output		2.0V 4.5V 6.0V	98 20 17	195 39 33	246 49 42	291 58 49	ns ns ns
t_S	Minimum Setup Time at A, B and C Inputs		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time at A, B and C Inputs		2.0V 4.5V 6.0V		50 10 8	63 13 11	75 15 13	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V 4.5V 6.0V		80 16 14	100 20 18	120 24 21	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Typical Application



TL/F/5310-3

6-Line to 64-Line Decoder with Input Address Storage

National Semiconductor

microCMOS

MM54HC138/MM74HC138 3-to-8 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC138/MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, $\overline{G2A}$ and $\overline{G2B}$) are provided to ease the cascading of decoders.

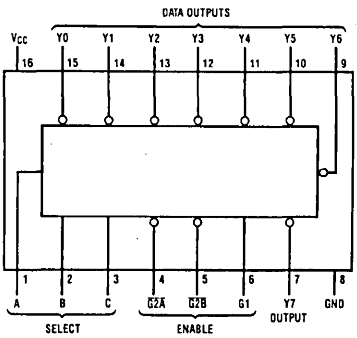
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



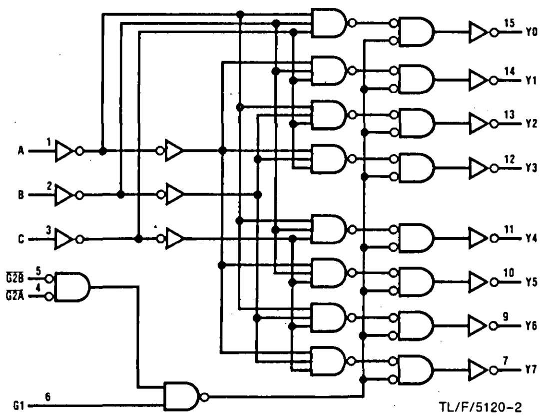
TOP VIEW

TL/F/5120-1

MM54HC138/MM74HC138

54HC138 (J) 74HC138 (J,N)

Logic Diagram



TL/F/5120-2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2}$ = G2A + G2B

H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, Binary Select to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, G1 to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		23	30	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		18	25	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay Binary Select to any Output Low to High		2.0V 4.5V 6.0V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}	Maximum Propagation Delay Binary Select to any Output High to Low		2.0V 4.5V 6.0V	100 20 17	200 40 34	252 40 43	298 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1 to any Output		2.0V 4.5V 6.0V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V 4.5V 6.0V	82 28 22	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V 4.5V 6.0V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	μF
C_{PD}	Power Dissipation Capacitance	(Note 5)		75				μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC139/MM74HC139 Dual 2-To-4 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC139/MM74HC139 contain two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1, and B1 or A2, and B2) cause one of the four normally high outputs to go low.

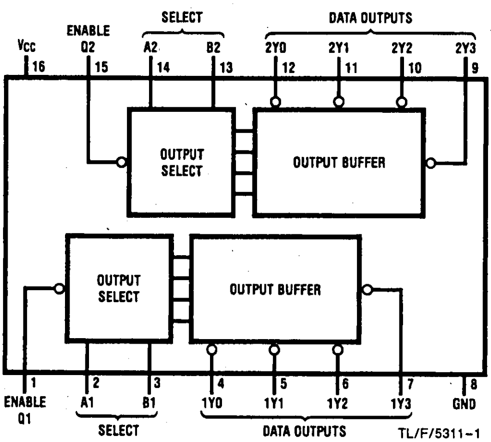
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally as well as pin equivalent to the 54LS139/74LS139. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delays —
  Select to outputs (4 delays): 18 ns
  Select to output (5 delays): 28 ns
  Enable to output: 20 ns
- Low power: 40 μW quiescent supply power
- Fanout of 10 LS-TTL devices
- Input current maximum 1 μA, typical 10 pA

Connection Diagram

Dual-In-Line



TL/F/5311-1

MM54HC139/MM74HC139

54HC139 (J) 74HC139 (J,N)

Truth Table

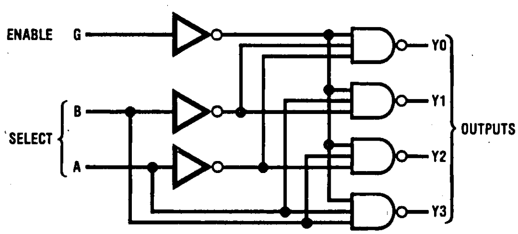
'HC139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HC139/MM74HC139



TL/F/5311-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 4 levels of delay		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 5 levels of delay		28	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to any Output		19	30	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 4 levels of delay		2.0V	110	175	219	254	ns
			4.5V	22	35	44	51	ns
			6.0V	18	30	38	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 5 levels of delay		2.0V	165	220	275	320	ns
			4.5V	33	44	55	64	ns
			6.0V	28	38	47	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to any Output		2.0V	115	175	219	254	ns
			4.5V	23	35	44	51	ns
			6.0V	19	30	38	44	ns
t_{TLH}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	μF
C_{PD}	Power Dissipation Capacitance (Note 5)	(Note 5)		75				μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC147/MM74HC147 10-to-4 Line Priority Encoder

General Description

This high speed 10-to-4 Line Priority Encoder utilizes micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, giving it a fanout of 10 LS-TTL loads.

The MM54HC147/MM74HC147 features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.

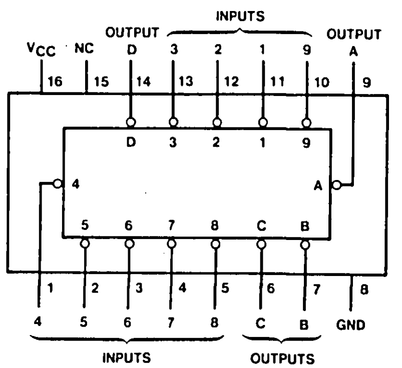
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent power consumption: 40 μW maximum at 25°C
- High speed: 31 ns propagation delay (typical)
- Very low input current: 10^{-5} μA typical
- Wide supply range: 2V to 6V

Connection Diagram

Dual-In-Line Package



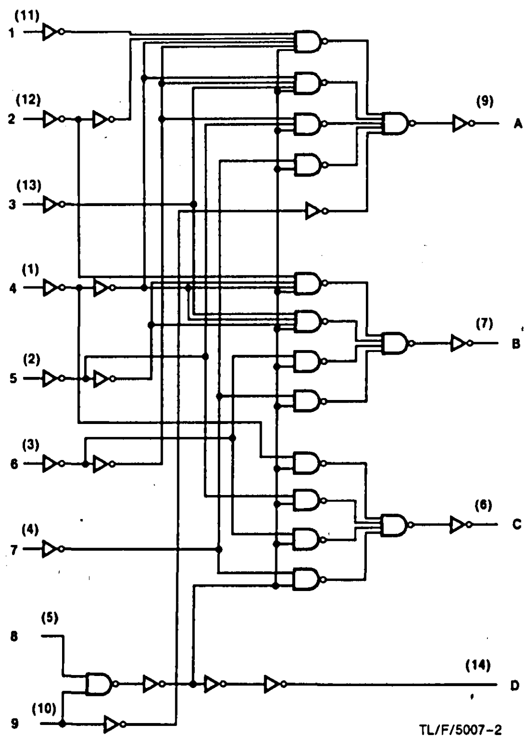
TOP VIEW

TL/F/5007-1

MM54HC147/MM74HC147

54HC147 (J) 74HC147 (J,N)

Logic Diagram



TL/F/5007-2

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.7	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		31	38	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	181 36 31	220 44 37	275 55 47	319 64 54	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		180				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC149/MM74HC149 8 Line to 8 Line Priority Encoder

General Description

This priority encoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. It is the logical combination of a '148 8-3 line priority encoder driving a '138 3-8 line decoder. Only one request output can be low at a time. The output that is low is dependent on the highest priority request that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, RQP, which goes low when any $\overline{RQP}$ is active.

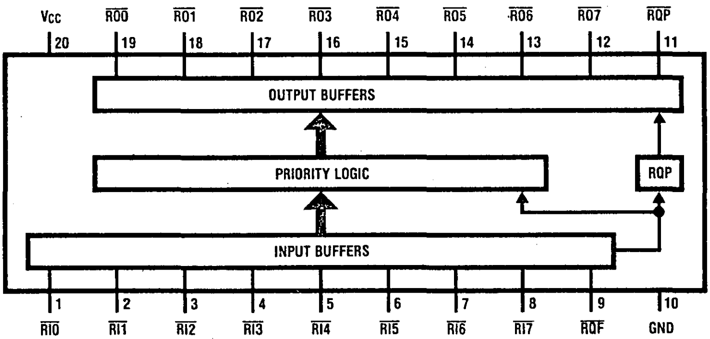
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

Features

- Propagation delay: 15 ns typical
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA max (74HC series)
- Wide input noise immunity

Connection Diagram

Dual-In-Line Package



MM54HC149/MM74HC149

54HC149 (J) 74HC149 (J,N)

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay RIn to a Different Output		23	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RQE}$ to Any Output		16	28	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay RIn to ROn (same output)		22	30	ns

AC Electrical Characteristics

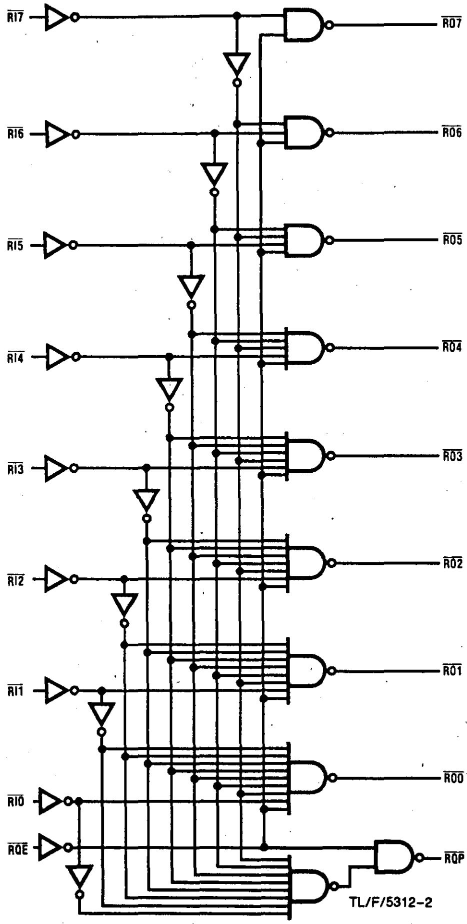
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay RIn to Same ROn		2.0V 4.5V 6.0V	120 22 20	175 35 30	218 44 38	260 53 45	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay RIn to Different ROn Output		2.0V 4.5V 6.0V		160 32 27	200 40 34	290 48 40	ns ns ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay $\overline{RQE}$ to Any Output		2.0V 4.5V 6.0V	70 22 18	155 31 26	190 39 33	230 46 39	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance Note 5			70				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Simplified Logic Diagram



TL/F/5312-2

National Semiconductor

microCMOS

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

General Description

This high speed DIGITAL MULTIPLEXER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family.

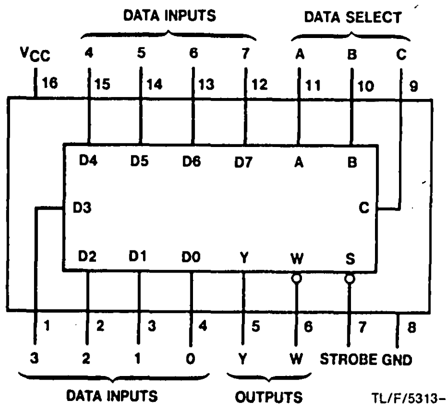
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum

Connection Diagram

Dual-In-Line



MM54HC151/MM74HC151

54HC151 (J) 74HC151 (J,N)

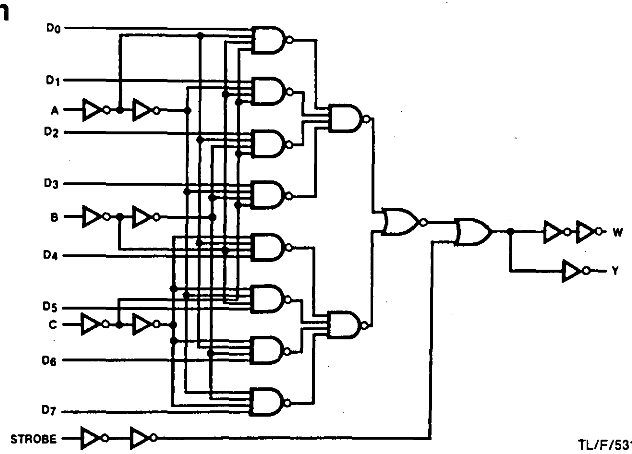
Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1...D7 = the level of the respective D input

Logic Diagram



TL/F/5313-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		24	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		16	21	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V 4.5V 6.0V	90 31 26	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		2.0V 4.5V 6.0V	95 32 27	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to Y		2.0V 4.5V 6.0V	70 27 23	195 39 33	244 49 41	283 57 48	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		2.0V 4.5V 6.0V	75 29 25	185 37 32	231 46 40	268 54 46	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		2.0V 4.5V 6.0V	50 21 18	140 28 24	175 35 30	203 41 35	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		2.0V 4.5V 6.0V	45 20 17	127 25 22	159 32 28	185 37 32	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC153/MM74HC153 Dual 4-Input Multiplexer

General Description

This 4-to-1 line multiplexer utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads. Information on the data inputs of each multiplexer is selected by the address on the A and B inputs, and is presented on the Y outputs. Each multiplexer possesses a strobe input which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

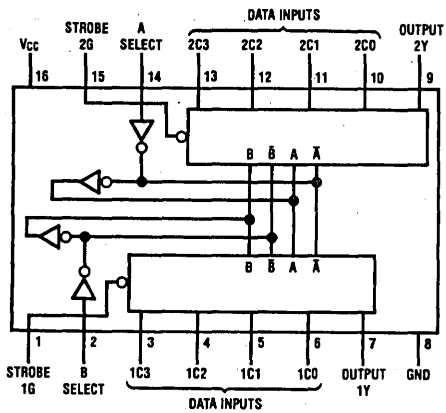
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5107-1

TOP VIEW
MM54HC153/MM74HC153

54HC153 (J) 74HC153 (J,N)

Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = don't care.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.3	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		26	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Data to Y		20	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		8	15	ns

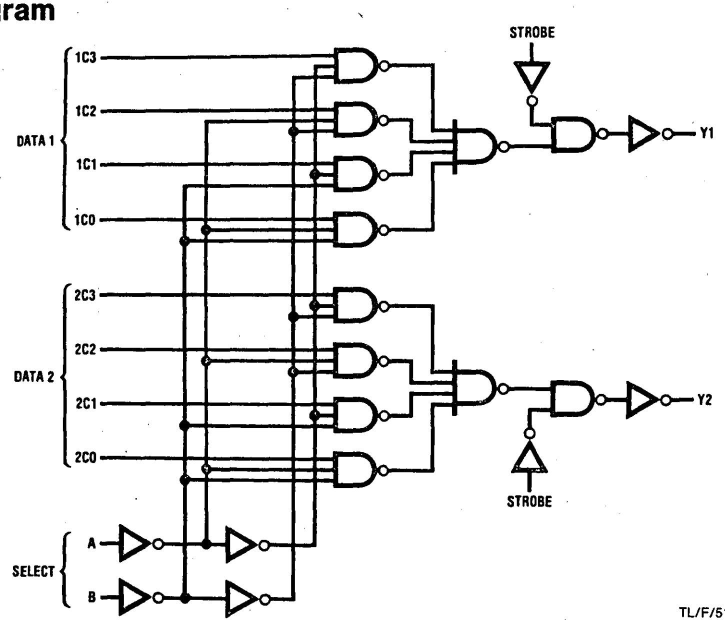
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V 4.5V 6.0V	131 29 25	158 35 30	198 44 38	237 52 45	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Data to Y		2.0V 4.5V 6.0V	99 22 19	126 28 23	158 35 29	189 42 35	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		2.0V 4.5V 6.0V	50 12 10	86 19 16	108 24 20	129 29 24	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)(per package) Outputs Enabled Outputs Disabled		 90 25				 pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5107-2

National Semiconductor

microCMOS

MM54HC154/MM74HC154 4-to-16 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses high noise immunity, and low power consumption of CMOS with speeds similar to low power Schottky TTL circuits.

The MM54HC154/MM74HC154 have 4 binary select inputs (A, B, C, and D). If the device is enabled these inputs determine which one of the 16 normally high outputs will go low. Two active low enables ($\overline{G1}$ and $\overline{G2}$) are provided to ease cascading of decoders with little or no external logic.

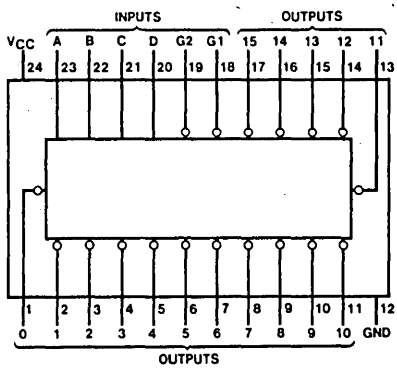
Each output can drive 10 low power Schottky TTL equivalent loads, and is functionally and pin equivalent to the 54LS154/74LS154. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 21 ns
- Power supply quiescent current: 80 μA (74HC)
- Wide power supply voltage range: 2–6V
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5122-1

TOP VIEW

MM54HC154/MM74HC154

54HC154 (J) 74HC154 (J,N)

Truth Table

Inputs						Low Output*
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

*All others high

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL}, $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$, $\overline{G2}$ or A, B, C, D		21	32	ns

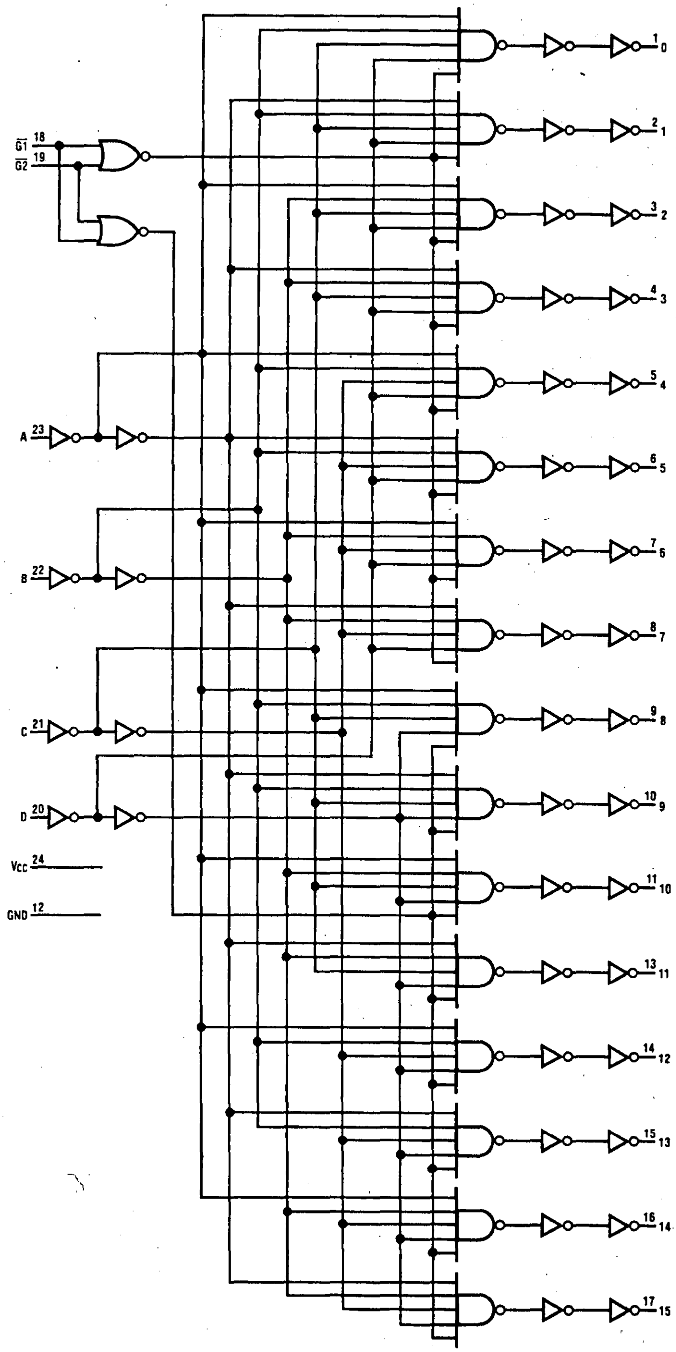
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$ or $\overline{G2}$ or A, B, C, D		2.0V	63	160	190	220	ns
			4.5V	24	36	42	46	ns
			6.0V	20	30	35	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5122-2

National Semiconductor

microCMOS

MM54HC157/MM74HC157 Quad 2-Input Multiplexer MM54HC158/MM74HC158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed QUAD 2-to-1 LINE DATA SELECTOR/MULTIPLEXERS utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HC157/MM74HC157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HC158/MM74HC158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

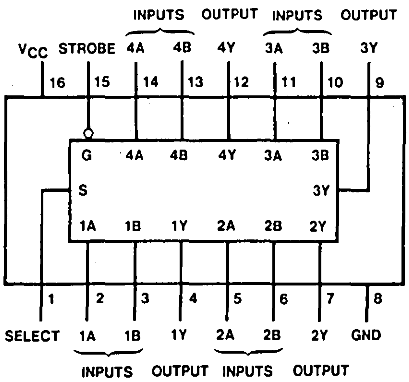
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μA maximum

Connection Diagrams

Dual-In-Line Package

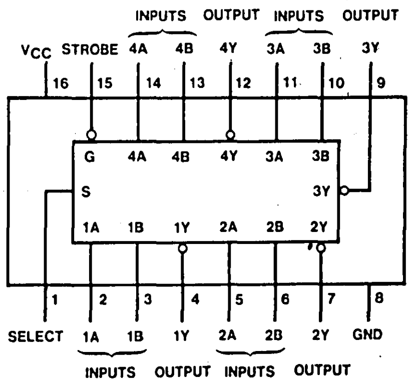


TOP VIEW
MM54HC157/MM74HC157

TL/F/5314-1

54HC157 (J) 74HC157 (J,N)

Dual-In-Line Package



TOP VIEW
MM54HC158/MM74HC158

TL/F/5314-2

54HC158 (J) 74HC158 (J,N)

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HC157	HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

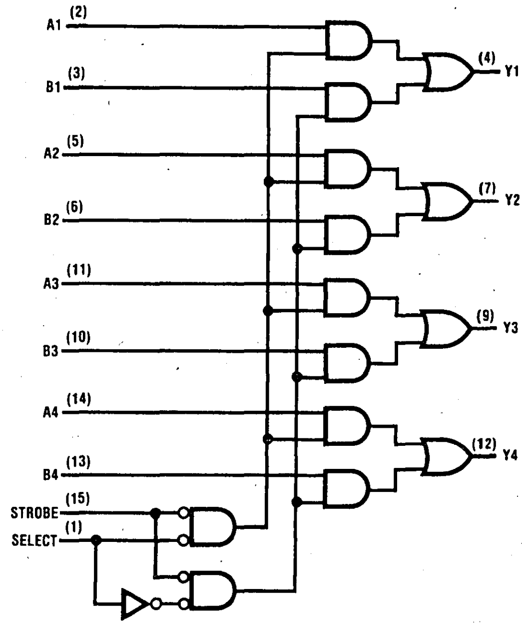
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		2.0V	58	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)							pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

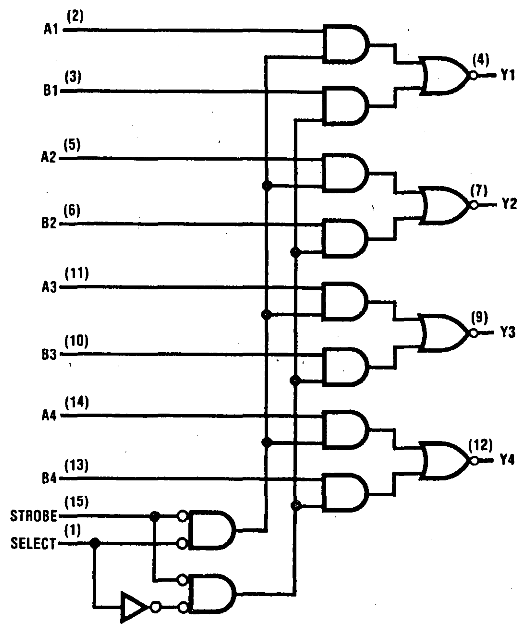
Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams



TL/F/5314-3

'HC157



TL/F/5314-4

'HC158

National Semiconductor

microCMOS

MM54HC160/MM74HC160 Synchronous Decade Counter with Asynchronous Clear MM54HC161/MM74HC161 Synchronous Binary Counter with Asynchronous Clear MM54HC162/MM74HC162 Synchronous Decade Counter with Synchronous Clear MM54HC163/MM74HC163 Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HC160/MM74HC160, MM54HC161/MM74HC161, MM54HC162/MM74HC162, and MM54HC163/MM74HC163 synchronous presettable counters utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HC160 and the 'HC162 are 4 bit decade counters, and the 'HC161 and the 'HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HC162/MM74HC162 and MM54HC163/MM74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HC160/MM74HC160 and MM54HC161/MM74HC161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

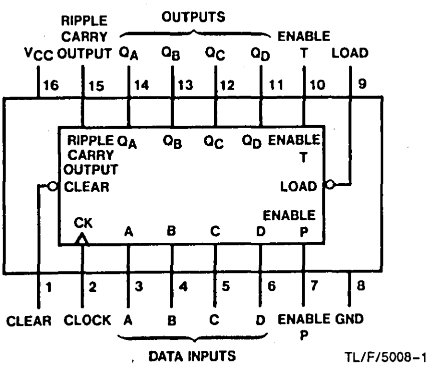
Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay; clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V

Connection Diagram



TL/F/5008-1

54HC160 (J) 74HC160 (J,N)
54HC161 (J) 74HC161 (J,N)
54HC162 (J) 74HC162 (J,N)
54HC163 (J) 74HC163 (J,N)

Truth Tables

'HC160/HC161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to RC		30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		27	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 40 45	5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		2.0V 4.5V 6.0V	100 32 28	215 43 37	271 54 46	320 64 54	ns ns ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		2.0V 4.5V 6.0V	88 18 15	175 35 30	220 44 37	260 52 44	ns ns ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		2.0V 4.5V 6.0V	95 30 26	205 41 35	258 52 44	305 61 52	ns ns ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V 4.5V 6.0V	85 17 14	170 34 29	214 43 36	253 51 43	ns ns ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		2.0V 4.5V 6.0V	90 28 24	195 39 33	246 49 42	291 58 49	ns ns ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		2.0V 4.5V 6.0V	80 16 14	160 32 27	202 40 34	238 48 41	ns ns ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		2.0V 4.5V 6.0V	100 32 28	220 44 37	277 55 47	328 66 55	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V		125 25 21	158 32 27	186 37 32	ns ns ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock		2.0V 4.5V 6.0V		150 30 26	190 38 32	225 45 38	ns ns ns
t_H	Minimum Hold Time Data from Clock		2.0V 4.5V 6.0V		50 10 9	63 13 11	75 15 13	ns ns ns
t_W	Minimum Pulse Width Clock, Clear, or Load		2.0V 4.5V 6.0V		80 16 14	100 20 17	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	40 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns

AC Electrical Characteristics (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

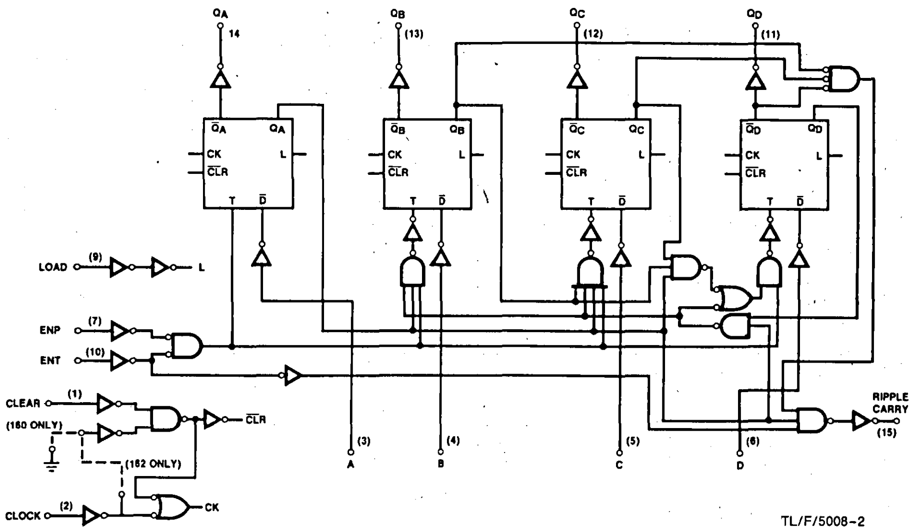
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

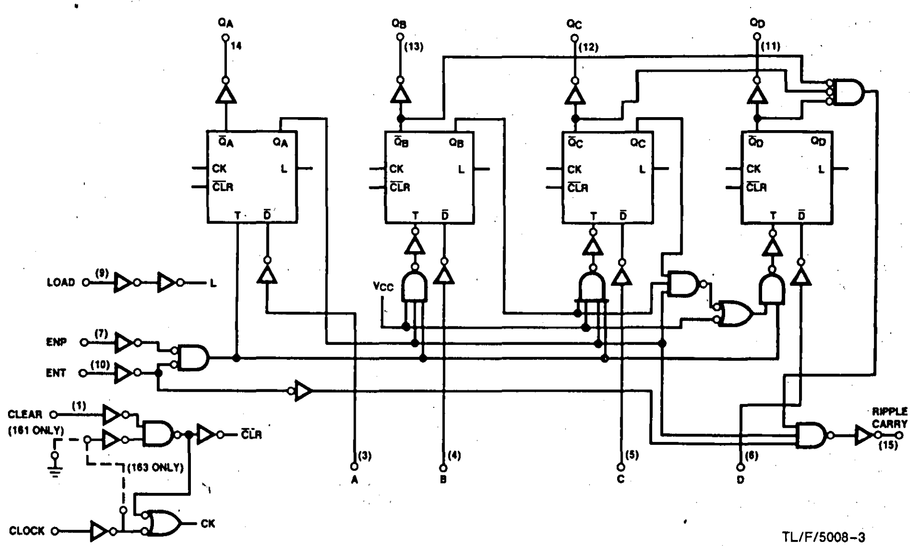
Logic Diagrams

MM54HC160/MM74HC160 or MM54HC162/MM74HC162



TL/F/5008-2

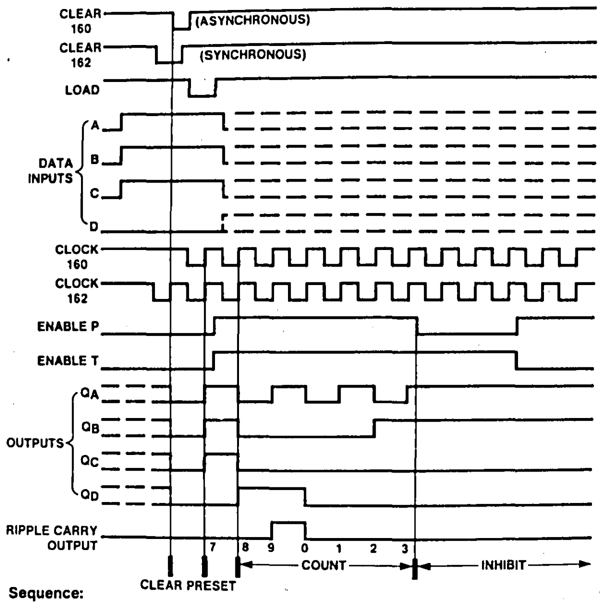
MM54HC161/MM74HC161 or MM54HC163/MM74HC163



TL/F/5008-3

Logic Waveforms

160, 162 Synchronous Decade Counters Typical Clear, Preset, Count and Inhibit Sequences

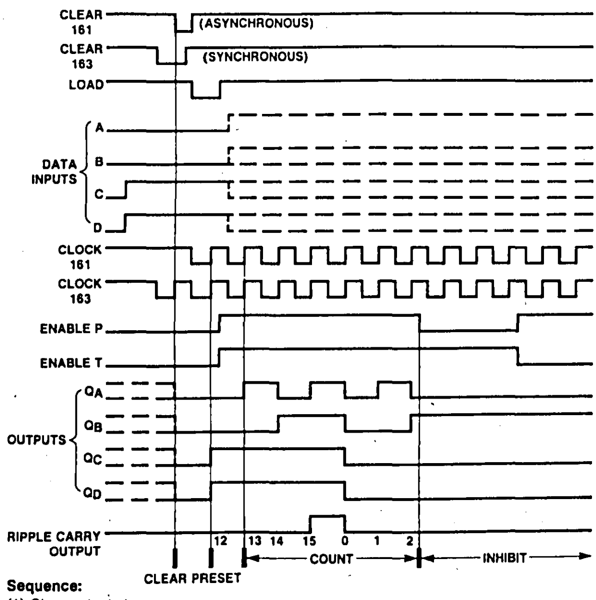


TL/F/5008-4

Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161, 163 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008-5

Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

National Semiconductor

microCMOS

MM54HC164/MM74HC164 8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HC164/MM74HC164 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-BIT SHIFT REGISTER has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-BIT REGISTER during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

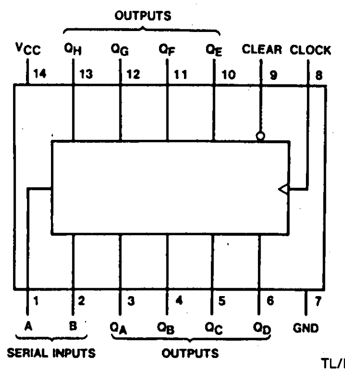
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5315-1

MM54HC164/MM74HC164

54HC164 (J) 74HC164 (J,N)

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

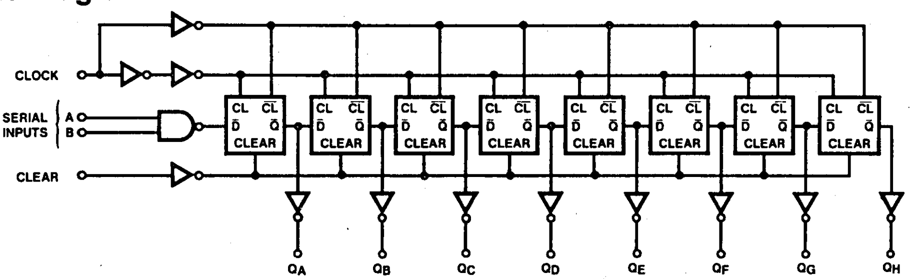
X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



TL/F/5315-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		23	35	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	0	ns
t_S	Minimum Set Up Time Data to Clock		12	20	ns
t_H	Minimum Hold Time Clock to Data		1	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V 4.5V 6.0V	115 13 20	175 35 30	218 44 38	254 51 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		2.0V 4.5V 6.0V	140 28 24	205 41 35	256 51 44	297 59 51	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	−7 −3 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V	25 14 12	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V	−2 0 1	5 5 5	5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width Clear or Clock		2.0V 4.5V 6.0V	22 11 10	80 16 14	100 20 18	120 24 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V		75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	5.0V	150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC165/MM74HC165
Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM54HC165/MM74HC165 high speed PARALLEL-IN/ SERIAL-OUT SHIFT REGISTER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

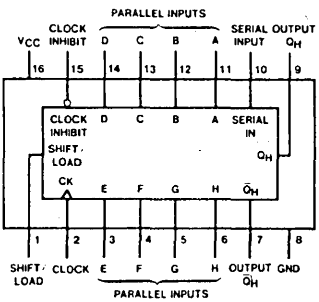
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5316–1

MM54HC165/MM74HC165

54HC165 (J) 74HC165 (J,N)

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND V_{CC}=2–6V	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$ V_{CC}=2–6V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_S	Minimum Set Up Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Set Up Time Shift/Load to Clock		11	20	ns
t_S	Minimum Set Up Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

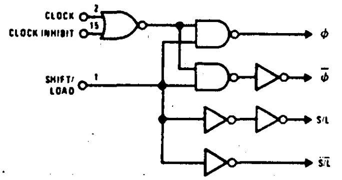
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		2.0V 4.5V 6.0V	70 21 18	150 30 26	189 38 33	225 45 39	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/ Parallel Load to Q_H		2.0V 4.5V 6.0V	70 21 18	175 35 30	220 44 37	260 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V 4.5V 6.0V	70 21 18	150 30 26	189 38 33	225 45 39	ns ns ns
t_S	Minimum Set Up Time Serial Input to Clock, or Parallel Data to Shift/Load		2.0V 4.5V 6.0V	35 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time Shift/Load to Clock		2.0V 4.5V 6.0V	38 12 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time Clock Inhibit to Clock		2.0V 4.5V 6.0V	35 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Clock		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 9 8	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Block Diagram



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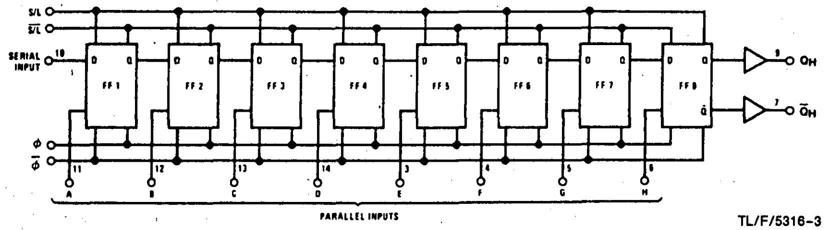


TL/F/5316-3

National Semiconductor

microCMOS

MM54HC166/MM74HC166 8-Bit Serial or Parallel Input/Serial Output Shift Register with Reset

General Description

These shift registers utilize microCMOS technology, 3.5 micron silicon gate P-well CMOS. The MM54HC166/MM74HC166 are 8-bit shift registers with an output from the last stage. Data may be loaded into the register in either parallel or serial form.

When the shift/load input is low, the data is loaded asynchronously in parallel. When the shift/load input is high, the data is loaded serially on the rising edge of either Clock 1 or Clock 2 (see the Function Table). Reset is asynchronous and active low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Wide power supply range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA max (74HC series)
- Fanout of 10 LS-TTL loads

Function Table and Connection Diagram

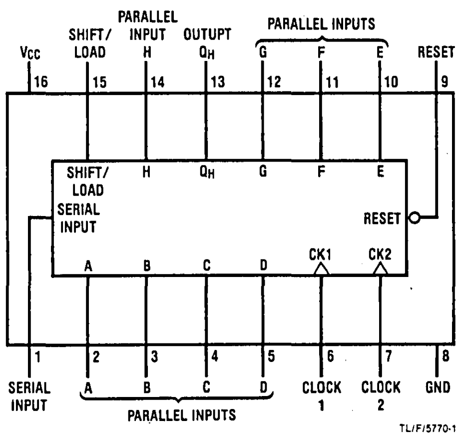
Inputs						Internal Stages		Output	Operation
Reset	Shift/ Load	Clock 1	Clock 2	Serial Input	A-H	Q_A	Q_B	Q_H	
H	L	X	X	X	a…h	a	b	h	Asynchronous Parallel Load
H	H	↑	L	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 1
H	H	↑	L	H	X	H	Q_{An}	Q_{Gn}	
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 2
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}	
H	H	X	H	X	X	no change			Inhibited Clock
H	H	H	X	X	X				
H	H	L	L	X	X	no change			No Clock
L	X	X	X	X	X	L	L	L	Asynchronous Reset

X = don't care

↑ = transition from low to high

Q_{An}-Q_{Gn} = data shifted from the preceding stage

Dual-In-Line Package



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Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40°C to 85°C Guaranteed Limits	54HC T_A=−55°C to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10%, the worst-case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V, respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage, so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or Q_H		15	25	ns
t_{PHL}, t_{PLH}	Maximm Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Reset to Q_H				ns
t_S	Minimum Set-Up Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Set-Up Time Shift/Load to Clock		11	20	ns
t_S	Minimum Set-Up Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40°C$ to $85°C$	54HC $T_A=-55°C$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or Q_H		2.0V 4.5V 6.0V	70 21 18	150 30 26	189 38 33	225 45 39	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		2.0V 4.5V 6.0V	70 21 18	150 30 26	189 38 33	225 45 39	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V 4.5V 6.0V	70 21 18	150 30 26	189 38 33	225 45 39	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q_H		2.0V 4.5V 6.0V	88 23 20	175 35 30	220 44 38	260 52 45	ns ns ns
t_S	Minimum Set-Up Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V 4.5V 6.0V	35 11 9	100 20 17	125 25 21	150 30 25	ns ns ns

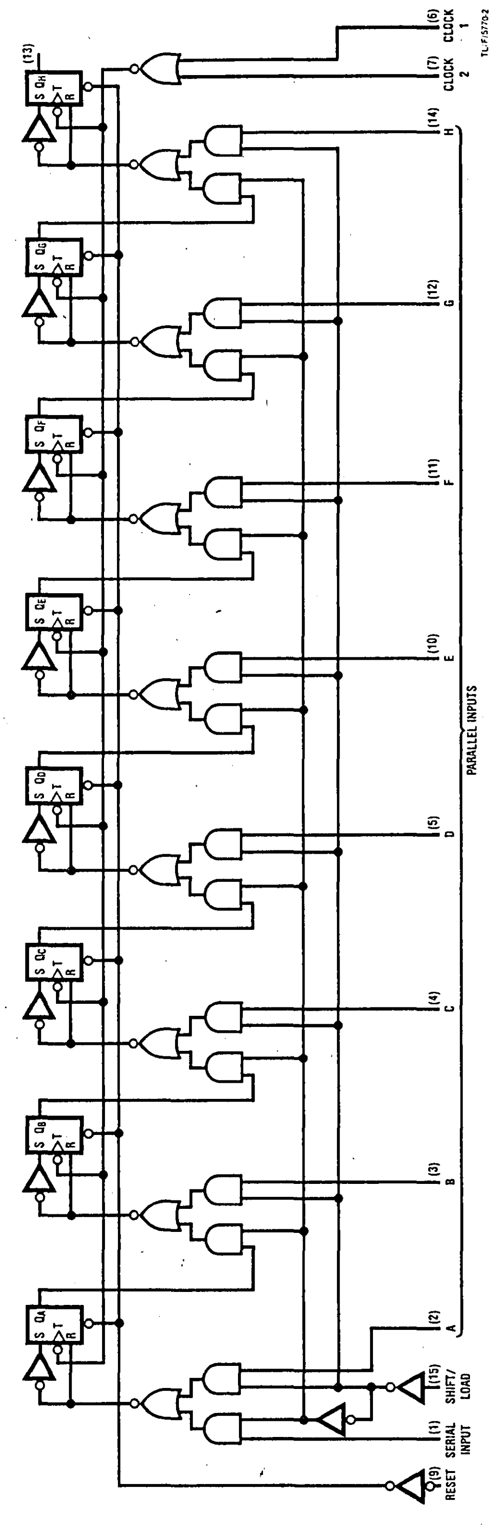
AC Electrical Characteristics (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	74HC $T_A = -40°C$ to 85°C Guaranteed Limits	54HC $T_A = -55°C$ to 125°C Guaranteed Limits	Units
t_S	Minimum Set-Up Time Shift/Load to Clock		2.0V 4.5V 6.0V	38 12 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set-Up Time Clock Inhibit to Clock		2.0V 4.5V 6.0V	35 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Clock		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 9 8	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



National Semiconductor

PRELIMINARY

microCMOS

MM54HC169/MM74HC169 4-Bit Up/Down Synchronous Binary Counter

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power and high noise immunity of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits.

These counters are incremented or decremented on the rising edge of the CLK, clock, input if ENT and ENP are held low. The counters increment when the U/D input is at a logic "1", and will decrement when U/D is low. The ENT input is fed forward to enable the carry output. RCO, ripple carry output, once enabled, will produce a low level pulse while the count is 0 (down count mode) or when the count is all 1s (up mode).

These counters are presettable, that is, they may be loaded when LOAD is taken low and a rising edge appears on the CLK input.

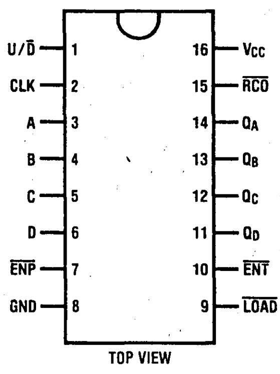
The MM54HC169/MM74HC169 are functional, speed and pin equivalent to the equivalent LS-TTL circuit. Its inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 2.0V to 6.0V
- High input noise immunity
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HC)

Connection Diagram

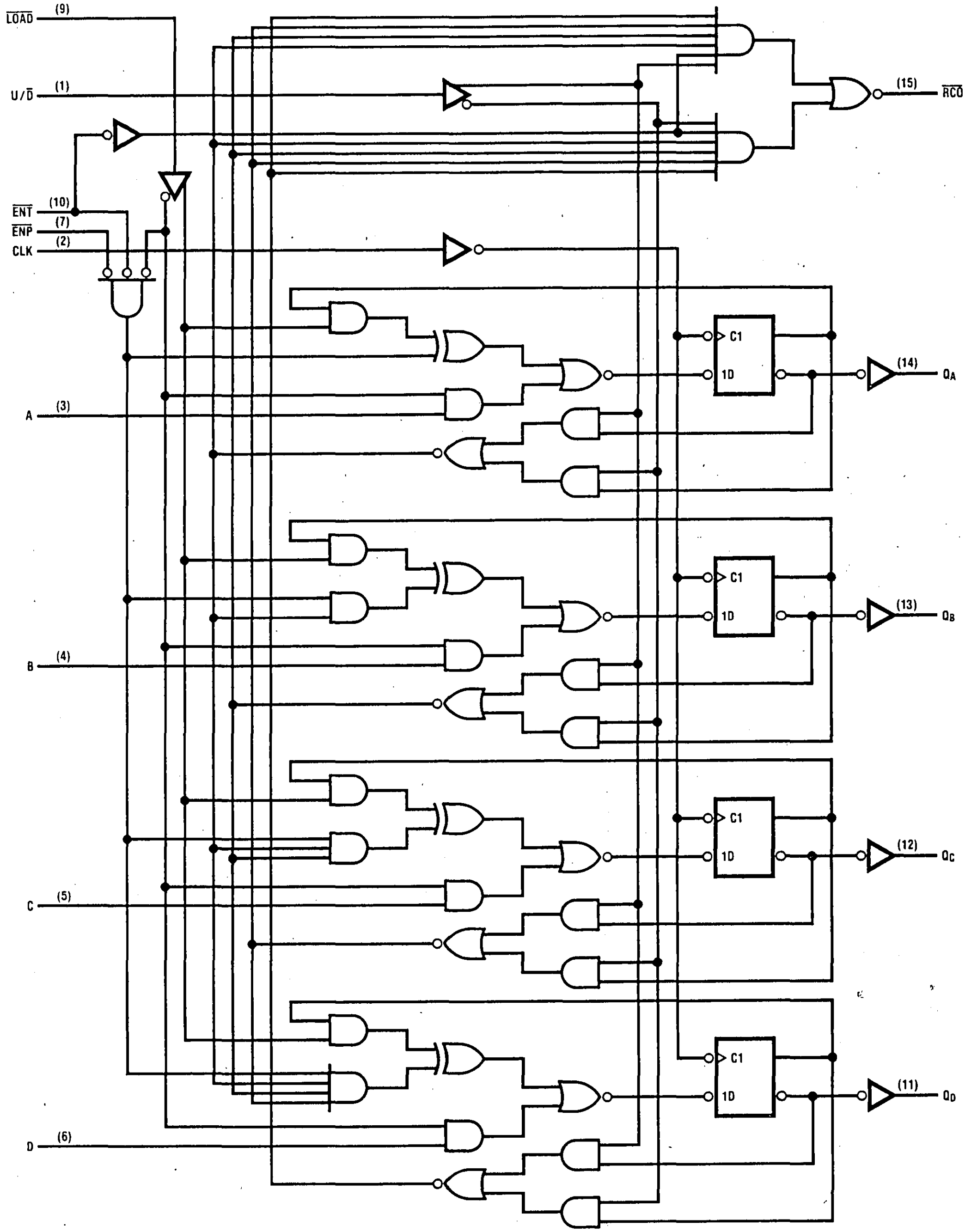
Dual-In-Line Package



TOP VIEW

TL/F/5771-1

Logic Diagram



TL/F/5771-2

National Semiconductor

microCMOS

MM54HC173/MM74HC173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54HC173/MM74HC173 is a high speed TRI-STATE QUAD D TYPE FLIP-FLOP that utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It possesses the low power consumption and high noise immunity of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device. The outputs are buffered, allowing this circuit to drive 15 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The TRI-STATE outputs allow the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Clearing is enabled by taking the CLEAR input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

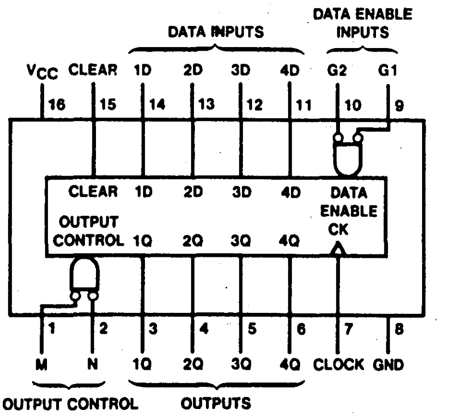
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating supply voltage range: 2–6V
- TRI-STATE outputs
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 6 mA minimum

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5317-1

MM54HC173/MM74HC173

54HC173 (J) 74HC173 (J,N)

Truth Table

Inputs					Output
Clear	Clock	Data Enable		Data	Output
		G1	G2	D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H
When either M or N (or both) is (are) high the output is disabled to the high-impedance state: however, sequential operation of the flip-flops is not affected.					

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V		0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	$V_{OUT}=V_{CC}$ or GND Enable=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay: Clock to Q			31	ns
t_{PHL}	Maximum Propagation Delay: Clear to Q		18	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	16	25	ns
t_S	Minimum Data Set Up Time			20	ns
t_S	Minimum Data Enable Set Up Time			20	ns
t_H	Minimum Data Hold Time			0	ns
t_H	Minimum Data Enable Hold Time			0	ns
t_W	Minimum Clock Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V 4.5V 6.0V	10 45 55	5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	80 110	175 225	220 280	262 338	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	23 28	35 45	44 56	53 68	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	21 26	30 38	38 48	45 57	ns ns
t_{PHL}	Maximum Propagation Delay from Clear to Q	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	70 100	150 200	189 252	224 298	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	20 25	30 40	38 50	45 60	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	17 22	26 34	32 43	38 51	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF $C_L=150$ pF $C_L=50$ pF $C_L=150$ pF $C_L=50$ pF $C_L=150$ pF	 2.0V 2.0V 4.5V 4.5V 6.0V 6.0V	 70 100 20 25 17 22	 150 200 30 40 26 34	 189 252 38 50 32 43	 224 298 45 60 38 51	 ns ns ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	70 20 17	150 30 26	189 38 32	224 45 38	ns ns ns
t_S	Minimum Data or Data Enable Set Up Time		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_{REM}	Minimum Removal Time		2.0V 4.5V 6.0V		90 18 15	112 22 19	135 26 22	ns ns ns
t_H	Minimum Data or Data Enable Hold Time		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Clear or Clock Pulse Width		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 17	120 24 20	ns ns ns

AC Electrical Characteristics (Continued)

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	5	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance	(per flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

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MM54HC174/MM74HC174 Hex D Flip-Flops With Clear

General Description

These edge triggered flip-flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

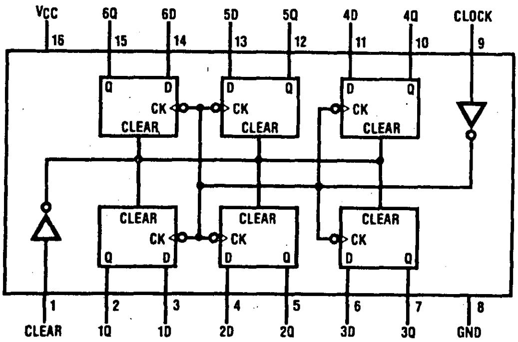
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC174/MM74HC174 is functionally as well as pin compatible to the 54LS174/74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74HC series)
- Output drive: 10 LSTTL loads

Connection Diagram

Dual-In-Line Package

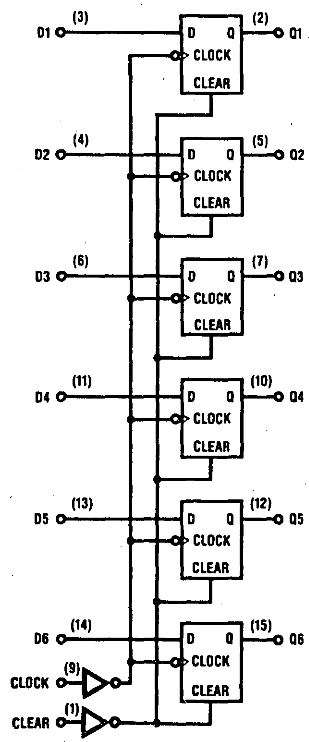


TL/F/5318–1

TOP VIEW
MM54HC174/MM74HC174

54HC174 (J)   74HC174 (J,N)

Logic Diagram



TL/F/5318–2

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock or Clear to Output		16	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_S	Minimum Set Up Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		0	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock or Clear to Output		2.0V 4.5V 6.0V	55 18 16	165 33 28	206 41 35	248 49 42	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	1 1 1	5 5 5	5 5 5	5 5 5	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V	42 12 10	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V	1 1 1	5 5 5	5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width Clock or Clear		2.0V 4.5V 6.0V	35 10 8	80 16 14	106 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		136				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC175/MM74HC175
Quad D-Type Flip-Flop With Clear

General Description

This high speed D-TYPE FLIP-FLOP with complementary outputs utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Information at the D inputs of the MM54HC175/MM74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four Q outputs to a logical "1."

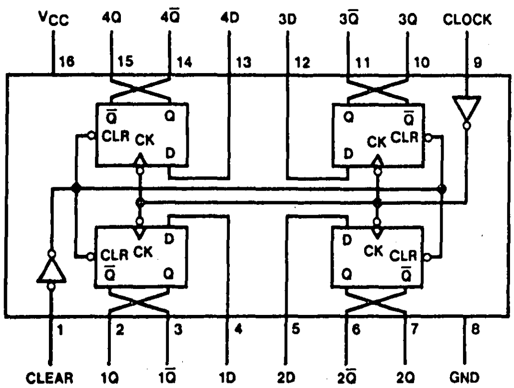
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum (74HC)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5319-1

MM54HC175/MM74HC175

54HC175 (J) 74HC175 (J,N)

Truth Table
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		60	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		13	21	ns
t_{REC}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set Up Time, Data to Clock			20	ns
t_H	Minimum Hold Time, Data from Clock			0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics

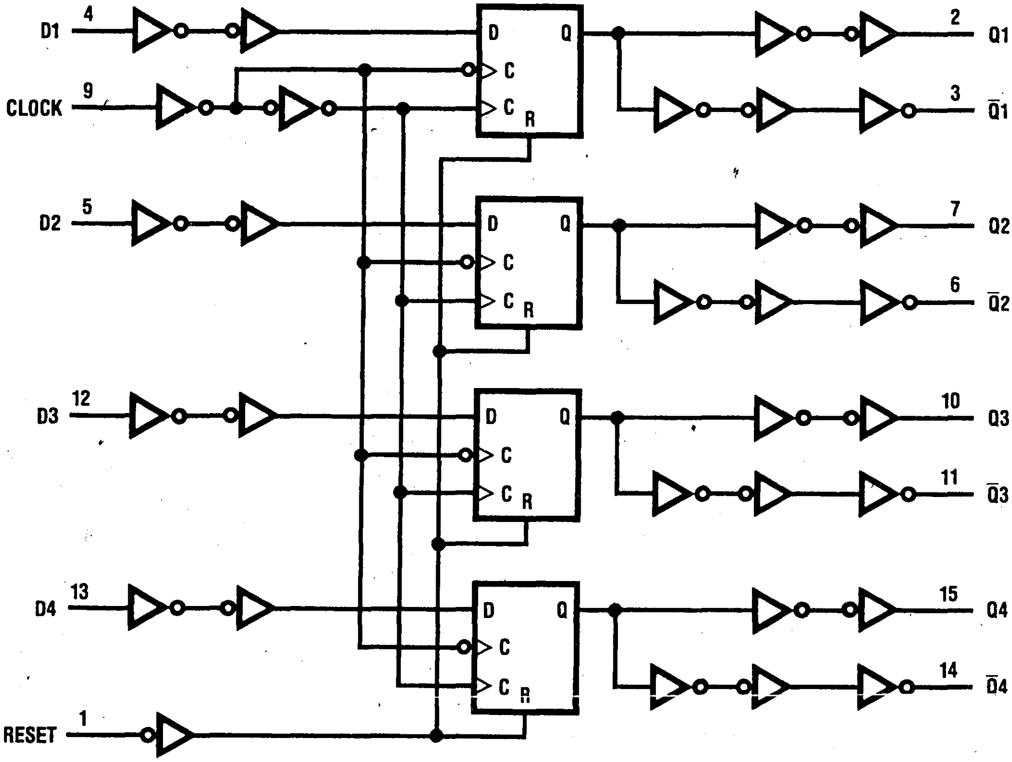
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	12 60 70	6 30 35	5 24 28	4 20 24	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	80 15 13	150 30 26	190 38 32	225 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	64 14 12	125 25 21	158 32 27	186 37 32	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Data from Clock		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clear or Clock		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 17	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 9 8	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5319-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC181/MM74HC181 Arithmetic Logic Units/Function Generators

General Description

These arithmetic logic units (ALU)/function generators utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The MM54HC181/MM74HC181 are arithmetic logic unit (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the MM54HC182 or MM74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading HC182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the MM54HC182/MM74HC182.

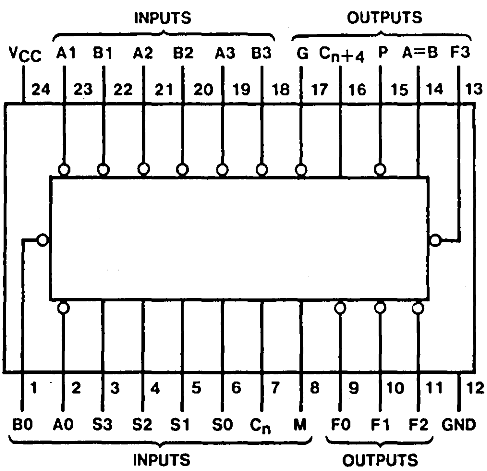
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features

- Full look-ahead for high-speed operations on long words
- Arithmetic operating modes:
  Addition
  Subtraction
  Shift operand a one position magnitude comparison
  Plus Twelve other arithmetic operations
- Logic function modes:
  Exclusive-OR
  Comparator
  AND, NAND, OR, NOR
  Plus ten other logic operations
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



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TOP VIEW

MM54HC181/MM74HC181

54HC181 (J)   74HC181 (J,N)

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Outputs
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to produce A—B.

The 181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+_4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control inpu (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The MM54HC181/MM74HC181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

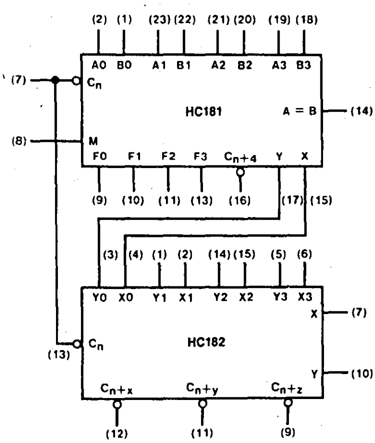

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Figure 1

Table 1

Selection				Active High Data		
				M=H Logic Functions	M=L; Arithmetic Operations	
S3	S2	S1	S0		C_n=H (no carry)	C_n=L (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A Plus 1
L	L	L	H	F=$\overline{A+B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	F=$\overline{A}$B	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Compl)	F=Zero
L	H	L	L	F=$\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	F=$\overline{B}$	F=(A + B) Plus A$\overline{B}$	F=(A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F=A ⊕ B	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$ + B	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\overline{B}$) Plus AB	F=(A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A + $\overline{B}$	F=(A + B) Plus A	F=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + $\overline{B}$) Plus A	F=(A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

*Each bit is shifted to the next more significant position.

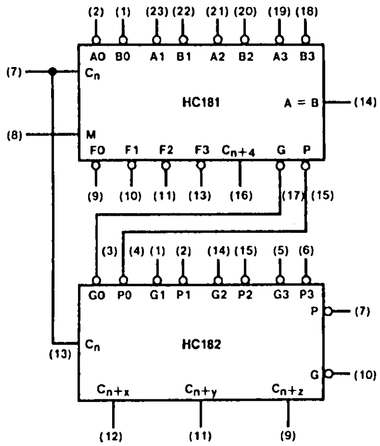

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Figure 2

Table 2

Selection				Active Low Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A + B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$ Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage (any output except A=B)	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
I_{LKG}	Maximum Leakage Open Drain Output Current (A=B Output)	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}	6.0V		0.5	5.0	10	μA
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to C_n+4		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_N+4	M=0V, S0=S3=V_{CC} S1=S0=0V ($\overline{\text{Sum}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_N+4	M=0V,S0=S3=0V S1=S2=V_{CC} ($\overline{\text{Diff.}}$ mode)	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to any F	M=0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff.}}$ mode)	13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M=0V, S0= S3=V_{CC} S1=S2=0V ($\overline{\text{Sum}}$ mode)	14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M=0V, S0= S3=V_{CC} S1=S2=0V ($\overline{\text{Sum}}$ mode)	17	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	17	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M=0V, S0= S3=V_{CC} S1=S2=0V ($\overline{\text{Sum}}$ mode)	28	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	32	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M=V_{CC} (logic mode)	32	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to A=B	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	36	50	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to C_n+4		2.0V 4.5V 6.0V	55 17 14	120 24 20	160 30 25	200 36 30	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_n+4	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	110 35 30	250 50 43	325 63 53	375 75 65	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	120 40 35	280 56 48	350 70 60	420 84 72	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	55 17 14	120 24 20	160 30 25	200 36 30	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M = 0V, S0 = S3 = V_{CC}, S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	55 17 14	120 24 20	160 30 25	200 36 30	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	70 20 17	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	70 20 17	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	70 20 17	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	115 35 30	240 48 41	300 60 51	360 72 61	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	120 40 34	275 55 47	344 69 59	344 83 69	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M = V_{CC} (logic mode)	2.0V 4.5V 6.0V	120 40 34	275 55 47	344 60 59	344 83 69	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	120 40 35	280 56 48	350 70 60	420 84 72	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = V_{CC}, S0 = S3 = 0 V

Parameter	Input Under Test	Other Input Same Bit: Apply V_{CC}	Other Input Same Bit: Apply GND	Other Data Inputs: Apply V_{CC}	Other Data Inputs: Apply GND	Output Under Test	Output Waveform
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase

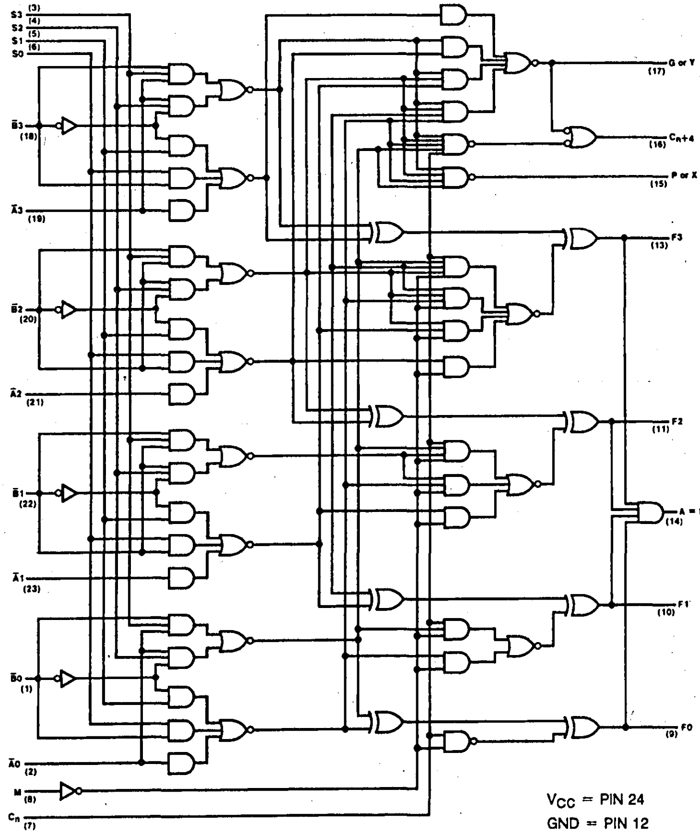
$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = V_{CC} S1 = S2 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit: Apply V_{CC}	Other Input Same Bit: Apply GND	Other Data Inputs: Apply V_{CC}	Other Data Inputs: Apply GND	Output Under Test	Output Waveform
t_{PHL}, t_{PLH}	A_I	B_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

$\overline{\text{Diff}}$ Mode Test Table
Function Inputs: S1 = S2 = V_{CC}, S0 = S3 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit: Apply V_{CC}	Other Input Same Bit: Apply GND	Other Data Inputs: Apply V_{CC}	Other Data Inputs: Apply GND	Output Under Test	Output Waveform
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	A=B	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	A=B	Out-of-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



V_{CC} = PIN 24
GND = PIN 12

TL/F/5320-4

National Semiconductor

PRELIMINARY

microCMOS

MM54HC182/MM74HC182 Look-Ahead Carry Generator

General Description

The MM54HC182/MM74HC182 is a high speed LOOK-AHEAD CARRY GENERATOR utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These circuits are capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

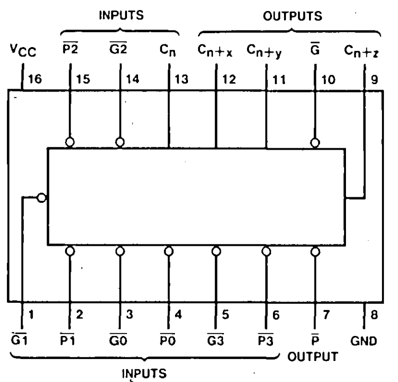
Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

Features

- TTL pinout compatible
- Typical propagation delay: 18 ns (Clock to Q)
- Wide Operating Supply Voltage Range: 2–6V
- Low Input Current: < 1 μA
- Low Quiescent Supply Current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL Loads

Connection Diagram

Dual-In-Line Package

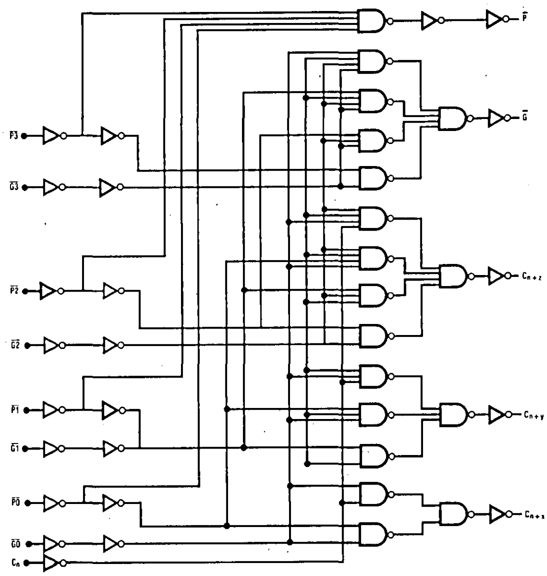


TOP VIEW TL/F/5321-1

MM54HC182/MM74HC182

54HC182 (J) 74HC182 (J,N)

Logic Diagram



TL/F/5321-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T=25°C Typ	T=25°C Guaranteed Limits	74HC T=−40 to 85°C Guaranteed Limits	54HC T=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, $t_r=t_f$=6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn to P		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Cn to any output		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn or Gn to any output		23	35	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T = 25°C Typ	T = 25°C Guaranteed Limits	74HC T = −40 to 85°C Guaranteed Limits	54HC T = −55 to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn to P		2.0V 4.5V 6.0V	45 18 15	112 28 22	140 35 27	162 40 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cn to any output		2.0V 4.5V 6.0V	50 20 16	125 30 24	156 37 30	182 44 35	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn or Gn to any output		2.0V 4.5V 6.0V	62 25 22	155 37 33	194 46 42	225 54 48	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Equations

$C_{n+x} = G0 + P0\ C_n$

$C_{n+y} = G1 + P1\ G0 + P1\ P0\ C_n$

$C_{n+z} = G2 + P2\ G1 + P2\ P1\ P0\ C_n$

$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$

$\overline{P} = \overline{P3\ P2\ P1\ P0}$

or

$\overline{C}_{n+x} = \overline{Y0\ (X0 + C_n)}$

$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + C_n)]}$

$\overline{C}_{n+z} = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + C_n)]\}}$

$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$

$X = X3 + X2 + X1 + X0$

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$ (OUTPUT)
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$ (OUTPUT)
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x} (OUTPUT)
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+z} OUTPUT

$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z} (OUTPUT)
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FUNCTION TABLE FOR C_{n+y} OUTPUT

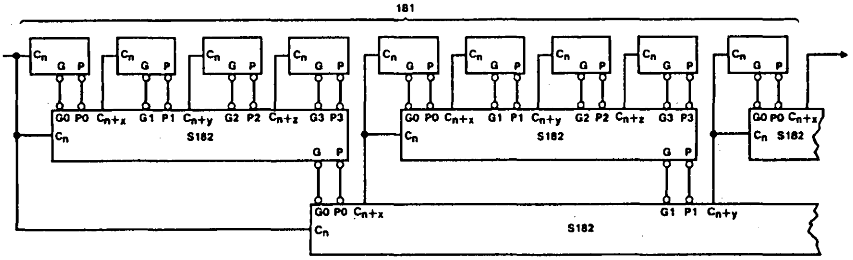
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y} (OUTPUT)
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

H = high level L = low level X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



TL/F/5321-3

A and B inputs, and F outputs of 181 are not shown.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC190/MM74HC190 Synchronous Decade Up/Down Counters with Mode Control MM54HC191/MM74HC191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL.

These circuits are synchronous, reversible, up/down counters. The MM54HC191/MM74HC191 are 4-bit binary counters and the MM54HC190/MM74HC190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

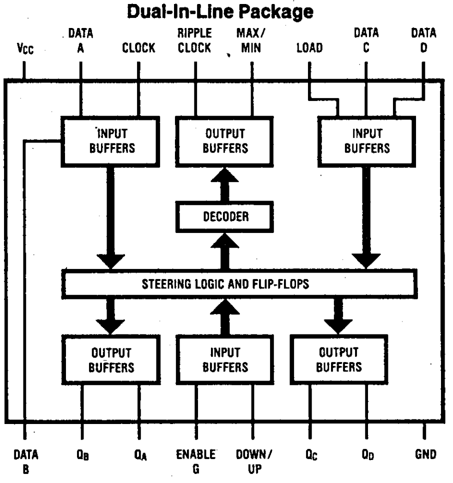
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Typical propagation delay
  Clock to output: 24 ns
- Typical operating frequency: 50 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5322

Load	Enable G	Down/ Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Asynchronous inputs Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency				40	25	MHz
t_{PLH}, t_{PHL}	Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30	50	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27	40	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Ripple Clock		16	24	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24	36	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Max/Min		30	50	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Ripple Clock		29	45	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Max/Min		22	33	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		22	33	ns
$t_{W(CLOCK)}$	Width of Clock, Clear or Load Input Pulse				10	20	ns
t_{SETUP}	Data Setup Time					20	ns
t_{HOLD}	Data Hold Time					0	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency				2.0V 4.5V 6.0V	10 38 40	4 20 23	3 15 18	2 13 15	MHz MHz MHz
t_{PLH}, t_{PHL}	Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		2.0V 4.5V 6.0V	106 32 29	290 58 49	360 72 61	435 87 73	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		2.0V 4.5V 6.0V	93 28 25	230 46 39	290 57 49	345 69 58	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Ripple Clock		2.0V 4.5V 6.0V	62 18 16	150 30 26	190 37 32	225 45 37	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		2.0V 4.5V 6.0V	90 27 24	220 44 37	275 55 46	330 66 56	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Max/Min		2.0V 4.5V 6.0V	108 33 30	290 58 49	360 72 61	435 87 73	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Ripple Clock		2.0V 4.5V 6.0V	98 30 28	265 53 45	330 66 56	398 80 68	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Max/Min		2.0V 4.5V 6.0V	85 25 23	200 40 54	250 50 42	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		2.0V 4.5V 6.0V	85 25 23	200 40 34	250 50 42	300 60 51	ns ns ns
t_W	Width of Clock, Load or Clear Input Pulse				2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_{SETUP}	Data Setup Time				2.0V 4.5V 6.0V	20 10 8	100 20 17	125 25 21	150 30 25	ns ns ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF $t_r=t_f=6$ ns (unless otherwise specified)

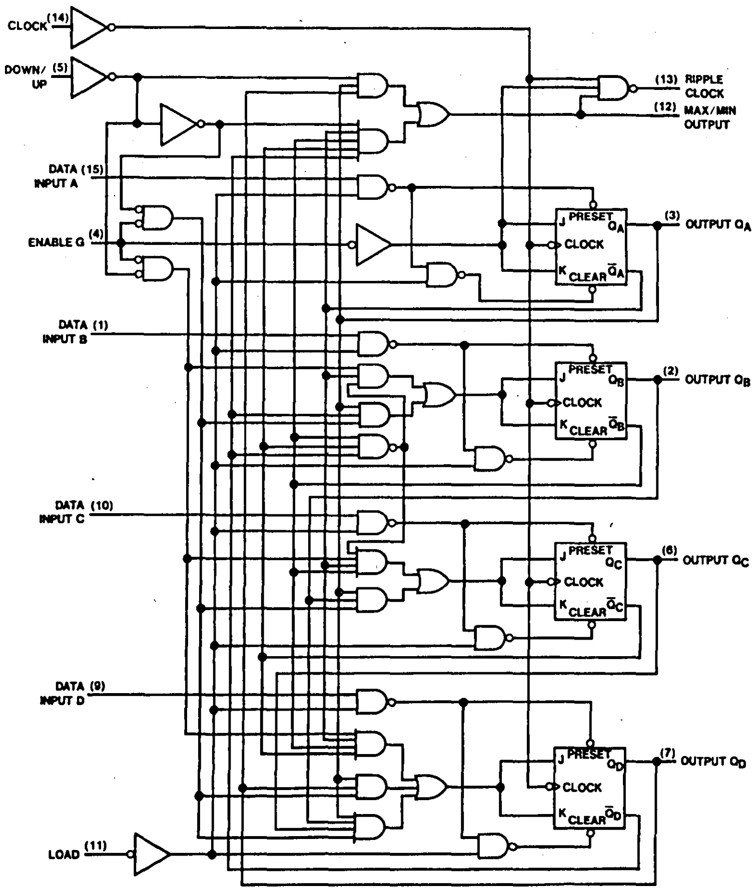
Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
							Guaranteed Limits			
t_H	Data Hold Time				2.0V		0	0	0	ns
					4.5V		0	0	0	ns
					6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				2.0V		75	95	110	s
					4.5V		15	19	22	ns
					6.0V		13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				2.0V		1000	1000	1000	ns
					4.5V		500	500	500	ns
					6.0V		400	400	400	ns
C_{IN}	Input Capacitance					5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)					100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams

'HC190 Decade Counters

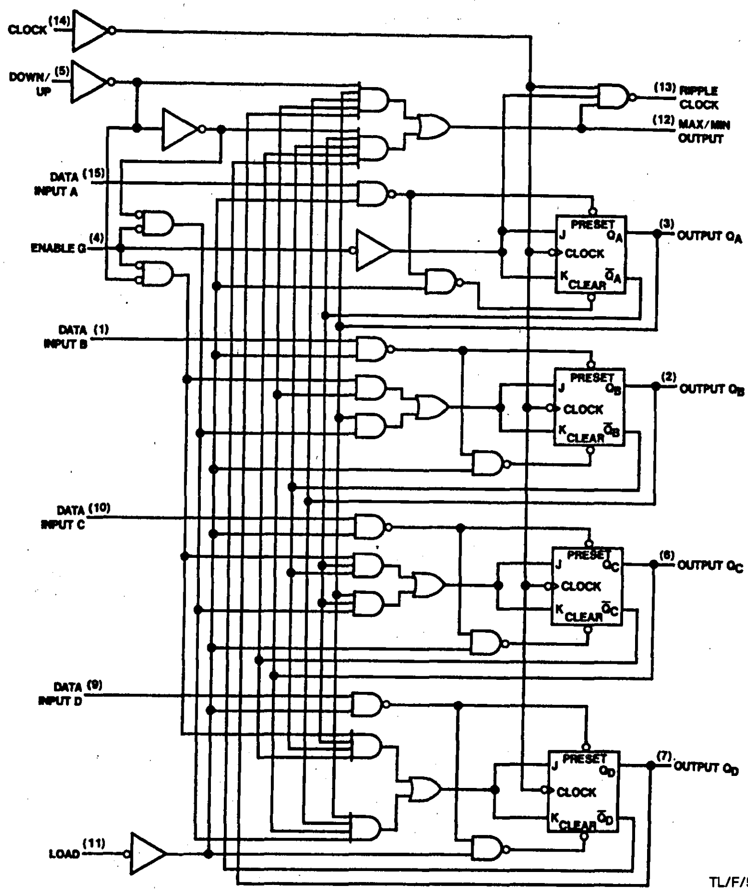


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/5322-2

Logic Diagrams (Continued)

'HC191 Binary Counters

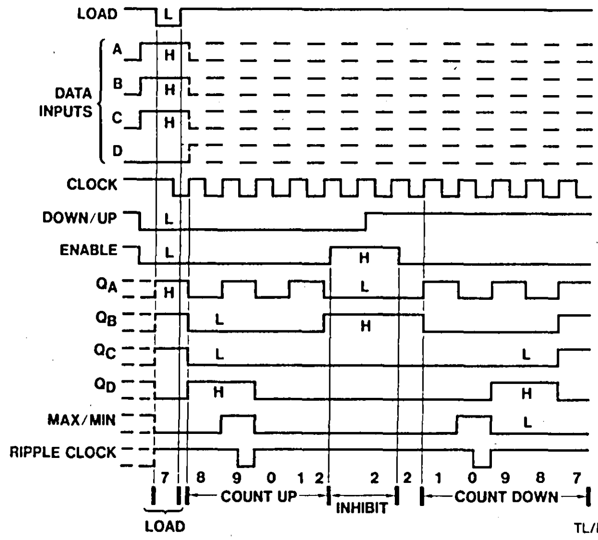


TL/F/5322-3

Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

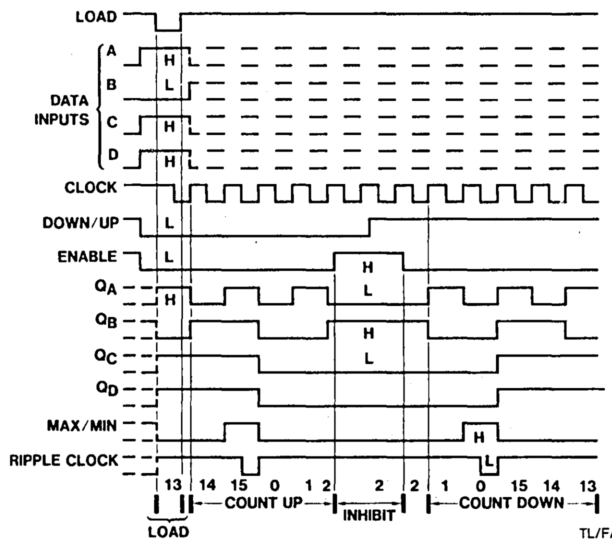
'HC190 Synchronous Decade Counters
Typical Load, Count, and Inhibit Sequences



TL/F/5322-4

Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

'HC191 Synchronous Binary Counters
Typical Load, Count, and Inhibit Sequence



TL/F/5322-5

Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

National Semiconductor

microCMOS

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HC192/MM74HC192 is a decade counter, and the MM54HC193/MM74HC193 is a binary counter. Both counters have two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counters can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

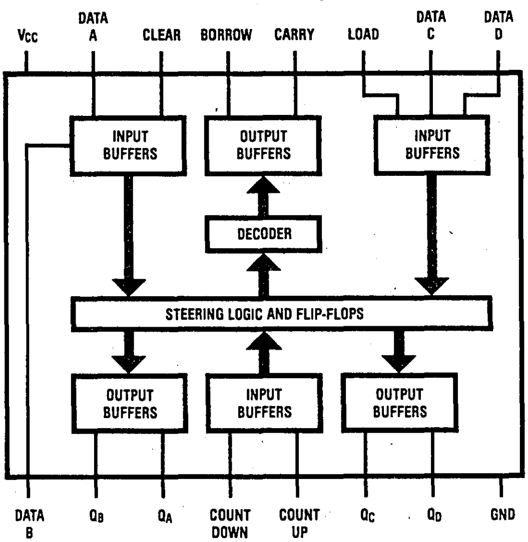
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Clock to output: 20 ns
- Typical operating frequency: 27 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- 4 mA output drive

Connection Diagram

Dual-In-Line Package



TL/F/5011-1

Truth Table

Count Up	Count Down	Clear	Load	Function
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = High level

L = Low level

↑ = Transition from low-to-high

X = Don't care

MM54HC192/MM74HC192
MM54HC193/MM74HC193

54HC192 (J) 74HC192 (J,N)
54HC193 (J) 74HC193 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns $C_L = 15$ pF (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Count Up		27	20	MHz
		Count Down		31	24	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry		17	26	ns
t_{PHL}	Maximum Propagation Delay High to Low			18	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Down to Borrow		16	24	ns
t_{PHL}	Maximum Propagation Delay High to Low			15	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q		28	40	ns
t_{PHL}	Maximum Propagation Delay High to Low			36	52	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q		30	42	ns
t_{PHL}	Maximum Propagation Delay High to Low			40	55	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		35	47	ns
t_W	Minimum Pulse Width	Clear	'HC192	40	52	ns
			'HC193	20	26	ns
		Load		10	20	ns
		Count Up/Down		15	22	ns
t_{SD}	Minimum Setup time	Data to Load		10	20	ns
t_{HD}	Minimum Hold Time			−3	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock			10	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency	Count Up	2.0V	5	3	2.5	2	MHz
			4.5V	25	18	14	12	MHz
			6.0V	29	20	16	13	MHz
		Count Down	2.0V	5	4	3	2	MHz
			4.5V	27	20	16	11	MHz
			6.0V	31	23	18	12	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry	2.0V	30	140	175	210	ns
			4.5V	13	28	35	42	ns
			6.0V	11	24	30	36	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f = 6$ ns (Continued)

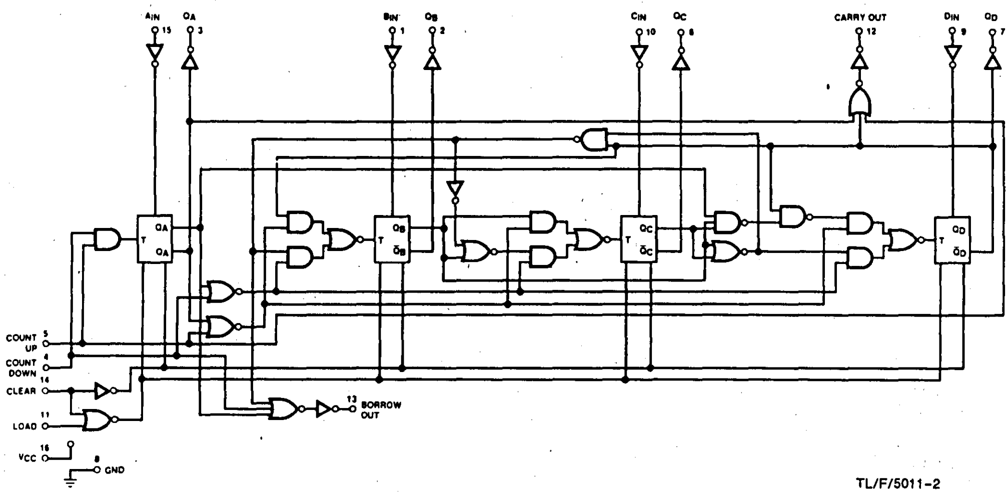
Symbol	Parameter	Conditions		V_{CC}	T_A=25°C Typ	Guaranteed Limits	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay	Count Down to Borrow		2.0V	39	130	163	195	ns
				4.5V	16	26	33	39	ns
				6.0V	14	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q		2.0V	77	215	269	323	ns
				4.5V	35	43	54	65	ns
				6.0V	30	37	46	55	ns
t_{PHL}	Maximum Propagation Delay High to Low			2.0V	95	275	344	413	ns
				4.5V	45	55	69	83	ns
				6.0V	38	47	59	71	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q		2.0V	85	230	288	345	ns
				4.5V	37	46	58	69	ns
				6.0V	30	39	49	59	ns
t_{PHL}	Maximum Propagation Delay High to Low			2.0V	102	290	363	435	ns
				4.5V	47	58	73	87	ns
				6.0V	39	49	61	74	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		2.0V	85	265	331	398	ns
				4.5V	42	53	66	80	ns
				6.0V	38	45	56	68	ns
t_W	Minimum Pulse Width	Clear	'HC192	2.0V	119	260	325	390	ns
				4.5V	42	52	65	78	ns
				6.0V	38	45	56	68	ns
		Load		2.0V	31	100	125	150	ns
				4.5V	10	20	25	30	ns
				6.0V	9	17	21	26	ns
		Count Up/Down		2.0V	43	110	138	165	ns
				4.5V	17	22	28	33	ns
				6.0V	15	19	24	29	ns
		Clear	'HC193	2.0V	70	130	163	195	ns
				4.5V	21	26	33	39	ns
				6.0V	19	22	28	33	ns
t_{SD}	Minimum Setup Time	Data To Load		2.0V	30	100	125	150	ns
				4.5V	10	20	25	30	ns
				6.0V	9	17	22	25	ns
t_{HD}	Minimum Hold Time			2.0V	−30	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−3	0	0	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock		2.0V	−20	10	10	10	ns
				4.5V	−3	10	10	10	ns
				6.0V	−2	10	10	10	ns
t_r, t_f	Maximum Input Rise & Fall Time			2.0V		500	500	500	ns
				4.5V		300	300	300	ns
				6.0V		200	200	200	ns
C_{IN}	Input Capacitance				5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)				100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

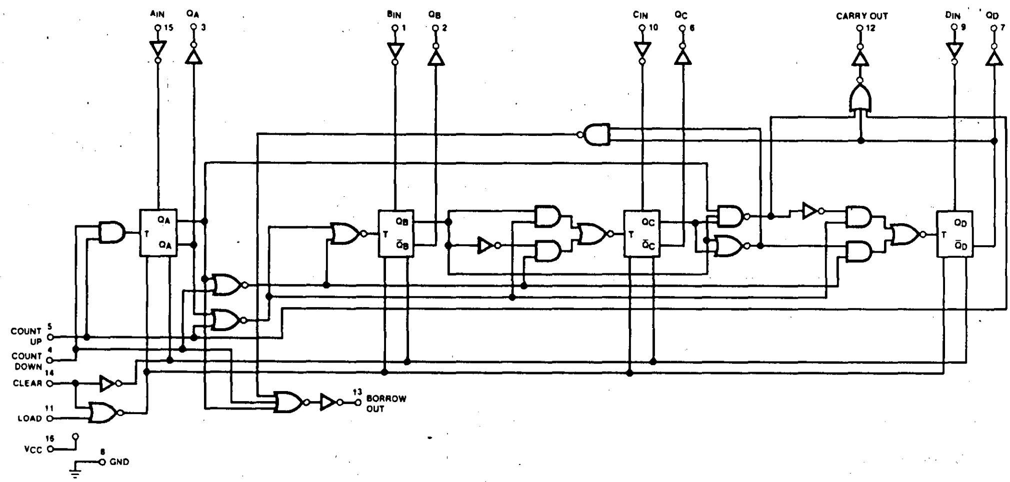
Logic Diagrams

MM54HC192 Synchronous 4-Bit Up/Down Decade Counter



TL/F/5011-2

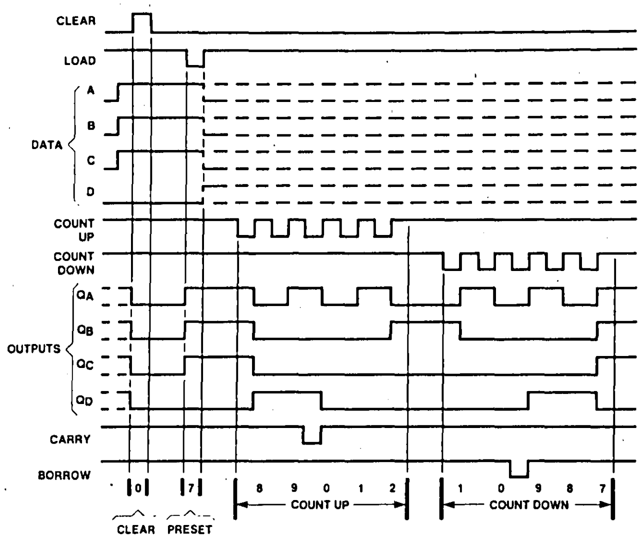
MM54HC193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5011-3

Logic Waveforms

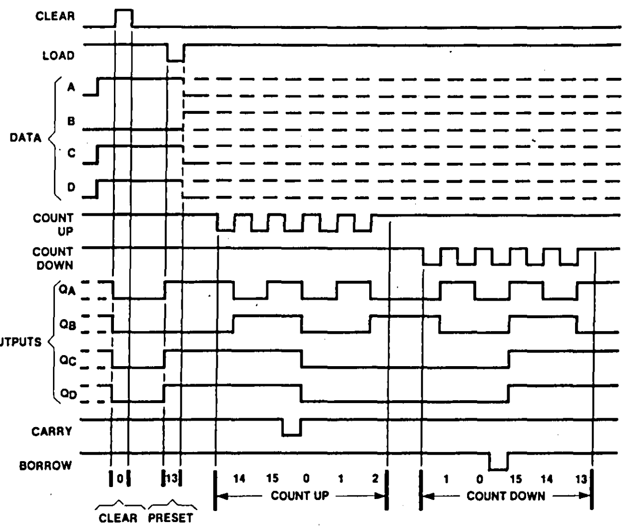
'HC192 Synchronous Decade Counters
Typical Clear, Load, and Count Sequences



TL/F/5011-4

Sequences:
(1) Clear outputs to zero
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

'HC193 Synchronous Binary Counters
Typical Clear, Load, and Count Sequences



TL/F/5011-5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

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MM54HC194/MM74HC194 4-Bit Bidirectional Universal Shift Register

General Description

This 4-bit high speed BIDIRECTIONAL SHIFT REGISTER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads. This device operates at speeds similar to the equivalent low power Schottky part.

This BIDIRECTIONAL SHIFT REGISTER is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: PARALLEL (broadside) LOAD; SHIFT RIGHT (in the direction Q_A toward Q_D); SHIFT LEFT; INHIBIT CLOCK (do nothing).

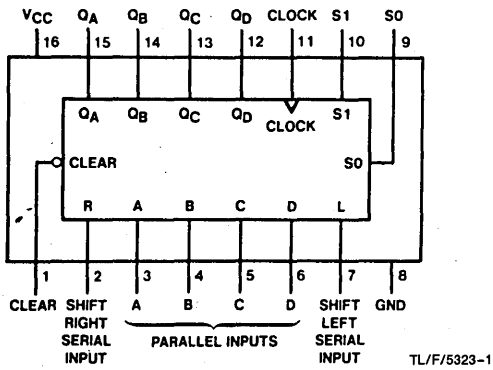
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into their respective flip flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 160 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram Dual-In-Line Package



MM54HC194/MM74HC194

54HC194 (J) 74HC194 (J,N)

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S2		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		17	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		19	25	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Set Up Time (A, B, C, D to Clock)			20	ns
t_S	Minimum Set Up Time Mode Controls to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset		9	16	ns
t_H	Minimum Hold Time Any Input		−3	0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

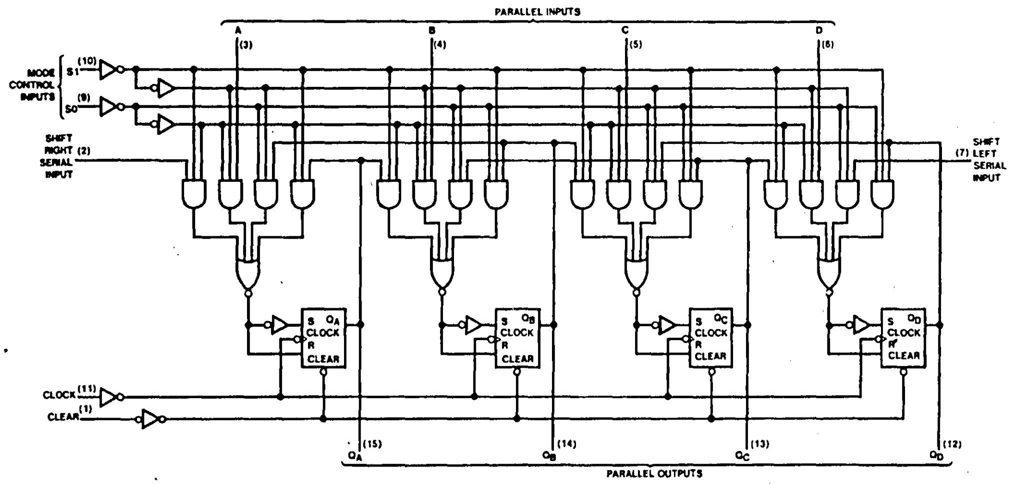
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	70	145	183	216	ns
			4.5V	15	29	37	45	ns
			6.0V	12	25	31	37	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V	80	150	189	216	ns
			4.5V	15	30	37	45	ns
			6.0V	12	26	31	37	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{REM}	Minimum Removal Time Reset Inactive to Clock		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_S	Minimum Set Up Time (A, B, C, or D to Clock)		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Time Mode Controls to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Any Input		2.0V	−10	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Reset		2.0V	30	80	100	120	ns
			4.5V	89	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

MM54HC194/MM74HC194



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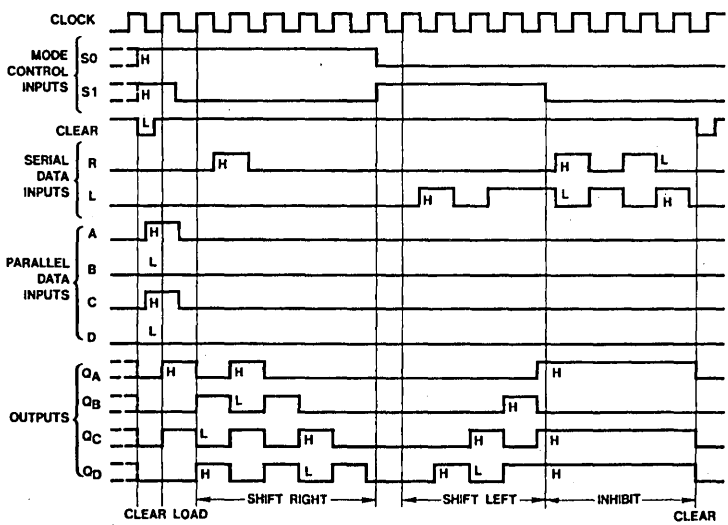
Timing Diagram



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National Semiconductor

microCMOS

MM54HC195/MM74HC195 4-Bit Parallel Shift Register

General Description

The MM54HC195/MM74HC195 is a high speed 4-bit SHIFT REGISTER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads at LS type speeds.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes: Parallel Load; Shift from Q_A towards Q_D.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

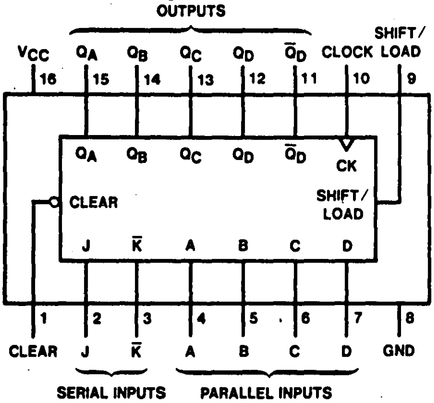
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: 16 ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



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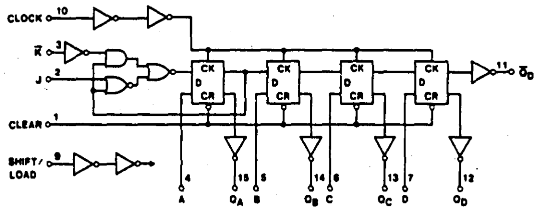
MM54HC195/MM74HC195

54HC195 (J) 74HC195 (J,N)

Logic Diagram



TL/F/5324–2

Function Table

Inputs									Outputs				
Clear	Shift/Load	Clock	Serial J	Serial $\overline{K}$	Parallel A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		14	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		16	25	ns
t_{REM}	Minimum Removal Time, Shift/Load to Clock			0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Set Up Time, (A, B, C, D, J, $\overline{K}$ to Clock)			20	ns
t_S	Minimum Set Up Time, Shift/Load to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset			16	ns
t_H	Minimum Hold Time, any Input except Shift/Load			0	ns

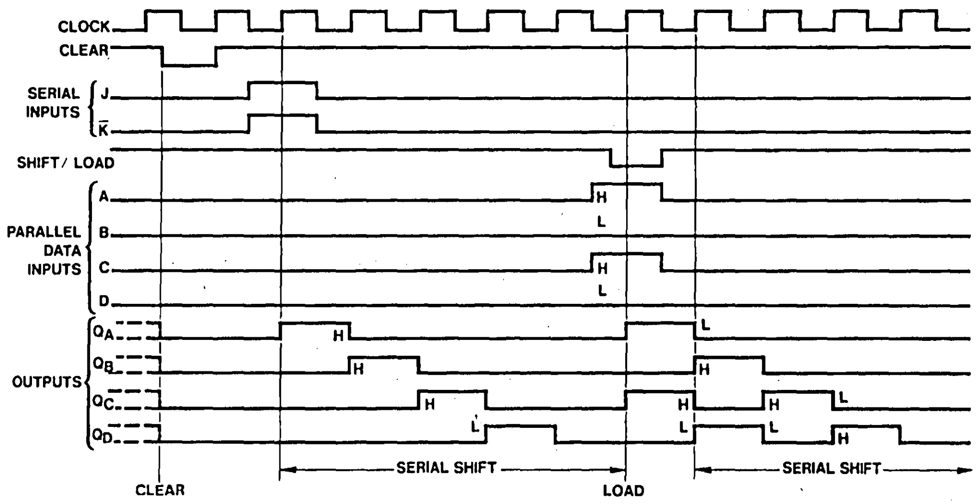
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V	70	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	12	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	70	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{REM}	Minimum Removal Time, Shift Load to Clock		2.0V	−2	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_S	Minimum Set Up Time, (A, B, C, D, J, $\overline{K}$ to Clock)		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Up Time, Shift/Load to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Any Input except Shift/Load		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Pulse Width, Clock or Reset		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Timing Diagram



TL/F/5324-3

National Semiconductor

microCMOS

MM54HC221A/MM74HC221A Dual Non-Retriggerable Monostable Multivibrator

General Description

The MM54/74HC221A high speed monostable multivibrators (one shots) utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC221A can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC221A is a non-retriggerable, and therefore cannot be retriggered until the output pulse times out.

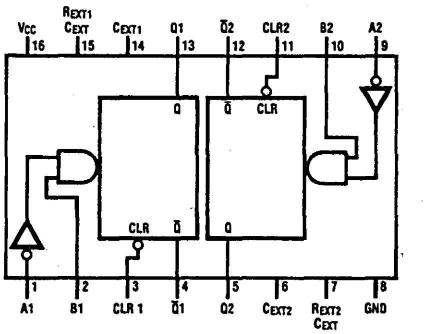
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})\ (C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise or fall times

Connection Diagram

Dual-In-Line Package



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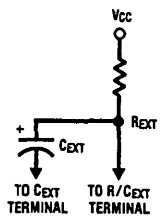
TOP VIEW
MM54HC221A/MM74HC221A

54HC221A (J) 74HC221A (J,N)

Timing Component



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Truth Table

Inputs			Outputs	
Clear	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔
↑	L	H	⎍	⊔

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (All other pins)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Standby)	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable	$V_{IN}=V_{CC}$ or GND R/C_{EXT} = 0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

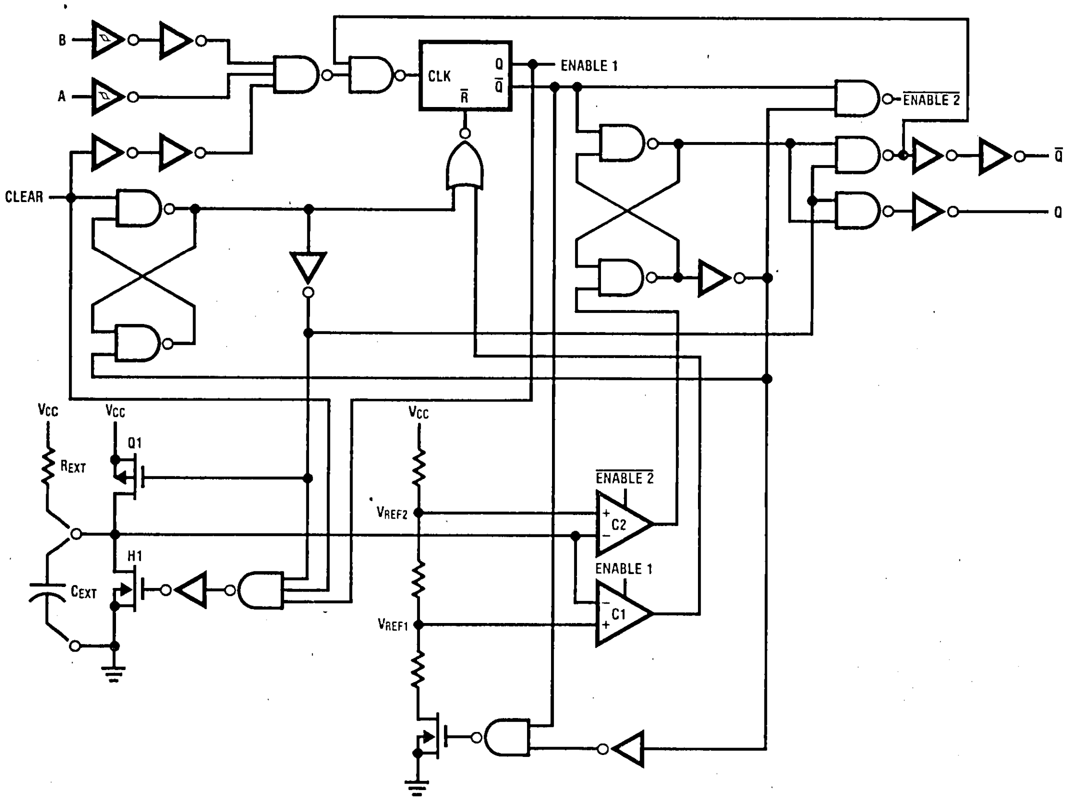
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	36	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		20	31	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		µs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns(unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		2.0V 4.5V 6.0V	77 26 21	169 42 32	194 51 39	210 57 44	ns ns ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		2.0V 4.5V 6.0V	88 29 24	197 48 38	229 60 46	250 67 51	ns ns ns
t_{PHL}	Maximum Propagation Delay Clear to Q		2.0V 4.5V 6.0V	54 23 19	114 34 28	132 41 33	143 45 36	ns ns ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		2.0V 4.5V 6.0V	56 25 20	116 36 29	135 42 34	147 46 37	ns ns ns
t_W	Minimum Pulse Width A, B, Clear		2.0V 4.5V 6.0V	57 17 12	123 30 21	144 37 27	157 42 30	ns ns ns
t_{REM}	Minimum Clear Removal Time		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ $R_{EXT}=6$ kΩ ($V_{CC}=2V$)	2.0V 4.5V 6.0V	1.5 450 380				µs ns ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ µF $R_{EXT}=10$ kΩ — Min	4.5V	1	0.9			ms
		Max	4.5	1	1.1			ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)			12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (Other Inputs)			6	10	10	10	pF

Logic Diagram



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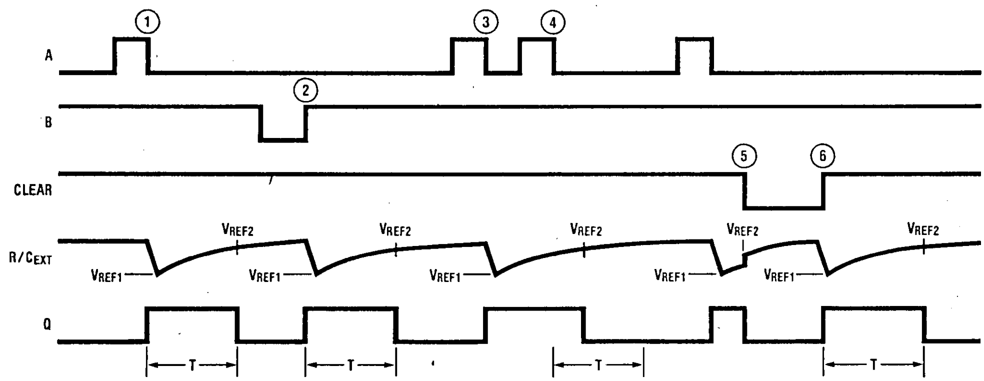
Theory of Operation



TL/F/5206-6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ NO RETRIGGERING
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER ('HC123, 'HC221A ONLY)

FIGURE 1

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}②. The 'HC221 can also be triggered when clear goes from GND to V_{CC} (while A is at Gnd and B is at V_{CC}⑥.)

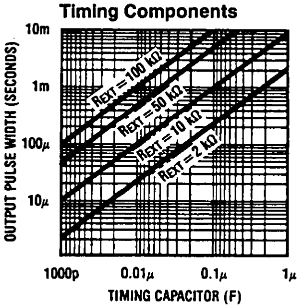
It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC221 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

The 'HC221 is non-retriggerable and will ignore input transitions on A and B until it has timed out ③ and ④.

RESET OPERATION

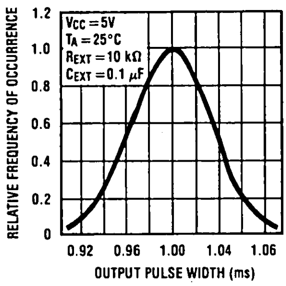
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



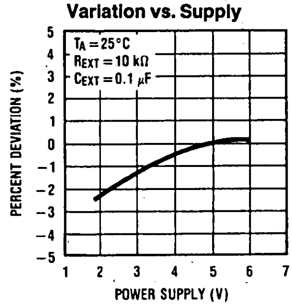
TL/F/5206-7

Typical Distribution of Output Pulse Width, Part to Part



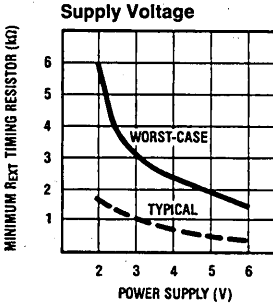
TL/F/5206-8

Typical 1ms Pulse Width Variation vs. Supply



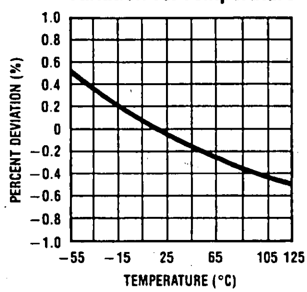
TL/F/5206-9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5206-10

Typical 1 ms Pulse Width Variation vs. Temperature



TL/F/5206-11

Note: R and C are not subjected to temperature. The C is polypropolyne.

National Semiconductor

microCMOS

MM54HC237/MM74HC237 3-to-8 Line Decoder With Address Latches

General Description

These devices utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

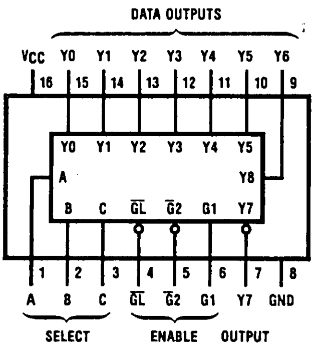
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

Connection Diagram

Dual-In-Line Package

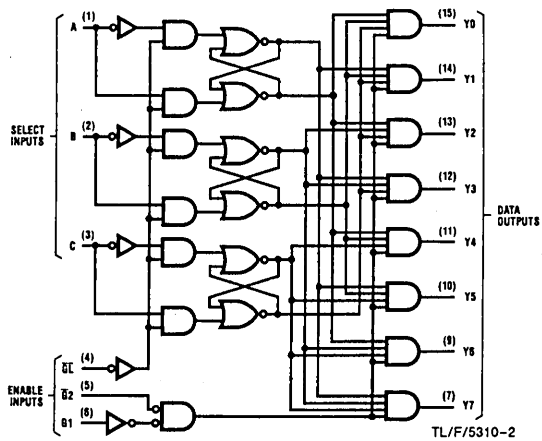


TOP VIEW TL/F/5326-1

MM54HC237/MM74HC237

54HC237 (J) 74HC237(J,N)

Functional Block Diagram



TL/F/5310-2

Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		20	41	ns
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		16	32	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		22	44	ns
t_{PHL}	Maximum Propagation Delay GL to any Y Output		17	33	ns
t_{PLH}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		16	35	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		14	25	ns
t_S	Minimum Set Up Time at A, B and C inputs		10	20	ns
t_H	Minimum Hold Time at A, B and C inputs		−3	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		9	16	ns

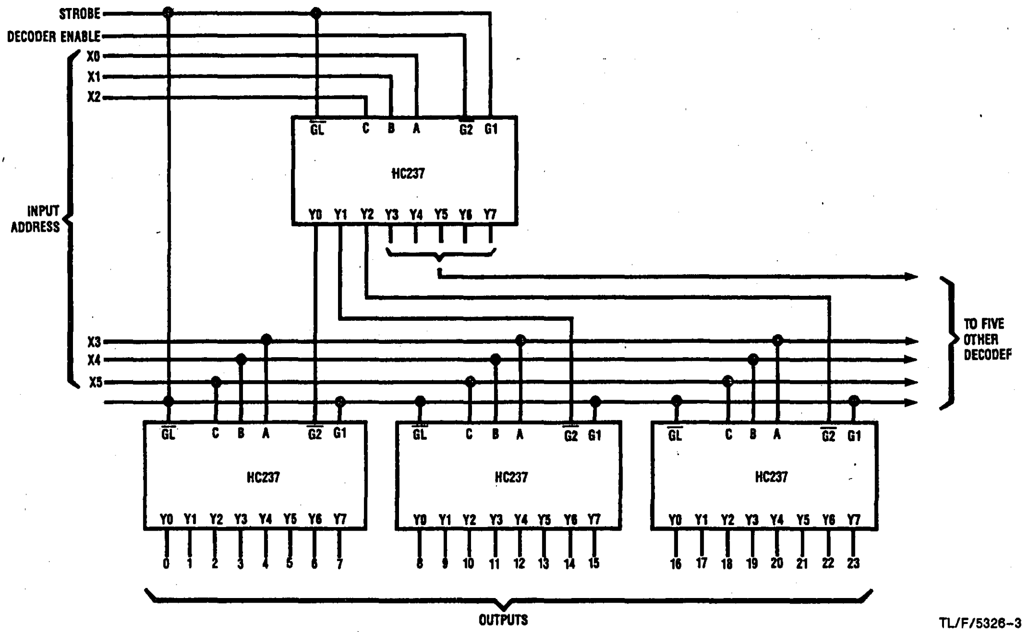
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	100	235	296	350	ns
			4.5V	24	47	59	70	ns
			6.0V	20	40	50	60	ns
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	80	185	233	276	ns
			4.5V	19	37	47	55	ns
			6.0V	17	31	40	47	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	63	ns
t_{PHL}	Maximum Propagation Delay $\overline{GL}$ to any Y Output		2.0V	95	190	239	283	ns
			4.5V	19	38	48	75	ns
			6.0V	16	32	41	48	ns
t_{PLH}	Maximum Propagation Delay, G1 or $\overline{G2}$ to Output		2.0V	100	200	252	298	ns
			4.5V	20	40	50	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		2.0V	73	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_S	Minimum Set Up Time at A, B and C Inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C Inputs		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Typical Application



TL/F/5326-3

6-Line to 64-Line Decoder with Input Address Storage

National Semiconductor

microCMOS

MM54HC240/MM74HC240 Inverting Octal TRI-STATE® Buffer MM54HC241/MM74HC241 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Each have a fanout of 15 LS-TTL equivalent inputs.

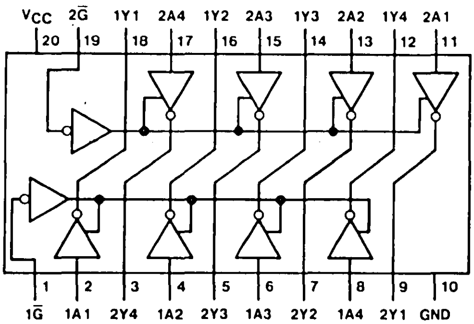
The MM54HC240/MM74HC240 is an inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers. MM54HC241/MM74HC241 is a non-inverting buffer that has one active low enable and one active high enable, each again controlling 4 buffers. Neither device has Schmitt trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 series)
- Output current: 6 mA

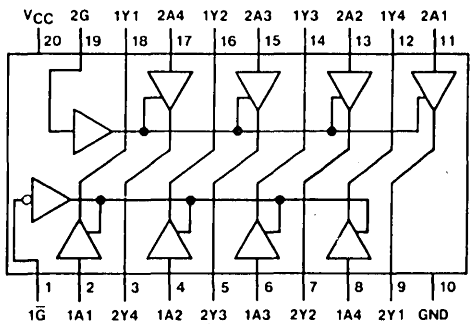
Connection Diagrams Dual-In-Line Packages



TOP VIEW TL/L/5020-1

MM54HC240/MM74HC240

54HC240 (J) 74HC240 (J,N)



TOP VIEW TL/L/5020-2

MM54HC241/MM74HC241

54HC241 (J) 74HC241 (J,N)

Truth Tables

('HC240)

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

('HC241)

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND $\overline{G}=V_{IH}$, $G=V_{IL}$	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ $C_L=45$ pF	14	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	28	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

AC Electrical Characteristics MM54HC241/MM74HC241

V_{CC}=5V, T_A=25°C, t_r=t_f=6 ns

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L=45 pF		13	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	R_L=1 kΩ	$1\overline{G}$	17	28	ns
		C_L=45 pF	$2\overline{G}$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Input	R_L=1 kΩ	$1\overline{G}$	15	25	ns
		C_L=5 pF	$2\overline{G}$	13	25	ns

AC Electrical Characteristics MM54HC241/MM74HC241

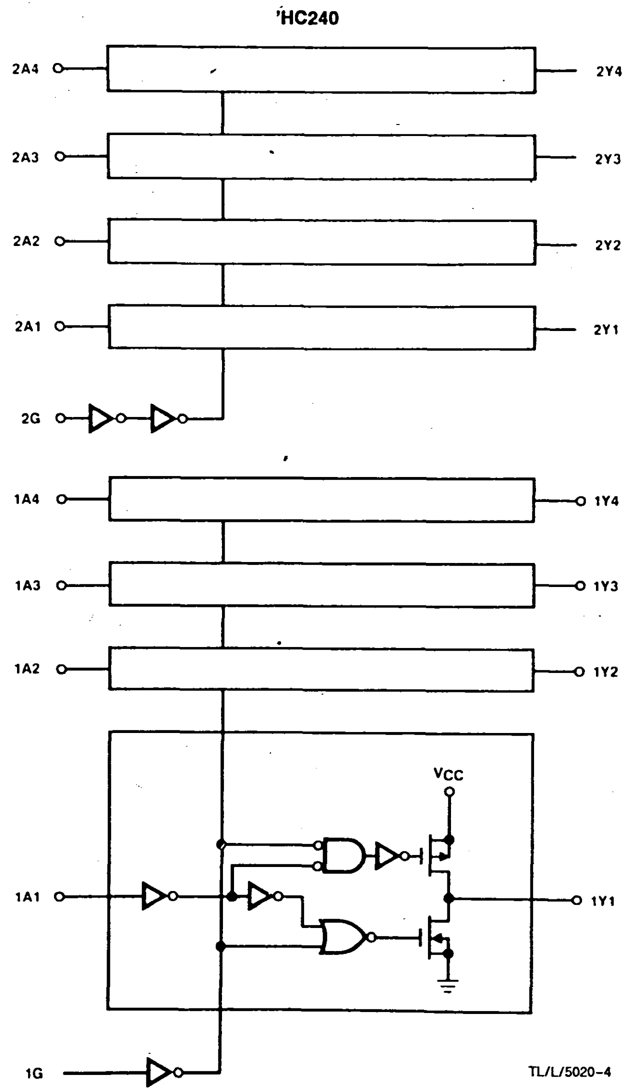
V_{CC}=2.0V to 6.0V, C_L=50 pF, t_r=t_f=6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L=50 pF	2.0V	58	115	145	171	ns
		C_L=150 pF	2.0V	83	165	208	246	ns
		C_L=50 pF	4.5V	14	23	29	34	ns
		C_L=150 pF	4.5V	17	33	42	49	ns
		C_L=50 pF	6.0V	10	20	25	29	ns
		C_L=150 pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L=1 kΩ						
		C_L=50 pF	2.0V	75	150	189	224	ns
		C_L=150 pF	2.0V	100	200	252	298	ns
		C_L=50 pF	4.5V	15	30	38	45	ns
		C_L=150 pF	4.5V	20	40	50	60	ns
		C_L=50 pF	6.0V	13	26	32	38	ns
		C_L=150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L=1 kΩ	2.0V	75	150	189	224	ns
		C_L=50 pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}$=V_{IH}, G=V_{IL}		12				pF
		$\overline{G}$=V_{IL}, G=V_{IH}		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams



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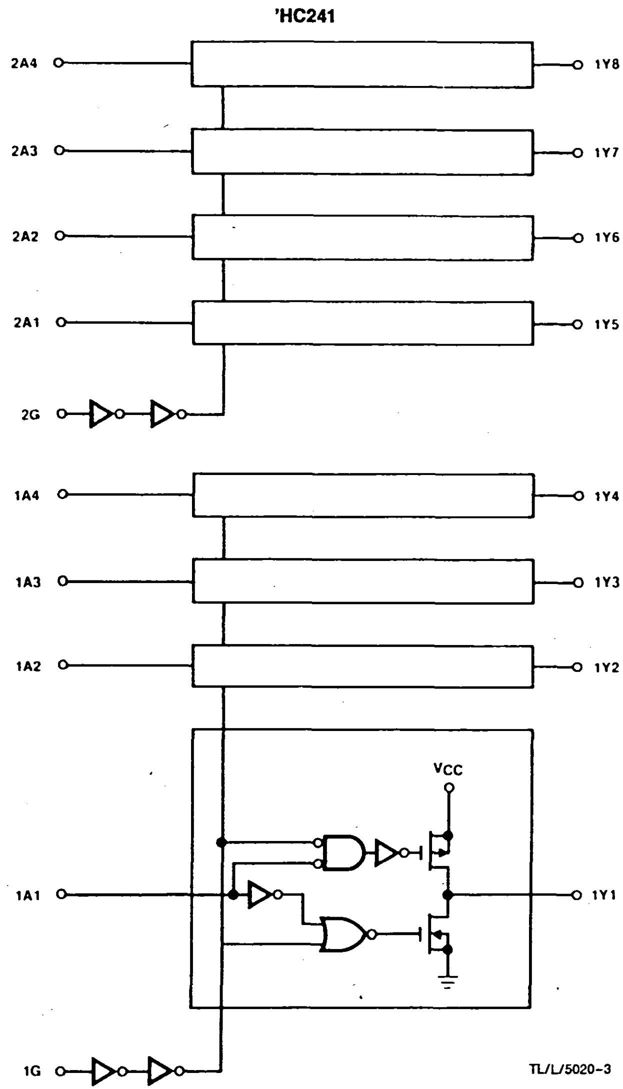


TL/L/5020-3

National Semiconductor

microCMOS

MM54HC242/MM74HC242 Inverting Quad TRI-STATE® Transceiver MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional inverting and non-inverting buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances. These circuits possess the low power dissipation and high noise immunity associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LS-TTL loads.

The MM54HC242/MM74HC242 is a non-inverting buffer and the MM54HC243/MM74HC243 is an inverting buffer. Each device has one active high enable (GBA), and one active low enable (GAB). GBA enables the A outputs and GAB enables the B outputs. This device does not have Schmitt trigger inputs.

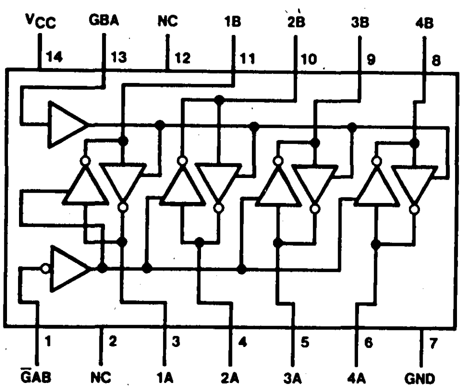
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs
- Two way asynchronous communication
- High output current: 6 mA (74HC)
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74HC)

Connection Diagrams

Dual-In-Line Package



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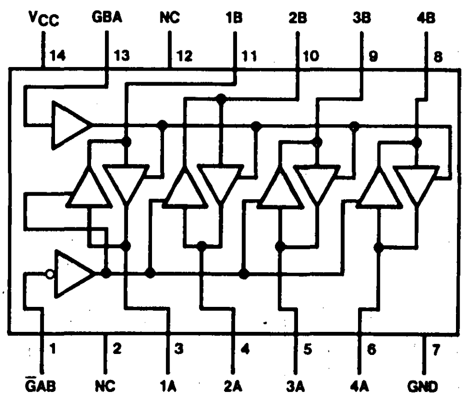
TOP VIEW

MM54HC242/MM74HC242

54HC242 (J) 74HC242 (J,N)

Dual-In-Line Package



TL/L/5019-2

TOP VIEW

MM54HC243/MM74HC243

54HC243 (J) 74HC243 (J,N)

Truth Tables

Control Inputs		Data Port Status	
$\overline{\text{GAB}}$	GBA	A	B
H	H	$\overline{\text{OUTPUT}}$	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	$\overline{\text{OUTPUT}}$

Control Inputs		Data Port Status	
$\overline{\text{GAB}}$	GBA	A	B
H	H	OUTPUT	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	OUTPUT

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{G}AB=V_{IH}$, GBA= V_{IL} ($\overline{G}AB$ and GBA only)	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics (MM54HC242/MM74HC242)

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PHL}	Maximum Output Disable Time from Active Output	$R_L=$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics MM54HC242/MM74HC242

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	18	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

AC Electrical Characteristics (MM54HC243/MM74HC243)

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=k\Omega$ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=k\Omega$ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics MM54HC243/MM74HC243

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

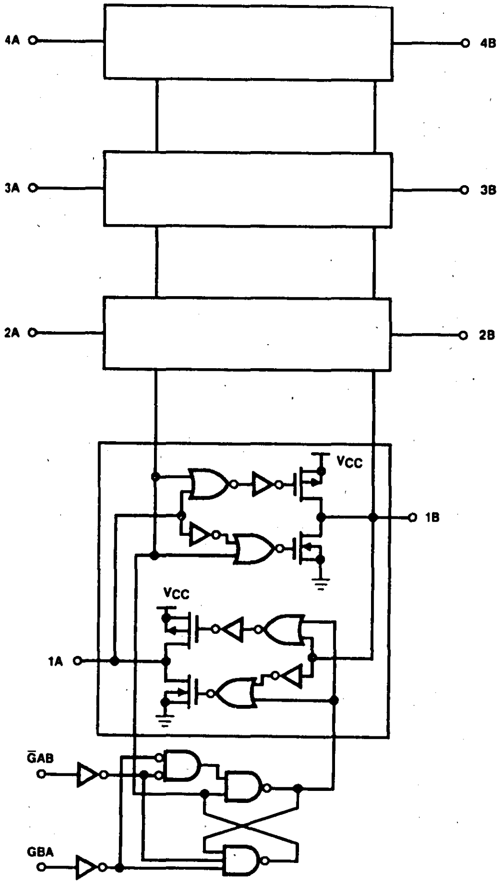
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	88	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=1\ k\Omega$						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=1\ k\Omega$ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

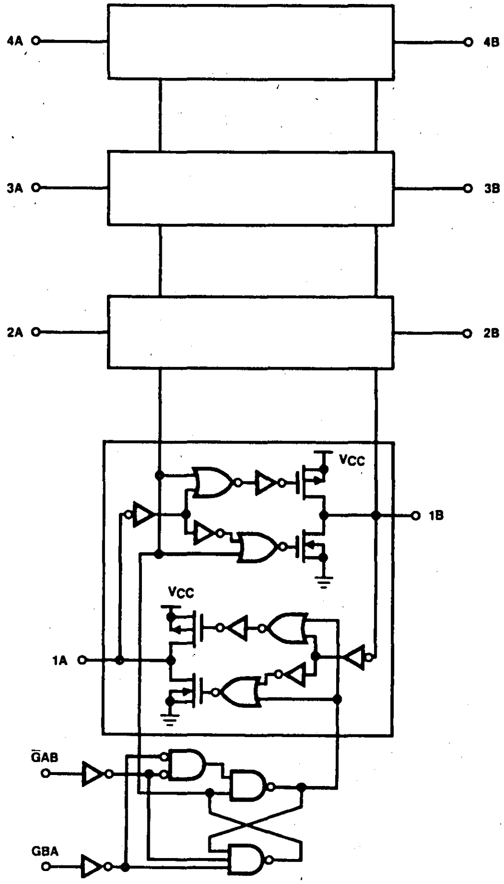
Logic Diagrams

MM54HC242/MM74HC242



TL/L/5019-3

MM54HC243/MM74HC243



TL/L/5019-4

National Semiconductor

microCMOS

MM54HC244/MM74HC244 Octal TRI-STATE® Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and are general purpose high speed non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. All three devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC244/MM74HC244 is a non-inverting buffer and has two active low enables (1G and 2G). Each enable independently controls 4 buffers. This device does not have Schmitt trigger inputs.

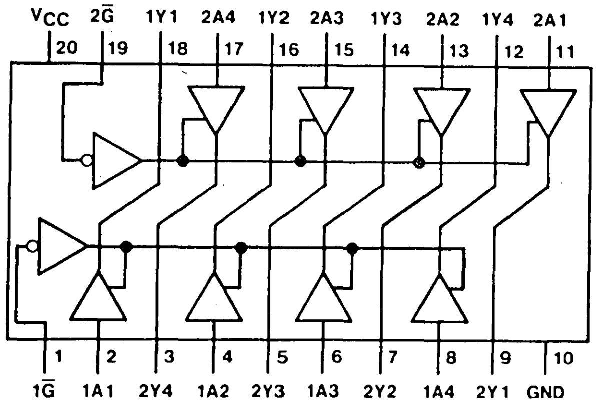
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 series)
- Output current: 6 mA

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5327-1

MM54HC244/MM74HC244

54HC244 (J) 74HC244 (J,N)

Truth Table

('HC244)

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|\le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH}, or V_{IL} V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC244/MM74HC244

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay From Active Output	$R_L=1$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V\text{-}6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

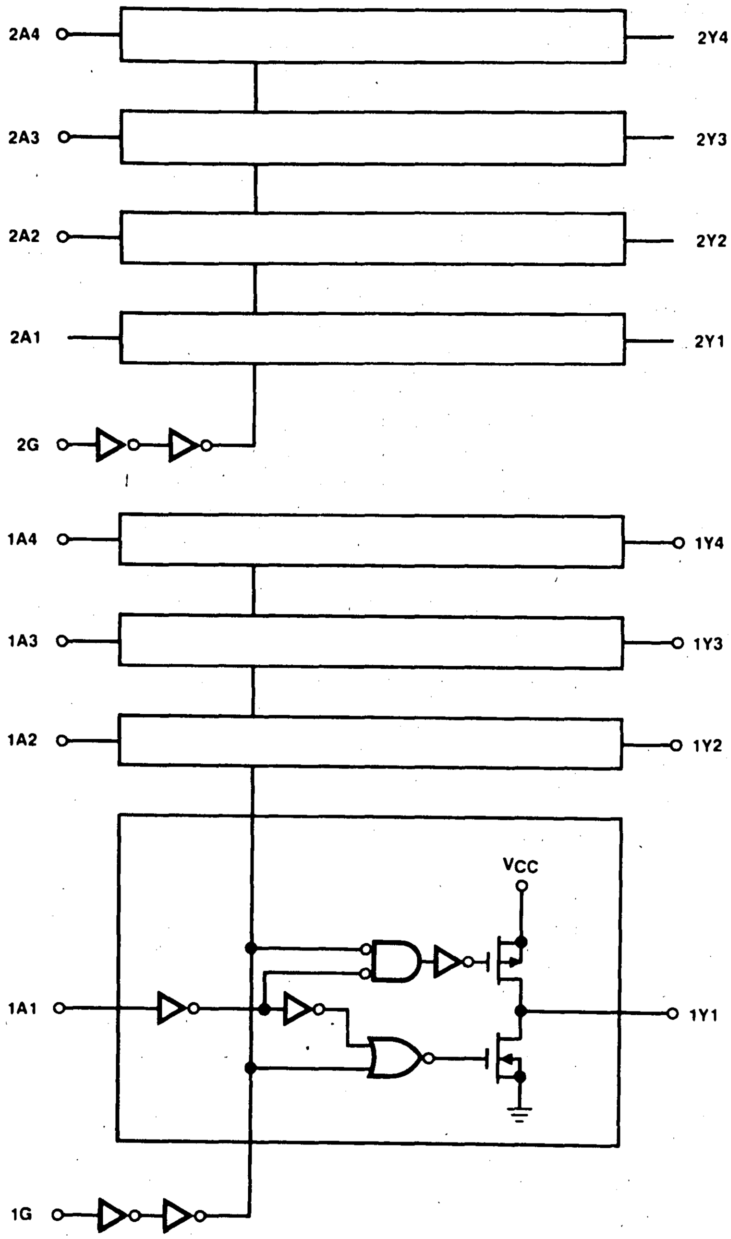
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	750	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	.75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$		12				pF
		$\overline{G}=V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

'HC244



TL/F/5327-2

MM54HC245/MM74HC245 Octal TRI-STATE® Transceiver

General Description

These TRI-STATE bi-directional buffers utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

This device has an active low enable input $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC245/MM74HC245 transfers true data from one bus to the other.

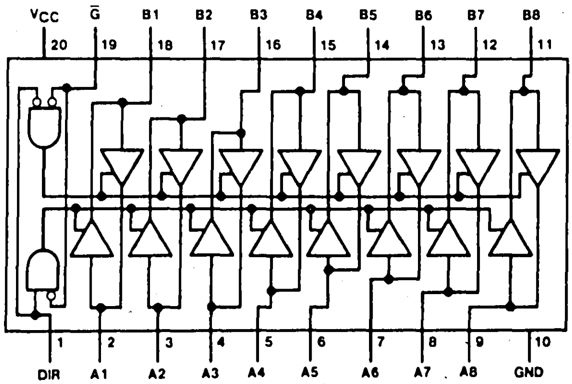
This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)
- Same as the '645

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5165-1

MM54HC245/MM74HC245

54HC245 (J) 74HC245 (J,N)

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC}+1.5V
DC Input/Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	$V_{IN}=V_{CC}$ to GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND Enables $\overline{G}=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45$ pF	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	32	42	ns

AC Electrical Characteristics

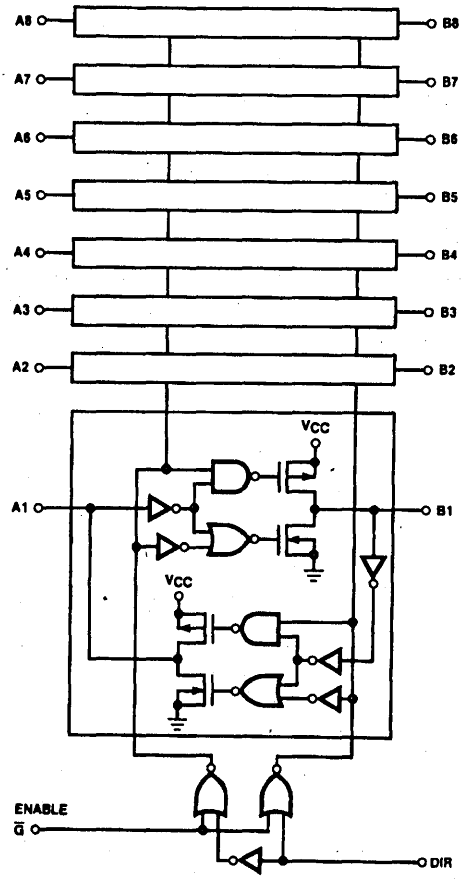
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50$ pF	2.0V	29	72	88	96	ns
		$C_L = 150$ pF	2.0V	38	96	116	128	ns
		$C_L = 50$ pF	4.5V	14	18	22	24	ns
		$C_L = 150$ pF	4.5V	18	24	29	32	ns
		$C_L = 50$ pF	6.0V	14	18	22	24	ns
		$C_L = 150$ pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	70	184	224	240	ns
		$C_L = 150$ pF	2.0V	80	216	260	284	ns
		$C_L = 50$ pF	4.5V	35	46	56	60	ns
		$C_L = 150$ pF	4.5V	41	54	65	71	ns
		$C_L = 50$ pF	6.0V	31	41	50	54	ns
		$C_L = 150$ pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 50$ pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time	$C_L=50$ pF	2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G} = V_{IL}$		100				pF
		$\overline{G} = V_{IH}$		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5165-2

'HC245

National Semiconductor

microCMOS

MM54HC251/MM74HC251 8-Channel TRI-STATE® Multiplexer

General Description

This 8-CHANNEL DIGITAL MULTIPLEXER with TRI-STATE outputs utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

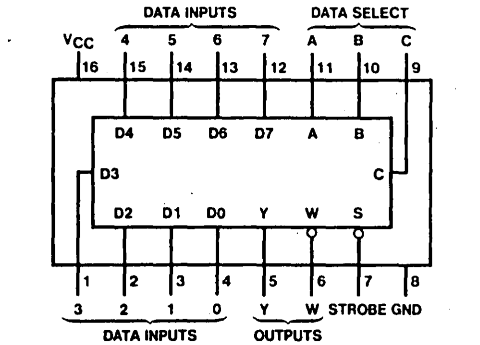
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 54HC/74HC logic family is speed, function, as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  Data Select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC)
- TRI-STATE outputs for interface to bus oriented systems

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5328-1

MM54HC251/MM74HC251

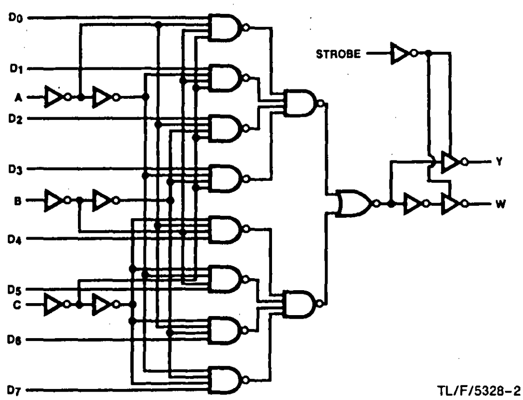
54HC251 (J) 74HC251 (J,N)

Truth Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

Logic Diagram



TL/F/5328-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE® Leakage Current	Strobe=V_{CC} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	$R_L=1k$ $C_L=50$ pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	$R_L=1k$ $C_L=50$ pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1k$ $C_L=5$ pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1k$ $C_L=5$ pF	27	35	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V 4.5V 6.0V	90 31 26	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		2.0V 4.5V 6.0V	95 32 27	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		2.0V 4.5V 6.0V	70 27 23	195 39 33	244 49 41	283 57 48	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		2.0V 4.5V 6.0V	75 29 25	185 37 32	231 46 40	268 54 46	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	$R_L=1k$	2.0V 4.5V 6.0V	45 21 18	150 30 26	188 38 33	218 44 38	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	$R_L=1k$	2.0V 4.5V 6.0V	45 21 18	145 29 25	181 36 31	210 42 36	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1k$	2.0V 4.5V 6.0V	60 29 25	220 44 37	275 55 46	319 64 54	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1k$	2.0V 4.5V 6.0V	60 30 26	195 39 33	244 49 41	283 57 48	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

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MM54HC253/MM74HC253 Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HC253/MM74HC253 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads. The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

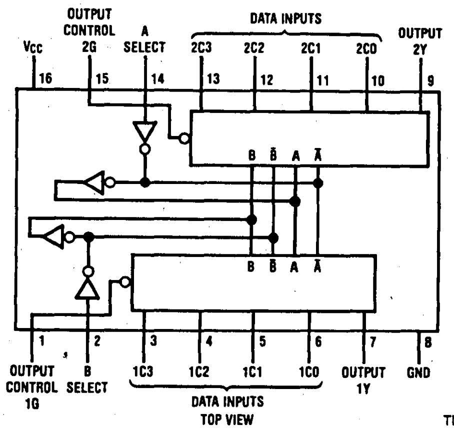
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5108-1

MM54HC253/MM74HC253

54HC253 (J) 74HC253 (J,N)

Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	Strobe=V_{CC} $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=15$ pF

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		24	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		18	23	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output to a Logic Level	$R_L=1k$	13	18	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output to High Impedance State	$R_L=1k$	18	27	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

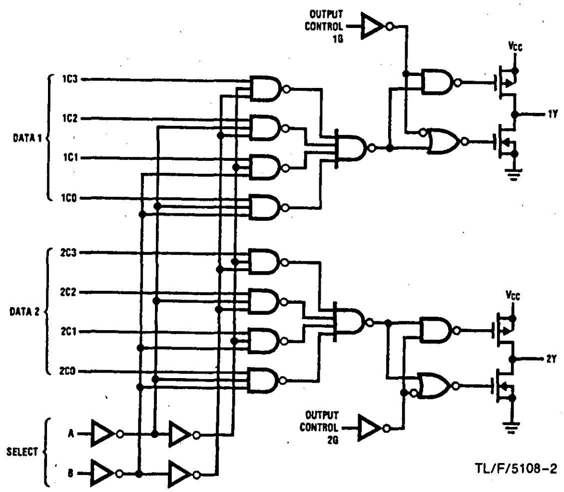
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	158	198	237	ns
			4.5V	29	35	44	53	ns
			6.0V	24	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	126	158	189	ns
			4.5V	22	28	35	42	ns
			6.0V	19	23	29	35	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1\ k\Omega$	2.0V	63	90	113	135	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1\ k\Omega$	2.0V	90	135	169	203	ns
			4.5V	20	30	38	45	ns
			6.0V	17	25	31	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						
		Outputs Enabled		90				pF
		Outputs Disabled		25				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

'HC253



TL/F/5108-2

National Semiconductor

microCMOS

MM54HC257/MM74HC257
Quad 2-Channel TRI-STATE® Multiplexer

General Description

This QUAD 2-TO-1 LINE DATA SELECTOR/MULTIPLEXER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

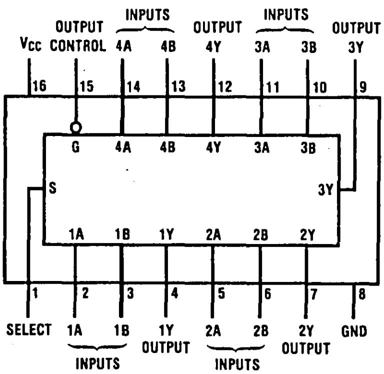
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- TRI-STATE outputs for connection to system buses.

Connection and Logic Diagrams

Dual-In-Line Package

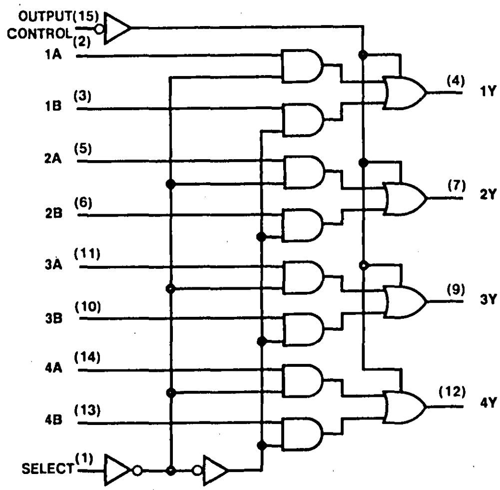


TOP VIEW

TL/F/5329-1

MM54HC257/MM74HC257

54HC257 (J) 74HC257 (J,N)



TL/F/5329-2

Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	$V_{OUT}=V_{CC}$ or GND $OC=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L=45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	13	21	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L=50$ pF	2.0V	50	100	125	150	ns
		$C_L=150$ pF	2.0V	70	150	189	224	ns
		$C_L=50$ pF	4.5V	10	20	25	30	ns
		$C_L=150$ pF	4.5V	15	30	38	45	ns
		$C_L=50$ pF	6.0V	9	17	21	25	ns
		$C_L=150$ pF	6.0V	13	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	2.0V	50	100	125	150	ns
		$C_L=150$ pF	2.0V	70	150	190	221	ns
		$C_L=50$ pF	4.5V	10	20	29	30	ns
		$C_L=150$ pF	4.5V	15	30	38	45	ns
		$C_L=50$ pF	6.0V	10	17	21	25	ns
		$C_L=150$ pF	6.0V	17	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Any Y Output to a Logic Level	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per mux)						
		Enable		30				pF
		Disabled		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2 f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC259/MM74HC259 8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

This device utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM54HC259/MM74HC259 has a single data input (D), 8 latch outputs (Q1–Q8), 3 address inputs (A, B, and C), a common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addressed output. The data is stored when ENABLE transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

If enable is held high and CLEAR is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

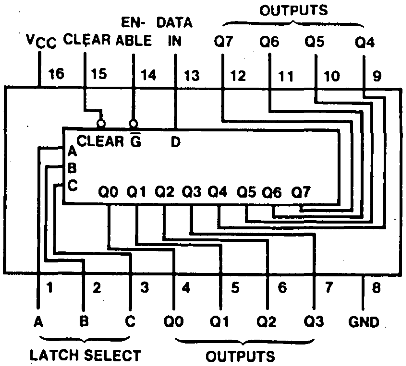
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide supply range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)

Connection Diagram

Dual-In-Line Package



TL/F/5006-1

MM54HC259/MM74HC259

54HC259 (J)   74HC259 (J,N)

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

D = the level at the data input

Q_{i0} the level of Q_i (i = 0, 1 . . . 7, as appropiate) before the indicated steady-state input conditions were established.

Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

($V_{CC}=5.0V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=15$ pF unless otherwise specified.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		20	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		20	35	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		17	27	ns
t_W	Minimum Enable Pulse Width		10	16	ns
t_W	Minimum Clear Pulse Width		10	16	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	ns
t_S	Minimum Setup Time Select or Data to Enable		15	20	ns
t_H	Minimum Hold Time Data or Address to Enable		−2	0	ns

AC Electrical Characteristics $t_r=t_f=6$ ns, $C_L=50$ pF, $V_{CC}=2.0V$–$6.0V$

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V 4.5V 6.0V	60 19 17	180 37 32	225 46 40	250 52 45	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		2.0V 4.5V 6.0V	72 21 18	220 43 37	275 54 46	310 60 52	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		2.0V 4.5V 6.0V	65 27 23	200 40 35	250 50 44	280 58 50	ns ns ns
t_{PHL}	Maximum Propagation Delay Clear to Output		2.0V 4.5V 6.0V	50 18 16	150 31 26	190 39 32	210 44 37	ns ns ns
t_W	Minimum Pulse Width Clear or Enable		2.0V 4.5V 6.0V		80 16 14	100 20 18	120 24 20	ns ns ns
t_S	Minimum Setup Time Address or Data to Enable		2.0V 4.5V 6.0V		100 20 15	125 25 19	150 28 25	ns ns ns
t_H	Minimum Hold Time Address or Data to Enable		2.0V 4.5V 6.0V	−10 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

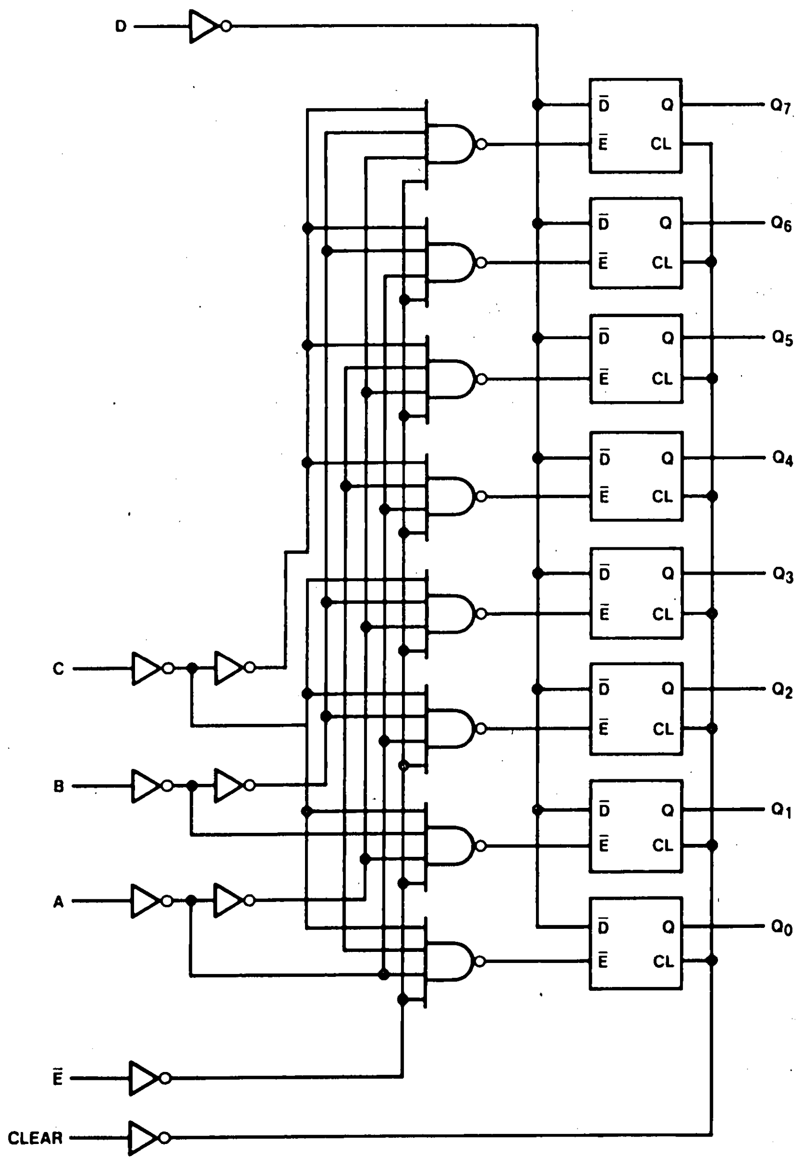
Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

MM54HC259/74HC259

1

Logic Diagram

MM54HC259/MM74HC259



TL/F/5006-2

National Semiconductor

microCMOS

MM54HC266/MM74HC266 Quad 2-Input Exclusive NOR Gate

General Description

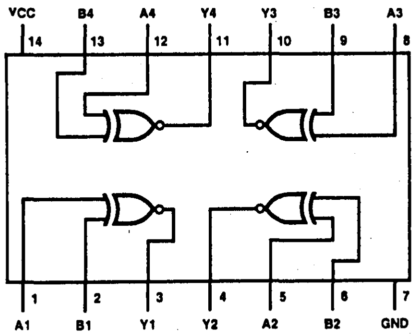
This exclusive NOR gate utilizies microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/MM74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. However, unlike the 'LS266 which is an open collector gate the 'HC266 has standard CMOS push-pull outputs. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads
- Push-pull output

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5330-1

MM54HC266/MM74HC266

54HC266 (J) 74HC266 (J,N)

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC273/MM74HC273 Octal D Flip-Flops With Clear

General Description

These edge triggered flip-flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

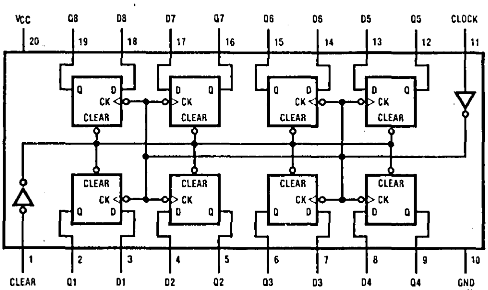
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC273/MM74HC273 is functionally as well as pin compatible to the 54LS273/74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74 series)
- Output drive: 10 LSTTL loads

Connection Diagram

Dual-In-Line Package

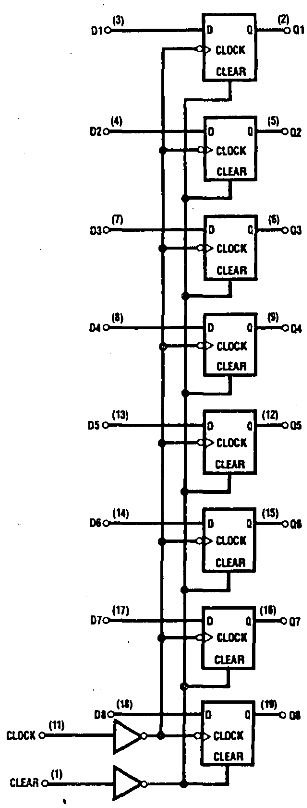


TL/F/5331-1

MM54HC273/MM74HC273

54HC273 (J) 74HC273 (J,N)

Logic Diagram



TL/F/5331-2

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)

L = Low level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		−2	0	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V 4.5V 6.0V	50 21 19	160 32 27	200 40 33	240 48 40	ns ns ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0V 4.5V 6.0V	50 21 19	160 32 27	200 40 33	240 48 40	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	30 10 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V	30 10 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V	−10 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clock or Clear		2.0V 4.5V 6.0V	30 10 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		175				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC280/MM74HC280 9-Bit Odd/Even Parity Generator/Checker

General Description

The MM54HC280/MM74HC280 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits. It possesses the ability to drive 10 LS-TTL loads.

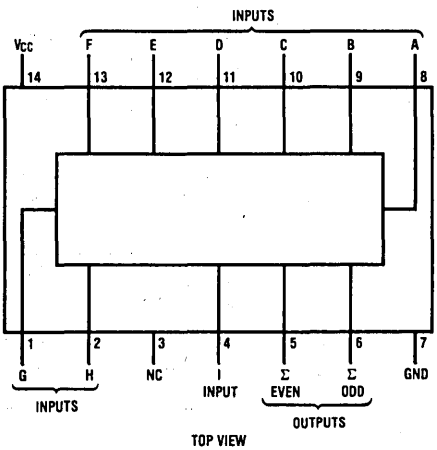
This parity generator/checker features odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading devices. The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 28 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5121-1

MM54HC280/MM74HC280

54HC280 (J) **74HC280 (J,N)**

Function Table

Numbers of Inputs A thru 1 that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L= low level

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		28	35	ns

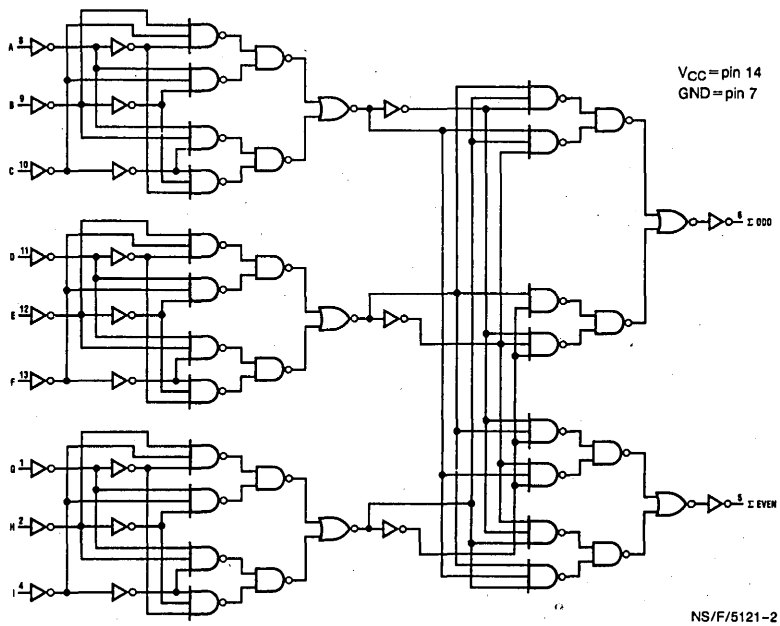
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



'HC280

National Semiconductor

PRELIMINARY

microCMOS

MM54HC283/MM74HC283 4-Bit Binary Adder with Fast Carry

General Description

This full adder performs the addition of two 4-bit binary numbers utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

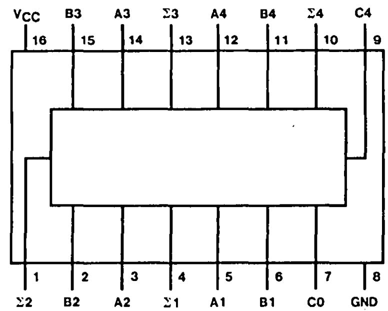
- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide supply range: 2V to 6V
- Low quiescent power consumption: 8 μA at 25°C
- Low input current: <1 μA

Typical Add Times

Two 8-Bit Words	Two 16-Bit Words
25 ns	45 ns

Connection Diagram

Dual-In-Line Package



TL/F/5332-1

MM54HC283/MM74HC283

54HC283 (J) 74HC283 (J,N)

Truth Table

Input				Output					
				When C0 = L			When C0 = H		
						When C2 = L			When C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ1 or Σ2		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ3		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ4		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_i or B_i to Σ_i		15	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		11	17	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_i or B_i to C4		12	17	ns

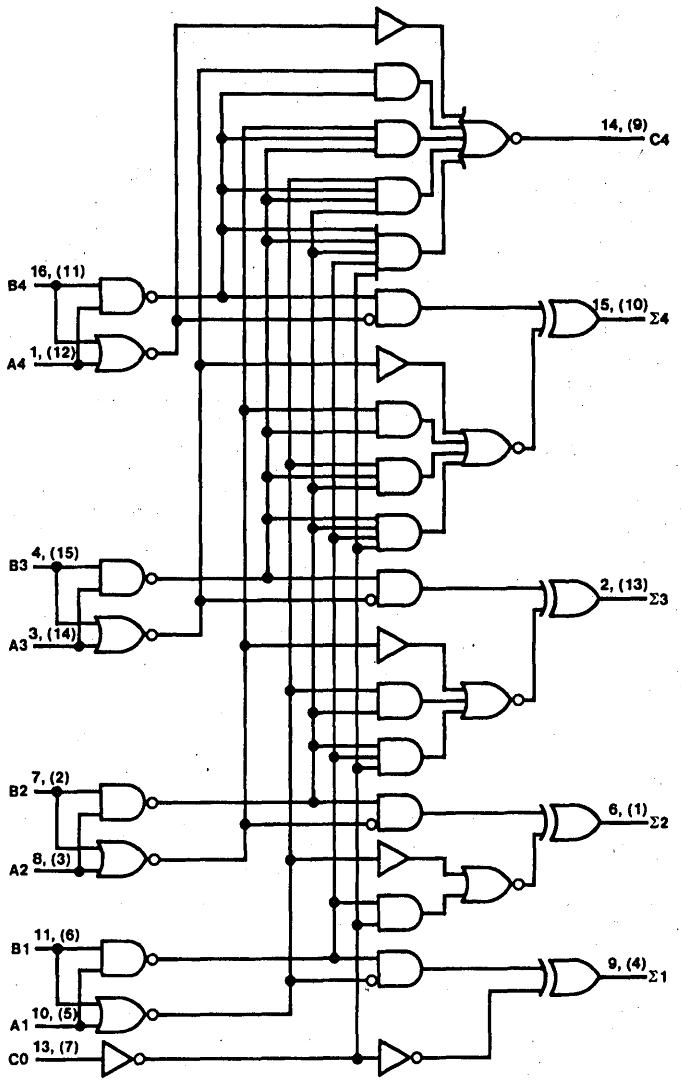
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ1 or Σ2		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ3		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ4		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_i or B_i to Σ_i		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		2.0V	52	125	156	188	ns
			4.5V	17	25	31	38	ns
			6.0V	14	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_i or B_i to C4		2.0V	56	130	162	195	ns
			4.5V	18	26	32	39	ns
			6.0V	14	22	27	33	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	µF
C_{PD}	Power Dissipation Capacitance (Note 5)							µF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5332-2

'HC283

National Semiconductor

PRELIMINARY

microCMOS

MM54HC292/MM74HC292, MM54HC294/MM74HC294 Programmable Frequency Dividers/Digital Timers

General Description

These high speed dividers/timers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These programmable frequency dividers/digital timers contain 31 flip-flops ('HC292) or 15 flip-flops ('HC294) plus 30 gates on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'HC292 and TP on the 'HC294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the truth table below.)

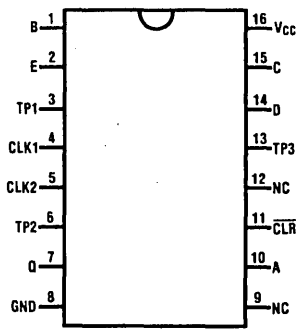
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Count divider chain
- Digitally programmable from 2^2 to 2^n (n = 31 for 'HC292, n = 15 for 'HC294)
- Usable frequency range from DC to 30 MHz
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Easily cascadable
- Output drive capability: 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



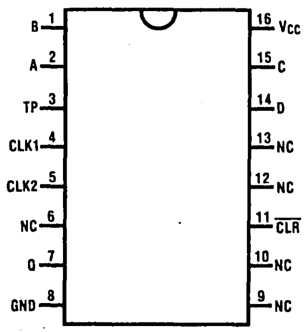
TL/F/5333-1

TOP VIEW

MM54HC292/MM74HC292

54HC292 (J) 74HC292 (J,N)

Dual-In-Line Package



TL/F/5333-2

TOP VIEW

MM54HC294/MM74HC294

54HC294 (J) 74HC294 (J,N)

Truth Table

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to Q Output		80	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to TP Output		80		ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to Q Output		80		ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to TP Output	$\overline{CLR}$ to TP Output	80		ns
t_{REM}	Minimum Removal Time, $\overline{CLR}$ to CLK1, CLK2	$\overline{CLR}$ to CLK1, CLK2	10	20	ns
t_W	Minimum Pulse Width $\overline{CLR}$ to CLK1, CLK2	CLK1, CLK2	10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	5 27 32	4 21 25	3 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to Q Output		2.0V 4.5V 6.0V	300 80 70	600 120 100	750 150 125	900 180 150	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to TP Output		2.0V 4.5V 6.0V	380 80 70				ns ns ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to Q Output		2.0V 4.5V 6.0V	380 80 70				ns ns ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to TP Output		2.0V 4.5V 6.0V	380 80 70				ns ns ns
t_{REM}	Minimum Removal Time $\overline{CLR}$ to CLK1, CLK2		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time (Q Output)		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_W	Minimum Pulse Width $\overline{CLR}$, CLK1, CLK2		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

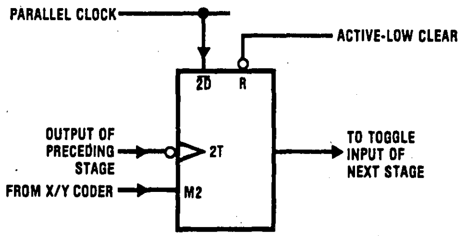
Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Operation

A brief look at the digital timing capabilities will show that with a 1-MHz input frequency, programming for 2^{10} will give a period of 1.024 ms, and 2^{20} will give a period of 1.05s, 2^{26} will give a period of 1.12 min, and 2^{31} will give a period of 35.79 min.

The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode-control inputs of several flip-flops. These flip flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

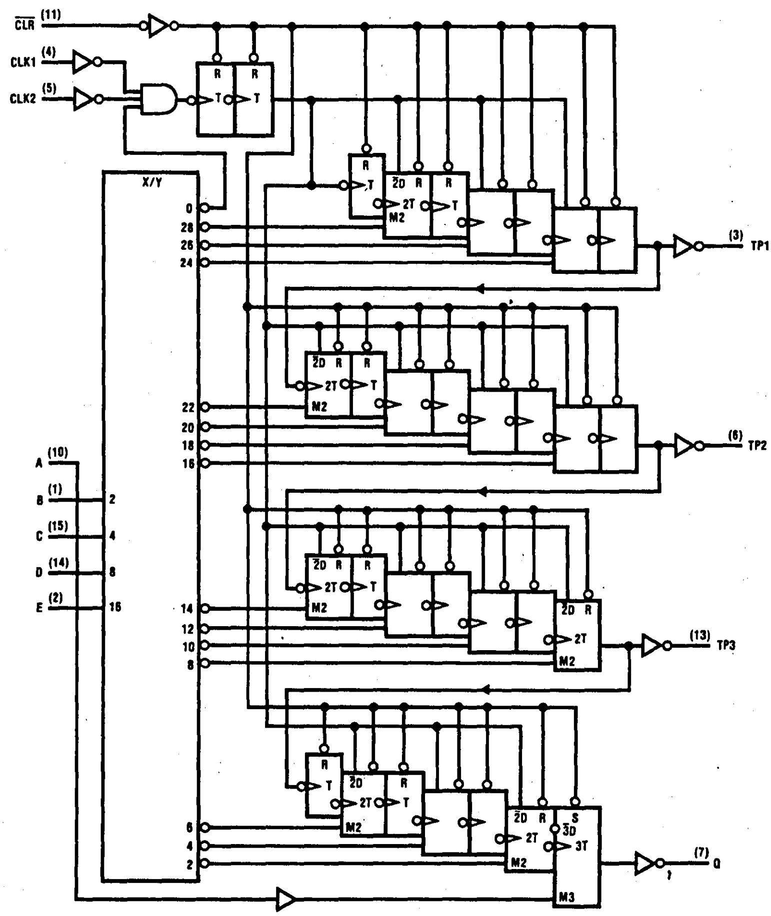
The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of the flip-flop is enabled, and the signal from the parallel clock line ($f_{IN} \div 4$) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.



TL/F/5333-3

Functional Block Diagram (Positive Logic)

'HC292



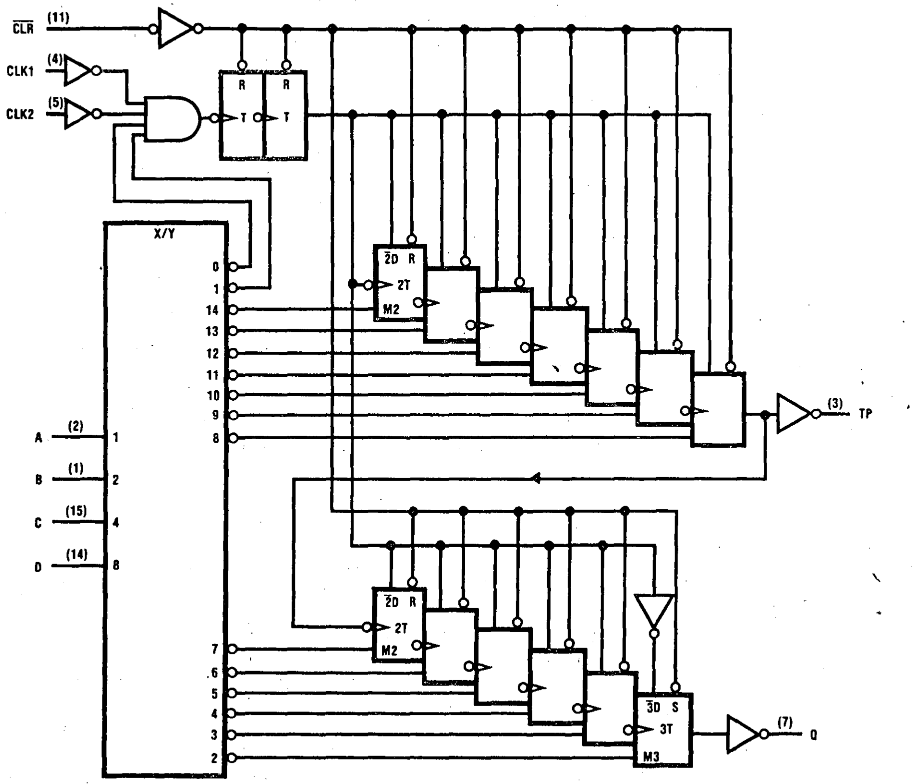
TL/F/5333-6

'HC292 Function Table

Programming Inputs					Frequency Division							
					Q		TP1		TP2		TP3	
E	D	C	B	A	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

Functional Block Diagram (Positive Logic)

'HC294



TL/F/5333-7

'HC294 Function Table

Programming Inputs				Frequency Division			
				Q		TP	
D	C	B	A	Binary	Decimal	Binary	Decimal
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

National Semiconductor

PRELIMINARY

microCMOS

MM54HC298/MM74HC298 Quad 2-Multiplexers With Storage

General Description

These high speed quad two input multiplexers with storage utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Both circuits feature high noise immunity and low power consumption associated with CMOS circuitry, along with speeds comparable to low power Schottky TTL logic.

These circuits are controlled by the signals WORD SELECT and CLOCK. When the WORD SELECT input is taken low Word 1 (A1, B1, C1 and D1) is presented to the inputs of the flip-flops, and when WORD SELECT is high Word 2 (A2, B2, C2 and D2) is presented to the inputs of the flip-flops. The selected word is clocked to the output terminals on the negative edge of the clock pulse.

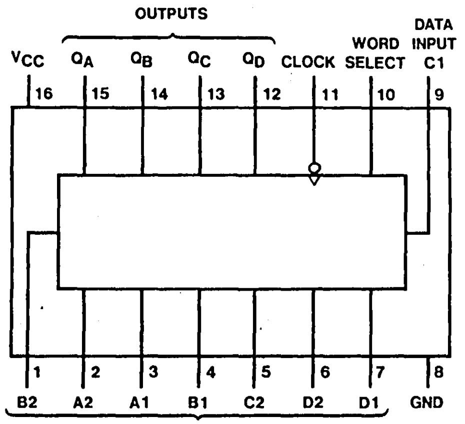
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Clock to output: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum

Connection and Logic Diagrams

Dual-In-Line Package

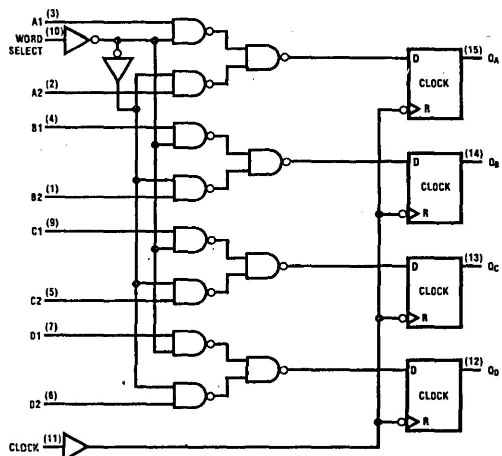


TOP VIEW

TL/F/5334-2

MM54HC298/MM74HC298

54HC298 (J) 74HC298 (J,N)



TL/F/5334-1

Truth Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1, a2, etc. = The level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC2}\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}/$

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Parameter			Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Ouput			21	32	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	32	ns
t_W	Width of Clock Pulse, High or Low Level			10	16	ns
t_{SETUP}	Setup Time	Data		5	20	ns
		Word Select		10	20	
t_{HOLD}	Hold Time	Data		−2	0	ns
		Word Select		−2	0	

AC Electrical Characteristics

$C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter		Conditions	V_{CC}	54HC/74HC $T_A=25°C$ Typ	54HC/74HC $T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output			2.0V 4.5V 6.0V	75 25 20	185 37 31	231 46 39	278 56 47	ns ns ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output			2.0V 4.5V 6.0V	75 25 20	185 37 31	231 46 39	278 56 47	ns ns ns
t_W	Width of Clock Pulse High or Low Level			2.0V 4.5V 6.0V	35 10 9	80 16 14	100 20 18	120 24 21	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			2.0V 4.5V 6.0V	90 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_{SETUP}	Set-up Time	Data		2.0V 4.5V 6.0V	35 5 4	100 20 17	125 25 21	150 30 25	ns ns ns
		Word Select		2.0V 4.5V 6.0V	40 10 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_{HOLD}	Hold Time	Data		2.0V 4.5V 6.0V	−10 −3 −2	0 0 0	0 0 0	0 0 0	ns ns ns
		Word Select		2.0V 4.5V 6.0V	−10 −3 −2	0 0 0	0 0 0	0 0 0	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)								pF
C_{IN}	Maximum Input Capacitance				5	10	10	10	pF

Typical Applications

Figure 1 illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the MM54HC298/MM74HC298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

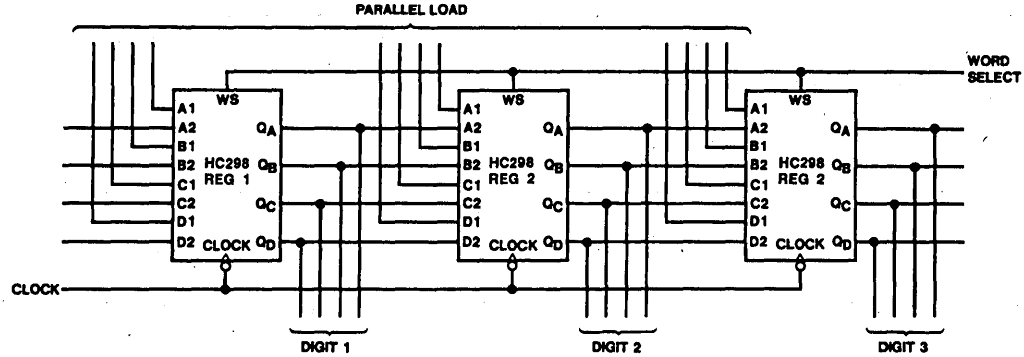


FIGURE 1

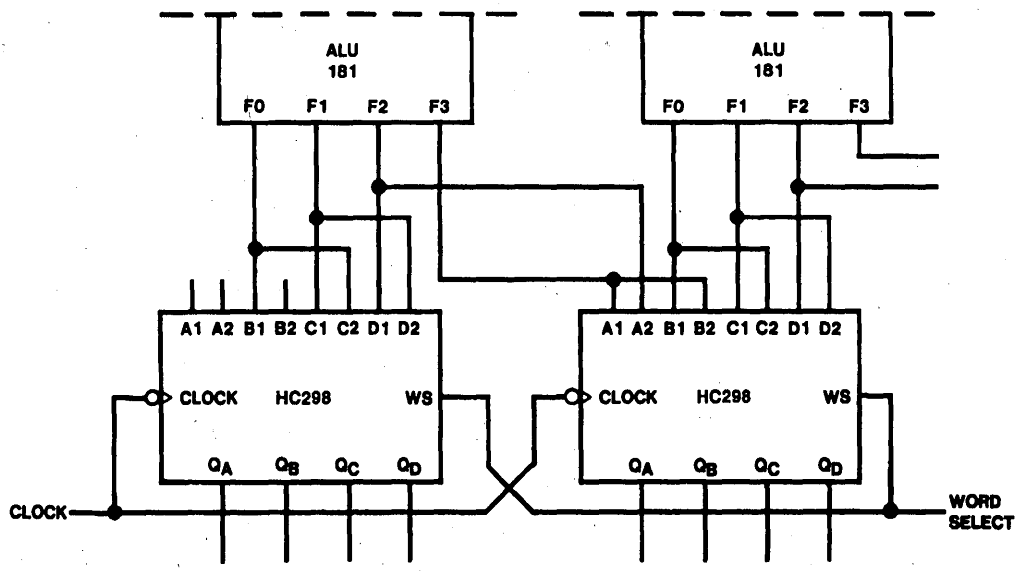


FIGURE 2

National Semiconductor

microCMOS

MM54HC299/MM74HC299 8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HC299/MM74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S0 and S1 high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

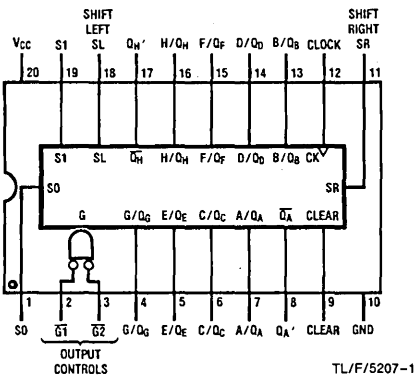
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency 40 MHz
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HC)
- High output drive for bus applications
- Low quiescent current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5207-1

TOP VIEW

MM54HC299/MM74HC299

54HC299 (J) 74HC299 (J,N)

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X	H	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA ($Q_{A'}$, $Q_{H'}$) ±35 mA (others)
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
	$Q_{A'}$ & $Q_{H'}$ Outputs	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA $\|I_{OUT}\|\le 5.2$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V V
	A/Q_A thru H/Q_H Outputs	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 6.0$ mA $\|I_{OUT}\|\le 7.8$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
	$Q_{A'}$ and $Q_{H'}$ Outputs	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4$ mA $\|I_{OUT}\|\le 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V V
	A/Q_A thru H/Q_H Outputs	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 6$ mA $\|I_{OUT}\|\le 7.8$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±0.5	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=45$ pF

Symbol	Parameter		Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			40	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $Q_{A'}$ or $Q_{H'}$			25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to $Q_{A'}$ or $Q_{H'}$			39	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_A–Q_H		$C_L=45$ pF	25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A–Q_H		$C_L=45$ pF	28	40	ns
t_{PZL}, t_{PZH}	Maximum Enable Time		$C_L=45$ pF $R_L=1$ kΩ	10	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time		$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_S	Minimum Set-Up Time	Select			20	ns
		Data			20	
t_H	Minimum Hold Time	Select			0	ns
		Data			0	
t_W	Minimum Pulse Width			12	20	ns
t_{REM}	Clear Removal Time				10	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3.5	MHz
			4.5V		25	20	18	MHz
			6.0V		29	23	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $Q_{A'}$ or $Q_{H'}$		2.0V	15	170	210	240	ns
			4.5V	27	38	48	54	ns
			6.0V	25	35	44	49	ns
t_{PHL}	Maximum Propagation Delay Clear to $Q_{A'}$ or $Q_{H'}$		2.0V	70	200	250	280	ns
			4.5V	30	44	55	62	ns
			6.0V	26	38	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_A–Q_H	$C_L=50$ pF	2.0V	65	170	210	240	ns
		$C_L=150$ pF	2.0V	100	206	260	295	ns
		$C_L=50$ pF	4.5V	27	38	48	54	ns
		$C_L=150$ pF	4.5V	34	46	57	66	ns
		$C_L=50$ pF	6.0V	25	35	44	49	ns
		$C_L=150$ pF	6.0V	31	39	49	55	ns
t_{PHL}	Maximum Propagation Delay Clear to Q_A–Q_H	$C_L=50$ pF	2.0V	70	200	250	280	ns
		$C_L=150$ pF	2.0V	110	236	295	325	ns
		$C_L=50$ pF	4.5V	30	44	55	62	ns
		$C_L=150$ pF	4.5V	37	52	65	75	ns
		$C_L=50$ pF	6.0V	26	38	46	52	ns
		$C_L=150$ pF	6.0V	32	46	57	64	ns

AC Electrical Characteristic (Continued)

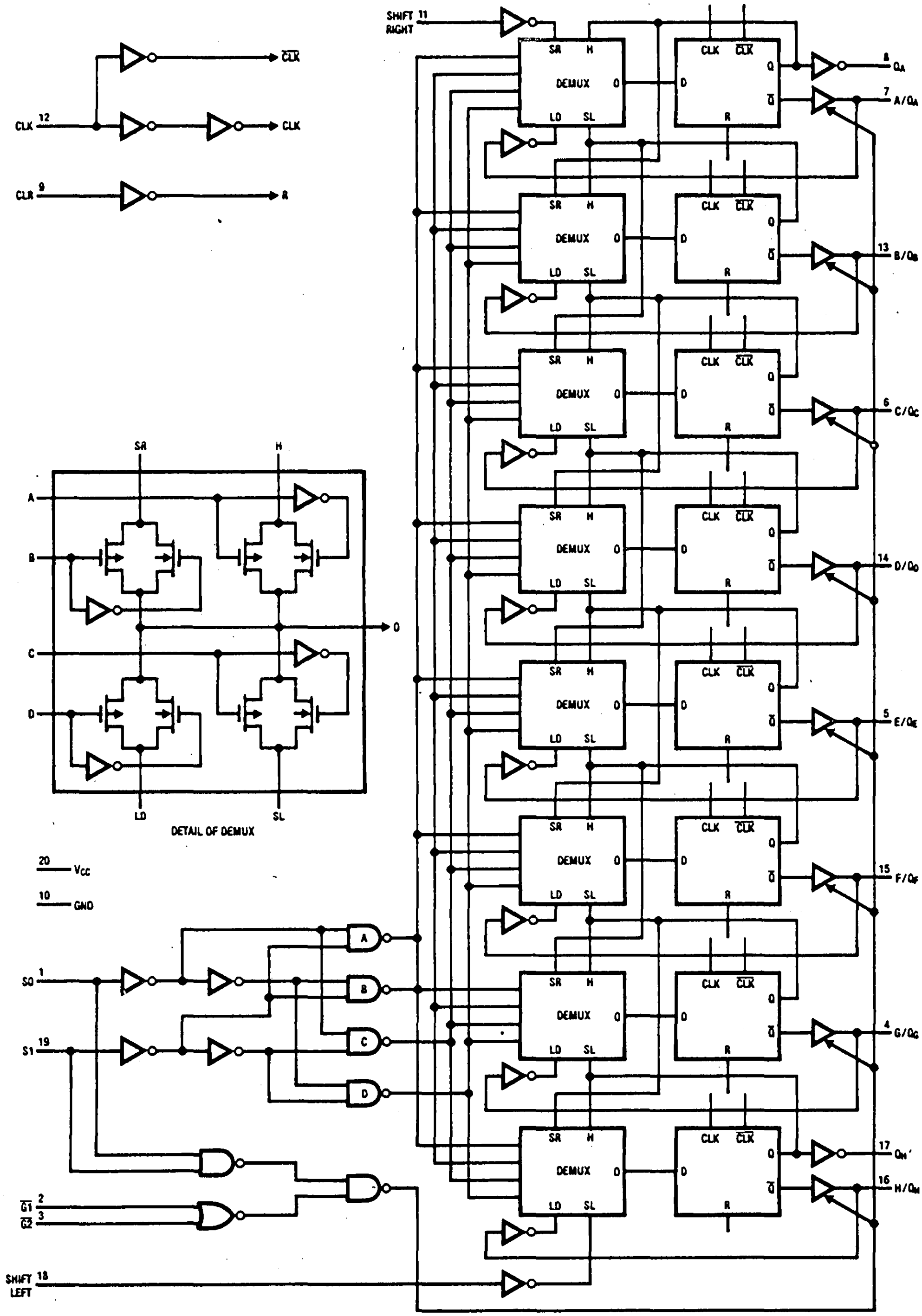
$C_L = 50$ pF ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	74HC $T_A = -40$ to 85°C Guaranteed Limits	54HC $T_A = -55$ to 125°C Guaranteed Limits	Units
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	70	160	200	225	ns
		$C_L = 150$ pF	2.0V	90	220	275	310	ns
		$C_L = 50$ pF	4.5V	22	32	40	45	ns
		$C_L = 150$ pF	4.5V	30	44	55	62	ns
		$C_L = 50$ pF	6.0V	19	28	34	38	ns
		$C_L = 150$ pF	6.0V	24	47	47	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ	2.0V	70	160	200	225	ns
		$C_L = 50$ pF	4.5V	22	32	40	45	ns
			6.0V	19	28	34	38	ns
t_S	Minimum Set Up Time, Data Select S_L or S_R		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data Select, S_L or S_R		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{REM}	Minimum Clear Removal Time		2.0V		10	10	10	ns
			4.5V		10	10	10	ns
			6.0V		10	10	10	ns
t_W	Minimum Pulse Width, Clock and Clear		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_r, t_f	Maximum Input Rise and Fall Time				500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance	Outputs Enabled		240				pF
		Outputs Disabled		110				pF
C_{IN}	Maximum Input Capacitance Capacitance			5	10	10	10	pF
C_{OUT}	Maximum TRI-STATE Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5207-2

National Semiconductor

microCMOS

MM54HC354/MM74HC354, MM54HC356/MM74HC356 8-Channel TRI-STATE® Multiplexers with Latches

General Description

The MM54HC354/MM74HC354 and MM54HC356/MM74HC356 utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They exhibit the high noise immunity and low power dissipation of standard CMOS integrated circuits, along with the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data select address is stored in transparent latches that are enabled by a low level address on pin 11, $\overline{SC}$. Data on the 8 input lines is stored in a parallel input/output register which in the MM54HC354/MM74HC354 is composed of 8 transparent latches enabled by a low level on pin 9, $\overline{DC}$, and in the MM54HC356/MM74HC356 is composed of 8 edge-triggered flip-flops, clocked by a low to high transition on pin 9, CLK. Both true (Y) and complementary (W) TRI-STATE outputs are available on both devices.

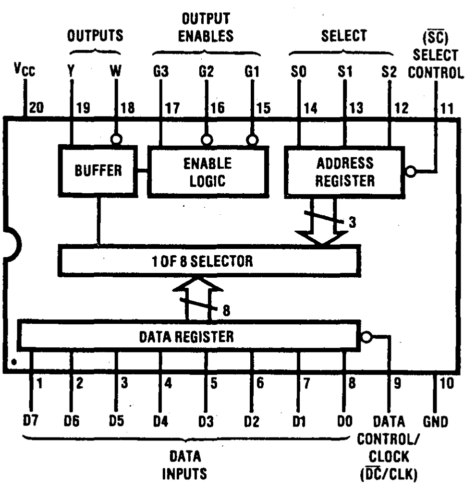
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS-TTL logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Transparent latches on data select inputs
- Choice of data registers:
  Transparent ('354)
  Edge-triggered ('356)
- TRI-STATE complementary outputs with fan-out of 15 LS-TTL loads
- Typical propagation delay:
  Data to output ('354): 32 ns
  Clock to output ('346): 35 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5208–1

MM54HC354/MM74HC354, MM54HC356/MM74HC356

54HC354 (J) 74HC354 (J,N)
54HC356 (J) 74HC356 (J,N)

Function Table

Inputs								Outputs	
Select†			Data Control 'HC354	Clock 'HC356	Output Enables				
S1	S2	S0	$\overline{DC}$	CLK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0...D7 = the level steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'HC356
$D0_n$...$D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.
†This column shows the input address set-up with $\overline{SC}$ low.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| < 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{G1}=V_{CC}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

MM54HC354/MM74HC354

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	$C_L=45$ pF	32	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	$C_L=45$ pF	38	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L=45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L=45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	23	32	ns
t_S	Minimum Set-Up Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or $\overline{DC}$		10	15	ns

MM54HC356/MM74HC356

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L=45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L=45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	23	32	ns
t_S	Minimum Set-Up Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or CLK		10	15	ns

AC Electrical Characteristics

$V_{CC} = 2.0–6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified) (Note 6)

MM54HC354/MM74HC354

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
					Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	$C_L = 50$ pF	2.0V	90	235	294	352	ns
		$C_L = 150$ pF	2.0V	100	275	344	412	ns
		$C_L = 50$ pF	4.5V	35	47	59	70	ns
		$C_L = 150$ pF	4.5V	40	55	68	83	ns
		$C_L = 50$ pF	6.0V	26	40	50	60	ns
		$C_L = 150$ pF	6.0V	32	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	$C_L = 50$ pF	2.0V	115	270	337	405	ns
		$C_L = 150$ pF	2.0V	125	310	387	465	ns
		$C_L = 50$ pF	4.5V	40	54	68	82	ns
		$C_L = 150$ pF	4.5V	46	62	78	93	ns
		$C_L = 50$ pF	6.0V	32	46	58	69	ns
		$C_L = 150$ pF	6.0V	38	52	66	78	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L = 50$ pF	2.0V	120	285	356	427	ns
		$C_L = 150$ pF	2.0V	130	325	406	488	ns
		$C_L = 50$ pF	4.5V	42	57	71	86	ns
		$C_L = 150$ pF	4.5V	50	65	81	97	ns
		$C_L = 50$ pF	6.0V	34	48	60	72	ns
		$C_L = 150$ pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L = 50$ pF	2.0V	120	300	375	450	ns
		$C_L = 150$ pF	2.0V	110	340	425	510	ns
		$C_L = 50$ pF	4.5V	45	60	75	90	ns
		$C_L = 150$ pF	4.5V	52	68	85	102	ns
		$C_L = 50$ pF	6.0V	36	51	64	77	ns
		$C_L = 150$ pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	50	125	156	188	ns
		$C_L = 150$ pF	2.0V	60	165	206	248	ns
		$C_L = 50$ pF	4.5V	18	25	31	38	ns
		$C_L = 150$ pF	4.5V	25	33	41	49	ns
		$C_L = 50$ pF	6.0V	15	21	26	32	ns
		$C_L = 150$ pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ	2.0V	68	165	206	248	ns
		$C_L = 50$ pF	4.5V	24	33	40	46	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Set-Up Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	6	50	60	75	ns
			4.5V	3	10	13	15	ns
			6.0V	3	10	13	15	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ or $\overline{DC}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	27	ns
			6.0V	10	15	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						
		Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

AC Electrical Characteristics

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified) (Note 6)

MM54HC356/MM74HC356

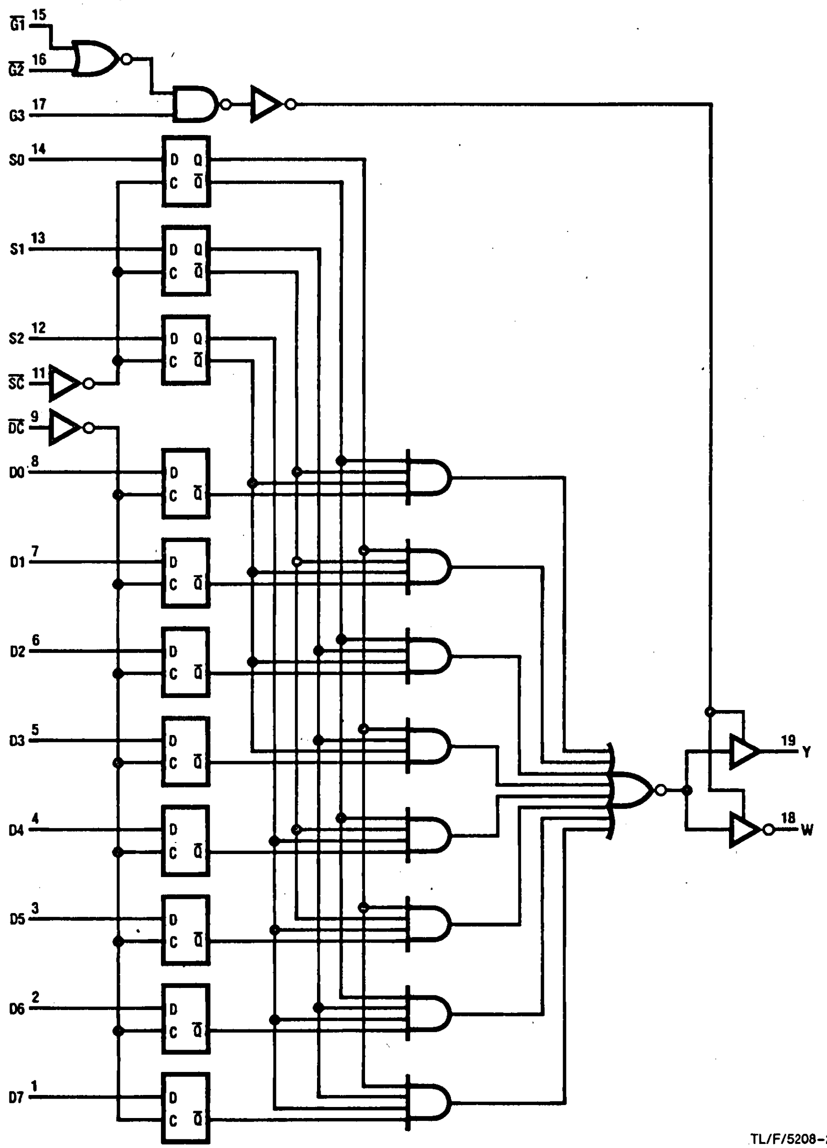
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	C_L = 50 pF	2.0V	100	225	318	338	ns
		C_L = 150 pF	2.0V	110	295	369	442	ns
		C_L = 50 pF	4.5V	36	51	63	76	ns
		C_L = 150 pF	4.5V	42	59	73	90	ns
		C_L = 50 pF	6.0V	28	43	53	64	ns
		C_L = 150 pF	6.0V	34	50	63	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	41	49	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Set-Up Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	6	50	50	50	ns
			4.5V	3	10	10	10	ns
			6.0V	3	10	10	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ to CLK		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	10	15	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						
		Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

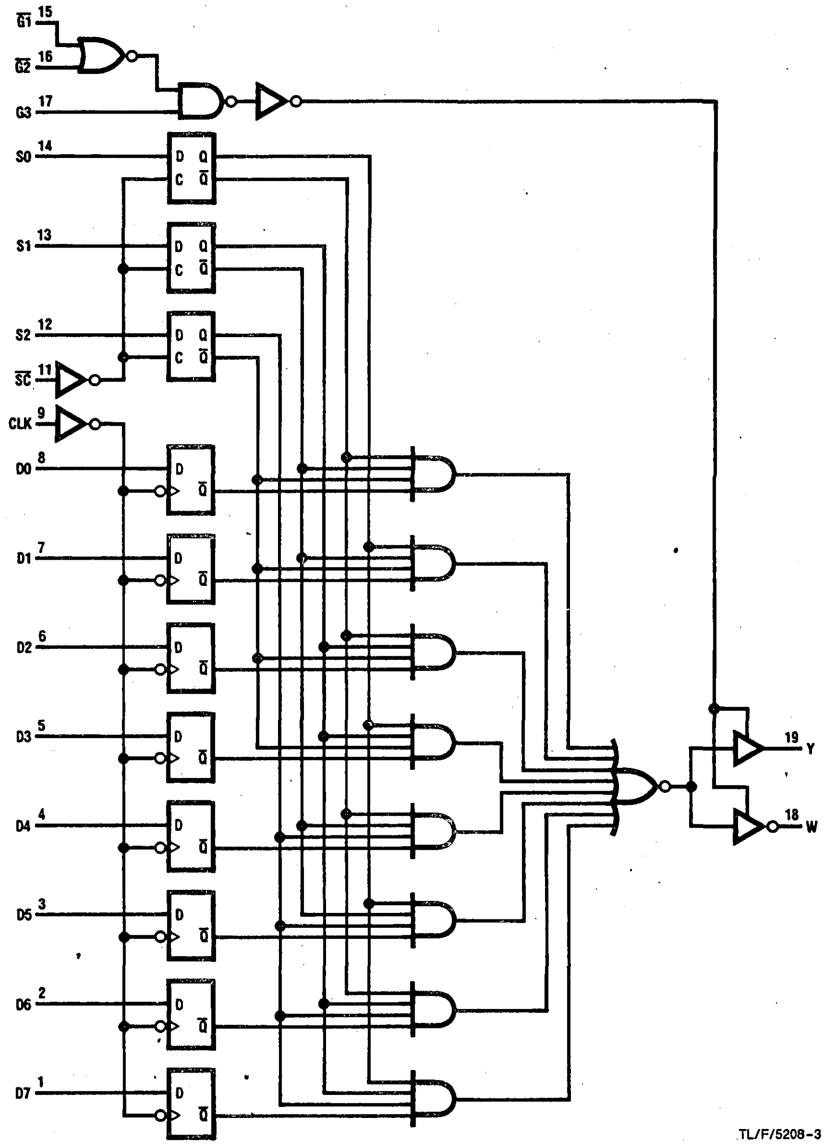
HC354



TL/F/5208-2

Logic Diagram

HC356



TL/F/5208-3

National Semiconductor

microCMOS

MM54HC365/MM74HC365 Hex TRI-STATE® Buffer
MM54HC366/MM74HC366 Inverting Hex TRI-STATE Buffer
MM54HC367/MM74HC367 Hex TRI-STATE Buffer
MM54HC368/MM74HC368 Inverting Hex TRI-STATE Buffer

General Description

These TRI-STATE buffers are general purpose high speed inverting and non-inverting buffers that utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. All 4 circuits are capable of driving up to 15 low power Schottky inputs.

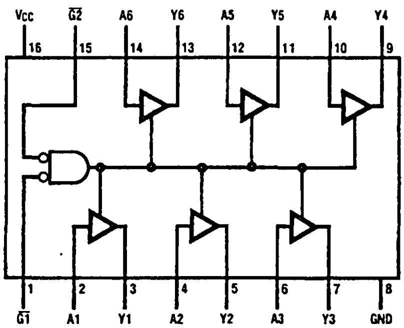
The MM54/74HC366 and the MM54/74HC368 are inverting buffers, where as the MM54/74HC365 and the MM54/74HC367 are non-inverting buffers. The MM54/74HC365 and the MM54/MM74HC366 have two TRI-STATE control inputs ($\overline{G1}$ and $\overline{G2}$) which are NORed together to control all six gates. The MM54/74HC367 and the MM54/74HC368 also have two output enables, but one enable ($\overline{G1}$) controls 4 gates and the other ($\overline{G2}$) controls the remaining 2 gates.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74 series)
- Output drive capability: 15 LS-TTL loads

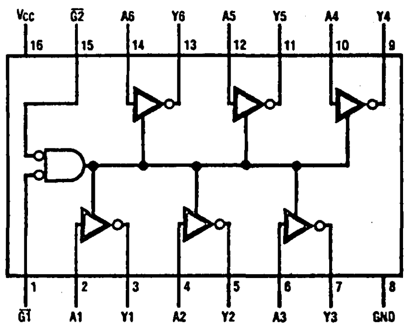
Connection Diagrams Dual-In-Line Package



TL/F/5209-1

MM54HC365/MM74HC365

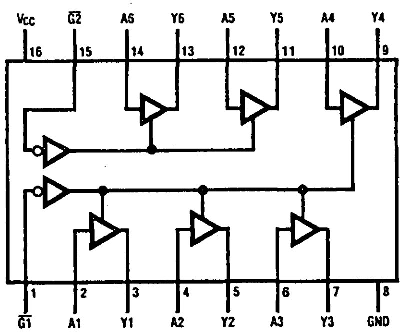
54HC365 (J) 74HC365 (J,N)



TL/F/5209-2

MM54HC366/MM74HC366

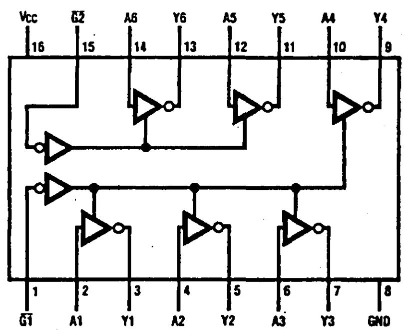
54HC366 (J) 74HC366 (J,N)



TL/F/5209-3

MM54HC367/MM74HC367

54HC367 (J) 74HC367 (J,N)



TL/F/5209-4

MM54HC368/MM74HC368

54HC368 (J) 74HC368 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{G}=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC365/MM74HC365

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	15	22	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ, $C_L=45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ, $C_L=5$ pF	25	36	ns

AC Electrical Characteristics MM54HC365/MM74HC365

$V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	35	105	130	150	ns
		$C_L=150$ pF	2.0V	45	135	168	205	ns
		$C_L=50$ pF	4.5V	14	24	30	36	ns
		$C_L=150$ pF	4.5V	17	29	36	45	ns
		$C_L=50$ pF	6.0V	11	19	24	28	ns
		$C_L=150$ pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	90	230	287	345	ns
		$C_L=150$ pF	2.0V	98	245	306	367	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	38	53	66	80	ns
		$C_L=50$ pF	6.0V	25	35	43	52	ns
		$C_L=150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ, $C_L=50$ pF	2.0V	58	175	218	260	ns
			4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

AC Electrical Characteristics MM54HC366/MM74HC366

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	36	ns

AC Electrical Characteristics MM54HC366/MM74HC366

$V_{CC}=2.0–6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	90	230	287	345	ns
		$C_L=150$ pF	2.0V	98	245	306	367	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	38	53	66	80	ns
		$C_L=50$ pF	6.0V	25	35	43	52	ns
		$C_L=150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	58	175	218	260	ns
			4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

AC Electrical Characteristics MM54HC367/MM74HC367

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	22	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	33	ns

AC Electrical Characteristics MM54HC367/MM74HC367

$V_{CC}=2.0\text{–}6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	35	105	130	150	ns
		$C_L=150$ pF	2.0V	45	135	168	205	ns
		$C_L=50$ pF	4.5V	14	24	30	36	ns
		$C_L=150$ pF	4.5V	17	29	36	45	ns
		$C_L=50$ pF	6.0V	11	19	24	28	ns
		$C_L=150$ pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	69	172	216	250	ns
		$C_L=150$ pF	2.0V	75	187	233	280	ns
		$C_L=50$ pF	4.5V	24	38	47	57	ns
		$C_L=150$ pF	4.5V	29	46	57	69	ns
		$C_L=50$ pF	6.0V	22	35	43	52	ns
		$C_L=150$ pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	117	146	220	ns
			4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

Inputs $\overline{G}$	Inputs A	Output Y
H	X	Z
L	H	H
L	L	L

AC Electrical Characteristics MM54HC368/MM74HC368

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	11	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ, $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	33	ns

AC Electrical Characteristics MM54HC368/MM74HC368

$V_{CC}=2.0–6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	69	172	216	250	ns
		$C_L=150$ pF	2.0V	75	187	233	280	ns
		$C_L=50$ pF	4.5V	24	38	47	57	ns
		$C_L=150$ pF	4.5V	29	46	57	69	ns
		$C_L=50$ pF	6.0V	22	35	43	52	ns
		$C_L=150$ pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	117	146	220	ns
			4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			10	20	20	20	pF

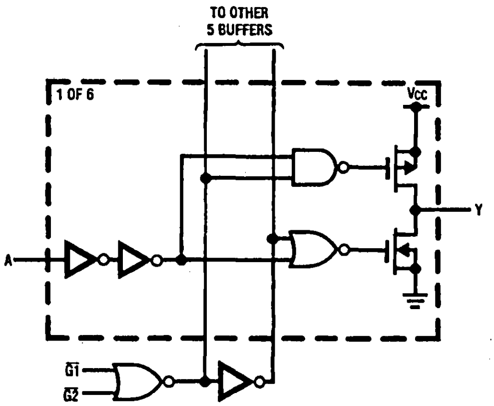
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

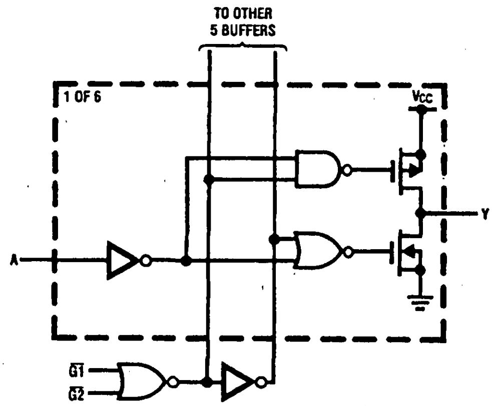
Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Logic Diagrams



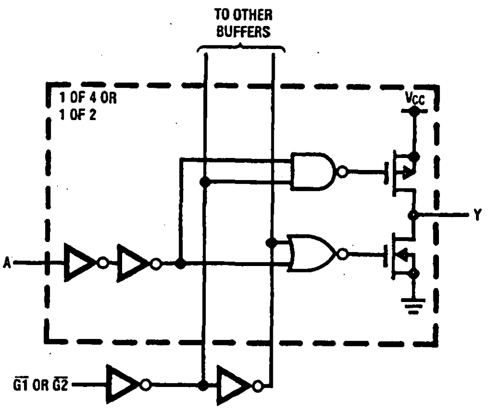
TL/F/5209-5

MM54HC365/MM74HC365



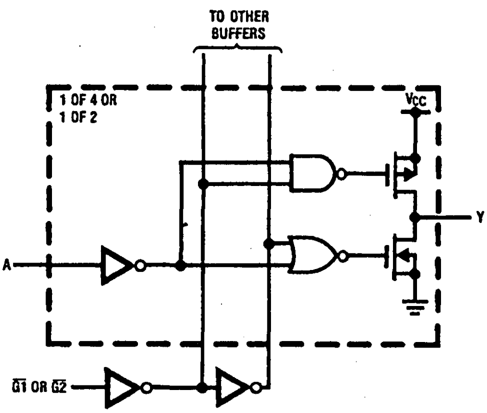
TL/F/5209-6

MM54HC366/MM74HC366



TL/F/5209-7

MM54HC367/MM74HC367



TL/F/5209-8

MM54HC368/MM74HC368

National Semiconductor

microCMOS

MM54HC373/MM74HC373 TRI-STATE® Octal D-Type Latch

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

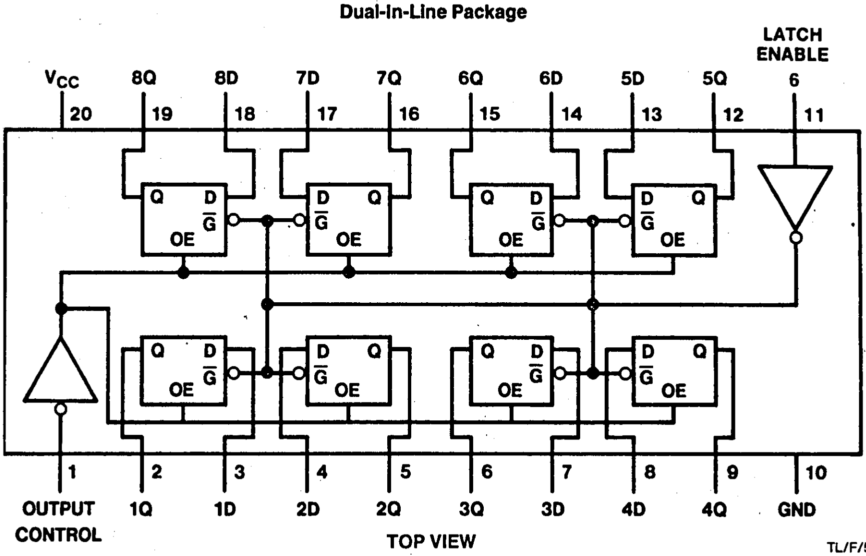
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5335-1

MM54HC373/MM74HC373

54HC373 (J) 74HC373 (J,N)

Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	H
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$ or V_{IL}, OC=V_{IH} $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	50	150	188	225	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V	5	25	31	38	ns
			4.5V	2	5	6	8	ns
			6.0V	2	5	6	8	ns
t_H	Minimum Hold Time		2.0V	20	50	60	75	ns
			4.5V	6	10	13	20	ns
			6.0V	6	10	13	20	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch)						
		$OC=V_{CC}$		30				pF
		$OC=GND$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

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MM54HC374/MM74HC374 TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed Octal D-Type Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

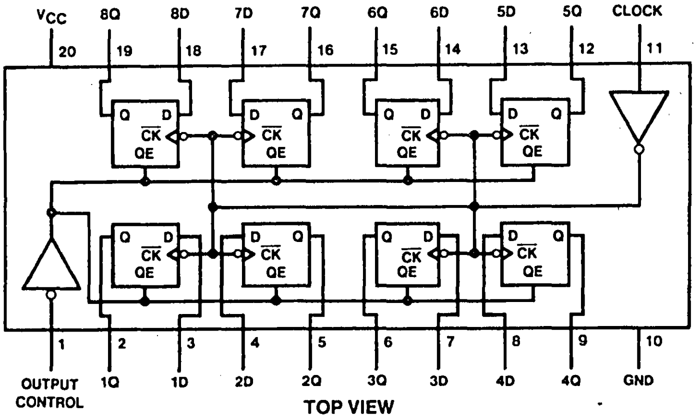
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5336-1

MM54HC374/MM74HC374

54HC374 (J) 74HC374 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$, OC=V_{IH} $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=$ kΩ $C_L=45$ pF	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=5$ pF	17	25	ns
t_S	Minimum Set Up Time			20	ns
t_H	Minimum Hold Time			5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0–6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V 4.5V 6.0V		6 30 35	5 24 28	4 20 23	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	68 110	180 230	225 288	270 345	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	22 30	36 46	45 57	48 69	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	20 28	31 40	39 50	46 60	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	50 80	150 200	189 250	225 300	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	21 30	30 40	37 50	45 60	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	19 26	26 35	31 44	39 53	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	50 21 19	150 30 26	189 37 31	225 45 39	ns ns ns
t_S	Minimum Set Up Time		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time		2.0V 4.5V 6.0V		25 5 5	31 5 5	38 5 5	ns ns ns
t_W	Minimum Pulse Width		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop) $OC=V_{CC}$ $OC=GND$		 30 50				 pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC390/MM74HC390 Dual 4-Bit Decade Counter MM54HC393/MM74HC393 Dual 4-Bit Binary Counter

General Description

These counter circuits contain independent ripple carry counters and utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. The MM54HC390/MM74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter. The MM54HC393/M74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

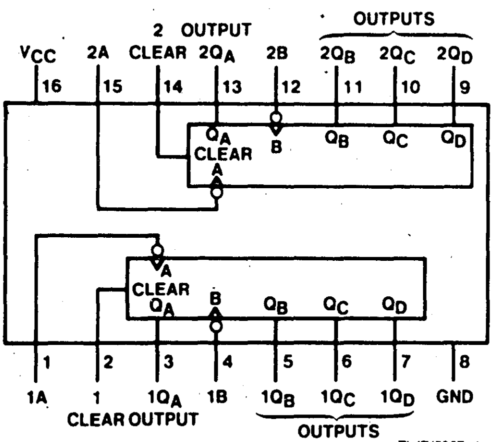
Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. These counters are functionaly as well as pin equivalent to the 54LS390/74LS390 and the 54LS393/74LS393, respectively. All inputs are protected from damage due to static discharge by diodes to V_C and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

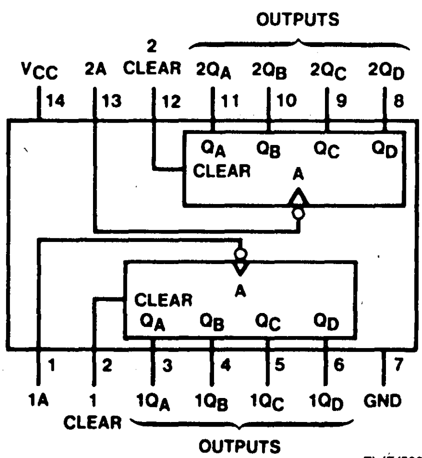


TL/F/5337-1

MM54HC390/MM74HC390

54HC390 (J) 74HC390 (J,N)

Dual-In-Line Package



TL/F/5337-2

MM54HC393/MM74HC393

54HC393 (J) 74HC393 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC390/MM74HC390

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency, Clock A or B		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A connected to Clock B)		32	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		15	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		20	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Output		15	28	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_W	Minimum Pulse Width, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A connected to Clock B)		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		2.0V	50	130	160	195	ns
			4.5V	16	26	33	39	ns
			6.0V	13	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		2.0V	60	185	230	280	ns
			4.5V	20	37	46	55	ns
			6.0V	17	32	40	48	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		2.0V	55	165	210	250	ns
			4.5V	17	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

AC Electrical Characteristics MM54HC393/MM74HC393

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_B		19	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C		23	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_D		27	50	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		15	28	ns
t_{REM}	Minimum Removal Time		−2	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

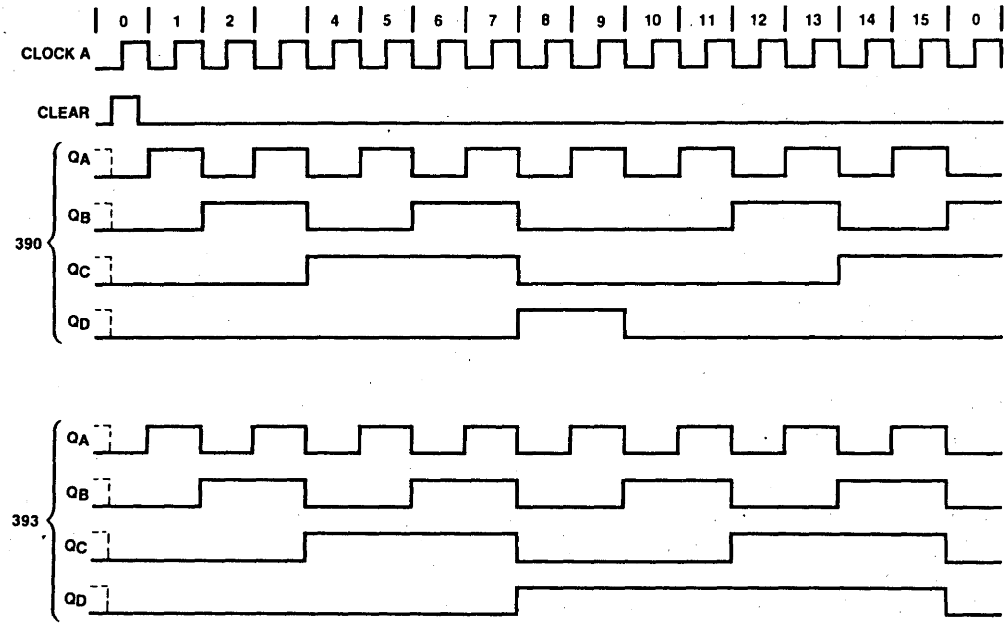
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_B		2.0V	68	190	240	285	ns
			4.5V	23	38	47	57	ns
			6.0V	20	32	40	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_C		2.0V	90	240	300	360	ns
			4.5V	30	48	60	72	ns
			6.0V	26	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_D		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}	Maximum Propagation Delay Clear to any Q		2.0V	54	165	210	250	ns
			4.5V	18	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Clear Removal Time		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		42				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Timing Waveforms



TL/F/5337-3

National Semiconductor

microCMOS

MM54HC423A/MM74HC423A Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC423A high speed monostable multivibrators (one shots) utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC423 cannot be triggered from clear.

The 'HC423A is retriggerable. That is it may be triggered repeatedly while its outputs are generating a pulse and the pulse will be extended.

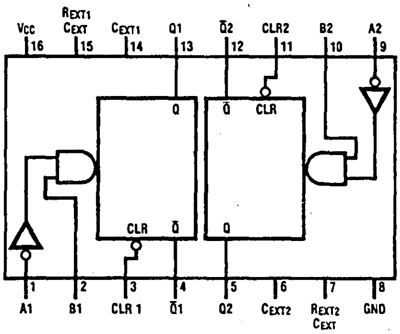
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})\ (C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: $\pm$5% (typ)
- Schmitt Trigger A & B inputs allow infinite rise and fall times on these inputs

Connection Diagram

Dual-In-Line Package

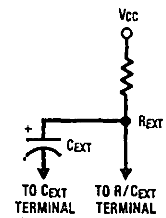


TOP VIEW TL/F/5206-1

MM54HC423A/MM74HC423A

54HC423 (J) 74HC423 (J,N)

Timing Component



TL/F/5206-2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⊓ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5V to +7.0V
DC Input Voltage(V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.96	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 4$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN}=V_{CC} or GND	5.0V		0.5	5.0	5.0	μA
I_{IN}	Maximum Input Current (All other pins)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Standby)	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN}=V_{CC} or GND R/C_{EXT}=0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

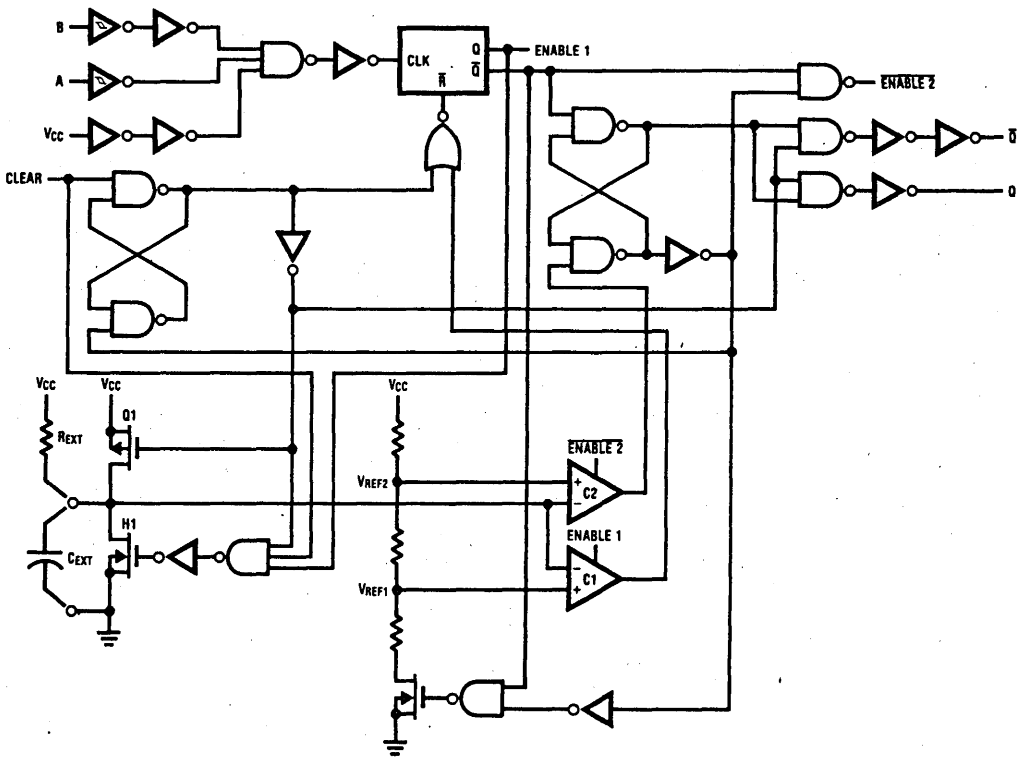
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (Unless otherwise specified)

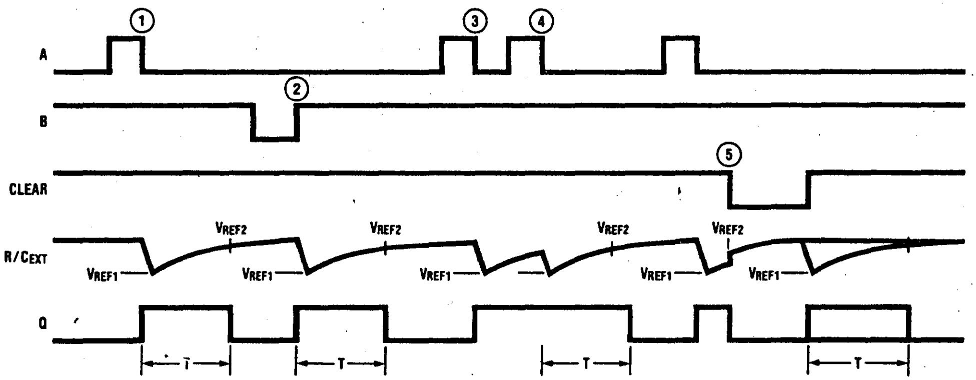
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V	0	0	0	0	ns
				4.5V	0	0	0	0	ns
				6.0V	0	0	0	0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5				μs
		$R_{EXT}=2$ kΩ		4.5V	450				ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380				ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9			ms
			Max	4.5V	1	1.1			ms
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				6	10	10	10	pF

Logic Diagram



TL/F/5206-5

Theory of Operation



TL/F/5206-6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING

FIGURE 1

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one-shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the one-shot in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}②.)

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC423 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

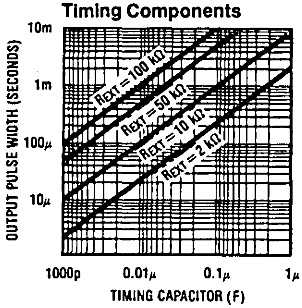
RETRIGGER OPERATION

The 'HC423A is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

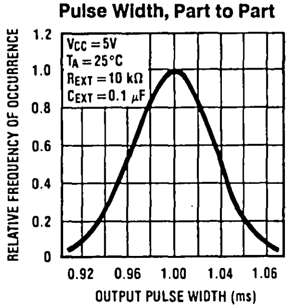
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



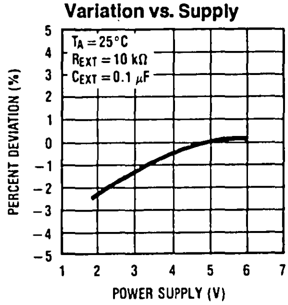
TL/F/5206-7

Typical Distribution of Output Pulse Width, Part to Part



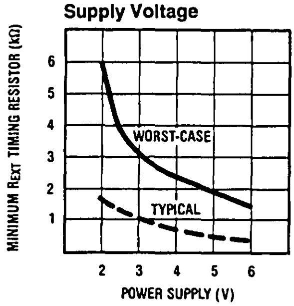
TL/F/5206-8

Typical 1ms Pulse Width Variation vs. Supply



TL/F/5206-9

Minimum R_{EXT} vs. Supply Voltage



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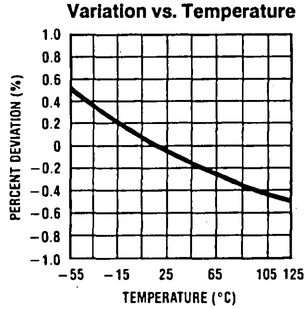
Typical 1ms Pulse Width Variation vs. Temperature



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Note: R and C are not subjected to temperature. The C is polypropolyne.

National Semiconductor

microCMOS

MM54HC521/MM74HC521 8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

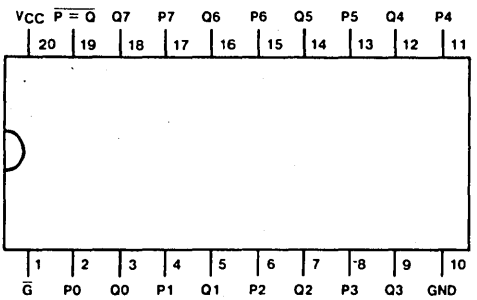
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 series)
- Large output current: 4 mA (74 series)

Connection and Logic Diagrams

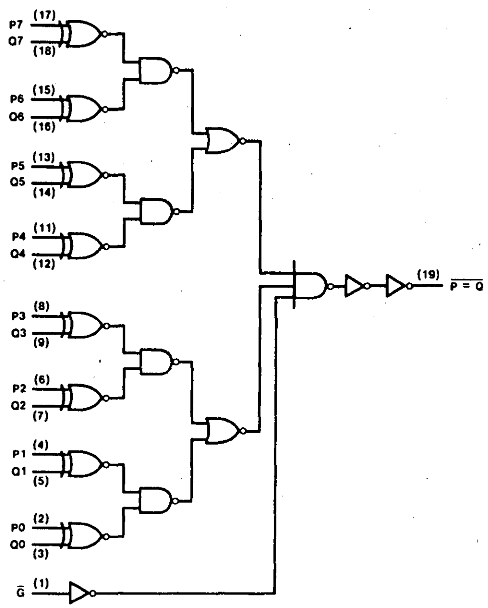
Dual-In-Line Package



TOP VIEW TL/F/5018-1

MM54HC521/MM74HC521

54HC521 (J) 74HC521 (J,N)



TL/F/5018-2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC533/MM74HC533 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

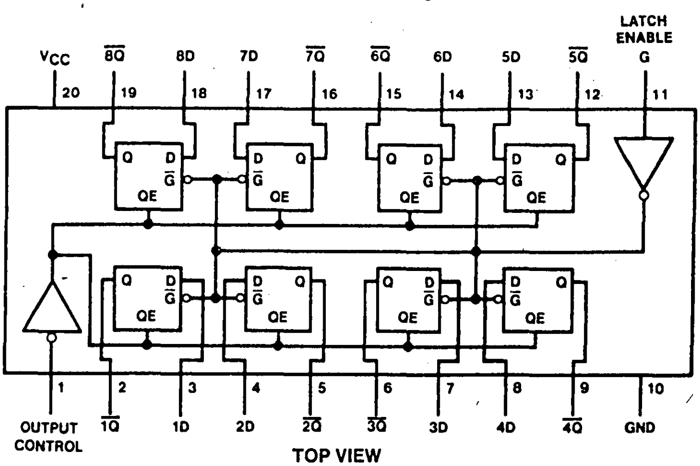
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA, maximum (74HC series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5339-1

MM54HC533/MM74HC533

54HC533 (J) 74HC533 (J,N)

Truth Table

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA $\|I_{OUT}\| \leq 7.8$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA $\|I_{OUT}\| \leq 7.8$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V–6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	50 21 19	150 30 26	188 37 31	225 45 39	ns ns ns
t_S	Minimum Set Up Time		2.0V 4.5V 6.0V	5 2 2	25 5 5	31 6 6	38 8 8	ns ns ns
t_H	Minimum Hold Time		2.0V 4.5V 6.0V	20 6 6	50 10 10	60 13 13	75 20 20	ns ns ns
t_W	Minimum Pulse Width		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch) $OC=V_{CC}$ $OC=Gnd$		 30 50				 pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

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MM54HC534/MM74HC534 TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These high speed Octal D-Type Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

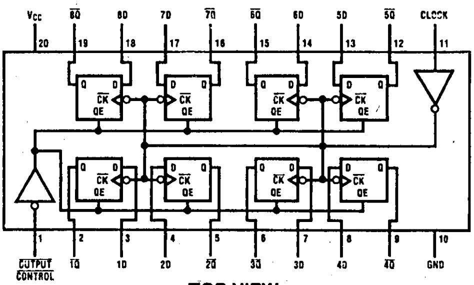
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5340–1

MM54HC534/MM74HC534

54HC534 (J) 74HC534 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High impedance state

$\overline{Q}_0$ = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $\overline{Q}$	$C_L=45$ pF	23	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	21	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	25	ns
t_S	Minimum Set Up Time		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	29	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	25	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	50	150	189	225	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)						pF
		$OC=V_{CC}$		30				
		$OC=Gnd$		50				
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC540/MM74HC540 Inverting Octal TRI-STATE® Buffer MM54HC541/MM74HC541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC540/MM74HC540 is an inverting buffer and the MM54HC541/MM74HC541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

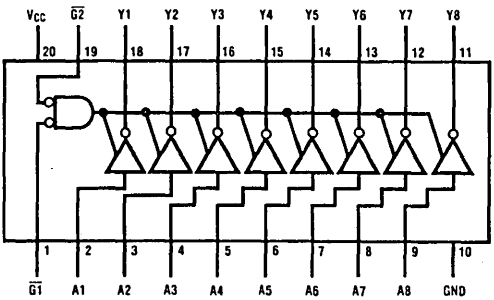
In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Output current: 6 mA

Connection Diagrams

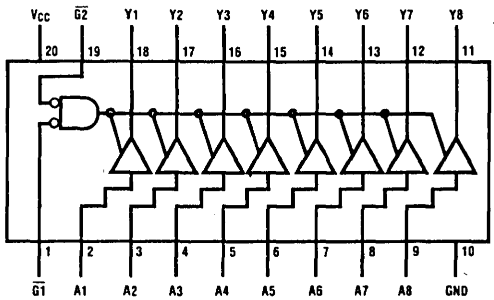
Dual-In-Line Package



TL/F/5341-1

MM54HC540/MM74HC540

54HC540 (J) 74HC540 (J,N)



TL/F/5341-2

MM54HC541/MM74HC541

54HC541 (J) 74HC541 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$ or V_{IL}, $\overline{G}=V_{IH}$ $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	$C_L=45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	$C_L=45$ pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	83	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	18	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	11	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$OC=V_{CC}$		10				pF
		$OC=GND$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15.	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC543/MM74HC543 Octal Registered Transceiver

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The HC543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable and output enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

For data flow from A to B, for example, the A-to-B enable ($\overline{EAB}$) input must be 'low' in order to enter data from A0–A7 or take data from B0–B7, as indicated in the I/O Control Table. With $\overline{EAB}$ low, a low signal on A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both low, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but uses the $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Features

- Octal TRI-STATE outputs for μP bus applications
- Output drive capability: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Separate controls for data flow in each direction

I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{EAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	X	X	Storing	Hi-Z
X	H	—	Storing	—
X	—	H	—	Hi-Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs*

*Before $\overline{LEAB}$ low-to-high transition

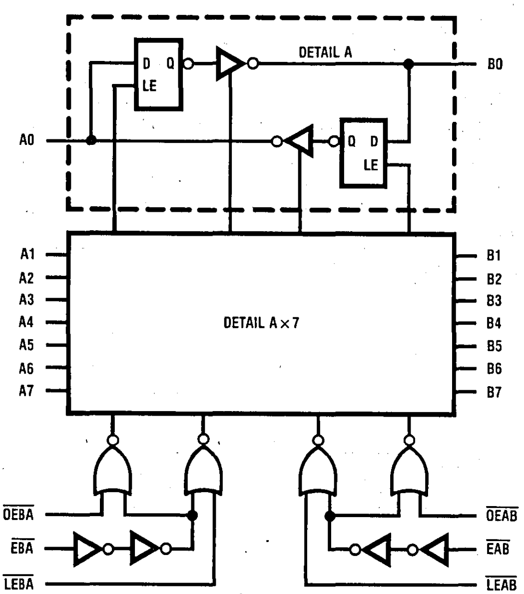
H = high voltage level

L = low voltage level

X = Don't care

†A-to-B data flow shown: B-to-A flow control is the same, except uses $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

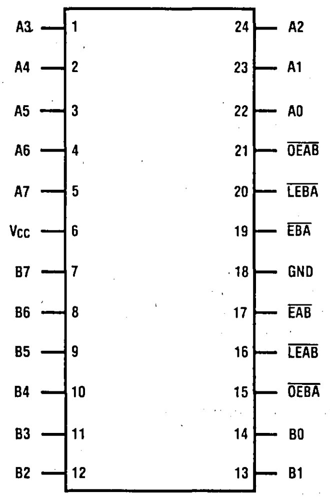
Logic Diagram



TL/F/6129-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6129-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC544/MM74HC544 Octal Registered Inverting Transceiver

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The HC544 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable and output enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

For data flow from A to B, for example, the A-to-B enable ($\overline{EAB}$) input must be 'low' in order to enter data from A0–A7 or take data from B0–B7, as indicated in the I/O Control Table. With $\overline{EAB}$ low, a low signal on A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both low, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but uses the $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Features

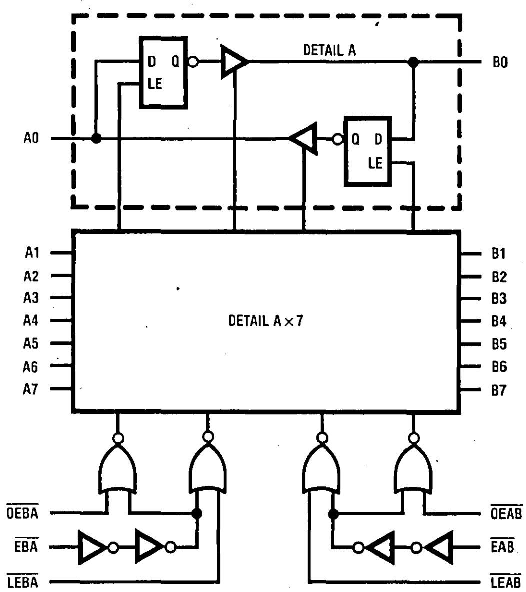
- Inverting outputs
- Octal TRI-STATE outputs for μP bus applications
- Output drive capability: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Separate controls for data flow in each direction

I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{EAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	X	X	Storing	Hi-Z
X	H	—	Storing	—
X	—	H	—	Hi-Z
L	L	L	Transparent	Current $\overline{A}$ Inputs
L	H	L	Storing	Previous $\overline{A}$ Inputs*

* Before $\overline{LEAB}$ low-to-high transition
H = high voltage level
L = low voltage level
X = don't care
†A-to-B data flow shown: B-to-A flow control is the same, except uses $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

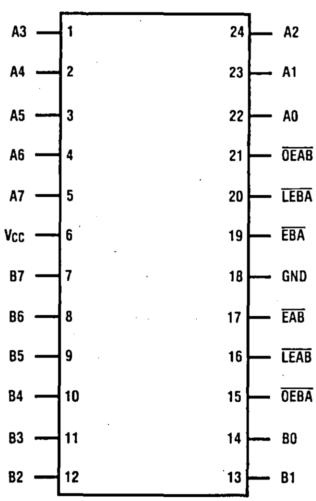
Logic Diagram



TL/F/6130-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6130-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC550/MM74HC550 Octal Registered Transceiver with Status Flags

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The MM54HC550/MM74HC550 contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer.

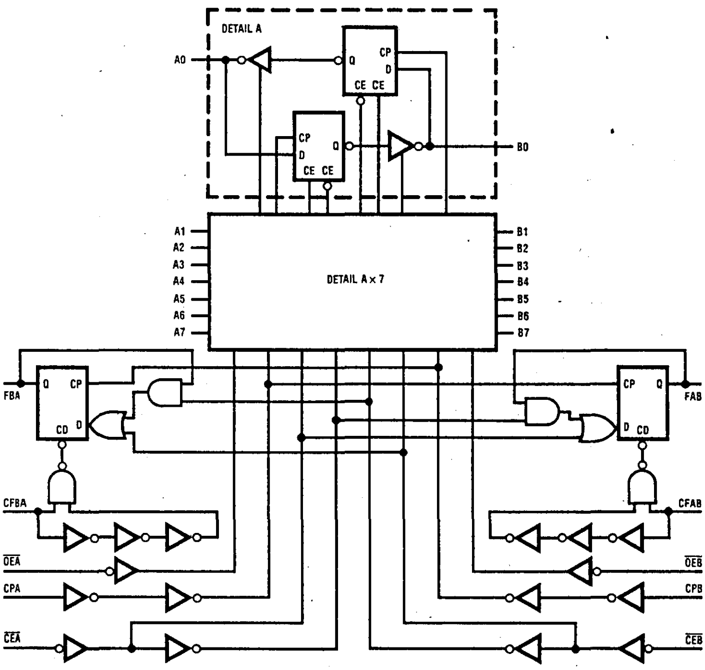
Data applied to the A inputs is entered and stored on the rising edge of the A clock pulse (CPA), provided that the A clock enable ($\overline{CEA}$) is low; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes high. Data thus entered from the A inputs is present at the inputs to the B output buffers, but appears only on the B I/O pins when the B output enable ($\overline{OEB}$) signal is made low. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a low-to-high transition to the CFAB input. Optionally, the $\overline{OEA}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output high. A low signal on $\overline{OEA}$ enables the A output buffers and a low-to-high transition on CFBA clears the FBA flag.

Features

- Output drive: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flag

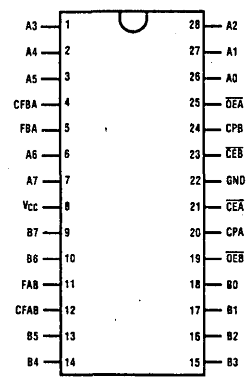
Logic Diagram



TL/F/6124-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6124-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC551/MM74HC551 Octal Registered Inverting Transceiver with Status Flags

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The MM54HC551/MM74HC551 contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer.

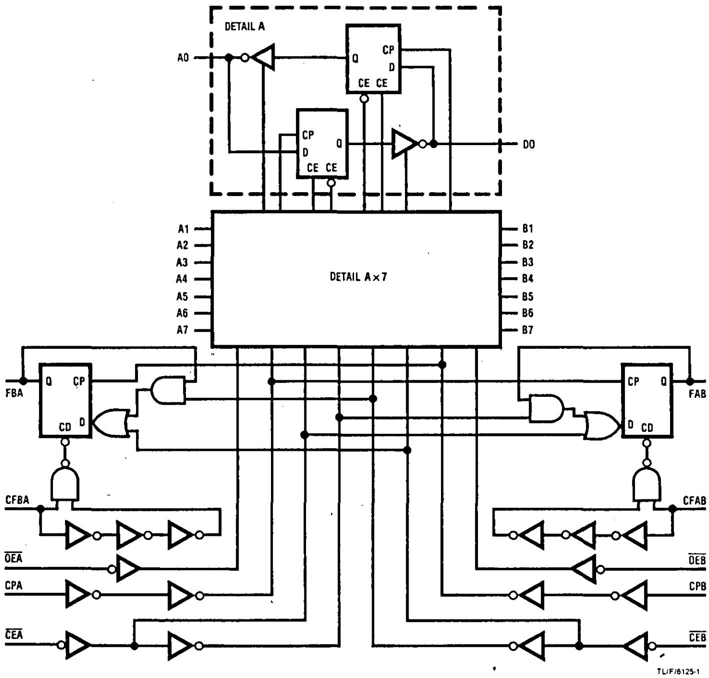
Data applied to the A inputs is entered and stored on the rising edge of the A clock pulse (CPA), provided that the A clock enable ($\overline{CEA}$) is low; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes high. Data thus entered from the A inputs is present at the inputs to the B output buffers, but appears only on the B I/O pins when the B output enable ($\overline{OEB}$) signal is made low. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a low-to-high transition to the CFAB input. Optionally, the $\overline{OEA}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output high. A low signal on $\overline{OEA}$ enables the A output buffers and a low-to-high transition on CFBA clears the FBA flag.

Features

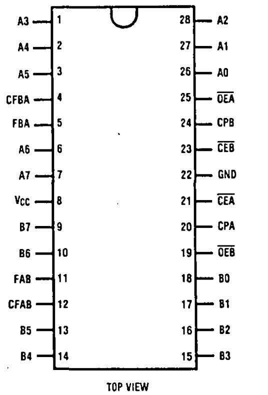
- Inverting outputs
- Output drive: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flag

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6124-2

National Semiconductor

microCMOS

MM54HC563/MM74HC563 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is high, the Q outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

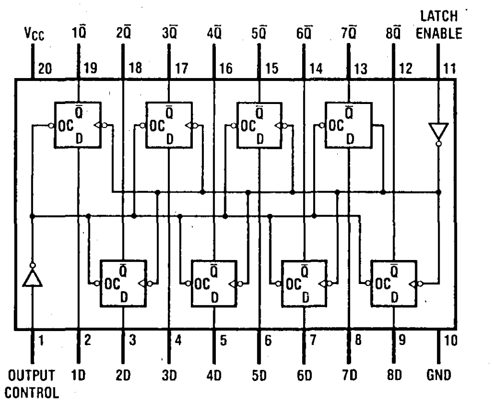
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Same as 580

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5210-1

MM54HC563/MM74HC563

54HC563 (J) 74HC563 (J,N)

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q0}$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CC})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $O_C=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$			8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time		10	15	ns
t_H	Minimum Hold Time		2	5	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0–6.0V$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	45	110	138	165	ns
		$C_L=150$ pF	2.0V	58	150	188	225	ns
		$C_L=50$ pF	4.5V	14	22	28	33	ns
		$C_L=150$ pF	4.5V	21	30	38	40	ns
		$C_L=50$ pF	6.0V	12	19	24	29	ns
		$C_L=150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	46	115	143	173	ns
		$C_L=150$ pF	2.0V	60	155	194	233	ns
		$C_L=50$ pF	4.5V	14	23	29	35	ns
		$C_L=150$ pF	4.5V	21	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	55	140	175	210	ns
		$C_L=150$ pF	2.0V	67	180	225	270	ns
		$C_L=50$ pF	4.5V	15	28	35	42	ns
		$C_L=150$ pF	4.5V	24	36	45	54	ns
		$C_L=50$ pF	6.0V	14	24	30	36	ns
		$C_L=150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	40	125	156	188	ns
		$C_L=50$ pF	4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time Data to LE		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time LE to Data		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width, LE D_o		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	$OE=V_{CC}$		30				pF
		$OE=GND$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC564/MM74HC564
TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These octal D-type flip-flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

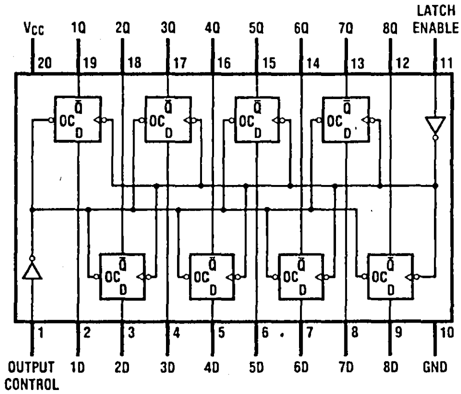
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Same as 576

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5211-1

MM54HC564/MM74HC564

54HC564 (J) 74HC564 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High Impedance State
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $O_C=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set-Up Time			20	ns
t_H	Minimum Hold Time			0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	40	115	143	173	ns
		$C_L=150$ pF	2.0V	51	155	194	233	ns
		$C_L=50$ pF	4.5V	13	23	29	35	ns
		$C_L=150$ pF	4.5V	19	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	45	140	175	210	ns
		$C_L=150$ pF	2.0V	59	180	225	270	ns
		$C_L=50$ pF	4.5V	14	28	35	42	ns
		$C_L=150$ pF	4.5V	20	36	45	54	ns
		$C_L=50$ pF	6.0V	12	24	30	36	ns
		$C_L=150$ pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	35	125	156	188	ns
		$C_L=50$ pF	4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Set-Up Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	8	16	20	24	ns
			6.0V	7	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC=VCC		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC573/MM74HC573 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE(LE) input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL OC input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

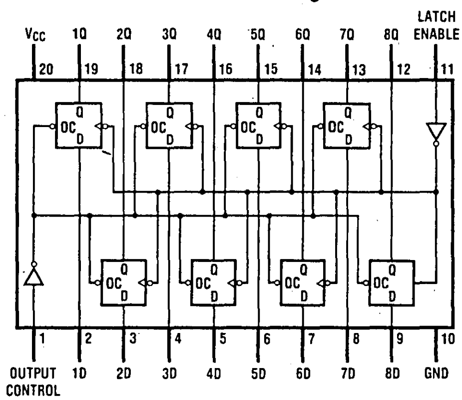
The 54HC/74HC logic family is speed, function and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5212-1

MM54HC573/MM74HC573

54HC573 (J) 74HC573 (J,N)

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $O_C=V_{IH}$	6.0V		±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	µA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time		10	15	ns
t_H	Minimum Hold Time		2	5	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Q	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	45 58	110 150	138 188	165 225	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	14 21	22 30	28 38	33 40	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	12 19	19 26	24 33	29 39	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	46 60	115 155	143 194	173 233	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	14 21	23 31	29 47	35 47	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	12 19	20 27	25 34	30 41	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	55 67	140 180	175 225	210 270	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	15 24	28 36	35 45	42 54	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	14 22	24 31	30 39	36 47	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	40 13 12	125 25 21	156 31 27	188 38 32	ns ns ns
t_S	Minimum Set Up Time Data to LE		2.0V 4.5V 6.0V	30 10 9	75 15 13	95 19 16	110 22 19	ns ns ns
t_H	Minimum Hold Time LE to Data		2.0V 4.5V 6.0V		25 5 4	31 6 5	38 7 6	ns ns ns
t_W	Minimum Pulse Width LE		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	$OE=V_{CC}$ $OE=GND$		30 50				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC574/MM74HC574 TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed octal D-type flip-flops utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

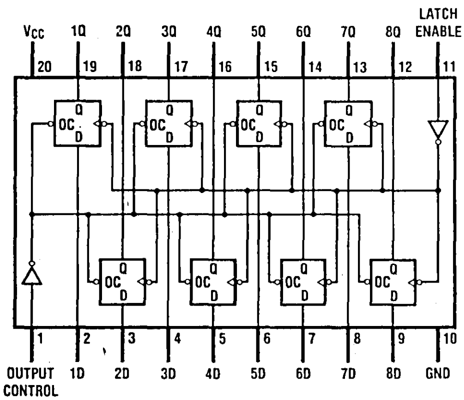
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



TL/F/5213–1

TOP VIEW

MM54HC574/MM74HC574

54HC574 (J)   74HC574 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND O_C=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set-Up Time			20	ns
t_H	Minimum Hold Time			0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V 4.5V 6.0V		6 30 35	5 24 28	4 20 23	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	40 51	115 155	143 194	173 233	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	13 19	23 31	29 47	35 47	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	12 18	20 27	25 34	30 41	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF $C_L=150$ pF	 2.0V 2.0V	 45 59	 140 180	 175 225	 210 270	 ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	14 20	28 36	35 45	42 54	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	12 18	24 31	30 39	36 47	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	35 12 10	125 25 21	156 31 27	188 38 32	ns ns ns
t_S	Minimum Set-Up Time Data to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
t_W	Minimum Clock Pulse Width		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC=VCC OC=GND		30 50				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC589/MM74HC589 8-Bit Shift Registers with Input Latches and TRI-STATE® Serial Output

General Description

This high speed shift register utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

The 'HC589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Data is serially entered on the SER pin. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and a TRI-STATE output to enable the wire-ORing of multiple devices on a serial bus.

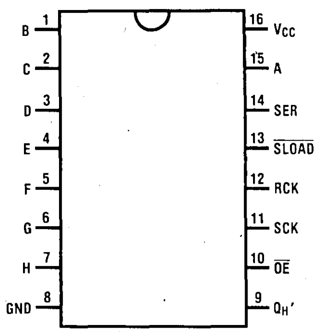
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-Bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load
- Guaranteed shift frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE output for 'Wire-OR'

Connection Diagram

Dual-In-Line Package



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MM54HC589/MM74HC589

54HC589 (J) 74HC589 (J,N)

Truth Table

RCK	SCK	$\overline{\text{SLOAD}}$	$\overline{\text{OE}}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	X	L	Serial output in high impedance state
X	↑	H	H	Shift register clocked $Q_M = Q_{n-1}$, Q_O = SER

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = logic '0'	25	45	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	25	ns
t_S	Minimum Set Up Time From RCK to SCK		10	20	ns
t_S	Minimum Set Up Time From SER to SCK		10	20	ns
t_S	Minimum Set Up Time From Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$		8	16	ns

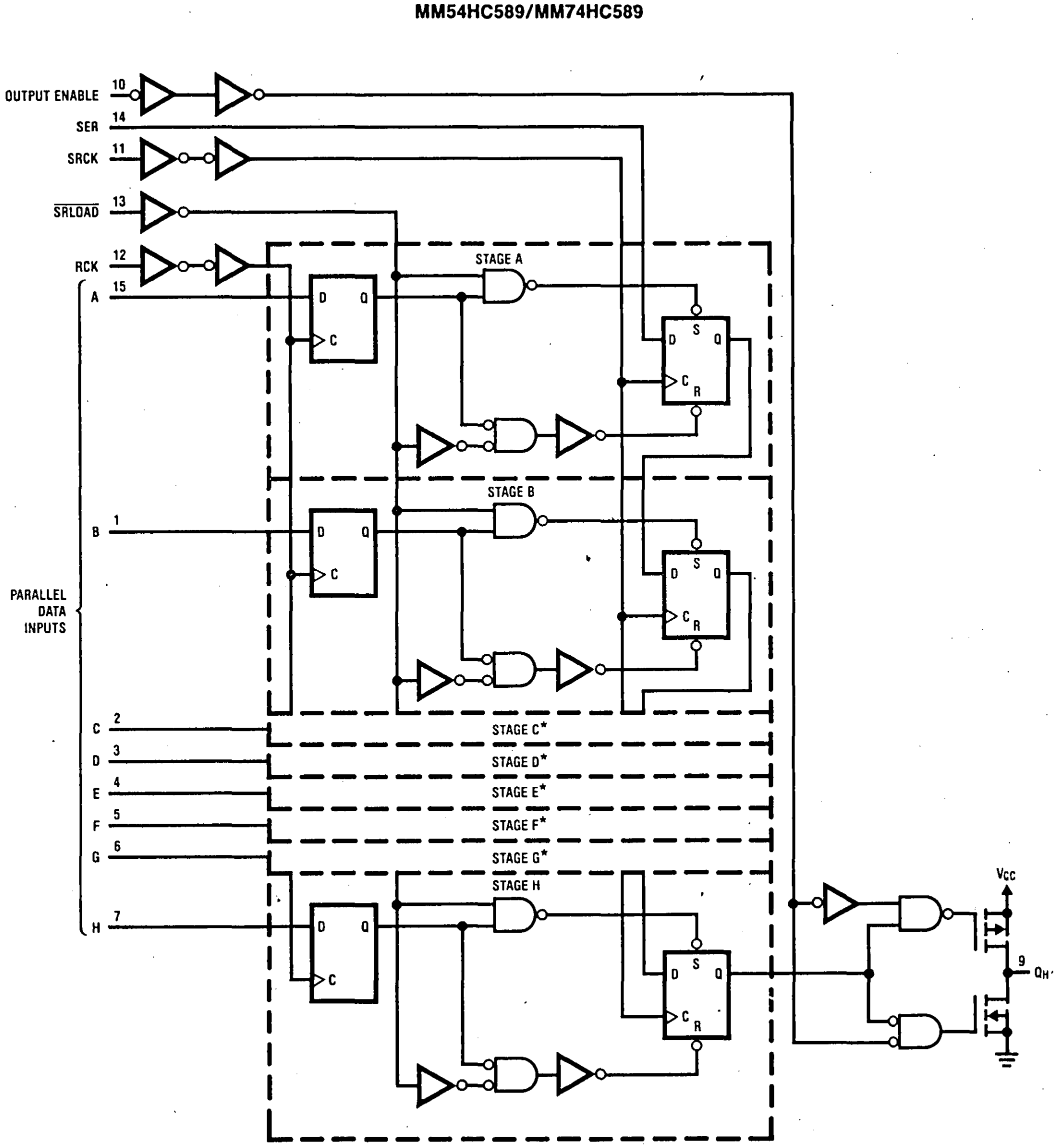
AC Electrical Characteristics $V_{CC}=2.0$–$6V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency for SCK		2.0V 4.5V 6.0V		5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK or $\overline{SRLOAD}$ to $Q_{H'}$		2.0V 4.5V 6.0V	62 20 18	175 35 30	220 43 37	266 52 45	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SRLOAD}$ to Q_H	$C_L=150$ pF	2.0V 4.5V 6.0V	120 31 28	225 45 38	284 57 48	335 67 57	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$		2.0V 4.5V 6.0V	80 25 21	210 42 36	265 53 45	313 63 53	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay RCK to Q_H'	$C_L=150$ pF	2.0V 4.5V 6.0V	80 25 21	210 52 44	265 66 56	313 77 66	ns ns ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	2.0V 4.5V 6.0V	70 22 20	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ	2.0V 4.5V 6.0V	70 22 20	150 30 26	189 38 32	224 45 38	ns ns ns
t_S	Minimum Set Up Time From RCK to SCK		2.0V 4.5V 6.0V		100 20 17	125 25 22	150 30 25	ns ns ns
t_S	Minimum Set Up Time From SER to SCK		2.0V 4.5V 6.0V		100 20 17	125 25 22	150 30 25	ns ns ns
t_S	Minimum Set Time From Inputs A thru H to RCK		2.0V 4.5V 6.0V		100 20 17	125 25 22	150 30 25	ns ns ns
t_H	Minimum Hold Time		2.0V 4.5V 6.0V	−5 0 1	5 5 5	5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$, $\overline{SLOAD}$		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 17	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1500 500 400	1500 500 400	1500 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 6 5	60 12 10	75 15 12	90 18 15	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Functional Block Diagram (positive logic)



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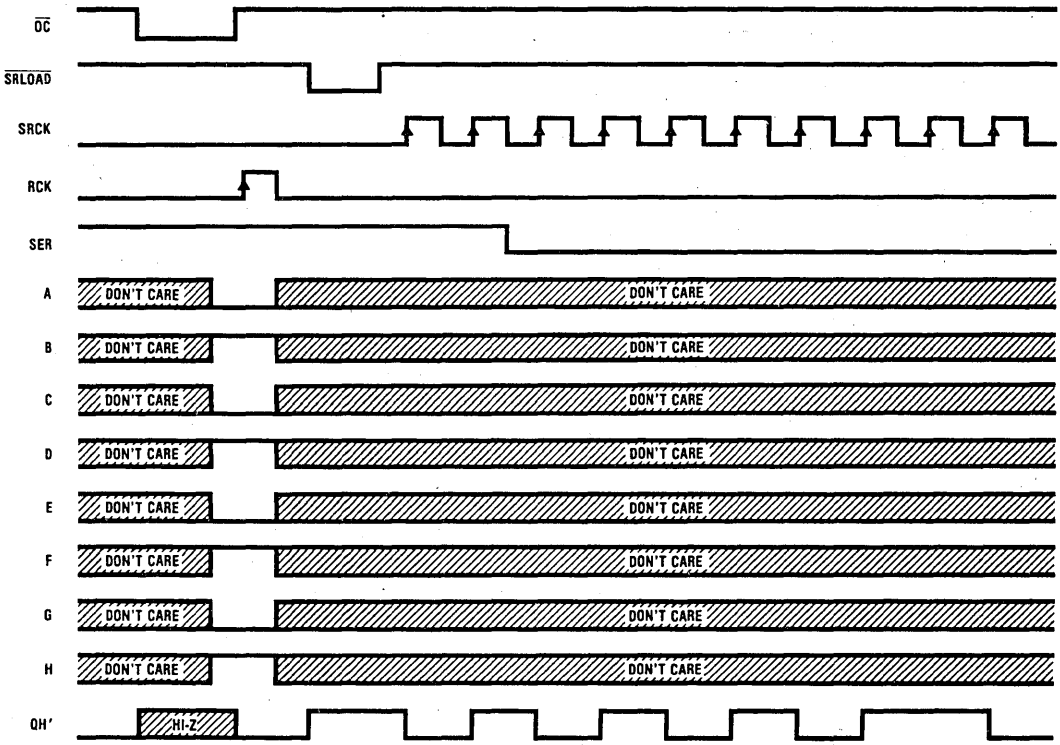
Logic Timing Diagram

MM54HC589/MM74HC589



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National Semiconductor

PRELIMINARY

microCMOS

MM54HC590/MM74HC590 8-Bit Binary Counter with TRI-STATE® Output Register

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power and high noise immunity of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits.

The MM54HC590/MM74HC590 contain an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{\text{CCKEN}}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{\text{RCO}}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{\text{RCO}}$ of the first stage to the $\overline{\text{CCKEN}}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{\text{RCO}}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed TRI-STATE outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus.

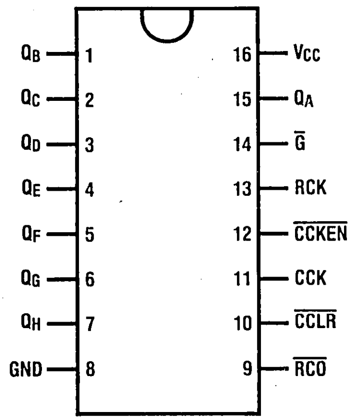
The MM54HC590/MM74HC590 are functional, speed and pin equivalent to the equivalent LS-TTL circuit. Its inputs are protected from damage due to the electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 2.0V to 6.0V
- High input noise immunity
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HC)

Connection Diagram

Dual-In-Line Package



TOP VIEW

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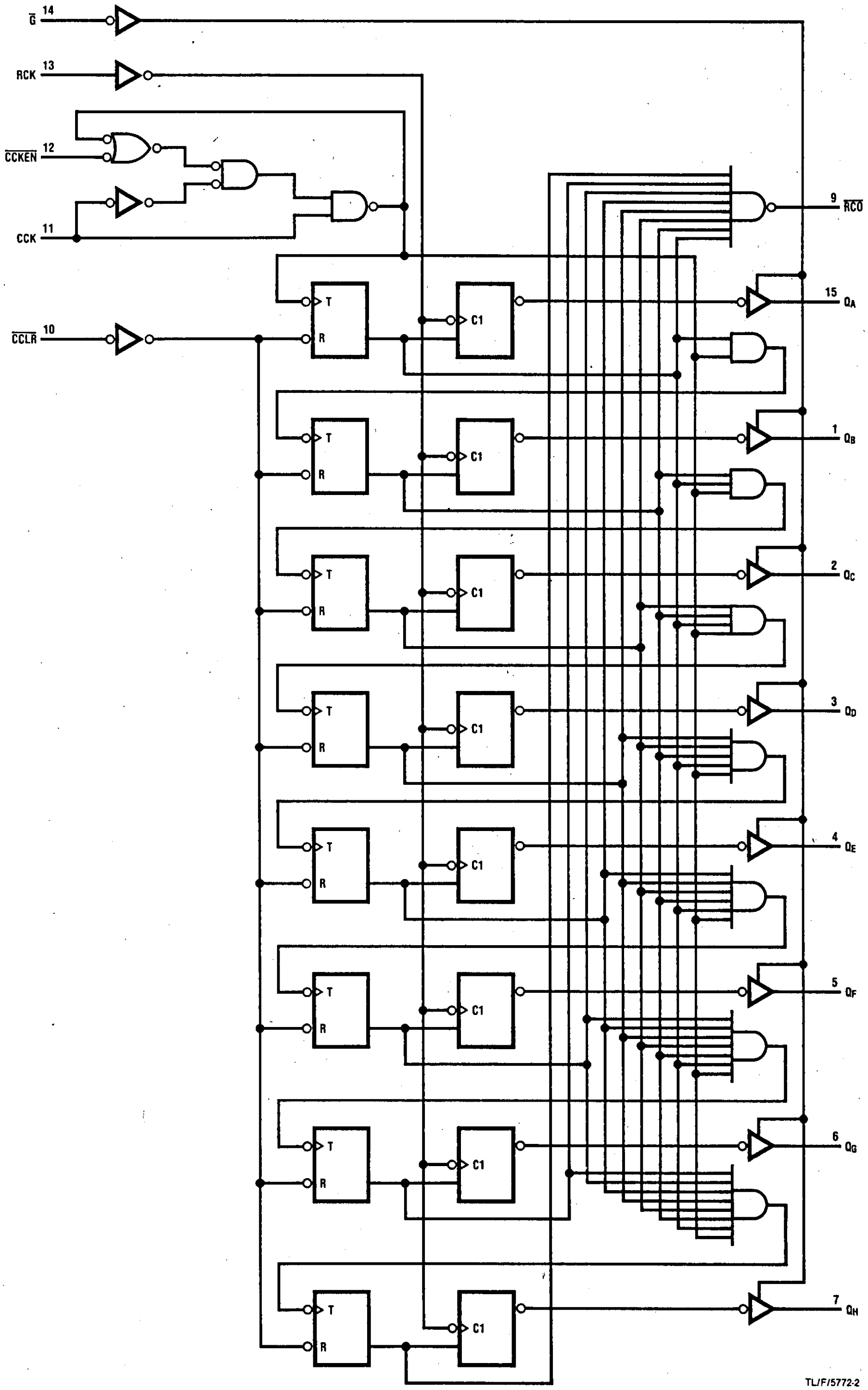
Logic Diagram



TL/F/5772-2

National Semiconductor

microCMOS

MM54HC592/MM74HC592 8-Bit Binary Counter with Input Register MM54HC593/MM74HC593 8-Bit Binary Counter with Bidirectional Input Register/Counter Outputs

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power and high noise immunity of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits.

The MM54HC592/MM74HC592 and the MM54HC593/MM74HC593 contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{RCO}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, $\overline{CLOAD}$, input is taken low.

The 'HC592 differs from the 'HC593 in that the latter device has bidirectional input/output pins. The TRI-STATE® outputs of the counter can be enabled and are active when enable input, G, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The 'HC593 also has a second clock enable pin, $\overline{CCKEN}$, which is active high and it also has an active low register clock enable, $\overline{RCKEN}$.

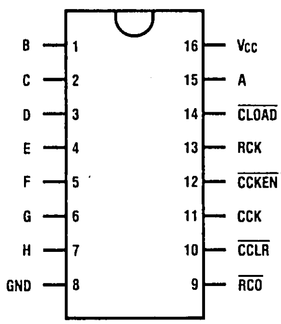
The MM54HC592/MM74HC592 and the MM54HC593/MM74HC593 are functional, speed and pin equivalent to the equivalent LS-TTL circuit. Their inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 2.0V to 6.0V
- High input noise immunity
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HC)

Connection Diagrams

Dual-In-Line Package
MM54HC592/MM74HC592



TOP VIEW

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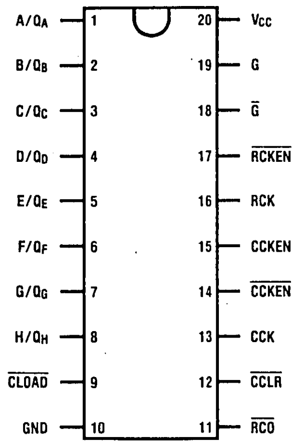
Dual-In-Line Package
MM54HC593/MM74HC593

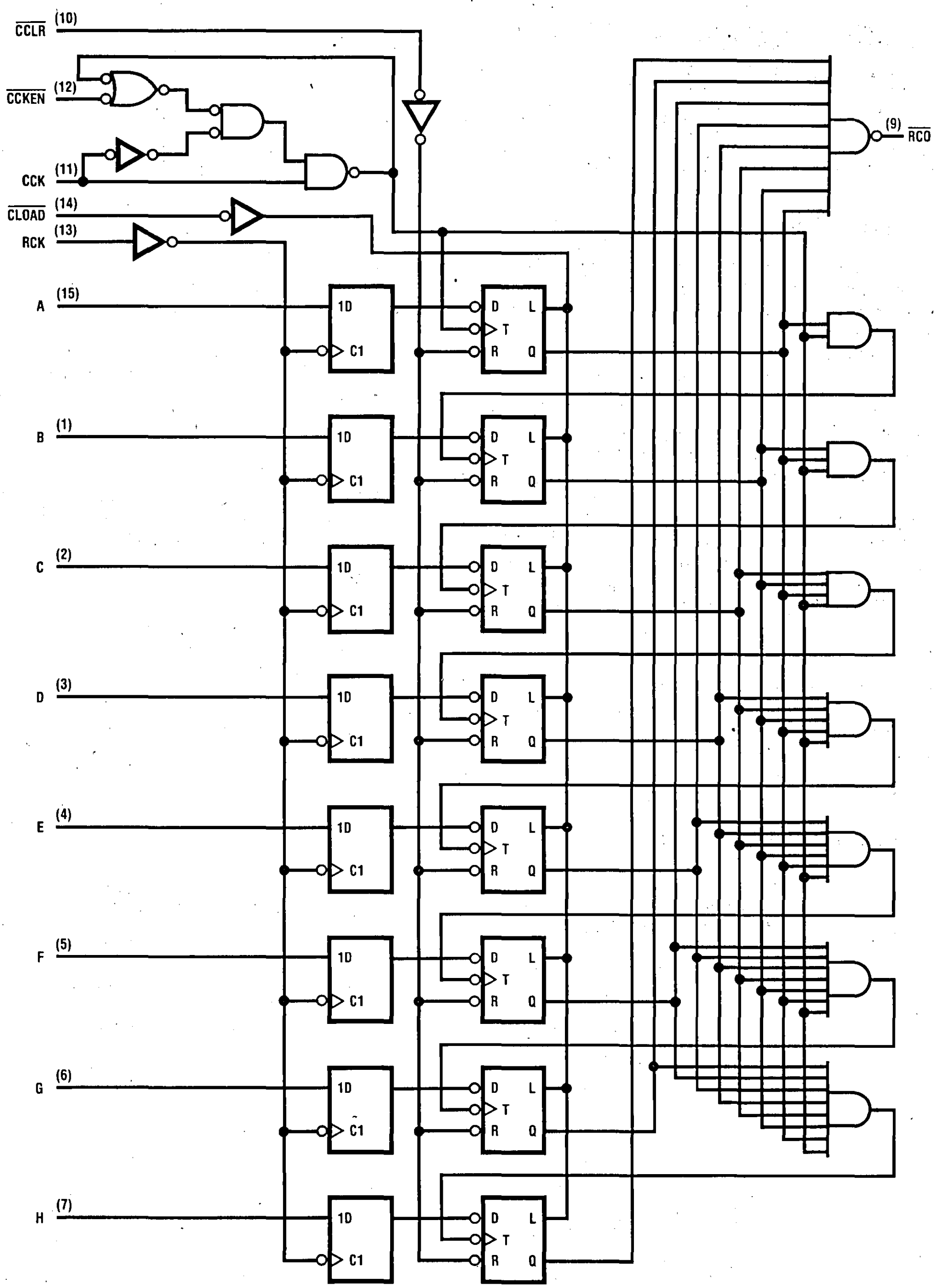


TOP VIEW

TL/F/5773-2

Logic Diagrams

MM54/74HC592



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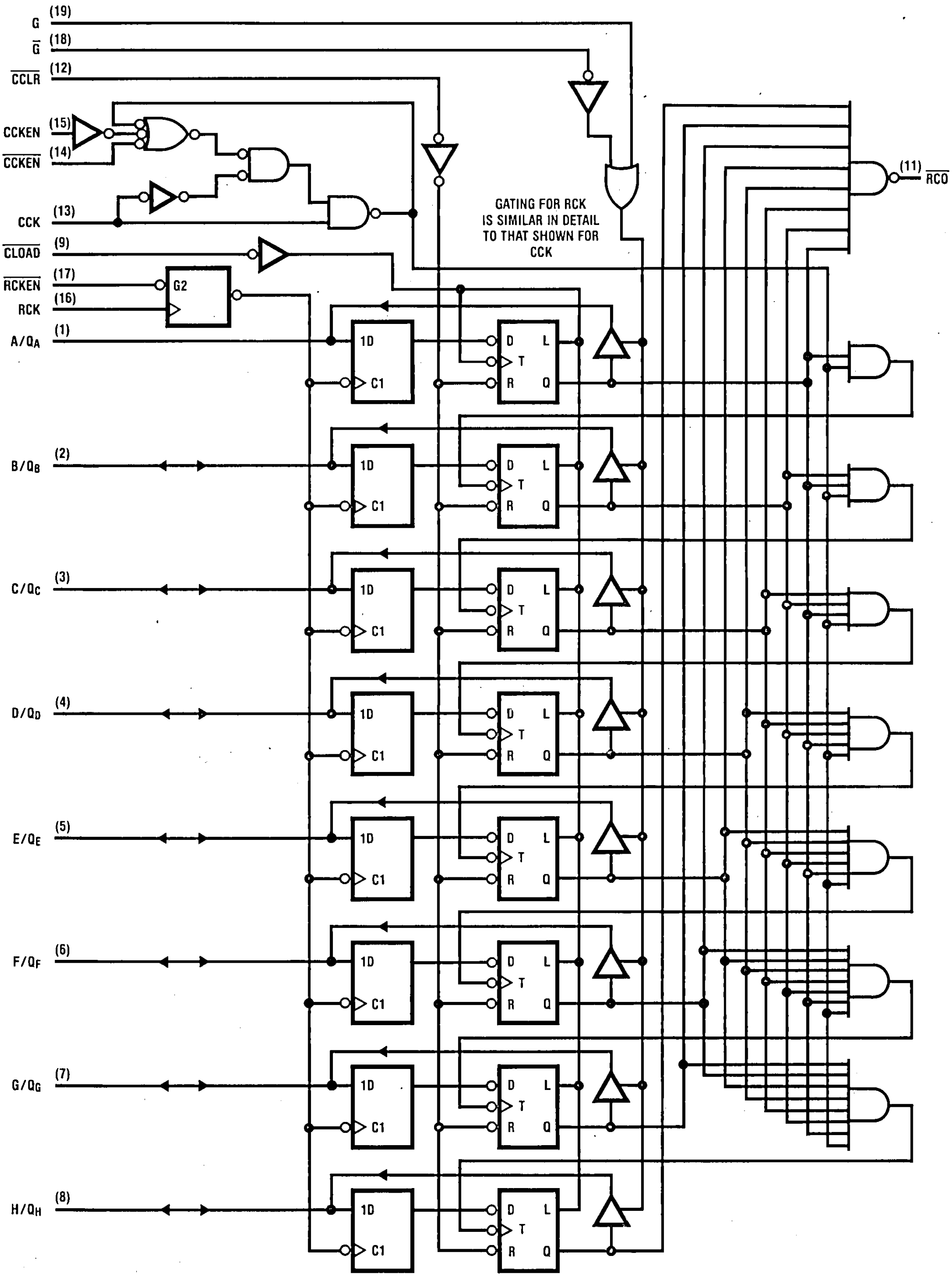
Logic Diagrams (Continued)

MM54/74HC593



TL/F/5773-4

National Semiconductor

PRELIMINARY

microCMOS

MM54HC595/MM74HC595
8-Bit Shift Registers with Output Latches

General Description

This high speed shift register utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 TRI-STATE® outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

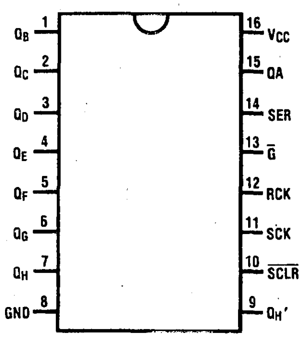
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-Bit Serial-In, Parallel-Out Shift Register With Storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift Register Has Direct Clear
- Guaranteed Shift Frequency: DC to 30 MHz

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5342-1

MM54HC595/MM74HC595

54HC595 (J) 74HC595 (J,N)

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	1	Q_A thru Q_H = Tri-State
X	X	L	X	Shift Register cleared $Q_{H'} = 0$
X	↑	H	X	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	X	Contents of Shift Register transferred to output latches

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
	$Q_{H'}$	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	4.5V 6.0V	4.2 5.2	3.98 5.48	3.84 5.34	3.7 5.2	V V
	Q_A thru Q_H	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
	$Q_{H'}$	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4$ mA $\|I_{OUT}\| \le 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
	Q_A thru Q_H	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT}=V_{CC} or GND Enable=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to $Q_{H'}$	$C_L=45$ pF	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L=45$ pF	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time From $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time From $\overline{G}$ to Q_A thru Q_H	$R_L=$ kΩ $C_L=5$ pF	15	25	ns
t_S	Minimum Set Up Time From SER to SCK			20	ns
t_S	Minimum Set Up Time From $\overline{SCLR}$ to SCK			20	ns
t_S	Minimum Set Up Time From SCK to RCK (See Note 5)			40	ns
t_H	Minimum Hold Time From SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

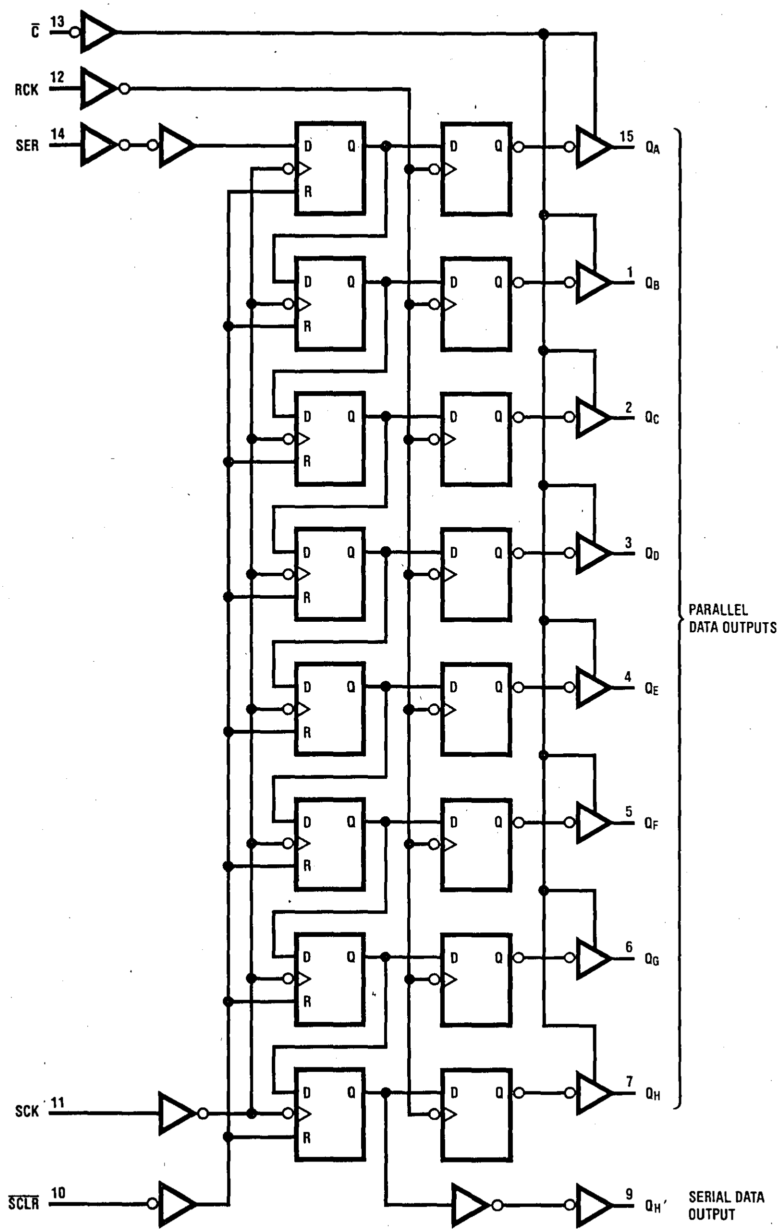
AC Electrical Characteristics $V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V 4.5V 6.0V	10 45 50	5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	58 83	115 165	145 208	171 246	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	14 17	23 33	29 42	34 49	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	10 14	20 28	25 35	29 42	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to Q_A thru Q_H	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V	70 105	150 200	188 225	225 250	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	21 28	30 40	38 50	45 60	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	18 26	26 34	33 43	39 51	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable From $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ $C_L=50$ pF $C_L=150$ pF	 2.0V 2.0V	 75 100	 150 200	 189 252	 224 298	 ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V	15 20	30 40	38 50	45 60	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V	13 17	26 34	32 43	38 51	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time From $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_S	Minimum Set Up Time From SER to SCK		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time From $\overline{SCLR}$ to SCK		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time From SCK to RCK		2.0V 4.5V 6.0V		200 40 34	250 50 42	300 60 50	ns ns ns
t_H	Minimum Hold Time SER to SCK		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width of SCK or RCLK		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 22	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G}=V_{CC}$ $G=GND$		90 150				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 7: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram (positive logic)



TL/F/5342-3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC597/MM74HC597
8-Bit Shift Registers with Input Latches

General Description

This high speed shift register utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The 'HC597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

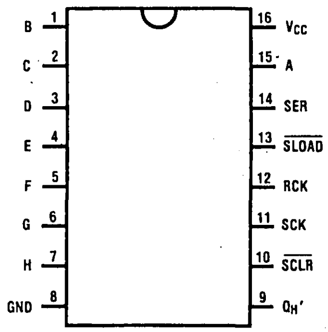
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-Bit Parallel Storage Register Inputs
- Wide operating voltage range: 2V–6V
- Shift Register has Direct Overriding Load and Clear
- Guaranteed Shift Frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5343-1

MM54HC597/MM74HC597

54HC597 (J) 74HC597 (J,N)

Truth Table

RCK	SCK	$\overline{\text{SLOAD}}$	$\overline{\text{SCLR}}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked $Q_n = Q_n\text{-}1$, $Q_0 = \text{SER}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = logic'0'	25	45	ns
t_{PHL}	Maximum Propagation Delay From $\overline{SCLR}$ to $Q_{H'}$		20	30	ns
t_{REM}	Minimum Removal Time, $\overline{SCLR}$ to SCK		10	20	ns
t_S	Minimum Set Up Time From RCK to SCK		30	40	ns
t_S	Minimum Set Up Time From SER to SCK		10	20	ns
t_S	Minimum Set Up Time From Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$ $\overline{SLOAD}$		10	16	ns

AC Electrical Characteristics

$V_{CC}=2.0–6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency for SCK		2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$		2.0V	62	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$		2.0V	65	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = Logic '0'	2.0V	120	250	312	375	ns
			4.5V	30	50	65	75	ns
			6.0V	28	43	53	65	ns
t_{PHL}	Maximum Propagation Delay From $\overline{SCLR}$ to $Q_{H'}$		2.0V	66	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{REM}	Minimum Removal Time $\overline{SCLR}$ to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Up Time From RCK to SCK		2.0V		200	250	300	ns
			4.5V		40	50	60	ns
			6.0V		34	42	50	ns
t_S	Minimum Set Up Time From SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns

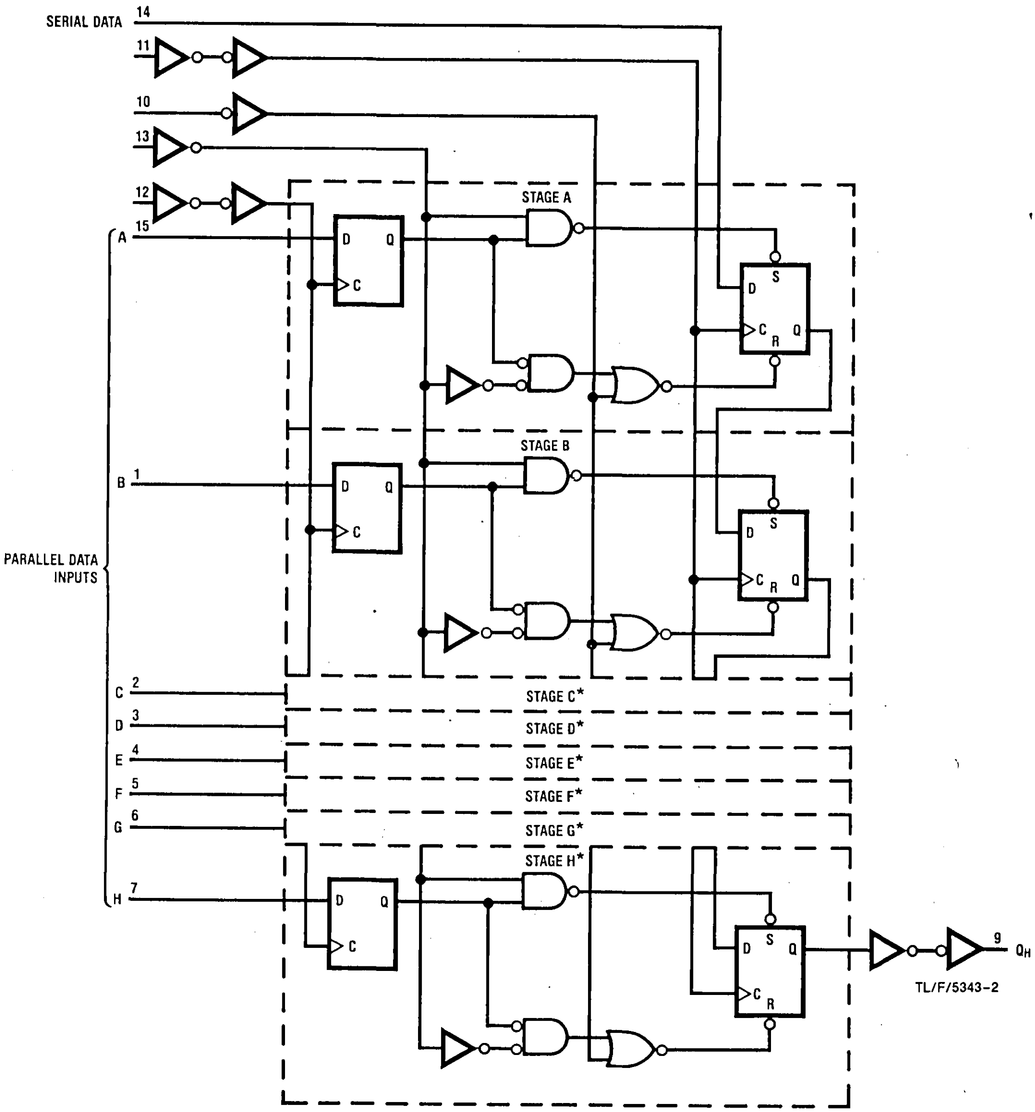
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Guaranteed Limits			
t_S	Minimum Set Up Time From Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Functional Block Diagram (Positive logic)



TL/F/5343-2

National Semiconductor

microCMOS

MM54HC640/MM74HC640 Inverting Octal TRI-STATE® Transceiver MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

Each device has an active enable $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC640/MM74HC640 transfers inverted data from one bus to other and the MM54HC643/MM74HC643 transfers inverted data from the A bus to the B bus and true data from the B bus to the A bus.

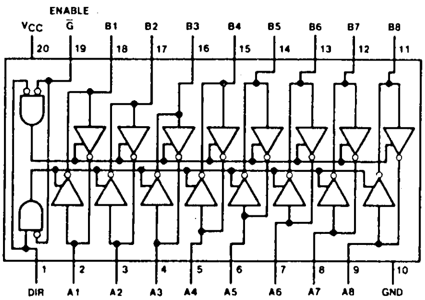
These devices can drive up to 15 LS-TTL Loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High Output Drive: 6 mA (min)

Connection Diagrams

Dual-In-Line Package

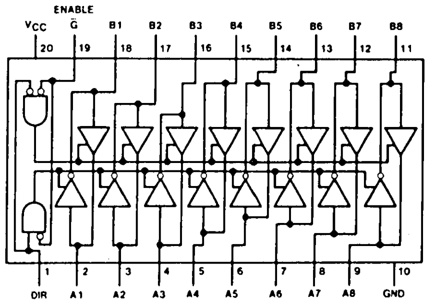


TOP VIEW TL/F/5344-1

MM54HC640/MM74HC640

54HC640 (J) 74HC640 (J,N)

Dual-In-Line Package



TOP VIEW TL/F/5344-2

MM54HC643/MM74HC643

54HC643 (J) 74HC643 (J,N)

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND Enable$\overline{G}=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	17	ns
t_{PHZ}, t_{PLZ}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	33	42	ns
t_{PZH}, t_{PZL}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	32	42	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

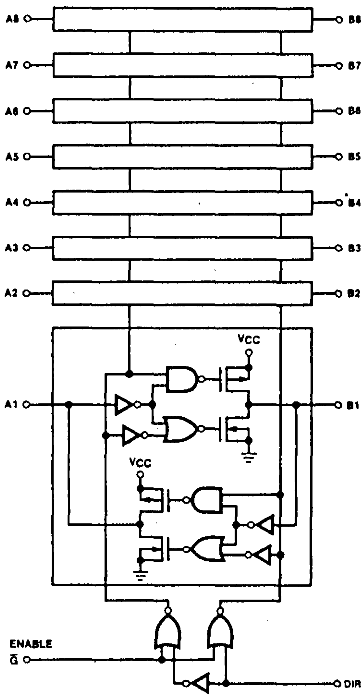
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	29	72	88	96	ns
		$C_L=150$ pF	2.0V	38	96	116	128	ns
		$C_L=50$ pF	4.5V	14	18	22	24	ns
		$C_L=150$ pF	4.5V	18	24	29	32	ns
		$C_L=50$ pF	6.0V	14	18	22	24	ns
		$C_L=150$ pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	70	184	224	240	ns
		$C_L=150$ pF	2.0V	80	216	260	284	ns
		$C_L=50$ pF	4.5V	35	46	56	60	ns
		$C_L=150$ pF	4.5V	41	54	65	71	ns
		$C_L=50$ pF	6.0V	31	41	50	54	ns
		$C_L=150$ pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{THL}, t_{TLH}	Output Rise and Fall Time		2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	643 B-A $\overline{G}=V_{IL}$		100				pF
		640(643 A-B) $\overline{G}=V_{IL}$		120				pF
		643 $\overline{G}=V_{IH}$		12				pF
		640(643 A-B) $\overline{G}=V_{IH}$		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

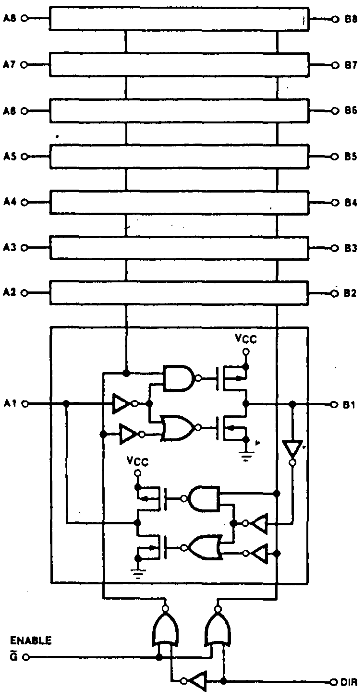
Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams

'HC640



'HC643



National Semiconductor

microCMOS

MM54HC646/MM74HC646 Non-Inverting Octal Bus Transceiver/Registers MM54HC648/MM74HC648 Inverting Octal Bus Transceiver/Registers

General Description

These transceivers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and contain two sets of TRI-STATE® outputs, two sets of D-type flip-flops, and control circuitry designed for high speed multiplexed transmission of data.

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the G, DIR, CAB, CBA, SAB, SBA control inputs. The enable input, G, controls whether any bus outputs are enabled. The direction control, DIR, determines which bus is enabled, and hence the direction data flows: The SAB, SBA inputs control whether the latched data (stored in D type flip flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock CAB, and CBA, for storing data. Data is latched on the rising edge of the clock.

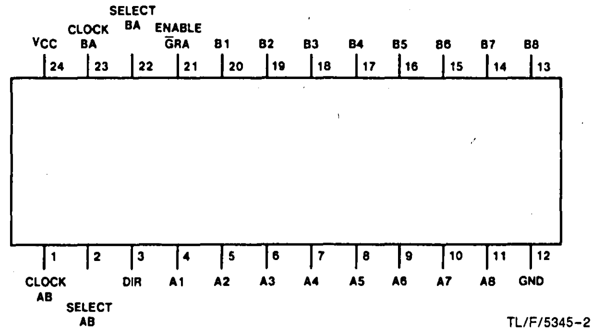
Each output can drive up to 15 low power Schottky TTL loads. These devices are functionally and pin compatible to their LS-TTL counterparts. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

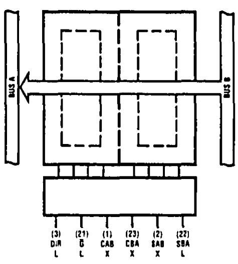
- Typical propagation delay: 14 ns
- TRI-STATE outputs
- Bi-directional communication
- Wide power supply range: 2–6V
- Low quiescent supply current: 160 μA maximum (74HC)
- High output current: 6 mA (74HC)

Connection Diagrams

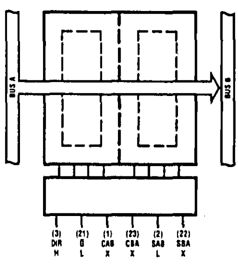
Dual-In-Line Package



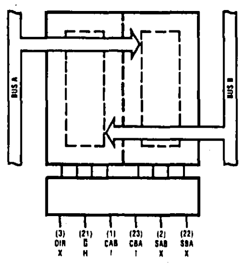
TL/F/5345-2



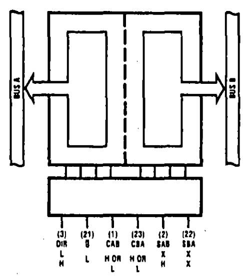
Real-Time Transfer Bus B to Bus A



Real-Time Transfer Bus A to Bus B



Storage from A, B, or A and B



TL/F/5345-1

Transfer Stored Data to A or B

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.96	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	$V_{OUT}=V_{CC}$ or GND $\overline{G}=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Truth Table

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	646	648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Input	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = High Level L = Low Level X = Irrelevant ↑ = low-to-high level transition

The data output functions i.e., data at the bus pins may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled.

The data output functions i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

AC Electrical Characteristics MM54HC646/MM74HC646

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=45$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=45$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=45$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC646/MM74HC646

$V_{CC}=2.0–6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	2.0V	180	290	363	435	ns
		$C_L=150$ pF	2.0V	210	340	425	510	ns
		$C_L=50$ pF	4.5V	39	58	72	87	ns
		$C_L=150$ pF	4.5V	47	68	85	102	ns
		$C_L=50$ pF	6.0V	34	50	63	75	ns
		$C_L=150$ pF	6.0V	39	58	72	87	ns

AC Electrical Characteristics MM54HC646/MM74HC646 (Continued)

$V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=50$ pF	2.0V	180	290	363	435	ns
		$C_L=150$ pF	2.0V	210	340	425	510	ns
		$C_L=50$ pF	4.5V	39	58	72	87	ns
		$C_L=150$ pF	4.5V	47	68	85	102	ns
		$C_L=50$ pF	6.0V	34	50	63	75	ns
		$C_L=150$ pF	6.0V	39	58	72	87	ns
t_{PZH}, t_{PZH}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	80	175	219	263	ns
		$C_L=150$ pF	2.0V	120	225	281	338	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
		$C_L=150$ pF	4.5V	31	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	$R_L=1$ kΩ	2.0V	85	175	219	263	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			15	20	20	20	pF

AC Electrical Characteristics MM54HC648/MM74HC648

V_{CC} = 5V, T_A = 25°C, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		44	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	C_L = 50 pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	C_L = 50 pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	C_L = 50 pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	C_L = 50 pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ Input to A or B Output	R_L = 1 kΩ C_L = 45 pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ C_L = 5 pF	17	30	ns

AC Electrical Characteristics MM54HC648/MM74HC648

V_{CC} = 2.0–6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	C_L = 50 pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	C_L = 50 pF	2.0V	60	180	189	225	ns
		C_L = 150 pF	2.0V	80	200	250	300	ns
		C_L = 50 pF	4.5V	21	30	37	45	ns
		C_L = 150 pF	4.5V	30	40	50	60	ns
		C_L = 50 pF	6.0V	18	26	31	39	ns
		C_L = 150 pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	C_L = 50 pF	2.0V	110	220	275	330	ns
		C_L = 150 pF	2.0V	150	270	338	405	ns
		C_L = 50 pF	4.5V	31	44	55	66	ns
		C_L = 150 pF	4.5V	40	54	68	81	ns
		C_L = 50 pF	6.0V	28	38	47	57	ns
		C_L = 150 pF	6.0V	34	47	59	71	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	C_L = 50 pF	2.0V	180	290	363	435	ns
		C_L = 150 pF	2.0V	210	340	425	510	ns
		C_L = 50 pF	4.5V	39	58	72	87	ns
		C_L = 150 pF	4.5V	47	68	85	102	ns
		C_L = 50 pF	6.0V	34	50	63	75	ns
		C_L = 150 pF	6.0V	39	58	72	87	ns

AC Electrical Characteristics MM54HC648/MM74HC648 (Continued)

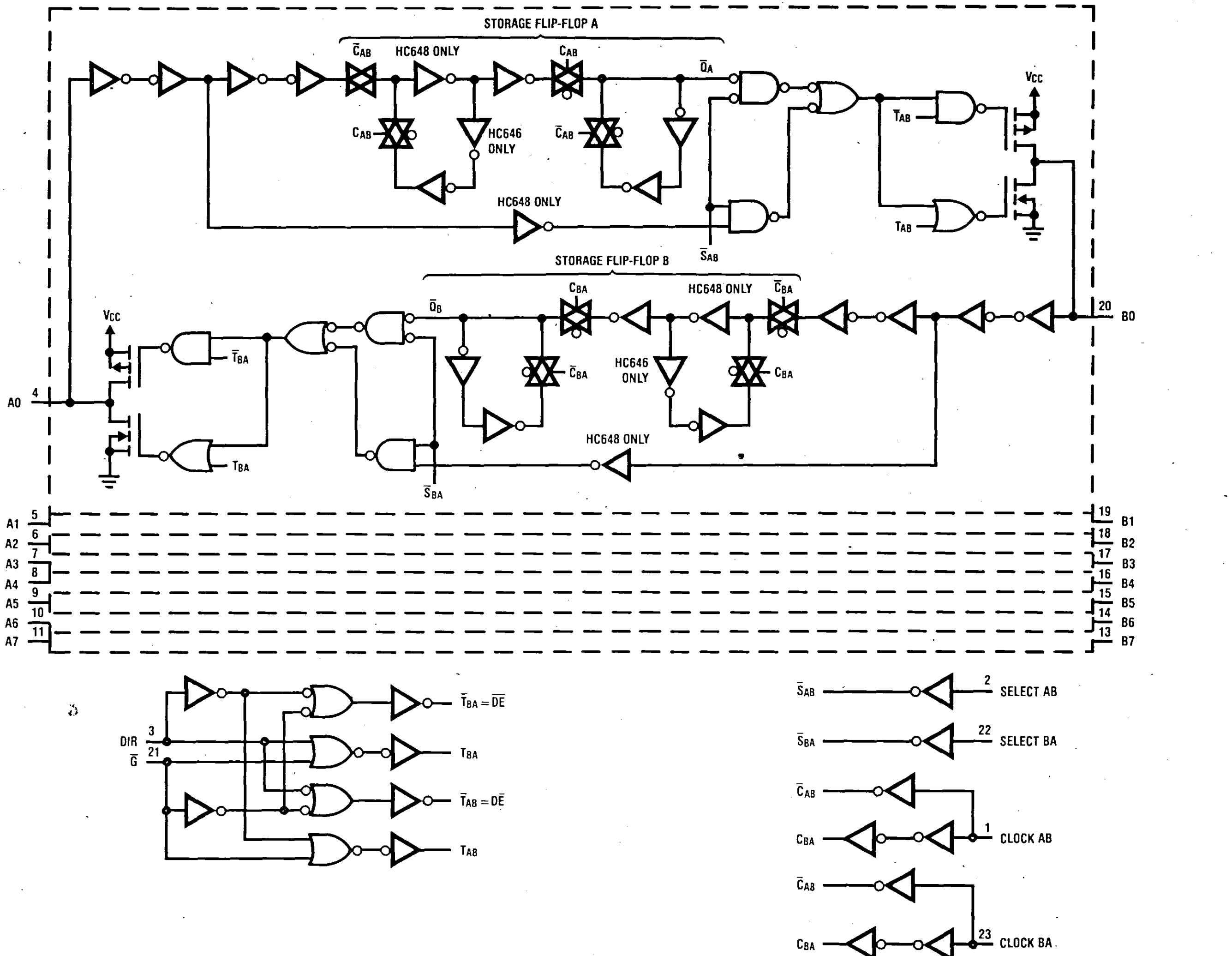
V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	C_L = 50 pF	2.0V	180	290	363	435	ns
		C_L = 150 pF	2.0V	210	340	425	510	ns
		C_L = 50 pF	4.5V	39	58	72	87	ns
		C_L = 150 pF	4.5V	47	68	85	102	ns
		C_L = 50 pF	6.0V	34	50	63	75	ns
		C_L = 150 pF	6.0V	39	58	72	87	ns
t_{PZL}, t_{PZL}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	80	175	219	263	ns
		C_L = 150 pF	2.0V	120	225	281	338	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
		C_L = 150 pF	4.5V	31	45	56	68	ns
		C_L = 50 pF	6.0V	21	30	37	45	ns
		C_L = 150 pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ	2.0V	85	175	219	263	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
		C_L = 50 pF	4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5345-3

National Semiconductor

microCMOS

MM54HC688/MM74HC688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

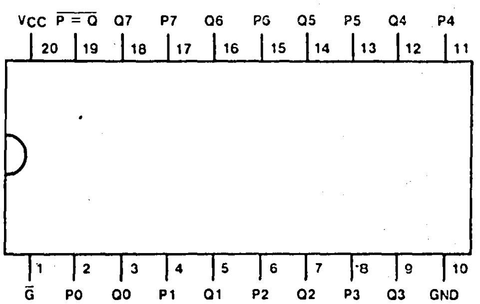
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 series)
- Large output current: 4 mA (74 series)
- Same as 'HC521

Connection and Logic Diagrams

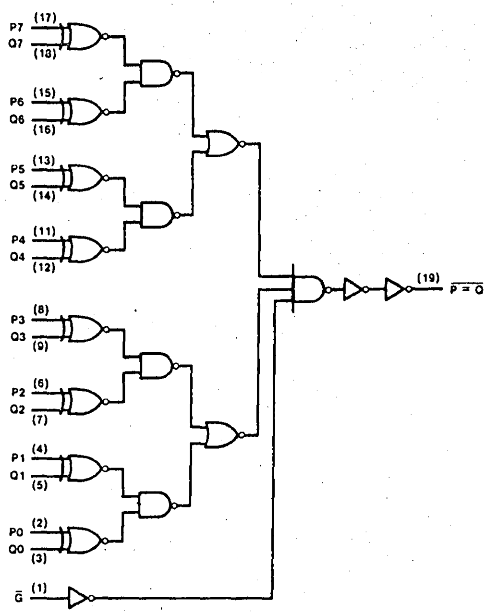
Dual-In-Line Package



TOP VIEW TL/F/5018-1

MM54HC688/MM74HC688

54HC688 (J) 74HC688 (J,N)



TL/F/5018-2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	60 22 19	175 35 30	220 44 38	263 53 45	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	45 15 13	120 24 20	150 30 25	180 36 30	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC4002/MM74HC4002 Dual 4-Input NOR Gate

General Description

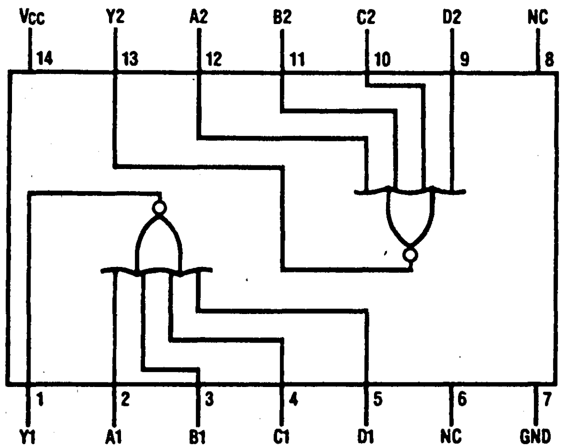
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4002/74HC4002 is functionally equivalent and pin-out compatible with the CD4002B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5154-1

MM54HC4002/MM74HC4002

54HC4002 (J) 74HC4002 (J,N)

$$Y = \overline{A + B + C + D}$$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage		2.0V 4.5V 6.0V		0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V V V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4$ mA $\lvert I_{OUT}\rvert \leq 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4016/MM74HC4016 Quad Analog Switch

General Description

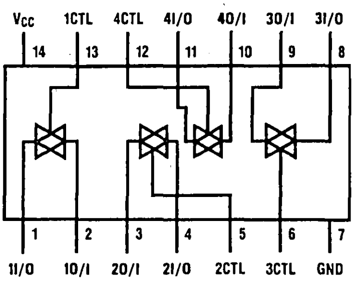
These devices are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low 'on' resistance and low 'off' leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. The '4016 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low 'on' resistance: 50Ω typical
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TL/F/5350–1

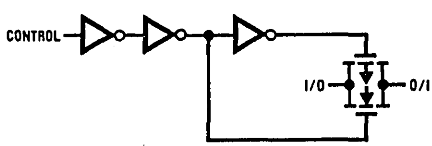
TOP VIEW
MM54HC4016/MM74HC4016

54HC4016 (J) 74HC4016 (J,N)

Truth Table

Input	Switch
CTL	I/O-O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5350–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	6.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum 'ON' Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} to GND (Figure 1)	4.5V	100				Ω
			9.0V	50				Ω
			12.0V	30				Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} or GND (Figure 1)	2.0V	120				Ω
			4.5V	50				Ω
			9.0V	35				Ω
			12.0V	20				Ω
R_{ON}	Maximum 'ON' Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	4.5V	10				Ω
			9.0V	5				Ω
			12.V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch 'OFF' Leakage Current	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{CTL}=V_{IL} (Figure 2)	5.5V	10				nA
			9.0V	15				nA
			12.0V	20				nA
I_{IZ}	Maximum Switch 'ON' Leakage Current	V_{OS}=V_{CC} or GND V_{CTL}=V_{IH} (Figure 3)	5.5V	10				nA
			9.0V	15				nA
			12.0V	20				nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	5.5V		2.0	20	40	μA
			9.0V		8.0	80	160	μA
			12.0V		16.0	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so these values should be used.

Note 5: At supply voltages (V_{CC}-V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

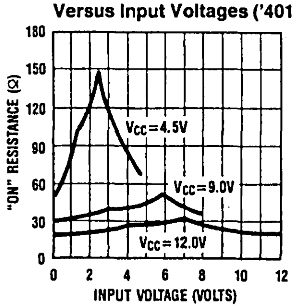
AC Electrical Characteristics

V_{CC}=2.0V–6.0V V_{EE}=0V to 6V, C_L=15 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V 4.5V 9.0V 12.0V	25 5 4 3				ns ns ns ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L=1 kΩ	2.0V 4.5V 9.0V 12.0V	32 8 6 5				ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	2.0V 4.5V 9.0V 12.0V	45 15 10 8				ns ns ns ns
f_{MAX}	Maximum Switch Frequency Response 20 log (V_I/V_O)=-3 dB		4.5V 9.0V	100 120				MHz MHz
	Cross Talk Control to Switch	(Figure 7)	4.5V	180				mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	4.5V					MHz
	Crosstalk, Switch Input to Output (Frequency at -50 dB)							MHz
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CLT}=GND		5				pF

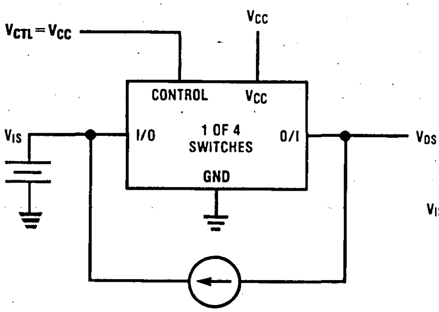
Typical Performance Characteristics

Typical "On" Resistance Versus Input Voltages ('4016)



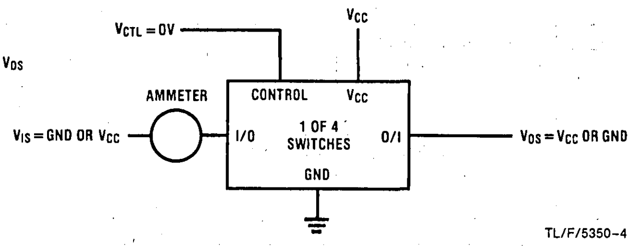
TL/F/5350-17

AC Test Circuits and Switching Time Waveforms



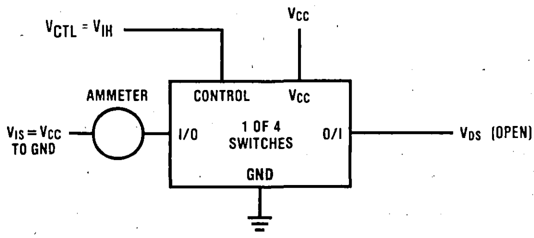
TL/F/5350-3

FIGURE 1. "ON" Resistance



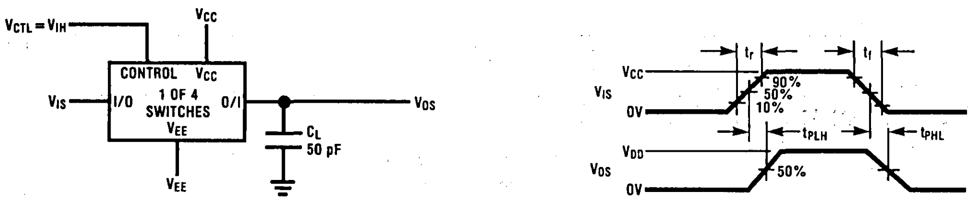
TL/F/5350-4

FIGURE 2. "OFF" Channel Leakage Current



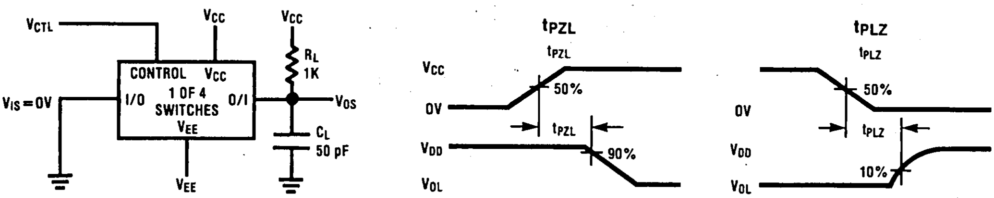
TL/F/5350-5

FIGURE 3. "ON" Channel Leakage Current



TL/F/5350-6 TL/F/5350-7

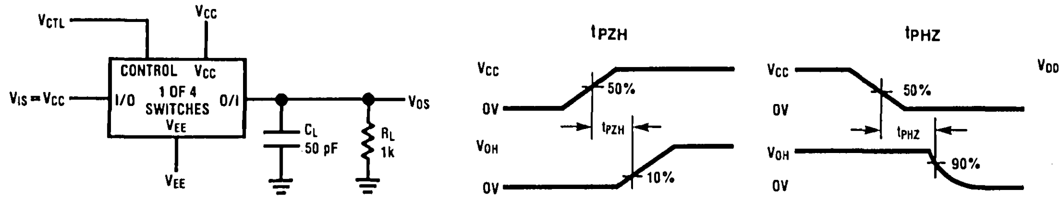
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5350-8 TL/F/5350-9

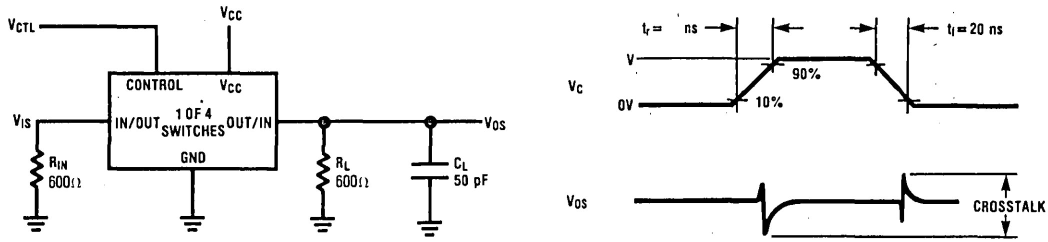
FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



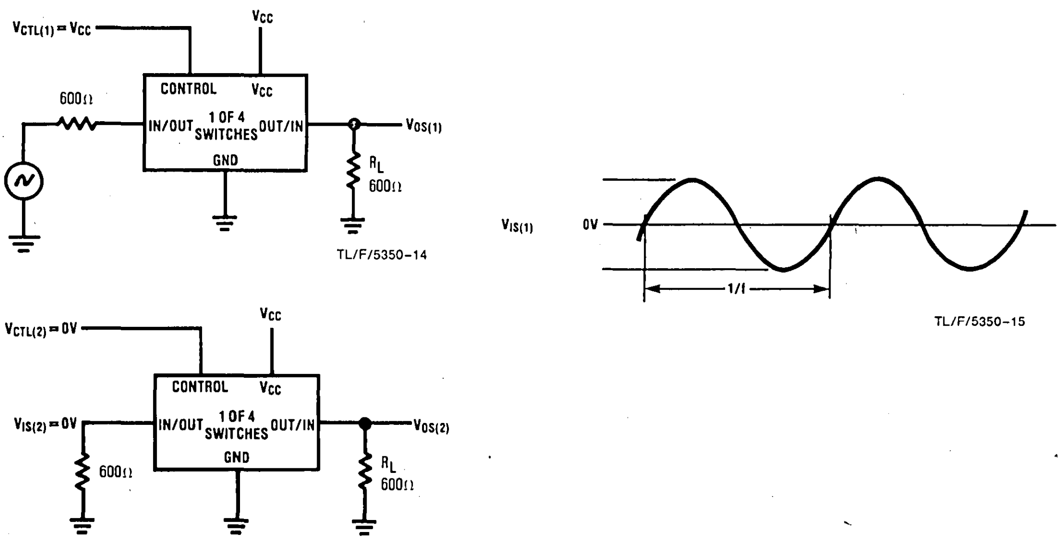
TL/F/5350-10 TL/F/5350-11

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5350-12 TL/F/5350-13

FIGURE 7. Crosstalk: Control Input to Signal Output



TL/F/5350-16

FIGURE 8: Crosstalk Between Any Two Switches

National Semiconductor

microCMOS

MM54HC4017/MM74HC4017
Decade Counter/Divider with 10 Decoded Outputs

General Description

The MM54HC4017/MM74HC4017 is a 5-stage Johnson counter with 10 decoded outputs that utilizes micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output transitions low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low.

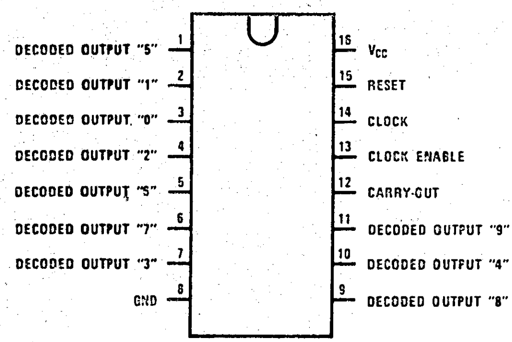
The MM54HC4017/MM74HC4017 is functionally and pinout equivalent to the CD4017BM/CD4017BC. It can drive up to 10 low power Schottky equivalent loads. All inputs are protected from damage due to static discharge by diodes from V_{CC} and ground.

Features

- Wide power supply range: 2–6V
- Typical operating frequency: 30 MHz
- Fanout of 10 LS-TTL loads.
- Low quiescent current: 80 μA (74HC series)
- Low input current: 1.0 μA

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5351-1

MM54HC4017/MM74HC4017

54HC4017 (J) 74HC4017 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		26	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable Decode-Out Lines		27	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		23	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		23	40	ns
t_S	Minimum Clock Inhibit Data Set-Up Time		12	20	ns
t_W	Minimum Clock or Reset Pulse Width		8	16	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns

AC Electrical Characteristics $V_{CC}=2.0–6.0V$, C_L50 pF $t_r=t_f=6$ ns (unless otherwise specified)

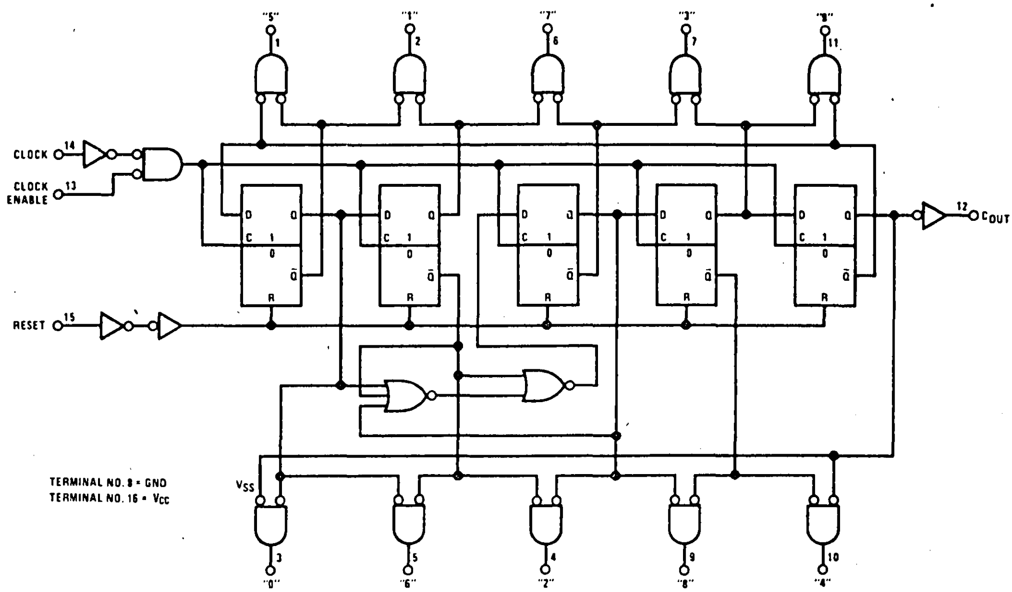
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	2.0V 4.5V 6.0V		4 20 23	3 16 18	3 13 15	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		2.0V 4.5V 6.0V	89 25 20	250 50 43	312 63 54	375 75 65	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Decode Out Line		2.0V 4.5V 6.0V	90 25 20	250 50 43	312 63 54	375 75 65	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		2.0V 4.5V 6.0V	82 22 18	230 46 39	288 58 49	345 69 59	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		2.0V 4.5V 6.0V	82 22 18	230 46 39	288 58 49	345 69 59	ns ns ns
t_W	Minimum Reset or Clock Pulse Width		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 21	ns ns ns
t_{REM}	Minimum Reset Removal Time		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Minimum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic and Timing Diagrams

MM54HC4017/MM74HC4017



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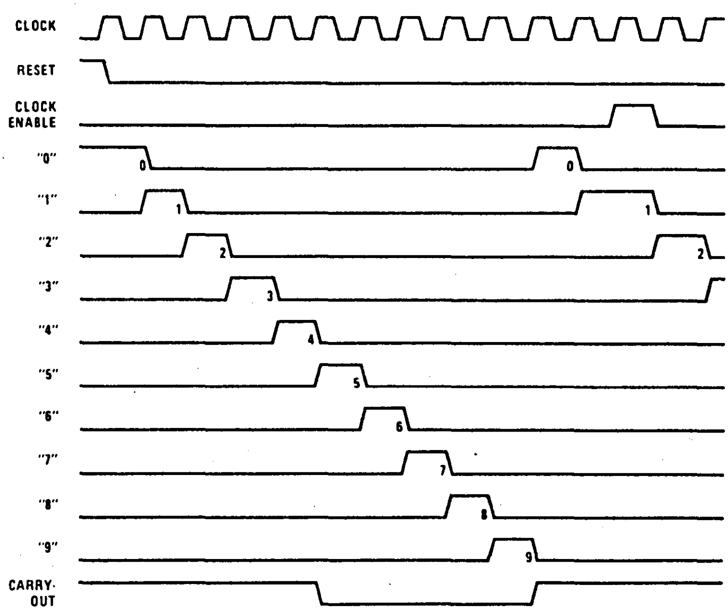


TL/F/5351-3

National Semiconductor

microCMOS

MM54HC4020/MM74HC4020 14 Stage Binary Counter MM54HC4024/MM74HC4024 7 Stage Binary Counter MM54HC4040/MM74HC4040 12 Stage Binary Counter

General Description

The MM54HC4020/74HC4020, MM54HC4024/74HC4024, MM54HC4040/74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4020 is a 14 stage counter, the 'HC4040 is a 12 stage counter, and the 'HC4024 is a 7 stage counter. All these devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

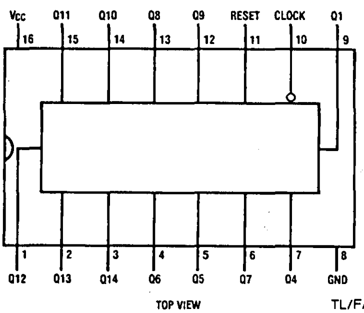
These devices are pin equivalent to the CD4020, CD4024 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Output drive capability: 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Packages



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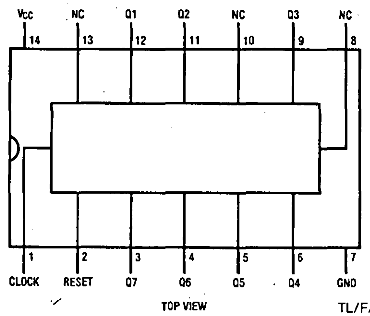
MM54HC4020/MM74HC4020

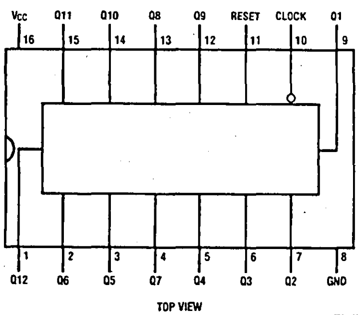
54HC4020 (J) 74HC4020 (J, N)



TL/F/5216-2

MM54HC4024/MM74HC4024

54HC4024 (J) 74HC4024 (J, N)



TL/F/5216-3

MM54HC4040/MM74HC4040

54HC4040 (J) 74HC4040 (J, N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to Any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency ('4020 and '4040)		2.0V 4.5V 6.0V	10 40 50	4 20 24	3 16 19	3 13 16	MHz MHz MHz
f_{MAX}	Maximum Operating Frequency ('4024)		2.0V 4.5V 6.0V	10 50 60	5 25 29	4 20 23	3 17 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V 4.5V 6.0V	80 21 18	210 42 36	265 53 45	313 63 53	ns ns ns
t_{PHL}	Maximum Propagation Delay Reset to Q ('4024 only)		2.0V 4.5V 6.0V	80 21 18	210 42 36	265 53 45	313 63 53	ns ns ns
t_{PHL}	Maximum Propagation Delay Reset to Any Q ('4020 and '4040)		2.0V 4.5V 6.0V	72 24 20	240 40 41	302 60 51	358 72 61	ns ns ns
t_{REM}	Minimum Reset Removal Time		2.0V 4.5V 6.0V		100 20 16	126 25 21	149 50 25	ns ns ns
t_W	Minimum Pulse Width		2.0V 4.5V 6.0V		90 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 10 9	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time				1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

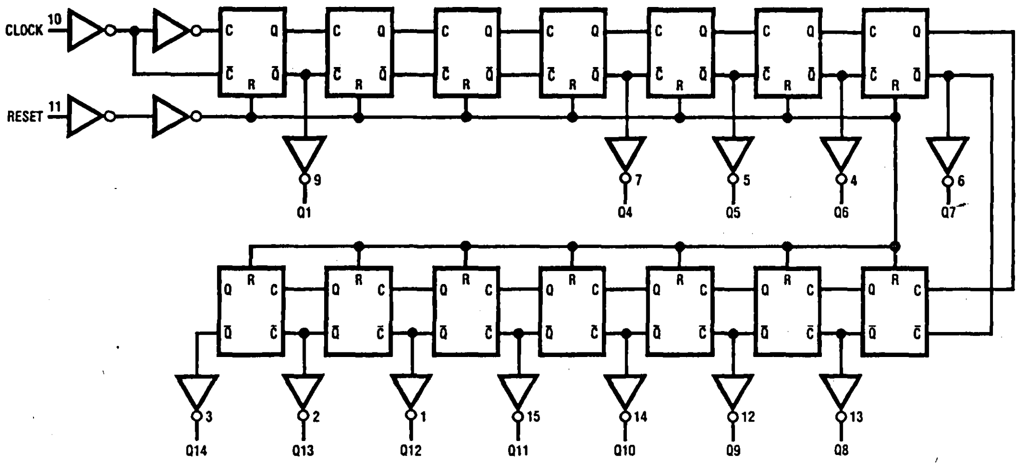
Note 5: Typical Propagation delay time to any output can be calculated using: $t_P = 17+12(N-1)$ ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 7: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams

MM54HC4020/MM74HC4020



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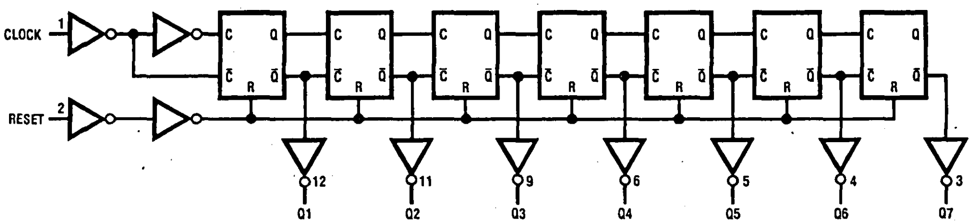
MM54HC4024/MM74HC4024



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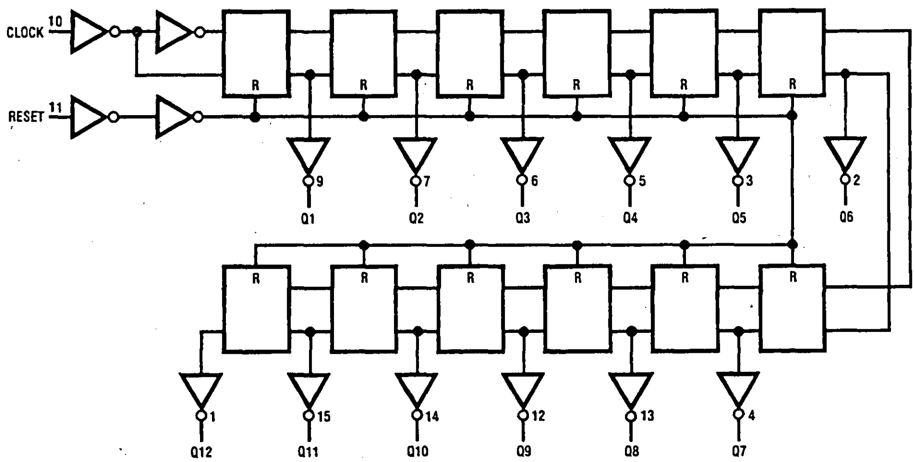
MM54HC4040/MM74HC4040



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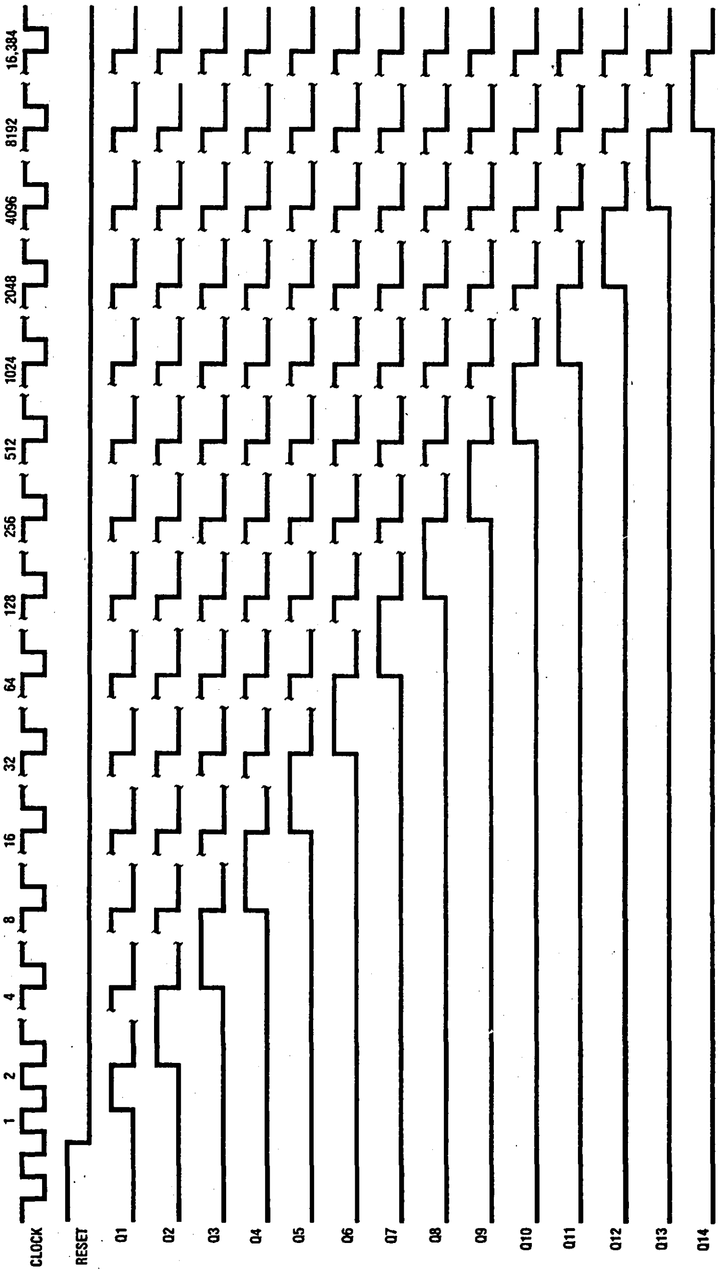
Timing Diagram



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National Semiconductor

PRELIMINARY

microCMOS

MM54HC4046/MM74HC4046 CMOS Phase Lock Loop

General Description

The MM54HC4046/MM74HC4046 is a low power phase lock loop utilizing 3.5μ silicon-gate P-well microCMOS Technology to obtain high frequency operation both in the phase comparator and VCO sections. This device contains a low power linear voltage controlled oscillator (VCO), a source follower, and three phase comparators. The three phase comparators have a common signal input and a common comparator input. The signal input has a self biasing amplifier allowing signals to be either capacitively coupled to the phase comparators with a small signal or directly coupled with standard input logic levels. This device is similar to the CD4046 except that the Zener diode of the metal gate CMOS device has been replaced with a third phase comparator.

Phase comparator I is an exclusive OR (XOR) gate. It provides a digital error signal that maintains a 90 phase shift between the VCO's center frequency and the input signal (50% duty cycle input) waveforms. This phase detector is more susceptible to locking onto harmonics of the input frequency than phase comparator I, but provides better noise rejection.

Phase comparator III is an SR flip-flop gate. It can be used to provide the phase comparator functions and is similar to the first comparator in performance.

Phase comparator II is an edge sensitive digital sequential network. Two signal outputs are provided, a comparator output and a phase pulse output. The comparator output is a TRI-STATE® output that provides a signal that locks the VCO output signal to the input signal with 0 phase shift between them. This comparator is more susceptible to noise throwing the loop out of lock, but is less likely to lock onto harmonics than the other two comparators.

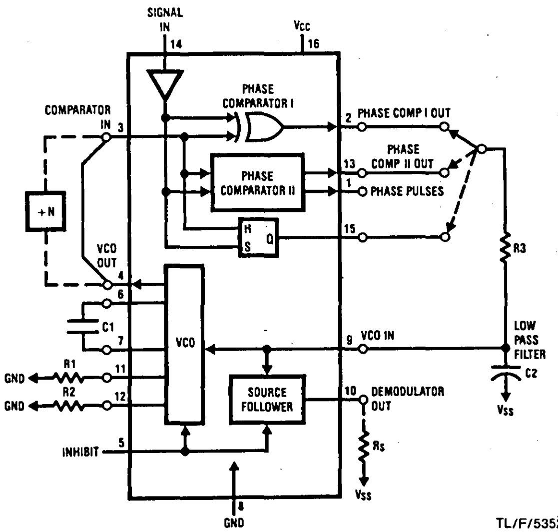
In a typical application all three comparators feed an external filter network which in turn feeds the VCO input. This input is a very high impedance CMOS input which also drives the source follower. The VCO's operating frequency is set by three external components connected to the C1A, C1B, R1 and R2 pins. An inhibit pin is provided to disable the VCO and the source follower, providing a method of putting the IC in a low power state.

The source follower is a MOS transistor whose gate is connected to the VCO input and whose drain connects the Demodulator output. This output normally is used by tying a resistor from pin 10 to ground, and provides a means of looking at the VCO input without loading down modifying the characteristics of the PLL filter.

Features

- Low dynamic power consumption: (V_{CC} = 4.5V)
- Maximum VCO operating frequency: 20 MHz (V_{CC} = 4.5V)
- Fast comparator response time (V_{CC} = 4.5V)
  - Comparator I: 20 ns
  - Comparator II: 25 ns
  - Comparator III: 20 ns
- VCO has high linearity and high temperature stability

Block and Connection Diagrams



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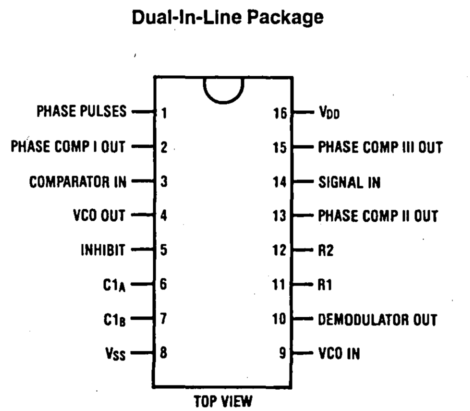

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Absolute Maxmum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to + 7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 8.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 3,5,9)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IN}	Maximum Input Current (Pin 14)	$V_{IN}=V_{CC}$ or GND	6.0V		2	3	4	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{G}=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 2.0 to 6.0V, CL = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified).

Symbol	Parameters	Conditions	V_{CC}	T = 25°C Typ	T = 25°C Guaranteed Limits	74HC Guaranteed Limits	54HC Guaranteed Limits	Units
	AC Coupled Input Sensitivity, Signal In	C (series) = 100 pF, f_{IN} = 500 kHz	2.0V 4.5V 6.0V	100 200 300	200 400 600	225 450 650	250 500 700	mV mV mV
t_r, t_f	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 9 8	75 15 12	95 19 15	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
Phase Comparator I								
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	58 20 18	165 35 30	206 44 38	250 52 45	ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance							pF
Phase Comparator II								
t_{PHL}, t_{PLH}	Maximum Propagation Delay Comp. Output		2.0V 4.5V 6.0V	60 20 18	150 30 25	190 38 32	225 45 38	ns ns ns
t_{PZL}	Maximum TRI-STATE Enable Time		2.0V 4.5V 6.0V	60 20 18	150 30 25	190 38 32	225 45 38	ns ns ns
t_{PZH}	Maximum TRI-STATE Enable Time		2.0V 4.5V 6.0V	72 22 19	200 40 34	250 50 42	300 60 51	ns ns ns
t_{PLZ}	Maximum TRI-STATE Disable Time		2.0V 4.5V 6.0V	72 22 19	200 40 34	250 50 42	300 60 51	ns ns ns
t_{PHZ}	Maximum TRI-STATE Disable Time		2.0V 4.5V 6.0V	72 22 19	200 40 34	250 50 42	300 60 51	ns ns ns
t_{PHL}	Maximum Propagation Delay High to Low to Phase Pulses		2.0V 4.5V 6.0V	72 22 19	200 40 34	250 50 42	300 60 51	ns ns ns
t_{PLH}	Maximum Propagation Delay Low to High to Phase Pulses		2.0V 4.5V 6.0V	72 22 19	200 40 34	250 50 42	300 60 51	ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance							pF
Phase Comparator III								
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V					ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance							pF

AC Electrical Characteristics (Continued)

V_{CC} = 2.0 to 6.0V, CL = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified).

Symbol	Parameters	Conditions	V_{CC}	T = 25°C		74HC	54HC	Units
				Typ	Guaranteed Limits			
Voltage Controlled Oscillator (Specified to operate from V_{CC} = 3.0V to 6.0V								
f_{MAX}	Maximum Operating Frequency	C1 = 10 pF, R1 = 100, R2 = 00 $VCO_{in} = V_{CC}$	4.5V 6.0V		20 25	18 23	15 20	MHz MHz
	Linearity	VCO_{in} = 2.25 ± 1V VCO_{in} = 3 ± 1.5V	4.5V 6.0V	1.0 1.0				% %
	Temperature-Frequency Stability	No Frequency Offset	4.5V 6.0V					%/ C %/ C
	Temperature-Frequency Stability	Frequency Offset	4.5V 6.0V					%/ C %/ C
	Duty Cycle			50				%
Demodulator Output								
	Offset Voltage VCO_{in}-V_{dem}	R_s = 1 kΩ		1.5	2.2	2.7	3.2	V
	Linearity	R_s = 5 kΩ	2.0V		0.1	0.2	0.3	%

Detailed Circuit Description

VOLTAGE CONTROLLED OSCILLATOR/SOURCE FOLLOWER

The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor 1 and capacitor C1 are selected to determine the center frequency of the VCO (see typical performance curves). R2 can be used to set the offset frequency with 0V at VCO input. If R2 is omitted the VCO range is from 0 Hz; as R2 is decreased, the offset frequency is increased. The effect of R2 is shown in the design information table and typical performance curves. By increasing the value of R2 the lock range of the PLL is decreased and the gain (volts/Hz) is increased. Thus, for a narrow lock range, large swings on the VCO input will cause less frequency variation.

Internally, the resistors set a current in a current mirror, as shown in *Figure 1*. The mirrored current drives one side of

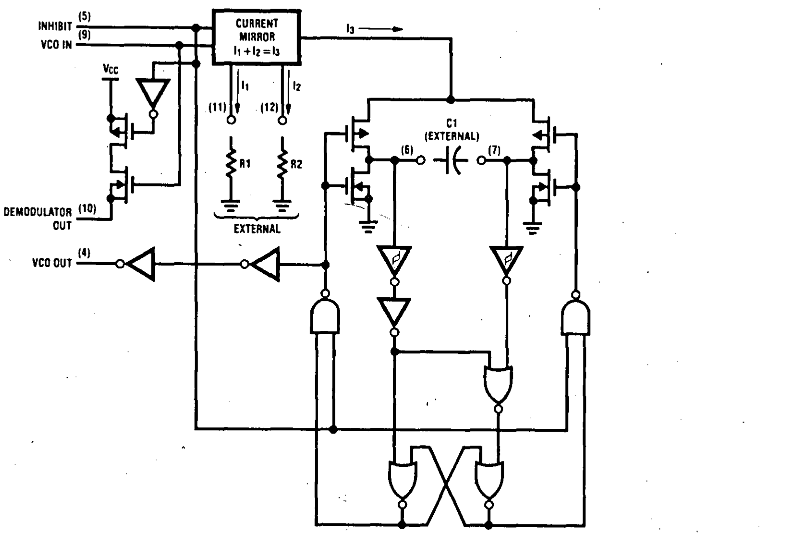

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FIGURE 1. Logic Diagram for VCO

Detailed Circuit Description (Continued)

the capacitor; once the capacitor charges up to the threshold of the Schmitt Trigger the oscillator logic flips the capacitor over and causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to pin 4.

The input to the VCO is a very high impedance CMOS input and thus will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance, a source follower transistor is provided. This transistor can be used by connecting a resistor to ground and its drain output will follow the VCO input signal.

An inhibit signal is provided to allow disabling of the VCO and the source follower. This is useful if the internal VCO is not being used, but an external one is. A logic high on inhibit disables the VCO and source follower.

The output of the VCO is a standard high speed CMOS output with an equivalent LS-TTL fanout of 10. The VCO output is approximately a square wave. This output can either directly feed the comparator input of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

PHASE COMPARATORS

All three phase comparators have two inputs, Signal In and Comparator In. The Signal In has a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled then this input requires logic levels the same as standard 54HC/74HC. The comparator input is a standard digital input. Both input structures are shown in *Figure 3.*

The outputs of these comparators are essentially standard 54HC/74HC voltage outputs (comparator II is TRI-STATE).

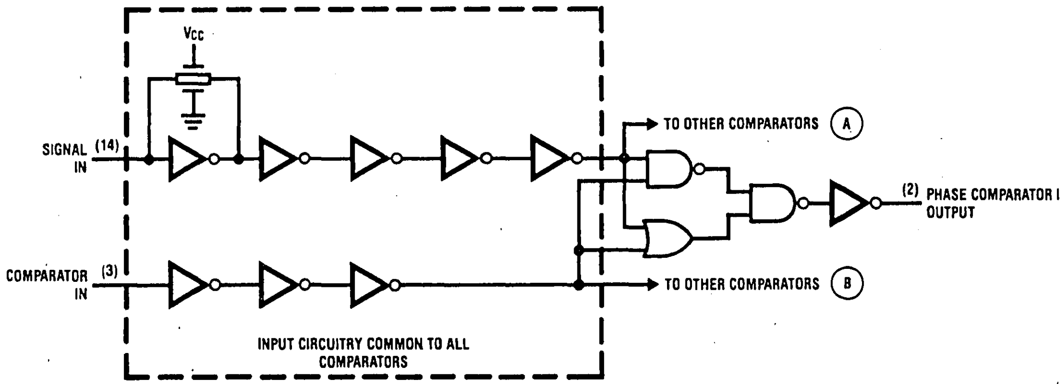

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FIGURE 3. Logic Diagram for Phase Comparator I and the Common Input Circuit for All Three Comparators

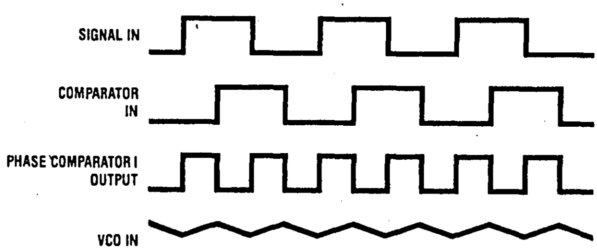

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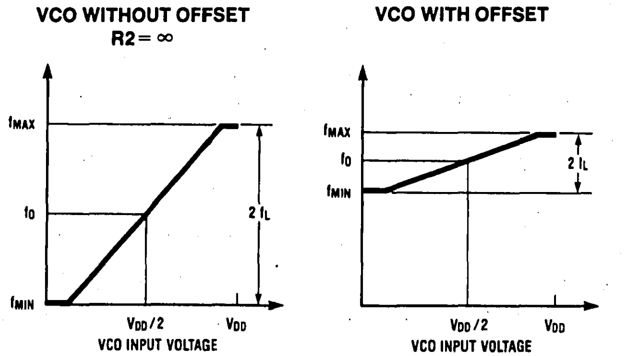
FIGURE 4. Typical Phase Comparator I Waveforms



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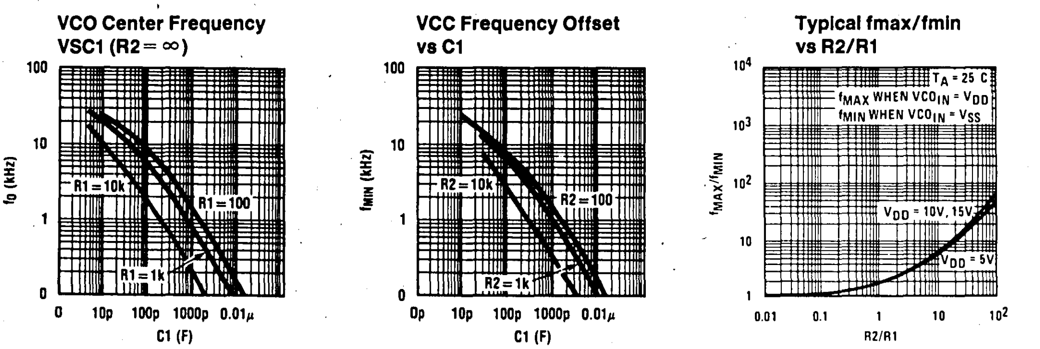
(a)

Comparator I		Comparator II		Comparator III	
$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$
–Given: f_0 –Use f_0 with *Figure 5a* to determine R1 and C1	–Given: f_0 and f_L –Calculate f_{min} from the equation $f_{min} = f_o - f_L$ –Use f_{min} with *Figure 5b* to determine R2 and C1 –Calculate f_{max}/f_{min} from the equation $f_{max}/f_{min} = f_o + f_L/f_o - f_L$ –Use f_{max}/f_{min} with *Figure 5c* to determine ratio R2/R1 to obtain R1	–Given: f_{max} –Calculate f_0 from the equation $f_o = f_{max}/2$ –Use f_0 with *Figure 5a* to determine R1 and C1	–Given: f_{min} and f_{max} –Use f_{min} with *Figure 5b* to determine R2 and C1 –Calculate f_{max}/f_{min} –Use f_{max}/f_{min} with *Figure 5c* to determine ratio R2/R1 to obtain R1		

(b)



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(c) (d) (e)

FIGURE 2. VCO Characteristics: a) Idealized Transfer Function
b) Determining External Components
c), d), e) Typical Frequency Characteristics versus Component Values

Detailed Circuit Description (Continued)

Thus in normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current output to the loop filter and this should be considered in the design. (The CD4046 also provides a voltage.)

Figure 5 shows the state tables for all three comparators.

PHASE COMPARATOR I

This comparator is a simple XOR gate similar to the 54/74HC86, and its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in *Figure 4.* The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector I is dependent on the loop filter employed. The capture range can be as large as the lock range, which is equal to the VCO frequency range.

To see how the detector operates, refer to *Figure 4.* When two square wave inputs are applied to this comparator, an output waveform whose duty cycle is dependent on the phase difference between the two signals results. As the phase difference increases, the output duty cycle increases and the voltage after the loop filter increases. Thus, in order to achieve lock when the PLL input frequency increases the VCO input, voltage must increase and the phase difference between comparator in and signal in will increase. At an input frequency equal to f_{min}, the VCO input is at 0V. This requires the phase detector output to be grounded; hence, the two input signals must be in phase. When the input frequency is f_{max}, the VCO input must be V_{CC} and the phase detector inputs must be 180° out of phase.

The XOR is more susceptible to locking onto harmonics of the signal input than the digital phase detector II. For instance, a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal to the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and the VCO range should be designed to prevent locking on to harmonics.

PHASE COMPARATOR II

This detector is a digital memory network. It consists of four flip-flops and some gating logic, a three state output and a phase pulse output as shown in *Figure 6*. This comparator acts only on the positive edges of the input signals and is thus independent of signal duty cycle.

Phase comparator II operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. *Figure 7* shows some typical loop waveforms. First assume that the signal input phase is leading the comparator input. This

Phase Comparator State Diagrams

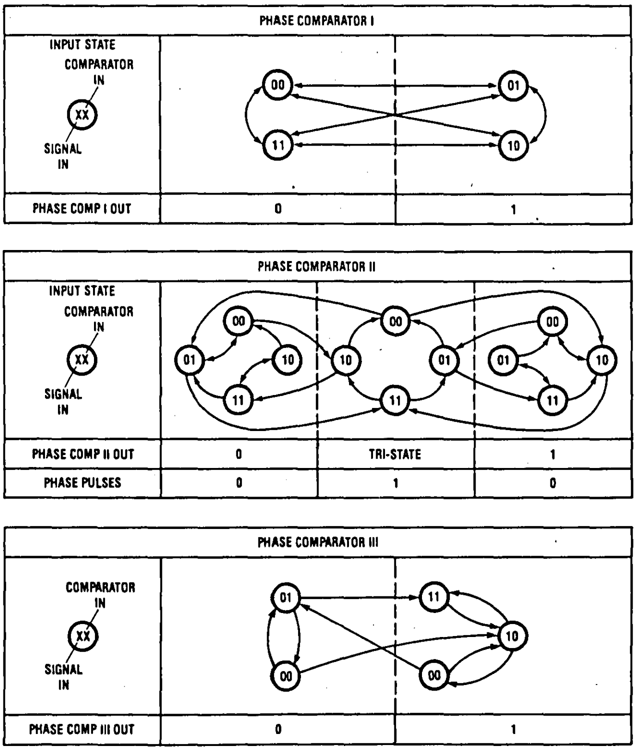

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FIGURE 5.

Detailed Circuit Description (Continued)

means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector II output is set high. This will cause the loop filter to charge up the VCO input, increasing the VCO frequency. Once the leading edge of the comparator input is detected, the output goes TRI-STATE holding the VCO input at the loop filter voltage. If the VCO still lags the signal then the phase detector will again charge up to VCO input for the time between the leading edges of both waveforms.

If the VCO leads the signal then when the leading edge of the VCO is seen, the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the signal is detected at which time the output disables itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveforms coincidental.

When the PLL is out of lock, the VCO will be running either slower or faster than the signal input. If it is running slower the phase detector will see more signal rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the signal, the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

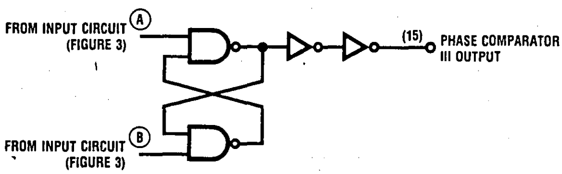
As one can see, when the PLL is locked the output of phase comparator II will be almost always disabled except for minor corrections at the leading edge of the waveforms. When the detector is TRI-STATE the phase pulse output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the comparator input and the signal input. The lock range of the PLL is the same as the capture range. Minimal power is consumed in the loop filter since in lock the detector output is a high impedance. Also, when no signal is present, the detector will see only VCO leading edges, so the comparator output will stay low, forcing the VCO to f_{min} operating frequency.

Phase comparator II is more susceptible to noise, causing the phase lock loop to unlock. If a noise pulse is seen on the signal input, the comparator treats it as another positive edge of the signal and will cause the output to go high until the VCO leading edge is seen, potentially for a whole signal input period. This would cause the VCO to speed up during that time. When using the phase comparator I, the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

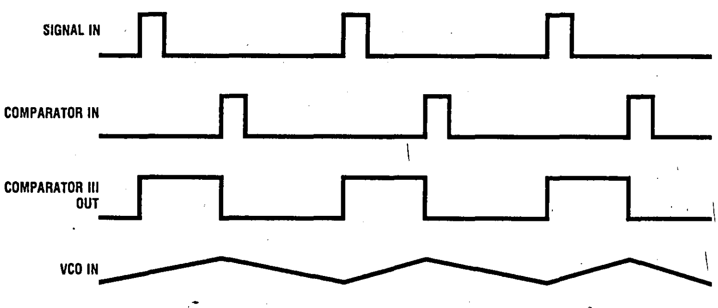
PHASE COMPARATOR III

This comparator is a simple SR flip-flop which can function as a phase comparator as shown in *Figure 8*. It has some similar characteristics to the edge sensitive comparator. To see how this detector works, assume input pulses are applied to the signal and comparator inputs as shown in *Figure 9*. When the signal input leads the comparator input, the flop is set. This will charge up the loop filter and cause the VCO to speed up, bringing the comparator into phase with the signal input. When using short pulses as input, this comparator behaves very similarly to the second comparator. But one can see that if the signal input is a long pulse, the output of the comparator will be forced to a one no matter how many comparator input pulses are received. Also, if the VCO input is a square wave (as it is) and the signal input is pulse, then the VCO will force the comparator output low much of the time. Therefore, it is ideal to condition the signal and comparator input to short pulses. This is most easily done by using a series capacitor.



TL/F/5352-11

FIGURE 8. Phase Comparator III Logic Diagram



TL/F/5352-12

FIGURE 9. Typical Waveforms for Phase Comparator III

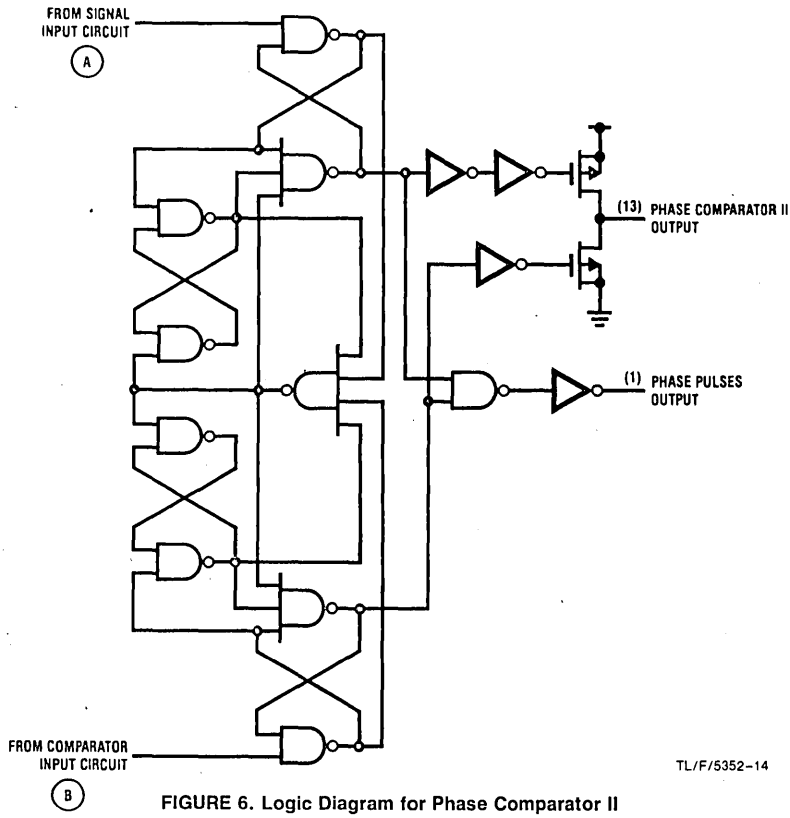


FIGURE 6. Logic Diagram for Phase Comparator II

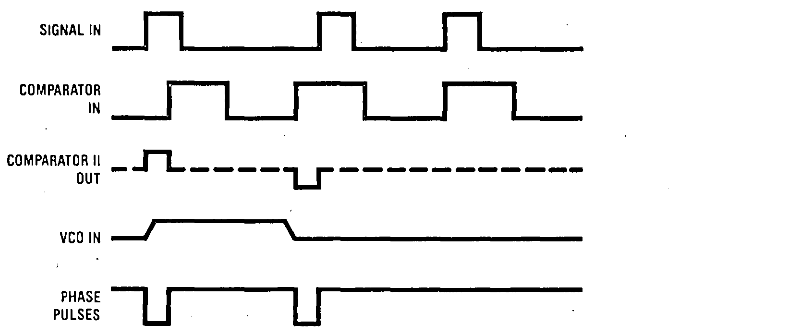


FIGURE 7. Typical Phase Comparator II Output Waveforms

National Semiconductor

microCMOS

MM54HC4049/MM74HC4049 Hex Inverting Logic Level Down Converter MM54HC4050/MM74HC4050 Hex Logic Level Down Converter

General Description

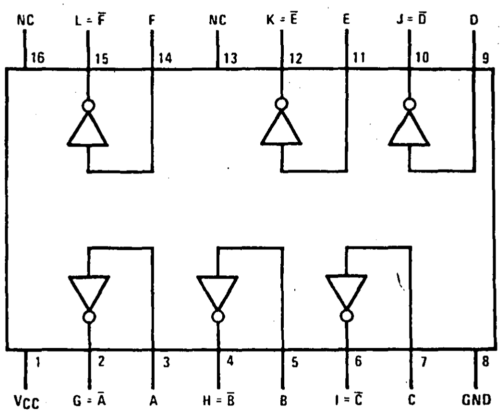
The MM54HC4049/MM74HC4049 and the MM54HC4050/MM74HC4050 utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC} thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. The MM54HC4049/MM74HC4049 is pin and functionally compatible to the CD4049BM/CD4049BC and the MM54HC4050/MM74HC4050 is compatible to the CD4050BM/CD4050BC

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA maximum (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



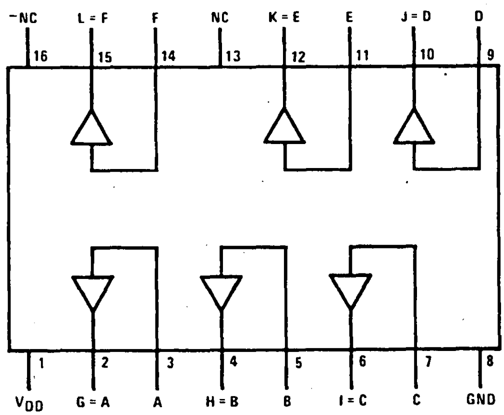
TOP VIEW

TL/F/5214-1

MM54HC4049/MM74HC4049

54HC4049 (J) 74HC4049 (J,N)

Dual-In-Line Package



TOP VIEW

TL/F/5214-2

MM54HC4050/MM74HC4050

54HC4050 (J) 74HC4050 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+18V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{ZK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input Voltage	0	15	V
(V_{IN})		V_{CC}	V
DC Output Voltage (V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40°C to 85°C	54HC T_A=−55°C to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
		V_{IN}=15V	6.0V		±0.5	±5	±5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40°$ to $85°C$	54HC $T_A=-55°$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	30 10 9	76 17 15	92 20 18	106 26 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4051/MM74HC4051 8 Channel Analog Multiplexer MM54HC4052/MM74HC4052 Dual 4 Channel Analog Multiplexer MM54HC4053/MM74HC4053 Triple 2 Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, Ground, and V_{EE}. This enables the connection of 0–5V logic signals when $V_{CC}=5V$ and an analog input range of ±5V when $V_{EE}=5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 Channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on". and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4 channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4 channel differential multiplexer.

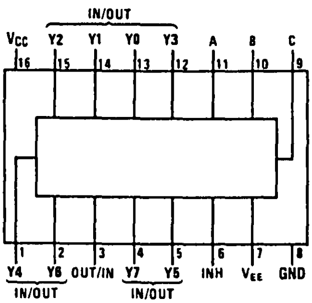
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configuration. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. (V_{CC}–V_{EE}=4.5V)
  30 typ. (V_{CC}–V_{EE}=9V)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

Connection Diagrams

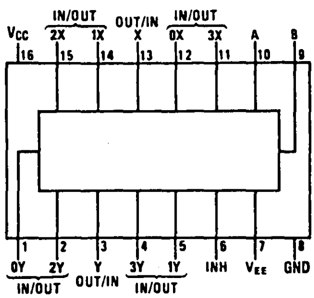
Dual-In-Line Package



TOP VIEW TL/F/5353-1

MM54HC4051/MM74HC4051

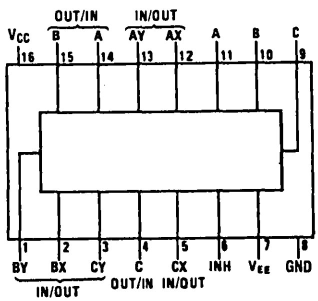
54HC4051 (J) 74HC4051 (J, N)



TOP VIEW TL/F/5353-2

MM54HC4052/MM74HC4052

54HC4052 (J) 74HC4052 (J, N)



TOP VIEW TL/F/5353-3

MM54HC4053/MM74HC4053

54HC4053 (J) 74HC4053 (J, N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
Supply Voltage(V_{EE})		0	−6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} to V_{EE} (Figure 1)	GND	4.5V	40				Ω
			−4.5V	4.5V	30				Ω
			−6.0V	6.0V	20				Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} or V_{EE} (Figure 1)	GND	2.0V	100				Ω
			GND	4.5V	40				Ω
			−4.5V	4.5V	20				Ω
			−6.0V	6.0V	15				Ω
R_{ON}	Maximum "ON"Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	GND	4.5V	10				Ω
			−4.5V	4.5V	5				Ω
			−6.0V	6.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2−6V				±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{CTL}=V_{IL} (Figure 2)	GND	6.0V	10				nA
			−6.0V	6.0V	20				nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND V_{CTL}=V_{IH} (Figure 3)	GND	6.0V	20				nA
			−6.0V	6.0V	40				nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	GND	6.0V		8	80	160	μA
			−6.0V	6.0V		16	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}-V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	25 5 4 3				ns ns ns ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	92 18 16 15				ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	65 28 18 16				ns ns ns
f_{MAX}	Minimum Switch Frequency Response 20log(V_I/V_O) = 3 dB		GND −4.5V	4.5V 4.5V	100 120				MHz MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
	Crosstalk, Switch Input to Output (Frequency at -50 dB								MHz
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input 4051 Common 4052 Common 4053 Common			15 90 45 30				pF
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AY
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AY
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AY
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms

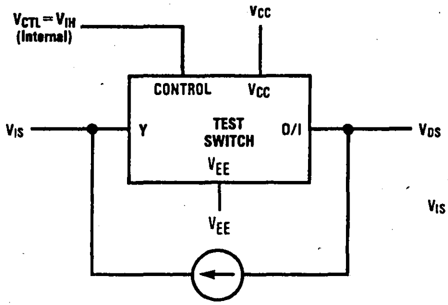


FIGURE 1. "ON" Resistance

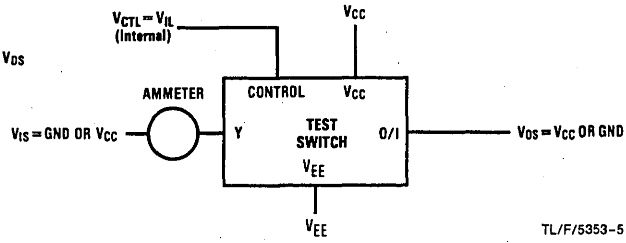


FIGURE 2. "OFF" Channel Leakage Current

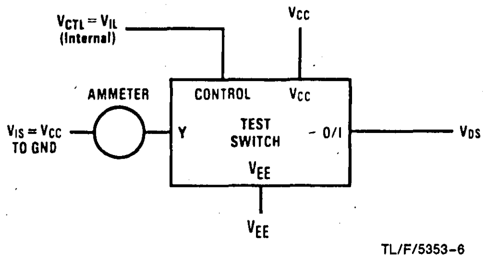


FIGURE 3. "ON" Channel Leakage Current

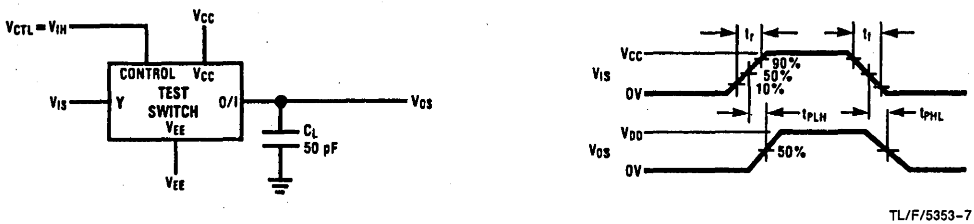


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

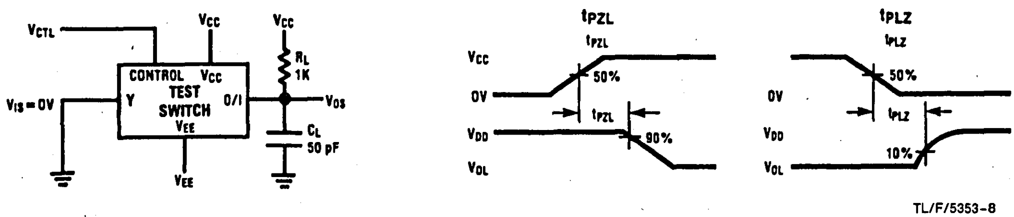


FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

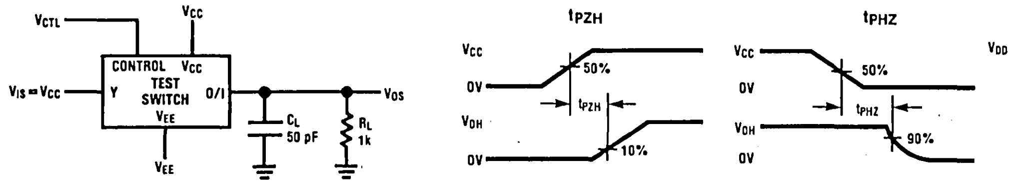


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FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

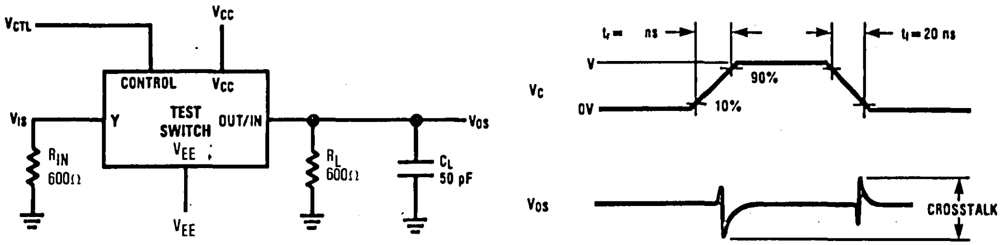

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FIGURE 7. Crosstalk: Control Input to Signal Output

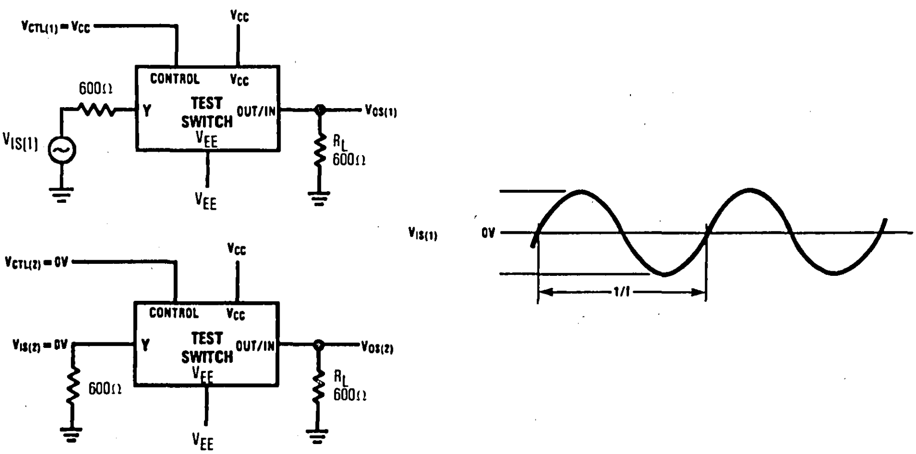

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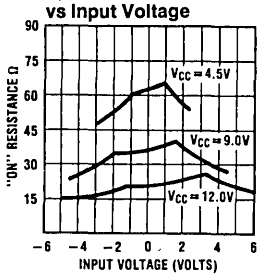
FIGURE 8. Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs Input Voltage

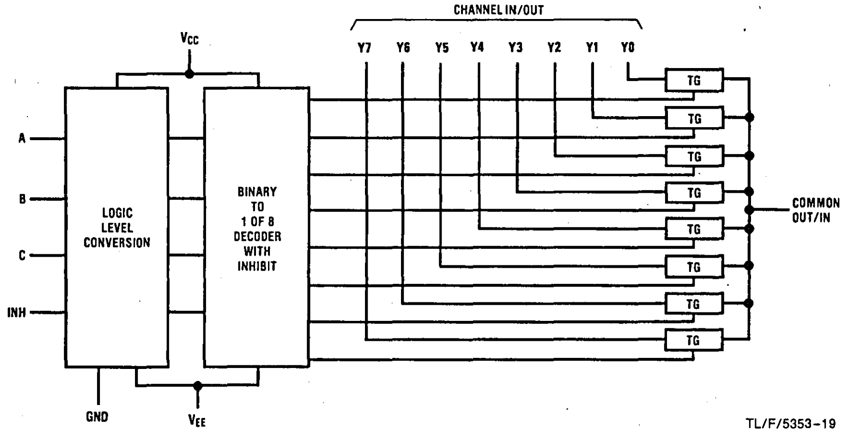


$V_{CC} = -V_{EE}$

TL/F/5353–18

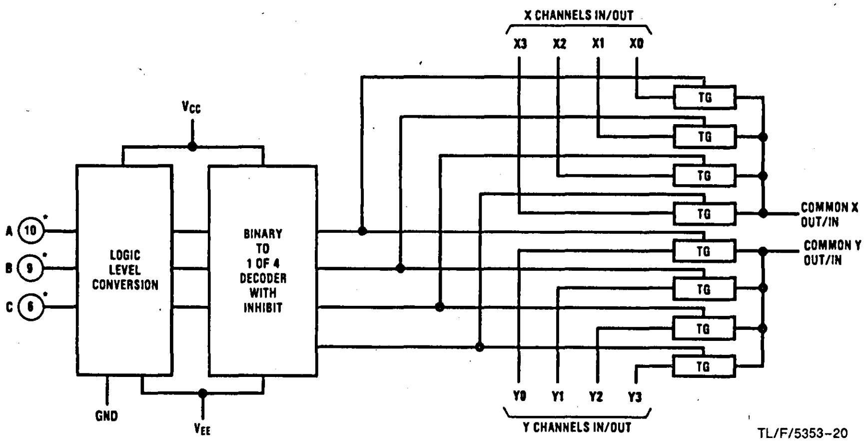
Logic Diagrams

MM54HC4051/MM74HC4051



TL/F/5353-19

MM54HC4052/MM74HC4052



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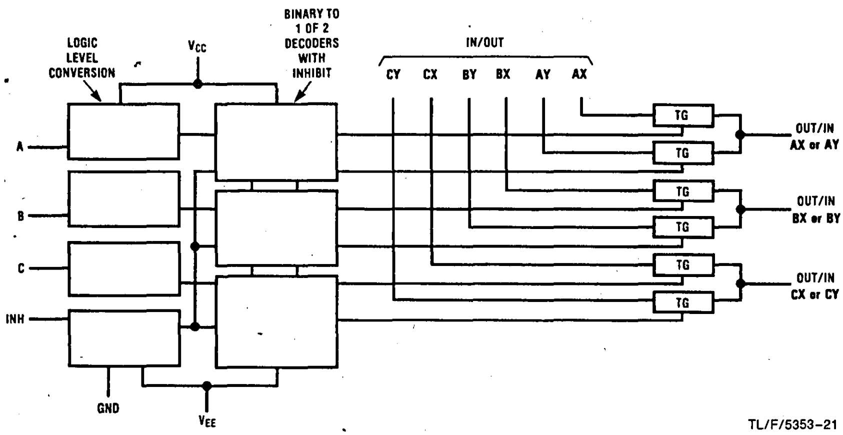
MM54HC4053/MM64HC4053



TL/F/5353-21

National Semiconductor

microCMOS

MM54HC4060/MM74HC4060 14 Stage Binary Counter

General Description

The MM54HC4060/MM74HC4060 is a high speed binary ripple carry counter. These counters are implemented utilizing microCMOS technology, 3.5 micron silicon gate P-well CMOS, to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4060 is a 14-stage counter which increments on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input. The 'HC4060 also has two additional inputs to enable easy connection of either an RC or crystal oscillator.

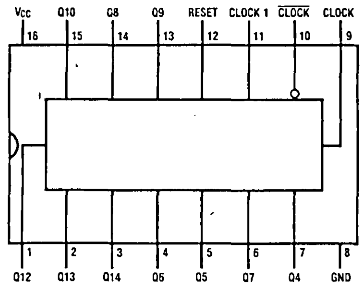
This device is pin equivalent to the CD4060. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

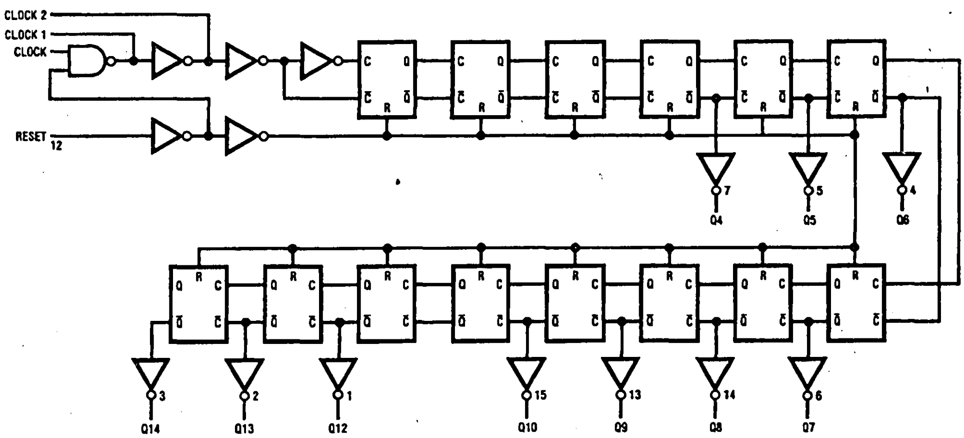


TL/F/5216-4

MM54HC4060/MM74HC4060

54HC4060 (J) 74HC4060 (J, N)

Logic Diagram



TL/F/5216-8

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current(I_{CD})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC Vcc or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	(except pins 11 and 12)	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	(except pins 11 and 12)	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|\leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C ceramic "J" package: −12 mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		40	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_4	(Note 5)	40	55	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Reset to Any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

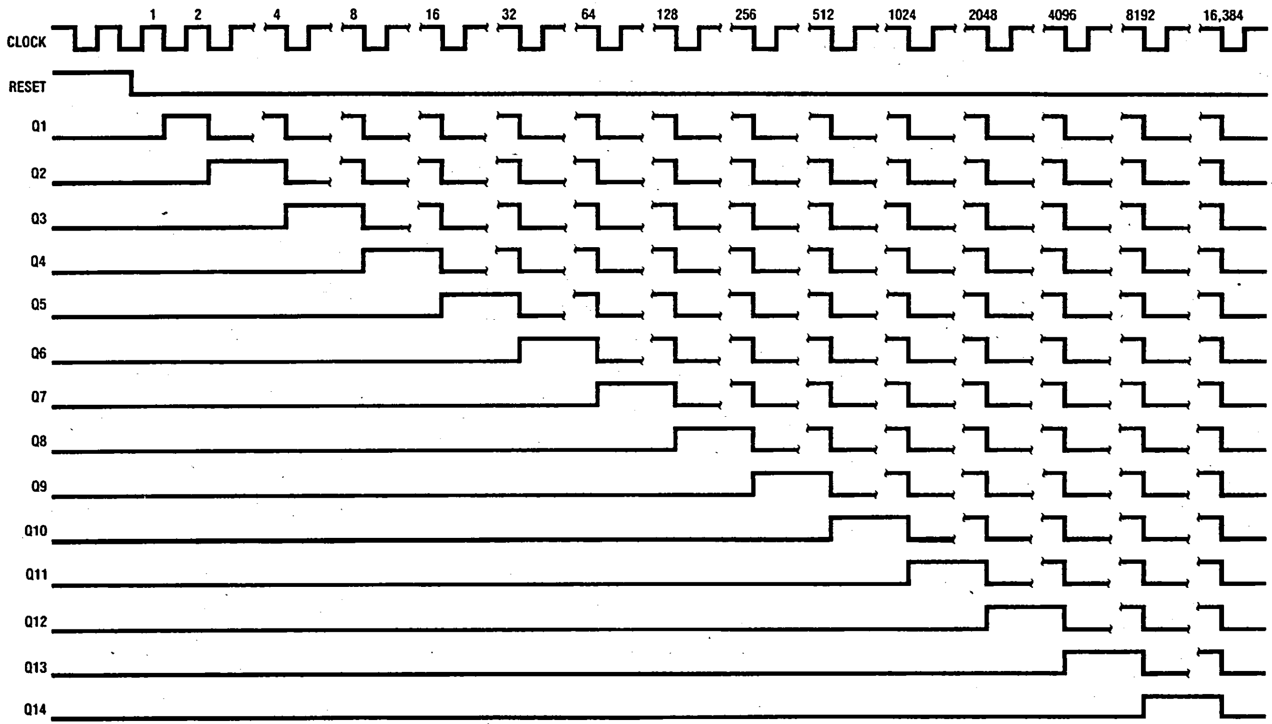
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		T_A 74HC $T_A=-40$ to 85°C	T_A 54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 40 50	4 20 24	3 16 19	3 13 16	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_4		2.0V 4.5V 6.0V	120 42 35	300 60 47	375 75 59	450 90 62	ns ns ns
t_{PHL}	Maximum Propagation Delay Reset to Any Q		2.0V 4.5V 6.0V	72 24 20	240 48 41	302 60 51	358 72 61	ns ns ns
t_{REM}	Minimum Reset Removal Time		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_W	Minimum Pulse Width		2.0V 4.5V 6.0V		80 16 14	100 20 17	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 10 9	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: t_P 17+12(N−1) ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 7: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Timing Diagram



TL/F/5216–11

microCMOS

MM54HC4066/MM74HC4066 Quad Analog Switch

General Description

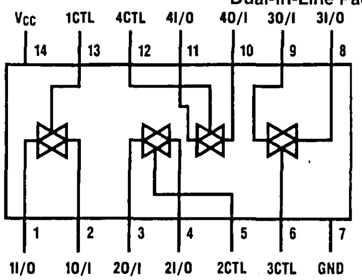
These devices are digitally controlled analog switches utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the '4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The '4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5350-1

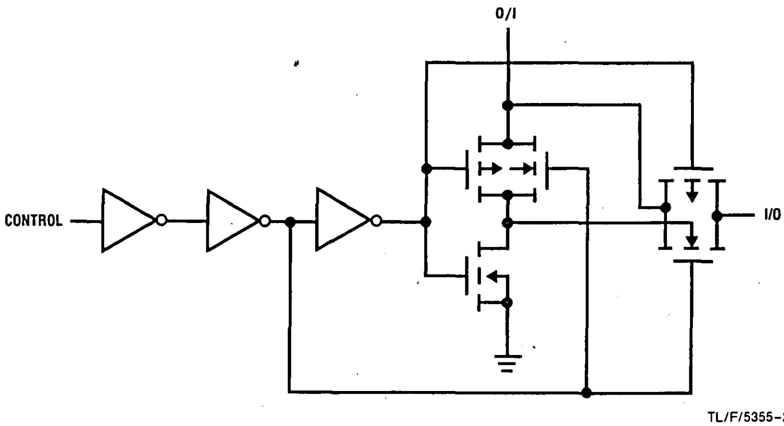
MM54HC4066/MM74HC4066

54HC4066 (J) 74HC4066 (J,N)

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5355-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=9.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	5.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA	4.5V	100				Ω
		V_{IS}=V_{CC} to GND	9.0V	50				Ω
		(Figure 1)	12.0	30				Ω
			2.0V	120				Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA	4.5V	50				Ω
		V_{IS}=V_{CC} or GND	9.0V	35				Ω
		(Figure 1)	12.0V	20				Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH}	4.5V	10				Ω
		V_{IS}=V_{CC} to GND	9.0V	5				Ω
			12.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2−6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND	5.5V	10				nA
		V_{IS}=GND or V_{CC}	9.0V	15				nA
		V_{CTL}=V_{IL} (Figure 2)	12.0V	20				nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND	5.5V	10				nA
		V_{CTL}=V_{IH}	9.0V	15				nA
		(Figure 3)	12.0V	20				nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND	5.5V		2.0	20	40	μA
		I_{OUT}=0 μA	9.0V		8.0	80	160	μA
			12.0V		16.0	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

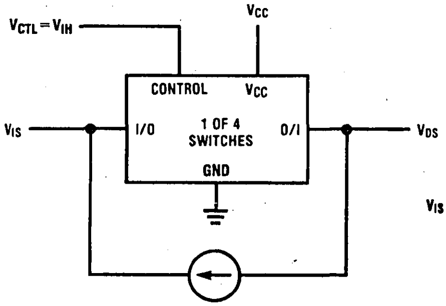
Note 5: At supply voltages (V_{CC}−V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified)

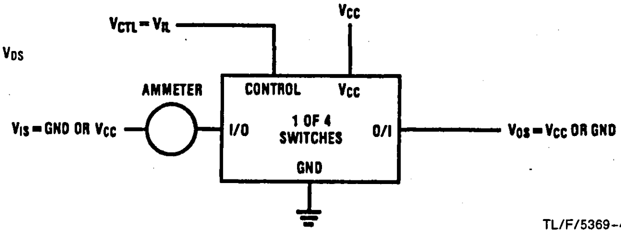
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	74HC T_A = −40 to 85°C Guaranteed Limits	54HC T_A = −55 to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50			ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	9	11	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	2.0V	32	80	100	120	ns
			4.5V	8	16	20	24	ns
			9.0V	6	14	18	21	ns
			12.0V	5	12	15	18	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	2.0V	45	150	187	225	ns
			4.5V	15	30	38	45	ns
			9.0V	10	20	25	30	ns
			12.0V	8	16	20	24	
f_{MAX}	Minimum Switch Frequency Response $20\log(V_I/V_O) = 3$ dB		4.5V	100				MHz
			9.0V	120				MHz
	Cross Talk Control to Switch	(Figure 7)	4.5V	180				mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	4.5V					MHz
	Crosstalk, Switch Input to Switch Output (Frequency at -50 dB)							MHz
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input		15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		5				pF

AC Test Circuits and Switching Time Waveforms



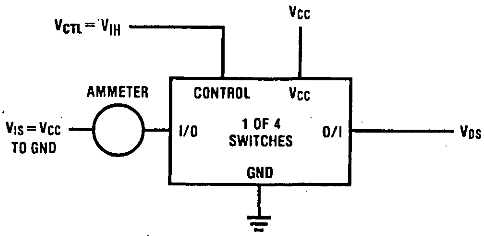
TL/F/5355-3

FIGURE 1. "ON" Resistance



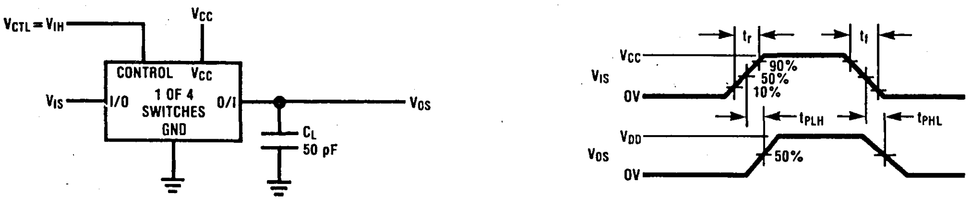
TL/F/5369-4

FIGURE 2. "OFF" Channel Leakage Current



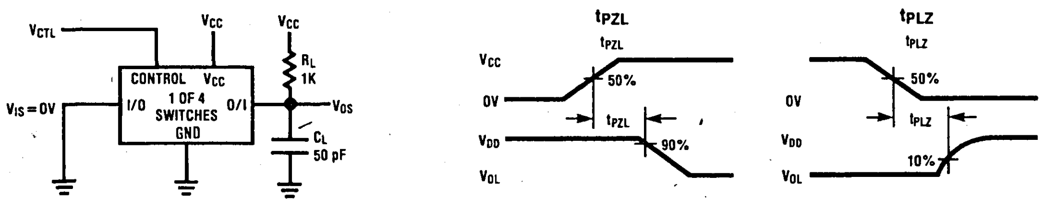
TL/F/5369-5

FIGURE 3. "ON" Channel Leakage Current



TL/F/5355-6

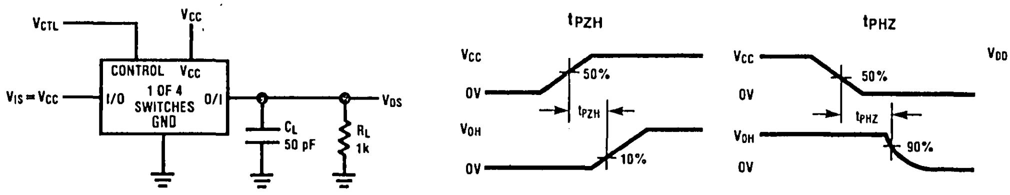
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5355-7

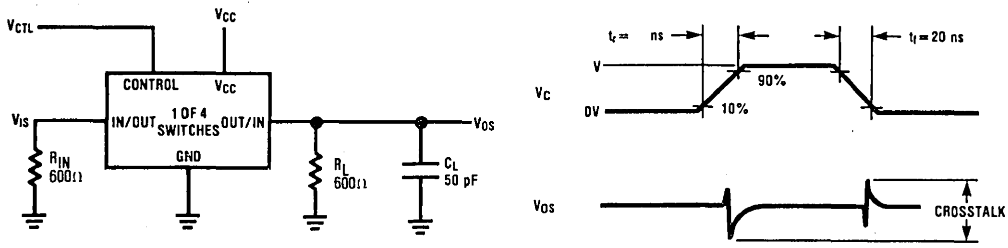
FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



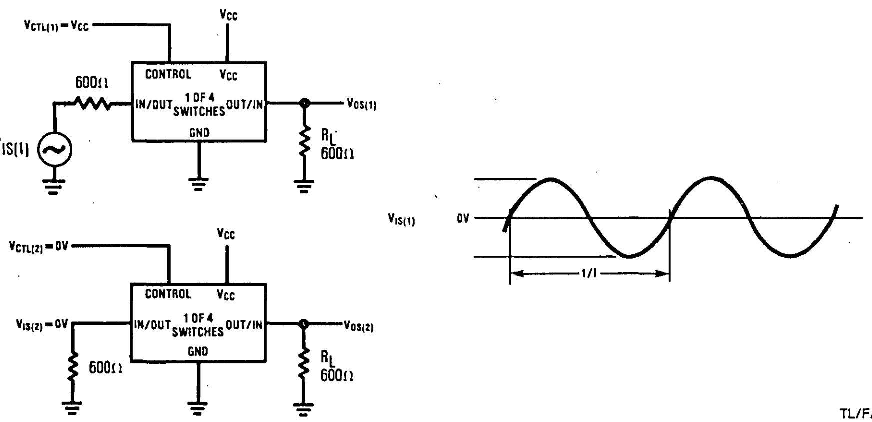
TL/F/5355-8

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5355-9

FIGURE 7. Crosstalk: Control Input to Signal Output

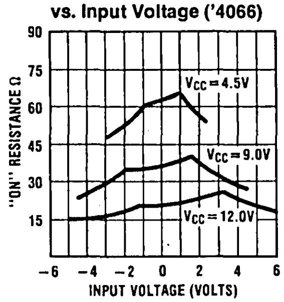


TL/F/5355-10

FIGURE 8: Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs. Input Voltage ('4066)



TL/F/5355-18

National Semiconductor

microCMOS

MM54HC4075/MM74HC4075 Triple 3-Input OR Gate

General Description

These OR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4075/74HC4075 is functionally equivalent and pin-out compatible with the CD4075B and MC14075B metal gate CMOS devices. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

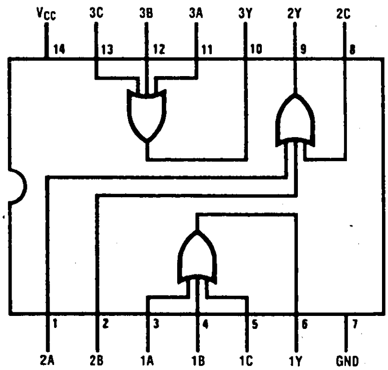
Features

- Typical propagation delay: 11 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

Y=A+B+C



TOP VIEW

TL/F/5155–1

MM54HC4075/MM74HC4075

54HC4075 (J)   74HC4075 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	40 12 10	115 23 20	145 29 25	171 34 29	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 10 9	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		30				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC4078/MM74HC4078 8-Input NOR/OR Gate

General Description

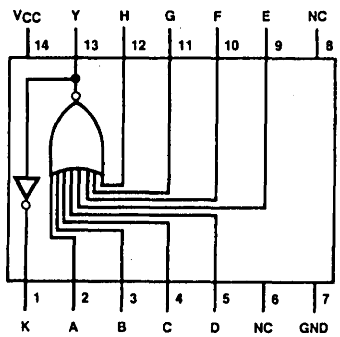
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. Both outputs are buffered, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC4078/74HC4078 is functionally equivalent and pin-out compatible with the CD4078B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



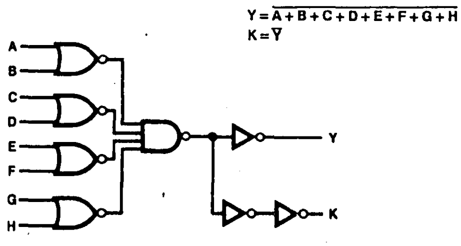
TOP VIEW

TL/F/5135-1

MM54HC4078/MM74HC4078

54HC4078 (J) 74HC4078 (J,N)

Logic Diagram



TL/F/5135-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC4078/MM74HC4078

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y to Output		14	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K to Output		16	24	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y to Output		2.0V 4.5V 6.0V	47 17 14	130 26 22	160 33 28	195 39 33	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K to Output		2.0V 4.5V 6.0V	50 20 17	140 28 24	175 35 30	210 42 36	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 10 9	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4316/MM74HC4316 Quad Analog Switch with Level Translator

General Description

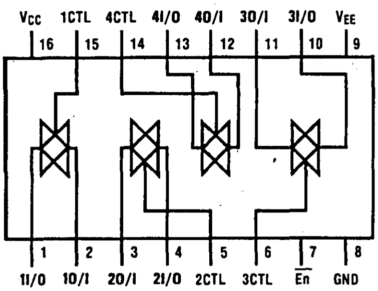
These devices are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the '4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The '4316 also has a common enable input in addition to each switch's control which when low will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5369-1

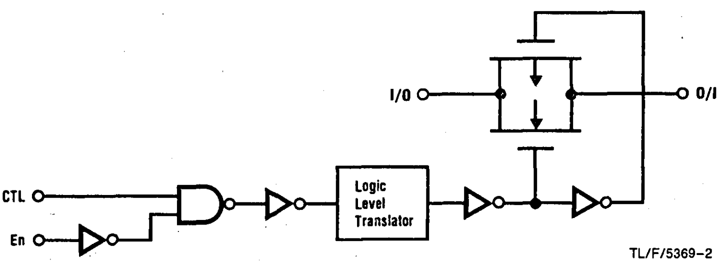
MM54HC4316/MM74HC4316

54HC4316 (J) 74HC4316 (J,N)

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Logic Diagram



TL/F/5369-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
Supply Voltage(V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Minimum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA	GND	4.5V	100				Ω
		V_{IS}=V_{CC} to V_{EE}	−4.5V	4.5V	40				Ω
		(Figure 1)	−6.0V	6.0V	30				Ω
			GND	2.0V	200				Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA	GND	4.5V	50				Ω
		V_{IS}=V_{CC} to V_{EE}	−4.5V	4.5V	20				Ω
		(Figure 1)	−6.0V	6.0V	15				Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH}	GND	4.5V	10				Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	5				Ω
			−6.0V	6.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND			6.0V	±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND	GND	5.5V	10				nA
		V_{IS}=GND or V_{CC}	−6.0V	6.0V	10				nA
		V_{CTL}=V_{IL} (Fig 2)							
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND	GND	5.5V	15				nA
		V_{CTL}=V_{IH}	−6.0V	6.0V	20				nA
		(Figure 3)							
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND	GND	6.0V		2.0	20	40	μA
		I_{OUT}=0 μA	−6.0V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

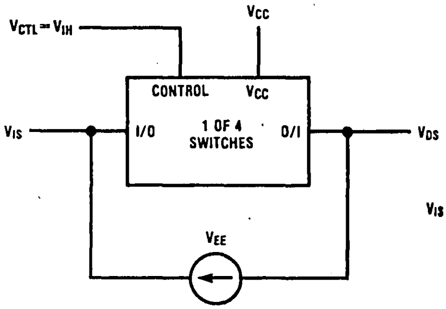
Note 5: At supply voltages (V_{CC}−V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V C_L = 50 pF (unless otherwise specified)

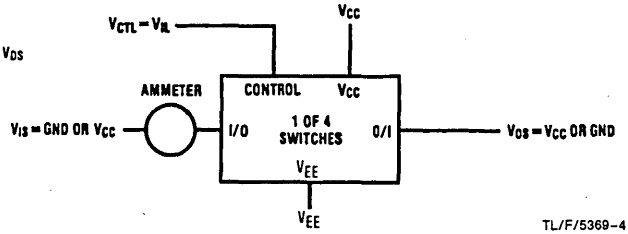
Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	38	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	10	12	ns
			−6.0V	6.0V	3	7	9	10	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	GND	2.0V	32	165	206	250	ns
			GND	4.5V	8	35	43	53	ns
			−4.5V	4.5V	6	30	37	45	ns
			−6.0V	6.0V	5	28	35.	42	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND	2.0V	45	165	206	250	ns
			GND	4.5V	15	35	43	53	ns
			−4.5V	4.5V	10	30	37	45	ns
			−6.0V	6.0V	8	28	35	42	
f_{MAX}	Minimum Switch Frequency Response $20\log(V_I/V_O) = 3$ dB		GND	4.5V	100				MHz
			−4.5V	4.5V	120				MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				$mV_{P\text{-}P}$
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
	Crosstalk, Switch Input to Switch Output (Frequency at -50 dB)								MHz
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND			5				pF

AC Test Circuits and Switching Time Waveforms



TL/F/5369-3

FIGURE 1. "ON" Resistance



TL/F/5369-4

FIGURE 2. "OFF" Channel Leakage Current

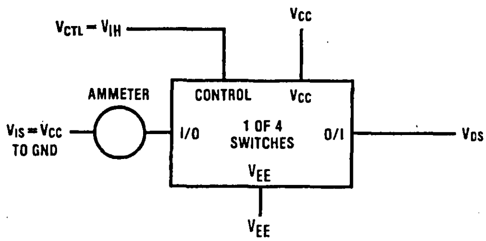


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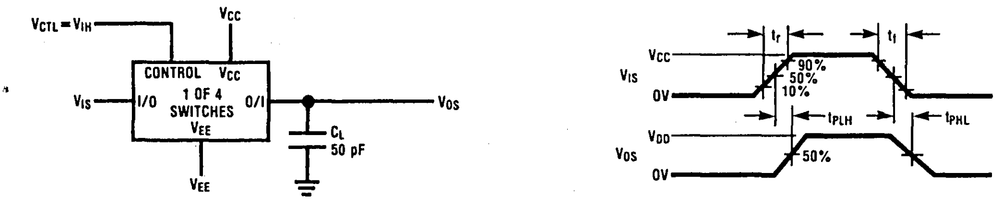
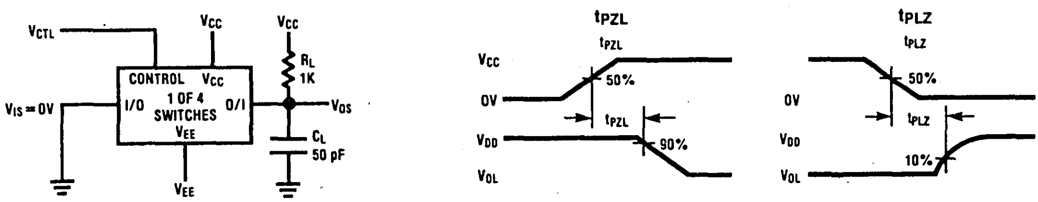
FIGURE 3. "ON" Channel Leakage Current



TL/F/5355-6

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5355-7

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

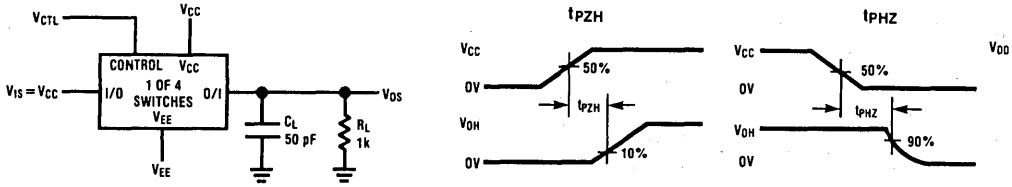


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

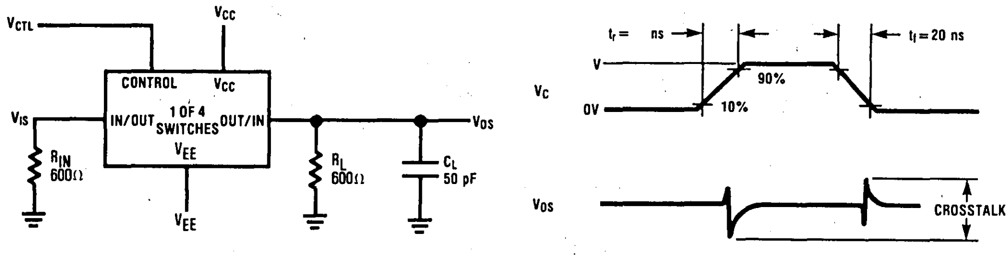


FIGURE 7. Crosstalk: Control Input to Signal Output

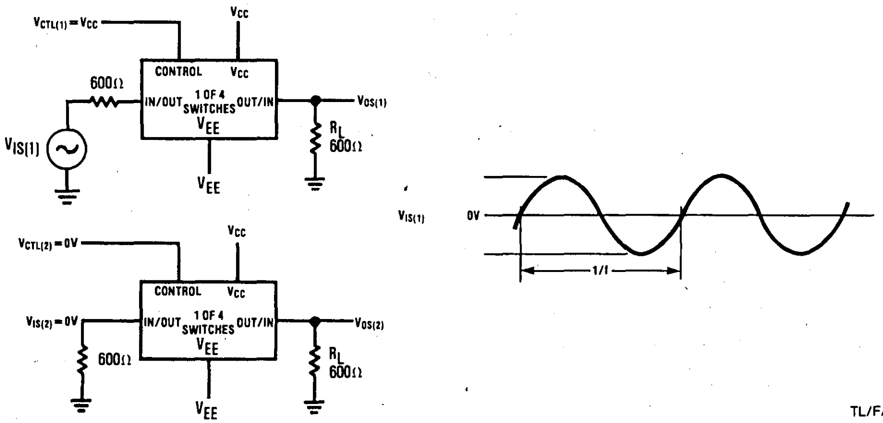
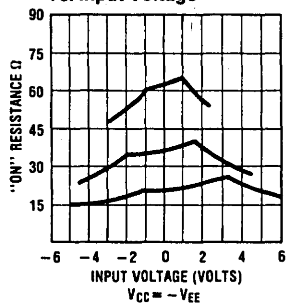


FIGURE 8: Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "ON" Resistance Vs. Input Voltage



TL/F/5369-17

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4351/MM74HC4351 8 Channel Analog Multiplexer with Latches MM54HC4352/MM74HC4352 Dual 4 Channel Analog Multiplexer with Latches MM54HC4353/MM74HC4353 Triple 2 Channel Analog Multiplexer with Latches

General Description

These multiplexers are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. The analog channel select lines are latched to enable storage of the selected channel. This storage register is composed of flow through latches that follow the data when $\overline{LE}$ is high and latch the data when $\overline{LE}$ is taken low.

Three supply pins are provided for V_{CC}, Ground, and V_{EE}. This enables the connection of 0-5V logic signals when $V_{CC}=5V$ and an analog input range of ±5V when $V_{EE}=-5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4351/MM74HC4351: This device connects together the outputs of 8 switches, thus achieving an 8 channel multiplexer. The binary code placed on the A, B, and C select lines determine which one of the eight switches is "on", and connects one of the eight inputs to the common output.

MM54HC4352/MM74HC4352: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4 channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4 channel differential multiplexer.

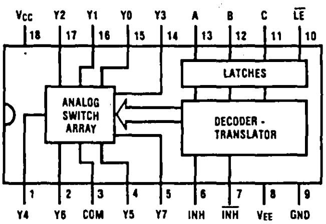
MM54HC4353/MM74HC4353: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of a single-pole-double throw configuration. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Typical Switch Enable Time: 18 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Logic level translation to enable 5V logic with ±5 analog signals
- Low quiescent current: 80 μA max. (74HC)
- Matched Switch characteristics.
- Latched Select Lines to enable interface to multiplexed data buses.

Connection Diagrams

Dual-In-Line Package



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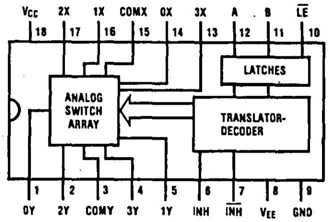
MM54HC4351/MM74HC4351

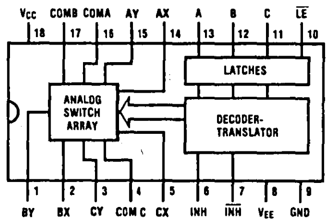
54HC4351 (J) 74HC4351 (J,N)



TL/F/5372-2

MM54HC4352/MM74HC4352

54HC4352 (J) 74HC4352 (J,N)



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MM54HC4353/MM74HC4353

54HC4353 (J) 74HC4353 (J,N)

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
Supply Voltage(V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T=25°C		74HC T=−40 to 85°C	54HC T=−55 to 125°C	Units
					Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA	GND	4.5V	40				Ω
		V_{IS}=V_{CC} to V_{EE}	−4.5V	4.5V	30				Ω
		(Figure 1)	−6.0V	6.0	20				Ω
			GND	2.0V	100				Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA	GND	4.5V	40				Ω
		V_{IS}=V_{CC} to V_{EE}	−4.5V	4.5V	20				Ω
		(Figure 1)	−6.0V	6.0V	15				Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH}	GND	4.5V	10				Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	5				Ω
			−6.0V	6.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND		6.0V		±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND	GND	6.0V	15				nA
		V_{IS}=GND or V_{CC}	−6.0V	6.0V	20				nA
		V_{CTL}=V_{IL} (Fig. 2)							
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND	GND	6.0V	15				nA
		V_{CTL}= V_{IH}	−6.0V	6.0V	20				nA
		(Figure 3)							
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND	GND	6.0V		8.0	80	160	μA
		I_{OUT}=0 μA	−6.0V	6.0V		16	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

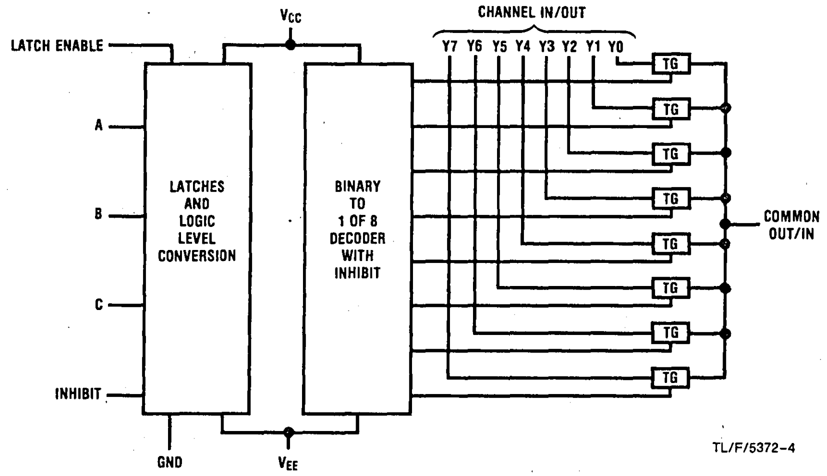
Note 5: At supply voltages (V_{CC}-V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V to −6V, C_L = 50 pF, (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25				ns
			GND	4.5V	5				ns
			−4.5V	4.5V	4				ns
			−6.0V	6.0V	3				ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	GND	2.0V	92				ns
			GND	4.5V	18				ns
			−4.5V	4.5V	16				ns
			−6.0V	6.0V	15				ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND	2.0V	65				ns
			GND	4.5V	20				ns
			−4.5V	4.5V	18				ns
			−6.0V	6.0V	16				
t_s	Maximum Setup Time, Data to LE			2.0V		100	125	150	ns
				4.5V		20	24	28	ns
				6.0V		17	21	24	ns
t_H	Maximum Hold Time, LE to Data			2.0V		0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
f_{MAX}	Minimum Switch Frequency Response $20\log(V_I/V_O) = -3$ dB	(Figure 6)	GND	4.5V	100				MHz
			−4.5V	4.5V	120				MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				mV_{PP}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
	Crosstalk, Switch Input to Output (Frequency at -50 dB)								MHz
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input			15				pF
		'4351 Common			90				
		'4352 Common			45				
		'4353 Common			30				
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Logic Diagrams



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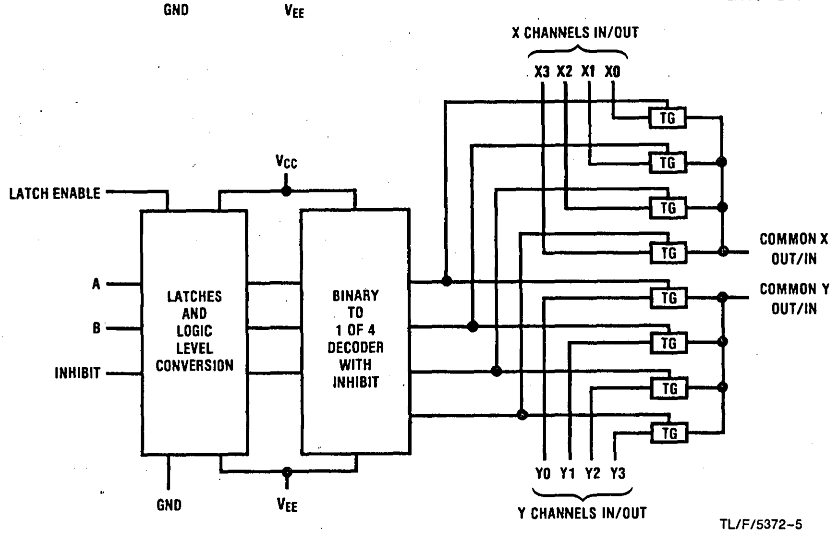

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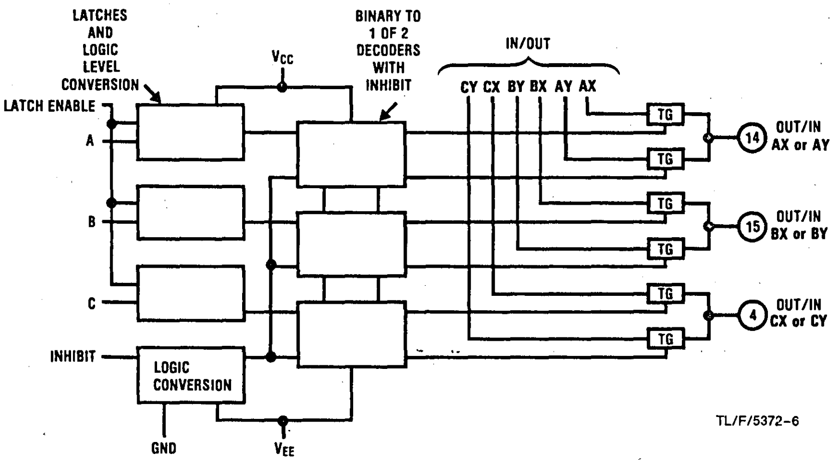

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Logic Diagrams (Continued)

'HC4351

Inh	$\overline{Inh}$	$\overline{LE}$	C	B	A	"On" Channel
H	X	X	X	X	X	None
X	L	X	X	X	X	None
L	H	H	L	L	L	Y0
L	H	H	L	L	H	Y1
L	H	H	L	H	L	Y2
L	H	H	L	H	H	Y3
L	H	H	H	L	L	Y4
L	H	H	H	L	H	Y5
L	H	H	H	H	L	Y6
L	H	H	H	H	H	Y7
L	H	L	X	X	X	Last Selected Channel "On"
X	X	↓	X	X	X	Selected Channel Latched

'HC4352

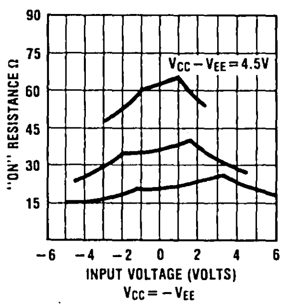
Inh	$\overline{Inh}$	$\overline{LE}$	B	A	"On" Channels	
					X	Y
H	X	X	X	X	None	
X	L	X	X	X	None	
L	H	H	0	0	0X	0Y
L	H	H	0	1	1Y	1Y
L	H	H	1	0	2Y	2Y
L	H	H	1	1	3Y	3Y
L	H	L	X	X	Last Selected Channels "On"	
X	X	↓	X	X	Selected Channels Latched	

'HC4353

Inh	$\overline{Inh}$	$\overline{LE}$	C	B	A	"On" Channels		
						C	B	A
H	X	X	X	X	X	None		
X	L	X	X	X	X	None		
L	H	H	L	L	L	CX	BX	AX
L	H	H	L	L	H	CX	BX	AY
L	H	H	L	H	L	CX	BY	AX
L	H	H	L	H	H	CX	BY	AY
L	H	H	H	L	L	CY	BX	AX
L	H	H	H	L	H	CY	BX	AY
L	H	H	H	H	L	CY	BY	AX
L	H	H	H	H	H	CY	BY	AY
L	H	L	X	X	X	Last Selected Channels "On"		
X	X	↓	X	X	X	Selected Channels Latched		

Typical Performance Characteristics

Typical "On" Resistance vs. Input Voltage



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AC Test Circuits and Switching Time Waveforms

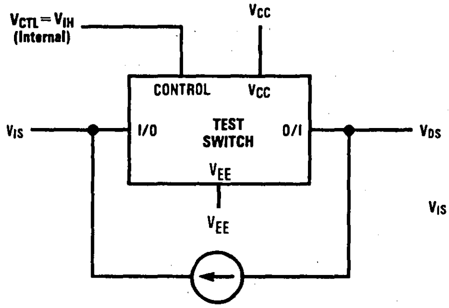

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FIGURE 1. "ON" Resistance

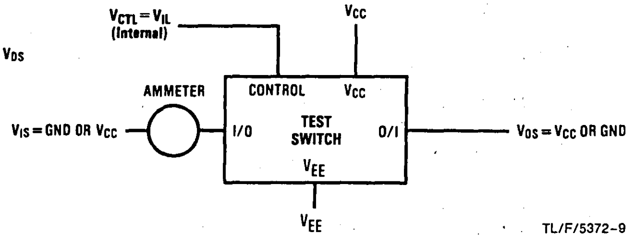

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FIGURE 2. "OFF" Channel Leakage Current

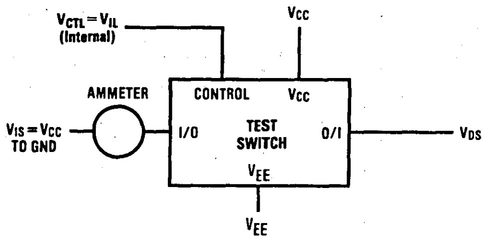

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FIGURE 3. "ON" Channel Leakage Current

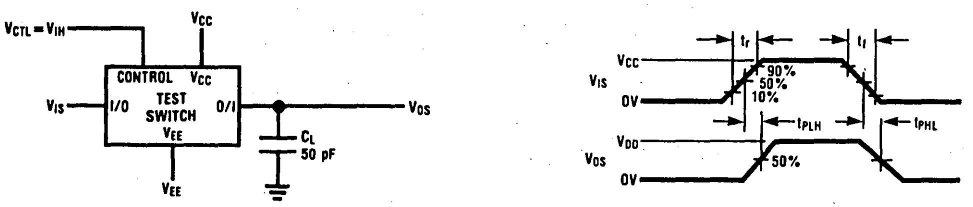

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FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

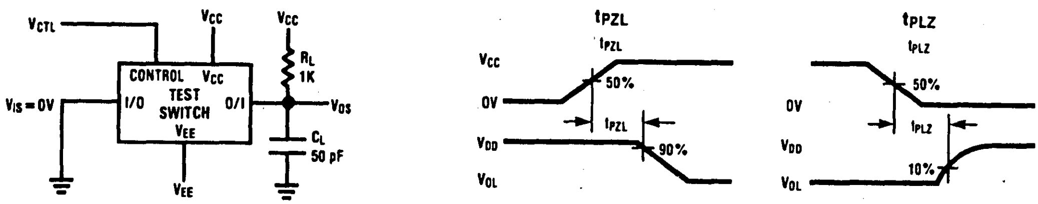

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FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

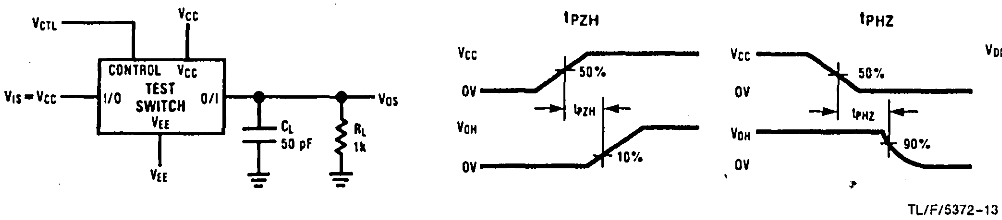


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

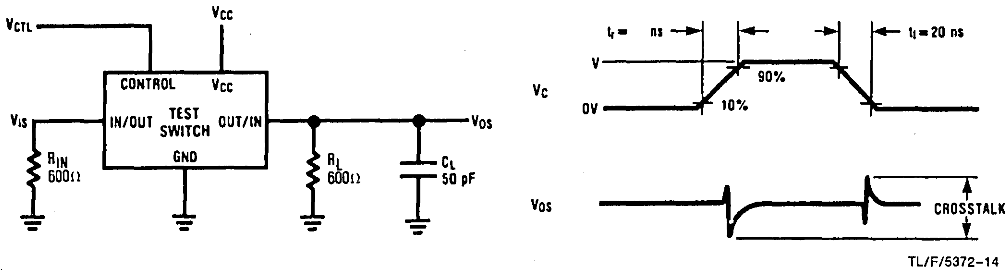


FIGURE 7. Crosstalk: Control Input to Signal Output

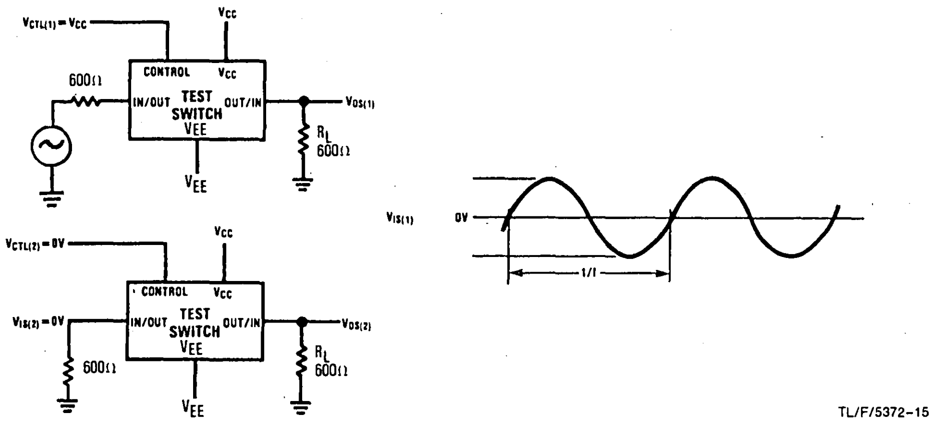


FIGURE 8: Crosstalk Between Any Two Switches

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4514/MM74HC4514 4-to-16 Line Decoder with Latch

General Description

This utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS decoder, which is well suited to memory address decoding or data routing application. It possesses high noise immunity and low power dissipation usually associated with CMOS circuitry, yet speeds comparable to low power Schottky TTL circuits. It can drive up to 10 LS-TTL loads.

The MM54HC4514/MM74HC4514 contain a 4-to-16 line decoder and a 4-bit latch. The latch can store the data on the select inputs, thus allowing a selected output to remain high even though the select data has changed. When the LATCH ENABLE input to the latches is high the outputs will change with the inputs. When LATCH ENABLE goes low the data on the select inputs is stored in the latches. The four select inputs determine which output will go high provided the INHIBIT input is low. If the INHIBIT input is high all outputs are held low thus disabling the decoder.

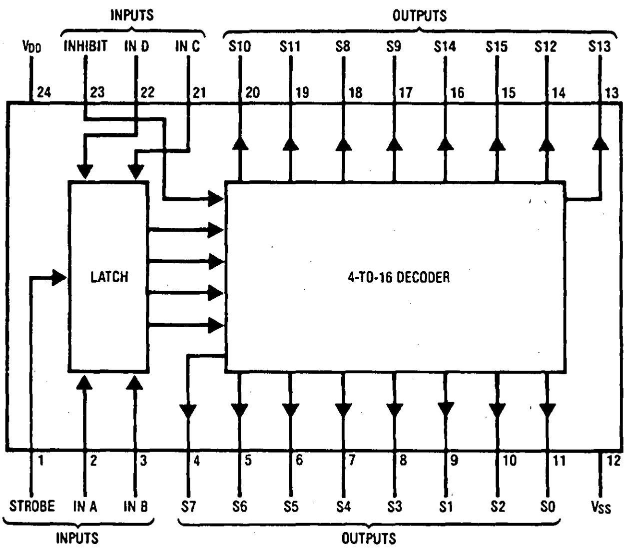
The MM54HC4514/MM74HC4514 is functionally and pinout equivalent to the CD4514BM/CD4514BC and the MC1451BA/MC1451BC. All inputs are protected against damage due to static discharge diodes from V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Low quiescent power: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5215-1

MM54HC4514/MM74HC4514

54HC4514 (J) 74HC4514 (J,N)

Truth Table

LE	Inhibit	Data Inputs D	C	B	A	Selected Output High
H	L	L	L	L	L	S0
H	L	L	L	L	H	S1
H	L	L	L	H	L	S2
H	L	L	L	H	H	S3
H	L	L	H	L	L	S4
H	L	L	H	L	H	S5
H	L	L	H	H	L	S6
H	L	L	H	H	H	S7
H	L	H	L	L	L	S8
H	L	H	L	L	H	S9
H	L	H	L	H	L	S10
H	L	H	L	H	H	S11
H	L	H	H	L	L	S12
H	L	H	H	L	H	S13
H	L	H	H	H	L	S14
H	L	H	H	H	H	S15
X	H	X	X	X	X	All Outputs = 0
L	L	X	X	X	X	Latched Data

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	30	ns
t_{PHL}	Maximum Propagation Delay LE to Output		18	30	ns
t_{PLH}	Maximum Propagation Delay LE to Output		24	40	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		16	30	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		24	40	ns
t_S	Minimum Set Up Time, Date to LE			20	ns
t_H	Minimum Hold Time, LE to Data			5	ns
t_H	Minimum Pulse Width, Latch Enable			16	ns

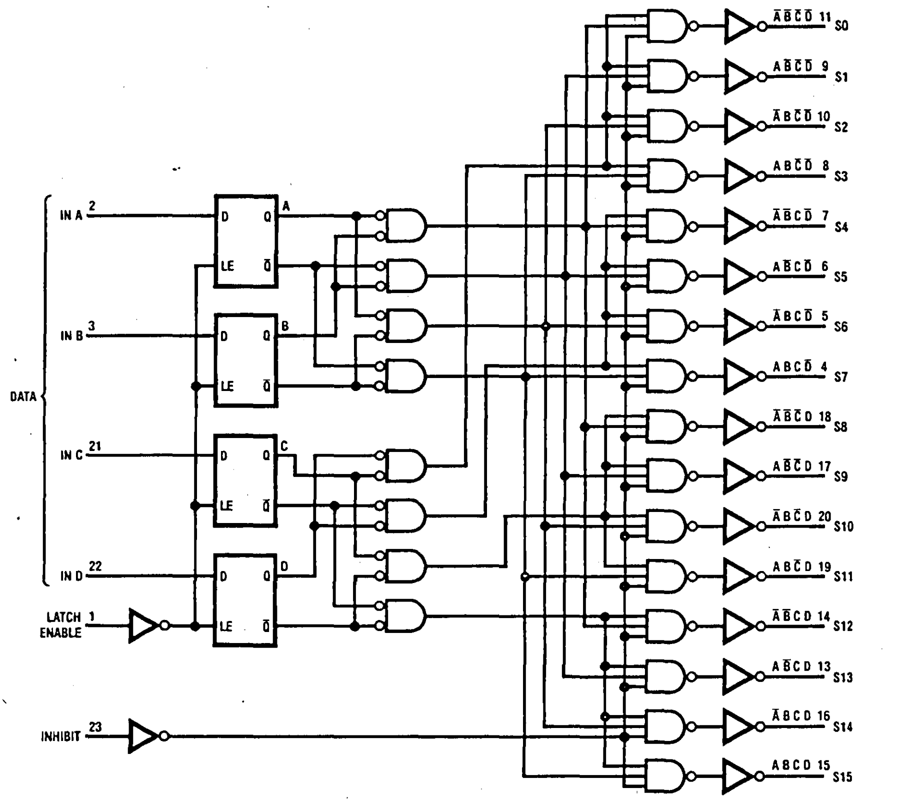
AC Electrical Characteristics $V_{CC}=2.0V-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	80	175	220	263	ns
			4.5V	18	35	44	53	ns
			6.0V	16	30	38	45	ns
t_{PHL}	Maximum Propagation Delay LE to Output		2.0V	80	175	220	263	ns
			4.5V	19	35	44	53	ns
			6.0V	17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay LE to Output		2.0V	120	230	290	343	ns
			4.5V	27	46	58	69	ns
			6.0V	22	39	49	58	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		2.0V	70	175	220	263	ns
			4.5V	18	35	44	53	ns
			6.0V	16	30	38	45	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		2.0V	120	230	290	343	ns
			4.5V	27	46	58	69	ns
			6.0V	22	39	49	58	ns
t_S	Minimum Set Up Time, Data to LE		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time, LE to Data		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width, Latch Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5215-2

National Semiconductor

microCMOS

MM54HC4538/MM74HC4538 Dual Retriggerable Monostable Multivibrator

General Description

The MM54HC4538/MM74HC4538 high speed monostable multivibrators (one shots) are implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

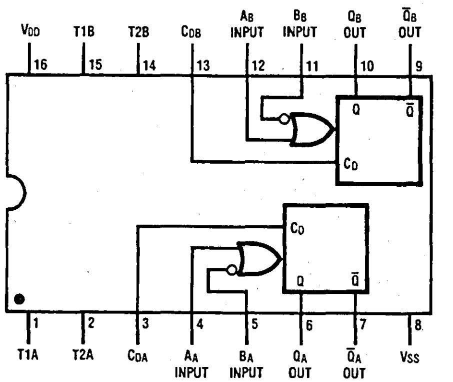
Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC4538 is retriggerable. That is, it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = 0.7(R) (C) where PW is in seconds, R is in Ohms, and C is in Farads. This device is pin compatible with the CD4528, and the CD4538 one shots. All inputs are protected from damage due to static discharge by diodes to Vcc and ground.

Features

- Schmitt trigger on A and B inputs
- Wide power supply range: 2–6V
- Typical Trigger Propagation Delay: 32 ns
- Fanout of 10 LS-TTL loads (74HC)
- Low Input current: 1 μA max

Connection Diagram Dual-In-Line Package

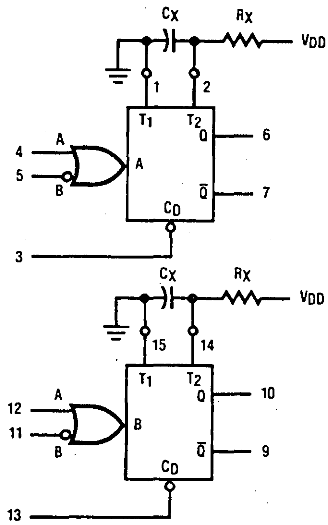


TL/F/5217-1

MM54HC4538/MM74HC4538

54HC4538 (J) 74HC4538 (J,N)

Block Diagram



RX AND CX ARE EXTERNAL COMPONENTS

TL/F/5217-2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⊔
H	↑	H	⎍	⊔

H = High Level
L = Low Level
↑ = Transistion from Low to High
↓ = Transistion from High to Low
⎍ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to Vcc+1.5V
DC Output Voltage(V_{OUT})	−0.5 to Vcc+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Reset only)			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 2, 14)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.5	±5.0	±10	μA
I_{IN}	Maximum Input Current (All other pins)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$ Pins 2 and 14=0.5V_{CC}	6.0V	100	150	250	400	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Propagation Delay A, or B to Q		23	45	ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$		26	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		23	45	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		26	45	ns
t_W	Minimum Pulse Width A, B or Clear		10	16	ns

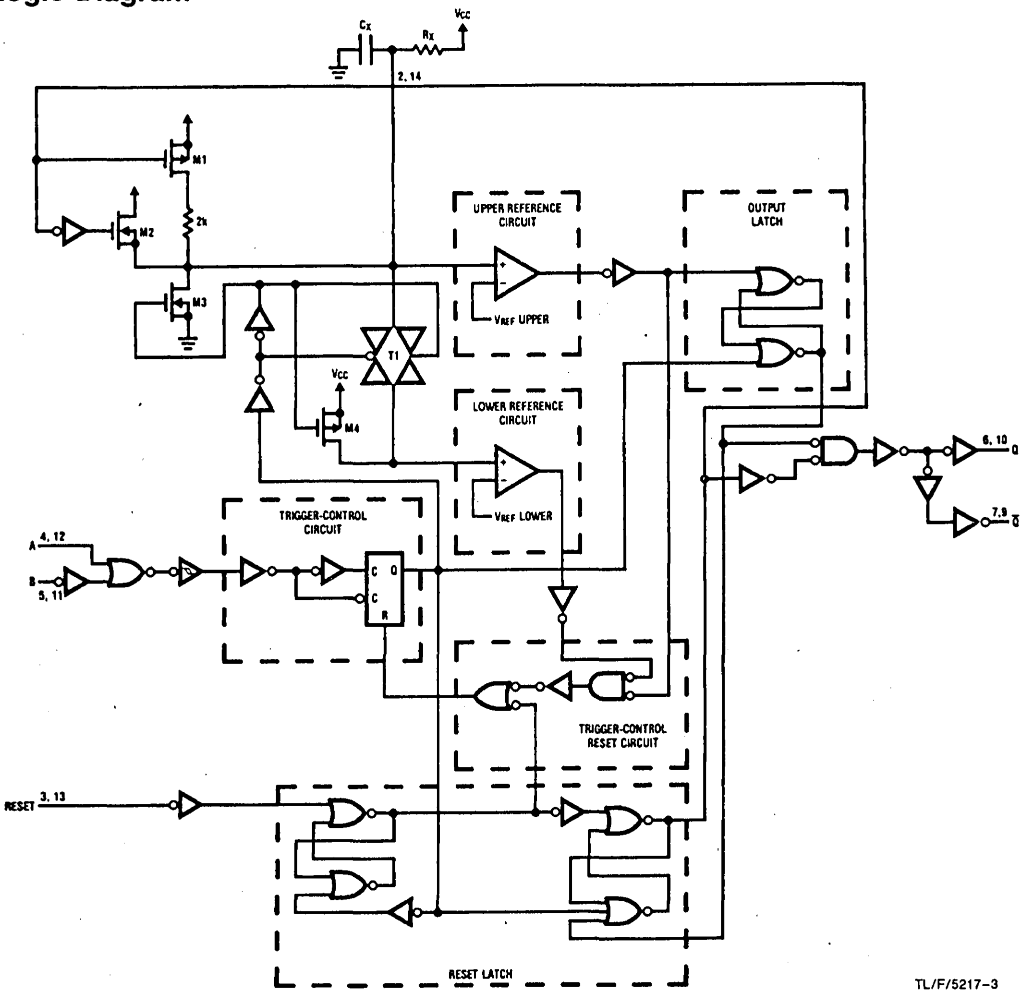
AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (Unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$ Typ	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
						Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay A, or B to Q			2.0V	100	250	315	373	ns
				4.5V	25	50	63	75	ns
				6.0V	21	43	54	63	ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$			2.0V	110	275	347	410	ns
				4.5V	28	55	69	82	ns
				6.0V	23	47	59	70	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	100	250	315	373	ns
				4.5V	25	50	63	75	ns
				6.0V	21	43	54	63	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	110	275	347	410	ns
				4.5V	28	55	69	82	ns
				6.0V	23	47	59	70	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	10	15	19	22	ns
				6.0V	8	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time (Reset only)			2.0V		1000	1000	1000	ns
				4.5V		500	500	500	ns
				6.0V		400	400	400	ns
t_W	Minimum Pluse Width A, B, Clear			2.0V		80	101	119	ns
				4.5V		16	20	24	ns
				6.0V		14	17	20	ns
t_{WQ}	Output Pulse Width	Cx=12 pF Rx=1 kΩ	Min	3.0V	283	190			ns
				5.0V	147	120			ns
			Max	3.0V	283	400			ns
				5.0V	147	185			ns
t_{WQ}	Output Pulse Width	Cx=100 pF Rx=10 kΩ	Min	3.0V	1.2				μs
				5.0V	1.0				μs
			Max	3.0V	1.2				μs
				5.0V	1.0				μs
t_{WQ}	Output Pulse Width	Cx=1000 pF Rx=10 kΩ	Min	3.0V	10.5	9.4			μs
				5.0V	10.0	9.3			μs
			Max	3.0V	10.5	11.6			μs
				5.0V	10.0	11.7			μs
C_{IN}	Maximum Input Capacitance (Pins 2 & 14)				25				pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per one shot)			150				pF
Δt_{WQ}	Pulse Width Match Between Circuits in Same Package				±1				%

Note 5: C_{PD} determines the no load dynamic consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5217-3

Circuit Operation

The 'HC4538 operates as follows (refer to logic diagram). In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{REF} Lower = $\frac{1}{3}V_{CC}$). C_X then charges, through R_X, back up to the upper reference voltage (V_{REF} Upper = $\frac{2}{3}V_{CC}$), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic diagram and the timing diagram.

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in logic diagram).

Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, timing diagram).

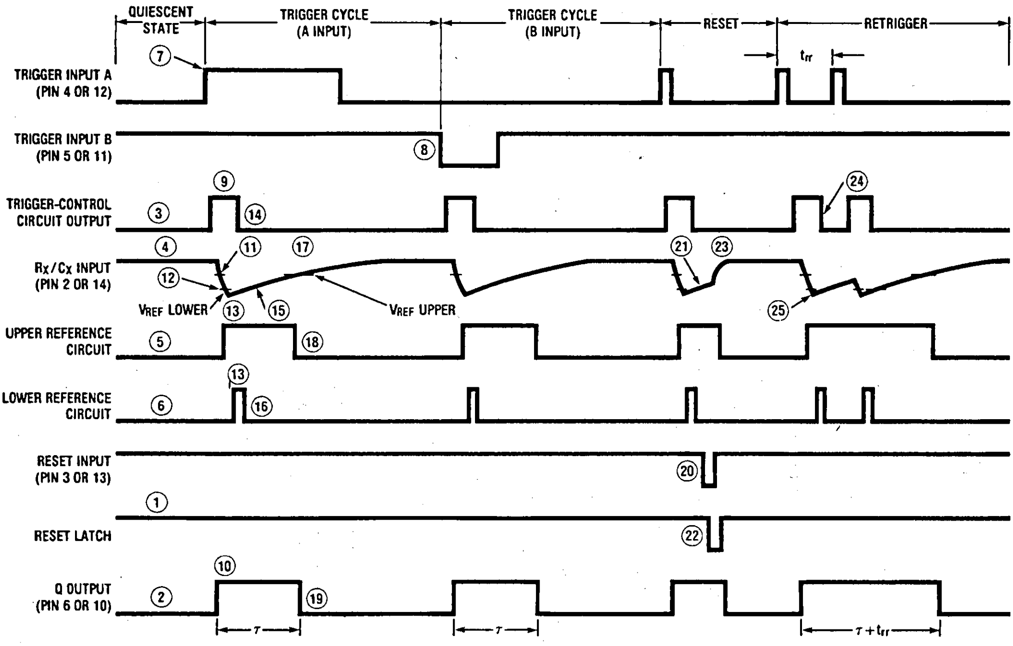
The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The 'HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

Timing Diagram



TL/F/5217–4

Circuit Operation (Continued)

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 'HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_XC_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 'HC4538 to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 'HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

RETRIGGER OPERATION

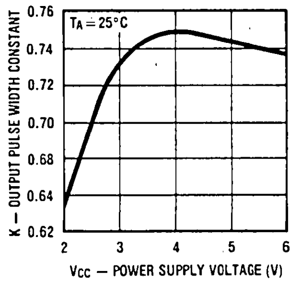
In the retriggerable mode, the 'HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr}(\text{ns}) \cong 72 + \frac{V_{CC}(\text{volts}) \bullet C_X(\text{pF})}{30.5}, \text{ at room temperature}$$

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_X/(30 \text{ mA})$. For example, if $V_{CC} = 5V$ and $C_X = 15 \mu F$, the V_{CC} supply must turn off no faster than $t = (15V) \bullet (15 \mu F)/30 \text{ mA} = 2.5 \text{ ms}$. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected from V_{CC} to the C_X pin.



TL/F/5217-5

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT00/MM74HCT00 Quad 2 Input NAND Gate

General Description

The MM54HCT00/MM74HCT00 are NAND gates fabricated using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pin-out compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

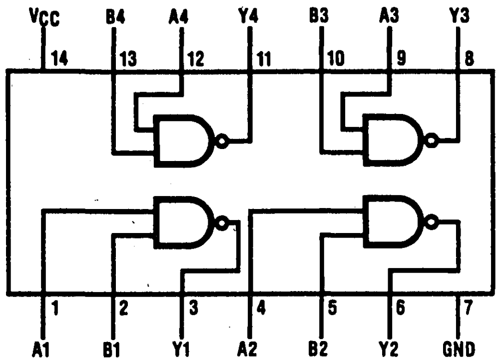
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 14 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at > 5 MHz
- High fan-out, 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



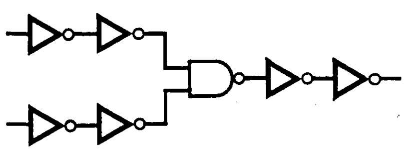
TOP VIEW

TL/F/5295-1

MM54HCT00/MM74HCT00

54HCT00 (J) 74HCT00 (J,N)

Logic Diagram



TL/F/5295-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note: 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$, (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		12	18	ns

AC Electrical Characteristics $V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF, (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT04/74HCT04 Hex Inverter

General Description

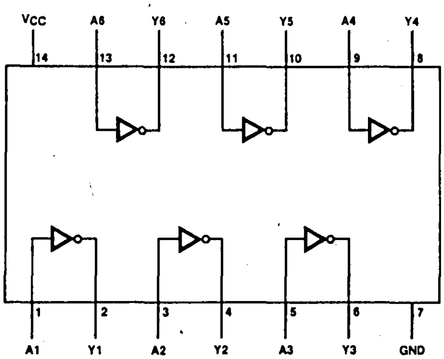
The MM54HCT04/74HCT04 are logic functions fabricated using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS - low quiescent power and wide power supply range, but are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS devices. The MM54HCT04/MM74HCT04, triple buffered, inverting hex inverters, feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at 5 MHz
- High fan-out: ≥ 10 LS loads
- Inverting, triple buffered

Connection Diagram



TOP VIEW

TL/F/5296-1

MM54HCT04/MM74HCT04

54HCT04 (J) 74HCT04 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note: 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$, (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF, (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power comsumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT05/MM74HCT05 Hex Inverter (Open Drain)

General Description

The MM54HCT05/MM74HCT05 are logic functions fabricated using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also input-output characteristically and pin-out compatible with standard DM54LS/DM74LS logic families. The MM54HCT05/MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

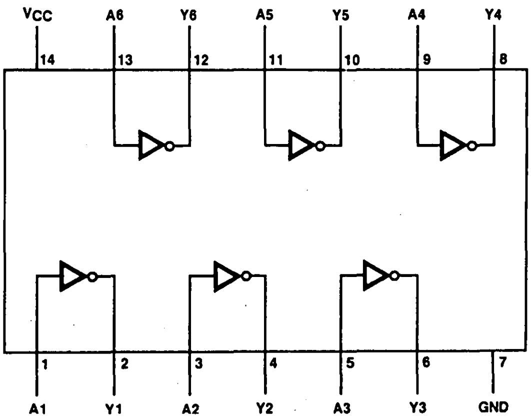
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fan-out of 10 LS-TTL loads
- Typical propagation delays:
  - t_{PLH} (with 1 kΩ resistor) 10 ns
  - t_{PHL} (with 1 kΩ resistor) 8 ns

Connection Diagram

Dual-In-Line Package



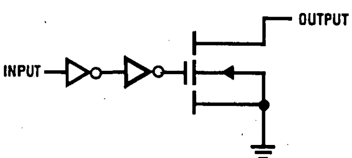
TOP VIEW

TL/F/5069-1

MM54HCT05/MM74HCT05

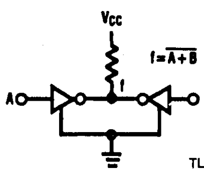
54HCT05 (J) 74HCT05 (J,N)

Logic Diagram



TL/F/5358-2

Typical Application



TL/F/5358-3

MM54HCT05/MM74HCT05

Note: Can be extended to more than 2 inputs.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC}=5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}, R_L=1 kμ $\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC} 0.1	V_{CC} 0.1	V_{CC} 0.1	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} $\lvert I_{OUT}\rvert$=20 μA $\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V $\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN}=V_{IH} or VIL, V_{OUT}=V_{CC}		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay	R_L=1 kΩ	8	15	ns
t_{PLH}	Maximum Propagation Delay	R_L=1 kΩ	9	16	ns

AC Electrical Characteristics V_{CC}=5V ±10%, C_L=50 pF, t_r=t_f=6 ns unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay	R_L=1 kΩ	10	22	28	33	ns
t_{PLH}	Maximum Propagation Delay	R_L=1 kΩ	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) R_L=∞		20			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}, and the no load dynamic current consumption, I_S=C_{PD} V_{CC} f+I_{CC}.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT34/74HCT34 Non-Inverter

General Description

The MM54HCT34/74HCT34 are logic functions fabricated using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS - low quiescent power and wide power supply range, but are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS devices. The MM54HCT34/MM74HCT34, triple buffered, inverting hex inverters, feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

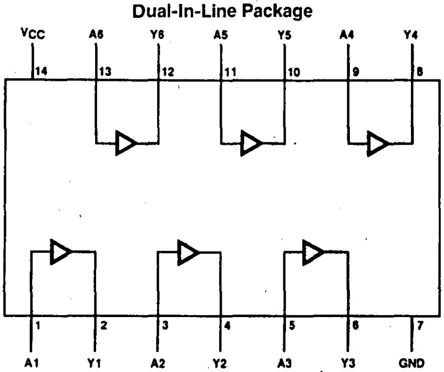
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: T_{PLH}, T_{PHL} = 8 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at 5 MHz
- High fan-out: ≥ 10 LS loads
- Inverting, triple buffered

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5296-1

MM54HCT34/MM74HCT34

54HCT34 (J) 74HCT34 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note: 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$, (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	15	ns

AC Electrical Characteristics

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF, (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	24	27	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power comsumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT74/MM74HCT74 Dual D Flip-Flop with Preset and Clear

General Description

The MM54HCT74/MM74HCT74 utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS, to achieve operation speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

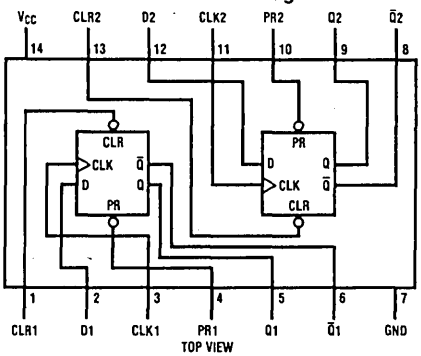
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5106-1

MM54HCT74/MM74HCT74
54HCT74 (J) 74HCT74 (J,N)

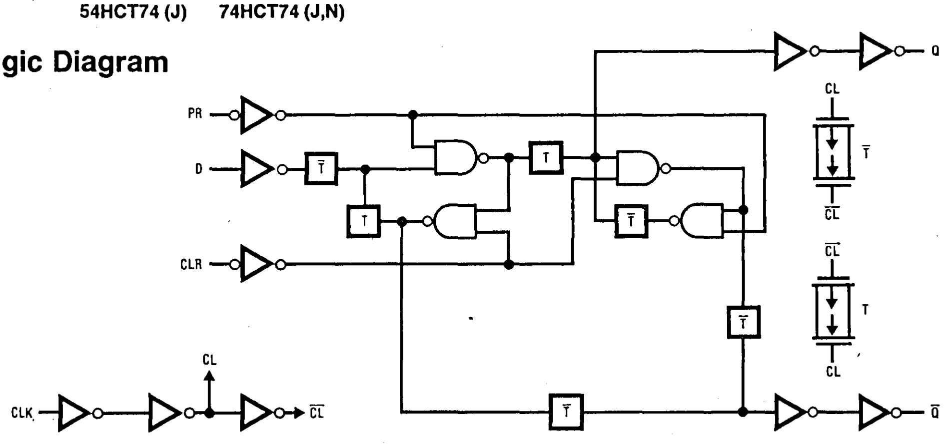
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Logic Diagram



TL/F/5106-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} Ground.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency from Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set Up Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics

$V_{CC}=5.0V\pm10\%$ $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

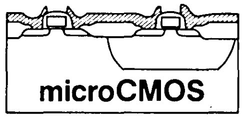
Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q or $\overline{Q}$		21	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		21	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Set Up Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		9	16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY



MM54HCT76/MM74HCT76
MM54HCT112/MM74HCT112
Dual J-K Flip-Flops with Preset and Clear

General Description

These flip-flops utilize silicon gate CMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These flip-flops have independent J, K, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The flip-flops are edge-triggered and change state on the negative-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

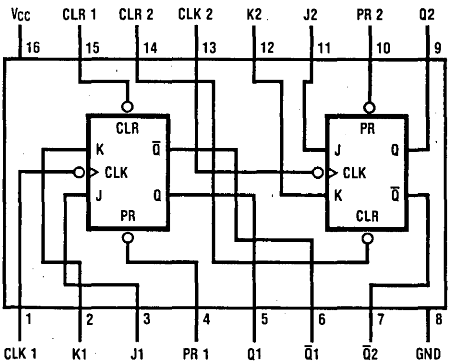
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5762-1

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q0	$\overline{Q}0$

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C	74HCT T_A=−40°C to 85°C	54HCT T_A=−55°C to 125°C	Units
				Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set-Up Time J or K Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

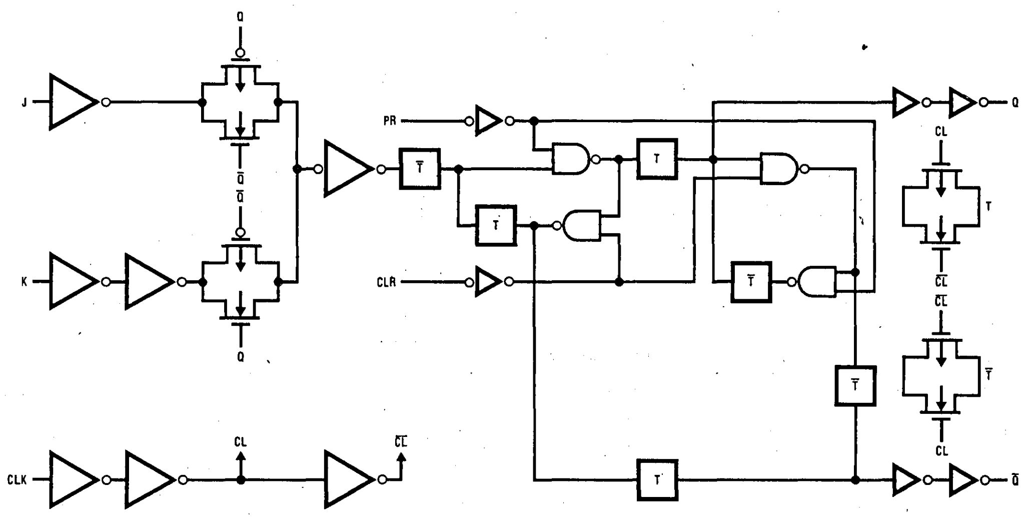
AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified (Note 6)

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to 85°C	54HCT $T_A = -55°C$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\bar{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\bar{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Set-Up Time J or K to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5762-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT107/MM74HCT107 Dual J-K Flip-Flops with Clear

General Description

The MM54HCT107/MM74HCT107 utilize silicon gate CMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These flip-flops have independent J, K, clear and clock inputs and Q and $\overline{Q}$ outputs. The flip-flops are edge-triggered and change state on the negative-going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level on the input.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

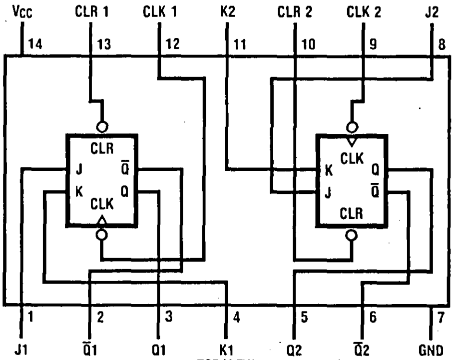
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current 8 μA maximum (74HCT Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



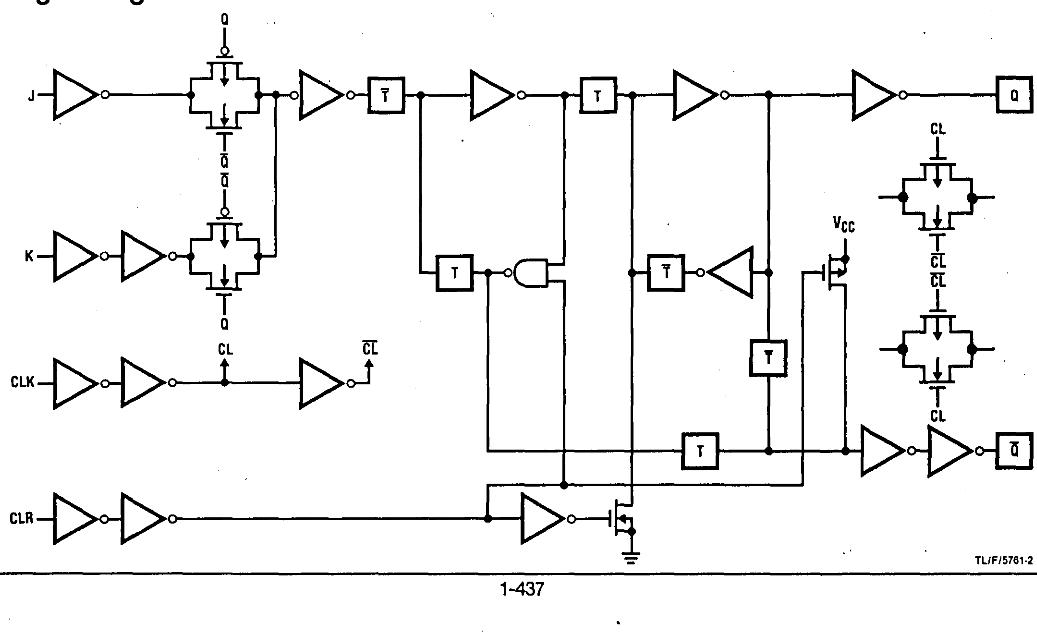
TOP VIEW

TL/F/5761-1

Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q0	$\overline{Q0}$

Logic Diagram



TL/F/5761-2

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Voltage (V_{IN})	$-1.5V$ to $V_{CC}+1.5V$
DC Output Voltage (V_{OUT})	$-0.5V$ to $V_{CC}+0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per Pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	$-65°C$ to $+150°C$
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	-40	$+85$	°C
MM54HCT	-55	$+125$	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC}=5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Conditions	$T_A=25°C$ Typ	$T_A=25°C$	74HCT $T_A=-40°C$ to 85°C	54HCT $T_A=-55°C$ to 125°C	Units
				Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert=20\ \mu A$	V_{CC}	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
		$\lvert I_{OUT}\rvert=4.0$ mA, $V_{CC}=4.5V$	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert=4.8$ mA, $V_{CC}=5.5V$	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert=20\ \mu A$	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert=4.0$ mA, $V_{CC}=4.5V$	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert=4.8$ mA, $V_{CC}=5.5V$	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND, V_{IH} or V_{IL}		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$		4.0	40	80	μA
		$V_{IN}=2.4V$ or $0.5V$ (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set-Up Time J or K Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or K		-3	0	ns
t_W	Minimum Pulse Width Clock, Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to 85°C	54HCT $T_A = -55°C$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Set-Up Time J or K to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT109/MM74HCT109 Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These high speed J-$\overline{K}$ FLIP-FLOPS utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

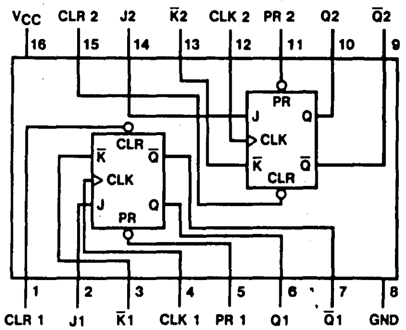
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HCT series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



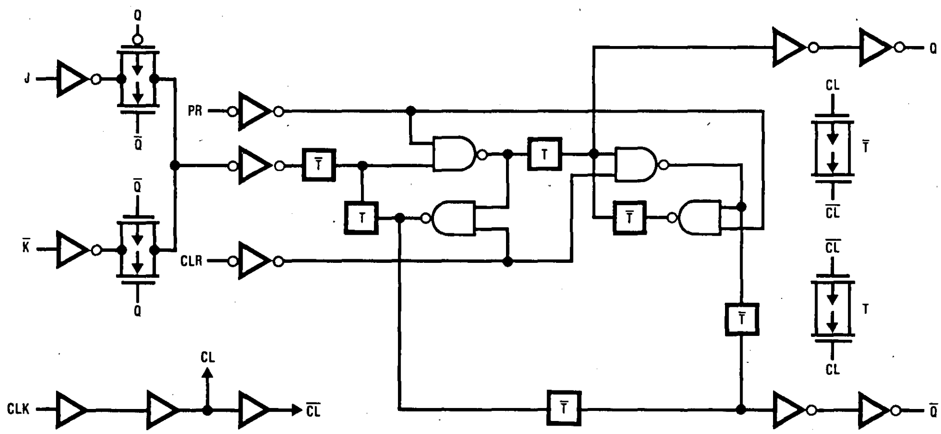
TL/F/5306-1

MM54HCT109/MM74HCT109
54HCT109 (J) 74HCT109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5306-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set Up Time J or $\overline{K}$ Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics

$V_{CC}=5.0V$ ±10% $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Set Up Time J or $\overline{K}$ to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT138/MM74HCT138 3-to-8 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM54HCT138/MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

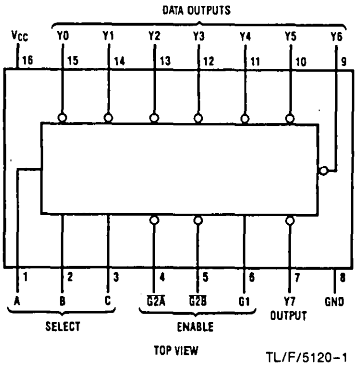
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

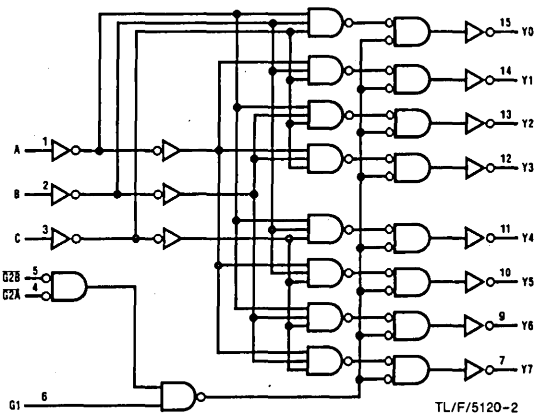


TL/F/5120-1

MM54HCT138/MM74HCT138

54HCT138 (J) 74HCT138 (J,N)

Logic Diagram



TL/F/5120-2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

H = high level L = low level X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input pin. All other inputs are held at V_{CC} or ground.

AC Electrical Characteristics $T_A=25°C$, $V_{CC}=5.0V$, $t_r=t_f=6$ ns $C_L=15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, A, B, or C to Output		20	35	ns
t_{PLH}	Maximum Propagation Delay, A, B, or C to Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, G1 to Y Output		14	25	ns
t_{PLH}	Maximum Propagation Delay, G1 to Y Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		17	30	ns
t_{PLH}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		13	25	ns

AC Electrical Characteristics

$V_{CC}=5V \pm 10\%$ $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay A, B, or C to Output		24	40	50	60	ns
t_{PLH}	Maximum Propagation Delay A, B, or C to Output		18	30	38	45	ns
t_{PHL}	Maximum Propagation Delay G1 to Y Output		17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay G1 to Y Output		20	30	38	45	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		23	35	43	52	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{IN}	Input Capacitance			5	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)					pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT139/MM74HCT139 Dual 2-To-4 Line Decoder

General Description

The MM54HCT139/MM74HCT139 is a high speed silicon-gate CMOS decoder that is well suited to memory address decoding or data routing applications. It possesses an input threshold and output drive similar to LS-TTL and the low standby of CMOS logic.

The device is comprised of two independent one-of-four decoders each with a single active low enable input (G1 or G2). Data on the select inputs (A1, B1 or A2, B2) cause one of the four normally high outputs to go low.

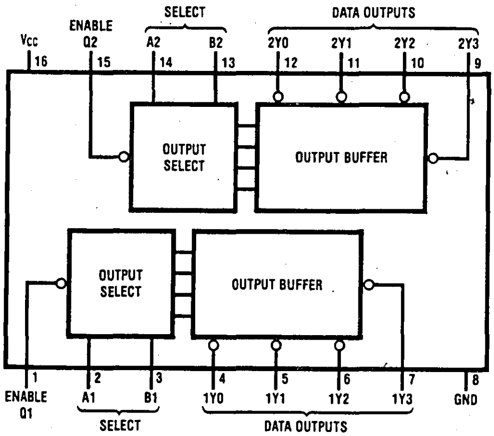
All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground. The device is capable of driving 10 low power Schottky TTL equivalent loads.

The MM54HCT139/MM74HCT139 is functionally and pin equivalent to the 54LS139/74LS139 and can be used as a plug in replacement to reduce system power consumption in existing systems.

Features

- Typical propagation delays: 20 ns
- Low quiescent current: 40 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram Dual-In-Line Package



TL/F/5311-1

TOP VIEW
MM54HCT139/MM74HCT139
54HCT139 (J) 74HCT139 (J,N)

Truth Table

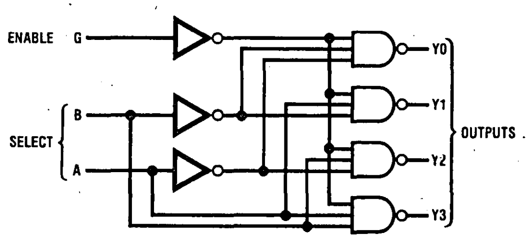
'HCT139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HCT139/MM74HCT139



TL/F/5311-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	20 mA
DC Output Current, per Pin (I_{OUT})	25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	C
MM54HCT	−55	+125	C
Input Rise/Fall Time (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	Typ	Guaranteed Limits			Units
				T=25°C	T=25°C	74HCT T=−40 to 85°C	54HCT T=−55 to 125°C	
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|=20\ \mu A$ $\|I_{OUT}\|=4.0$ mA, $V_{CC}=4.5V$ $\|I_{OUT}\|=4.8$ mA, $V_{CC}=5.5V$		V_{CC}	$V_{CC}-.1$ 3.98 4.98	$V_{CC}-.1$ 3.84 4.84	$V_{CC}-.1$ 3.7 4.7	V V V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|=20\ \mu A$ $\|I_{OUT}\|=4.0$ mA, $V_{CC}=4.5V$ $\|I_{OUT}\|=4.8$ mA, $V_{CC}=5.5V$			0.10 0.26 0.26	0.10 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND $V_{IN}=V_{IH}$ or V_{IL}			±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$ (Note 4)			4	40	80	μA
		V_{IN}=2.4V or 0.5V $I_{OUT}=0\ \mu A$ (Note 4)			300	400	440	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs at V_{CC} or GND.

AC Electrical Characteristics

(V_{CC}, Temperature and loading of LS-TTL)

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
$t_{PLH, PHL}$	Maximum Propagation delay, Binary Select to any output		18	30	ns
$t_{PLH, PHL}$	Maximum Propagation delay, Enable to any output		18	30	ns

AC Electrical Characteristics

(Full Range of V_{CC} and Temperature) $V_{CC}=5V$ ±10%, $C_L=50$ pF (Unless Otherwise Specified)

Symbol	Parameter	Condition	Typ	Guaranteed Limits			Units
			$T_A=25C$	$T_A=25C$	74HCT $T_A=-40$ to 85C	54HCT $T_A=-55$ to 125	
$t_{PLH, PHL}$	Maximum Propagation Delay, Binary Select to any Output		20	35	44	51	ns
$t_{PLH, PHL}$	Maximum Propagation Delay, Enable to any Output		21	35	44	51	ns
$t_{TLH, THL}$	Maximum Output Rise and Fall Time		9	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	Note 5					pF
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=(C_{PD}\ V_{CC}\ ^2)\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT149/MM74HCT149 8 Line to 8 Line Priority Encoder

General Description

This priority encoder is implemented in microCMOS Technology, 3.0 micron silicon gate N-well CMOS. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority, encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. It is the logical combination of a '148 8–3 line priority encoder driving a '138 3–8 line decoder. Only one request output can be low at a time. The output that is low is dependent on the highest priority request input that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RI}$ is active.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

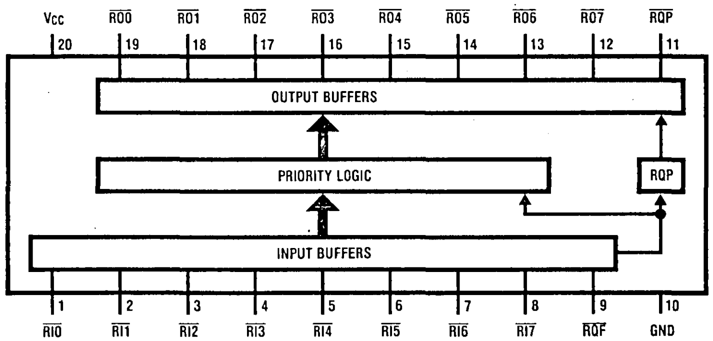
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Internal switched pull up resistors provided to reduce power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5312-1

MM54HCT149/MM74HCT149

54HCT149 (J) 74HCT149 (J,N)

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RQE}$ to any Output		16	28	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay $\overline{RI}n$ to $\overline{RO}n$ (same Output)		23	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RI}n$ to a different Output		22	30	ns

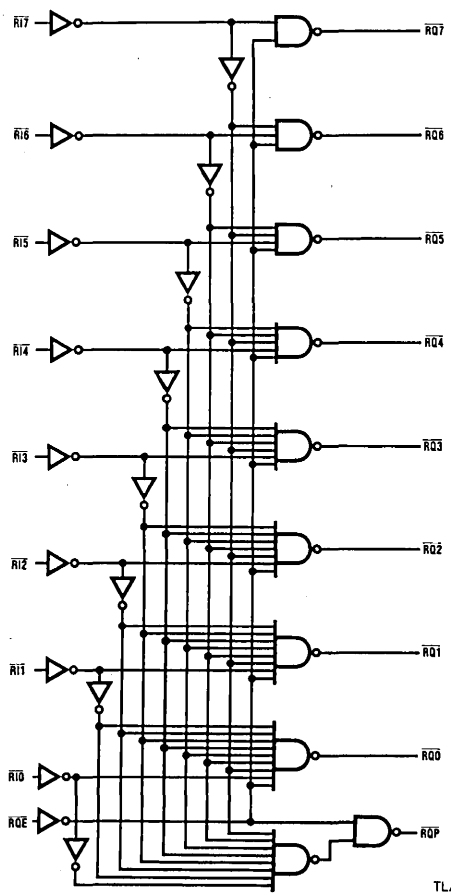
AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pf $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RQE}$ to any Output		17	31	39	46	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay $\overline{RI}n$ to $\overline{RO}n$ (same Output)		18	32	40	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RI}n$ to a different Output		20	35	44	53	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)		50			pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Simplified Logic Diagram



TL/F/5312-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT155/MM74HCT155 Dual 2-to-4 Line Decoder/Demultiplexers

General Description

The MM54HCT155/MM74HCT155 is a high speed silicon gate CMOS decoder/demultiplexer. It features dual 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground. The device is capable of driving 10 low power Schottky TTL equivalent loads.

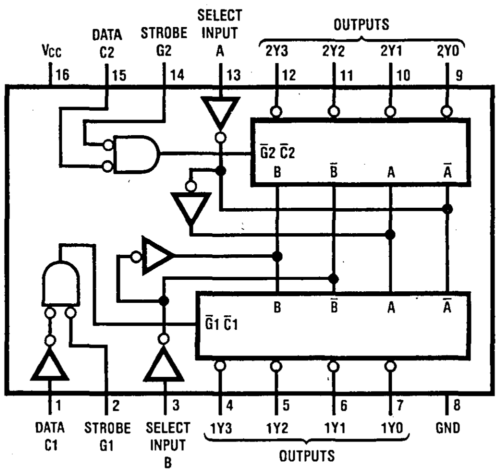
The MM54HCT155/MM74HCT155 is functionally and pin equivalent to the 54LS155/74LS155 and can be used as a plug-in replacement to reduce system power consumption in existing systems.

Features

- Applications:
  - Dual 2-to-4 line decoder
  - Dual 1-to-4 line demultiplexer
  - 3-to-8 line decoder
  - 1-to-8 line demultiplexer
- Typical propagation delay: 22 ns
- Low Quiescent current: 8 μA maximum (74HC Series)

Connection Diagram

Dual-In-Line Package



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Truth Tables

2-TO-4 LINE DECODER OR 1-TO-4 LINE DEMULTIPLEXER

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-TO-8 LINE DECODER OR 1-TO-8 LINE DEMULTIPLEXER

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
IC	B	A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

IC = inputs C1 and C2 connected together
GI = inputs G1 and G2 connected together
H = high level
L = low level
X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Voltage (V_{IN})	$-1.5V$ to $V_{CC}+1.5V$
DC Output Voltage (V_{OUT})	$-0.5V$ to $V_{CC}+0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per Pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	$-65°C$ to $+150°C$
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	-40	$+85$	°C
MM54HCT	-55	$+125$	°C
Input Rise/Fall Time (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC}=5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Guaranteed Limits			Units
				T=25°C	T=25°C	74HCT T=−40°C to 85°C	54HCT T=−55°C to 125°C	
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum High Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert=20\ \mu A$ $\lvert I_{OUT}\rvert=4.0$ mA, $V_{CC}=4.5V$ $\lvert I_{OUT}\rvert=4.8$ mA, $V_{CC}=5.5V$		V_{CC}	$V_{CC}-0.1$ 3.98 4.98	$V_{CC}-0.1$ 3.84 4.84	$V_{CC}-0.1$ 3.7 4.7	V V V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert=20\ \mu A$ $\lvert I_{OUT}\rvert=4.0$ mA, $V_{CC}=4.5V$ $\lvert I_{OUT}\rvert=4.8$ mA, $V_{CC}=5.5V$			0.10 0.26 0.26	0.10 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND $V_{IN}=V_{IH}$ or V_{IL}			± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0.0\ \mu A$ (Note 4)			8	80	160	μA
		$V_{IN}=2.4V$ or $0.5V$ $I_{OUT}=0.0\ \mu A$ (Note 4)						mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Power dissipation temperature deratings: plastic N package: -12 mW/°C from 65°C to 85°C; ceramic J package: -12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs at V_{CC} or GND.

AC Electrical Characteristics V_{CC}, temperature and loading of LS-TTL; $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output		19	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output		24	35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C_1 to any Output		25	35	ns

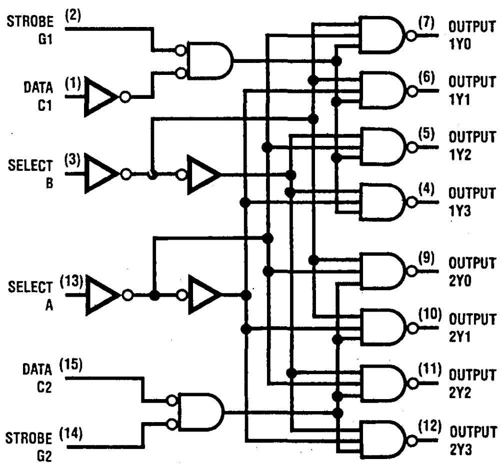
AC Electrical Characteristics

Full range of V_{CC} and temperature; $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF unless otherwise specified

Symbol	Parameter	Conditions	Typ	Guaranteed Limits			Units
			T=25°C	T=25°C	74HCT T=−40°C to 85°C	54HCT T=−55°C to 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output		21	35	44	51	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output		26	40	50	60	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C_1 to any Output		27	40	50	60	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance	Note 5					pF
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5759-2

MM54HCT157/MM74HCT157 Quad 2-Input Multiplexer MM54HCT158/MM74HCT158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed QUAD 2-to-1 LINE DATA SELECTOR/MULTIPLEXERS utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HCT157/MM74HCT157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HCT158/MM74HCT158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

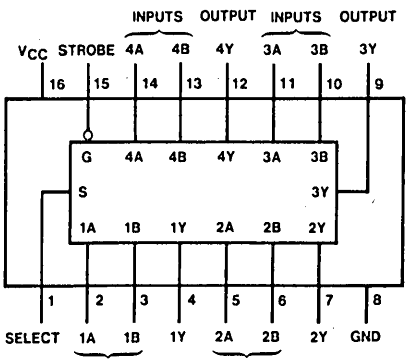
The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Power supply range: 5V ± 10%
- Low power supply quiescent current: 80 μA maximum (74HCT series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μA maximum
- Completely TTL compatible

Connection Diagrams

Dual-In-Line Package

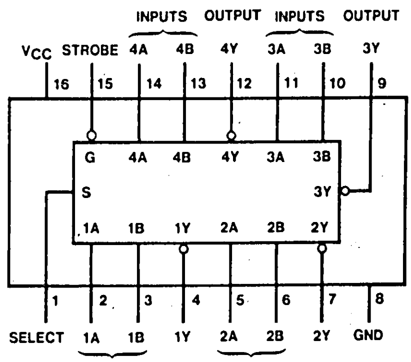


TOP VIEW
MM54HCT157/MM74HCT157

TL/F/5314-1

54HCT157 (J) 74HCT157 (J,N)

Dual-In-Line Package



TOP VIEW
MM54HCT158/MM74HCT158

TL/F/5314-2

54HCT158 (J) 74HCT158 (J,N)

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HCT157	HCT158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	4.5V		4.4	4.4	4.4	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 4.8$ mA	5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$		0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 4.8$ mA	5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HCT at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

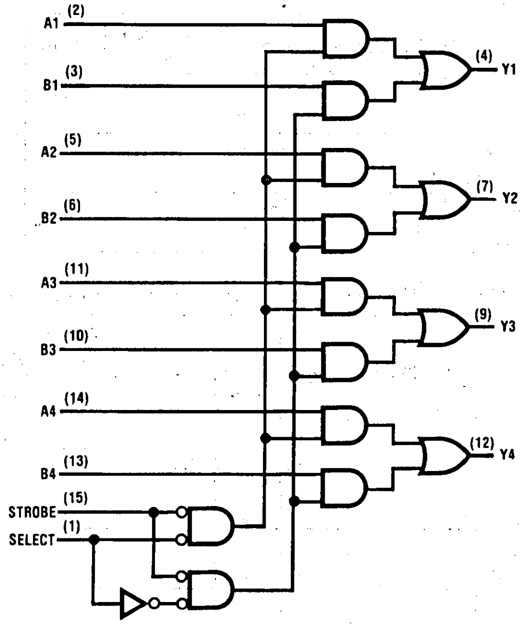
AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output			13	25	32	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output			13	25	32	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output			12	23	29	34	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			8	15	19	22	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)							pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

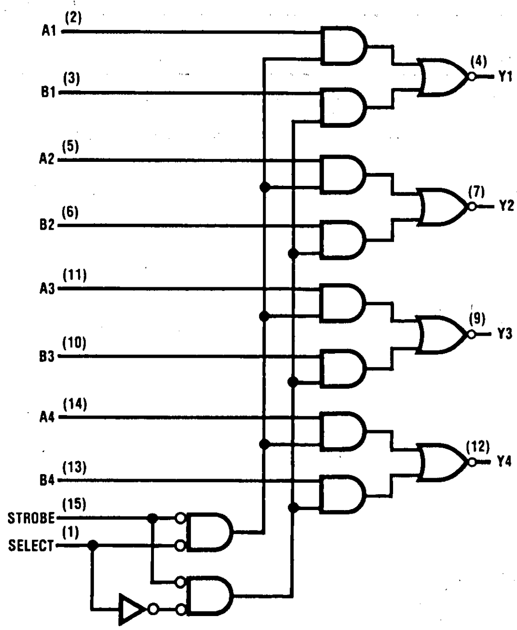
Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams



TL/F/5314-3

'HCT157



TL/F/5314-4

'HCT158

National Semiconductor

microCMOS

MM54HCT160/MM74HCT160 Synchronous Decade Counter with Asynchronous Clear MM54HCT161/MM74HCT161 Synchronous Binary Counter with Asynchronous Clear MM54HCT162/MM74HCT162 Synchronous Decade Counter with Synchronous Clear MM54HCT163/MM74HCT163 Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HCT160/74HCT160, MM54HCT161/74HCT161, MM54HCT162/74HCT162, MM54HCT163/74HCT163 synchronous presettable counters utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HCT160 and the 'HCT162 are 4-bit decade counters, and the 'HCT161 and the 'HCT163 are 4-bit binary counters. All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HCT162/MM74HCT162 and MM54HCT163/MM74HCT163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HCT160/MM74HCT160 and MM54HCT161/MM74HCT161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

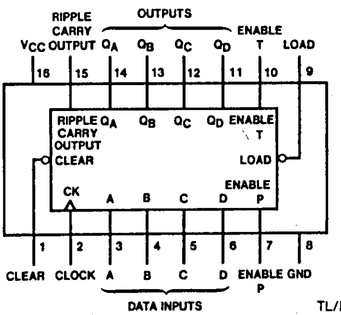
These circuits are TTL input and output compatible and are plug in replaceable for 'LS16X Series counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay: clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V
- TTL Input Compatible Inputs

Connection Diagram



TL/F/5008-1

54HCT160 (J) 74HCT160 (J,N)
54HCT161 (J) 74HCT161 (J,N)
54HCT162 (J) 74HCT162 (J,N)
54HCT163 (J) 74HCT163 (J,N)

Truth Tables

'HCT160/HCT161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HCT162/HCT163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 µA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$					
		$\lvert I_{OUT}\rvert$=20 µA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, I_{OUT}=0 µA		2.0	20	40	µA
		V_{IN}=2.4V or 0.5V (Note 4)	300	500			µA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note: 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		24	36	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		20	30	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		21	28	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		15	26	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		29	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		40	27	21	18	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		22	43	54	64	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		18	35	44	52	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		21	41	52	61	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		20	39	49	58	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		16	32	40	48	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		32	44	55	66	ns
t_{REM}	Minimum Removal Time Clear to Clock			25	32	37	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	38	45	ns
t_H	Minimum Hold Time Data from Clock			10	13	15	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		8	15	19	22	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	90				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HCT164/MM74HCT164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HCT164/MM74HCT164 utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-BIT SHIFT REGISTER has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-BIT REGISTER during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

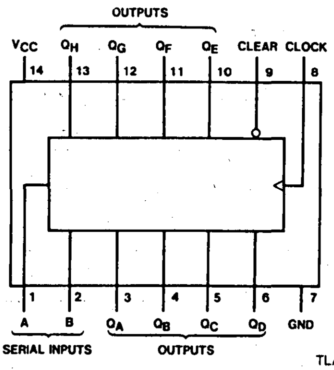
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL Input compatible

Connection Diagram

Dual-In-Line Package



TL/F/5315–1

TOP VIEW MM54HCT164/MM74HCT164

54HCT164 (J) 74HCT164 (J,N)

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

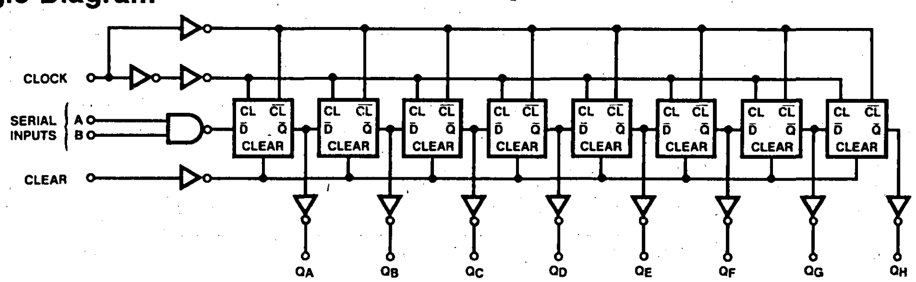
X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



TL/F/5315–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.4V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} Ground.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency From Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		20	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clear to Q		24	36	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set Up Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data		0	5	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		10	18	ns

AC Electrical Characteristics

$V_{CC}=5.0V\pm10\%$ $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q		23	37	46	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clear to Q		27	41	51	61	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Set Up Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data		0	5	0	0	ns
t_W	Minimum Pulse Width Clock, or Clear		10	18	22	27	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT166/MM74HCT166 8-Bit Serial or Parallel Input/Serial Output Shift Register with Reset

General Description

These shift registers utilize microCMOS technology, 3.0 micron silicon gate N-well CMOS. The MM54HCT166/MM74HCT166 are 8-bit shift registers with an output from the last stage. Data may be loaded into the register in either parallel or serial form.

When the shift/load input is low, the data is loaded asynchronously in parallel. When the shift/load input is high, the data is loaded serially on the rising edge of either Clock 1 or Clock 2 (see the Function Table). Reset is asynchronous and active low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

These devices are input and output characteristic and pinout compatible with standard 54LS/74LS logic families. 54HCT/74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Wide power supply range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA max (74HCT series)
- Fanout of 10 LS-TTL loads
- TTL-compatible inputs

Function Table and Connection Diagram

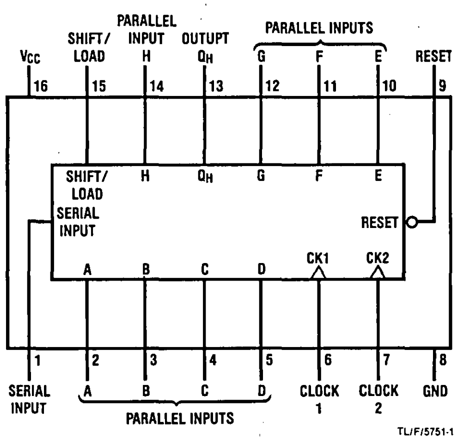
Inputs						Internal Stages		Output	Operation
Reset	Shift/ Load	Clock 1	Clock 2	Serial Input	A-H	Q_A	Q_B	Q_H	
H	L	X	X	X	a...h	a	b	h	Asynchronous Parallel Load
H	H	↑	L	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 1
H	H	↑	L	H	X	H	Q_{An}	Q_{Gn}	
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 2
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}	
H	H	X	H	X	X	no change			Inhibited Clock
H	H	H	X	X	X				
H	H	L	L	X	X	no change			No Clock
L	X	X	X	X	X	L	L	L	Asynchronous Reset

X = don't care

↑ = transition from low to high

Q_{An}-Q_{Gn} = data shifted from the preceding stage

Dual-In-Line Package



TL/F/5751-1

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V±10% unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40°C to 85°C	54HCT T_A=−55°C to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND I_{OUT}=0 μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		15	25	ns
t_{PHL}, t_{PLH}	Maximm Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Reset to Q_H		21	30	ns
t_S	Minimum Set-Up Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Set-Up Time Shift/Load to Clock		11	20	ns
t_S	Minimum Set-Up Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to $85°C$	54HCT $T_A = -55°C$ to $125°C$	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		45	27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or Q_H		21	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		21	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		21	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q_H		24	35	44	52	ns
t_S	Minimum Set-Up Time Serial Input to Clock or Parallel Data to Shift/Load		11	20	25	30	ns
t_S	Minimum Set-Up Time Shift/Load to Clock		12	20	25	30	ns

AC Electrical Characteristics (Continued)

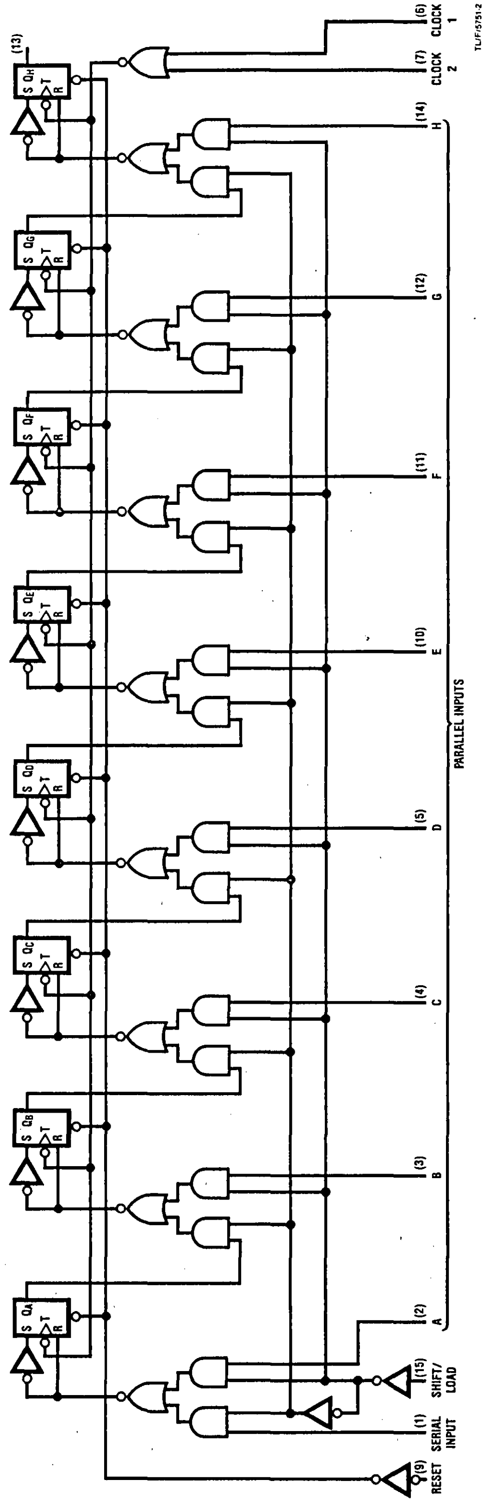
$V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to $85°C$	54HCT $T_A = -55°C$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_S	Minimum Set-Up Time Clock Inhibit to Clock		11	20	25	30	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	0	0	ns
t_W	Minimum Pulse Width, Clock		9	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		9	15	19	22	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Package)	100				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



National Semiconductor

PRELIMINARY

microCMOS

MM54HCT169/MM74HCT169 4-Bit Up/Down Synchronous Binary Counter

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power of CMOS logic while offering the high speed operation and large output drive typically associated with bipolar circuits. This device is input compatible with the 54LS/74LS and other TTL output compatible circuits, and may be used as a lower power direct replacement for the LS equivalent device.

These counters are incremented or decremented on the rising edge of the CLK, clock, input if $\overline{ENT}$ and $\overline{ENP}$ are held low. The counters increment when the U/$\overline{D}$ input is at a logic "1", and will decrement when U/$\overline{D}$ is low. The $\overline{ENT}$ input is fed forward to enable the carry output. $\overline{RCO}$, ripple carry output, once enabled, will produce a low level pulse while the count is 0 (down count mode) or when the count is all 1s (up mode).

These counters are presettable, that is, they may be loaded when $\overline{LOAD}$ is taken low and a rising edge appears on the CLK input.

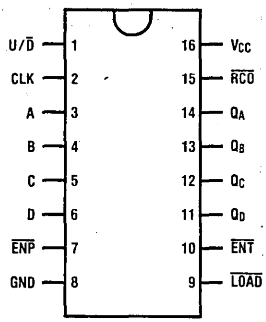
The MM54HCT169/MM74HCT169 are functional, speed and pin equivalent to the equivalent LS-TTL circuit, and may be used as a direct replacement for the equivalent LS-TTL IC. Its inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 4.5V to 5.5V
- Guaranteed TTL compatible input logic levels: 2.0V and 0.8V
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HCT)

Connection Diagram

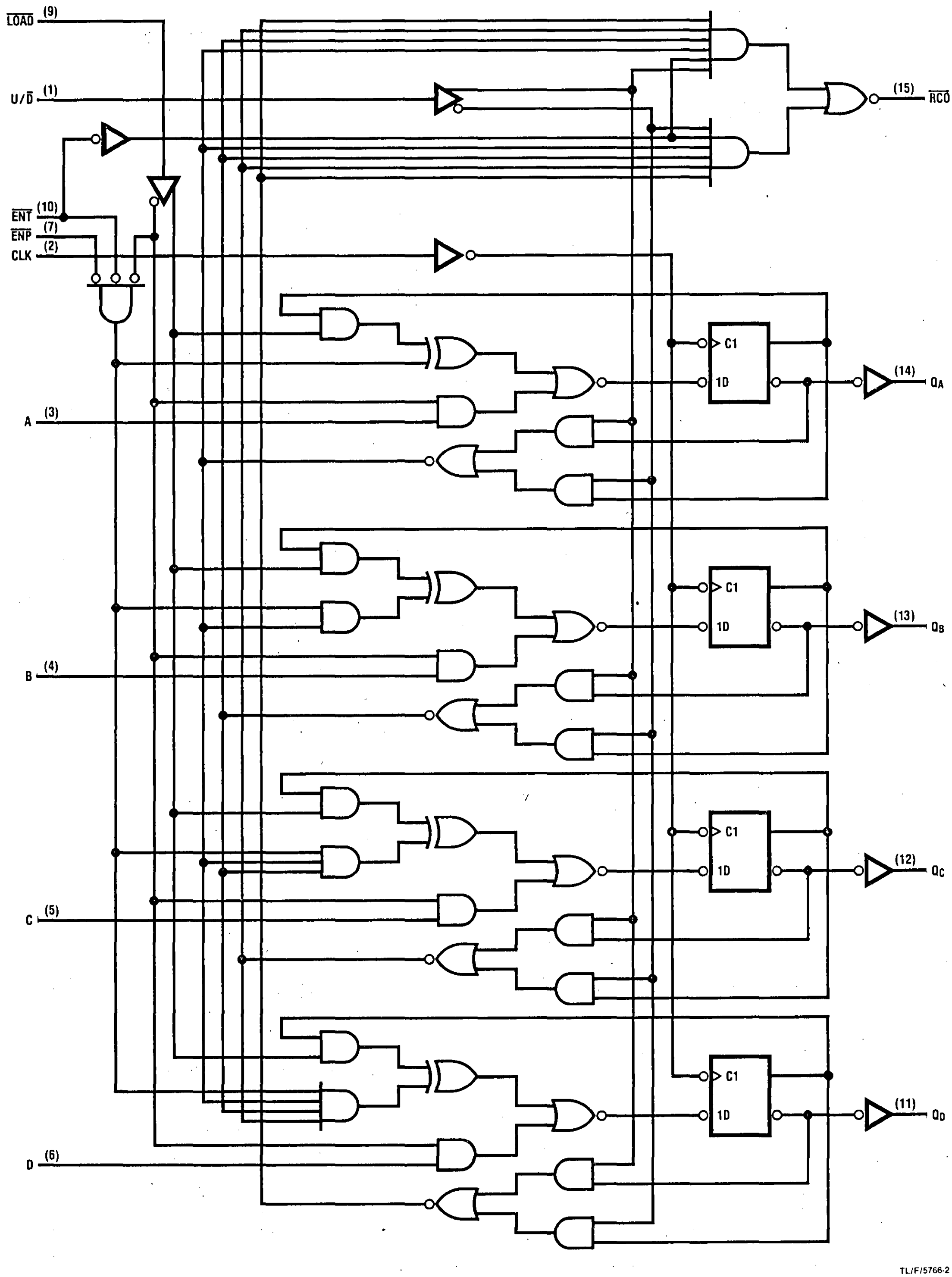
Dual-In-Line Package



TOP VIEW

TL/F/5766-1

Logic Diagram



MM54/74HCT169

1

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT174/MM74HCT174 Hex D Flip-Flops with Clear

General Description

The MM54HCT174/MM74HCT174 utilize 3.0 micron N-well microCMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear and independent Q outputs. Data on a D input, having the specified set-up and hold time, is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

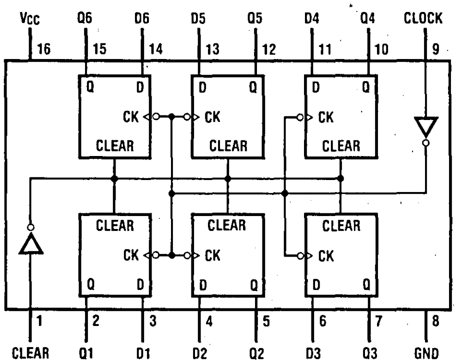
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

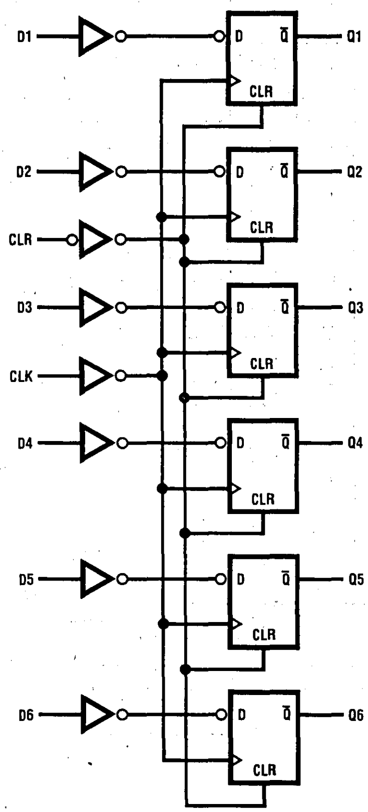
Dual-In-Line Package



TOP VIEW

TL/F/5763-1

Logic Diagram



TL/F/5763-2

Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↑ = transition from low to high level
Q0 = the level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40°C to 85°C Guaranteed Limits	54HCT T_A=−55°C to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		18	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set-Up Time D to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Q		−3	0	ns
t_W	Minimum Pulse Width Clock or Clear		8	16	ns

AC Electrical Characteristics $V_{CC}=5.0V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40°C$ to 85°C	54HCT $T_A=-55°C$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		22	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Set-Up Time D to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to D		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD} V_{CC} f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HCT191/MM74HCT191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize microCMOS technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL.

These circuits are synchronous, reversible, up/down counters. The MM54HCT191/MM74HCT191 are 4-bit binary counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as divide by N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

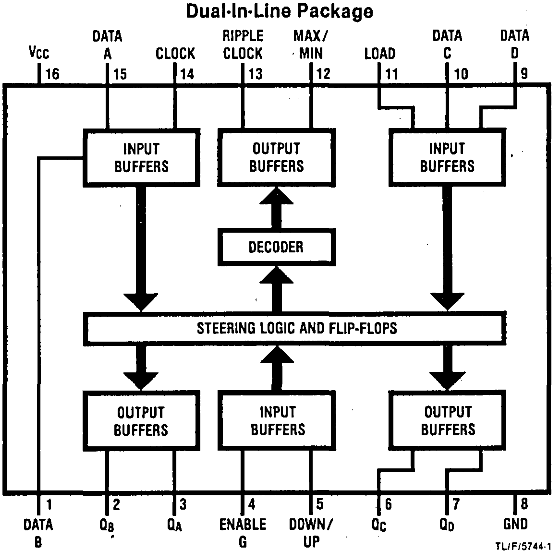
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay, clock to output: 24 ns
- Typical operating frequency: 50 MHz
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5744-1

Truth Table

Load	Enable G	Down/Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C Typ	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
				Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\lvert I_{OUT}\rvert$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$ = 20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF unless otherwise specified (Note 6)

Symbol	Parameter	From Input	To Output	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Clock Frequency				40	25	MHz
t_{PLH}, t_{PHL}	Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30	50	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27	40	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Ripple Clock		16	24	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24	36	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Max/Min		30	50	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Ripple Clock		29	45	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Max/Min		22	33	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		22	33	ns
$t_{W(CLOCK)}$	Width of Clock Load Input Pulse				10	20	ns
t_{SET-UP}	Data Set-Up Time					20	ns
t_{HOLD}	Data Hold Time					0	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified (Note 6)

Symbol	Parameter	From Input	To Output	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to $85°C$	54HCT $T_A = -55°C$ to $125°C$	Units
					Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency				38	20	15	13	MHz
t_{PLH}, t_{PHL}	Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		32	58	72	87	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		28	46	57	69	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Ripple Clock		18	30	37	45	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		27	44	55	66	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Max/Min		33	58	72	87	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Ripple Clock		30	53	66	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Max/Min		25	40	50	60	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		25	40	50	60	ns
t_W	Width of Clock, Load Input Pulse					20	25	30	ns
t_{SET-UP}	Data Set-Up Time				10	20	25	30	ns
t_H	Data Hold Time					0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time					15	19	22	ns

AC Electrical Characteristics

(Continued) $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified (Note 6)

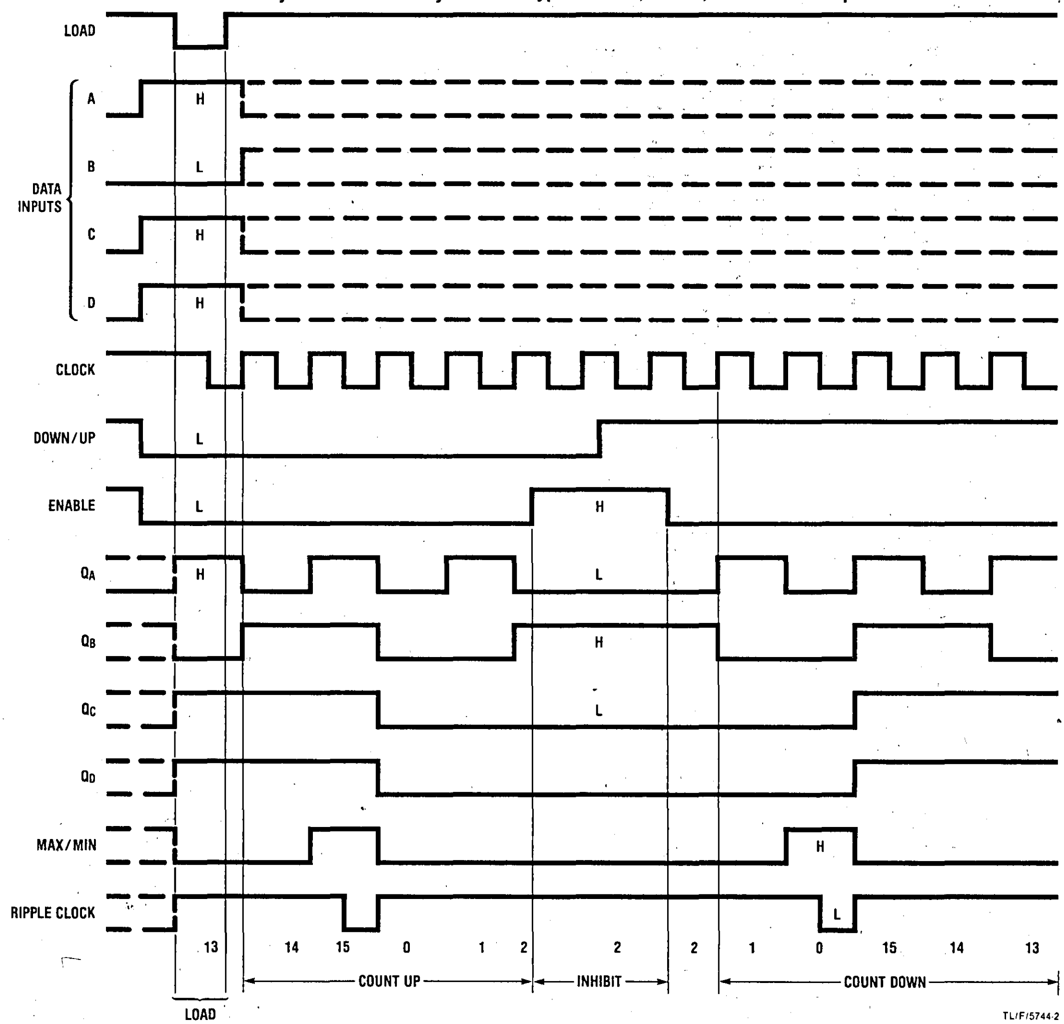
Symbol	Parameter	From Input	To Output	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to 85°C	54HCT $T_A = -55°C$ to 125°C	Units
					Typ		Guaranteed Limits		
t_r, t_f	Maximum Input Rise and Fall Time					500	500	500	ns
C_{IN}	Input Capacitance				5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)				100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Timing Diagram

HCT191 Synchronous Binary Counter Typical Load, Count, and Inhibit Sequence



Sequence:

(1) Load (preset) to binary thirteen.

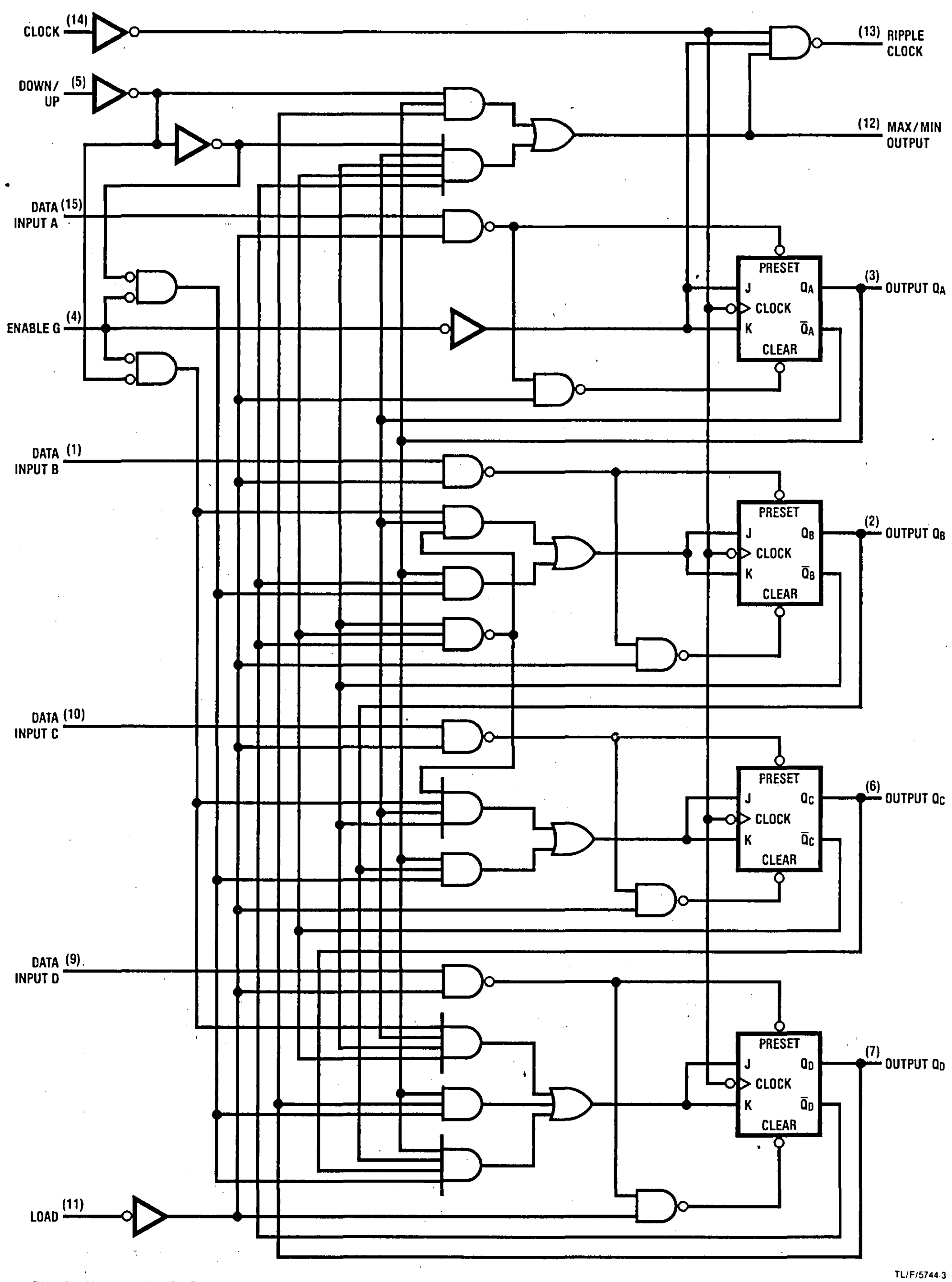
(2) Count up to fourteen, fifteen, zero, one, and two.

(3) Inhibit.

(4) Count down to one, zero, fifteen, fourteen, and thirteen.

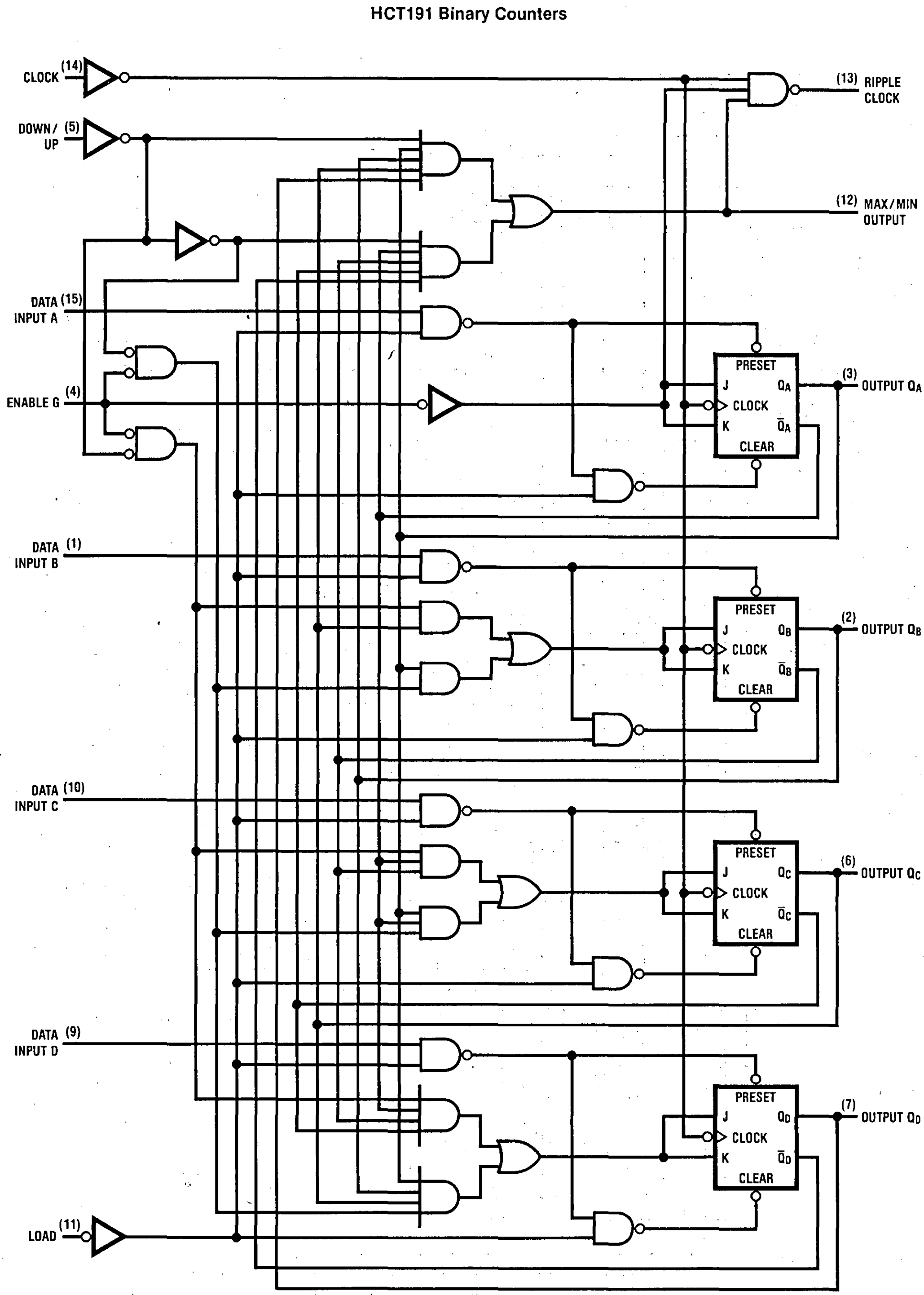
Logic Diagrams

HCT191



Pin 16 = V_{CC}, pin 8 = GND

Logic Diagrams (Continued)



Pin 16 = V_{CC}, pin 8 = GND

PRELIMINARY

microCMOS

MM54HCT193/MM74HCT193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize microCMOS technology, 3.0 micron silicon gate N-well CMOS to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HCT193/MM74HCT193 is a binary counter having two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low-to-high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This device has TTL compatible inputs. It can drive 15 LS-TTL loads.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low, the data is loaded independently of either clock input. This feature allows the counter to be used as a divide-by-n counter by modifying the count length with the preset inputs.

In addition, the HCT191 can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative-going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

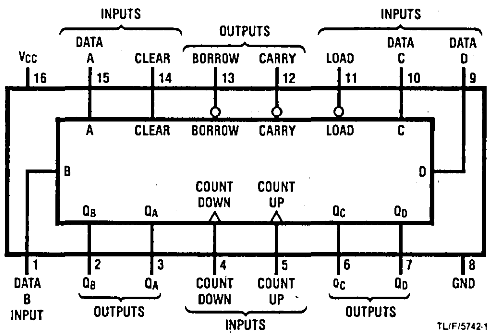
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, clock to output: 18 ns
- Typical operating frequency: 27 MHz
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5742-1

Truth Table

Count Up	Count Down	Clear	Load	Function
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level
L = low level
↑ = transition from low-to-high
X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		4.0	40	80	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF unless otherwise specified (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Clock Frequency	Count Up		25	MHz
		Count Down		25	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to CARRY	17	26	ns
t_{PHL}	Maximum Propagation Delay High to Low	Count Up to CARRY	18	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Down to BORROW	16	24	ns
t_{PHL}	Maximum Propagation Delay High to Low	Count Down to BORROW	15	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up or Down to Q	28	40	ns
t_{PHL}	Maximum Propagation Delay High to Low	Count Up or Down to Q	36	52	ns
t_{PLH}	Maximum Propagation Delay Low to High	Load to Q	30	42	ns
t_{PHL}	Maximum Propagation Delay High to Low	Load to Q	40	55	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q	35	47	ns
t_W	Minimum Pulse Width	Clear		16	ns
		Load		16	ns
		Count Up/Down		16	ns
t_{SD}	Minimum Set-Up Time	Data to Load	10	20	ns
t_{HD}	Minimum Hold Time	Data to Load	−3	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock		10	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (Note 6)

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to $85°C$	54HCT $T_A = -55°C$ to $125°C$	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency	Count Up	25	20	16	12	MHz
		Count Down	27	20	16	12	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to CARRY	13	28	35	42	ns
t_{PHL}	Maximum Propagation Delay High to Low	Count Up to CARRY	16	26	33	39	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay	Count Down to BORROW	16	26	33	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		8	15	19	22 19	ns ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up or Down to Q	35	43	54	65	ns
t_{PHL}	Maximum Propagation Delay High to Low	Count Up or Down to Q	35	43	54	65	ns

AC Electrical Characteristics (Continued) $V_{CC}=5V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (Note 6)

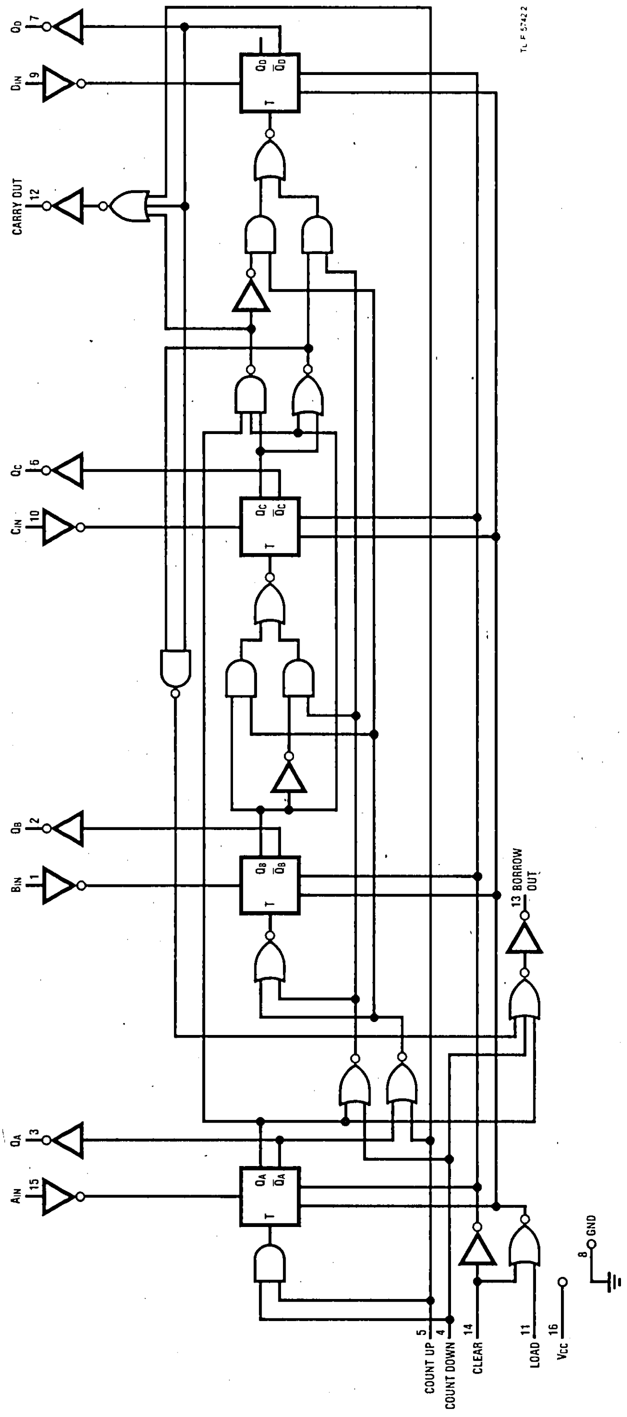
Symbol	Parameter	Conditions		$T_A=25°C$		74HCT $T_A=-40°C$ to $85°C$	54HCT $T_A=-55°C$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay Low to High	Load to Q		30	40	50	60	ns
t_{PHL}	Maximum Propagation Delay High to Low	Load to Q		30	40	50	60	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		30	40	50	60	ns
t_W	Minimum Pulse Width	Clear		42	16	20	24	ns
		Load		10	16	20	24	ns
		Count Up/Down		17	16	20	24	ns
		Clear	'HC193	21	16	20	24	ns
t_{SD}	Minimum Set-Up Time	Data to Load		10	20	25	30	ns
t_{HD}	Minimum Hold Time	Data to Load		−3	0	0	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock		−3	10	10	10	ns
t_r, t_f	Maximum Input Rise and Fall Time				300	300	300	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

MM54HCT193/MM74HCT193 Synchronous 4-Bit Up/Down Binary Counter



National Semiconductor

PRELIMINARY

microCMOS

MM54HCT240/MM74HCT240 Inverting Octal TRI-STATE® Buffer MM54HCT241/MM74HCT241 Octal TRI-STATE Buffer MM54HCT244/MM74HCT244 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT240/MM74HCT240 is an inverting buffer and the MM54HCT244/MM74HCT244 is non-inverting buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers. MM54HCT241/MM74HCT241 is also a non-inverting buffer like the 244 except that the 241 has one active high enable, each again controlling 4 buffers.

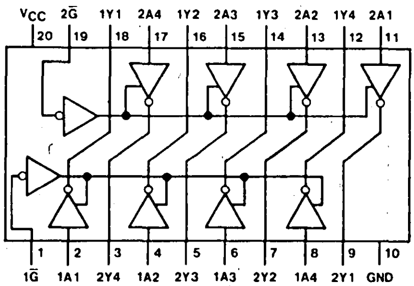
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA

Connection Diagrams

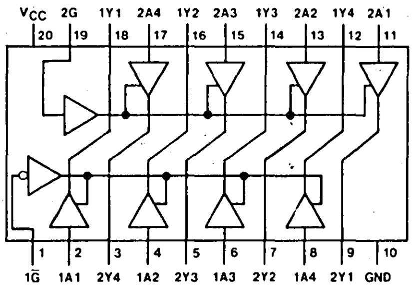
Dual-In-Line Packages



TOP VIEW TL/L/5020-1

MM54HCT240/MM74HCT240

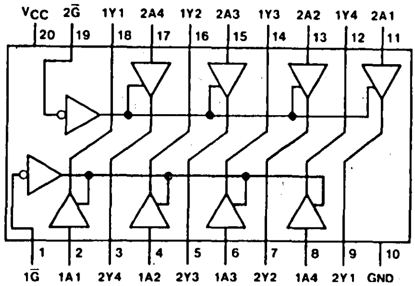
54HCT240 (J) 74HCT240 (J,N)



TOP VIEW TL/L/5020-2

MM54HCT241/MM74HCT241

54HCT241 (J) 74HCT241 (J,N)



TOP VIEW TL/F/5327-1

MM54HCT244/MM74HCT244

54HCT244 (J) 74HCT244 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND, $\overline{G}=V_{IH}$, $G=V_{IL}$		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

Truth Tables

'HCT240

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

'HCT241

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

'HCT244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H=high level, L=low level, Z=high impedance

AC Electrical Characteristics MM54HCT240/MM74HCT240

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$, (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	14	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	20	30	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	16	25	ns

AC Electrical Characteristics MM54HCT240/MM74HCT240

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions		$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		14	20	25	30	ns
		$C_L=150$ pF		20	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	$C_L=50$ pF	15	30	38	45	ns
			$C_L=150$ pF	26	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF		16	25	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}=V_{CC}$ $\overline{G}=GND$	5 90				pF pF

AC Electrical Characteristics MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$, (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	14	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	20	30	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	16	25	ns

AC Electrical Characteristics MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

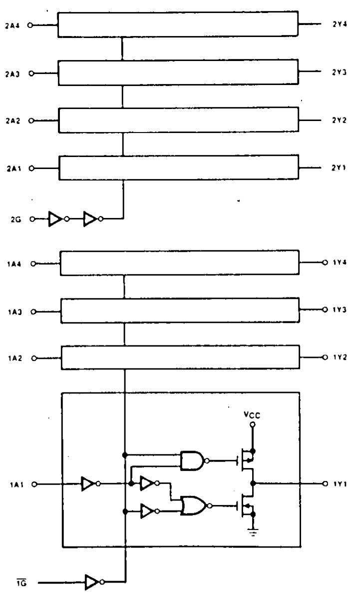
Symbol	Parameter	Conditions		$T_A=25°C$ Typ	$T_A=25°C$ Guaranteed Limits	74HCT $T_A=-40$ to 85°C Guaranteed Limits	54HCT $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		14	20	25	30	ns
		$C_L=150$ pF		20	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	$C_L=50$ pF	21	30	38	45	ns
			$C_L=150$ pF	26	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF		16	25	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}=V_{CC}$ $\overline{G}=GND$	5 90				pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

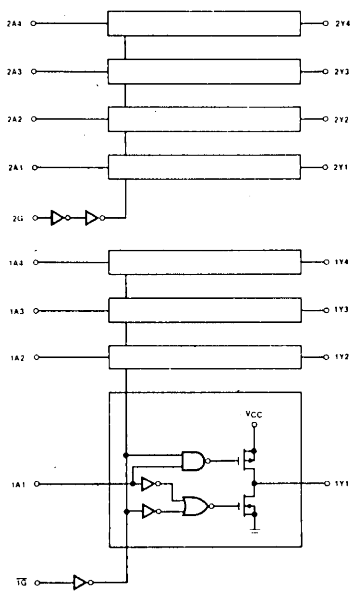
Logic Diagrams

'HCT240



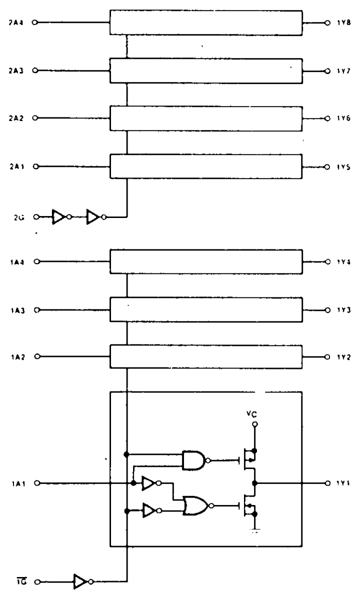
TL/L/5020-3

'HCT241



TL/L/5020-4

'HCT244



TL/F/5327-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT245/MM74HCT245 Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bi-directional buffer utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

This device is TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

MM54HCT245/MM74HCT245 has one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A.

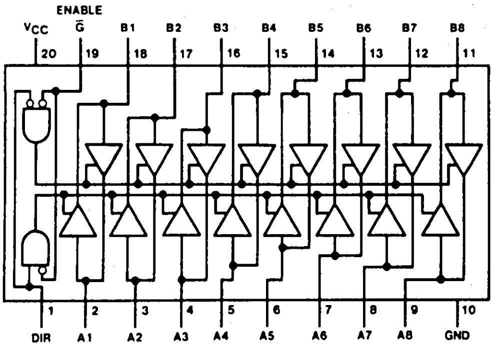
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typ.
- High speed: 16 ns typical propagation delay
- Low Power: 80 μA (74 Series)

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5165-1

MM54HCT245/MM74HCT245

54HCT245 (J) 74HCT245 (J,N)

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	245
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H = high level L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

(V_{CC}=5V±10%, unless otherwise specified.)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or ground.

AC Electrical Characteristics MM54HCT245/MM74HCT245

$V_{CC}=5.0V$, $t_r=t_f=6$ ns, $T_A=25°C$, (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	20	25	ns

AC Electrical Characteristics MM54HCT245/74HCT245

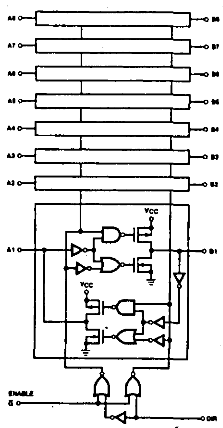
$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions		$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		14	23	29	34	ns
		$C_L=150$ pF		17	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	$C_L=50$ pF	31	42	53	63	ns
			$C_L=150$ pF	35	49	62	74	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF		8	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance	(Note 5) $\overline{G} = V_{CC}$ $\overline{G}$ = GND		7 100				pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



National Semiconductor

microCMOS

MM54HCT257/MM74HCT257 Quad 2-Channel TRI-STATE® Multiplexer

General Description

This QUAD 2-TO-1 LINE DATA SELECTOR/MULTIPLEXER utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

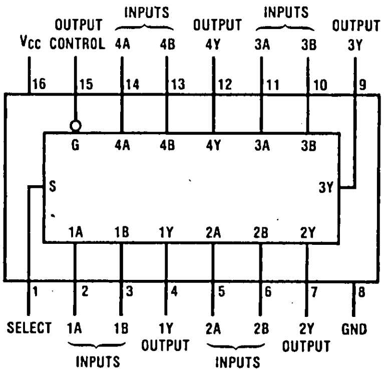
The 54HCT/74HCT logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 µA maximum (74HCT series)
- TRI-STATE outputs for connection to system buses.
- Completely TTL compatible

Connection and Logic Diagrams

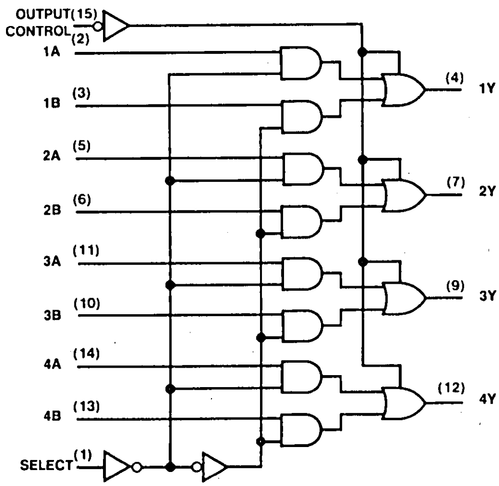
Dual-In-Line Package



TOP VIEW TL/F/5329-1

MM54HCT257/MM74HCT257

54HCT257 (J) 74HCT257 (J,N)



TL/F/5329-2

Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=4.5V		500	ns

DC Electrical Characteristics (Note 4) V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			0.9	0.9	0.9	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	4.5	4.4	4.4	4.4	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA V_{CC}=4.5V $\|I_{OUT}\| \le 7.8$ mA V_{CC}=5.5V	4.2	3.98 4.98	3.84 4.84	3.7 4.7	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 6.0$ mA V_{CC}=4.5V $\|I_{OUT}\| \le 7.8$ mA V_{CC}=5.5V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	$V_{OUT}=V_{CC}$ or GND OC=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=45 pF, t_r=t_f=6 ns (unless otherwise noted.)

Symbol	Parameter	Condition	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Select to any Output		19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A or B to any Output		24	38	ns
t_{PZH}, t_{PZL}	Maximum Enable Time	R_L = 1 kΩ	20	30	ns
t_{PHZ}, t_{PLZ}	Maximum 1	R_L = 1 kΩ C_L = 5 pF	15	25	ns

AC Electrical Characteristics V_{CC}=5V ± 10%, t_r=t_f=6 ns, C_L = 50 pF (unless otherwise noted.)

Symbol	Parameter	Condition	T_A = 25°C		74HCT T_A =-40°C to 85°C	54HCT T_A = -55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Output	C_L = 150 pF	12 12	20 30	25 38	30 45	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Output	C_L = 150 pF	 15	20 30	25 38	30 45	ns ns
t_{PZH}, t_{PZL}	Maximum Enable to any Output		21	30	38	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		9	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)						pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption. $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT273/MM74HCT273 Octal D Flip-Flop with Clear

General Description

The MM54HCT273/MM74HCT273 utilizes 3.0 micron N-well microCMOS technology. It has input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear and independent Q outputs. Data on a D input, having the specified set-up and hold time is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

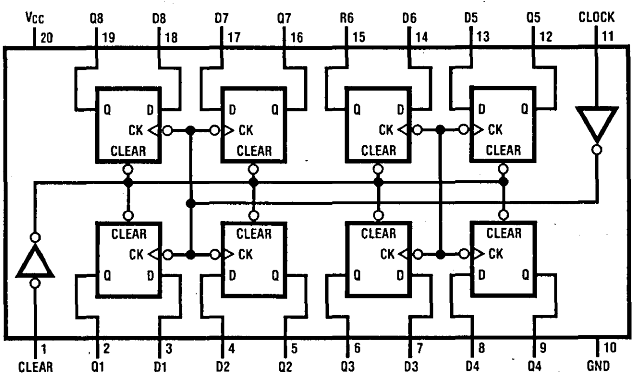
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

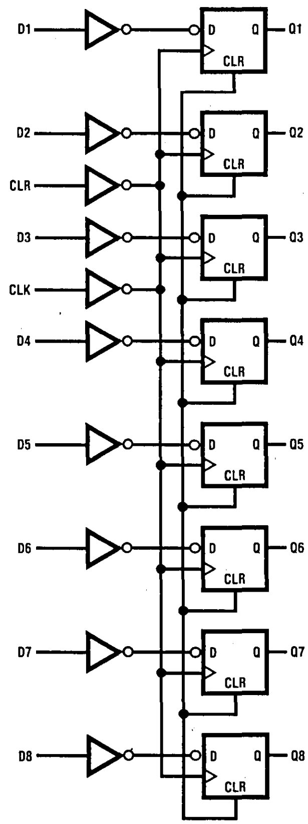
Dual-In-Line Package



TOP VIEW

TL/F/5760-1

Logic Diagram



TL/F/5760-2

Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↑ = transition from low to high level
Q0 = the level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	74HCT T_A = −40°C to 85°C Guaranteed Limits	54HCT T_A = −55°C to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		18	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set-Up Time D to Clock		10	20	ns
t_H	Minimum Hold Time Clock to D		−3	0	ns
t_W	Minimum Pulse Width Clock or Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified (Note 6)

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to 85°C	54HCT $T_A = -55°C$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		22	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Set-Up Time D to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to D		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT299/MM74HCT299 8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HCT299/MM74HCT299 is TTL input compatible. It features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines, S0 and S1, high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

The MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These devices are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

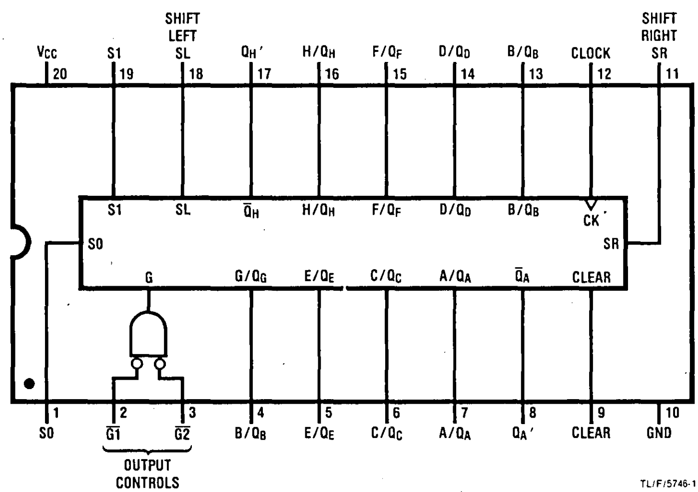
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TRI-STATEable I/O
- Output drive capability: 15 LS-TTL loads
- Cascadable for n-bit word lengths
- Clock-independent clear

Connection Diagram

Dual-In-Line Package



TL/F/5746-1

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X	H	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high, the eight input/output terminals are disabled to the high impedance state; however, sequential operation or clearing of the register is not affected.

MM54HCT323/MM74HCT323
8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HCT323/MM74HCT323 is TTL input compatible. It features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines, S0 and S1, high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A synchronous CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

The MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These devices are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

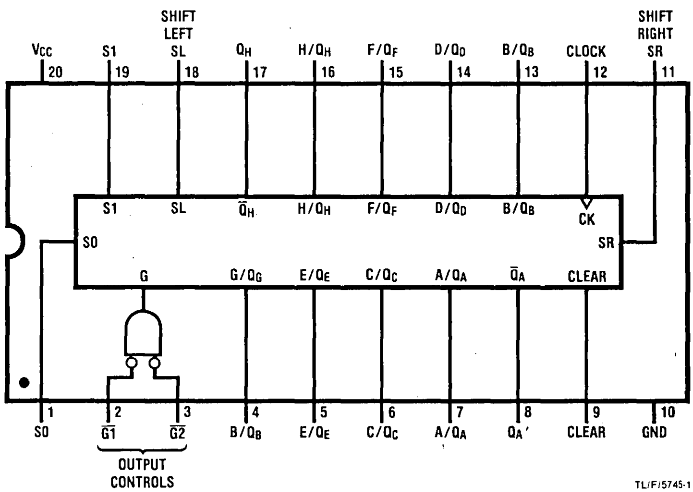
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TRI-STATEable I/O
- Output drive capability: 15 LS-TTL loads
- Cascadable for n-bit word lengths
- Synchronous clear

Connection Diagram

Dual-In-Line Package



TL/F/5745-1

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Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	$\uparrow$	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	$\uparrow$	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	$\uparrow$	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	$\uparrow$	X	H	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	$\uparrow$	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	$\uparrow$	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	L
Load	H	H	H	X	X	$\uparrow$	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high, the eight input/output terminals are disabled to the high impedance state; however, sequential operation or clearing of the register is not affected.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT373/MM74HCT373 TRI-STATE® Octal D-Type Latch MM54HCT374/MM74HCT374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT373/MM74HCT373 Octal D-TYPE LATCHES and MM54HCT374/MM74HCT374 Octal D-TYPE FLIP FLOPS utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pinout compatible. The TRI-STATE outputs are capable of driving 15 LS TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT373/MM74HCT373 LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT374/MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

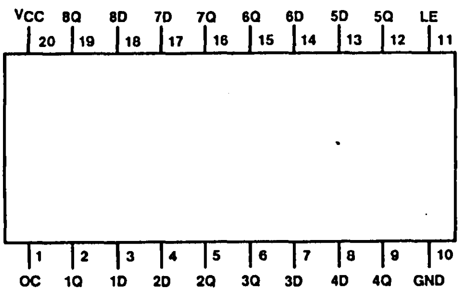
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

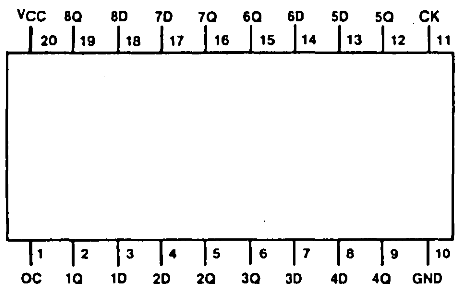


TL/F/5367-1

MM54HCT373/MM74HCT373

54HCT373 (J) 74HCT373 (J,N)

Dual-In-Line Package



TL/F/5367-2

MM54HCT374/MM74HCT374

54HCT374 (J) 74HCT374 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°G
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		|I_{OUT}|=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		|I_{OUT}|=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		|I_{OUT}|=20 μA	0	0.1	0.1	0.1	V
		|I_{OUT}|=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT373/MM74HCT373

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT373/MM74HCT373

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=50$ pF $C_L=150$ pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=50$ pF $C_L=150$ pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

Truth Tables

'373

Output Control	LE	Data	373 Output	573 Output
L	H	H	H	L
L	H	L	L	H
L	L	X	Q_0	$\overline{Q0}$
H	X	X	Z	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance

'374

Output Control	Clock	Data	Output (374)	Output (534)
L	↑	H	H	L
L	↑	L	L	H
L	L	X	Q_0	$\overline{Q_0}$
H	X	X	Z	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established.

AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified)

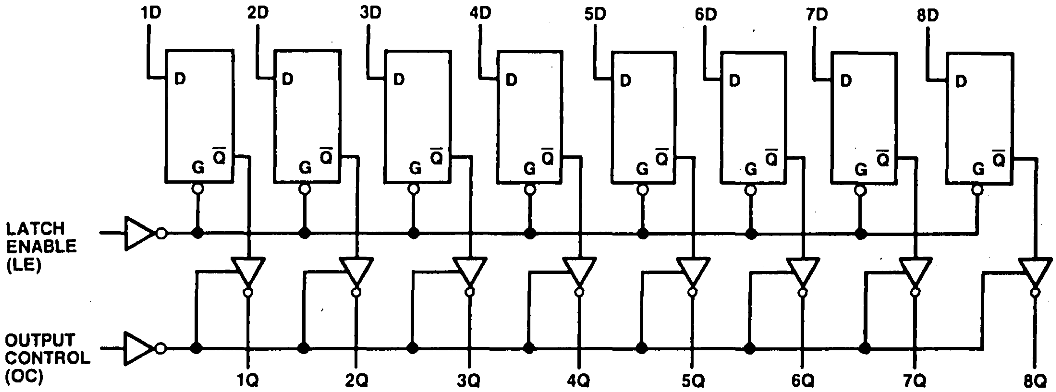
Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=50$ pF $C_L=150$ pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+\ I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

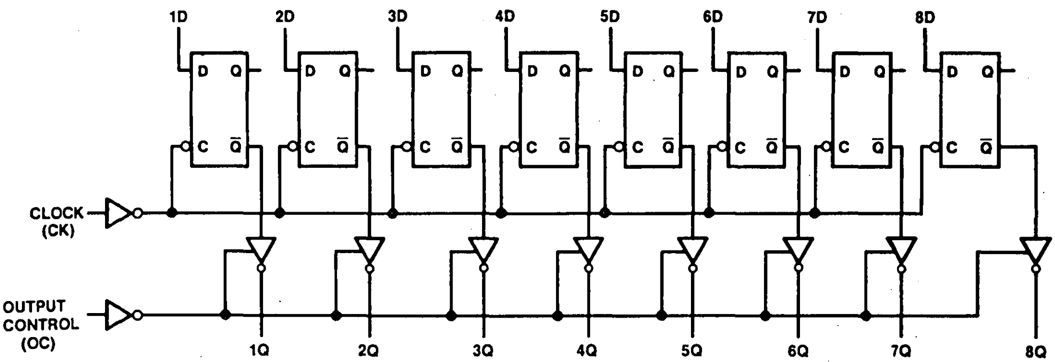
Logic Diagrams

MM54HCT373/MM74HCT373



TL/F/5367-4

MM54HCT374/MM74HCT374



TL/F/5367-5

MM54/74HCT521

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT521/MM74HCT521 8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

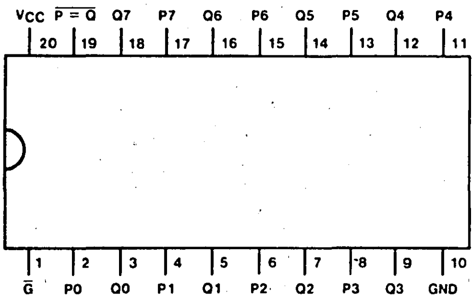
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL Input Compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Large output current: 4 mA

Connection and Logic Diagrams

Dual-In-Line Package

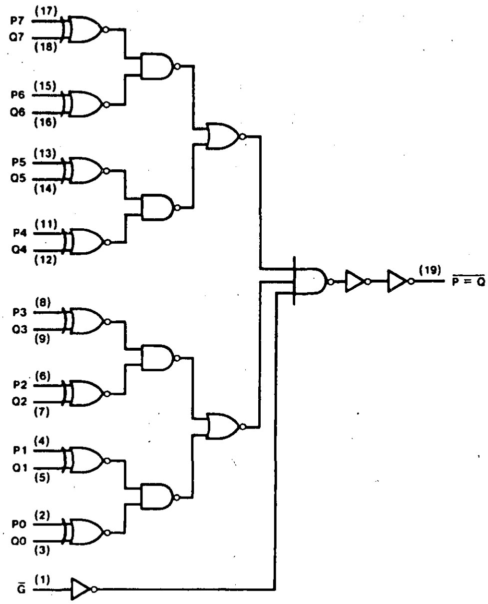


TOP VIEW

TL/F/5018-1

MM54HCT521/MM74HCT521

54HCT521 (J) 74HCT521 (J,N)



TL/F/5018-2

Truth Table

Inputs		$\overline{P=Q}$
Data P, Q	Enable $\overline{G}$	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

(V_{CC}=5V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=0.8V or 2.0V					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−.1	V_{CC}−.1	V_{CC}−.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V0.8V or 2.0V					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	0.5				mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_F = 6 ns (unless otherwise noted.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay - P or Q to Output		19	30	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		13	22	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		13	20	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		10	18	ns

AC Electrical Characteristics V_{CC} = 5V ± 10%, C_L = 50 pF, t_r = t_f = 6 ns, (unless otherwise specified.)

			T_A = 25°C		74HCT T_A = −40°C to 85°C	54HCT T_A = −55 to 125°C	
Symbol	Parameter	Condition	Typ	Guaranteed Limits			Units
t_{PHL}	Maximum Propagation Delay - P or Q to Output		23	35	44	53	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		16	24	30	36	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		16	24	30	36	ns
t_{PLH}	Maximum Propagation Delay - Enable to Output		11	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		45				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT533/MM74HCT533 TRI-STATE® Octal D-Type Latch MM54HCT534/MM74HCT534 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT533/MM74HCT533 Octal D-TYPE LATCHES and MM54HCT534/MM74HCT534 Octal D-TYPE FLIP FLOPS utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pinout compatible. The TRI-STATE outputs are capable of driving 15 LS TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT533/MM74HCT533 LATCH ENABLE input is high, the $\overline{Q}$ outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT534/MM74HCT534 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

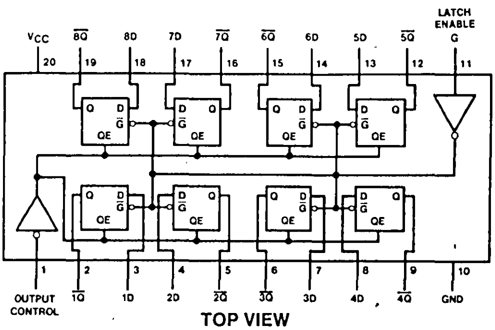
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 18 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

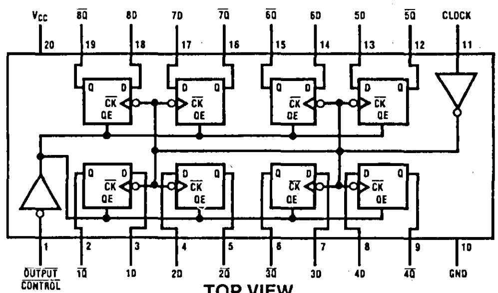


TOP VIEW

MM54HCT533/MM74HCT533

TL/F/5339-1

Dual-In-Line Package



TOP VIEW

TL/F/5340-1

MM54HCT534/MM74HCT534

Truth Tables

'HCT533

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

'HCT534

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
$\overline{Q}_0$ = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V $\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	 V_{CC} 4.2 5.7	 V_{CC}−0.1 3.98 4.98	 V_{CC}−0.1 3.84 4.84	 V_{CC}−0.1 3.7 4.7	 V V V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V $\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	 0 0.2 0.2	 0.1 0.26 0.26	 0.1 0.33 0.33	 0.1 0.4 0.4	 V V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT533/MM74HCT533

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT533/MM74HCT533

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=50$ pF $C_L=150$ pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=50$ pF $C_L=150$ pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

AC Electrical Characteristics MM54HCT534/MM74HCT534

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT534/MM74HCT534

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=50$ pF $C_L=150$ pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+\ I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT540/MM74HCT540 Inverting Octal TRI-STATE® Buffer MM54HCT541/MM74HCT541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT540/MM74HCT540 is an inverting buffer and the MM54HCT541/MM74HCT541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

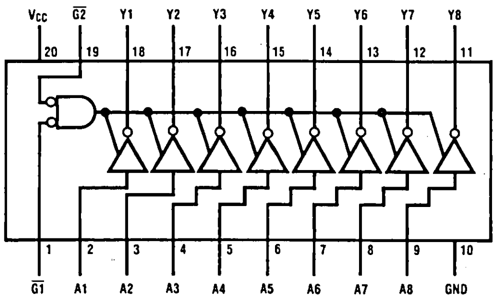
In order to enhance PC board layout, the 'HCT540 and 'HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA

Connection Diagrams

Dual-In-Line Package

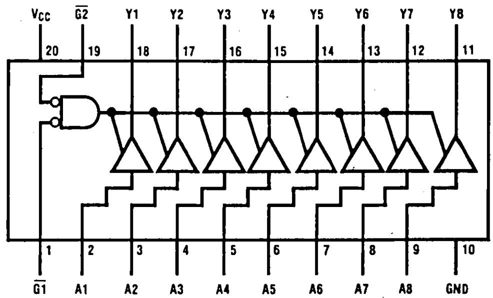


TOP VIEW

TL/F/5341-1

MM54HCT540/MM74HCT540

54HCT540 (J) 74HCT540 (J,N)



TOP VIEW

TL/F/5341-2

MM54HCT541/MM74HCT541

54HCT541 (J) 74HCT541 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert=20\ \mu A$	V_{CC}	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
		$\lvert I_{OUT}\rvert=6.0$ mA, $V_{CC}=4.5V$	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert=7.2$ mA, $V_{CC}=5.5V$	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\lvert I_{OUT}\rvert=20\ \mu A$	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert=6.0$ mA, $V_{CC}=4.5V$	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert=7.2$ mA, $V_{CC}=5.5V$	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND, $\overline{G}=V_{IH}$		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0\ \mu A$		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

AC Electrical Characteristics MM54HCT540/MM74HCT540

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	14	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	13	25	ns

AC Electrical Characteristics MM54HCT540/MM74HCT540

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		12	20	25	30	ns
		$C_L=150$ pF		22	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	$C_L=50$ pF	15	30	38	45	ns
			$C_L=150$ pF	20	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}=V_{CC}$ $\overline{G}=GND$	12 50				pF pF

AC Electrical Characteristics MM54HCT541/MM74HCT541

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	15	25	ns

AC Electrical Characteristics MM54HCT541/MM74HCT541

V_{CC}=5.0V ±10%, t_r=t_f=6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L=50 pF		14	23	29	34	ns
		C_L=150 pF		17	33	42	49	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L=1 kΩ	C_L=50 pF	17	30	38	45	ns
			C_L=150 pF	22	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L=1 kΩ C_L=50 pF		17	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L=50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}$=V_{CC}	12				pF
			$\overline{G}$=GND	45				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT543/MM74HCT543 Octal Registered Transceiver

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are also input and output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The HCT543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable and output enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

For data flow from A to B, for example, the A-to-B enable ($\overline{EAB}$) input must be 'low' in order to enter data from A0–A7 or take data from B0–B7, as indicated in the I/O Control Table. With $\overline{EAB}$ low, a low signal on A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both low, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but uses the $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Features

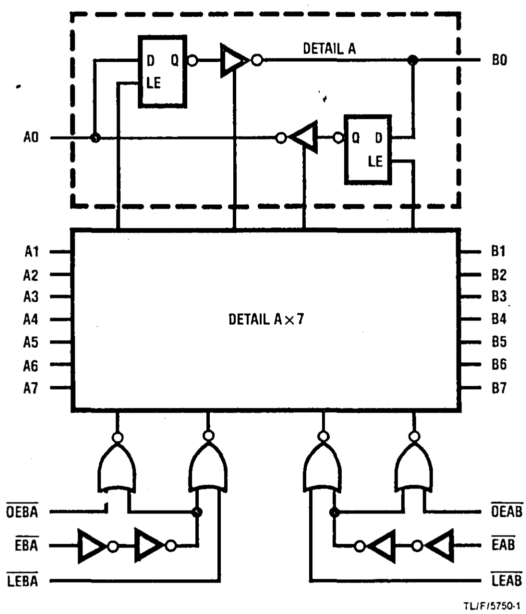
- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications
- Output drive capability: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Separate controls for data flow in each direction

I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{EAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	X	X	Storing	Hi-Z
X	H	—	Storing	—
X	—	H	—	Hi-Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs *

* Before $\overline{LEAB}$ low-to-high transition
H = high voltage level
L = low voltage level
X = don't care
†A-to-B data flow shown: B-to-A flow control is the same, except uses $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

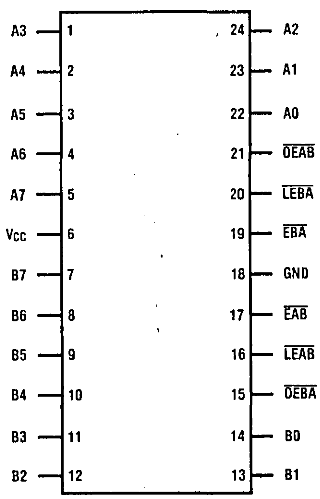
Logic Diagram



TL/F/5750-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5750-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT544/MM74HCT544 Octal Registered Inverting Transceiver

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are also input and output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The HCT544 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable and output enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

For data flow from A to B, for example, the A-to-B enable ($\overline{EAB}$) input must be 'low' in order to enter data from A0–A7 or take data from B0–B7, as indicated in the I/O Control Table. With $\overline{EAB}$ low, a low signal on A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both low, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but uses the $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Features

- Inverting outputs
- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications
- Output drive capability: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Separate controls for data flow in each direction

I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{EAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0-B7
H	X	X	Storing	Hi-Z
X	H	—	Storing	—
X	—	H	—	Hi-Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs*

* Before $\overline{LEAB}$ low-to-high transition

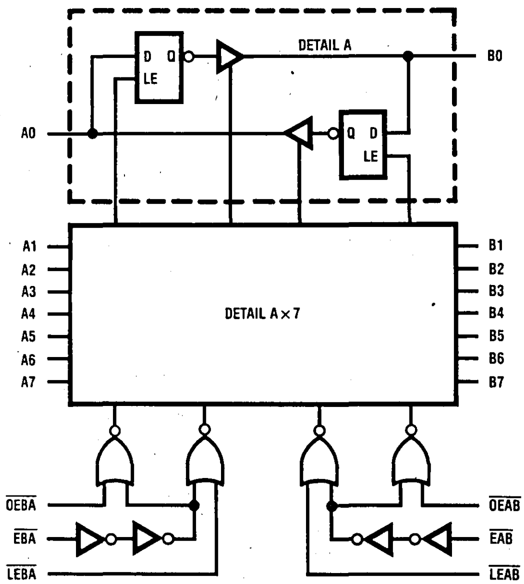
H = high voltage level

L = low voltage level

X = don't care

†A-to B data flow shown: B-to-A flow control is the same, except uses $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

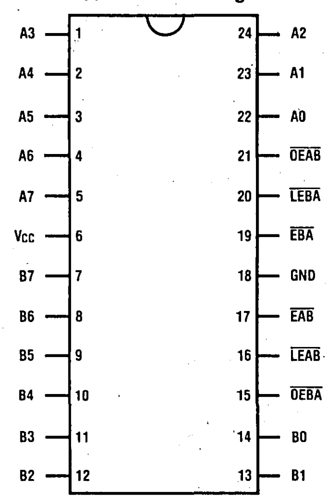
Logic Diagram



TL/F/5749-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5749-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT550/MM74HCT550 Octal Registered Transceiver with Status Flags

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are also input and output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The MM54HCT550/MM74HCT550 contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer.

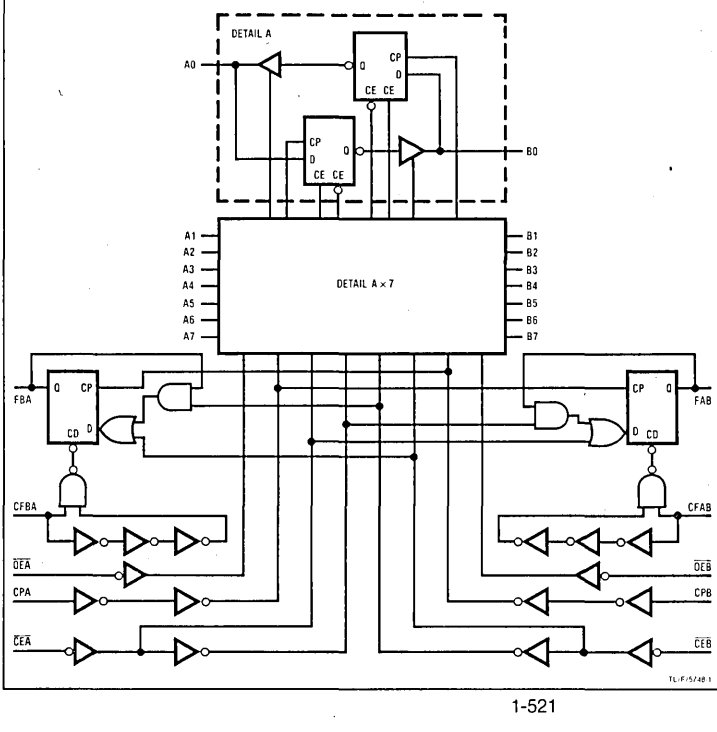
Data applied to the A inputs is entered and stored on the rising edge of the A clock pulse (CPA), provided that the A clock enable ($\overline{CEA}$) is low; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes high. Data thus entered from the A inputs is present at the inputs to the B output buffers, but appears only on the B I/O pins when the B output enable ($\overline{OEB}$) signal is made low. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a low-to-high transition to the CFAB input. Optionally, the $\overline{OEA}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output high. A low signal on $\overline{OEA}$ enables the A output buffers and a low-to-high transition on CFBA clears the FBA flag.

Features

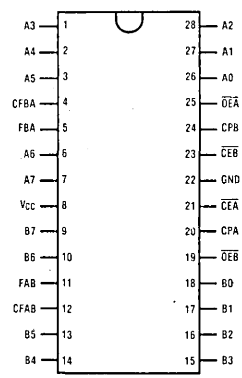
- TTL compatible inputs
- Output drive: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5748-2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT551/MM74HCT551 Octal Registered Inverting Transceiver with Status Flags

General Description

This octal transceiver utilizes microCMOS technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. These devices possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. They are also input and output compatible with LS-TTL, and can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

The MM54HCT551/MM74HCT551 contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer.

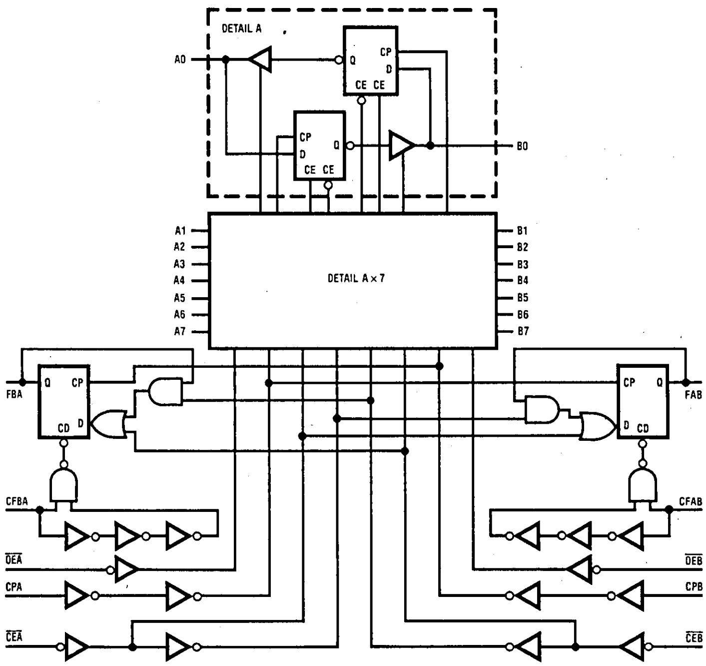
Data applied to the A inputs is entered and stored on the rising edge of the A clock pulse (CPA), provided that the A clock enable ($\overline{CEA}$) is low; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes high. Data thus entered from the A inputs is present at the inputs to the B output buffers, but appears only on the B I/O pins when the B output enable ($\overline{OEB}$) signal is made low. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a low-to-high transition to the CFAB input. Optionally, the $\overline{OEA}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output high. A low signal on $\overline{OEA}$ enables the A output buffers and a low-to-high transition on CFBA clears the FBA flag.

Features

- Inverting outputs
- TTL compatible inputs
- Output drive: 15 LS-TTL loads
- Large output current: 6 mA
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags

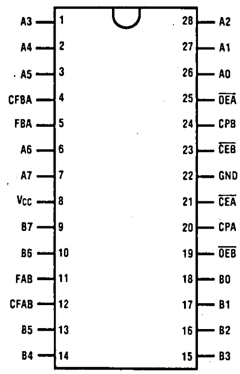
Logic Diagram



TL/F/5747-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5747-2

National Semiconductor

microCMOS

MM54HCT563/MM74HCT563 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is high, the Q outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

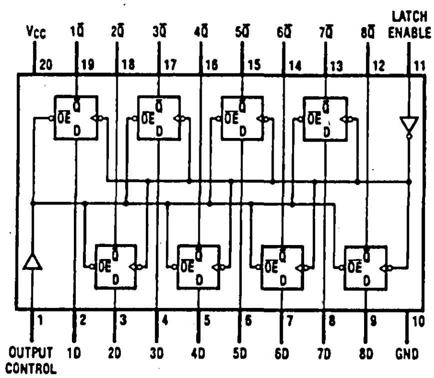
The 54HCT/74HCT logic family is speed, function and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74 series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- TTL input characteristic compatible

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5210-1

MM54HCT563/MM74HCT563

54HCT563 (J) 74HCT563 (J,N)

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q0}$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HCT T_A=−40 to 85°C Guaranteed Limits	54HCT T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT563/MM74HCT563

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT563/MM74HCT563

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=50$ pF $C_L=150$ pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=50$ pF $C_L=150$ pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

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microCMOS

MM54HCT564/MM74HCT564 TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These octal D-type flip-flops utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

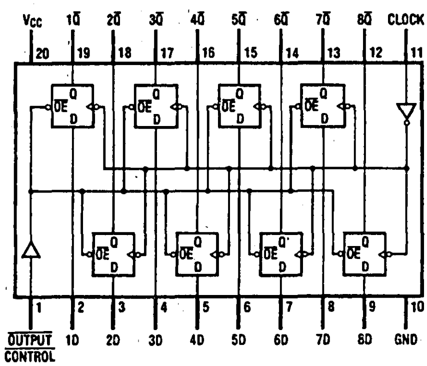
The 54HCT/74HCT logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- TTL input characteristic compatible

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5211-1

MM54HCT564/MM74HCT564

54HCT564 (J) 74HCT564 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High Impedance State
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable = V_{IH} or V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT564/MM74HCT564

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT564/MM74HCT564

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=50$ pF $C_L=150$ pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

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MM54HCT573/MM74HCT573 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE(LE) input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

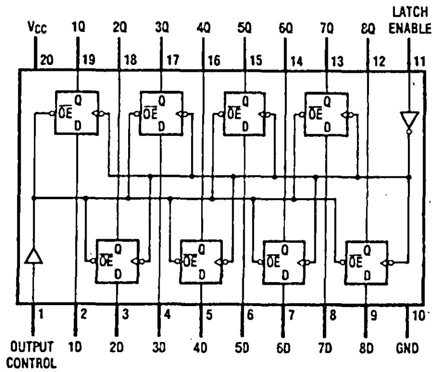
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- TTL input characteristic compatible
- Typical propagation delay: 14 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5212-1

MM54HCT573/MM74HCT573

54HCT573 (J) 74HCT573 (J,N)

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time		10	15	ns
t_H	Minimum Hold Time		2	5	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pf (unless otherwise noted.)

Symbol	Parameter	Conditions	$T_A=25°C$ Typ	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to $\overline{Q}$	$C_L=50$ pF $C_L=150$ pF	14 21	22 30	28 38	33 40	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF $C_L=150$ pF	14 21	23 31	29 47	35 47	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF $C_L=150$ pF	 15 24	 28 36	 35 45	 42 54	 ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	13	25	31	38	ns
t_S	Minimum Set Up Time		10	15	19	22	ns
t_H	Minimum Hold Time			5	5	5	ns
t_W	Minimum Pulse Width		9	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	7	12	15	18	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$OE=V_{CC}$ $OE=GND$	30 50				pF pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HCT574/MM74HCT574 TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed octal D-type flip-flops utilize micro-CMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

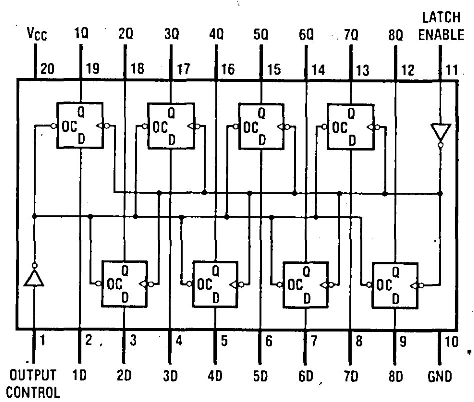
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

Features

- TTL input characteristic compatible
- Typical propagation delay: 15 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



TL/F/5213-1

TOP VIEW

MM54HCT574/MM74HCT574

54HCT574 (J) 74HCT574 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\lvert I_{OUT}\rvert$=20 μA	0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set-Up Time			20	ns
t_H	Minimum Hold Time			0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF $C_L=150$ pF	13 19	23 31	29 47	35 47	ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ					
		$C_L=50$ pF $C_L=150$ pF	14 20	28 36	35 45	42 54	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	12	25	31	38	ns
t_S	Minimum Set-Up Time			20	25	30	ns
t_H	Minimum Hold Time			0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	7	12	15	18	ns
t_W	Minimum Pulse Width		9	16	20	24	ns
t_r,t_f	Maximum Output Rise and Fall Time			500	500	500	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=VCC OC=GND	30 50				pF pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HCT590/MM74HCT590 8-Bit Binary Counter with TRI-STATE® Output Register

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits. This device is input compatible with 54LS/74LS and other TTL output compatible circuits, and may be used as a lower power direct replacement for the LS equivalent device.

The MM54HCT590/MM74HCT590 contain an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{\text{CCKEN}}$, is low. When the counter increments to the all ones condition ripple carry out, $\overline{\text{RCO}}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{\text{RCO}}$ of the first stage to the $\overline{\text{CCKEN}}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{\text{RCO}}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed TRI-STATE outputs which are enabled when the enable input, $\overline{\text{G}}$, is taken low. This enables connection of this part to a system bus.

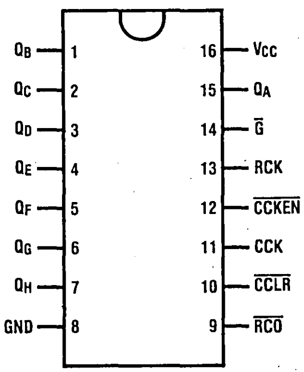
The MM54HCT590/MM74HCT590 are functional, speed and pin equivalent to the equivalent LS-TTL circuit, and may be used as a direct replacement for the equivalent LS-TTL IC. Its inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 4.5V to 5.5V
- Guaranteed TTL compatible input logic levels: 2.0V and 0.8V
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HCT)

Connection Diagram

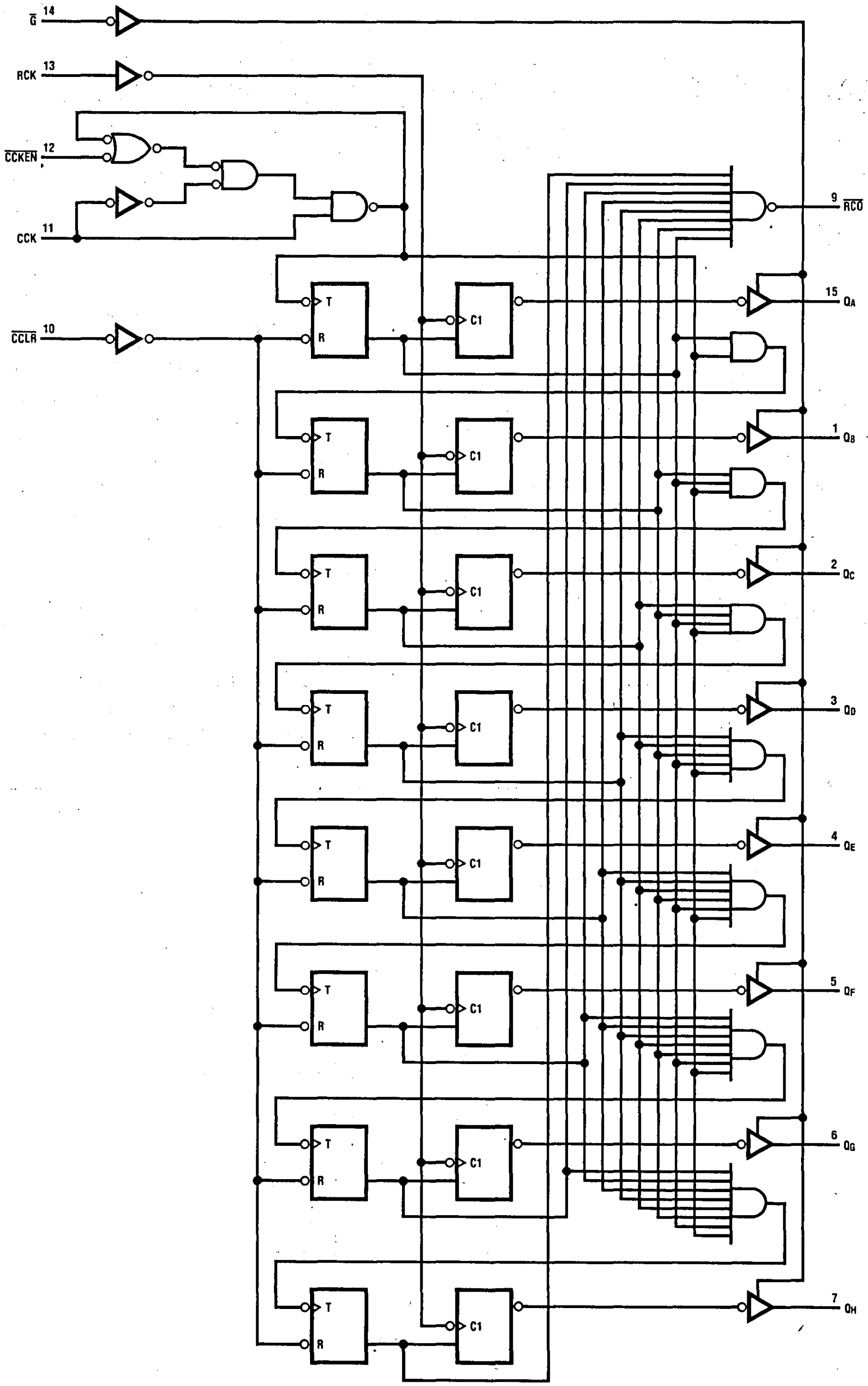
Dual-In-Line Package



TOP VIEW

TL/F/5768-1

Logic Diagram



TL/F/5768-2

National Semiconductor

microCMOS

MM54HCT592/MM74HCT592 8-Bit Binary Counter with Input Register
MM54HCT593/MM74HCT593 8-Bit Binary Counter with Bidirectional Input Register/Counter Outputs

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits. This device is input compatible with 54LS/74LS and other TTL output compatible circuits, and may be used as a lower power direct replacement for the LS equivalent device.

The MM54HCT592/MM74HCT592 and the MM54HCT593/MM74HCT593 contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{\text{CCKEN}}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{\text{RCO}}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{\text{RCO}}$ of the first stage to the $\overline{\text{CCKEN}}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{\text{RCO}}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, $\overline{\text{CLOAD}}$, input is taken low.

The 'HCT592 differs from the 'HCT593 in that the latter device has bidirectional input/output pins. The TRI-STATE® outputs of the counter can be enabled and are active when enable input, $\overline{\text{G}}$, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The 'HCT593 also has a second clock enable pin, CKEN, which is active high and it also has an active low register clock enable, $\overline{\text{RCKEN}}$.

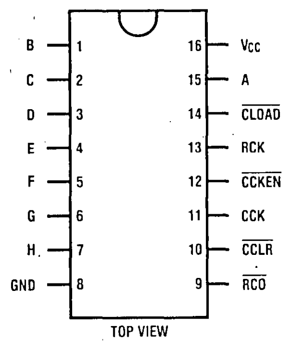
The MM54HCT592/MM74HCT592 and the MM54HCT593/MM74HCT593 are functional, speed and pin equivalent to the equivalent LS-TTL circuit and may be used as a direct replacement for the equivalent LS-TTL IC. Their inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 4.5V to 5.5V
- Guaranteed TTL compatible input logic levels: 2.0V and 0.8V
- Wide operating frequency range: 30 MHz
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HCT)

Connection Diagrams

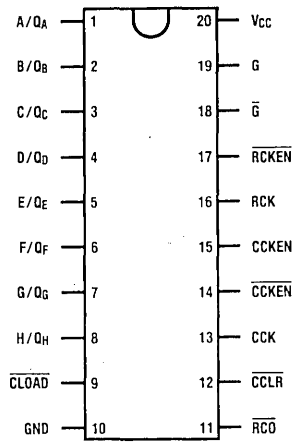
Dual-In-Line Package
MM54HCT592/MM74HCT592



TOP VIEW

TL/F/5769-1

Dual-In-Line Package
MM54HCT593/MM74HCT593

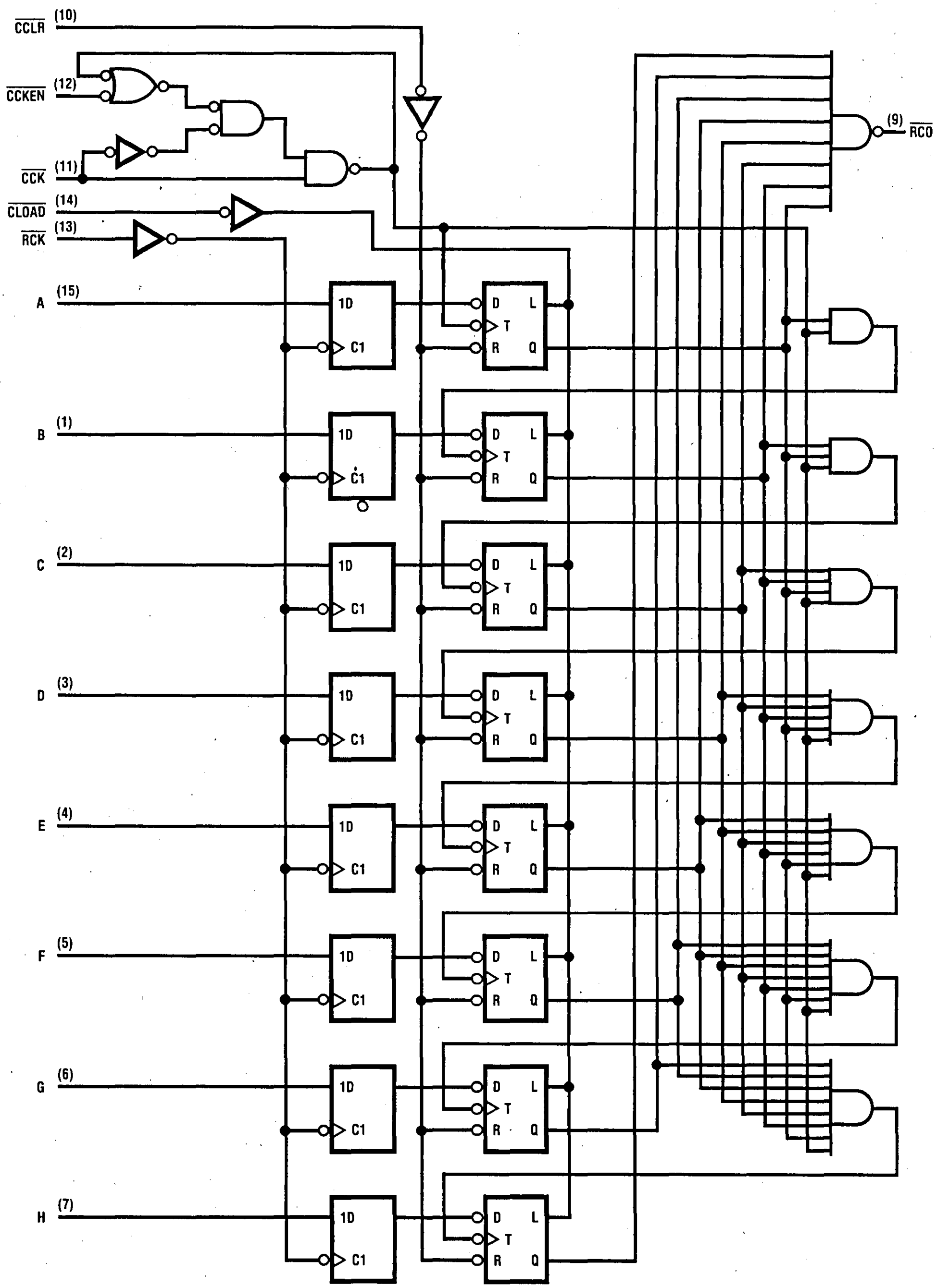


TOP VIEW

TL/F/5769-2

Logic Diagrams

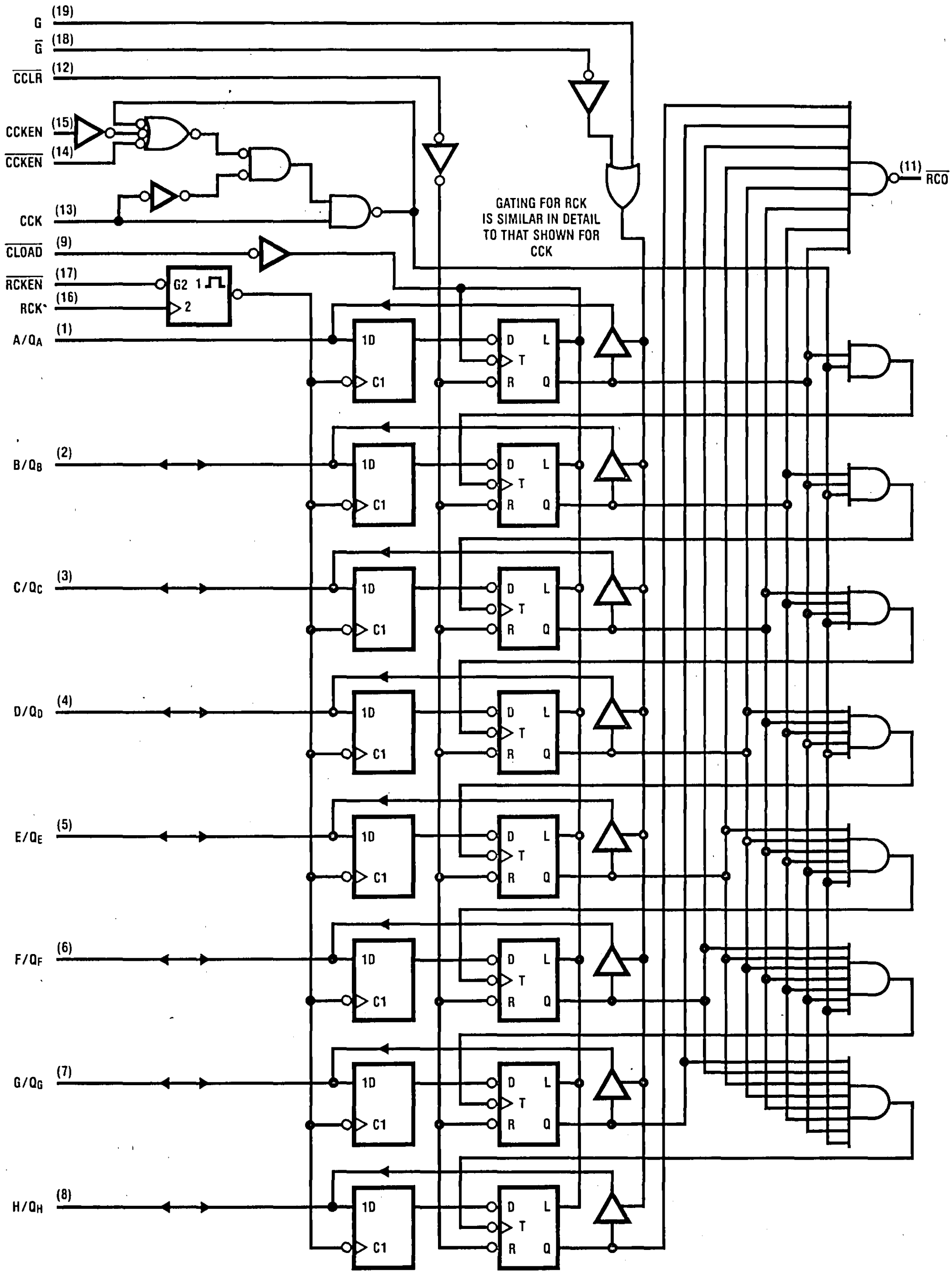
HCT592



TL/F/5769-3

Logic Diagrams (Continued)

HCT593



TL/F/5769-4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE® Transceiver MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Both the MM54HCT640/74HCT640 and the MM54HCT643/74HCT643 have one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The MM54HCT640/74HCT640 transfers inverted data from one bus to the other. The MM54HCT643/74HCT643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus.

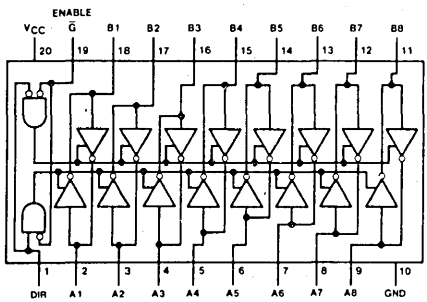
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typical.
- High Speed: 12 ns typical propagation delay
- Low power: 80 μA maximum (74HCT)

Connection Diagrams

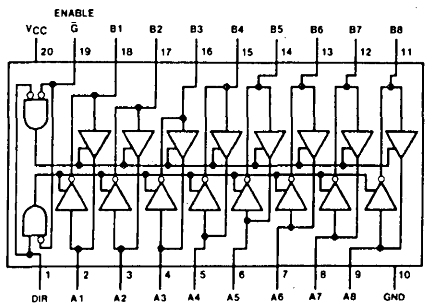
Dual-In-Line Package



TOP VIEW TL/F/5344-1

MM54HCT640/MM74HCT640

54HCT640 (J) 74HCT640 (J,N)



TOP VIEW TL/F/5344-2

MM54HCT643/MM74HCT643

54HCT643 (J) 74HCT643 (J,N)

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC}=5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}-0.1	V_{CC}-0.1	V_{CC}-0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable$\overline{G}$=V_{IH} or V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC}=5.0V, t_r=t_f=6 ns, T_A=25°C (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L=45 pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L=45 pF R_L=1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L=5 pF R_L=1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT640/MM74HCT640

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		17	23	29	34	ns
		$C_L=150$ pF		17	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1k\Omega$	$C_L=50$ pF	31	42	53	63	ns
			$C_L=150$ pF	35	49	62	74	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1k\Omega$ $C_L=50$ pF		21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}=V_{CC}$ $\overline{G}=GND$	7 100				pF pF

AC Electrical Characteristics MM54HCT643/MM74HCT643

$V_{CC}=5.0V$, $t_r=t_f=6$ ns, $T_A=25°C$ (unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	20	25	ns

AC Electrical Characteristics MM54HCT643/MM74HCT643

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		17	23	29	34	ns
		$C_L=150$ pF		17	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1k\Omega$	$C_L=50$ pF	31	42	53	63	ns
			$C_L=150$ pF	35	49	62	74	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=50$ pF		21	30	38	45	ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}=V_{CC}$ $\overline{G}=GND$	7 100				pF pF

Note 5: C_{PD} determines the no load power consumption. $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$. The no load dynamic current consumption, $I_S=C_{PD}V_{CC}+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HCT688/MM74HCT688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

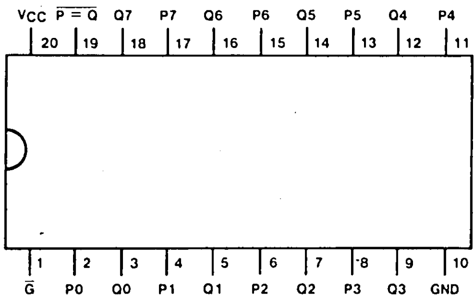
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL Input Compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Large output current: 4 mA
- Same as HCT521

Connection and Logic Diagrams

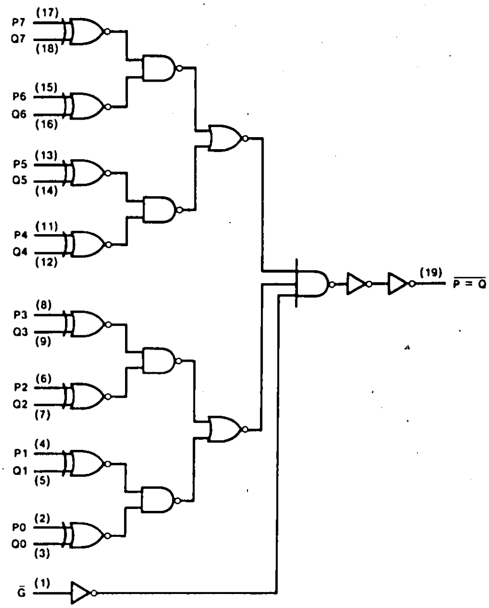
Dual-In-Line Package



TOP VIEW TL/F/5018-1

MM54HCT688/MM74HCT688

54HCT688 (J) 74HCT688 (J,N)



TL/F/5018-2

Truth Table

Inputs		
Data P, Q	Enable $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

(V_{CC}=5V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=0.8V or 2.0V					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−.1	V_{CC}−.1	V_{CC}−.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V0.8V or 2.0V					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay - P or Q to Output		19	30	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		13	22	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		13	20	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		10	18	ns

AC Electrical Characteristics V_{CC} = 5V ± 10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified.)

Symbol	Parameter	Condition	T_A = 25°C		74HCT T_A = -40°C to 85°C	54HCT T_A = -55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay - P or Q to Output		23	35	44	53	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		16	24	30	36	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		16	24	30	36	ns
t_{PLH}	Maximum Propagation Delay - Enable to Output		11	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		45				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC}$ and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HCU04/MM74HCU04 Hex Inverter

General Description

These inverters utilize microCMOS Technology, 3.5 micro silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

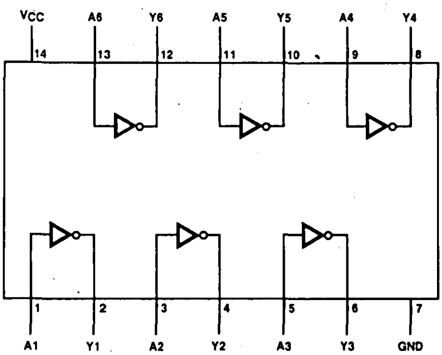
The MM54HCU04/MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns
- Fan out of 15 LS-TTL loads
- Quiescent power consumption: 10 μA maximum at room temperature
- Typical input current: 10^{-5} μA

Connection and Schematic Diagrams

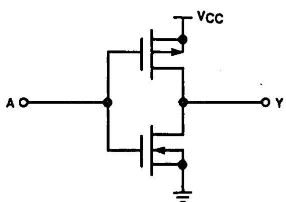
Dual-In-Line Package



TL/F/5296-1

TOP VIEW
MM54HCU04/MM74HCU04

54HCU04 (J) 74HCU04 (J,N)



TL/F/5296-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.7	1.7	1.7	V
			4.5V		3.6	3.6	3.6	V
			6.0V		4.8	4.8	4.8	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.8	0.8	0.8	V
			6.0V		1.1	1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.8	1.8	1.8	V
			4.5V	4.5	4.0	4.0	4.0	V
			6.0V	6.0	5.5	5.5	5.5	V
		V_{IN} = GND $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.2	0.2	0.2	V
			4.5V	0	0.5	0.5	0.5	V
			6.0V	0	0.5	0.5	0.5	V
		$V_{IN}=V_{CC}$ $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		7	13	ns

AC Electrical Characteristics

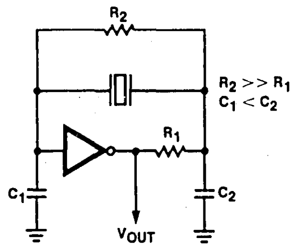
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	49	82	103	120	ns
			4.5V	9.9	16	21	24	ns
			6.0V	8.4	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		90				pF
C_{IN}	Maximum Input Capacitance			8	15	15	15	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

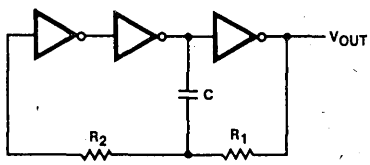
Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Typical Applications



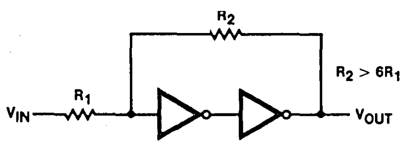
TL/F/5296-3

FIGURE 1. Crystal Oscillator



TL/F/5296-4

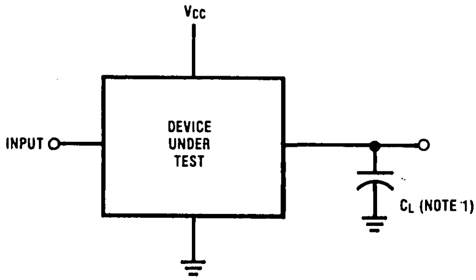
FIGURE 2. Stable RC Oscillator



TL/F/5296-5

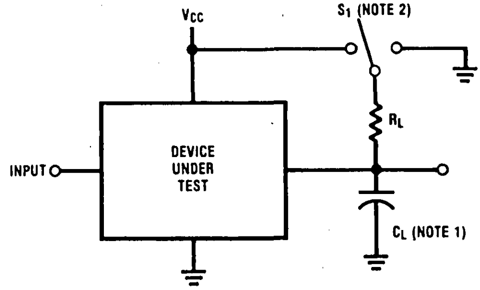
FIGURE 3. Schmitt Trigger

MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms



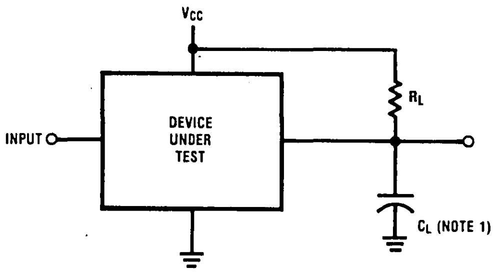
TL/F/5376-1

Test Circuit for Push Pull Outputs



TL/F/5376-2

Test Circuit for TRI-STATE Output Tests

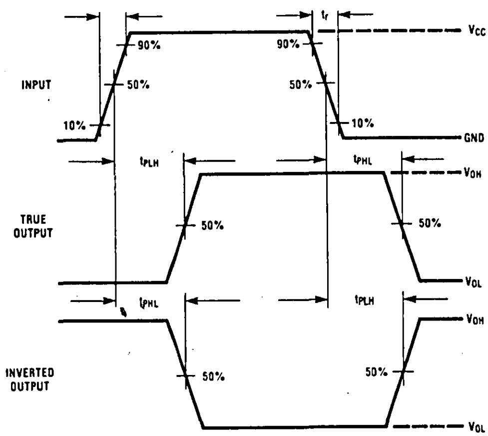


TL/F/5376-3

Test Circuit for Open Drain Outputs

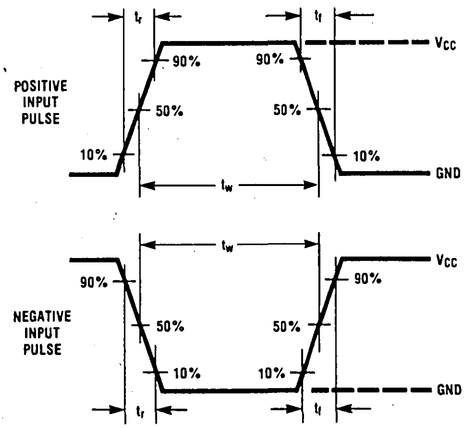
Note 1: C_L includes load and test jig capacitance.

Note 2: $S1 = V_{CC}$ for t_{PZL}, and t_{PLZ} measurements.
$S1 = Gnd$ for t_{PZH}, and t_{PHZ} measurements.



TL/F/5376-4

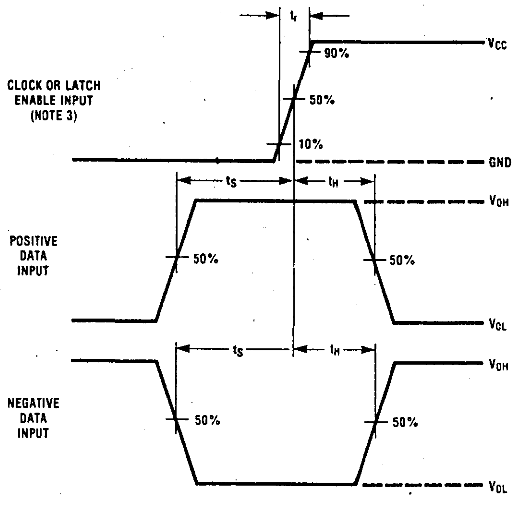
Propagation Delay Waveforms



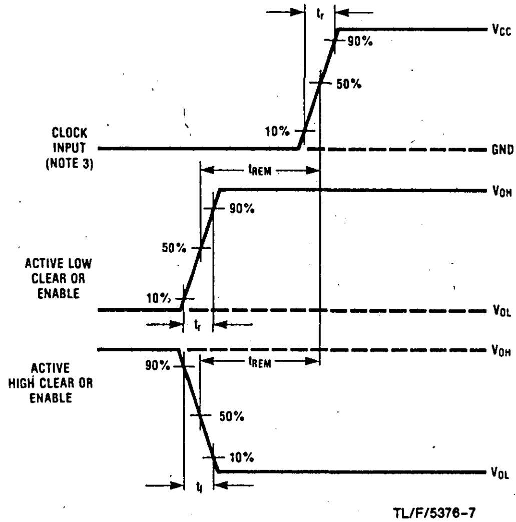
TL/F/5376-5

Input Pulse Width Waveforms

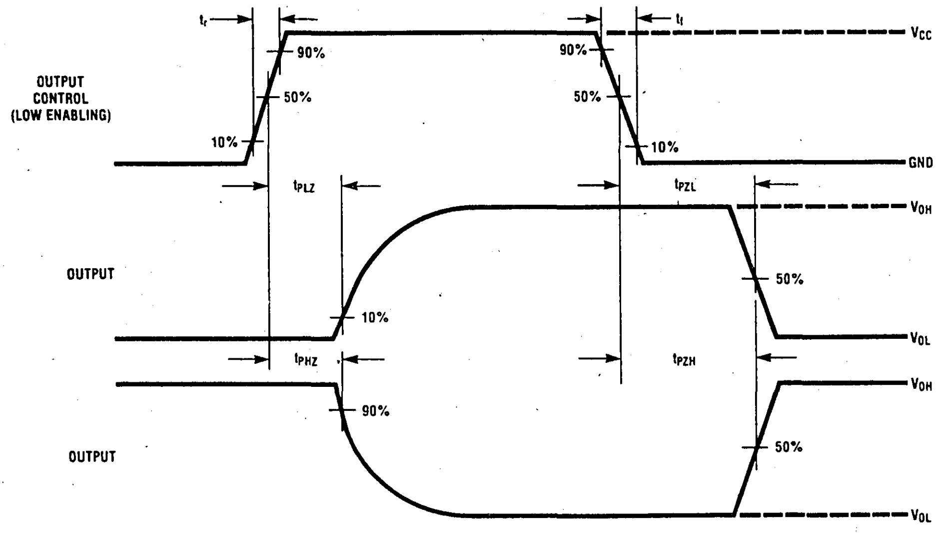
MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms (Continued)



Setup and Hold Time Waveforms



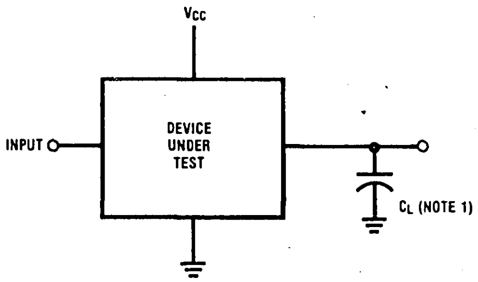
Removal Time Waveforms



TRI-STATE Output Enable and Disable Waveforms

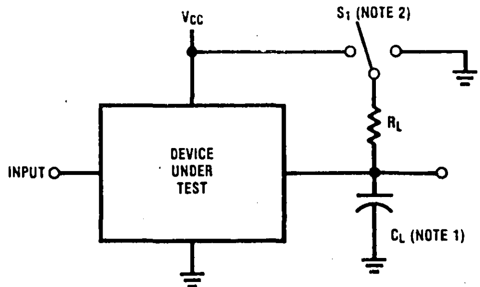
Note 3: Waveform for negative edge sensitive circuits will be inverted

MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms



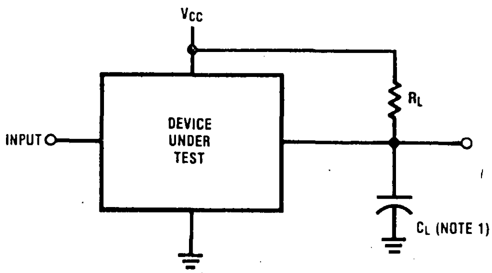
TL/F/5376-1

Test Circuit for Push Pull Outputs



TL/F/5376-2

Test Circuit for TRI-STATE Output Tests

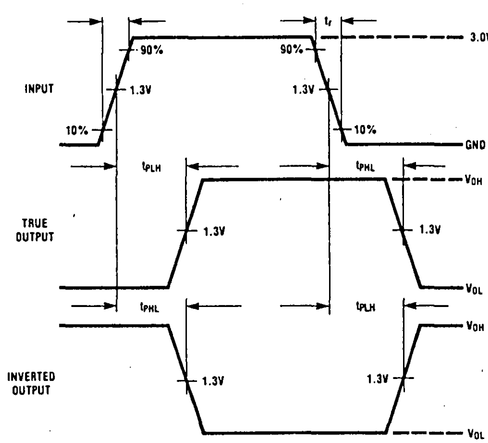


TL/F/5376-3

Test Circuit for Open Drain Outputs

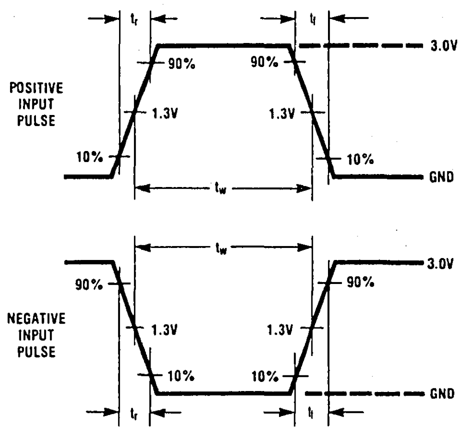
Note 1: C_L includes load and test jig capacitance.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.



TL/F/5376-9

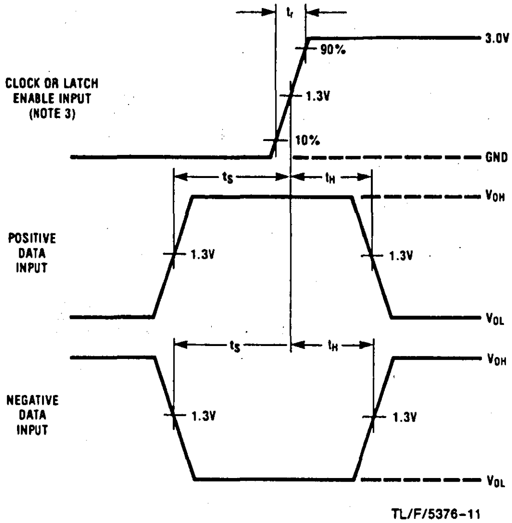
Propagation Delay Waveforms



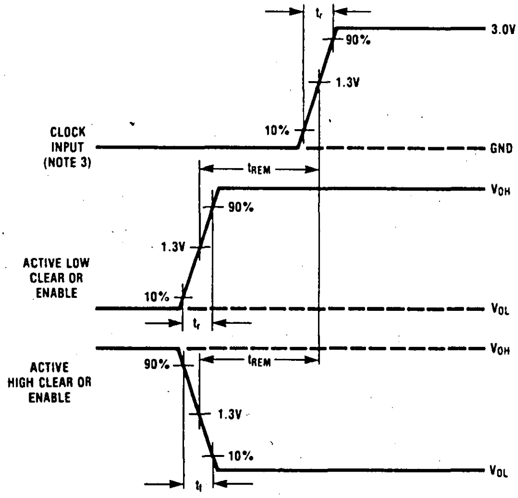
TL/F/5376-10

Input Pulse Width Waveforms

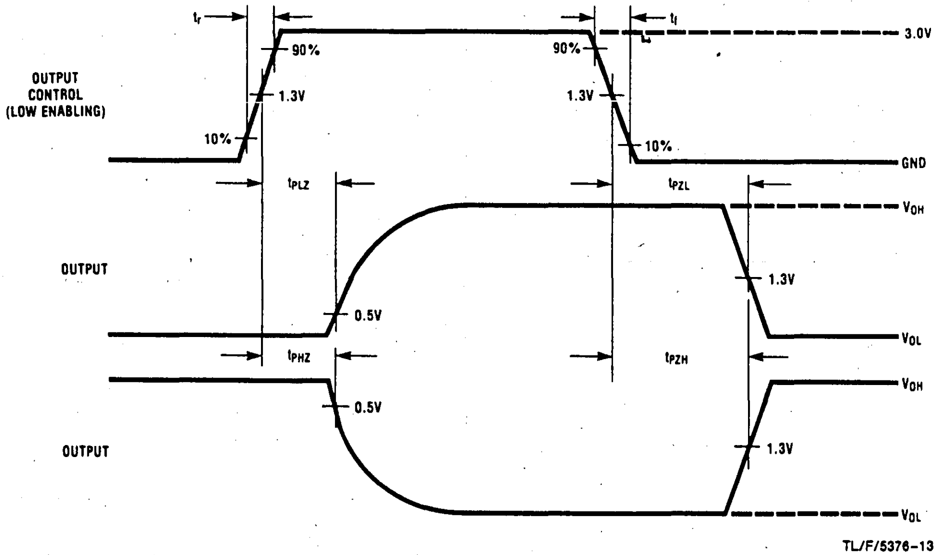
MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms (Continued)



Setup and Hold Time Waveforms



Removal Time Waveforms



TRI-STATE Output Enable and Disable Waveforms

Note 3: Waveform for negative edge sensitive circuits will be inverted

Section 2

Semi-Custom Circuits

2

Introduction

Gate arrays are very popular semi-custom IC products. They can be thought of as the next step in the evolution of complex chips.

In brief, a gate array is a geometric pattern of basic gates contained on one chip. It is possible to selectively interconnect these gates to form a complex function for customer-specific logic applications.

This concept originated a number of years ago in many computer houses. The more recent appearance of gate arrays in major new computer systems has attracted attention to this technique of providing digital circuits.

PRODUCING THE SYSTEM-ON-A-CHIP

Gate arrays take the industry one step closer to the complete system on a single silicon chip. The objective is to combine the logic of a large number of SSI and MSI packages (which would occupy a large part of a PC board) and squeeze all this logic onto a single gate array chip. Systems designers will therefore exchange logic chip catalogs for macrocell libraries, and PC board layouts for placement and routing of interconnects on a silicon wafer. Circuit design is finally returning to the systems houses.

Through the modern miracle of software, systems designers will convert their logic diagrams into the detailed information that is needed to make IC interconnection masks. The semiconductor manufacturer will then make these masks and pattern some existing, nearly finished wafers with this custom interconnect pattern.

Software-generated test tapes will verify product functionality, and these ICs will then be shipped to the customer—a cycle that is not much different from photographic film processing: a roll of film is sent in, and prints are returned.

There are many benefits that result from the use of gate arrays. One of the more important is the reduction in the time required to design a new system. Performance advantages also result because of higher levels of integration, yielding higher speed for the same power dissipation, or a reduction in power consumption. The smaller total number of external connections between components also increases system reliability.

DESIGNING GATE ARRAY PRODUCTS

The major events involved in designing a gate array are shown in *Figure 2-1.*

Taken in sequence, the steps are:

1. The entry (by the customer) of the logic design into a computer system via a graphic capture or a netlist (an alphanumeric format).
2. A logic simulation then ensures the proper functioning. During this phase, test programs are generated and fault-graded to ensure adequate detection of bad chips. The solution to this testing problem is a major part of the gate array design and often requires additional logic. To help solve this problem, special circuitry has been included in the base array design of National's larger array chips.
3. With a proper logic diagram (which also solves the testing requirements), the next step is the placement or location of the specific macrocells. This is followed by a routing program that interconnects the macros. Transient analysis programs can then show the timing to expect since the added capacitance loading of the actual interconnect lines is used.
4. From here, pattern generator (PG) tapes are made which allow the fabrication of the masks: 1st-layer metal, 2nd-layer metal, and the via mask for connection between the metal layers. These masks are then used to pattern your custom logic onto existing silicon wafers.
5. Finished parts are final tested and shipped, completing the design cycle.

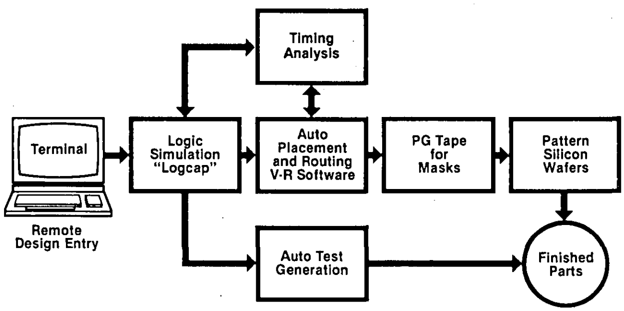


FIGURE 2-1. The Development System for Gate Arrays

PROVIDING NEW GATE ARRAY TECHNOLOGIES

National continues to develop new technologies for high-performance gate arrays and offers a dual-metal silicon-gate CMOS family, as well as a high-speed bipolar ECL family. The SCX series CMOS gate arrays have been in production in both 3-micron and 2-micron drawn geometries and provide typical gate delays of 2 ns and 1 ns, respectively. For applications demanding sub-nanosecond delays, the MCA series of ECL gate arrays is available and provides the ultimate in high-speed performance.

DESIGN AUTOMATION IS THE KEY TO SUCCESS

National's design automation tools start with a full complement of hardware macros, the basic building blocks from which a user can select functions to implement his logic. From these logic blocks come an ever increasing list of software macros. These are made up of hardware macros that have been pre-arranged and verified for 7400 series logic implementation.

All hardware and software macros are supported by a fully integrated CAE/CAD system that includes graphic workstation data entry, timing verification, logic simulation, fault grading, design verification, and 100% auto-place-and-route.

The present product offerings in CMOS gate arrays are listed in *Figure 2-2.*

Notice that the new 2 μm products have internal propagation delays of only 1 ns and can be operated at up to 110 MHz toggle frequencies. The largest array size contains 6090 equivalent 2-input gates.

THE USE OF NEWER PACKAGES

These new gate array products have large numbers of potential inputs and outputs to accommodate different design architectures. National has developed new packages for these devices such as the 124-pin grid array (PGA) shown in *Figure 2-3.*

Specific array designs, however, can be done in a wide variety of package options, including leaded chip carriers, plastic and ceramic leadless chip carriers, and standard DIPs. Lead counts range from 28 to 172 pins.

The customer offerings in semi-custom will be expanded to include cell arrays and functional block arrays. This is a very dynamic market—please contact your National sales representative for the current status of our semi-custom circuit capability.

2

Device (Technology)	2-Input Eq. Gates	Internal t_{PD} (ns)	Toggle Frequency (MHz)
SCX6306 (3 μm)	648	2.0	70
SCX6312 (3 μm)	1260	2.0	70
SCX6324 (3 μm)	2385	2.0	70
SCX6348 (3 μm)	4860	2.0	70
SCX6360 (3 μm)	6090*	2.0	70
SCX6206 (2 μm)	648	1.0	110
SCX6212 (2 μm)	1260	1.0	110
SCX6224 (2 μm)	2385	1.0	110
SCX6248 (2 μm)	4860	1.0	110
SCX6260 (2 μm)	6090*	1.0	110

*Plus 2500 additional gates for on-chip self test.

FIGURE 2-2. Current CMOS Gate Arrays

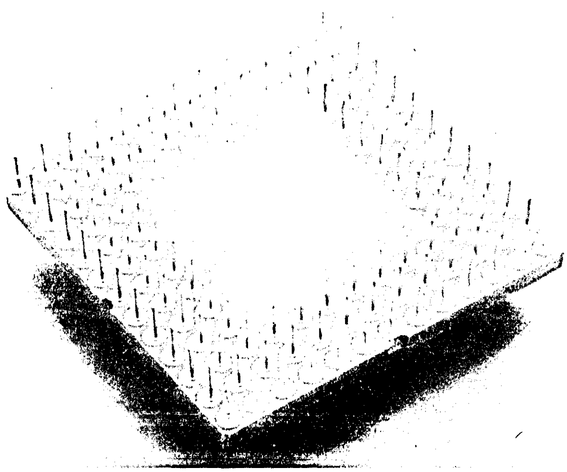


FIGURE 2-3. A 124-Pin Grid Array Package for the 2.4k Array

SCX Series of 2-Micron and 3-Micron CMOS Gate Arrays

Technology	Device	2-Input Eq. Gates	Gate Delay (ns)†	Toggle Freq. (MHz)‡	Input Pads	I/O Pads
3μ	6306	648	2	70	—	37
	6312	1260	2	70	17	42
	6324	2385	2	70	55	56
	6325	2430	2	70	12	76
	6348	4860	2	70	53	54
	6360*	6090	2	70	66	88
2μ	6212	1260	1	110	17	42
	6224	2385	1	110	55	56
	6225	2430	1	110	12	76
	6248	4860	1	110	53	54
	6260*	6090	1	110	66	88

*advanced gate array architecture with on-chip test facility
†typical 2-input gates
‡assumes fanout of 3 for typical D flip/flop

Features

- Latch-up proof, state-of-the-art 3μ/2μ dual-metal silicon-gate microCMOS technology
- Ultra-high performance—2 ns/1 ns typical gate delays
- High density—to the equivalent of 6000 2-input gates
- Self-test capability—available on 6000-gate devices
- Advanced high-density packages—up to 172 pins
- Complete hardware/software macrocell libraries
- 100% auto-place-and-route—supported by a fully integrated design automation system
- Full 883B screening over military temperature range

National Semiconductor

microCMOS

SCX 6324 microCMOS 2.4k Gate Array NS000U Option User's Note

Introduction

The SCX 6324 CMOS 2.4k Gate Array is fabricated on a 3-micron, dual metal, N- Well, 5V microCMOS Process which typically provides internal propagation delay of 2ns for a 2-input NAND gate.

The Test Chip Option of the SCX 6324A (NS000U option) contains all macro cells currently available for design (as of October, 1982). It is intended for engineering evaluation and as a sampling part for AC performance demonstration.

A schematic drawing follows and a test setup scheme is shown on page 2-9.

Test Set Up

The Test Chip option of the SCX6324 contains circuitry for engineering evaluation of macro functions that are currently available. Some circuits may have unprotected inputs/outputs, thus evaluations should be done under a controlled environment. Users are advised to use only those circuits that are mentioned in this note. Connections to any other pins may cause damage to the device.

A test set-up scheme is suggested in *Figure 4* for reference, together with a selection table for each macro given in Table 1.

Input Pull-Up: All inputs (except pins 87 and 88) are provided with internal pull-up; grounded inputs will source approximately 8μA each at 25°C and $V_{DD} = 5V$.

AC Performance of a Macro: The outputs of all macros are fed to the external pins via a MUX and an output buffer, so their exact AC performance should be found by subtracting the delay due to these MUXs and buffers. Pins 59 and 55 (labelled as "input signal reference") can be used to determine this extra delay.

Internal TRI-STATE® Macro: S9 and S10 are TRI-STATE buffers intended for use within the array. They are brought out to the external pin in this Test Chip option. A scope probe with low loading should be used to give better approximation of their performance. A low capacitance FET probe is recommended. It is unlikely that much less than 8–10pF of parasitic loading can be achieved. (See Note 2.)

Unprotected I/O Pins: There are I/O pins in this option that are not protected. Extreme care should be exercised in using them to avoid latch-up, oxide rupture, etc.

NOTE: This document also applies to the 2-micron SCX 6224 test chip in terms of circuit configuration and pin arrangement.

Metal Loading Evaluation: Three strings of inverters are included in this Test Chip for the metal loading evaluation. One is without any extra metal loading except for interconnect; the other two are loaded with 200-mil run of either metal 1 or metal 2 at each inverter stage. Refer to the schematic drawing for details. (See Note 1.)

Notes:

1. Other than on these gate strings (see "Metal Loading Evaluation" above), no additional loading capacitance is added. All other macros are generally connected with a minimal amount of interconnect—the amount of parasitic capacitance incurred is not shown.
2. All macros intended for internal array use, but brought directly to output pins, are *not* protected against latch-up. (All true output buffer options of the I/O are fully protected.)

On-Chip Test Circuit

All options of the SCX6324 are provided with on-chip test circuitry, at the cost of a single input pin, to create TEST MODE. With this pin active (LOW), two additional pre-defined inputs are jointly employed to force all outputs to HIGH, LOW or Hi-Z states and thus reduce test time in gathering output parametrics. These two pins further function as conventional inputs (either TTL or CMOS when in TEST MODE, HIGH) with no performance penalty apparent to the user.

TEST MODE CONTROL (TMC): A LOW at this input will activate the test circuitry. All output buffers are to be driven by TEST DATA (DT) and TRI-STATE TEST CONTROL (TSTC) pins.

TRI-STATE TEST CONTROL (TSTC): A HIGH at this input, together with TMC low, puts all TRI-STATE output buffers to Hi-Z state.

TEST DATA (DT): Input to this pin, with TMC low, forces all outputs to either HIGH or LOW.

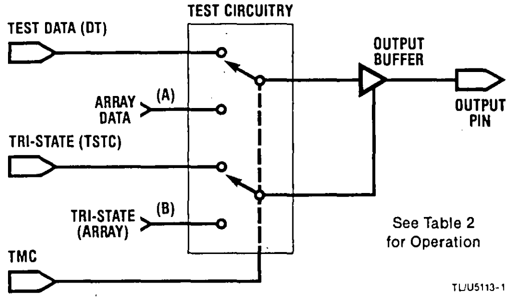


FIGURE 1

Table 1. Macro Selection (See Test Setup)

Macro Type	Macro Function	Macro Output	SEL "S"	Input Signal	Output Pin Number
S1	2 I/P NAND	0	ON	A = D0, B = D1	60
S2	3 I/P NAND	0	ON	A = D0, B = D1, C = D2	58
S3	2 I/P NAND w/QB	0	ON	A = D0, B = D1	54 for C
S3	2 I/P NAND w/QB	1	OFF	A = D0, B = D1	54 for D
S4	2 I/P NOR	0	ON	A = D0, B = D1	107
S5	3 I/P NOR	0	ON	A = D0, B = D1, C = D2	109
S6	2 I/P NOR w/QB	0	ON	A = D0, B = D1	115 for C
S6	2 I/P NOR w/QB	1	OFF	A = D0, B = D1	115 for D
S7	Clock Buffer	0	ON	A = D0	31
S8	Inverter	0	ON	A = D0	33
S9	TRI-STATE Buffer		N/A	A = D0, EB = D1	36
S10	TRI-STATE Buffer		N/A	A = D0, E = D1	35
S11	2 I/P Exclusive-OR	1	OFF	A = D0, B = D1	108
S12	NAND RS Latch	0	ON	SB = D0, RB = D1	37 for Q
S12	NAND RS Latch	1	OFF	SB = D0, RB = D1	37 for QB
S13	NOR RS Latch	0	ON	R = D0, S = D1	39 for Q
S13	NOR RS Latch	1	OFF	R = D0, S = D1	39 for QB
S14	2-2 OR-NAND	0	ON	A = D0, B = D1, C = D2, D = D3	47 for E
S14	2-2 OR-NAND	1	OFF	A = D0, B = D1, C = D2, D = D3	47 for F
S15	2-2 AND-NOR	0	ON	A = D0, B = D1, C = D2, D = D3	120 for E
S15	2-2 AND-NOR	1	OFF	A = D0, B = D1, C = D2, D = D3	120 for F
S16	2:1 MUX	0	ON	A = D0	59
S16	2:1 MUX	1	OFF	B = D0	55
D1	4 I/P NAND	0	ON	A = D0, B = D1, C = D2, D = D3	56
D2	5 I/P NAND	0	ON	A = D0, B = D1, C = D2, D = D3, E = D4	57
D3	3 I/P NAND w/QB	0	ON	A = D0, B = D1, C = D2	52 for D
D3	3 I/P NAND w/QB	1	OFF	A = D0, B = D1, C = D2	52 for E
D4	4 I/P NOR	0	ON	A = D0, B = D1, C = D2, D = D3	113
D5	5 I/P NOR	0	ON	A = D0, B = D1, C = D2, D = D3, E = D4	112
D6	3 I/P NOR w/QB	0	ON	A = D0, B = D1, C = D2	117 for D
D6	3 I/P NOR w/QB	1	OFF	A = D0, B = D1, C = D2	117 for E
D9	D Flip-Flop	0	ON	CK = D0, D = D1	43 for Q
D9	D Flip-Flop	1	OFF	CK = D0, D = D1	43 for QB
T1	D Flip-Flop w/S,R	0	ON	CK = D0, D = D1, SB = D2, RB = D3	42 for Q
T1	D Flip-Flop w/S,R	1	OFF	CK = D0, D = D1, SB = D2, RB = D3	42 for QB

Table 2. On-Chip Test Circuit Operation

TMC	TSTC	DT	OUTPUT
H	X	X	Normal Operation
L	H	X	Hi-Z (TRI-STATE Buffers Only)
L	L	H	L
L	L	L	H

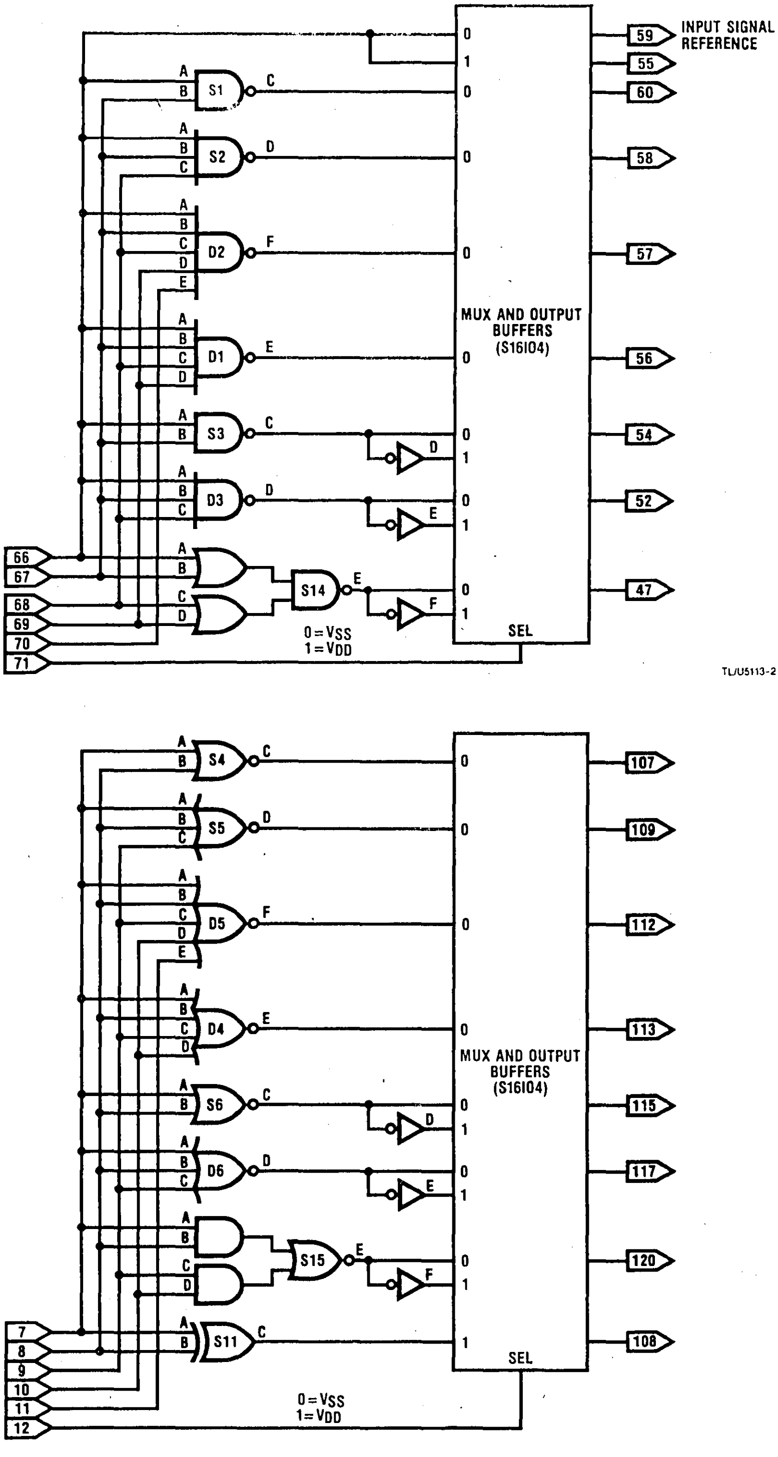
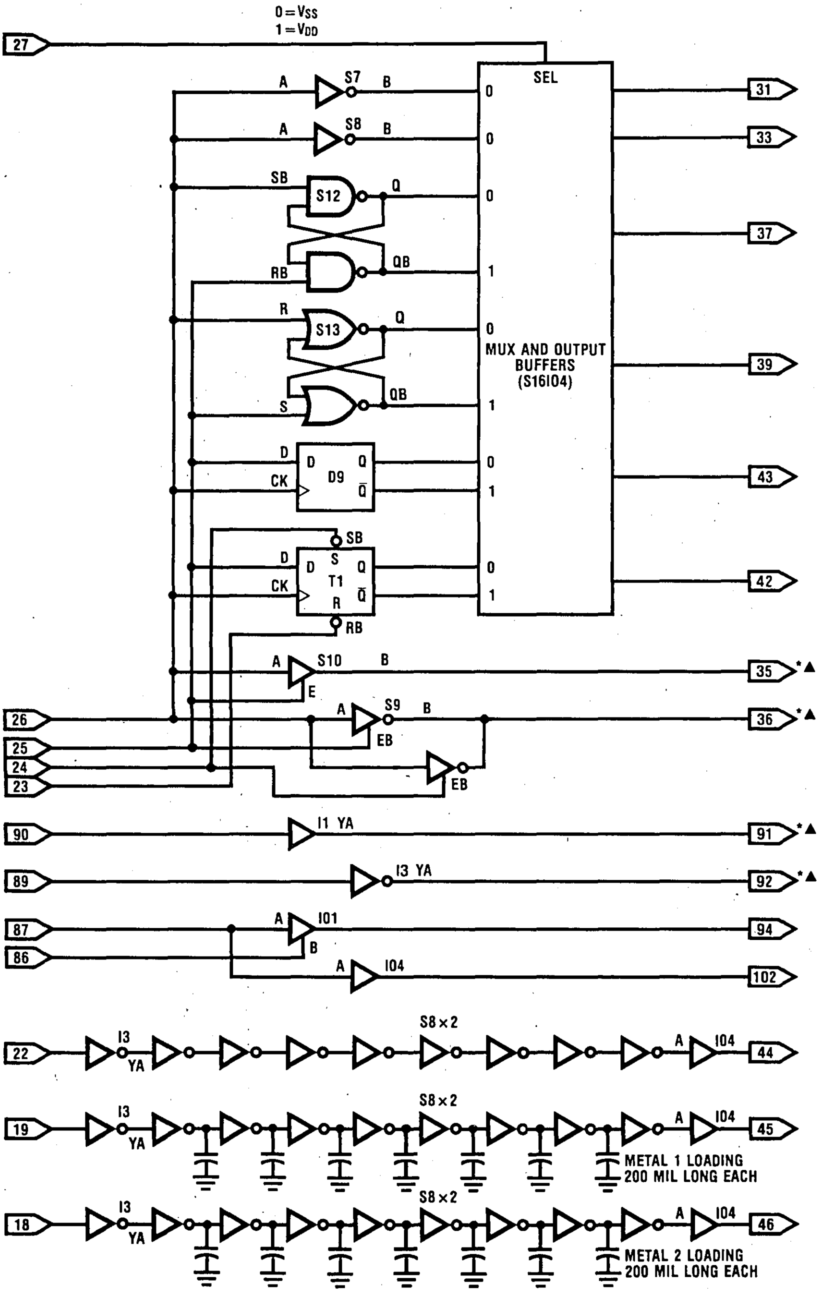

INPUT SIGNAL REFERENCE
MUX AND OUTPUT BUFFERS (S16104)
SEL
0 = VSS
1 = VDD
S1
S2
D2
D1
S3
D3
S14
59
55
60
58
57
56
54
52
47
66
67
68
69
70
71
TL/U5113-2
S4
S5
D5
D4
S6
D6
S15
S11
107
109
112
113
115
117
120
108
7
8
9
10
11
12
TL/U5113-3

FIGURE 2



Notes:

*: I/O D N: Do not have latch-up protection

▲: Not able to drive large load. See Note 2.

TL/U5113-4

FIGURE 3

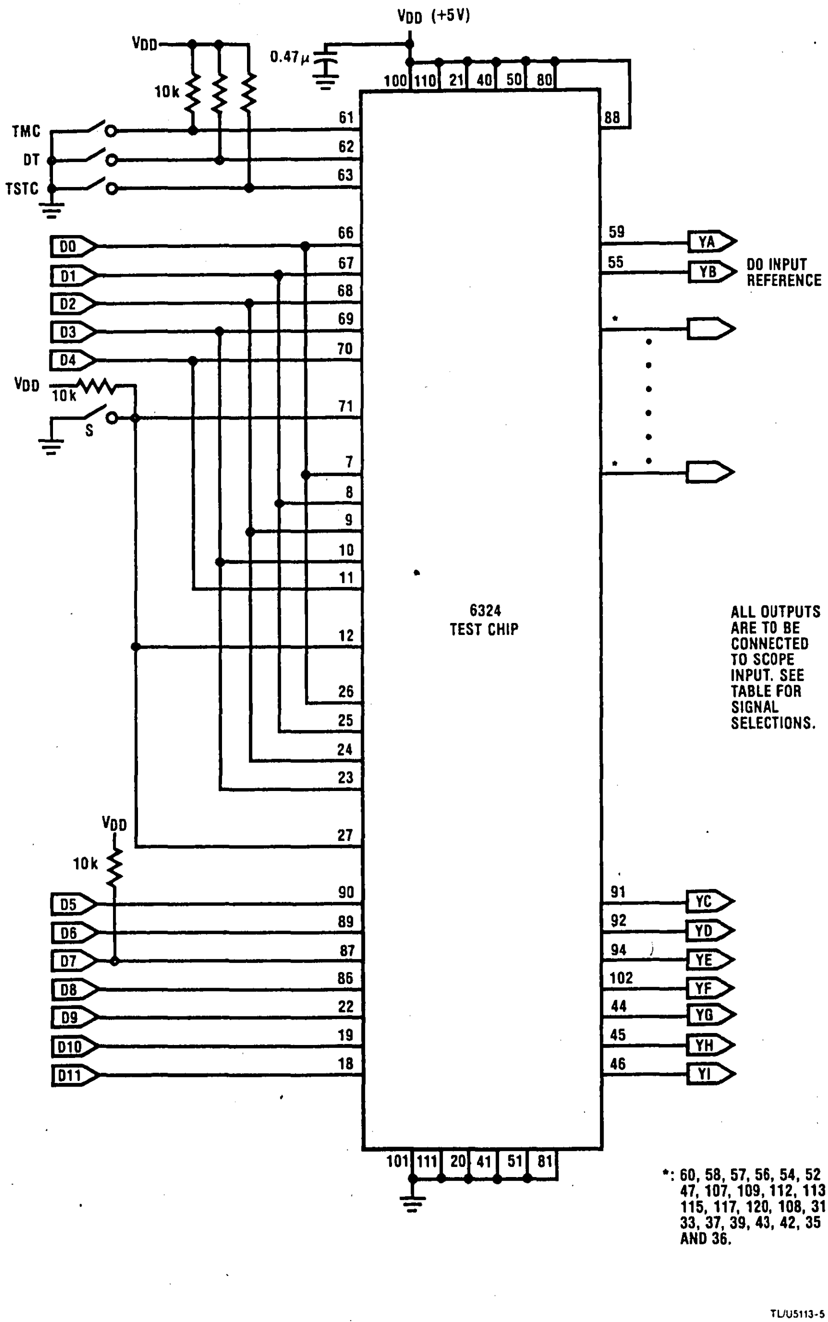
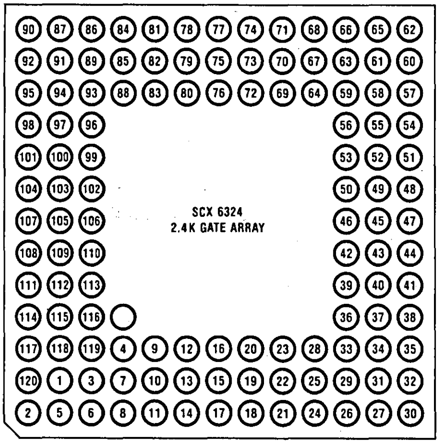

VDD (+5V)
VDD
0.47μ
10k
TMC
DT
TSTC
100 110 21 40 50 80
88
61
62
63
66
67
68
69
70
71
D0
D1
D2
D3
D4
VDD
10k
S
59
55
YA
YB
D0 INPUT REFERENCE
7
8
9
10
11
12
6324
TEST CHIP
ALL OUTPUTS ARE TO BE CONNECTED TO SCOPE INPUT. SEE TABLE FOR SIGNAL SELECTIONS.
26
25
24
23
VDD
27
10k
D5
D6
D7
D8
D9
D10
D11
90
89
87
86
22
19
18
91
92
94
102
44
45
46
YC
YD
YE
YF
YG
YH
YI
101 111 20 41 51 81
*: 60, 58, 57, 56, 54, 52 47, 107, 109, 112, 113 115, 117, 120, 108, 31 33, 37, 39, 43, 42, 35 AND 36.
TL/U5113-5

FIGURE 4

120-PIN MATRIX



TOP VIEW

TL/U5113-6

Order Information
SCX6324 NS000/U5

SCX CMOS Gate Array Family Application Guide

2

TABLE OF CONTENTS

1.0 GENERAL DESCRIPTION

National Semiconductor's CMOS gate array families utilize a dual layer metal technology (microCMOS) to achieve operating speeds similar to Schottky-TTL with the inherent lower power consumption of standard CMOS integrated circuits. The families are available in 3-micron (as drawn) and 2-micron process technology. The range of complexity is currently from 600 to 6000 gates. The gates are arranged in cells. Each cell has the equivalent of three 2-input NAND or NOR gates. All outputs have the ability to drive 10 LSTTL loads. All inputs have high noise immunity and are protected from static discharge.

National Semiconductor supports gate array designs with a variety of user/vendor interfaces. This ranges from producing arrays from the user's schematic to accepting databases for mask generation. A large dedicated staff of gate array professionals is available to help the user determine the most efficient and cost effective way to interface on any given design.

The design automation tools include workstation or text file entry (for schematic capture), logic and timing verifiers to substantiate the actual design, fault grading analysis to gauge testability and a large selection of macros (hardware and software) to speed and simplify the design.

2.0 PRODUCT FEATURES

- 2.0 ns internal propagation delay (3-micron)
- 1.0 ns internal propagation delay (2-micron)
- CMOS power dissipation
- All inputs and I/Os protected from over-voltage and latch-up
- LSTTL drive capability
- TTL/CMOS inputs and I/Os (programmable)
- Internal test circuitry
- Full design automation support
  - —Schematic capture
  - —Logic simulator with timing information
  - —Fault grading
  - —>80% cell utilization
  - —100% automatic placement and routing
- Extensive hardware and software macro library
- Multiple power rail pin connections
- Multiple packaging options in ceramic, plastic, leaded and leadless
- Pin counts to 124
- Full military specifications
- Alternately sourced

2.1 microCMOS Process and Circuit Personalization

The microCMOS process developed by National is based on P-type starting material, N-well technology and oxide isolation. After the basic transistors are formed (in their respective cells), two separate layers of metalization (M1 and M2) are placed on the wafers.

The processing steps and tooling requirements for all the wafers up to the metal layers are common and fixed. Circuit patterns—called "options"—are defined by the two metal layers and the VIAs. In this way, the user's design (or circuit personality) is imposed on the wafer.

All SCX gate arrays in the family use the same basic internal cell. There are eight pairs of N and P-type MOS transistors in each cell (see *Figure 2*). The power and ground lines (V_{DD} and V_{SS} buses, respectively) run up and down the cell. This cell is repeated in all four directions to form columns and rows in the core of the array. The structure of the internal core is optimized to the size of each family member.

National Semiconductor maintains an inventory of gate array wafers fabricated up to but before metalization. As the customer's options are designed and the last three patterns finalized, wafers are taken out of inventory and the fabrication process completed for the metal layers.

In this way, National Semiconductor can provide gate array users with quick turn-around cost effective designs while maintaining the quality, reliability and production control of an in-house (5-inch) wafer fab line.

2.2 Gate Array Basic Cell

Figure 1 and *Figure 2* show a microCMOS cross section and the basic internal cell respectively. The geometries are not drawn to scale and the exact topology has been modified for illustration purposes.

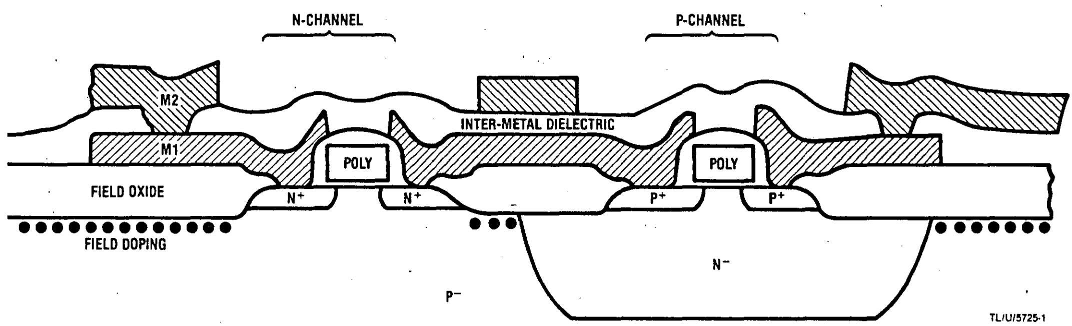


FIGURE 1. Cross Section

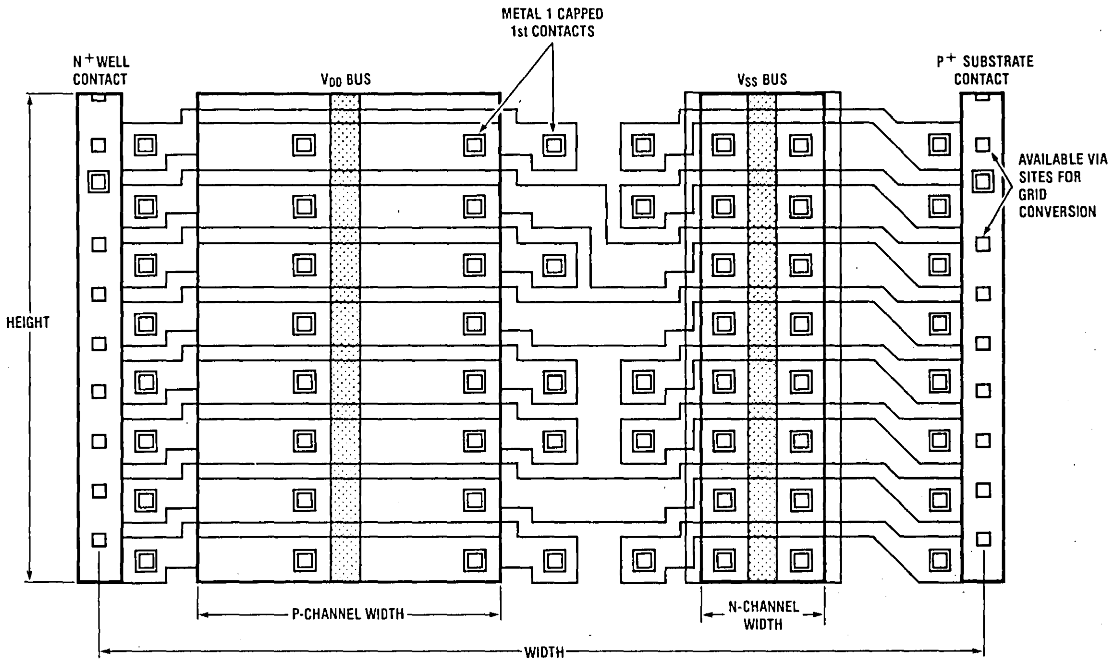


FIGURE 2. Cell

2.3 Power Dissipation

An outstanding feature of microCMOS circuits is their low power dissipation. CMOS circuits draw electrical current for basically two reasons:

(1) During transition from a logic "0" to a logic "1" or vice versa, there exists a finite time when the P-channel and N-channel devices associated with the logic element are both conducting. The CMOS circuit consumes power during this transition.

(2) When signals change state, the distributed capacitance in the circuit (and its load) need to be either charged or discharged. The electrical current required for this purpose increases power consumption.

Thus, power dissipation is dependent on operating voltage, nodal capacitance and the frequency of circuit operation. Mathematically speaking:

$$P_O = CV^2F$$

For estimation purposes, the value of:

35 μW/gate/MHz per gate equivalent can be used for elements within the array.

700 μW/MHz/output buffer at 15 pF load or 1500 μW/MHz/output at 50 pF load, can be used for the output buffers.

Power dissipation in a CMOS array is typically dominated by output buffers driving large capacitive loads.

Figure 3 will help in estimating power consumption in a particular design.

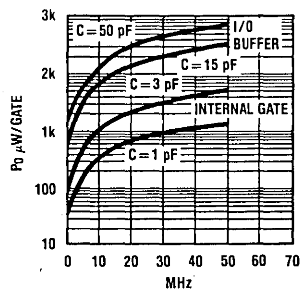


FIGURE 3. Power Consumption vs Frequency

2.4 Absolute Maximum Ratings

Exceeding the following absolute maximum ratings may result in permanent damage to the device.

Supply Voltage	$-0.5V$ to $7V$
Input or Output Voltage	$-0.5V$ to $V_{DD}+0.5V$
Storage Temperature	$-65°C$ to $150°C$
Power Dissipation (Package Dependent)	1W
Lead Temperature (Soldering, 10 seconds)	300°C

2.5 Recommended Operating Conditions

	Min	Max	Units
V_{DD}, Supply Voltage	2	6	V
V_I, V_O, Input or Output Voltage	V_{SS}	V_{DD}	V
I_O, High or Low Level Output Current	0	±25	mA
I_{DD}, V_{DD} or V_{SS} Current per Pad	0	±25	mA
T_A, Ambient Operating Temperature	−40	+85	°C

2.6 DC Electrical Characteristics

$V_{DD}=5V \pm 10\%$, min/max limits apply over recommended operating temperature range unless otherwise specified.

Symbol	Parameter	Min	Max	Units
V_{IH}	High Level Input Voltage at $V_O=0.1V$ or $V_{DD}-0.1V$, $I_O=20\ \mu A$	$0.7\ V_{DD}$		V
V_{IL}	Low Level Input Voltage at $V_O=0.5V$ or $V_{DD}-0.1V$, $I_O=20\ \mu A$		$0.2\ V_{DD}$	V
V_{OH}	High Level Output Voltage at $V_I=V_{DD}$ or GND, $I_O=20\ \mu A$	$V_{DD}-0.05$		V
V_{OL}	Low Level Output Voltage at $V_I=V_{DD}$ or GND, $I_O=20\ \mu A$		0.05	V
I_{OH}	High Level Output Current at $V_I=V_{DD}$ or GND, $V_O=V_{DD}-0.8V$	−4		mA
I_{OL}	Low Level Output Current at $V_I=V_{DD}$ or GND, $V_O=0.4V$	4		mA
V_{IH} TTL	Minimum High Level TTL Input Voltage (for TTL Input Option) at $V_O=0.5V$ or $V_{DD}-0.1V$, $I_O=20\ \mu A$	2		V
V_{IL} TTL	Maximum Low Level TTL Input Voltage (for TTL Input Option) at $V_O=0.5V$ or $V_{DD}-0.1V$, $I_O=20\ \mu A$		0.8	V
I_I	Input Current (Without Pull-Up Resistor) at $V_I=V_{DD}$ or GND		±1	μA
I_{CC}	Supply Current at $V_I=V_{DD}$ or GND, $T_A=25°C$		100	μA

2.7 AC Electrical Characteristics $V_{DD}=5V$, $T_A=25°C$, 3μ process.

Symbol	Parameter	Min	Max	Units
t_{PLH} t_{PHL}	Output Buffer (Non-Inverting, non-TRI-STATE®) $t_r=t_f=5$ ns, 0V–5V $C_L=15$ pF	2.6 2.4	6.1 5.7	ns ns
t_{PLH} t_{PHL}	Input Buffer (TTL Type, Non-Inverting) at $t_r=t_f=5$ ns, 0V–3V $C_L=1$ pF	2.0 2.5	4.78 5.94	ns ns
t_{PLH} t_{PHL}	Input Buffer (CMOS Type, Inverting) at $t_r=t_f=5$ ns, 0V–5V $C_L=1$ pF	1.3 0.85	3.0 2.0	ns ns
t_{PLH} t_{PHL} t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output TRI-STATE (Non-Inverting) at $t_r=t_f=5$ ns 0V–5V $C_L=50$ pF $R_L=1\ k\Omega$ Delays Measured at 50% Point Between Start and Target Voltage	4.5 4.7 4.6 4.2 3.5 3.5	10.4 10.9 10.7 9.8 8.1 8.1	ns ns ns ns ns ns ns
t_{PLH} t_{PHL} t_{PHL} t_{PLH}	Internal 2-Input NAND at $t_r=t_f=5$ ns, 0V–5V Load Equivalent to Fan-Out of 3 and 100 mils of Interconnect As Above with $C_L=0$ pF	1.4 1.8 1.5 1.5	3.3 4.1 1.2 1.2	ns ns ns ns

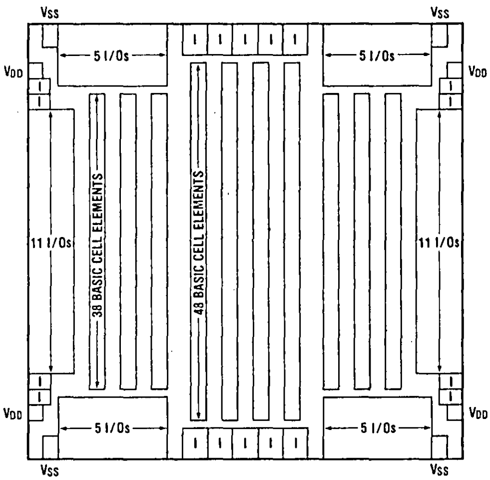
3.0 TOPOLOGY AND ROUTING RESOURCE DISTRIBUTION

The specific topology and routing resource distribution have been tailored for each family member. Architectural considerations include the ratio of inputs and I/Os to total cell count, power consumption and package inductance to power pins (for simultaneous switching outputs) and routing resources consistent with automatic place and route software. Internal cell utilizations of greater than 80% can be expected.

Individual topologies and a family summary follow.

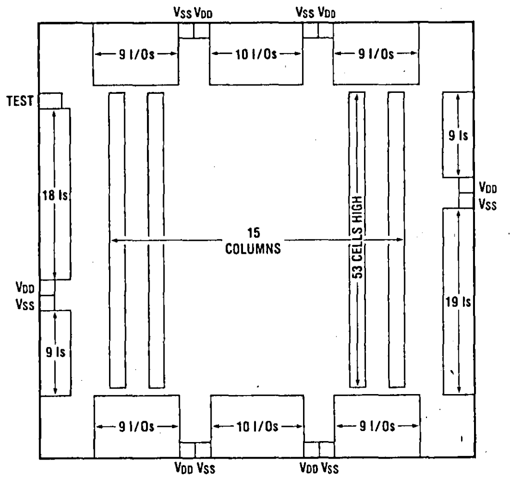
2

1.2k



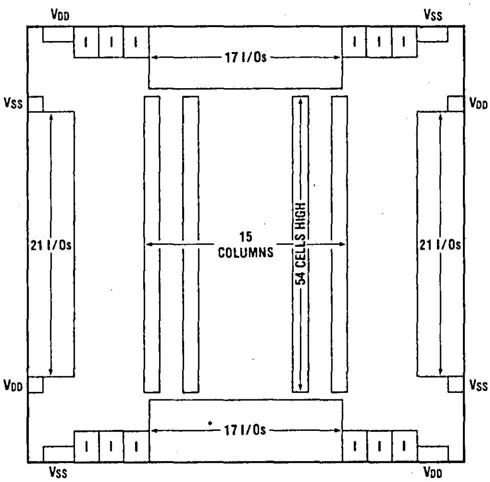
TL/U/5725-3

2.4k



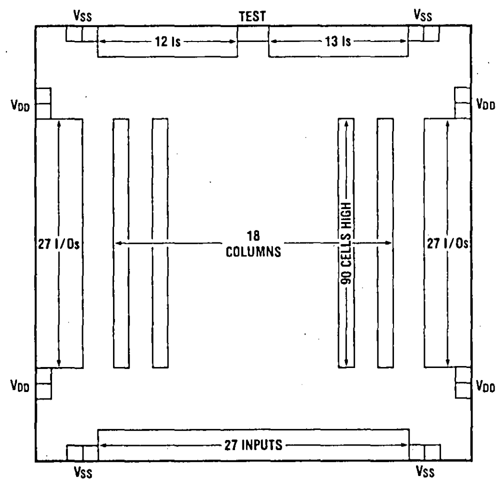
TL/U/5725-4

2.5k



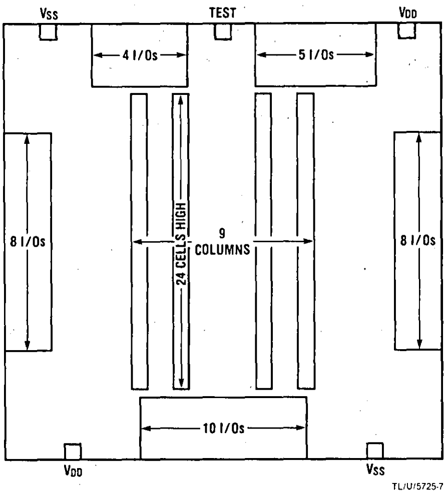
TL/U/5725-5

4.8k



TL/U/5725-6

600



Array Name	Internal Cells	Input Cells (Note 2)	I/O Cells	Total Pins (Note 1)	V_{DD} Pins	V_{SS} Pins
SCX6306	216	0	37	41	2	2
SCX6312	420	17	42	68	4	4
SCX6324	795	55	56	124	6	6
SCX6325	810	12	76	100	6	6
SCX6348	1620	53	54	124	8	8

Note 1: One of the pins is permanently set aside for testing purposes.

Note 2: Input and I/O cells are not considered part of the internal cell count.

4.0 ON-CHIP TEST CIRCUITRY

Each of the SCX gate arrays is provided with dedicated on-chip test circuitry. This circuitry forces all the outputs to specific states to facilitate output parametric testing. These parametric tests include leakage and current sourcing/sinking measurements on all output pins.

The on-chip test circuitry is enabled by a dedicated test mode control (TMC) pin. This pin is set aside for testing and cannot be used for any other purpose. A low at this input will activate the on-chip test circuitry. When the on-chip test circuitry is activated, the states of all outputs are determined by two other inputs; these are TRI-STATE test control (TSTC) and data test (DT). The TSTC and DT can share input pins with the user's design. They are only active when the TMC is enabled. The TSTC input has precedence over the DT input.

The TMC input is active for the following discussion.

When the TSTC input is active, all the output buffers are put into a high impedance mode. When TSTC is not active, the states of the output buffers are determined by the DT input. These two inputs can be assigned to any of the input pins. However, depending on the type of the input macro used for these two inputs, the outputs can have quite different states. This is because macros may have inverting or non-inverting inputs.

ON-CHIP TEST CIRCUITRY TRUTH TABLE

TMC	DT	TSTC	Output
0	X	Active	TRI-STATE
0	Non-Active	Non-Active	1
0	Active	Non-Active	0

DEFINITION OF TEST INPUT STATES

	Non-Inverting Macros	Inverting Macros
Non-Active	0	1
Active	1	0

5.0 MACROS

Three types of macros are available for designers to use: hardware macros, software macros (National Semiconductor standard library), and user generated software macros.

5.1 Hardware Macros

The SCX family of gate arrays offers an extensive library of hardware macros. Each macro has been fully characterized and functionally proven. The designer can select those macros that most efficiently implement the design. The electrical performance of the macros is characterized at two sets of conditions: best and worst-case. Under each set of conditions, the output loading is specified at 0 pF and 1.0 pF. The 1.0 pF load is equivalent to a fan-out of 3 and includes 100 mils length of metal interconnect. A single input load is equivalent to 0.17 pF and is defined as a load factor of 1.

National Semiconductor has very tight wafer fabrication guidelines. However, process parameters still do vary from wafer-to-wafer, lot-to-lot. The electrical specifications of the macros take into account such variations.

The logic macros are categorized by the number of array cells that each occupies. The prefix of the macro identifies the category.

Prefix	No. of Cells Occupied
S	1
D	2
T	3
Q	4
F	5
H	6

Category	Description
C001 (S1)	Triple 2-Input NAND Gate
C002 (S2)	Dual 3-Input NAND Gate
C003 (S3)	Dual 2-Input NAND/AND
C004 (S4)	Triple 2-Input NOR Gate
C005 (S5)	Dual 3-Input NOR Gate
C006 (S6)	Dual 2-Input NOR/OR
C007 (S7)	Triple Inverter/Clock Buffer
C008 (S8)	Quad Inverter
C009 (S9)	Dual TRI-STATE Inverting Buffer
C010 (S10)	Single Non-Inverting TRI-STATE Buffer
C011 (S11)	Single 2-Input Exclusive-OR
C012 (S12)	NAND R/S Latch with 2-Input NAND Gate
C013 (S13)	NOR R/S Latch with 2-Input NOR Gate
C014 (S14)	2-Input 2-Wide OR-NAND with Complement
C015 (S15)	2-Input 2-Wide AND-NOR with Complement
C016 (S16)	2-to-1 Multiplexer with Single Control Input
C049 (S18)	2-2 Buffer
C044 (S19)	Triple Inverter Buffer
C043 (S20)	Quadruple Inverter Buffer
C048 (S21)	Single 2-Input Exclusive NOR
C045 (S22)	1-3 Buffer
C061 (S23)	3-1 Buffer
C025 (S24)	Schmitt Trigger
C017 (D1)	Triple 4-Input NAND
C018 (D2)	Single 5-Input NAND
C019 (D3)	Triple 3-Input NAND/AND Complement
C020 (D4)	Triple 4-Input NOR
C021 (D5)	Single 5-Input NOR
C022 (D6)	Triple 3-Input NOR with Complement
C027 (D7)	Triple NAND Latch
C031 (D8)	Triple NOR Latch
C023 (D9)	D Flip-Flop
C047 (D10)	3-Input Exclusive OR
C062 (D11)	D-Latch with Set/Reset
C026 (D12)	1-Bit Transparent D-Latch with Reset and Enable
C024 (T1)	D-Type Flip-Flop with Inverted Set/Reset Inputs
C046 (T2)	4-Input Exclusive OR
C051 (T3)	D-Type Flip-Flop with Set/Reset Master Slave
C028 (T4)	4-to-1 Multiplexer with Inverted Enable Input
C029 (T5)	4-to-1 Multiplexer with Complement Output
C030 (T6)	4-Bit Parity Checker with Even-Odd Input
C032 (T7)	1-Bit Full Adder
C063 (Q1)	Multiplexed D Flip-Flop with Master-Slave Clocks
C050 (Q2)	JK Flip-Flop with Set/Reset Master Slave
C033 (Q3)	1-of-4 Decoder with Active Low Outputs and Enable Input
C034 (Q4)	D-Type Flip-Flop with Inverted Reset/Preset and Parallel Load
C070 (Q5)	Multiplexed D-Type Flip-Flop with Reset Input
C036 (Q6)	Toggle Enable Flip-Flop with Inverted Reset
C071 (Q7)	JK Flip-Flop with Set/Reset
C039 (F1)	2-Bit Serial In/Out and Paralleled Out Shift Register
C038 (F2)	Single Bit Up-Down Counter
C052 (H1)	JK Flip-Flop with Set/Reset
C040 (H2)	1-Bit Arithmetic Unit with 7 Functions
C041 (H3)	2-Bit Magnitude Comparator
C042 (H4)	2-Bit Serial/Parallel Shift Register
C066	8×4 RAM
C067	8×8 RAM
C068	8×12 RAM
C069	4-Bit Latch
C053	2-Input XOR Buffer
C054	2-Input 2-Wide OR-AND with Invert
C055	2-Input 2-Wide AND-OR with Invert
C056	2-to-1 Multiplexer Buffer
C057	5-Input NAND-AND
C058	5-Input NOR-OR
C059	Buffered D Flip-Flop
C060	Buffered D Flip-Flop with Set/Reset
C037	JK Flip-Flop with Set/Reset
C064	D Flip-Flop with Reset (Q Output Only)
C065	D Flip-Flop with Set/Reset
C035	Multiplexed D Flip-Flop with Reset

Note: The 'C000' designator is a common reference used between National Semiconductor and its alternate source for the purpose of consistency with users.

5.2 Software Macros

In addition to the pre-designed hardware macros, National Semiconductor offers a library of software macros. These software macros emulate the functions of the popular 7400 and 4000 logic families. From the designer's vantage point, these software macros are utilized as though they were hardware macros. The actual implementation of these higher order functions is handled by the design automation tools in a process that virtually expands the software macro into its hardware macro primitives.

Since the software macros reside in the design automation system, a designer may copy a software macro into his design, modify it to meet some special consideration, rename it, then reference it as a special or new software macro. This procedure is coordinated with NS gate array group.

National Semiconductor adds popular software macros to the existing library as required to meet user needs.

A representative list is shown in Table I. The cell count is a 'will not exceed' number, unused portions of cells are available for use in unrelated portions of the design.

TABLE I

PA Device	Cell Count	PA Device	Cell Count
7400	1.3	74163	24.0
7402	1.3	74164	28.5
7404	1.5	74165	31.5
7408	2.0	74166	33.7
7410	1.5	74168	26.6
7411	2.0	74169	26.6
7420	1.3	74170	38.6
7427	1.5	74173	20.0
7430	2.6	74174	19.0
7442	9.3	74181	41.7
7475	5.0	74182	10.0
7483	19.0	74191	31.0
7485	26.7	74192	28.2
7490	13.8	74193	28.0
7492	13.6	74194	24.7
7493	13.0	74195	20.0
7495	18.5	74241	9.0
7496	14.6	74244	8.7
7498	11.0	74245	16.7
74133	6.33	74251	10.0
74138	8.3	74253	9.0
74139	6.5	74257	7.0
74147	16.3	74259	17.6
74148	11.6	74273	24.9
74150	20.0	74280	19.1
74151	10.2	74283	21.7
74153	9.0	74299	62.6
74155	7.0	74356	33.3
74157	5.0	74373	13.0
74158	7.6	74374	21.0
74160	26.2	74390	14.2
74161	26.3	74393	14.0
74162	26.0		

5.3 Software Macros (User Generated)

The user always has the option of generating higher order software macros. This is true regardless of where the user decides to interface with the design automation system.

At the workstation level, the user simply creates the desired function from existing hardware macros, stores the function under a unique identifier name, then recalls it as a block of logic as required.

In the text file mode of schematic capture the user defines the higher order function in terms of the basic hardware macros. These higher order (custom) functions are then 'called' in the same manner as any other software macro.

6.0 PERIPHERAL MACROS

Interfacing to the SCX gate arrays is done through the peripheral buffers. There are two types of peripheral cells; input only and bi-directional I/O cells. The peripheral macros are not included in the count of internally available cells.

The buffers are located around the periphery of the die and the exact configuration is dependent on the particular family member under consideration. Reference section 3 for specific locations of input and I/O cells.

7.0 PACKAGING

The SCX family of microCMOS gate arrays is offered in a very wide variety of packages. The user is provided with many choices in terms of both package type and lead count. The package types offered include ceramic pin grid arrays, leaded ceramic chip carriers (LDCC), leadless ceramic chip carriers (LCC), plastic leaded chip carriers (PCC), ceramic DIPs, and plastic DIPs.

The availability of such a large variety of packages gives the user flexibility in making the following choices:

—Ceramic versus plastic

—Through-hole mount versus surface mount

—Variety of lead counts

The specific packages offered are listed in Table IIa.

Surface mounting of multi-lead components is rapidly gaining popularity. To provide the user flexibility, National Semiconductor offers its CMOS gate arrays in several surface mount package options: leaded and leadless ceramic chip carrier and the plastic chip carrier.

Surface mounting refers to component attachment, whereby the component leads or pads rest on the surface of the PCB instead of the traditional approach of inserting the leads into through-holes which go through the board. With surface mounting there are solder pads on the PCB which align with the leads or pads on the component. The resulting solder joint forms both the mechanical and electrical connections.

The primary reason for surface mounting is to allow leads to be placed closer together than the 0.100 inch standard for DIPs with through-hole mounting. Through-hole mounting on smaller than 0.100 inch space is difficult to achieve in production and is generally avoided. The move to 0.050 inch lead spacing offered with the current generation of surface mounted components, along with a switch from a dual-in-line format to a quad format, has achieved a threefold increase in component mounting density. A need to achieve greater density is a major driving force in today's marketplace.

Learning how to surface mount components to printed circuit boards requires the user to implement an assembly process not typically associated with through-hole insertion/wave soldering assembly methods.

Surface mounting involves three basic process steps:

1) Application of solder or solder paste to the printed circuit board
2) Positioning of the component onto the printed circuit
3) Reflowing of the solder or solder paste.

Table IIb lists the manufacturers currently offering sockets for each of the advanced package options listed in this data sheet. A matrix of which manufacturers to contact for each socket option is provided. The listing is divided into test/burn-in and production categories. There may be some individual sockets that will cover both requirements.

2

TABLE IIa. GATE ARRAY PACKAGE OPTIONS

Package Type	Pins	CMOS SCX Series 6306	6312/ 6212	6324/ 6224	6325/ 6225	6348/ 6248	6360/ 6260
Plastic DIP, N	28	■	■				
	40	■	■	■	■		
	48		■	■	■		
Ceramic DIP, (Side Braze), D	28	■	■				
	40	■	■	■	■		
	48		■	■	■		
Ceramic DIP, (Cerdip), J	28	■	■				
	40	■	■	■	■		
Plastic Leaded Chip Carrier, PCC	28	■	■				
	44	■	■	■	■		
	68		■	■	■	■	
	84			■	■	■	
	124			■	■	■	
Ceramic Leaded Chip Carrier, LDCC	124			■	■	■	■
Ceramic Leadless Chip Carrier, LCC	28	■	■				
	44	■	■	■	■		
	68		■	■	■	■	
	84			■	■	■	
	124			■	■	■	■
Ceramic Pin Grid Array, PGA	68			■	■	■	
	84			■	■	■	
	120/124			■	■	■	■
	149						
	172					■	■

TABLE IIb. SOCKET VENDORS

Package Type	Test/Burn-In	Production
Ceramic Pin Grid Array	Amp, Textool, Yamaichi, Thomas & Betts	Amp, Yamaichi, Thomas & Betts
Leaded Ceramic Chip Carrier	Yamaichi	Yamaichi
Leadless Ceramic Chip Carrier	Amp, Plastronics, Textool	Amp, Plastronics
Plastic Chip Carrier	Textool	Amp, Burndy, Robinson/Nugent

Vendor Location and Telephone

Amp Inc.
Harrisburg, PA
(715) 564-0100

Plastronics
Irving, TX
(214) 258-1906

Robinson/Nugent
New Albany, IN
(812) 945-0211

Burndy
Norwalk, CT
(203) 838-4444

Textool
Irving, TX
(214) 259-2678

Thomas & Betts
Raritan, NJ
(201) 469-4000

Yamaichi
c/o Napenthe Dist.
Palo Alto, CA
(415) 856-9332

8.0 PROPAGATION DELAYS

Propagation delays in CMOS arrays are a function of several factors:

- Supply voltage
- Junction temperature
- Process tolerance
- Fan-out loading
- Interconnection routing
- Input signal direction

To assist the designer in evaluating circuit performance under all operating conditions, National Semiconductor guarantees DC and AC parametrics over the full voltage and temperature range, as well as best-case and worst-case propagation delays. Process tolerance is included in the specifications.

Delays other than three for fan-out loading may be extrapolated for loads other than shown.

For example: a 2-input NAND (S1) drives six loads. What is the worst-case LO to HI delay?

From Table III
t_{PLH} for 0 pF = 1.82 ns (0 loads)
t_{PLH} for 1 pF = 4.95 ns (3 loads)

The delay per load = (4.95 − 1.82)/3 = 1.05 ns

Total delay = base delay (0 load) + six loads

8.12 ns = 1.82 ns + 6(1.05 ns)

What is the delay if the power supply is maintained at 5V and junction temperature is 80°C (approximately 65° ambient)?

From scaling factors (Table III note):

Worst-case junction temperature = 100°C

New junction temperature = 80°C

Improvement factor $= \frac{0.3\%}{°C}$ (100°C − 80°C) = 6%

Worst-case voltage = 4.5V

New voltage = 5.0V

Improvement factor $= \frac{2\%}{0.1V}$ (5.0V − 4.5V) = 10%

Derating factor = (1 − 0.06)(1 − 0.1) = 0.846

Total delay (scaled) = 8.12(0.846) = 6.86 ns

This form of calculation is handy for making estimates of critical paths during the initial design phase and can be used as a guide to determine which technology to use (i.e., 3μ or 2μ). The actual AC performance prediction will be provided by the design automation system after the designer has functionally verified his design in the logic simulator.

Propagation delays as a function of temperature and supply voltage are shown in *Figures 4 and 5* respectively. Utilization of these curves will speed the estimation of performance at other then specified values.

Representative macro types for the 3μ (Table III) and 2μ process (Table IV) are presented for comparison. Reference SCX family macro library book for complete specifications.

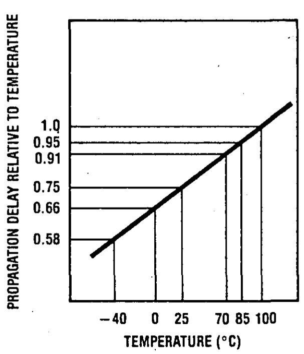


FIGURE 4. CMOS Propagation Delays as a Function of Temperature

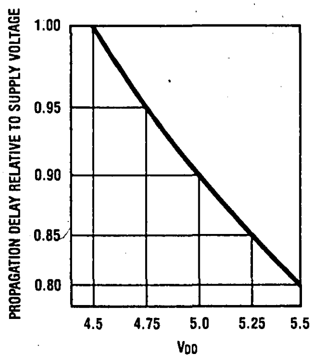


FIGURE 5. CMOS Propagation Delays as a Function of Supply Voltage

Best-Case	Worst-Case
Temperature = – 40°C Supply Voltage = 5.5V Extreme Process Parameters	Temperature = 100°C Supply Voltage = 4.5V Extreme Process Parameters

TABLE III. 3μ

Symbol	Function	LF	Best-Case		Worst-Case		C_{LOAD} (pF)
			t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	
S1	2-NAND	1	0.32 0.81	0.36 1.04	1.82 4.95	1.82 6.2	0 1
S2	3-NAND	1	0.36 0.85	0.54 1.55	2.3 5.45	3.3 9.4	0 1
S4	2-NOR	1	0.43 1.26	0.32 0.81	2.6 8.25	1.98 4.62	0 1
S5	3-NOR	1	0.54 1.76	0.32 0.81	3.95 12.6	2.3 4.95	0 1
S7	Clock Buffer	2	0.25 0.53	0.24 0.53	1.16 3.08	1.05 2.80	0 1
S8	Inverter	1	0.3 0.78	0.3 0.76	1.54 4.73	1.48 4.24	0 1
S11	2-XOR	2	0.34 1.12	0.29 1.0	5.2 10.8	5.3 9.7	0 1
D9	D Flip-Flop CLK to Q	1 3	 1.55 2.07	 1.39 1.94	 10.1 13.5	 8.5 11.6	 0 1
	CLK to Q_B		0.85 1.44	1.04 1.66	5.1 9.8	6.8 11.6	0 1
S9	TRI-STATE Inverter	1	0.45 1.35	0.45 1.2	2.75 8.45	1.95 6.9	0 1
S10	TRI-STATE Buffer	2	0.7 1.2	0.66 1.05	3.7 6.9	3.85 6.25	0 1
I_4	Inverting Input Buffer	CMOS	0.44 0.83	0.29 0.6	1.85 4.5	1.2 3.1	0 1
I_1	Input Buffer	TTL	0.75 1.22	0.81 1.41	3.6 7.15	5.5 9.25	0 1
I_6	Short Circuit Input	CMOS	0.05 0.20	0.05 0.20	0.10 0.65	0.10 0.65	0 1
IO_1	Input	TTL	0.75 1.22	0.81 1.41	3.6 7.15	5.5 9.25	0 1
	Output*	7	1.35 2.4	1.62 2.7	9.6 15.8	10.7 16.5	15 50
IO_2	Input (Inverting)	CMOS	0.43 0.83	0.3 0.61	1.87 4.5	1.24 3.03	0 1
	Output*	7	1.35 2.4	1.62 2.7	9.6 15.8	10.7 16.5	15 50
IO_3	Short Circuit Input	CMOS	0.43 0.83	0.30 0.61	1.87 4.50	1.24 3.03	0 1
	Output*		1.35 2.4	1.62 2.7	9.6 15.8	10.7 16.5	15 50
IO_4	Output	7	1.4 2.34	1.33 2.38	9.2 15.2	8.6 14.1	15 50

Note: All delays in nanoseconds.
*TRI-STATE active mode.
$t_r = t_f = 5$ ns for 3-micron.
$t_r = t_f = 2$ ns for 2-micron.
Voltage Derate = 2.0%/100 mV from 4.5V.
Temperature Derate = 0.3%/°C from 100°C.
LF = Load Factor.
1LF = 0.17 pF.

2

TABLE IV. 2μ

Symbol	Function	LF	Best-Case t_{PLH}	Best-Case t_{PHL}	Worst-Case t_{PLH}	Worst-Case t_{PHL}	C_{LOAD} (pF)
S1	2-NAND	1	0.095	0.19	0.75	0.95	0
			0.39	0.67	2.40	4.05	1
S2	3-NAND	1	0.09	0.27	0.95	1.65	0
			0.37	0.92	2.65	5.75	1
S4	2-NOR	1	0.16	0.15	1.1	0.95	0
			0.62	0.51	4.15	2.85	1
S5	3-NOR	1	0.23	0.16	1.65	1.13	0
			0.85	0.52	6.1	3.05	1
S7	Clock Buffer	2	0.07	0.13	0.45	0.55	0
			0.24	0.33	1.45	1.65	1
S8	Inverter	1	0.095	0.16	0.6	0.75	0
			0.36	0.52	2.35	2.6	1
S11	2-XOR	2	0.11	0.16	2.6	2.5	0
			0.54	0.53	5.8	5.65	1
D9	D Flip-Flop	1					
	CLK to Q	3	0.71	0.59	5.12	4.38	0
			1.02	0.94	7.0	6.25	1
	CLK to Q_B		0.35	0.54	2.38	3.3	0
			0.64	0.98	5.37	6.62	1
S9	TRI-STATE Inverter	1	0.18	0.18	1.2	1.35	0
			0.60	0.70	4.25	4.15	1
S10	TRI-STATE Buffer	2	0.30	0.27	1.9	1.8	0
			0.53	0.53	3.4	3.4	1
I_4	Inverting Input Buffer	CMOS	0.23	0.19	0.85	0.70	0
			0.45	0.39	2.30	1.80	1
I_1	Input Buffer	TTL	0.33	0.39	2.0	2.45	0
			0.60	0.78	3.70	4.80	1
I_6	Short Circuit Input	CMOS	0.04	0.04	0.07	0.07	0
			0.15	0.15	0.50	0.50	1
IO_1	Input	TTL	0.33	0.39	2.0	2.45	0
			0.60	0.78	3.7	4.8	1
	Output*	7	0.62	0.78	4.4	5.75	15
			1.15	1.55	7.0	9.75	50
IO_2	Input (Inverting)	CMOS	0.23	0.19	0.85	0.70	0
			0.45	0.39	2.30	1.80	1
	Output*	7	0.62	0.78	4.40	5.75	15
			1.15	1.55	7.0	9.75	50
IO_3	Short Circuit Input	CMOS	0.04	0.04	0.07	0.07	0
			0.15	0.15	0.50	0.50	1
	Output*		0.62	0.78	4.40	5.75	15
			1.15	1.55	7.0	9.75	50
IO_4	Output	7	0.65	0.63	4.75	4.5	15
			1.17	1.45	8.25	8.25	50

Note: All delays in nanoseconds.
*TRI-STATE active mode.
$t_r = t_f = 5$ ns for 3-micron.
$t_r = t_f = 2$ ns for 2-micron.
Voltage Derate = 2.0%/100 mV from 4.5V.
Temperature Derate = 0.3%/°C from 100°C.
LF = Load Factor.
1LF = 0.13 pF.

9.0 DESIGN AUTOMATION SYSTEM

The design automation system offers the end user a variety of interface points and techniques.

Figure 6 shows the standard gate array development flow and responsibilities. Alternative flows are available and are presented in Section 11.

The standard flow consists of four major quadrants. They are the user's site, user's responsibilities, National Semiconductor's technology center, National Semiconductor's responsibility. These represent the 'where' and 'who' aspects of task responsibility and location.

User Site

Logic design and definition are the user's responsibility and are completed at his/her site.

The design file consists of the netlist (wiring diagram) and the test vectors (pattern file). Each can be generated in a text file or as the output from a 'workstation'. The syntax of these files is in the 'hardware design language'.

The evaluation and acceptance of the completed prototypes are done by the user at his/her facilities. National Semiconductor offers technical assistance if necessary.

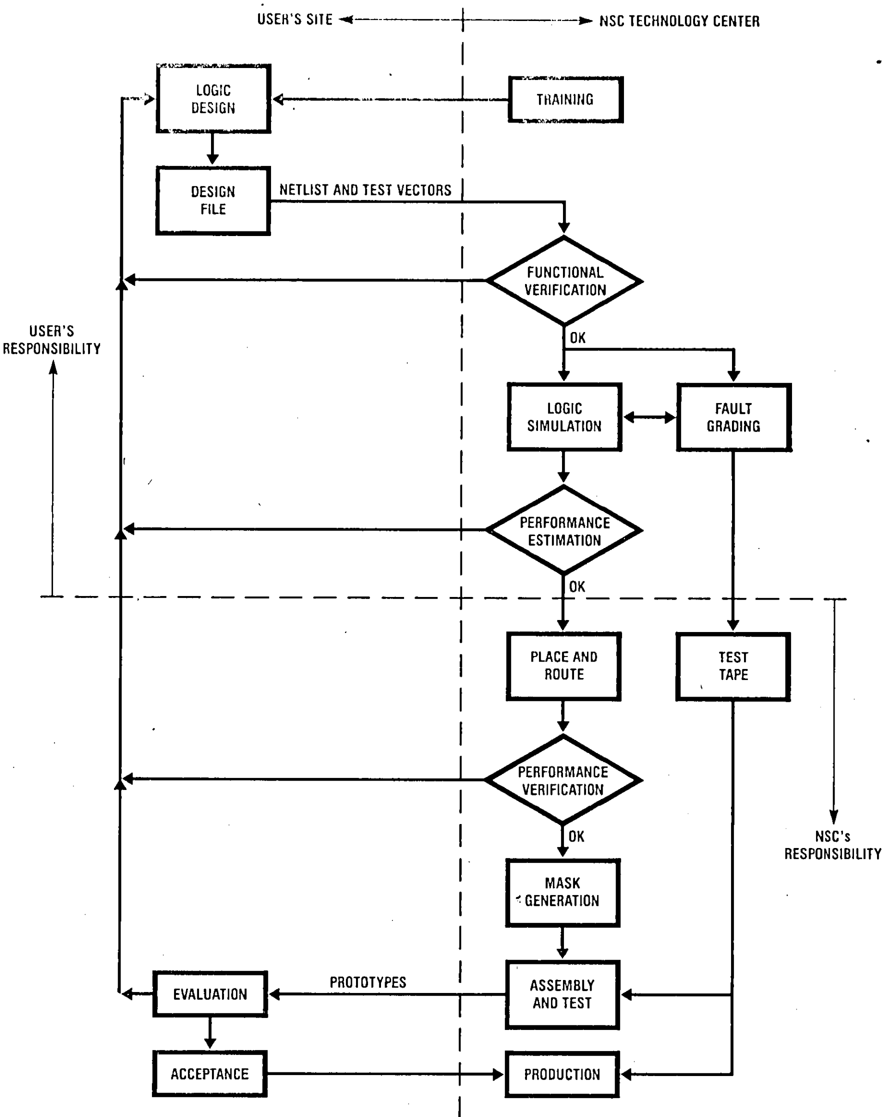


FIGURE 6. Standard Gate Array Development Process and Responsibilities

National Semiconductor Technology Center

Training includes actual interaction with the design automation system and, depending on the level of user experience, requires from three to five days to complete. All of the considerations necessary for the successful completion of the design are covered during the training. Topics such as hardware (i.e., speed, power, pinouts) and software considerations (i.e., logic simulation, fault grading, critical path analysis) are tailored to meet the user's needs. Training is provided at the closest technology center. Contact the local sales representative for the location nearest you.

Functional verification of the logic is accomplished by submitting the netlist and pattern files to the logic simulator. The simulator will predict the output results of the specified logic for the applied vectors. The designer can then determine if the specified logic meets the design objectives. Simulation under actual 'loaded' conditions occurs after functional verification and fault grading. Functional verification is the responsibility of the user.

Fault grading is a measure of the ability of the supplied vectors to detect induced logic errors (i.e., on-chip shorts). The vectors supplied eventually become the functional portion of the final production test tape. It is important that the fault grading figure of merit reach 85%. Fault grading is the responsibility of the user.

Performance estimation is the prediction that the logic simulator makes by considering actual macro loading and a projection of the interconnect lengths. This projection is based on an algorithm which relates fan-out to probable trace length. Performance estimation is the responsibility of the user.

Place and route are the actual implementation of the user's design file. Two pieces of design automation software are used to complete the routing.

Automatic place and route software completes the majority of interconnects and in most cases completes the entire array.

Interactive graphics software is used to complete any unrouted interconnects.

Place and route are the responsibility of National Semiconductor.

Performance verification is the rerunning of the 'performance estimation' software with the actual cell placements and associated trace lengths. Performance verification is the responsibility of the user.

Mask generation, assembly and test are completed by National Semiconductor.

Prototype evaluation and acceptance are the responsibility of the user.

National Semiconductor has a large staff of applications and consulting engineers available to assist users at any point in the array development process.

10.0 DESIGN EXAMPLE

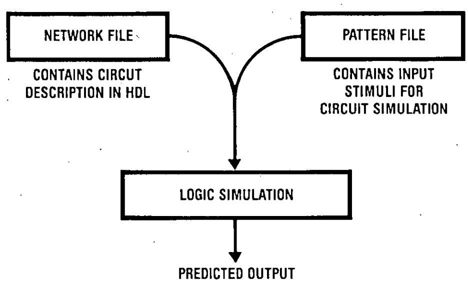
The two most popular ways of interfacing to the design automation system are 1) alphanumeric text entry and 2) workstation output. A different example will be given for each. In either case the design automation system requires two basics files to operate.

Network (File): The network file is the 'wiring diagram' of the design. It represents how the array is to be 'wired'. More specifically, it is the manner in which the hardware macros are interconnected. The syntax of the network file is specified by a hardware design language (HDL).

Pattern (File): The pattern file represents the stimuli or sequence of signals used to exercise the design specified by the network file. The pattern file ultimately becomes the functional portion of the final test tape used to screen production devices.

The logic simulator operates on the network and pattern files and predicts the logic output as a function of the pattern file.

Data Entry



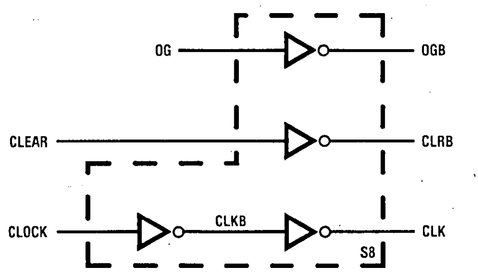
TL/U/5725-11

The simulator has two modes of operation. The first mode is used to verify the logical integrity of the design. The second mode considers capacitive circuit loading and anticipated wire lengths. The result of the second mode is the performance that can be expected after the circuit has been placed and routed.

The basic form of a network file is as follows.

```
$NETWORK                      (* BEGIN A NETWORK FILE *)
$ INP  INA INB ETC.           (* LIST ALL INPUT NAMES *)
$ OUT  OUTA OUTB ETC.         (* LIST ALL OUTPUT NAMES *)
        •
        •
        •
    MACRO CALLS               (* SPECIFY MACROS AND
                                        INTERCONNECTS *)
        •
        •
        •
$$*     COMMENTS              (* MAKE COMMENTS *)
        •
        •
        •
```

The macro call syntax for the following circuit fragment is as specified.



TL/U/5725-12

```
$SUBU  S8
  |    |
  |    |_______(* SPECIFIES A PARTICULAR
  |                  MACRO TYPE *)
  |____________(* SPECIFIES A HARDWARE MACRO *)

$$ANO          (* CIRCUIT NAME ASSOCIATED WITH
 |_______________ABOVE MACRO *)

                      ___(* DELIMITER *)
                     |
CLKB CLK CLRB OGB / CLOCK CLKB CLEAR OG
   |                |_______________|
   |                |__(* INPUTS TO MACRO ELEMENTS *)
   |
   |________(* OUTPUTS FROM MACRO ELEMENTS *)
```

If the designer were using the alphanumeric text mode of data entry, each unique macro and macro type would be specified in the above manner until the entire network had been specified.

In the workstation mode of schematic capture the designer would call and name each desired macro, then graphically interconnect each macro in the required fashion. The workstation would then 'compile' the schematic into the network file.

10.1 Text Mode

The design of a four-bit latch with TRI-STATE output is presented.

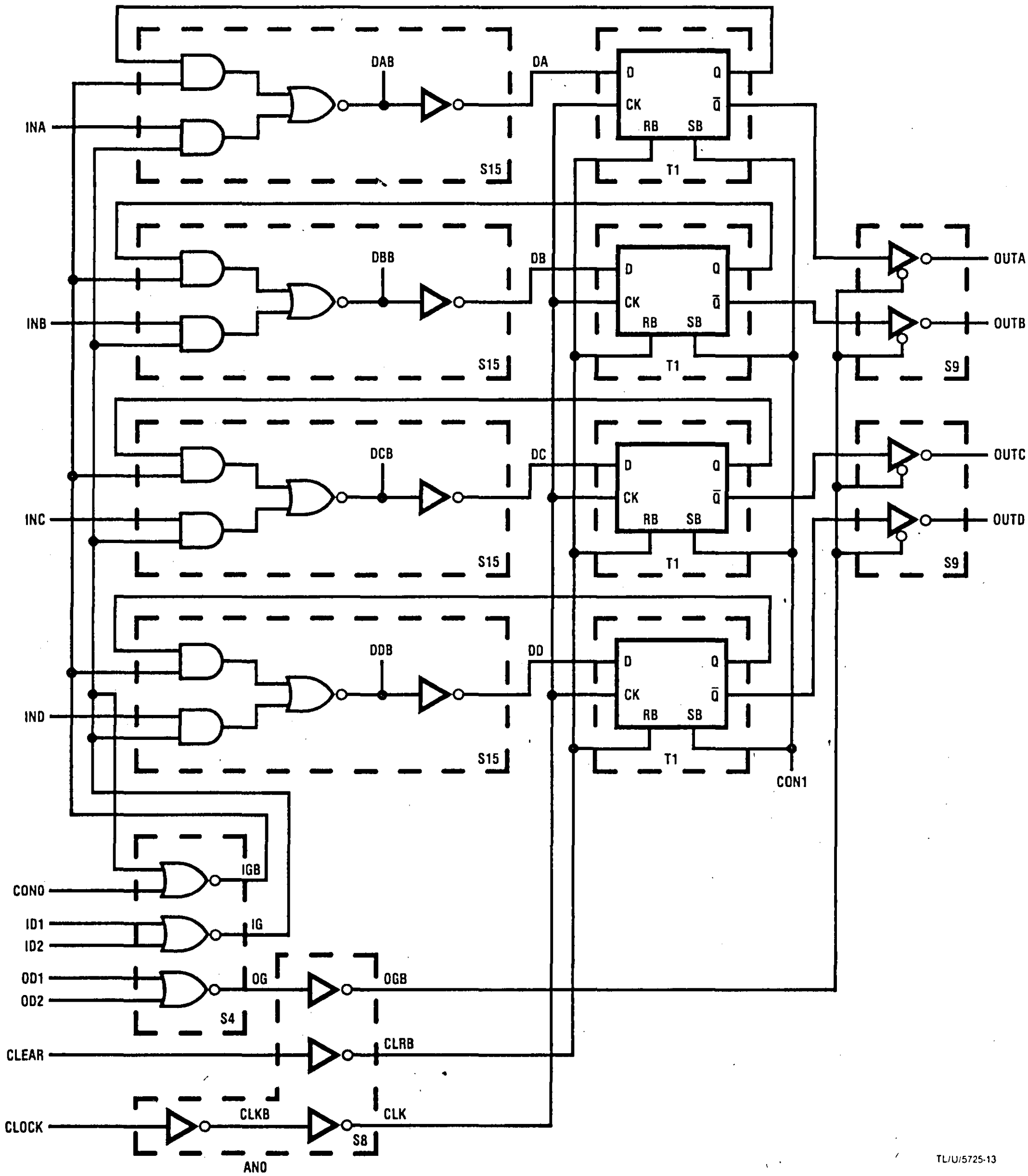


FIGURE 7

2

Listing 1

```
$$ ★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
$NETWORK
$INPUT  INA  INB  INC  IND  ID1  ID2  OD1  OD2  CLOCK  CLEAR
$OUTPUT  OUTA  OUTB  OUTC  OUTD
$$★  DM74173  MACRO
$SUBU  S8
$$AN0
CLKB  CLK  CLRB  OGB  /  CLOCK  CLKB  CLEAR  OG
$SUBU S4
$$AN1
IG  IGB  OG  /  ID1  ID2  IG  CON0  OD1  OD2
$SUBU S15
$$AN2
DAB  DA  /  INA  IG  IGB  QA
$SUBU  S15
$$AN3
DBB  DB  /  INB  IG  IGB  QB
$SUBU  S15
$$AN4
DCB  DC  /  INC  IG  IGB  QC
$SUBU  /  S15
$$AN5
DDB  DD  /  IND  IG  IGB  QD
$SUBU T1
$$AN6
QA  QAB  /  CON1  DA  CLK  CLRB
$SUBU  T1
$$AN7
QB  QBB  /  CON1  DB  CLK  CLRB
$SUBU T1
$$AN8
QC  QCB  /  CON1  DC  CLK  CLRB
$SUBU T1
$$AN9
QD  QDB  /  CON1  DD  CLK  CLRB
$SUBU S9
$$AN10
OUTA  OUTB  /  QAB  OGB  QBB  OGB
$SUBU S9
$$AN11
OUTC  OUTD  /  QCB  OGB  QDB  OGB
$$ ★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
```

10.2 Workstation Mode

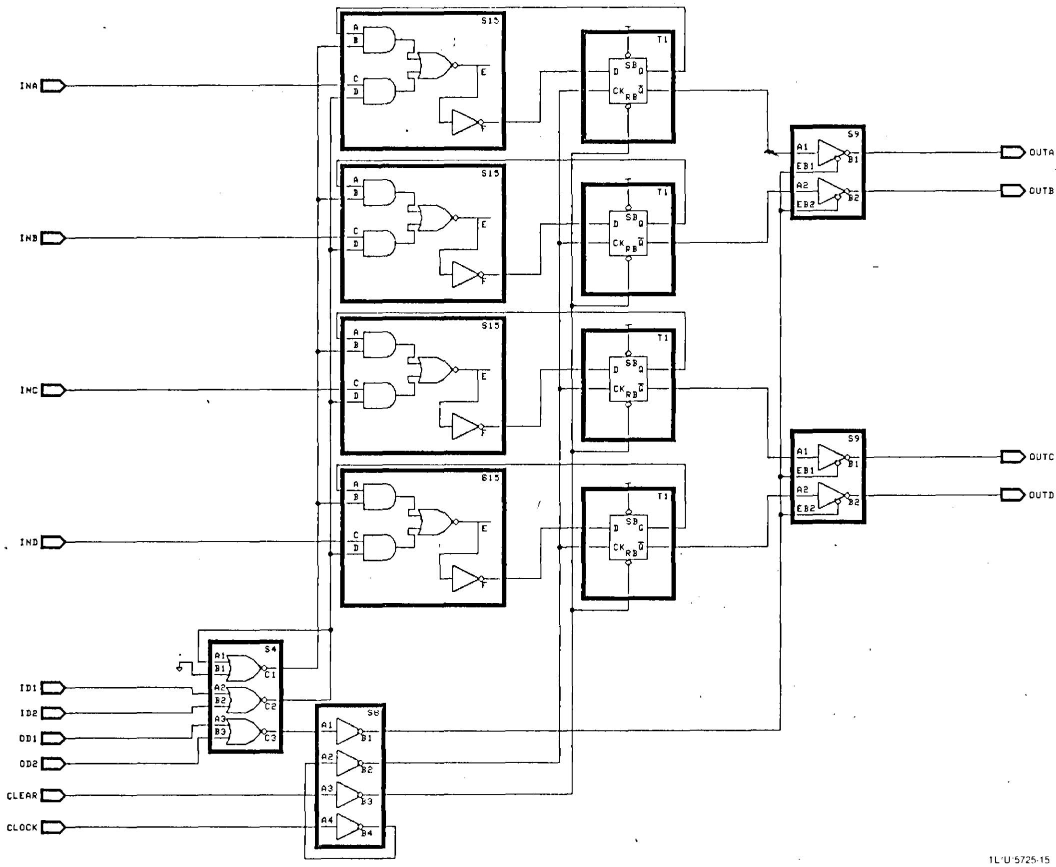


FIGURE 8

Listing 2

```
$NETWORK
$INPUT  CLEAR  CLOCK  ID1  ID2  INA  INB  INC  IND  OD1  OD2
$OUTPUT  OUTA  OUTB  OUTC  OUTD
$$★
$SUBU  S4
$$XCMP 1
XSIG29  XSIG27  XSIG18  /  XSIG27  GND  ID1  ID2  OD1  OD2
$$★
$SUBU  T1
$$XCMP 10
XSIG33  XSIG41  /  VCC  XSIG34  XSIG20  XSIG21
$$★
$SUBU  S9
$$XCMP 11
OUTA  OUTB  /  XSIG41  XSIG22  XSIG40  XSIG22
$$★
$SUBU  S9
$$XCMP 12
OUTC  OUTD  /  XSIG39  XSIG22  XSIG38  XSIG22
$$★
$SUBU  S8
$$XCMP 2
XSIG22  XSIG20   XSIG21  XSIG19  /  XSIG18  XSIG19  CLEAR  CLOCK
$$★
$SUBU  S15
$$XCMP 3
OPEN-1  XSIG37  /  XSIG30  XSIG29  IND  XSIG27
$$★
$SUBU  S15
$$XCMP 4
OPEN-2  XSIG36  /  XSIG31  XSIG29  INC  XSIG27
$$★
$SUBU  S15
$$XCMP 5
OPEN-3  XSIG35  /  XSIG32  XSIG29  INB   XSIG27
$$★
$SUBU  S15
$$XCMP 6
OPEN-4  XSIG34  /  XSIG33  XSIG29  INA  XSIG27
$$★
$SUBU  T1
$$XCMP 7
XSIG30  XSIG38  /  VCC  XSIG37  XSIG20  XSIG21
$$★
$SUBU  T1
$$XCMP 8
XSIG31  XSIG39  /  VCC  XSIG36  XSIG20  XSIG21
$$★
$SUBU  T1
$$XCMP 9
XSIG32  XSIG40  /  VCC  XSIG35  XSIG20  XSIG21
$$★
```

10.3 Pattern File

```
$CYCLE = 1000  1000 REPRESENTS THE NUMBER OF INTERVALS PER CYCLE   1 INTERVAL = 100 PICOSECONDS
$$★★★★★★★★★★★★★★★★★★★★★★★★★★★
$$★  PATTERN FILE CODING FOLLOWS
$$★★★★★★★★★★★★★★★★★★★★★★★★★★★
$$★  PATTERN FILE FOR TESTING DM74173
$$★  TEST SHOULD SWEEP 16 CYCLES
CLEAR  HI  1-2
INA  HI  1 3 5 7 11-12
INB  HI  1 3 5 7 11-12
INC  HI  1 3 5 7 11-12
IND  HI  1 3 5 7 11-12    INPUT SIGNALS USED TO SIMULATE THE NETWORK
ID1  HI  1 3 5-6
ID2  LO  1 3 7-8
OD1  HI  5-6 13-14
OD2  HI  7-8 15-16
CLOCK  LO  RPT  (01:  1-16)  SINGLE CLOCK REPEATING 01 THROUGH CYCLE 16

CIRCUIT INPUTS HI AT SPECIFIED CYCLE. LOW AT ALL OTHER CYCLES
CIRCUIT INPUT LO AT SPECIFIED CYCLE. HI AT ALL OTHER CYCLES
```


10.4 Simulator Output

	INPUTS AS SPECIFIED BY PATTERN FILE					OUTPUTS AS SPECIFIED BY PATTERN FILE
	IIII NNNN ABCD	II DD 12	OO DD 12	CLEAR	CLOCK	OOOO UUUU TTTT ABCD
1	1111	10	00	1	0	XXXX
**157	1111	10	00	1	0	0000
2	0000	01	00	1	1	0000
3	1111	10	00	0	0	0000
4	0000	01	00	0	1	0000
5	1111	11	10	0	0	0000
**134	1111	11	10	0	0	ZZZZ
6	0000	11	10	0	1	ZZZZ
7	1111	00	01	0	0	ZZZZ
8	0000	00	01	0	1	ZZZZ
9	0000	01	00	0	0	ZZZZ
**140	0000	01	00	0	0	1111
10	0000	01	00	0	1	1111
11	1111	01	00	0	0	1111
12	1111	01	00	0	1	1111
13	0000	01	10	0	0	1111
**129	0000	01	10	0	0	ZZZZ
14	0000	01	10	0	1	ZZZZ
15	0000	01	01	0	0	ZZZZ
16	0000	01	01	0	1	ZZZZ

SEQUENTIAL NUMBERS REPRESENT TIME CYCLES

ZZZZ = HIGH IMPEDANCE STATE
1111 = HIGH STATE
0000 = LOW STATE

**Intermittent numbers represent settling time in hundred-picoseconds that occur between time cycles.

11.0 ALTERNATIVE INTERFACES

Flexibility in the design automation system allows a variety of user/vendor interfaces. Options include:

- User supplies schematic, timing diagrams and parametric specifications. National Semiconductor implements the array.
- User 'captures' the design at his facility or at a National Semiconductor technology center. National Semiconductor supports a wide range of communication protocols for interfacing to industrial (mainframe) or personal computers. These are available with or without error control and communication rates of 300 to 9600 baud.
- User follows basic array development flow specified in *Figure 6*.
- User generates logic simulator compatible files from his workstation. Completes the array using National Semiconductor's design automation system.
- User generates compatible design files and logic verification in his/her simulator, then interfaces to design automation system at either fault grading, performance estimation, or 'place and route'.
- User supplies completed design files from National Semiconductor's alternate source, effectively entering design automation system just prior to digitizing.
- User provides all design files necessary for mask generation, essentially a 'customer owned tooling' (COT) approach.

Section 3

LSI/VLSI CMOS

3

Introduction

The new microCMOS technologies are also being used to provide functional-specific standard products. These LSI/VLSI circuits are of relatively large complexity and represent additional uses for the advanced CMOS processes.

A special group of LSI/VLSI circuitry exists within the popular MM54/74HC microCMOS logic family. These products make use of the product designation MM54/74HC9XX. An example of this 900 series is the MM74HC942—a high performance, low power, Bell 103 compatible single-chip modem. This product combines both digital and linear circuitry to bring the benefits of system level integration to modem and systems designers.

When considering a new design, it is important to keep in mind the wide range of standard products that are available. In addition to memories and microprocessors, the products in this section also enjoy high volume usage and can provide cost savings as well as reduce the complexity and amount of semi-custom or custom circuitry required to implement a new system.

National Semiconductor

MM5368 CMOS Oscillator Divider Circuit

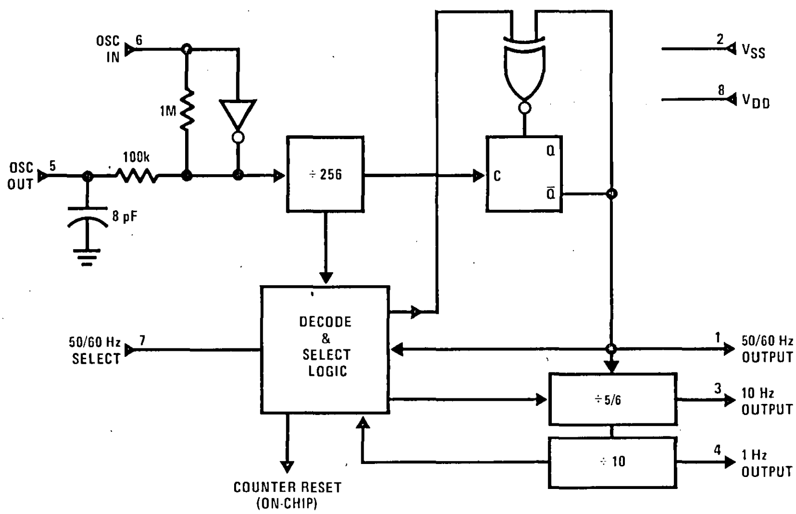
General Description

The MM5368 is a CMOS integrated circuit generating 50 or 60 Hz, 10 Hz, and 1 Hz outputs from a 32 kHz crystal (32,768 Hz). For the 60 Hz selected output the input time base is divided by 546.133, for the 50 Hz mode it is divided by 655.36. The 50/60 Hz output is then divided by 5 or 6 to obtain a 10 Hz output which is further divided to obtain a 1 Hz output. The 50/60 Hz select input can be floated for a counter reset.

Features

- 50/60 Hz output
- 1 Hz output
- 10 Hz output
- Low power dissipation
- Fully static operation
- Counter reset
- 3V–15V supply range
- On-chip oscillator — tuning and load capacitors are the only required external components besides the crystal. (For operation below 5V it may be necessary to use an ~ 1MΩ pullup on the oscillator output to insure start-up.)

Block Diagram

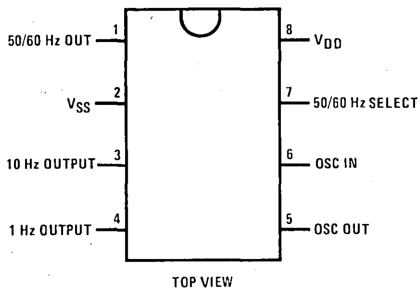


TL/F/6133-1

FIGURE 1

Connection Diagram

Dual-In-Line Package



TL/F/6133-2

FIGURE 2. Pin-Out

Order Number MM5368N
See NS Package N08E

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	$0°C$ to $+70°C$
Storage Temperature	$-65°C$ to $+150°C$
Maximum V_{DD} Voltage	16V
Operating V_{DD} Range	$3V \leq V_{DD} \leq 15V$
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating range, $V_{SS} = 0V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	$V_{DD} = 15V$; 50/60 Select Floating			10	μA
Operating Current Drain	$f_{IN} = 32$ kHz, $V_{DD} = 3V$			50	μA
	$f_{IN} = 32$ kHz, $V_{DD} = 15V$			1500	μA
Maximum Input Frequency	$V_{DD} = 3V$			64	kHz
	$V_{DD} = 15V$			500	kHz
Output Current Levels	$V_{DD} = 5V$				
Logical "1", Source	$V_{OH} = V_{SS} + 2.7V$			−400	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	400			μA
	$V_{DD} = 9V$				
Logical "1", Source	$V_{OH} = V_{SS} + 6.7V$			−1500	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	1500			μA
Input Current Levels	50/60 Select Input				
Logical "1" (I_{IH})	$V_{DD} = 3V$, $V_{IN} \geq 0.9V_{DD}$			50	μA
Logical "1" (I_{IH})	$V_{DD} = 15V$, $V_{IN} \geq 0.9V_{DD}$			3	mA
Logical "0" (I_{IL})	$V_{DD} = 3V$, $V_{IN} \leq 0.1V_{DD}$			20	μA
Logical "0" (I_{IL})	$V_{DD} = 15V$, $V_{IN} \leq 0.1V_{DD}$			1	mA

Functional Description *(Figure 1)*

The MM5368 initially divides the input time base by 256. From the resulting frequency (128 Hz for 32 kHz crystal) 8 clock periods are dropped or eliminated during 60 Hz operation and 28 clock periods are eliminated during 50 Hz operation. This frequency is then divided by 2 to obtain a 50 or 60 Hz output. This output is not periodic from cycle to cycle; however, the waveform repeats itself every second. Straight divide by 5 or 6 and 10 are used to obtain the 10 Hz output and the 1 Hz outputs.

The 60 Hz mode is obtained by tying pin 7 to V_{DD}. The 60 Hz output waveform can be seen in *Figure 3.* The 10 Hz and 1 Hz outputs have an approximate 50% duty cycle. In the 50 Hz mode the 50/60 select input is tied to V_{SS}. The 50 Hz output waveform can be seen in *Figure 3.* The 10 Hz output has an approximate 40% duty cycle and the 1 Hz output has an approximate 50% duty cycle.

For the 50/60 Hz select input floating, the counter chain is held reset, except for the initial toggle flip-flop which is needed for the reset function. A reset may also occur when the input is switched *(Figure 4).* To insure the floating state, current sourced from the input must be limited to 1.0 μA and current sunk by the input must be limited to 1.0 μA for $V_{DD} = 3V$.

Timing Diagrams

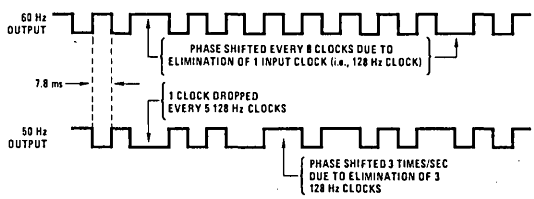
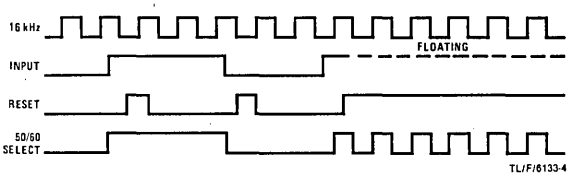


FIGURE 3. 50/60 Hz Output



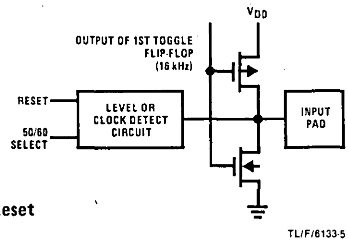
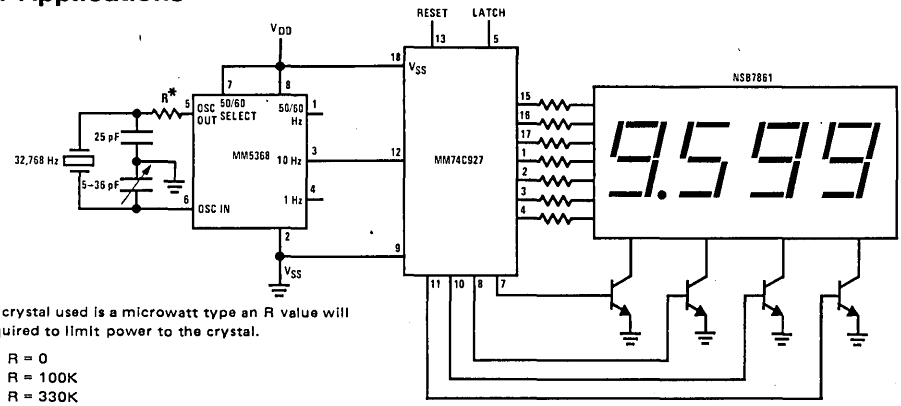


FIGURE 4. 50/60 Select and Reset

Typical Applications



*If the crystal used is a microwatt type an R value will be required to limit power to the crystal.

3V R = 0
5V R = 100K
10V R = 330K

FIGURE 5. 10 Minute (9:59.9) Timer

National Semiconductor

MM5369 Series 17 Stage Oscillator/Divider

General Description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the crystal frequency for tuning purposes and the 17th stage output. The MM5369 is available in an 8-lead dual-in-line epoxy package.

Features

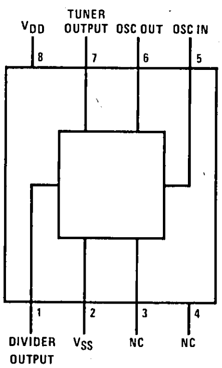
- Crystal oscillator
- Two buffered outputs
  - Output 1 crystal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10V)
- Wide supply range 3–15V
- Low power
- Fully static operation
- 8 lead dual-in-line package
- Low current

Options

- MM5369AA 3.58 MHz to 60 Hz
- MM5369EYR 3.58 MHz to 50 Hz
- MM5369EST 3.58 MHz to 100 Hz

Connection Diagram

Dual-In-Line Package



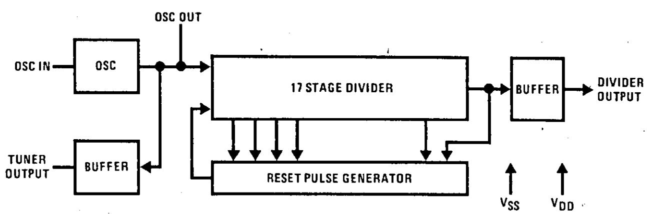
TOP VIEW

TL/F/6134-1

Order Number MM5369AA/N, MM5369EYR/N, MM5369EST/N
See NS Package N08E

FIGURE 1

Block Diagram



TL/F/6134-2

FIGURE 2

Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{DD} +0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	16V
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = GND, 3V $\leq V_{DD} \leq$ 15V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 15V			10	μA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V	DC		4.5	MHz
	V_{DD} = 6V	DC		2	MHz
Output Current Levels	V_{DD} = 10V				
	V_O = 5V				
Logical "1" Source		500			μA
Logical "0" Sink		500			μA
Output Voltage Levels	V_{DD} = 10V				
	I_O = 10 μA				
Logical "1"		9.0			V
Logical "0"				1.0	V

Note: For 3.58 MHz operation, V_{DD} must be ≥ 10V.

Functional Description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2*.

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

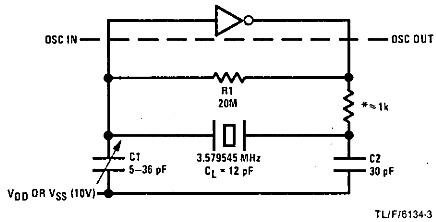
DIVIDER

A pulse is generated when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs.

Functional Description (Continued)



*To be selected based on xtal used

FIGURE 3. Crystal Oscillator Network

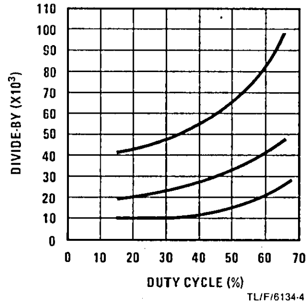


FIGURE 4. Plot of Divide-By vs Duty Cycle

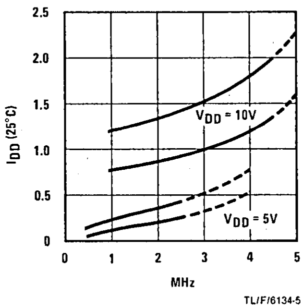


FIGURE 5. Typical Current Drain vs Oscillator Frequency

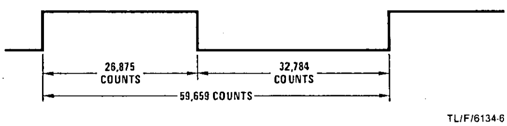


FIGURE 6. Output Waveform for Standard MM5369AA

National Semiconductor

MM53107 Series 17-Stage Oscillator/Divider

General Description

The MM53107 is a low threshold voltage CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from a 2.097152 MHz quartz crystal. An internal pulse is generated by the combinations of stages 1–4, 16 and 17 to set or reset the individual stages. The MM53107 is advanced one count on the positive transition of each clock pulse. One buffered output is available: the 17th stage 60 Hz output. The MM53107 is available in an 8-lead dual-in-line epoxy package.

Features

- Input frequency—2.097152 MHz
- Output frequency—60Hz
- Crystal oscillator
- High speed (2 MHz at V_{DD} = 2.5V)
- Wide supply range 2.5V–6V
- Low power (0.5 mW @ 2 MHz/2.5V)
- Fully static operation
- 8-lead dual-in-line package

3

Block and Connection Diagrams

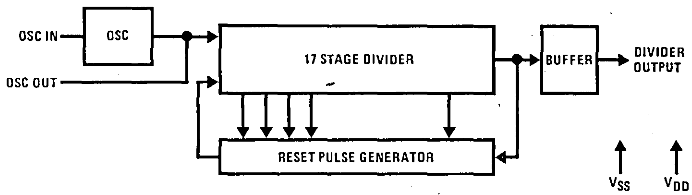
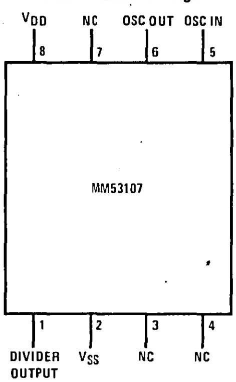


FIGURE 1

TL/F/6142-1

Dual-In-Line Package



TOP VIEW

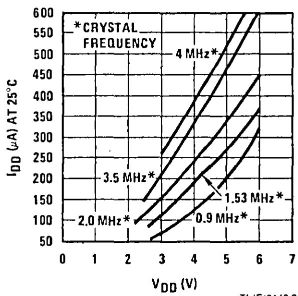
TL/F/6142-2

FIGURE 2

Order Number MM53107N
See NS Package N08E

Typical Performance Characteristics

Typical Current Drain vs Oscillator Frequency



TL/F/6142-3

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	7V
Operating V_{CC} Range	2.5V to 6V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = Gnd, $2.5V \leq V_{DD} \leq 6V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD}= 6V			10	µA
Operating Current Drain	V_{DD}= 2.5V, f_{IN} = 2.1 MHz			200	µA
Frequency of Oscillation	V_{DD}= 2.4V	dc		2.1	MHz
	V_{DD}= 6V	dc		4.0	MHz
Output Current Levels					
Logical "1" Source	V_{DD} = 4V,	100			µA
Logical "0" Sink	V_{OUT} = 2V	100			µA
Output Voltage Levels					
Logical "1"	V_{DD}= 6V, I_OSource = 10µA	5.0			V
Logical "0"	I_OSink = −10µA			1.0	V

Functional Description

A connection diagram for the MM53107 is shown in *Figure 2* and a block diagram is shown in *Figure 1.*

TIME BASE

A precision time base is provided by the interconnection of a 2,097,152 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the Osc In and the Osc Out terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

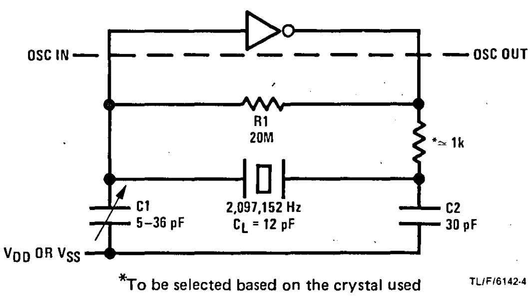
The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

A pulse is generated when divider stages 1–4, 16 and 17 are in the correct state. This pulse is used to set or reset individual stages of the counter, the modulus of the counter is 34,952 to provide 60 Hz.

OUTPUT

The Divide Output is the input frequency divided by 34,952. The output is a push-pull output.



*To be selected based on the crystal used

FIGURE 3. Crystal Oscillator Network

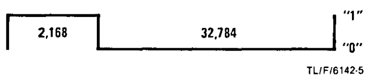


FIGURE 4. Duty Cycle for MM53107

National Semiconductor

MM58167A Microprocessor Real Time Clock

General Description

The MM58167A is a low threshold metal gate CMOS circuit that functions as a real time clock in bus oriented microprocessor systems. The device includes an addressable real time counter, 56 bits of RAM, and two interrupt outputs. A $\overline{\text{POWER DOWN}}$ input allows the chip to be disabled from the rest of the system for standby low power operation. The time base is a 32,768 Hz crystal oscillator.

Features

- Microprocessor compatible (8-bit data bus)
- Milliseconds through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- $\overline{\text{POWER DOWN}}$ input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock

Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table I. Any unused bits are held at a logical zero during a read and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example tens of hours cannot legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table I as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60μs above 4.0V and 300μs at 2.0V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones, then this RAM location will always compare.

The RAM is formatted the same as the real time counter, 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

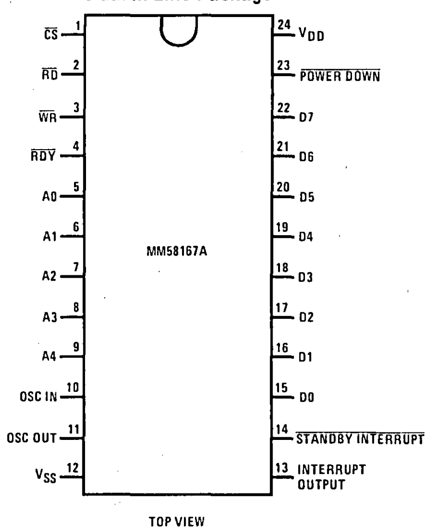
Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (*Figure 1*). Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to its reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupting frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the $\overline{\text{STANDBY INTERRUPT}}$ (open drain output, active low). This interrupt occurs when enabled and when a RAM/real time counter comparison occurs. The $\overline{\text{STANDBY INTERRUPT}}$ is enabled by writing a one on the D0 line at address 16_H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the STANDBY INTERRUPT is enabled, the interrupt will turn on immediately.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6148-1

Order Number MM58167AN
See NS Package N24C

Absolute Maximum Ratings

Voltage at All Pins	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	$-40°C$ to $85°C$
Storage Temperature	$-65°C$ to $150°C$
V_{DD}-V_{SS}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_{SS} = 0V$, $-40°C \leq T_A \leq 85°C$

Parameter	Conditions	Min	Max	Units
Supply Voltage				
V_{DD}	Outputs Enabled	4.0	5.5	V
V_{DD}	$\overline{\text{POWER}}$ $\overline{\text{DOWN}}$ Mode	2.0	5.5	V
Supply Current				
I_{DD}, Static	Outputs TRI-STATE® $f_{IN} = DC$, $V_{DD} = 5.5V$		10	μA
I_{DD}, Dynamic	Outputs TRI-STATE $f_{IN} = 32$ kHz, $V_{DD} = 5.5V$ $V_{IH} \geq V_{DD} - 0.3V$ $V_{IL} \leq V_{SS} + 0.3V$		20	μA
I_{DD}, Dynamic	Outputs TRI-STATE $f_{IN} = 32$ kHz, $V_{DD} = 5.5V$ $V_{IH} = 2.0V$, $V_{IL} = 0.8V$		5	mA
Input Voltage				
Logical Low		0.0	0.8	V
Logical High		2.0	V_{DD}	V
Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$	−1	1	μA
Output Impedance	I/O and INTERRUPT OUT			
Logical Low	$V_{DD} = 4.5V$, $I_{OL} = 1.6$ mA		0.4	V
Logical High	$V_{DD} = 4.5V$, $I_{OH} = -400$ μA	2.4		V
	$I_{OH} = -10$ μA	0.8 V_{DD}		V
TRI-STATE	$V_{SS} \leq V_{OUT} \leq V_{DD}$	−1	1	μA
Output Impedance	$\overline{\text{RDY}}$ and $\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$ (Open Drain Devices)			
Logical Low, Sink	$V_{DD} = 4.5V$, $I_{OL} = 1.6$ mA		0.4	V
Logical High, Leakage	$V_{OUT} \leq V_{DD}$		10	μA

Functional Description (Continued)

TABLE I. REAL TIME COUNTER FORMAT

Counter Addressed		Units D0	D1	D2	D3	Max BCD Code	Tens D4	D5	D6	D7	Max BCD Code
1/10,000 of Seconds	(00_H)	-	-	-	-	0	D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	-	-	2
Day of the Week	(05_H)	D0	D1	D2	-	7	-	-	-	-	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	-	-	3
Month	(07_H)	D0	D1	D2	D3	9	D4	-	-	-	1

(−) indicates unused bits

Functional Description (Continued)

TABLE II. ADDRESS CODES AND FUNCTIONS

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter—Ten Thousandths of Seconds
0	0	0	0	1	Counter—Hundredths and Tenths of Seconds
0	0	0	1	0	Counter—Seconds
0	0	0	1	1	Counter—Minutes
0	0	1	0	0	Counter—Hours
0	0	1	0	1	Counter—Day of Week
0	0	1	1	0	Counter—Day of Month
0	0	1	1	1	Counter—Month
0	1	0	0	0	RAM—Ten Thousandths of Seconds
0	1	0	0	1	RAM—Hundredths and Tenths of Seconds
0	1	0	1	0	RAM—Seconds
0	1	0	1	1	RAM—Minutes
0	1	1	0	0	RAM—Hours
0	1	1	0	1	RAM—Day of Week
0	1	1	1	0	RAM—Day of Month
0	1	1	1	1	RAM—Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counters Reset
1	0	0	1	1	RAM Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	GO Command
1	0	1	1	0	$\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$
1	1	1	1	1	Test Mode

All others unused

Functional Description (Continued)

The comparator is a cascaded exclusive NOR. Its output is latched 61 μs after the rising edge of the 1 kHz clock signal (input to the ten thousandths of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the thousandths of seconds counter should not be included in a compare because of the possibility of having a ripple delay greater than 61 μs. (For output timing see Interrupt Timing.)

Power Down Mode

The $\overline{\text{POWER DOWN}}$ input is essentially a second chip select. It disables all inputs and outputs except for the $\overline{\text{STANDBY INTERRUPT}}$. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain timekeeping and turn on the $\overline{\text{STANDBY INTERRUPT}}$ if programmed to do so. (The programming must be done before the $\overline{\text{POWER DOWN}}$ input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the $\overline{\text{POWER DOWN}}$ input should go to a logical zero at least 1 μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the $\overline{\text{POWER DOWN}}$ input back to a logical one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing all 1's (FF) at address 12_H or 13_H respectively.

A write pulse at address 15_H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This GO command is used for precise starting of the clock. The data on the data bus is ignored during the write. If the seconds counter is at a value greater than 39 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute.

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The status bit is set if this 1 kHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14_H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14_H will reset the status bit.

Oscillator

The oscillator used is the standard Pierce parallel resonant oscillator. Externally, 2 capacitors, a 20 MΩ resistor and the crystal are required. The 20 MΩ resistor is connected between OSC IN and OSC OUT to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200 kΩ. The capacitor values should be typically 20 pF–25 pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input levels should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, and $\overline{\text{CHIP SELECT}}$ signals are active low inputs. The $\overline{\text{READY}}$ signal is an open drain output. At the start of each read or write cycle the $\overline{\text{READY}}$ line (open drain) will pull low and will remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a write. $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ must be accompanied by a $\overline{\text{CHIP SELECT}}$ (see *Figures 3 and 4* for read and write cycle timing).

During a read or write, address bits must not change while chip select and control strobes are low.

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 kHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at $1F_H$.

Functional Description (Continued)

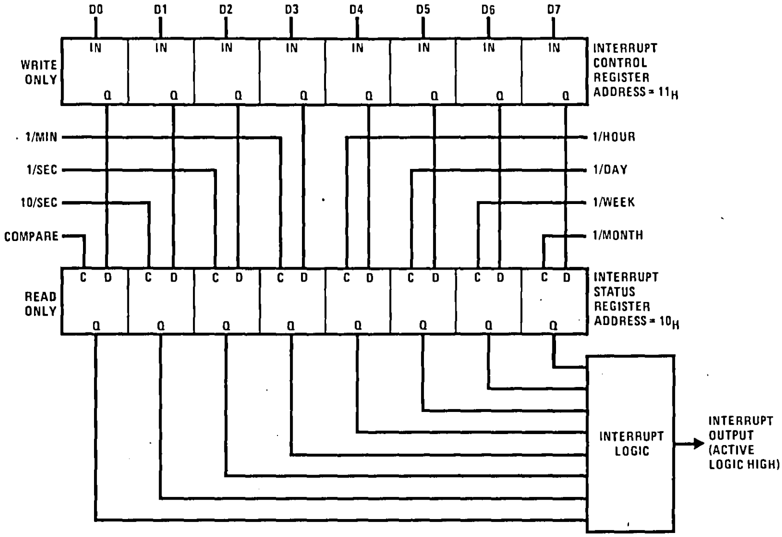
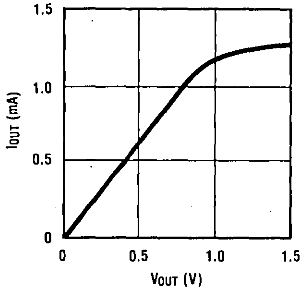


FIGURE 1. Interrupt Register Format

Standby Interrupt Typical Characteristics



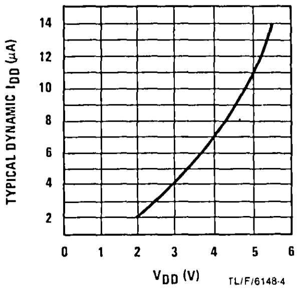


FIGURE 2. Typical Supply Current vs Supply Voltage During Power Down

Interrupt Timing $-40°C \leq T_A \leq 85°C$, $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$

Parameter		Min	Max	Units
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	μs
t_{SBYON}	Compare Valid to $\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$ (Pin 14) Low (Note 1)		5	μs
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	μs
t_{SBYOFF}	Trailing Edge of Write Cycle (D0 = 0; Address = 16_H) to $\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$ Off (High Impedance State)		5	μs

Note 1: The status register clocks are: the corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61 μs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing $-40°C \leq T_A \leq 85°C$, $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$

Parameter		Min	Max	Units
t_{AR}	Address Bus Valid to Read Strobe	100		ns
t_{CSR}	Chip Select to Read Strobe	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns
t_{RYDV}	Rising Edge of Ready to Data Valid		100	ns

Note 2: If $t_{AR} = 0$ and Chip Select, Address Valid or Read are coincident then they must exist for 1050 ns.

Write Cycle Timing $-40°C \le T_A \le 85°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

	Parameter	Min	Max	Units
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready Strobe Width		800	ns
t_{RYH}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	110		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Note 3: If data changes while $\overline{CS}$ and $\overline{WR}$ are low, then they must remain coincident for 1050 ns after the data change to ensure a valid write.
Data bus loading is 100 pF.
Ready output loading is 50 pF and 3 kΩ pull-up.
Input and output AC timing levels:
Logical one = 2.0V
Logical zero = 0.8V

Read and Write Cycle Timing Diagrams

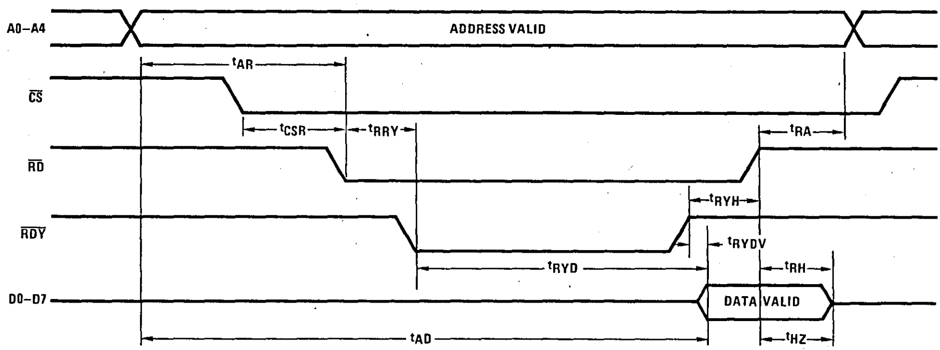


FIGURE 3. Read Cycle Timing

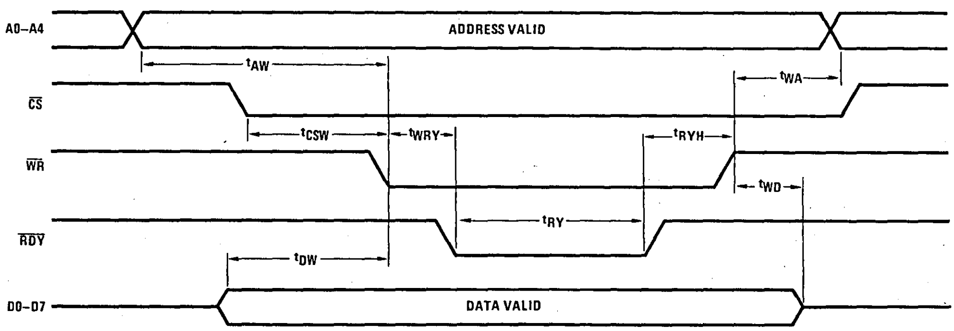
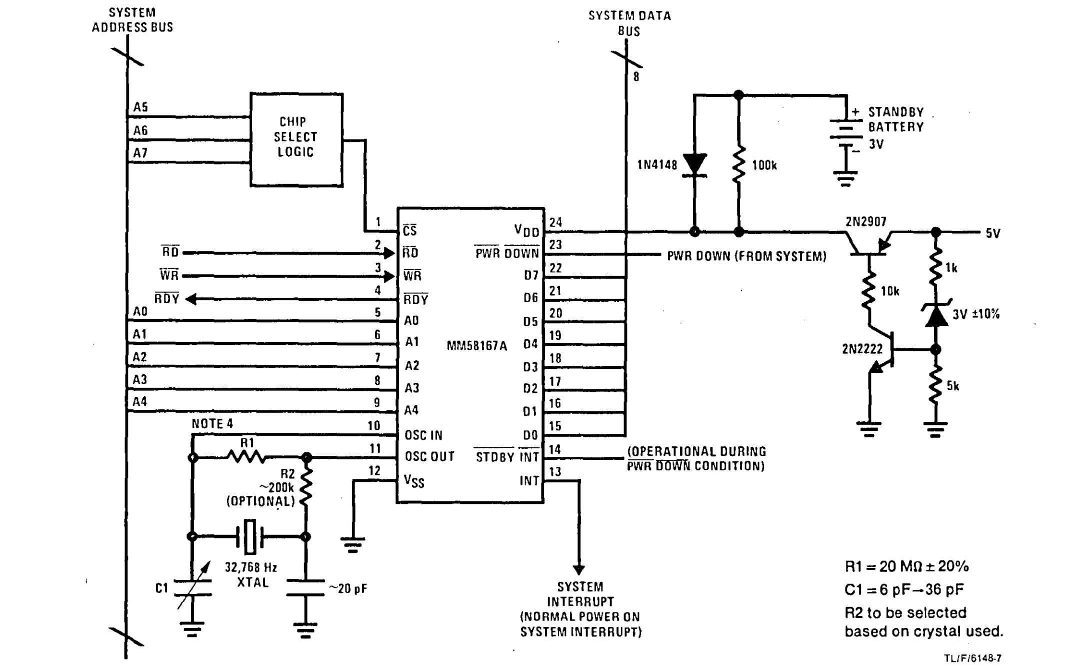


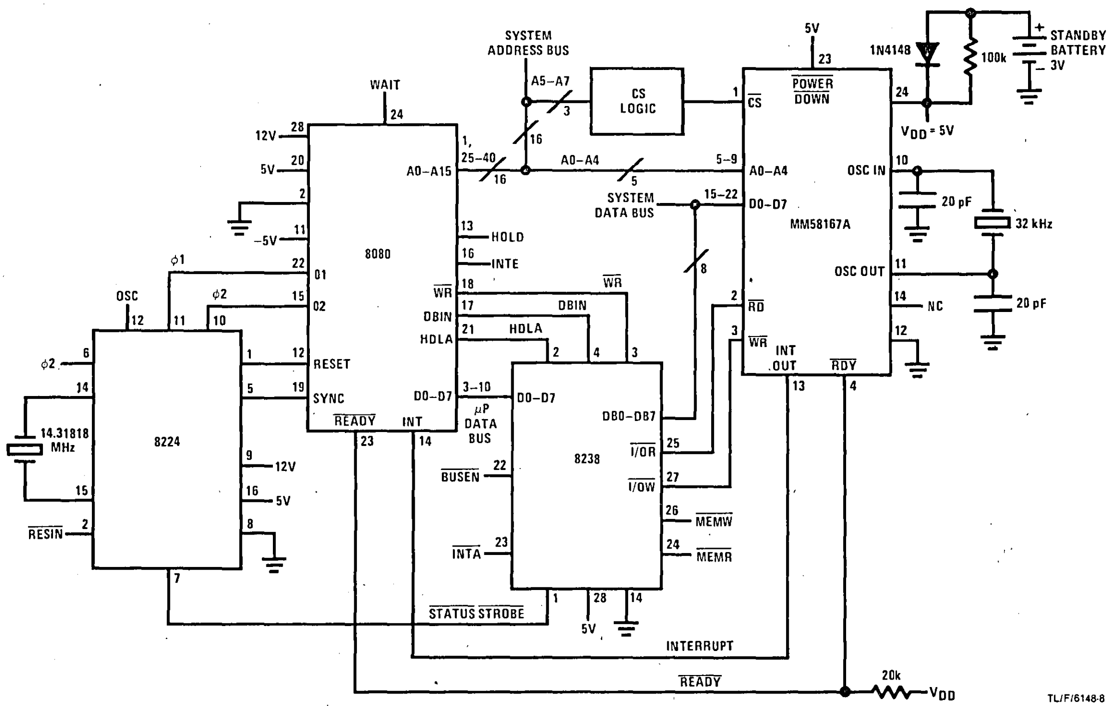
FIGURE 4. Write Cycle Timing

Typical Applications



Note 4: A ground line or ground plane guard trace should be included between pins 9 and 10 to insure the oscillator is not disturbed by the address line.

FIGURE 5. Typical Connection Diagram



Note 5: Must use 8238 or equivalent logic to insure advanced I/OW pulse; so that the ready output of the MM58167A is valid by the end of $\phi 2$ during the T2 microcycle.

Note 6: $t_{\phi 2} \geq t_{RS8080} + t_{DL8238} + t_{WRY58167A}$.

FIGURE 6. 8080 System Interface with Battery Backup

Block Diagram

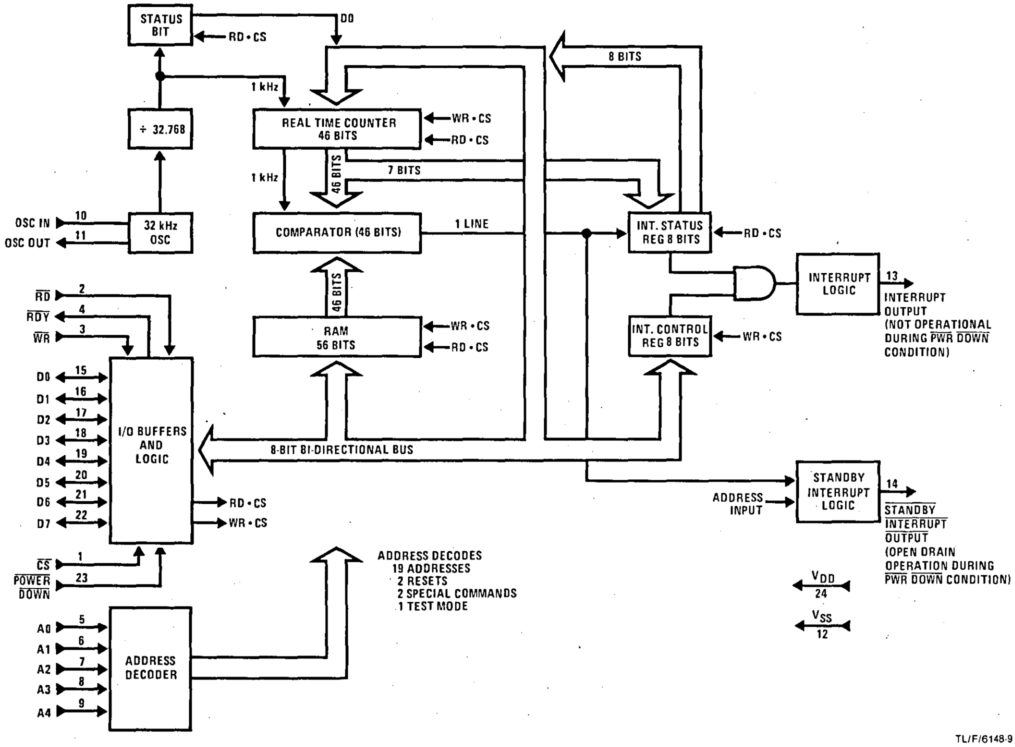


FIGURE 7

National Semiconductor

MM58174A Microprocessor-Compatible Real-Time Clock

General Description

The MM58174A is a low-threshold metal-gate CMOS circuit that functions as a real-time clock and calendar in bus-oriented microprocessor systems. The device includes an interrupt timer which may be programmed to one of three times. Time-keeping is maintained down to 2.2V to allow low power standby battery operation. The timebase is generated from a 32768 Hz crystal-controlled oscillator.

Features

- Microprocessor compatible
- Tenths of seconds, seconds, tens of seconds, minutes, tens of minutes, day of week, days, tens of days, months, tens of months, independent registers
- Automatic leap year calculation
- Internal pull-ups to safeguard data
- Protection for read during data changing
- Independent interrupt system with open drain output
- TTL compatible
- Low power standby operation (2.2V, 10μA)
- Low cost internally biased oscillator
- Low cost 16-pin dual-in-line package
- Available for commercial and military temperature ranges

Applications

- Point-of-sale terminals
- Word processors
- Teller terminals
- Event recorders
- Microprocessor-controlled instrumentation
- Microprocessor time clock
- TV/VCR reprogramming
- Intelligent telephone

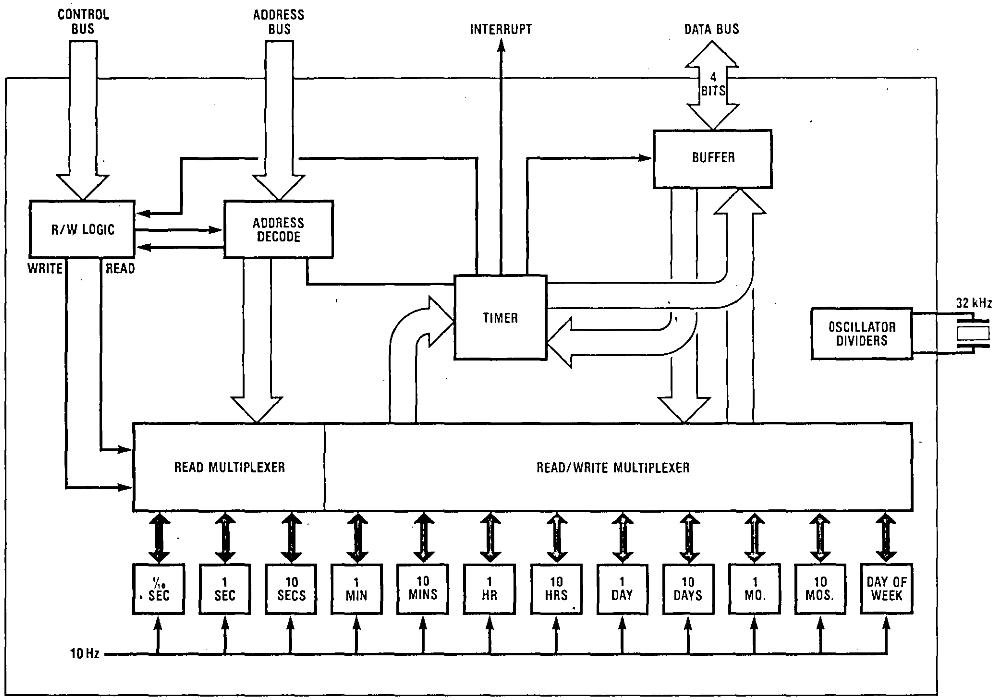


Figure 1. Block Diagram

Absolute Maximum Ratings

Voltage at All Inputs and Outputs	$V_{DD}+0.3$ to $V_{SS}-0.3$
Operating Temperature	
MM58174AN	−40°C to +85°C
Storage Temperature	−65°C to +150°C
$V_{DD}-V_{SS}$	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{SS}=0V$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	Standby mode (no READ or WRITE instructions)	2.2		5.5	V
		Operational mode	4		5.5	V
I_{DD}	Supply Current	$V_{DD}=2.2V$ (Standby) MM58174AN			10	μA
		$V_{DD}=5V$ (Operating)			1	mA
	Input Logic Levels For Signals: AD_0-AD_3, DB_0-DB_3, WR, RD, CS	$V_{DD}=5V$				
	Logic "1"		2			V
	Logic "0"				0.8	V
	Input Capacitance				10	pF
	Input Current Levels	$V_{DD}=5V$				
	Current to V_{SS} For Signals: AD_0-AD_3, DB_0-DB_3, RD	$V_{IN}=V_{DD}$			30	μA
	Internal Resistor to V_{DD} For Signals:					
	WR		30	100		kΩ
	CS		30	100		kΩ
	Output Logic Levels For Signals: DB_0-DB_3	$V_{DD}=5V$				
	Logic "1"	$I_{OH}=0.1mA$	2.4			V
	Logic "0"	$I_{OL}=1.6mA$			0.4	V
	INTERRUPT (Open Drain) Logic "0"	For $I_{DS}=-1.6$ mA			0.4	V
	Off Leakage	$V_{OUT}=5V$			5	μA

Functional Description

The MM58174 is a microprocessor bus-oriented real-time clock. The circuit includes addressable real-time counters for tenths of seconds through months and a write only register for leap year calculation. The counters are arranged as bytes of four bits each. When addressed a byte will appear on the data I/O bus so that each word can be accessed independently. If any byte does not contain four bits (e.g. days of the week uses only 3 bits), the unused bits will be unrecognized during a write operation and tied to V_{SS} during a read operation.

The addressable reset latch causes the pre-scaler, tenths of seconds, seconds, and tens of seconds to be held in a reset condition. If a register is updated during a read operation the I/O data is prevented from updating and a subsequent read will return the illegal b.c.d. code '1111'. The interrupt timer may be programmed for intervals of 0.5 second, 5 seconds, or 60 seconds and may be coded as a single or repeated operation. The open drain interrupt output is pulled to V_{SS} when the timer times out and reading the interrupt register provides the internal selected information.

Circuit Description

The block diagram shown in Figure 1 shows the structure of the CMOS clock chip. A 16-pin DIL package is used.

Crystal Oscillator

This consists of a CMOS inverter/amplifier with on-chip bias resistor and capacitors. A single 6-36 pF trimmer is all that is required to fine tune the crystal (see Figure 2). However, for improved stability, some crystals may require a capacitor of typical value 20pF to be added between pin 14 and ground. The output of the oscillator is blocked by the start/stop F/F.

Non-Integer Divider

This counter divides the incoming 32,768 Hz frequency by 15/16 down to 30,720 Hz.

Fixed Divider (512)

This is a standard 9-stage binary ripple counter. Output frequency is 60 Hz. This counter is reset to zero by start/stop F/F.

Fixed Divider (6)

This is a 3-stage Johnson counter with a 10 Hz output signal. This counter is reset to zero state by the start/stop F/F.

Synchronization Stage

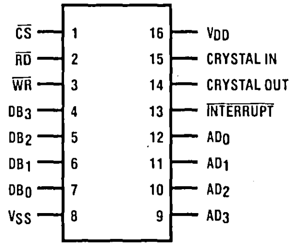
Both 10 Hz and 32,768 Hz clocks are fed into this section. It is used to generate a pulse of 15.25 μs width on the rising edge of each 10 Hz pulse.

This pulse is used to increment all the seconds, minutes, hours, days, months, and year counter and also to set the data changed F/F.

Data Changed F/F

This is set by the rising edge of each 10 Hz pulse to indicate that the clock value has changed since the last read operation. It is reset by any clock read command.

Connection Diagram



Top View

Order Number MM58174AN
See NS Package N16E

The flip-flop sets all data bus bits to a "1" during RD time indicating that a register has been updated. This transient condition may occur at the end of the Read Data strobe. Hence, invalid data may still be read from the clock, if the strobe width was less than 3 μs.

The possibility may be overcome by implementing a further read of the tenths of seconds register at the end of every series of reads (starting with a read at the tenths of seconds register) and checking for unchanged data.

Seconds Counters

There are three counters for Seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds

The outputs of all three counters can be separately multiplexed on to the command 4-bit output bus. Table 1 shows the address decoding for each counter. All three counters are reset to zero by the start/stop F/F.

Minutes Counters

There are two Minutes counters:

a) units of minutes

b) tens of minutes

Both counters are parallel loaded with data from the 4-bit input bus when addressed by the microprocessor and a Write Data Strobe pulse given. Similarly, the output of both counters can be read separately onto the common 4-bit output bus (Table 1).

Hours Counters

There are two Hours counters which will count in a 24-hour mode:

a) units of hours

b) tens of hours

Both counters have identical parallel load and read multiplex features to the Minutes counters.

Seven Day Counter

There is a 7-state counter which increments every 24 hours. It will have identical parallel load and read multiplex capabilities to the Minutes and Hours counters. The counter counts cyclically from 1-7.

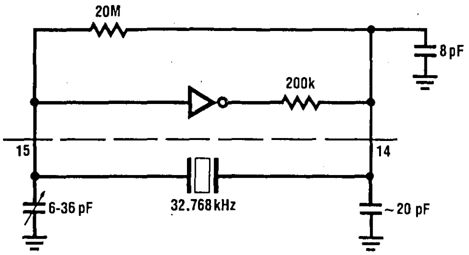


Figure 2. Crystal Oscillator

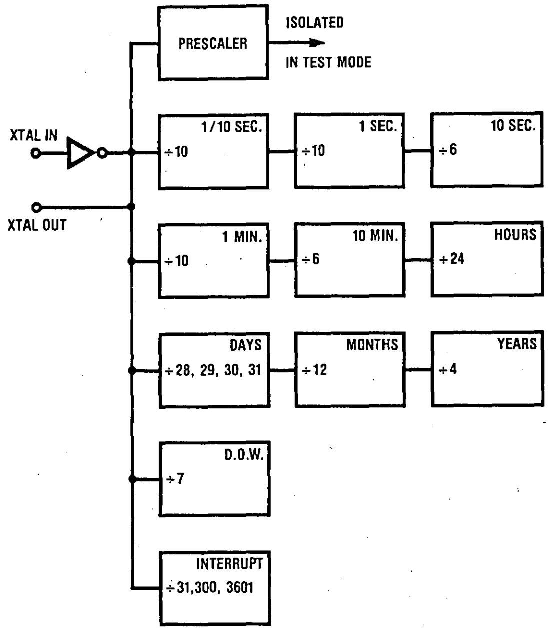


Figure 3. Test Mode Organization

Days Counter

There are two Days counters:

a) units of days

b) tens of days

The Days counters will count up to 28, 29, 30, or 31 days depending on the state of the Months counters and the Years Status Register. Days counters have parallel load and read multiplex capabilities.

Months Counters

There are two Months counters:

a) units of months

b) tens of months

The Months counters have parallel load and read multiplex capabilities.

Years Status Register

The Years Status register is a shift register of 4 bits. It will be shifted every year on December 31st. The status register must be set in accordance with Table 3. No readout capability is provided.

Chip Select ($\overline{CS}$)

An external chip select is provided. The chip enable is active low.

Counter and Register Selection

Table 1 shows the coding on the address lines AD_0–AD_3 which select the registers in the circuit to be either parallel loaded or read on to the output bus.

Start/Stop (Reset) Latch

A logic "1" on DB_0 at chip address 14 (E) will start the clock running, a logic "0" will stop the clock. This function allows the loading of time data into the clock and its precise starting. The clock starts at 0.1 seconds.

Test Mode

This mode is incorporated to facilitate production testing of the circuit. In this mode, the 32,768Hz clock is fed forward as shown in *Figure 3*. For normal operation, the circuit must be set to the non-test mode as part of the system initialization. This is accomplished by writing a logic "0" to DB_3 at AD_0.

Table 1. Address Decoding for Internal Registers

Selected Counter	Address Bits AD_3	AD_2	AD_1	AD_0	Mode
0 Test Only	0	0	0	0	Write Only
1 Tenths of secs.	0	0	0	1	Read Only
2 Units of secs.	0	0	1	0	Read Only
3 Tens of secs.	0	0	1	1	Read Only
4 Units of mins.	0	1	0	0	Read or Write
5 Tens of mins.	0	1	0	1	Read or Write
6 Units of hours	0	1	1	0	Read or Write
7 Tens of hours	0	1	1	1	Read or Write
8 Units of days	1	0	0	0	Read or Write
9 Tens of days	1	0	0	1	Read or Write
10 Day of week	1	0	1	0	Read or Write
11 Units of months	1	0	1	1	Read or Write
12 Tens of months	1	1	0	0	Read or Write
13 Years	1	1	0	1	Write Only
14 Stop/Start	1	1	1	0	Write Only
15 Interrupt	1	1	1	1	Read or Write

Table 2a. Interrupt Selection Data

Mode: Address 15, Write Mode				
Function	**DB_3**	**DB_2**	**DB_1**	**DB_0**
No Interrrupt	X	0	0	0
Int. at 60 sec. intervals*	0/1	1	0	0
Int. at 5.0 sec. intervals*	0/1	0	1	0
Int. at 0.5 sec. intervals*	0/1	0	0	1
* +16.6ms				

$DB_3 = 0$, single interrupt $DB_3 = 1$, repeated interrupt

Table 2b. Interrupt Read Back (Status)

Mode: Address 15, Read Mode				
Interrupt Status	**DB_3**	**DB_2**	**DB_1**	**DB_0**
Reset	X	0	0	0
60 sec. signal	X	1	0	0
5.0 sec. signal	X	0	1	0
0.5 sec. signal	X	0	0	1

X = don't care state

Table 3. Years Status Register

Mode: Address 13, Write Mode				
	DB_3	**DB_2**	**DB_1**	**DB_0**
Leap year	1	0	0	0
Leap year − 1	0	1	0	0
Leap year − 2	0	0	1	0
Leap year − 3	0	0	0	1

Note: Leap year counter rolls over on Dec. 31 @23:59:59

Interrupt System

The interrupt output and its frequency of operation is enabled by writing to address 15 (see Table 2a). To ensure correct operation, the interrupt should be serviced within 16.6 ms.

The interrupt is initialized by writing "0" to address 15 and reading the interrupt, i.e., reading at address 15 three times. Initialization must be performed at power on and also if the interrupt is not serviced correctly within 16.6 ms.

Servicing the Interrupt

In a typical system the open drain interrupt output is wired to the processor interrupt system. Hence, when the interrupt timer times out, the interrupt output is pulled low and the processor is interrupted.

The processor may then reset the interrupt by utilizing the following procedure:

Read Address 15 three times.

This resets the interrupt output and restarts the interrupt timer when in the repeat mode.

It is recommended that the interrupt output is connected to a unique processor port.

Crystal Parameters

Figure 4 is an electrical representation of the crystal along with some typical values. The 32.768 kHz crystal is an NT CUT (tuning fork type) or XY BAR for use in a parallel resonant Pierce oscillator.

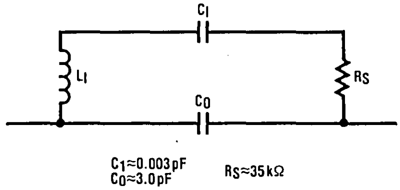


Figure 4. Typical Crystal Parameters

Device Initialization and Oscillator Setting

When first installed or if the battery back-up has failed, the MM58174A will require to be properly initialized. The following sequence is a suggested flow of operations to achieve this.

Action	Result
1) Apply power.	
2) Write '0' to address 15.	Clears interrupt timer chain.
3) Read 3 times from address 15.	Clears interrupt output logic.
4) Write '0' on DB3 to address 0.	Clears test mode.
5) Write '0' on DB0 to address 14.	Stops clock running.
6) Set up time-keeping registers.	Load real-time into device time registers, minutes to leap years.
7) Write '1' on DB0 to address 14.	Starts time-keeping synchronized to an external time source.
8) Program and start interrupts.	Commence interrupt timing, if so required.

Oscillator Setting

Directly connecting a frequency meter to the Crystal Out pin (14) will not allow correct frequency setting because of the extra capacitive loading of the meter. One possibility for setting is to use a high impedance probe or a CMOS buffer to keep the loading as low as possible (e.g., 100 × 2 pF probe). Alternatively, a buffered output of 16.384 kHz (OSC/2) can be produced on DB0 by applying the following procedure:

Action	Result
1) Write a '1' on DB3 to address 0.	Selects test mode.
2) Write a '1' on DB0 to address 14.	Starts clock timing.
3) Read at address 1 (tenths of secs).	'Data Changed' signal is read.
4) Read at address 1 and HOLD the strobe LOW.	16.384 kHz appears on DB0.
5) Adjust trimmer capacitor.	

There must be no extra activity on the $\overline{RD}$ line between steps 3 and 4 or only the normal 'Data Changed' signal will be observed on the data bus. Thus if the normal host processor system is being used to generate the chip waveforms, proper care must be taken.

Timing Waveforms

Read Mode

Figure 6 gives detailed timing for the transfer of data from peripheral to microprocessor. See Table 4.

All times are measured from (or to) valid logic "0" level = 0.8V or valid logic "1" level = 2.0V.

Write Mode

Figure 7 gives detailed timing for the transfer of data from Microprocessor to peripheral. See Table 5.

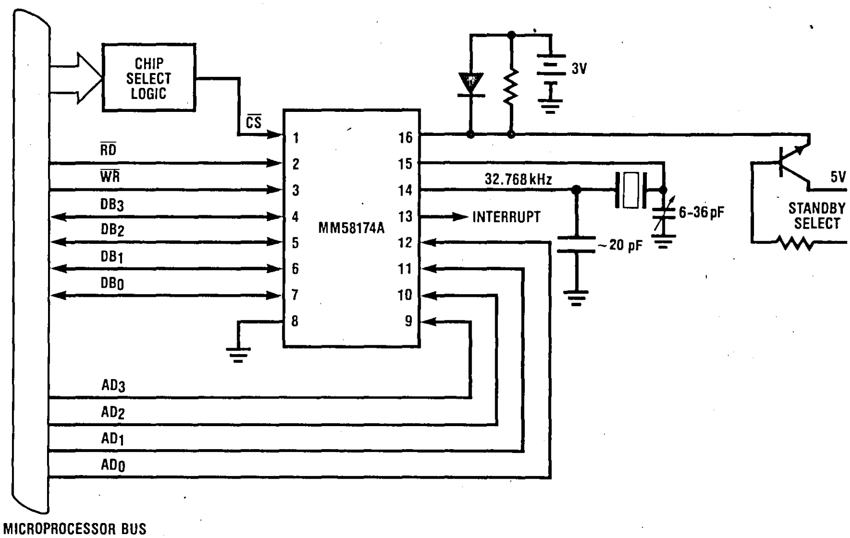


Figure 5. Typical Microprocessor Interface

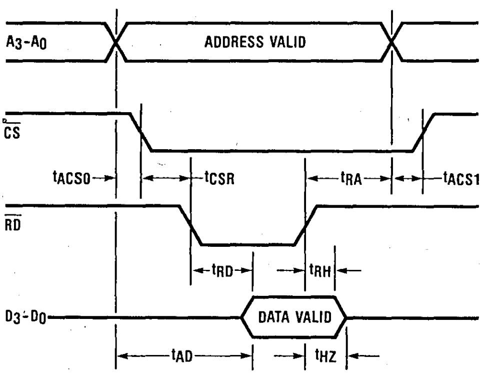


Figure 6. Read Cycle Waveforms

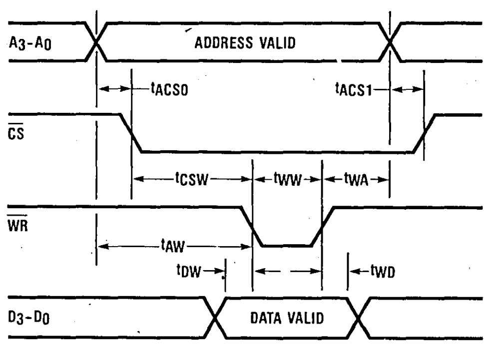


Figure 7. Write Cycle Waveforms

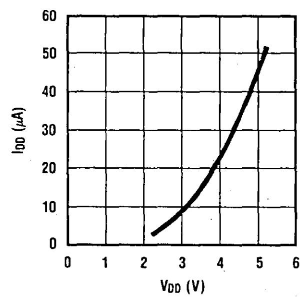


Figure 8. Typical Supply Current vs Supply Voltage During Power Down

Operating Conditions

MM58174AN $T_A = -40°C$ to $+85°C$
$V_{DD} = 5V$

Table 4. Timing: Data from Peripheral to Microprocessor

Symbol	Parameter	MM58174AN		Typ	Units	Comments
		Min	Max			
t_{ACS0}	Address Bus Valid to Chip Select ON ($\overline{CS} = 0$)	0			ns	
t_{CSR}	Chip Select ON to Read Strobe	0			ns	
t_{RD}	Read Cycle Access Time from Read Strobe to Data Bus Valid		900	450	ns	CL = 100 pF
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	0	330		ns	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	70		500	ns	
t_{ACS1}	Address Change to Chip Select OFF	0		40	ns	
t_{AD}	Address Bus Valid to Data Valid		1850	850	ns	CL = 100 pF
t_{HZ}	Time from Trailing Edge of Read Strobe until Interface Device Bus Drivers are in TRI-STATE® Mode	0	330		ns	
t_{RW}	Read Strobe Width		14		μs	
t_{AR}	Address Bus Valid to Read Strobe	500			ns	

Note 1: In order not to degrade timekeeping accuracy, the number of Read strobes in any one second should be less than 10,000.

Table 5. Timing: Data from Microprocessor to Peripheral

Symbol	Parameter	MM58174AN		Typ	Units	Comments
		Min	Max			
t_{ACS0}	Address Bus Valid to Chip Select ON ($\overline{CS} = 0$)	0			ns	
t_{CSW}	Chip Select ON to Write Strobe	0		450	ns	
t_{AW}	Address Bus Valid to Write Strobe	725			ns	
t_{WW}	Write Strobe Width	670			ns	
t_{DW}	Data Bus Valid Before Write Strobe	70			ns	
t_{WA}	Address Bus Hold Time Following Write Strobe	165			ns	
t_{WD}	Data Bus Hold Time Following Write Strobe	185			ns	
t_{ACS1}	Address Change to Chip Select OFF ($\overline{CS} = 1$)	0			ns	

Note 1: If address and write occur simultaneously, then they must exit for t_{AW} and t_{WW}.

National Semiconductor

MM58274 Microprocessor Compatible Real Time Clock

General Description

The MM58274 is fabricated using low threshold metal gate CMOS technology and is designed to operate in bus oriented microprocessor systems where a real time clock and calendar function are required. The on-chip 32.768 kHz crystal controlled oscillator will maintain timekeeping down to 2.2V to allow low power standby battery operation. This device is pin compatible with the MM58174 but continues timekeeping up to tens of years. Faster access times are also offered.

Applications

- Point of sale terminals
- Teller terminals
- Word processors
- Data logging
- Industrial process control

Features

- Same pin-out as MM58174A
- Timekeeping from tenths of seconds to tens of years in independently accessible registers
- Hours counter programmable for 12 or 24-hour operation
- Buffered crystal frequency output in test mode for easy oscillator setting
- Data-changed flag allows simple testing for time rollover
- Independent interrupting timer with open drain output
- Fully TTL compatible
- Low power standby operation (10 μA at 2.2V)
- Low cost 16-pin DIP

Block Diagram

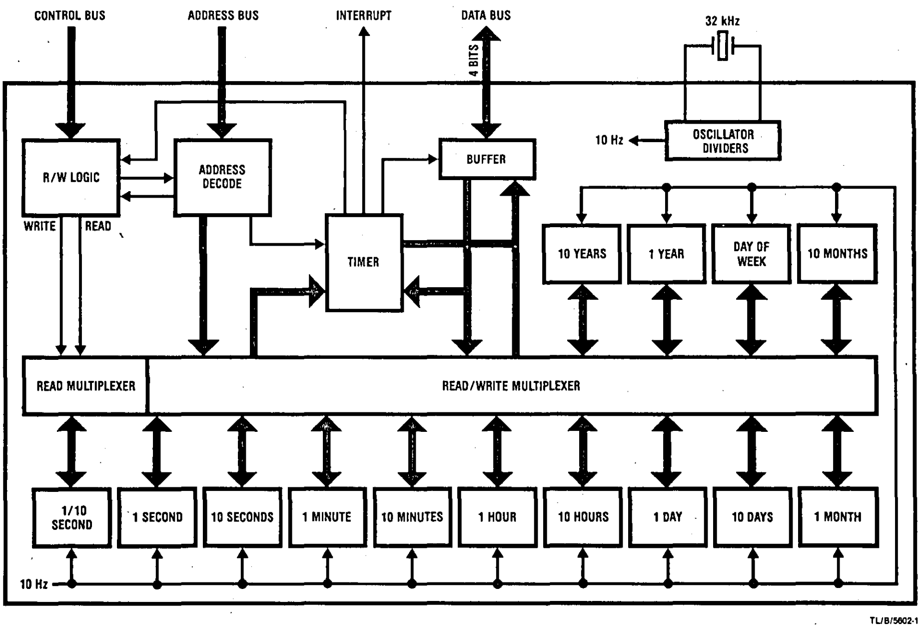


FIGURE 1

Absolute Maximum Ratings

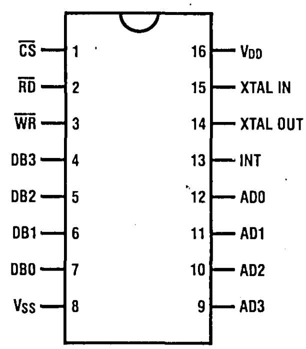
Voltage at All Inputs and Outputs	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Operating Temperature	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
$V_{DD}-V_{SS}$	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$ unless otherwise stated

Parameter	Conditions	Min	Typ	Max	Units
V_{DD}, Supply Voltage (Voltage at V_{DD} Pin)	Standby Mode (No Read or Write Instructions)	2.2			V
	Operational Mode	4.5		5.5	V
I_{DD}, Supply Current	Standby Mode ($V_{DD}=2.2V$)		4	10	μA
	Operational Mode ($V_{DD}=5V$)		1		mA
INPUT LOGIC LEVELS					
All Inputs (Except XTAL IN)	V_{IH} (Logic 1)	2.0			V
	V_{IL} (Logic 0)			0.8	V
	Input Capacitance			10	pF
INPUT CURRENT LEVELS (ACTIVE PULL-UPS TO V_{DD})					
AD0 to AD3 DB0 to DB3	$V_{IN}=V_{SS}$ $V_{DD}=5V$			20	μA
INTERNAL RESISTOR TO V_{DD}					
$\overline{WR}$		30	100		kΩ
$\overline{RD}$		30	100		kΩ
$\overline{CS}$		10	40		kΩ
OUTPUT LOGIC LEVELS					
DB0 to DB3	Logic 1 ($I_{OH}=0.2$ mA)	2.4			V
	Logic 0 ($I_{OL}=3.2$ mA)			0.4	V
Interrupt	Logic 0 ($I_{OL}=3.2$ mA)			0.4	V
	Off Leakage			2	μA

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/B/5602-2

FIGURE 2

Functional Description

The MM58274 is a bus oriented microprocessor real time clock. It has the same pin-out as the MM58174A while offering extended timekeeping up to units and tens of years. To enhance the device further, a number of other features have been added including: 12 or 24 hours counting, a testable data-changed flag giving easy error-free time reading and simplified interrupt control.

A buffered oscillator signal appears on the interrupt output when the device is in test mode. This allows for easy oscillator setting when the device is initially powered up in a system.

The counters are arranged as 4-bit words and can be randomly accessed for time reading and setting. The counters output in BCD (binary coded decimal) 4-bit numbers. Any register which has less than 4 bits (e.g., days of week uses only 3 bits) will return a logic 0 on any unused bits. When written to, the unused inputs will be ignored.

Functional Description (Continued)

Writing a logic 1 to the clock start/stop control bit resets the internal oscillator divider chain and the tenths of seconds counter. Writing a logic 0 will start the clock timing from the nearest second. The time then updates every 100 ms with all counters changing synchronously. Time changing during a read is detected by testing the data-changed bit of the control register after completing a string of clock register reads.

Interrupt delay times of 0.1s, 0.5s, 1s, 5s, 10s, 30s or 60s can be selected with single or repeated interrupt outputs. The open drain output is pulled low whenever the interrupt timer times out and is cleared by reading the control register.

CIRCUIT DESCRIPTION

The block diagram in *Figure 1* shows the internal structure of the chip. The 16-pin package outline is shown in *Figure 2.*

Crystal Oscillator

This consists of a CMOS inverter/amplifier with an on-chip bias resistor. Externally a 20 pF capacitor, a 6 pF–36 pF trimmer capacitor and a crystal are required to complete the 32.768 kHz timekeeping oscillator circuit.

The 6 pF–36 pF trimmer fine tunes the crystal load impedance, optimizing the oscillator stability. When properly adjusted (i.e., to the crystal frequency of 32.768 kHz), the circuit will display a frequency variation with voltage of less than 3 ppm/V.

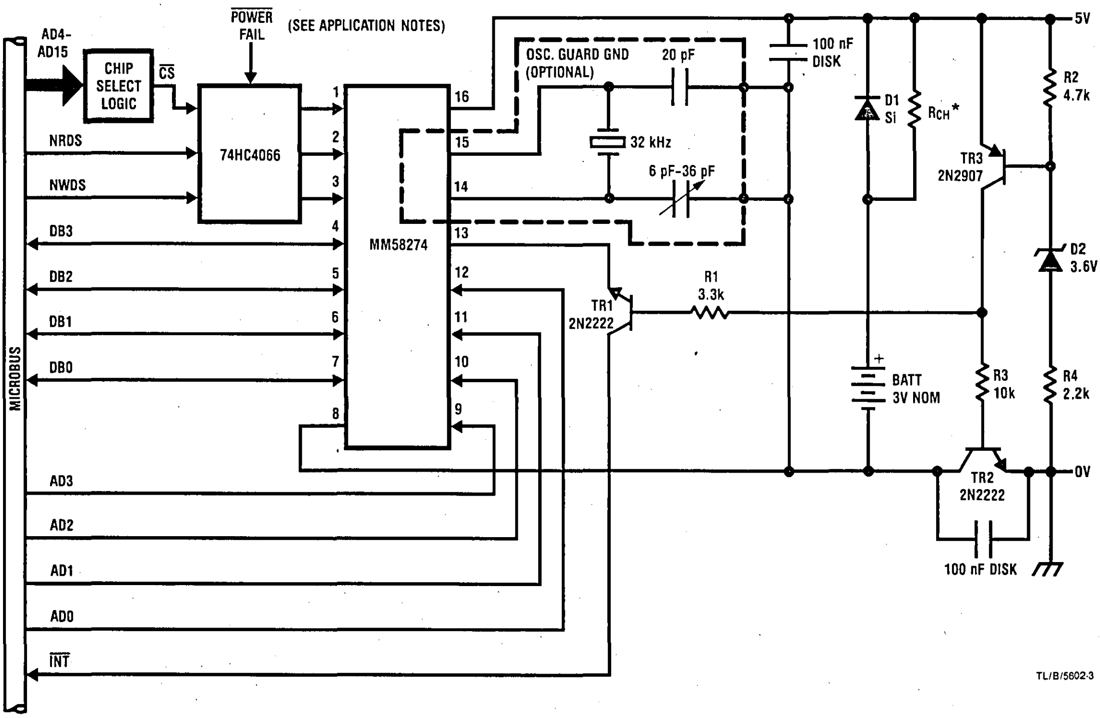
When the chip is enabled into test mode, the oscillator is gated onto the interrupt output pin giving a buffered oscillator output that can be used to set the crystal frequency when the device is installed in a system. For further information see the section on Test Mode.

Divider Chain

The crystal oscillator is divided down in three stages to produce a 10 Hz frequency setting pulse. The first stage is a non-integer divider which reduces the 32.768 kHz input to 30.720 kHz. This is further divided by a 9-stage binary ripple counter giving an output frequency of 60 Hz. A 3-stage Johnson counter divides this by six, generating a 10 Hz output. The 10 Hz clock is gated with the 32.768 kHz crystal frequency to provide clock setting pulses of 15.26 μs duration. The setting pulse drives all the time registers on the device which are synchronously clocked by this signal. All time data and the data-changed flag change on the falling edge of the clock setting pulse.

Data-Changed Flag

The data-changed flag is set by the clock setting pulse to indicate that the time data has been altered since the clock was last read. This flag occupies bit 3 of the control register where it can be tested by the processor to sense data-changed. It will be reset by a read of the control register. See the section, "Methods of Device Operation", for suggested clock reading techniques using this flag.



*Resistor is only used with NI-CAD cells. Omit for lithium, silver or other primary cells.

FIGURE 3. Typical System Connection Diagram

Functional Description (Continued)

Seconds Counters

There are three counters for seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds.

The registers are accessed at the addresses shown in Table I. The tenths of seconds register is reset to 0 when the clock start/stop bit (bit 2 of the control register) is set to logic 1. The units and tens of seconds are set up by the processor, giving time setting to the nearest second. All three registers can be read by the processor for time output.

Minutes Counters

There are two minutes counters:

a) units of minutes

b) tens of minutes.

Both registers may be read to or written from as required.

Hours Counters

There are two hours counters:

a) units of hours

b) tens of hours.

Both counters may be accessed for read or write operations as desired.

In 12-hour mode, the tens of hours register has only one active bit and the top three bits are set to logic 0. Data bit 1 of the clock setting register is the AM/PM indicator; logic 0 indicating AM, logic 1 for PM.

When 24-hour mode is programmed, the tens of hours register reads out two bits of data and the two most significant bits are set to logic 0. There is no AM/PM indication and bit 1 of the clock setting register will read out a logic 0.

In both 12/24-hour modes, the units of hours will read out four active data bits. 12 or 24-hour mode is selected by bit 0 of the clock setting register; logic 0 for 12-hour mode, logic 1 for 24-hour mode.

Days Counters

There are two days counters:

a) units of days

b) tens of days.

The days counters will count up to 28, 29, 30 or 31 depending on the state of the months counters and the leap year counter. The microprocessor has full read/write access to these registers.

Months Counters

There are two months counters:

a) units of months

b) tens of months.

Both these counters have full read/write access.

Years Counters

There are two years counters:

a) units of years

b) tens of years.

Both these counters have full read/write access. The years will count up to 99 and roll over to 00.

TABLE I. ADDRESS DECODING OF REAL-TIME CLOCK INTERNAL REGISTERS

Register Selected		Address (Binary) AD3	AD2	AD1	AD0	(Hex)	Access
0	Control Register	0	0	0	0	0	Split Read and Write
1	Tenths of Seconds	0	0	0	1	1	Read Only
2	Units Seconds	0	0	1	0	2	R/W
3	Tens Seconds	0	0	1	1	3	R/W
4	Units Minutes	0	1	0	0	4	R/W
5	Tens Minutes	0	1	0	1	5	R/W
6	Units Hours	0	1	1	0	6	R/W
7	Tens Hours	0	1	1	1	7	R/W
8	Units Days	1	0	0	0	8	R/W
9	Tens Days	1	0	0	1	9	R/W
10	Units Months	1	0	1	0	A	R/W
11	Tens Months	1	0	1	1	B	R/W
12	Units Years	1	1	0	0	C	R/W
13	Tens Years	1	1	0	1	D	R/W
14	Day of Week	1	1	1	0	E	R/W
15	Clock Setting/ Interrupt Registers	1	1	1	1	F	R/W

Functional Description (Continued)

Day of Week Counter

The day of week counter increments as the time rolls from 23:59 to 00:00 (11:59 PM to 12:00 AM in 12-hour mode). It counts from 1 to 7 and rolls back to 1. Any day of the week may be specified as day 1.

Clock Setting Register/Interrupt Register

The interrupt select bit in the control register determines which of these two registers is accessible to the processor at address 15. Normal clock and interrupt timing operations will always continue regardless of which register is selected onto the bus. The layout of these registers is shown in Table II.

The clock setting register is comprised of three separate functions:

a) leap year counter: bits 2 and 3

b) AM/PM indicator: bit 1

c) 12/24-hour mode set: bit 0 (see Table IIA).

The leap year counter is a 2-stage binary counter which is clocked by the months counter. It changes state as the time rolls over from 11:59 on December 31 to 00:00 on January 1.

The counter should be loaded with the 'number of years since last leap year' e.g., if 1980 was the last leap year, a clock programmed in 1983 should have 3 stored in the leap year counter. If the clock is programmed during a leap year, then the leap year counter should be set to 0. The contents of the leap year counter can be read by the μP.

The AM/PM indicator returns a logic 0 for AM and a logic 1 for PM. It is clocked when the hours counter rolls from 11:59 to 12:00 in 12-hour mode. In 24-hour mode this bit is set to logic 0.

The 12/24-hour mode set determines whether the hours counter counts from 1 to 12 or from 0 to 23. It also controls the AM/PM indicator, enabling it for 12-hour mode and forcing it to logic 0 for the 12-hour mode. The 12/24-hour mode bit is set to logic 0 for 12-hour mode and it is set to logic 1 for 24-hour mode.

IMPORTANT NOTE: *Hours mode and AM/PM bits cannot be set in the same write operation. See the section on* Initialization (Methods of Device Operation) *for a suggested setting routine.*

All bits in the clock setting register may be read by the processor.

The interrupt register controls the operation of the timer for interrupt output. The processor programs this register for single or repeated interrupts at the selected time intervals.

The lower three bits of this register set the time delay period that will occur between interrupts. The time delays that can be programmed and the data words that select these are outlined in Table IIB.

Data bit 3 of the interrupt register sets for either single or repeated interrupts; logic 0 gives single mode, logic 1 sets for repeated mode.

Using the interrupt is described in the Device Operation section.

TABLE IIA. CLOCK SETTING REGISTER LAYOUT

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 Indicates a Leap Year	R/W
AM/PM Indicator (12-Hour Mode)			X		0 = AM 1 = PM 0 in 24-Hour Mode	R/W
12/24-Hour Select Bit				X	0 = 12-Hour Mode 1 = 24-Hour Mode	R/W

TABLE IIB. INTERRUPT CONTROL REGISTER

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt output cleared, start/stop bit set to 1.	X	0	0	0
0.1 Second		0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second	DB3 = 0 for single interrupt DB3 = 1 for repeated interrupt	0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1

Timing Accuracy: single interrupt mode (all time delays): ±1 ms
Repeated Mode: ±1 ms on initial timeout, thereafter synchronous with first interrupt (i.e., timing errors do not accumulate).

Functional Description (Continued)

Control Register

There are three registers which control different operations of the clock:

a) the clock setting register

b) the interrupt register

c) the control register.

The clock setting and interrupt registers both reside at address 15, access to one or the other being controlled by the interrupt select bit; data bit 1 of the control register.

The clock setting register programs the timekeeping of the clock. The 12/24-hour mode select and the AM/PM indicator for 12-hour mode occupy bits 0 and 1, respectively. Data bits 2 and 3 set the leap year counter.

The interrupt register controls the operation of the interrupt timer, selecting the required delay period and either single or repeated interrupt.

The control register is responsible for controlling the operations of the clock and supplying status information to the processor. It appears as two different registers; one with write only access and one with read only access.

The write only register consists of a bank of four latches which control the internal processes of the clock.

The read only register contains two output data latches which will supply status information for the processor. Table III shows the mapping of the various control latches and status flags in the control register. The control register is located at address 0.

The write only portion of the control register contains four latches:

A logic 1 written into the test bit puts the device into test mode. This allows setting of the oscillator frequency as well as rapid testing of the device registers, if required. A more complete description is given in the Test Mode section. For normal operation the test bit is loaded with logic 0.

The clock start/stop bit stops the timekeeping of the clock and resets to 0 the tenths of seconds counter. The time of day may then be written into the various clock registers and the clock restarted synchronously with an external time source. Timekeeping is maintained thereafter.

A logic 1 written to the start/stop bit halts clock timing. Timing is restarted when the start/stop bit is written with a logic 0.

The interrupt select bit determines which of the two registers mapped onto address 15 will be accessed when this address is selected.

A logic 0 in the interrupt select bit makes the clock setting register available to the processor. A logic 1 selects the interrupt register.

The interrupt start/stop bit controls the running of the interrupt timer. It is programmed in the same way as the clock start/stop bit; logic 1 to halt the interrupt and reset the timer, logic 0 to start interrupt timing.

When no interrupt is programmed (interrupt control register set to 0), the interrupt start/stop bit is automatically set to a logic 1. When any new interrupt is subsequently programmed, timing will not commence until the start/stop bit is loaded with 0.

In the single interrupt mode, interrupt timing stops when a timeout occurs. The processor restarts timing by writing logic 0 into the start/stop bit.

In repeated interrupt mode the interrupt timer continues to count with no intervention by the processor necessary.

Interrupt timing may be stopped in either mode by writing a logic 1 into the interrupt start/stop bit. The timer is reset and can be restarted in the normal way, giving a full time delay period before the next interrupt.

In general, the control register is set up such that writing 0's into it will start anything that is stopped, pull the clock out of test mode and select the clock setting register onto the bus. In other words, writing 0 will maintain normal clock operation and restart interrupt timing, etc.

The read only portion of the control register has two status outputs:

Since the MM58274 keeps real time, the time data changes asynchronously with the processor and this may occur while the processor is reading time data out of the clock.

Some method of warning the processor when the time data has changed must thus be included. This is provided for by the data-changed flag located in bit 3 of the control register. This flag is set by the clock setting pulse which also clocks the time registers. Testing this bit can tell the processor whether or not the time has changed. The flag is cleared by a read of the control register but not by any write operations. No other register read has any effect on the state of the data-changed flag.

Data bit 0 is the interrupt flag. This flag is set whenever the interrupt timer times out, pulling the interrupt output low. In a polled interrupt routine the processor can test this flag to determine if the MM58274 was the interrupting device. This interrupt flag and the interrupt output are both cleared by a read of the control register.

TABLE III. THE CONTROL REGISTER LAYOUT

Access (addr0)	DB3	DB2	DB1	DB0
Read From:	Data-Changed Flag	0	0	Interrupt Flag
Write To:	Test 0 = Normal 1 = Test Mode	Clock Start/Stop 0 = Clock Run 1 = Clock Stop	Interrupt Select 0 = Clock Setting Register 1 = Interrupt Register	Interrupt Start/Stop 0 = Interrupt Run 1 = Interrupt Stop

Functional Description (Continued)

Both of the flags and the interrupt output are reset by the trailing edge of the read strobe. The flag information is held latched during a control register read, guaranteeing that stable status information will always be read out by the processor.

Interrupt timeout is detected and stored internally if it occurs during a read of the control register, the interrupt output will then go low only after the read has been completed.

A clock setting pulse occurring during a control register read will *not* affect the data-changed flag since time data read out before or after the control read will not be affected by the time change.

METHODS OF DEVICE OPERATION

Test Mode

National Semiconductor uses test mode for functionally testing the MM58274 after fabrication and again after packaging. Test mode can also be used to set up the oscillator frequency when the part is first commissioned.

Figure 4 shows the internal clock connections when the device is written into test mode. The 32.768 kHz oscillator is gated onto the interrupt output to provide a buffered output for initial frequency setting. This signal is driven from a TRI-STATE® output buffer, enabling easy oscillator setting in systems where interrupt is not normally used and there is no external resistor on the pin.

If an interrupt is programmed, the 32.768 kHz output is switched off to allow high speed testing of the interrupt timer. The interrupt output will then function as normal.

The clock start/stop bit can be used to control the fast clocking of the time registers as shown in *Figure 4*.

MM58274 Initialization

When it is first installed and power is applied, the device will need to be properly initialized. The following operation steps are recommended when the device is set up (all numbers are decimal):

1) Disable interrupt on the processor to allow oscillator setting. Write 15 into the control register: *The clock and interrupt start/stop bits are set to 1, ensuring that the clock and interrupt timers are both halted. Test mode and the interrupt register are selected.*

2) Write 0 to the interrupt register: *Ensure that there are no interrupts programmed and that the oscillator will be gated onto the interrupt output.*

3) Set oscillator frequency: *All timing has been halted and the oscillator is buffered out onto the interrupt line.*

4) Write 5 to the control register: *The clock is now out of test mode but is still halted. The clock setting register is now selected by the interrupt select bit.*

5) Set 12/24 Hours Mode: *Write to the clock setting register to select the hours counting mode required.*

6) Load Real-Time Registers: *All time registers (including Leap Years and AM/PM bit) may now be loaded in any order. Note that when writing to the clock setting register to set up Leap Years and AM/PM, the Hours Mode bit must not be altered from the value programmed in step 5.*

7) Write 0 to the control register: *This operation finishes the clock initialization by starting the time. The final control register write should be synchronized with an external time source.*

In general, timekeeping should be halted before the time data is altered in the clock. The data can, however, be altered at any time if so desired. Such may be the case if the user wishes to keep the clock corrected without having to stop and restart it; i.e., winter/summer time changing can be accomplished without halting the clock. This can be done in software by sensing the state of the data-changed flag and only altering time data just after the time has rolled over (data-changed flag set).

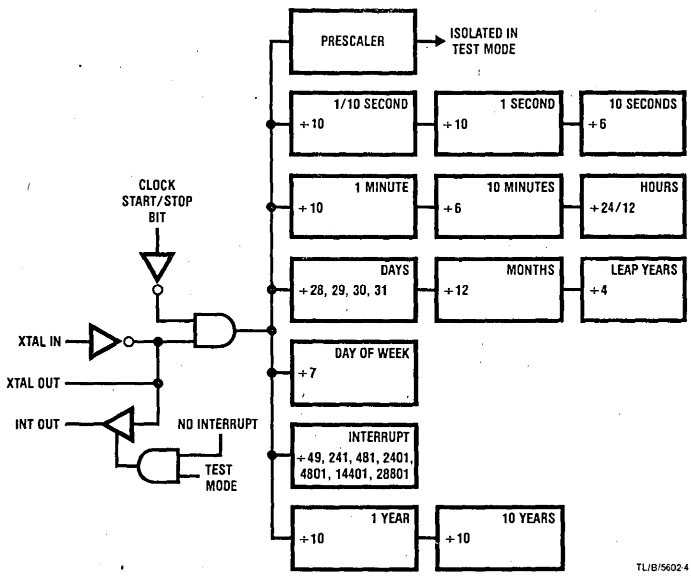


FIGURE 4. Test Mode Organization

Functional Description (Continued)

Reading the Time Registers

Using the data-changed flag technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1) Read the control register, address 0: *This is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.*

2) Read time registers: *All desired time registers are read out in a block.*

3) Read the control register and test DCF: *If DCF is cleared (logic 0), then no clock setting pulses have occurred since step 1. All time data is guaranteed good and time reading is complete.*

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may not be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

Interrupt Programming

The interrupt timer generates interrupts at time intervals which are programmed into the interrupt register. A single interrupt after delay or repeated interrupts may be programmed. Table IIB lists the different time delays and the data words that select them in the interrupt register.

Once the interrupt register has been used to set up the delay time and to select for single or repeat, it takes no further part in the workings of the interrupt system. All activity by the processor then takes place in the control register.

Initializing:

1) Write 3 to the control register (AD0): *Clock timing continues, interrupt register selected and interrupt timing stopped.*

2) Write interrupt control word to address 15: *The interrupt register is loaded with the correct word (chosen from Table IIB) for the time delay required and for single or repeated interrupts.*

3) Write 0 or 2 to the control register: *Interrupt timing commences. Writing 0 selects the clock setting register onto the data bus; writing 2 leaves the interrupt register selected. Normal timekeeping remains unaffected.*

On Interrupt:

Read the control register and test for Interrupt Flag (bit 0).

If the flag is cleared (logic 0), then the device is not the source of the interrupt.

If the flag is set (logic 1), then the clock did generate an interrupt. The flag is reset and the interrupt output is cleared by the control register read that was used to test for interrupt.

Single Interrupt Mode:

When appropriate, write 0 or 2 to the control register to restart the interrupt timer.

Repeated Interrupt Mode:

Timing continues, synchronized with the control register write which originally started interrupt timing. No further intervention is necessary from the processor to maintain timing.

In either mode interrupt timing can be stopped by writing 1 into the control register (interrupt start/stop set to 1). Timing for the full delay period recommences when the interrupt start/stop bit is again loaded with 0 as normal.

IMPORTANT NOTE: Using the interrupt timer places a constraint on the maximum Read Strobe width which may be applied to the clock. Normally all registers may be read from with a t_{RW} down to DC (i.e., $\overline{CS}$ and $\overline{RD}$ held continuously low). When the interrupt timer is active however, the maximum read strobe width that can be applied to the control register (Addr 0) is 30 ms.

This restriction is to allow the interrupt timer to properly reset when it times out. Note that it only affects reading of the control register—all other addresses in the clock may be accessed with DC read strobes, regardless of the state of the interrupt timer. Writes to any address are unaffected.

NOTES ON AC TIMING REQUIREMENTS

Although *Figures 5 and 6* show MICROBUS control signals used for clock access, this does not preclude the use of the MM58274 in other non-MICROBUS systems. *Figure 7* is a simplified logic diagram showing how the control signals are gated internally to control access to the clock registers. From this diagram it is clear that $\overline{CS}$ could be used to generate the internal data transfer strobes, with $\overline{RD}$ and $\overline{WR}$ inputs set up first. This situation is illustrated in *Figure 8.*

The internal data busses of the MM58274 are fully CMOS, contributing to the flexibility of the control inputs. When determining the suitability of any given control signal pattern for the MM58274, the timing specifications in Tables IV and V should be examined. As long as these timings are met (or exceeded) the MM58274 will function correctly.

When the MM58274 is connected to the system via a peripheral port, the freedom from timing constraints allows for very simple control signal generation, as in *Figure 9.* For reading (*Figure 9a),* Address, $\overline{CS}$ and $\overline{RD}$ may be activated simultaneously and the data will be available at the port after t_{AD}-max (700 ns). For writing (*Figure 9b*), the Address and data may be applied simultaneously and $\overline{CS}$ and $\overline{WR}$ strobed together.

Functional Description (Continued)

TABLE IV. READ TIMING: DATA FROM PERIPHERAL TO MICROPROCESSOR $V_{DD} = 5V \pm 0.5V$, $C_L = 100$ pF

Symbol	Parameter	Commercial Specification $T_A = -40°C$ to $+85°C$			Military Specification T_A – 55°C to +125°C			Units
		Min	Typ	Max	Min	Typ	Max	
t_{AD}	Address Bus Valid to Data Valid		550	700		550	775	ns
t_{CSD}	Chip Select On to Data Valid		250	375		250	425	ns
t_{RD}	Read Strobe On to Data Valid		250	375		250	425	ns
t_{RW}	Read Strobe Width (Note 1)			DC			DC	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	0			0			ns
t_{CSH}	Chip Select Hold Time from Trailing Edge of Read Strobe	0			0			ns
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	50	80	150	50	80	200	ns
t_{HZ}	Time from Trailing Edge of Read Strobe Until O/P Drivers are TRI-STATE	50	80	200	50	80	250	ns

TABLE V. WRITE TIMING: DATA FROM MICROPROCESSOR TO PERIPHERAL $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Commercial Specification $T_A = -40°C$ to $+85°C$			Military Specification T_A – 55°C to +125°C			Units
		Min	Typ	Max	Min	Typ	Max	
t_{AW}	Address Bus Valid to Write Strobe ↗ (Note 2)	650			750			ns
t_{CSW}	Chip Select On to Write Strobe ↗	350			450			ns
t_{DW}	Data Bus Valid to Write Strobe ↗	350			450			ns
t_{WW}	Write Strobe Width	350			450			ns
t_{WCS}	Chip Select Hold Time Following Write Strobe ↗	0			0			ns
t_{WA}	Address Bus Hold Time Following Write Strobe ↗	50			80			ns
t_{WD}	Data Bus Hold Time Following Write Strobe ↗	50			80			ns

Note 1: Except for special case restriction: with interrupts programmed, max read strobe width of control register (ADDR 0) is 30 ms. See section on Interrupt Programming.

Note 2: All timings measured to the trailing edge of write strobe (data latched by the trailing edge of $\overline{WR}$).

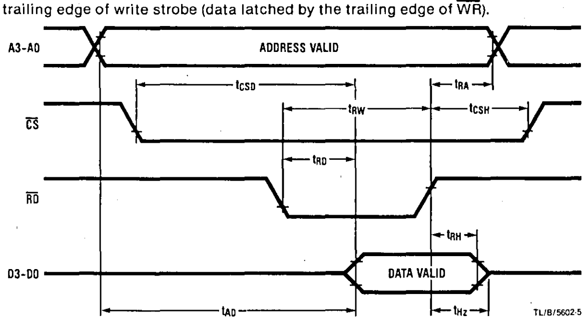


FIGURE 5. Read Cycle Timing

Functional Description (Continued)

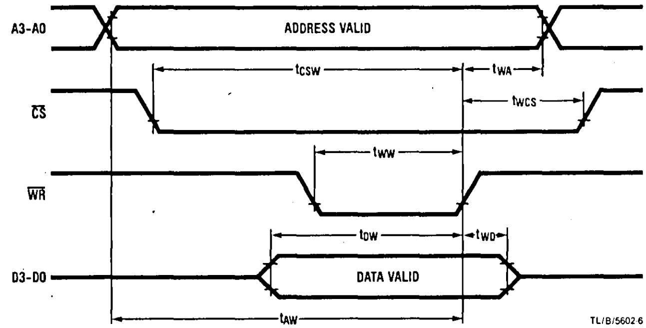


FIGURE 6. Write Cycle Timing

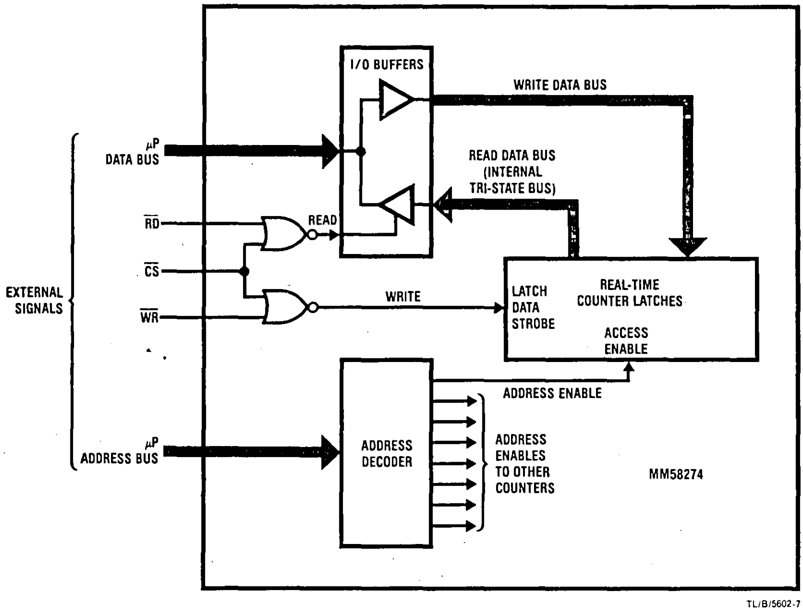


FIGURE 7. MM58274 Microprocessor Interface Diagram

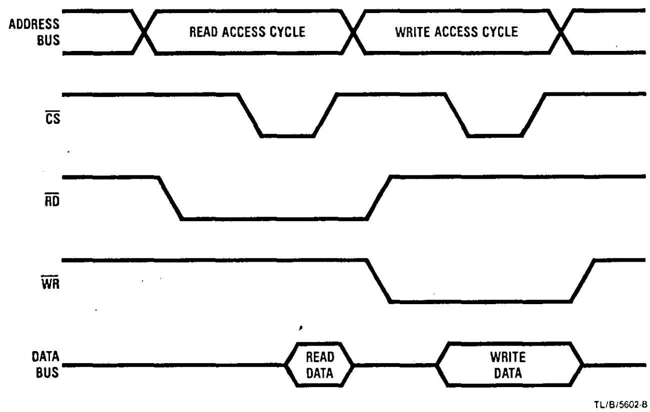
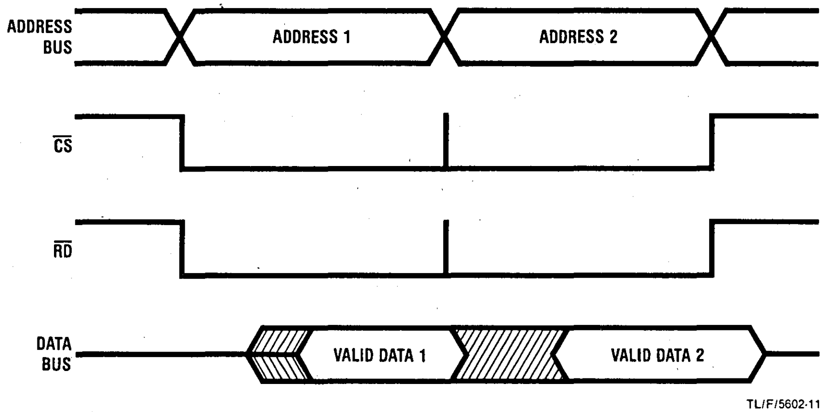
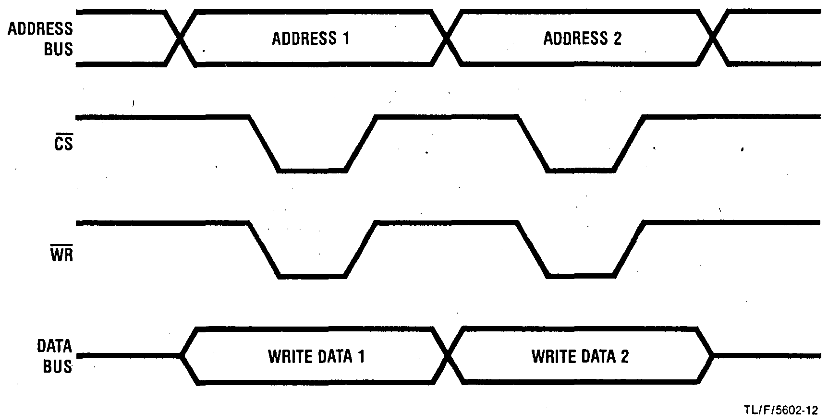


FIGURE 8. Valid MM58274 Control Signals Using Chip Select Generated Access Strobes

Functional Description (Continued)



a. Port Generated Read Access—2 Addresses Read Out



b. Port Generated Write Access—2 Addresses Written To

FIGURE 9. Simple Port Generated Control Signals

Functional Description (Continued)

APPLICATION NOTES

Time Reading Using Interrupt

In systems such as point of sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined in the section on methods of operation is ideal for this type of system. Some systems, however, need to sense a change in real time; e.g., industrial timers/process controllers, TV/VCR clocks, any system where real time is displayed.

The interrupt timer on the MM58274 can generate interrupts synchronously with the time registers changing, using software to provide the initial synchronization.

In single interrupt mode the processor is responsible for initiating each timing cycle and the timed period is accurate to ±1 ms.

In repeated interrupt mode the period from the initial processor start to the first timeout is also only accurate to ±1 ms. The following interrupts maintain accurate delay periods relative to the first timeout. Thus, to utilize interrupt to control time reading, we will use repeated interrupt mode.

In repeated mode the time period between interrupts is exact, which means that timeouts will always occur at the same point relative to the internal clock setting pulses. The case for 0.1s interrupts is shown in *Figure A-1*. The same is true for other delay periods, only there will be more clock setting pulses between each interrupt timeout. If we set up the interrupt timer so that interrupt always times out just after the clock setting pulse occurs (*Figure A-2*), then there is no need to test the data-changed flag as we know that the time data has just changed and will not alter again for another 100 ms.

This can be achieved as outlined below:

1) Follow steps 1 and 2 of the section on interrupt programming. In step 2 set up for repeated interrupt.

2) Read control register AD0: *This is a dummy read to reset the data-changed flag.*

3) Read control register AD0 until data-changed flag is set.

4) Write 0 or 2 to control register. Interrupt timing commences.

Time Reading with Very Slow Read Cycles

If a system takes longer than 100 ms to complete reading of all the necessary time registers (e.g., when CMOS processors are used or where high level interpreted language routines are used, then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

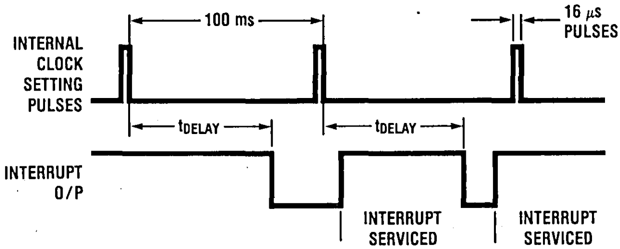
The technique below will detect both time changing *between* read strobes (i.e., between reading tens of minutes and units of hours) and also time changing *during* read, which can produce invalid data.

1) Read and store the value of the *lowest* order time register required.

2) Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.

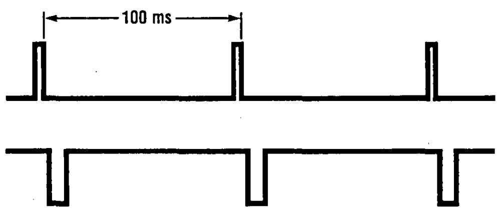
3) Read the lowest order register and compare it with the value stored previously in step 1. If it is still the same, then all time data is good. If it has changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads *must* both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no higher order register has changed either.



TL/B/5602-7

FIGURE A-1. Time Delay from Clock Setting Pulses to Interrupt Is Constant



TL/B/5602-8

FIGURE A-2. Interrupt Timer Synchronized with Clock Setting Pulses

3

National Semiconductor

PRELIMINARY

microCMOS

MM74HC942 300 Baud Modem

General Description

The MM74HC942 is a full duplex low speed modem. It provides a 300 baud bidirectional series interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC942 utilizes microCMOS Technology, 2 layers of polysilicon and 1 layer of metal P-well CMOS. Switched capacitor techniques are used to perform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600 Ω phone line. They can perform two to four wire conversion and drive the line at 0 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

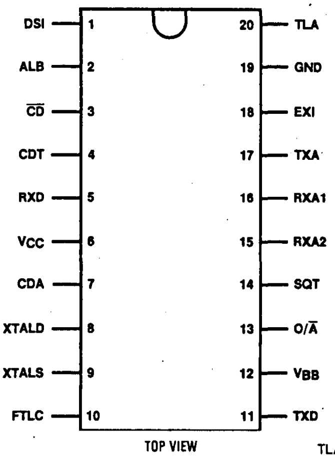
- Drives 600Ω at 0 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- ±5V supplies
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signalling systems
- Remote process control

Connection Diagram

Dual-In-Line Package



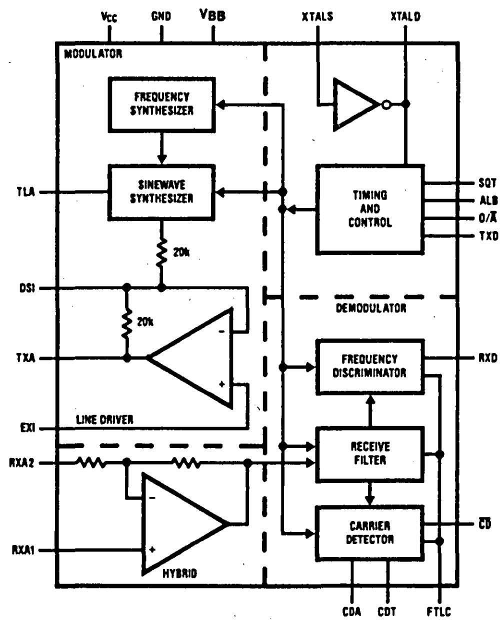
TOP VIEW

TL/F/5348-1

MM74HC942

Order Number MM74HC942J or MM74HC942N
See NS Package J20 or N20A

Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	-0.5 to $+7.0$V
Supply Voltage (V_{BB})	$+0.5$ to -7.0V
DC Input Voltage (V_{IN})	$V_{BB}-1.5$ to $V_{CC}+1.5$V
DC Output Voltage (V_{OUT})	$V_{BB}-0.5$ to $V_{CC}+0.5$V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to $+150$°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
Supply Voltage(V_{BB})	-4.5	-5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A) MM74HC	-40	$+85$	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

Symbol	Parameter	Conditions	T=25°C Typ	T=25°C Guaranteed Limits	74HC T=−40 to 85°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert=20\ \mu A$ $\lvert I_{OUT}\rvert=4.0$ mA, $V_{CC}=4.5$V	V_{CC}	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.7	V V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert=20\ \mu A$ $\lvert I_{OUT}\rvert=4.0$ mA, $V_{CC}=4.5$V		0.1 0.26	0.1 0.4	V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$, $V_{IL}=$GND ALB or SQT=GND Transmit Level = -9 dBm	8.0			mA
I_{CC}	Power Down Supply Current	ALB=SQT=V_{CC} $V_{IH}=V_{CC}$, $V_{IL}=$GND			250	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

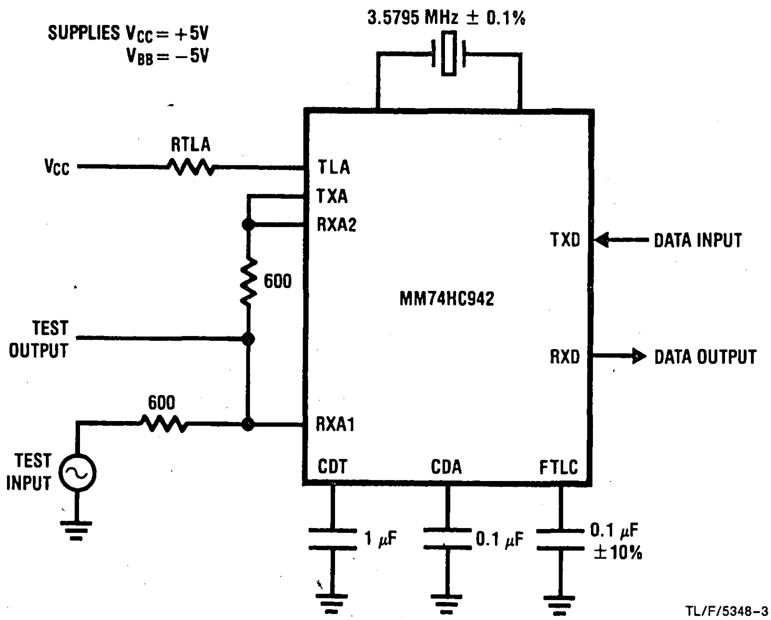
*The demodulator specifications apply to the MM74HC942 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC942 modulator.

AC Electrical Characteristics

Unless otherwise specified all specifications apply to the MM74HC942 over the range −40°C to +85°C using a V_{CC} = +5V ±10%, a V_{BB} = −5V ±10% and a 3.579MHz ±0.1% crystal.*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMITTER						
F_{CE}	Carrier Frequency Error				4	Hz
	Power Output	V_{CC}=5.0V R_{TLA} = 0 R_L=1.2 kΩ R_{TLA} = ∞		0 −12		dBm dBm
	2nd Harmonic Energy			−56		dBm
RECEIVE FILTER AND HYBRID						
	Hybrid Input Impedance (Pins 15 and 16)		50			kΩ
	FTLC Output Impedance		10		50	kΩ
	Adjacent Channel Rejection	RXA2=GND TXA=GND or V_{CC} Input to RXA1	60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)						
	Carrier Amplitude		−48		−12	dBm
	Dynamic Range			36		dB
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud		100		μS
	Bit Bias			5		%
	Carrier Detect Trip Points	CDA=1.2V Off to On On to Off		−44 −47		dBm dBm

AC Specification Circuit



TL/F/5348-3

Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data outpin pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system, XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	V_{BB}	Negative Supply: The recommended supply is −5V.
13	O/$\overline{A}$	Originate/$\overline{\text{Answer}}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded.
19	GND	Ground: This defines the chip 0V.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC942 uses frequency shift keying (FSK) of an audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC942 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC942 is capable of transmitting and receiving data simultaneously.

The tone allocation by the MM74HC942 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I BELL 103 ALLOCATION

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switched capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60 Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the $\overline{\text{FTLC}}$ pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques. The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{\text{CD}}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{\text{CD}}$ output remains stable. If carrier is lost $\overline{\text{CD}}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency produces one of four tones depending on the O/$\overline{\text{A}}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter. The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source impedances.

The transmit level is programmable by placing a resistor from TLA to VCC. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC942 will interface to most telephones. This arrangement is called the "permissive arrangement". The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

SNR can be maximized by adjusting the transmit level until the level at the exchange reaches −12 dBm. This must be done with the cooperation of the telephone company. The programming resistor used is specific for a given installation and is often included in the telephone jack at the installation. The modem is thus programmable and can be used with any jack correctly wired. This arrangement is called the universal registered jack arrangement and is possible with the MM74HC942. The values of resistors required to program the MM74HC942 follow the most common code in use; the universal service order code. The required resistors are given in Table II.

TABLE II Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ohms)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490
4	−8	3,610
5	−7	2,520
6	−6	1,780
7	−5	1,240
8	−4	866
9	−3	562
10	−2	336
11	−1	150
12	0	0

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on pin 4 sets the time interval that the carrier must be present before $\overline{\text{CD}}$ goes low. It also sets the time interval that carrier must be removed before $\overline{\text{CD}}$ returns high. The relevant timing equations are:

$T_{\overline{CD}L} \cong 6.4 \times C_{CDT}$ for $\overline{\text{CD}}$ going low

$T_{\overline{CD}H} \cong 0.54 \times C_{CDT}$ for $\overline{\text{CD}}$ going high

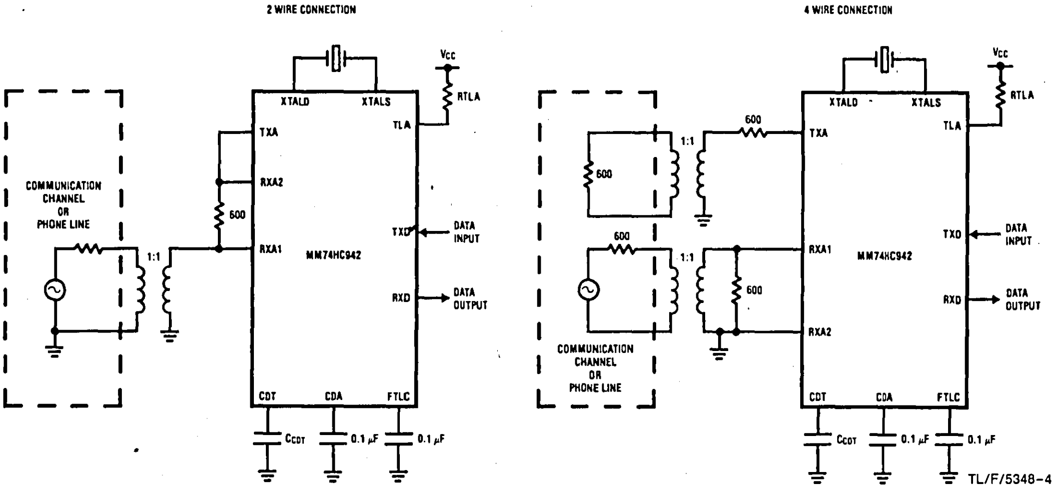
Where $T_{\overline{CD}L}$ & $T_{\overline{CD}H}$ are in seconds, and C_{CDT} is in μF.

Applications Information (Continued)

DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC942 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

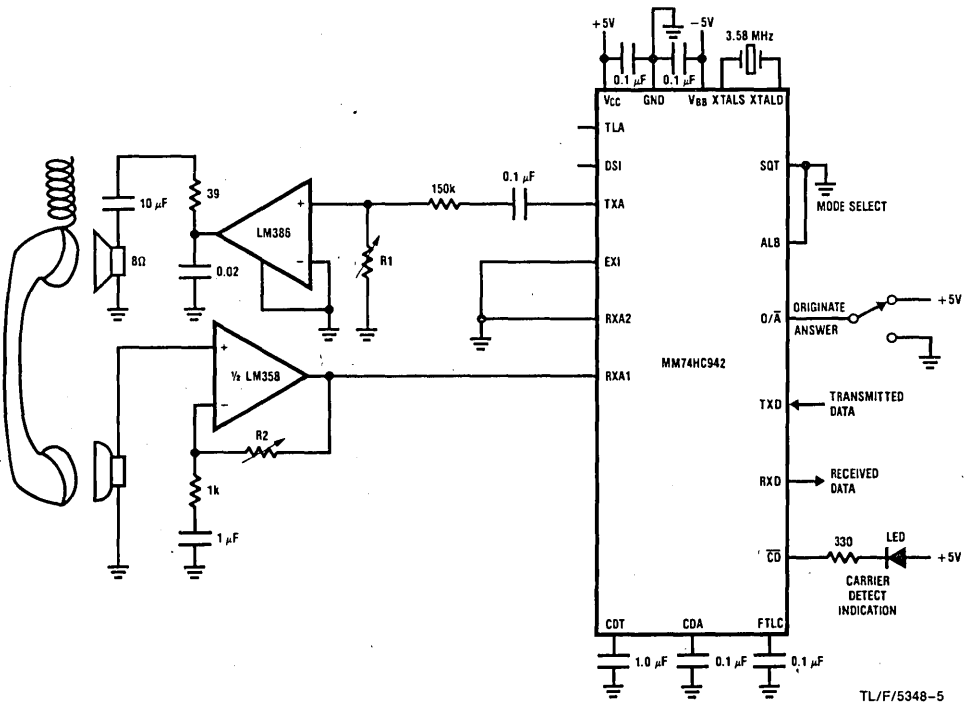
Interface Circuits for MM74HC942 300 Baud Modem



TL/F/5348-4

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5348-5

Note: The efficiency of the acoustic coupling will set the valves of R1 and R2.

National Semiconductor

PRELIMINARY

microCMOS

MM74HC943 300 Baud Modem

General Description

The MM74HC943 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC943 utilizes microCMOS Technology, 2 layers of polysilicon and 1 layer metal P-well CMOS. Switched capacitor techniques are used to peform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two to four wire conversion and drive the line at −9 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

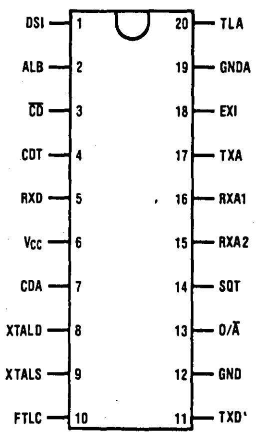
- 5V supply
- Drives 600Ω at −9 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signaling systems
- Remote process control

Connection Diagram

Dual-In-Line Package

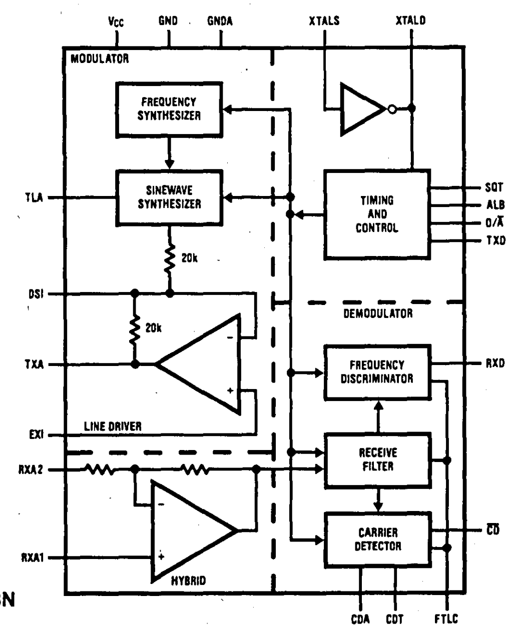


TOP VIEW TL/F/5349-1

MM74HC943

Order Number MM74HC943J or MM74HC943N
See NS Package J20A or N20A

Block Diagram



TL/F/5349-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions *	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	 V_{CC} 	 V_{CC}−0.1 3.84	 V_{CC}−0.1 3.7	 V V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V		 0.1 0.33	 0.1 0.4	 V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IH}=V_{CC}$, V_{IL}=GND ALB or SQT=GND Transmit Level=−9 dBm	8.0			mA
I_{CC}	Power Down Supply Current	ALB=SQT=V_{CC} $V_{IH}=V_{CC}$, V_{IL}=GND			250	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

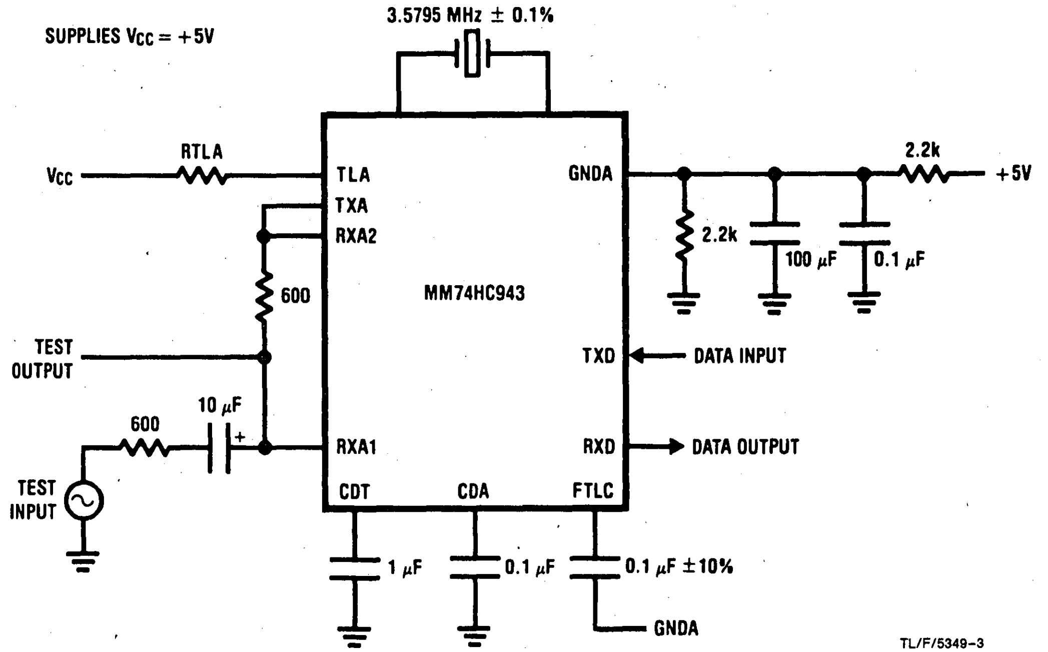
*The demodulator specifications apply to the MM74HC943 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC943 modulator.

AC Electrical Characteristics

Unless otherwise specified all specifications apply to the MM74HC943 over the range −40°C to +85°C using a V_{CC} of +5V ±10%, and a 3.579 MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error				1	4	Hz
	Power Output	V_{CC}=5.0V R_L=1.2 kΩ	R_{TLA} = 5490 R_{TLA} = ∞		−9 −12		dBm dBm
	2nd Harmonic Energy				−56		dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			10		50	kΩ
	Adjacent Channel Rejection	RXA2=GNDA, TXD=GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−12	dBm
	Dynamic Range				36		dB
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100		µS
	Bit Bias				5		%
	Carrier Detect Trip Points	CDA=1.2V	Off to On On to Off		−44 −47		dBm dBm

AC Specification Circuit



Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This input may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system. XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receiver filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	GND	Ground: This defines the chip 0V.
13	O/$\overline{A}$	Originate/$\overline{\text{Answer}}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded to GNDA.
19	GNDA	Analog Ground: Analog signals within the chip are referred to this pin.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC943 uses frequency shift keying (FSK) of audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC943 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC943 is capable of transmitting and receiving data simultaneously.

The tone allocation used by the MM74HC943 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. Bell 103 Tone Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switch capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency synthesizer produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter.

The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source inpedances.

The transmit level is programmable by placing a resistor from TLA to V_{CC}. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC943 will interface to most telephones. This arrangement is called the "permissive arrangement". The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ω)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$T_{\overline{CD}L} \cong 6.4 \times C_{CDT}$ for $\overline{CD}$ going low

$T_{\overline{CD}H} \cong 0.54 \times C_{CDT}$ for $\overline{CD}$ going high

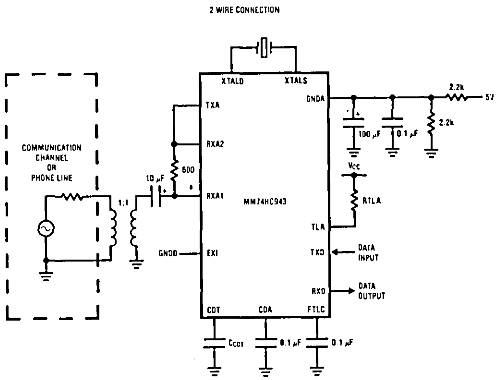
Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

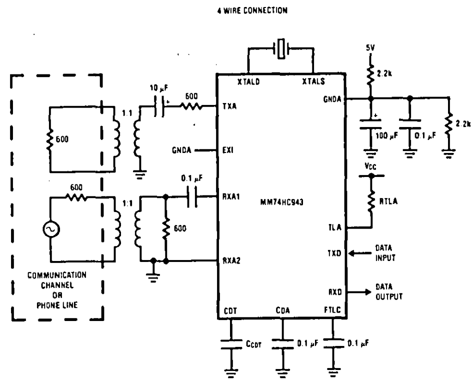
DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC943 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

Applications Information (Continued)

Interface Circuits for MM74HC943 300 Baud Modem



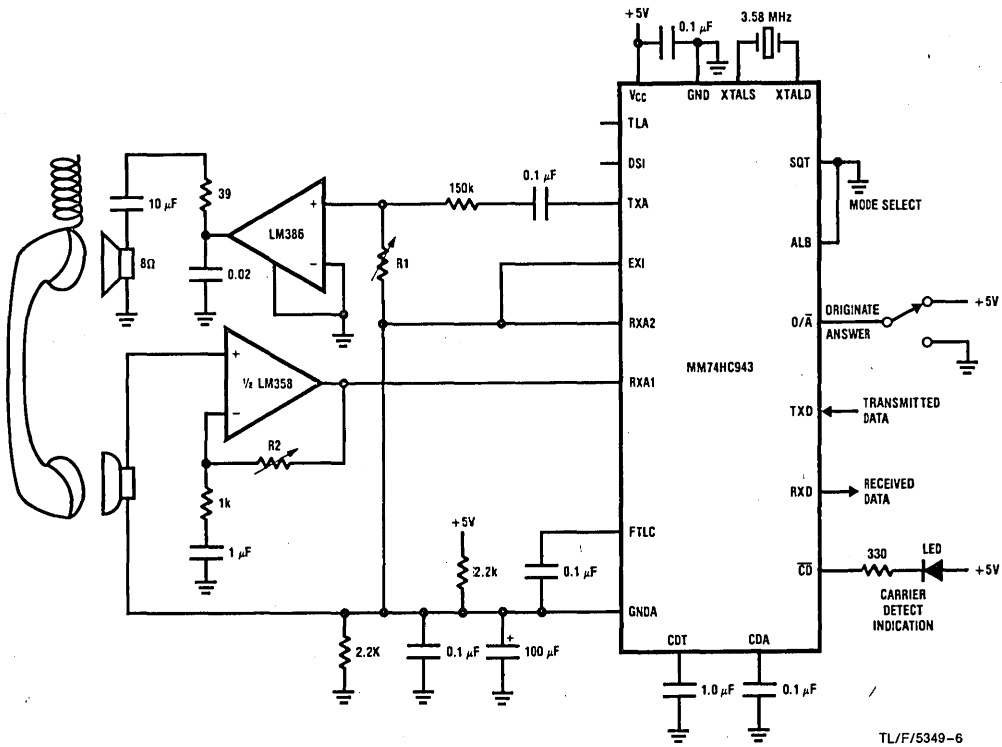


TL/F/5349–4

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

TL/F/5349–5

Complete Acoustically Coupled 300 Baud Modem



TL/F/5349–6

Note: The efficiency of the acoustic coupling will set the values of R1 and R2.

Section 4

Filters

4

Introduction

One of the most exciting new linear IC product families is the switched-capacitor filter building block circuits. These are examples of the use of switches to solve the filter problem—a departure from the traditional continuous analog solution (the RC active filter) to a new sampled-data approach.

Various realization schemes have used the interconnection of three op amps to form a basic resonator for a filter as shown in *Figure 4-1.*

These are called biquad and state variable RC active filters. This relatively large number of op amps reduces the dependency of the filter characteristics on the performance tolerances of both the active and the passive components.

PERFORMANCE OF THE TRADITIONAL RC INTEGRATOR

The performance of the traditional RC integrator—basic to this active filter (*Figure 4-2a*)—depends on both initial tolerances and the temperature drifts of the R and C values.

The idea of the switched-capacitor filter is to replace the R with a small-valued capacitor that repeatedly picks up an input charge and then dumps this charge into the summing junction of the op amp, as shown in *Figure 4-2b.*

The significant result is that labor-intensive tuning, or adjustment, of the component values that was needed with the RC active filter is no longer needed to obtain a desired filter characteristic. Performance now depends only on a well-controlled on-chip capacitor ratio and the frequency of an external clock. The repeatability and predictability of this low-cost, switched-capacitor CMOS filter is a key advantage.

4

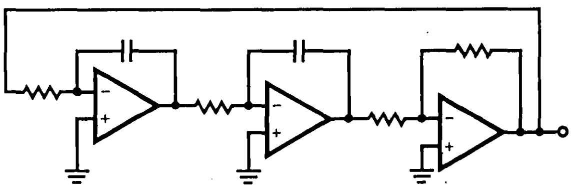
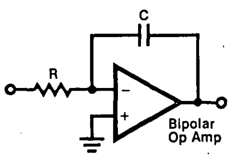
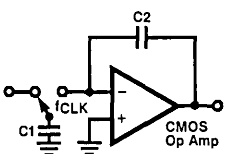


FIGURE 4-1. The Basic Three Op Amp Resonator Loop



a) The RC Integrator



b) The Switched-Capacitor Integrator

FIGURE 4-2. The Basic Idea of the Switched-Capacitor Filter

A GENERAL PURPOSE SWITCHED-CAPACITOR BUILDING BLOCK

A block diagram of the MF10 switched-capacitor building block that uses these concepts is shown in *Figure 4-3.* Two independent, second-order filter sections are available in this dual IC product. This particular basic interconnection is very flexible and allows all of the standard filter types (high pass, low pass, bandpass, notch, and all pass) to be easily realized.

A newer product, the MF5, that consists of one-half of the MF10, is also available. A spare CMOS op amp is part of the MF5, and fits in a standard 8-pin miniDIP package.

SPECIAL PRODUCTS FOR THE LOW PASS FUNCTION

In addition to the general purpose building block filters, active simulations of Butterworth low pass ladder filters (*Figure 4-4a*) are available, as well as 6th-order (*Figure 4-4b*) and 4th-order versions.

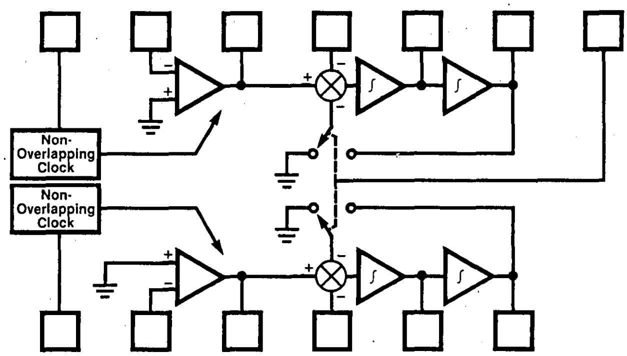
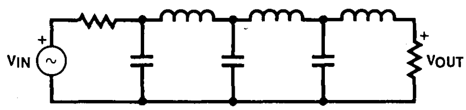
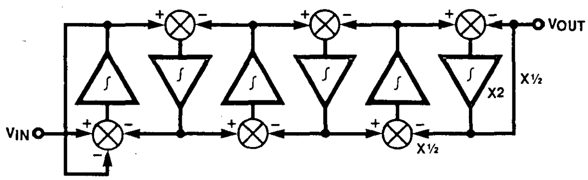


FIGURE 4-3. The Functional Diagram of the MF10 Switched-Capacitor Filter Building Block IC



a) The Basic Low Pass Ladder



b) Active Simulation

FIGURE 4-4. The Classic Low Pass Ladder Filter and the Electronic Simulation

National Semiconductor

PRELIMINARY

MF4 4th Order Switched Capacitor Butterworth Lowpass Filter

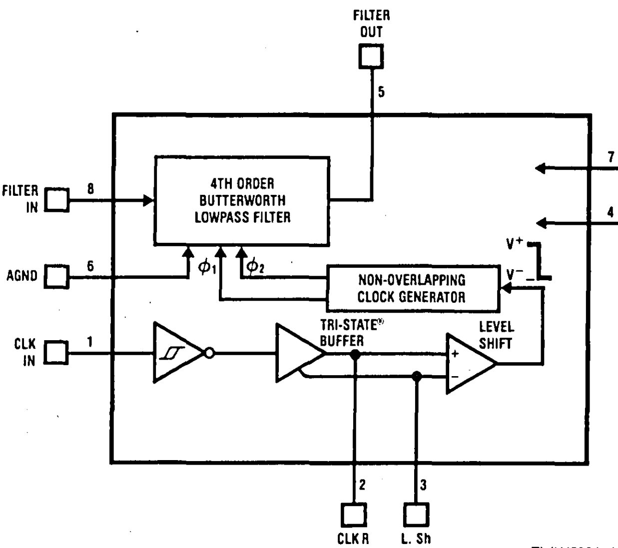
General Description

The MF4 is a versatile, easy to use, precision 4th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF4-50) or 100 to 1 (MF4-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF4 sections for higher order filtering.

Features

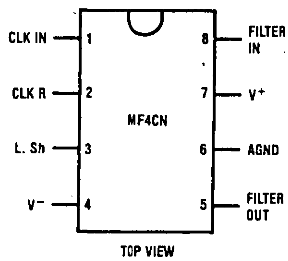
- Low Cost
- Easy to use
- No external components
- 8-pin mini-DIP
- Cutoff frequency accuracy of ±0.3%
- Cutoff frequency range of 0.1 Hz to 20 kHz
- 5V to 14V operation
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams



TL/H/5064-1

Dual-In-Line Package



TL/H/5064-2

Order Number MF4CN
See NS Package N08E

Absolute Maximum Ratings

Supply Voltage	14V
Power Dissipation	500 mW
Operating Temperature	0°C to 70°C(MF4CN)
Storage Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 7)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 5V$, $V^- = -5V$					
Cutoff Frequency Range (f_C) (Note 1)	MF4-50			0.1 20k	Hz (min) Hz (max)
	MF4-100			0.1 10k	Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	2.5	3.5		mA (max)
Clock Feedthrough (Peak-to-Peak)	$T_A = 25°C$ Filter Output	25			mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.15		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	$T_A = 25°C$ MF4-50 MF4-100	49.98±0.3%	49.98±0.8%	49.98±0.6%	(max) (max)
f_{CLK}/f_C Temperature Coefficient	MF4-50 MF4-100	±15			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−25.0	−24.0		dB (min)
DC Offset Voltage	MF4-50 MF4-100	−200 −400			mV mV
Output Swing	$R_L = 5$ kΩ	+4.0 −4.5	+3.5 −4.0		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	50 1.5			mA mA
Dynamic Range (Note 2)	$T_A = 25°C$ MF4-50 MF4-100	80 78			dB dB
Additional Magnitude Response Test Points (Note 4) MF4-50 ($f_C = 5$ kHz) Magnitude at	$T_A = 25°C$ $f_{CLK} = 250$ kHz f = 6000 Hz f = 4500 Hz	−7.57 −1.44	−7.57±0.27 −1.44±0.12		dB (max) dB (max)
MF4-100 ($f_C = 25$ kHz) Magnitude at	f = 3000 Hz f = 2250 Hz		±0.2 ±0.1		dB (max) dB (max)

Electrical Characteristics (Note 7)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 2.5V$, $V^- = -2.5V$					
Cutoff Frequency Range (f_C) (Note 1)	MF4-50 MF4-100			0.1 10k 0.1 5k	Hz (min) Hz (max) Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	1.5	2.25		mA (max)
Clock Feedthrough (Peak-to-Peak)	$T_A = 25°C$ Filter Output	15			mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.15		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	$T_A = 25°C$ MF4-50 MF4-100	50.07±0.3%	50.07±1.6%	50.07±0.6%	(max) (max)
f_{CLK}/f_C Temperature Coefficient	MF4-50 MF4-100	±25			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−25.0	−24.0		dB (min)
DC Offset Voltage	MF4-50 MF4-100	−150 −300			mV mV
Output Swing	$R_L = 5$ kΩ	1.5 −2.2	1.0 −1.7		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 28 0.5			 mA mA
Dynamic Range (Note 2)	$T_A = 25°C$ MF4-50 MF4-100	 80 78			 dB dB
Additional Magnitude Response Test Points (Note 4) MF4-50 ($f_C = 5$ kHz) Magnitude at	$T_A = 25°C$ $f_{CLK} = 250$ kHz f = 6000 Hz f = 4500 Hz	−7.57 −1.46	−7.57±0.54 −1.46±0.24		dB (max) dB (max)
MF4-100 ($f_C = 2.5$ kHz) Magnitude at	f = 3000 Hz f = 2250 Hz		±0.2 ±0.1		dB (max) dB (max)

Logic Input-Output Characteristics (Note 7) ($V^-=0V$, Note 5)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
SCHMITT TRIGGER					
V_{T+} Positive Going Threshold Voltage	$V^+=10V$	7.0	6.1		V (min)
			8.9		V (max)
	$V^+=5V$	3.5	3.1		V (min)
			4.4		V (max)
V_{T-} Negative Going Threshold Voltage	$V^+=10V$	3.0	1.3		V (min)
			3.8		V (max)
	$V^+=5V$	1.5	0.6		V (min)
			1.9		V (max)
Hysteresis ($V_{T+}-V_{T-}$)	$V^+=10V$	4.0	2.3		V (min)
			7.6		V (max)
	$V^+=5V$	2.0	1.2		V (min)
			3.8		V (max)
Logical "1" Output Voltage ($I_O=-10\ \mu A$) (Pin 2)	$V^+=10V$ $V^+=5V$		9.0 4.5		V (min) V (min)
Logical "0" Output Voltage ($I_O=10\ \mu A$) (Pin 2)	$V^+=10V$ $V^+=5V$		1.0 0.5		V (max) V (max)
Output Source Current	CLK R Shorted to Ground $V^+=10V$ $V^+=5V$	 6.0 1.5	 3.0 0.75		 mA (min) mA (min)
Output Sink Current	CLK R Shorted to V^+ $V^+=10V$ $V^-=5V$	 5.0 1.3	 2.5 0.65		 mA (min) mA (min)
TTL CLOCK INPUT (CLK R PIN) (Note 8)					
V_{IL} (Logical "0" Input Voltage)			0.8		V (max)
V_{IH} (Logical "1" Input Voltage)			2.0		V (min)
Leakage Current at CLK R Pin	$T_A=25°C$, L. Sh Pin Tied to Mid-Supply		2.0		μA (max)

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically μVrms for the MF4-50 and μVrms for the MF4-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically μVrms for both the MF4-50 and the MF4-100.

Note 3: The specifications for the MF4 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 4: Besides checking the cutoff frequency (f_C) and the stopband attenuation at 2 f_C, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB. For a further discussion see Applications Hints.

Note 5: For simplicity all the logic levels have been referenced to $V^-=0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: Unless otherwise stated, these specifications apply over the commercial temperature range of $0°C \le T_A \le 70°C$.

Note 8: The MF4 is operating with symmetrical split supplies and L. Sh is tied to ground.

Missing Values and "Application Hints" section will be added on final data sheet.

Pin Description

FILTER OUT — This is the output of the lowpass filter. It will typically sink 0.90 mA and source 3 mA. Typically, the output will swing to within 1V of each supply rail.

FILTER IN — This is the input to the lowpass filter. To minimize gain errors, the source impedance should be less than 2 kΩ. For more details see Application Hints section. Note that for single supply operation the input signal must be biased to mid-supply or AC coupled.

AGND — This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation, see *Figure 4.* For a further discussion on mid-supply biasing techniques see the Application Hints. For optimum filter performance a "clean" ground must be provided.

V^+, V^- — These are the positive and negative supply pins. The MF4 will operate over a supply range of 5V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.

CLK IN — This is the input of a CMOS Schmitt trigger. If an external CMOS logic level clock is to be used, it is applied to this pin.

L. Sh — The level shift pin serves two purposes. One, the voltage at this pin sets the input switching threshold of an internal level shift stage. The level shift stage converts either TTL or CMOS logic levels to full V^+ to V^- clock levels that are required by the internal non-overlapping clock generator. The threshold is approximately 2V above the voltage at the level shift pin.

Second, the voltage at this pin enables or disables an internal TRI-STATE buffer between the Schmitt trigger and the level shift stage. When tied to V^-, this buffer is enabled and the Schmitt trigger drives the level shift stage. When tied to mid-supply (ground where the MF4 is operating from symmetrical split supplies) or above, the buffer is disabled and is placed in a high impedance state. This allows an external TTL (if L. Sh is connected to ground) or CMOS logic level to be applied to the level shift stage via the CLK R pin.

CLK R — This pin serves as the input for a TTL logic level clock if the L. Sh pin is tied to ground and the MF4 is operating with dual supplies.

In the self-clocking mode an external resistor is tied from this pin to the CLK IN pin and an external capacitor is tied from the CLK IN pin to ground. This creates a Schmitt trigger oscillator. When using the self-clocking mode the L. Sh pin must be tied to V^-.

DUAL SUPPLY OPERATION

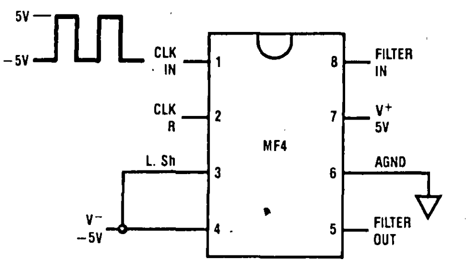


FIGURE 1. MF4 Driven with CMOS Level Clock ($V_{IH} \geq 0.8\ V_{CC}$* and $V_{IL} \leq 0.2\ V_{CC}$)

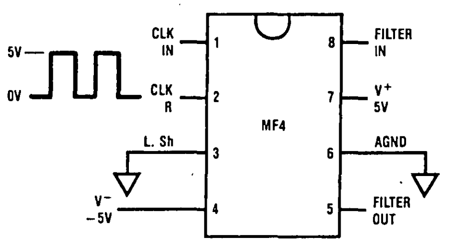
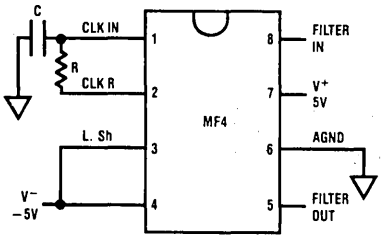


FIGURE 2. MF4 Driven with TTL Level Clock

*$V_{CC} = V^+ - V^-$

Pin Description (Continued)

DUAL SUPPLY OPERATION



$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

Typically for $V_{CC} = 10V$

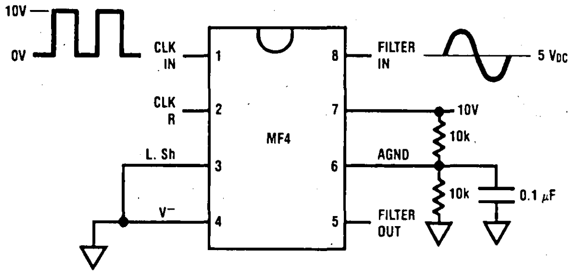
$$f_{CLK} = \frac{1}{1.69\ RC}$$

TL/H/5064-5

FIGURE 3. MF4 Driven with Schmitt Trigger Oscillator

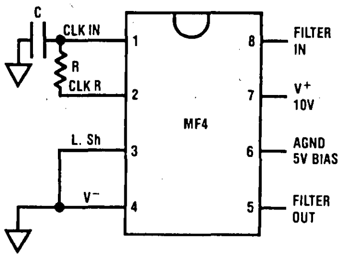
SINGLE SUPPLY OPERATION

If an external clock is used, it has to be of CMOS level because the clock is input to a CMOS Schmitt trigger.
The AGND pin must be biased to mid-supply.
The input signal should be DC biased to mid-supply or AC coupled to the input pin.



TL/H/5064-6

FIGURE 4a. MF4 Driven with an External Clock



$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

Typically for $V_{CC} = 10V$

$$f_{CLK} = \frac{1}{1.69\ RC}$$

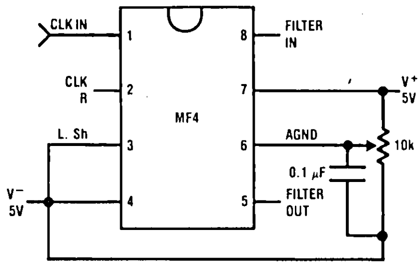
TL/H/5064-7

An external R and C can be used to generate an on-board clock; if so, the L. Sh pin should remain at ground.

FIGURE 4b. MF4 Driven with the Schmitt Trigger Oscillator

Pin Description (Continued)

OFFSET ADJUST



TL/H/5064-8

FIGURE 5. Typical Circuit for Adjusting the DC Offset of the Filter (See Application Hints on mid-supply bias generation) Filter Out should be referenced to AGND.

National Semiconductor

PRELIMINARY

MF5 Universal Monolithic Switched Capacitor Filter

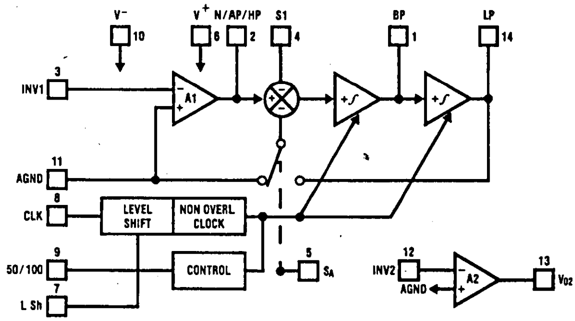
General Description

The MF5 consists of an extremely easy to use, general purpose CMOS active filter building block and an uncommitted op amp. The filter building block, together with an external clock and a few resistors, can produce various second order functions. The filter building block has 3 output pins. One of the output pins can be configured to perform highpass, allpass or notch functions and the remaining 2 output pins perform bandpass and lowpass functions. The center frequency of the filter can be directly dependent on the clock frequency or it can depend on both clock frequency and external resistor ratios. The uncommitted op amp can be used for cascading purposes, or for obtaining additional allpass and notch functions or for various other applications. Higher order filter functions can be obtained by cascading several MF5s or by using the MF5 in conjuction with the MF10 (dual switched capacitor filter building block). The MF5 is functionally compatible with the MF10. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 14-pin DIP
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variations
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- f_0 X Q range up to 200 kHz
- Operation up to 30 kHz
- Uncommitted op amp available

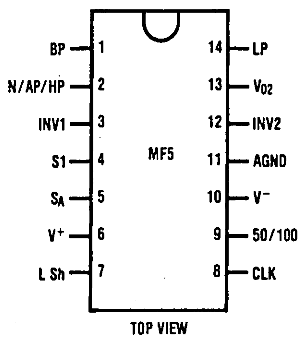
System Block Diagram



TL/H/5066-1

Connection Diagram

Dual-In-Line Package



Order Number MF5
See NS Packages J14A, N14A

TL/H/5066-2

National Semiconductor

PRELIMINARY

MF6 6th Order Switched Capacitor Butterworth Lowpass Filter

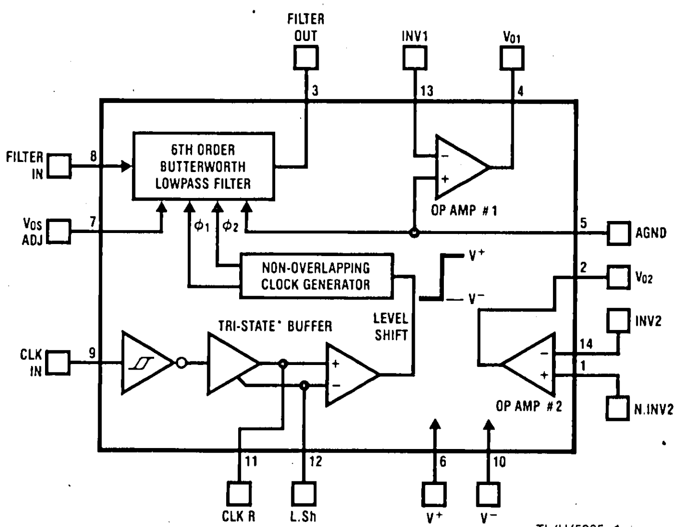
General Description

The MF6 is a versatile easy to use, precision 6th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF6-50) or 100 to 1 (MF6-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF6 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

Features

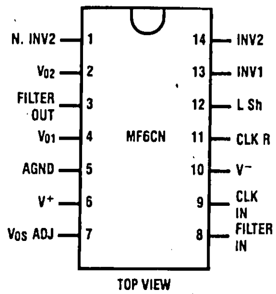
- Low cost
- Easy to use
- No external components
- 14-pin DIP
- Cutoff frequency accuracy of ±0.3%
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Two uncommitted op amps available
- 5V to 14V operation
- Cutoff frequency set by external internal clock

Block and Connection Diagrams



TL/H/5065-1

Dual-In-Line Package



TL/H/5065-2

Order Number MF6
See NS Package N14A

Absolute Maximum Ratings

Supply Voltage	14V	Storage Temperature	150°C
Power Dissipation	−500 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	0°C to 70°C (MF6CN)		

Electrical Characteristics (Filter) (Note 7)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 5V$, $V^- = -5V$					
Cutoff Frequency Range (f_C) (Note 1)	MF6-50 MF6-100			0.1 20k 0.1 10k	Hz (min) Hz (max) Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	4.0	6.0		mA (max)
Clock Feedthrough (Peak-to-Peak)	$T_A = 25°C$ Filter Output Op Amp #1 Output Op Amp #2 Output	 30 25 20			 mV mV mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2\ k\Omega$	0.0	±0.15		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	$T_A = 25°C$ MF6-50 MF6-100	 49.27±0.3% 98.97±0.3%	 49.27±0.6% 98.97±0.6%		 (max) (max)
f_{CLK}/f_C Temperature Coefficient	MF6-50 MF6-100	25 25			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−37.5	−36		dB (min)
DC Offset Voltage	MF6-50 MF6-100	−200 −300			mV mV
Output Swing	$R_L = 5\ k\Omega$	+4.0 −4.1	+3.5 −3.8		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 50 1.5			 mA mA
Dynamic Range (Note 2)	$T_A = 25°C$ MF6-50 MF6-100	 83 81			 dB dB
Additional Magnitude Response Test Points (Note 4) MF6-50 ($f_C = 5$ kHz) Magnitude at	$T_A = 25°C$ $f_{CLK} = 250$ kHz f = 6000 Hz f = 4500 Hz	 −9.47 −0.92	 −9.47±0.3 −0.92±0.1		 dB (max) dB (max)
MF6-100 ($f_C = 2.5$ kHz) Magnitude at	 f = 3000 Hz f = 2250 Hz	 −9.48 −0.97	 −9.48±0.3 −0.97±0.1		 dB (max) dB (max)

Electrical Characteristics (Continued) (Filter) (Note 7)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 2.5V$, $V^- = -2.5V$					
Cutoff Frequency Range (f_C) (Note 1)	MF6-50 MF6-100			0.1 10k 0.1 5k	Hz (min) Hz (max) Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	2.5	4.0		mA (max)
Clock Feedthrough (Peak-to-Peak)	$T_A = 25°C$ Filter Output Op Amp #1 Output Op Amp #2 Output	 20 10 10			 mV mV mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.15		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	$T_A = 25°C$ MF6-50 MF6-100	 49.45 ± 0.3% 99.35 ± 0.3%	 49.45 ± 0.6% 99.35 ± 0.6%		 (max) (max)
f_{CLK}/f_C Temperature Coefficient	MF6-50 MF6-100	−15 90			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−37.5	−36		dB (min)
DC Offset Voltage	MF6-50 MF6-100	−150 −300			mV mV
Output Swing	$R_L = 5$ kΩ	1.5 −2.2	1.0 −1.7		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 28 0.5			 mA mA
Dynamic Range (Note 2)	$T_A = 25°C$ MF6-50 MF6-100	 77 77			 dB dB
Additional Magnitude Response Test Points (Note 4) MF6-50 ($f_C = 5$ kHz) Magnitude at	$T_A = 25°C$ $f_{CLK} = 250$ kHz f = 6000 Hz f = 4500 Hz	 −9.54 −0.96	 −9.54 ± 0.3 −0.96 ± 0.1		 dB (max) dB (max)
MF6-100 ($f_C = 2.5$ kHz) Magnitude at	 f = 3000 Hz f = 2250 Hz	 −9.67 −1.01	 −9.67 ± 0.3 −1.01 ± 0.1		 dB (max) dB (max)

Electrical Characteristics (Both Op Amps) (Note 7)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 5V$, $V^- = -5V$					
DC Open Loop Gain	$T_A = 25°C$	72		67	dB (min)
Gain Bandwidth Product	$T_A = 25°C$	2.5	1.5		MHz (min)
Input Offset Voltage		8.0	20		mV (max)
Output Swing	$R_L = 2.5\ k\Omega$	4.0 −4.5	3.8 −4.0		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 54 3			 mA mA
Common-Mode Range (Op Amp #2 Only)		±3.9	±3.8		V (min)
CMRR (Op Amp #2 Only)		60			dB (min)
Input Bias Current	$T_A = 25°C$	10			pA
Slew Rate	$T_A = 25°C$	7.0			V/μs
$V^+ = 2.5V$, $V^- = -2.5V$					
DC Open Loop Gain	$T_A = 25°C$	67		62	dB (min)
Gain Bandwidth Product	$T_A = 25°C$	2.0	1.2		MHz (min)
Input Offset Voltage		8.0	20		mV (max)
Output Swing	$R_L = 2.5\ k\Omega$	1.5 −2.2	1.3 −1.7		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 29 1.0			 mA mA
Common-Mode Range (Op Amp #2 Only)		1.4 −1.5	1.3 −1.4		V (min) V (min)
CMRR (Op Amp #2 Only)		60			dB (min)
Input Bias Current	$T_A = 25°C$	10			pA
Slew Rate	$T_A = 25°C$	6			V/μs

Logic Input-Output Characteristics (Note 7) ($V^- = 0V$, Note 5)

Parameter	Conditions	Typical	Tested Limits	Design Limits	Units (Limits)
SCHMITT TRIGGER					
V_{T+} Positive Going Threshold Voltage	$V^+ = 10V$	7.0	6.1		V (min)
			8.9		V (max)
	$V^+ = 5V$	3.5	3.1		V (min)
			4.4		V (max)
V_{T-} Negative Going Threshold Voltage	$V^+ = 10V$	3.0	1.3		V (min)
			3.8		V (max)
	$V^+ = 5V$	1.5	0.6		V (min)
			1.9		V (max)
Hysteresis ($V_{T+} - V_{T-}$)	$V^+ = 10V$	4.0	2.3		V (min)
			7.6		V (max)
	$V^+ = 5V$	2.0	1.3		V (min)
			3.8		V (max)
Logical "1" Output Voltage ($I_O = -10\ \mu A$) (Pin 11)	$V^+ = 10V$		9.0		V (min)
	$V^+ = 5V$		4.5		V (min)
Logical "0" Output Voltage ($I_O = 10\ \mu A$) (Pin 11)	$V^+ = 10V$		1.0		V (max)
	$V^+ = 5V$		0.5		V (max)
Output Source Current (Pin 11)	CLK R Shorted to Ground				
	$V^+ = 10V$	6.0	3.0		mA (min)
	$V^+ = 5V$	1.5	0.75		mA (min)
Output Sink Current (Pin 11)	CLK R Shorted to V^+				
	$V^+ = 10V$	5.0	2.5		mA (min)
	$V^- = 5V$	1.3	0.65		mA (min)
TTL CLOCK INPUT (CLK R PIN) (NOTE 8)					
V_{IL} (Logical "0" Input Voltage)			0.8		V (max)
V_{IH} (Logical "1" Input Voltage)			2.0		V (min)
Leakage Current at CLK R Pin	$T_A = 25°C$, L. Sh Pin Tied to Mid-Supply		2.0		μA (max)

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μVrms for the MF6-50 and 250 μVrms for the MF6-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwith is typically 140 μVrms for both the MF6-50 and the MF6-100.

Note 3: The specifications for the MF6 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 4: Besides checking the cutoff frequency (f_C) and the stopband attenuation at 2 f_C, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB. For a further discussion see Application Hints.

Note 5: For simplicity all the logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: Unless otherwise stated, these specifications apply over the commercial temperature range of $0°C \leq T_A \leq 70°C$.

Note 8: The MF6 is operating with symmetrical split supplies and L. Sh is tied to ground.

"Application Hints" section will be added on final data sheet.

Pin Description

FILTER OUT This is the output of the lowpass filter. It will typically sink 0.90 mA and source 3 mA. Typically, the output will swing to within 1V of each supply rail.

V_{OS} ADJ If needed, this pin is used to adjust the DC offset of the lowpass filter. A typical circuit is shown in *Figure 5*, where a 50 kΩ pot is connected between V+ and V− and the wiper is connected to the V_{OS} ADJ pin. If the V_{OS} ADJ pin is not used it must be tied to AGND. The DC gain from the V_{OS} ADJ pin to the output of the filter is 2.5 to 3.0.

FILTER IN This is the input to the lowpass filter. To minimize gain errors, the source impedance should be less than 2 kΩ. For more details see Application Hints section. Note that for single supply operation the input signal must be biased to mid-supply or AC coupled.

V_{02}, INV2, N. INV2 V_{02} is the output of op amp #2. INV2 and N. INV2 are the inverting and non-inverting inputs of op amp #2, respectively. These are very high impedance inputs.

V_{01}, INV1 V_{01} is the output and INV1 is the inverting input of op amp #1. INV1 is also a high impedance input. The non-inverting input is connected to AGND (analog ground) internally Both op amp #1 and op amp #2 will typically sink 1.8 mA and source 3 mA and will swing to within 1V of each supply rail.

AGND This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation, see *Figure 4*. For a further discussion on mid-supply biasing techniques see the Application Hints. For optimum filter performance a "clean" ground must be provided.

V+, V− These are the positive and negative supply pins. The MF6 will operate over a supply range of 5V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.

CLK IN This is the input of a CMOS Schmitt trigger. If an external CMOS logic level clock is to be used, it is applied to this pin.

L. Sh The level shift pin serves two purposes. One, the voltage at this pin sets the input switching threshold of an internal level shift stage. The level shift stage converts either TTL or CMOS logic levels to full V+ to V− clock levels that are required by the internal non-overlapping clock generator. The threshold is approximately 2V above the voltage at the level shift pin.
Second, the voltage at this pin enables or disables an internal TRI-STATE buffer between the Schmitt trigger and the level shift stage. When tied to V−, this buffer is enabled and the Schmitt trigger drives the level shift stage. When tied to mid-supply (ground where the MF6 is operating from symmetrical split supplies) or above, the buffer is disabled and is placed in a high impedance state. This allows an external TTL (if L. Sh is connected to ground) or CMOS logic level to be applied to the level shift stage via the CLK R pin.

CLK R This pin serves as the input for a TTL logic level clock if the L. Sh pin is tied to ground and the MF6 is operating with dual supplies. In the self-clocking mode an external resistor is tied from this pin to the CLK IN pin and an external capacitor is tied from the CLK IN pin to ground. This creates a Schmitt trigger oscillator. When using the self-clocking mode the L. Sh pin must be tied to V−.

Dual Supply Operation

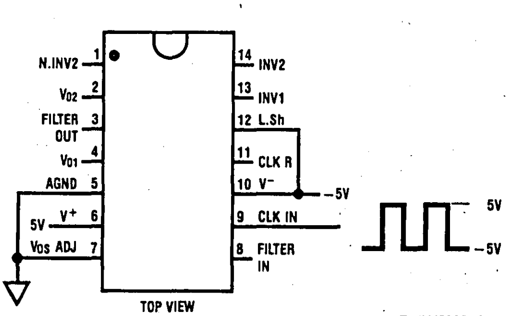


FIGURE 1. MF6 Driven with CMOS Logic Level Clock ($V_{IH} \geq 0.8\ V_{CC}$* and $V_{IL} \leq 0.2\ V_{CC}$)

*$V_{CC} = V^+ - V^-$

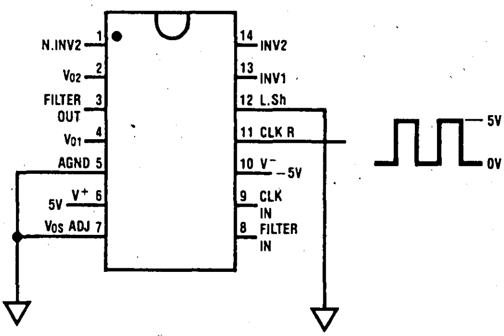
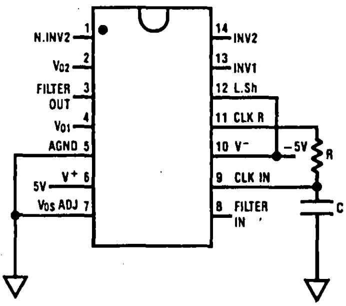


FIGURE 2. MF6 Driven with TTL Logic Level Clock

DUAL SUPPLY OPERATION



$$f_{CLK} = \frac{1}{\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \right) \left(\frac{V_{T+}}{V_{T-}} \right) \right]}$$

Typically for $V_{CC} = 10V$

$$f_{CLK} = \frac{1}{1.69\ RC}$$

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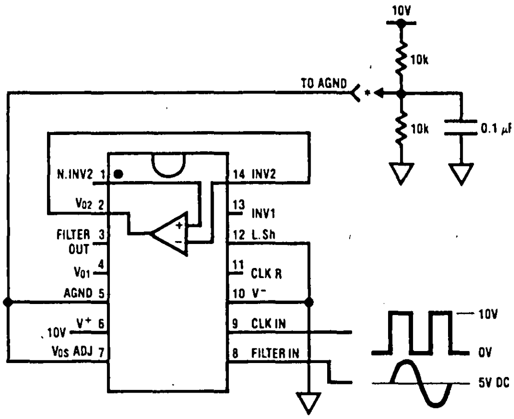
FIGURE 3. MF6 Driven with Schmitt Trigger Oscillator

SINGLE SUPPLY OPERATION

The AGND pin must be biased to mid-supply.
The input signal should be DC biased to
mid-supply or AC coupled to the input pin



* or buffer with op amp #2,
then apply to AGND

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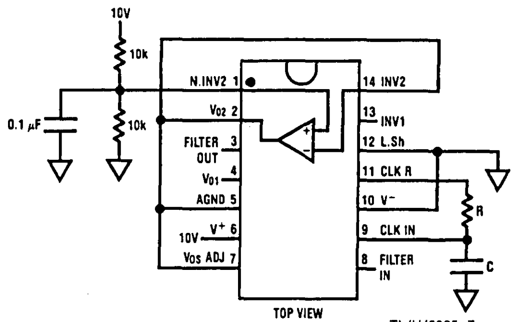
If an external clock is used, it has to be of CMOS logic
levels because the clock is input to a CMOS Schmitt trigger.

FIGURE 4a. MF6 Driven with an External Clock



$$f_{CLK} = \frac{1}{\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \right) \left(\frac{V_{T+}}{V_{T-}} \right) \right]}$$

Typically for $V_{CC}^* = 10V$

$$f_{CLK} = \frac{1}{1.69\ RC}$$

$^*V_{CC} = V^+ - V^-$

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An external R and C can be used to generate an on-
board clock, if so the L. Sh pin should remain at ground

FIGURE 4b. MF6 Driven with the Schmitt Trigger Oscillator

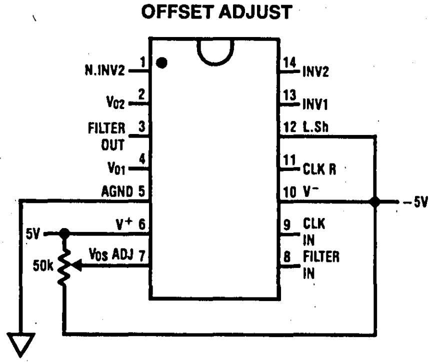

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FIGURE 5. Typical Circuit for Adjusting Filter DC Offset
If not used, connect V_{OS} ADJ pin to AGND)

National Semiconductor

MF10 Universal Monolithic Dual Switched Capacitor Filter

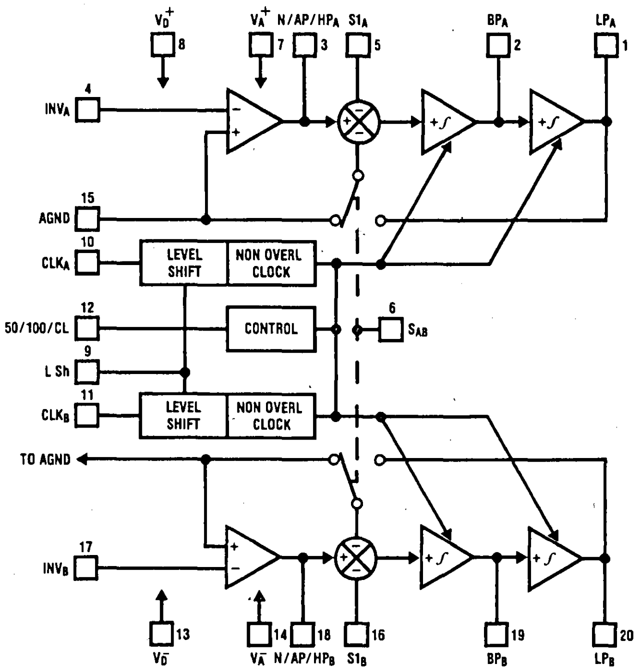
General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 20-pin 0.3" wide package
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_0 \times Q$ range up to 200 kHz
- Operation up to 30 kHz

System Block Diagram



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Absolute Maximum Ratings

Supply Voltage	14V	Storage Temperature	150°C
Power Dissipation	500 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	0°C to 70°C		

Electrical Characteristics (Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	$f_o \times Q < 200$ kHz	20	30		kHz
Clock to Center Frequency Ratio, f_{CLK}/f_o MF10BN MF10CN MF10BN MF10CN	 Pin 12 High, Q=10 $f_o \times Q < 50$ kHz, Mode 1 Pin 12 at Mid Supplies Q=10, $f_o \times Q < 50$ kHz, Mode 1		 49.94±0.2% 49.94±0.2% 99.35±0.2% 99.35±0.2%	 ±0.6% ±1.5% ±0.6% ±1.5%	
Q Accuracy (Q Deviation from an Ideal Continuous Filter) MF10BN MF10CN MF10BN MF10CN	 Pin 12 High, Mode 1 $f_o \times Q < 100$ kHz, $f_o < 5$ kHz Pin 12 at Mid Supplies $f_o \times Q < 100$ kHz $f_o < 5$ kHz, Mode 1		 ±2% ±2% ±2% ±2%	 ±4% ±6% ±3% ±6%	
f_o Temperature Coefficient	Pin 12 High (~50:1) Pin 12 Mid Supplies (~100:1) $f_o \times Q < 100$ kHz, Mode 1 External Clock Temperature Independent		±10 ±100		ppm/°C ppm/°C
Q Temperature Coefficient	$f_o \times Q < 100$ kHz, Q Setting Resistors Temperature Independent		±500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1=R2=10k			±2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			8	10	mA

Electrical Characteristics (Internal Op Amps) 25°C

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		±4	±5		V
Voltage Swing (Pins 1, 2, 19, 20) MF10BN MF10CN	$V_S = \pm 5V$, $R_L = 5k$	 ±3.8 ±3.2	 ±4 ±3.7		 V V
Voltage Swing (Pins 3 and 18) MF10BN MF10CN	$V_S = \pm 5V$, $R_L = 3.5k$	 ±3.8 ±3.2	 ±4 ±3.7		 V V
Output short Circuit Current Source Sink	$V_S = \pm 5V$		 3 1.5		 mA
Op Amp Gain BW Product			2.5		MHz
Op Amp Slew Rate			7		V/µS

Definition of Terms

f_{CLK}: the switched capacitor filter external clock frequency.

f_o: center of frequency of the second order function complex pole pair. f_o is measured at the bandpass output of each ½ MF10, and it is the frequency of the bandpass peak occurrence (*Figure 1*).

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each ½ MF10 and it is the ratio of f_o over the −3 dB bandwidth of the 2nd order bandpass filter, *Figure 1*. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain in (V/V) of the lowpass output of each ½ MF10 at $f \rightarrow 0$ Hz, *Figure 2*.

H_{OHP}: the gain in (V/V) of the highpass output of each ½ MF10 as $f \rightarrow f_{CLK}/2$, *Figure 3*.

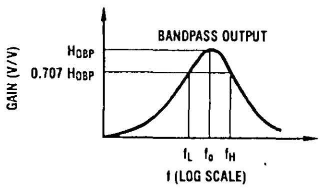
Q_Z: the quality factor of the 2nd order function complex zero pair, if any. (Q_Z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

f_z: the center frequency of the 2nd order function complex zero pair, if any. If f_z is different from f_o, and if the Q_Z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF-10.

H_{ON_1}: the notch output gain as $f \rightarrow 0$ Hz.

H_{ON_2}: the notch output gain as $f \rightarrow f_{CLK}/2$.

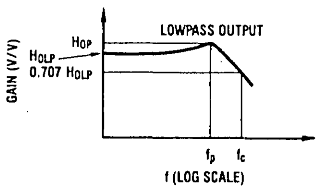


$$Q = \frac{f_o}{f_H - f_L}; \quad f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 1

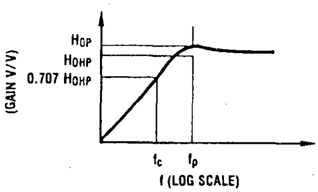


$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2



$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

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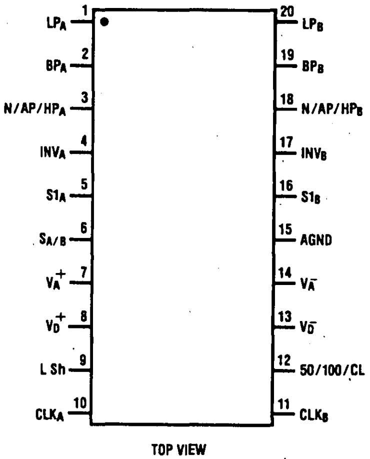
FIGURE 3

Connection Diagram

Dual-In-Line Package



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Order Number MF10BN or MF10CN
See NS Package N20A

Pin Description

LP, BP, N/AP/HR	These are the lowpass, bandpass, notch or allpass or highpass outputs of each 2nd order section. The LP and BP outputs can sink typically 1 mA and source 3 mA. The N/AP/HP output can typically sink and source 1.5 mA and 3 mA, respectively.
INV	This is the inverting input of the summing op amp of each filter. The pin has static discharge protection.
S1	S1 is a signal input pin used in the allpass filter configurations (see modes of operation 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ.
$S_{A/B}$	It activates a switch connecting one of the inputs of the filter's 2nd summer either to analog ground ($S_{A/B}$ low to V_A^-) or to the lowpass output of the circuit ($S_{A/B}$ high to V_A^+). This allows flexibility in the various modes of operation of the IC. $S_{A/B}$ is protected against static discharge.
V_A^+, V_D^+	Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
V_A^-, V_D^-	Analog and digital negative supply respectively. The same comments as for V_A^+ and V_D^+ apply here.
L Sh	Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the L Sh pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used but T²L clock levels, derived from 0V to 5V supply, are only available, the L Sh pin should be tied to the system ground. For single supply operation (0V and 10V) the V_D^-, V_A^- pins should be connected to the system ground, the AGND pin should be biased at 5V and the L Sh pin should also be tied to the system ground. This will accommodate both CMOS and T²L clock levels.
CLK (A or B)	Clock inputs for each switched capacitor filter building block. They should both be of the same level (T²L or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the op amps to settle which yields optimum filter operation.
50/100/CL	By tying the pin high a 50:1 clock to filter center frequency operation is obtained. Tying the pin at mid supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When the pin is tied low, a simple current limiting circuitry is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.
AGND	Analog ground pin; it should be connected to the system ground for dual supply operation or biased at mid supply for single supply operation. The positive inputs of the filter op amps are connected to the AGND pin so "clean" ground is mandatory. The AGND pin is protected against static discharge.

Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach will be appropriate. Since this may appear cumbersome and, since the MF10 closely approximates continuous filters, the following discussion is based on the well known frequency domain. The following illustrations refer to ½ of the MF10; the other ½ is identical. Each MF10 can produce a full 2nd order function, so up to 4th order functions can be performed by using cascading techniques.

MODE 1: Notch 1, Bandpass, Lowpass Outputs: $f_{notch} = f_o$ (See *Figure 4*)

f_o = center frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch} = center frequency of the imaginary zero pair $= f_o$.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = -\frac{R2}{R1}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$ = quality factor of the complex pole pair.

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$$

$$H_{OLP\,(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

The above expressions are important. They determine the swing at each output as a function of the desired Q of the 2nd order function.

MODE 1a: Non-Inverting BP, LP (See *Figure 5*)

$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$; $H_{OLP\,(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit dynamics: $H_{OBP_1} = Q$

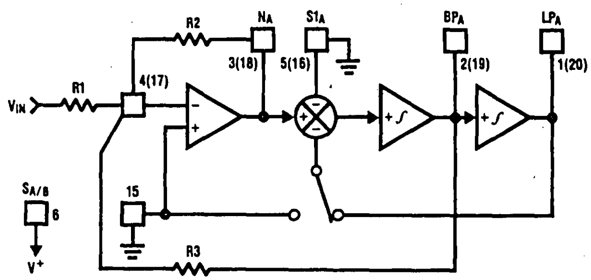

FIGURE 4. MODE 1

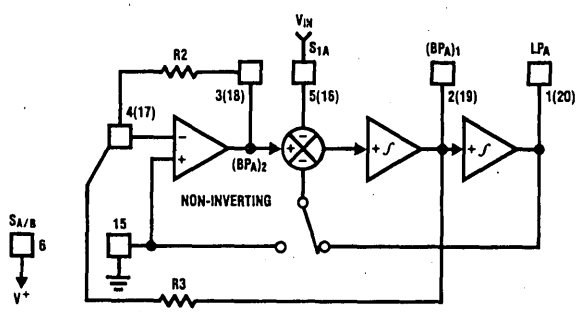

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FIGURE 5. MODE 1a

Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$
(See *Figure 6*)

f_o = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2/R4+1}{R2/R3}}$$

H_{OLP} = Lowpass output gain (as f → 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{OBP} = Bandpass output gain (at $f=f_o$) $-R3/R1$

H_{ON_1} = Notch output gain (as f → 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

$$H_{ON_2} = \text{Notch output gain} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = Q\sqrt{H_{ON_1}\,H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs
(See *Figure 7*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = \text{Highpass gain} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Bandpass gain (at } f=f_o) = -\frac{R3}{R1}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R4}{R1}$$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP} \times Q}$

$H_{OLP\,(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP\,(peak)} \cong Q \times H_{OHP}$ (for high Q's)

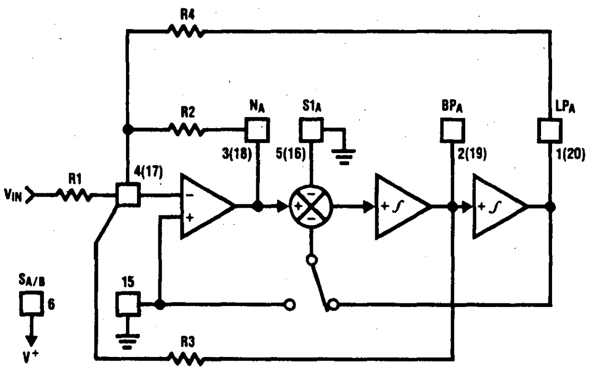
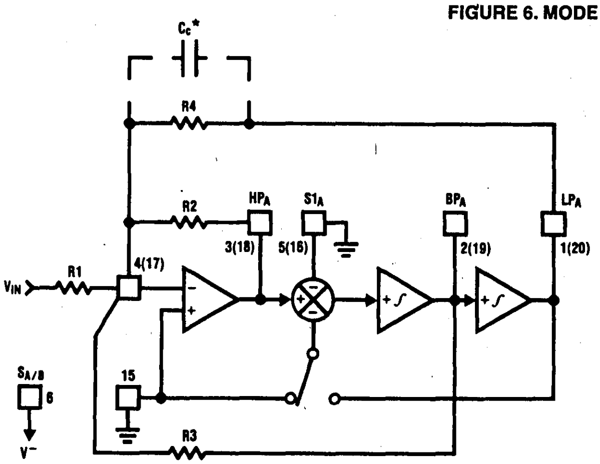


FIGURE 6. MODE 2



* In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF − 100 pF) across R4 to provide some phase lead.

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FIGURE 7. MODE 3

Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op Amp (See *Figure 8*)

$f_o \quad = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

$Q \quad = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$

$H_{OHP} \quad = -\frac{R2}{R1}$

$H_{OBP} \quad = -\frac{R3}{R1}$

$H_{OLP} \quad = -\frac{R4}{R1}$

$f_n \quad$ = notch frequency $= \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$

$H_{ON} \quad$ = gain of notch at $f = f_o = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right) \right\|$

$H_{n1} \quad$ = gain of notch (as $f \rightarrow 0$) $= \frac{R_g}{R_l} \times H_{OLP}$

$H_{n2} \quad$ = gain of notch $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See *Figure 9*)

$f_o \quad$ = center frequency

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$;

f_z^* = center frequency of the complex zero pair $\approx f_o$

$Q \quad = \frac{f_o}{BW} = \frac{R3}{R2}$;

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

$H_{OAP} \quad$ = Allpass gain $\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$

$H_{OLP} \quad$ = Lowpass gain (as $f \rightarrow 0$)

$= -\left(\frac{R2}{R1} + 1\right) = -2$

$H_{OBP} \quad$ = Bandpass gain (at $f = f_o$)

$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

* Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

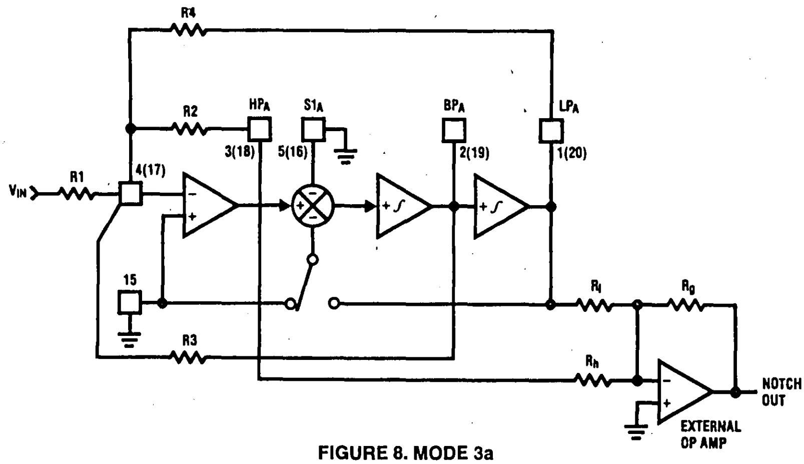

FIGURE 8. MODE 3a

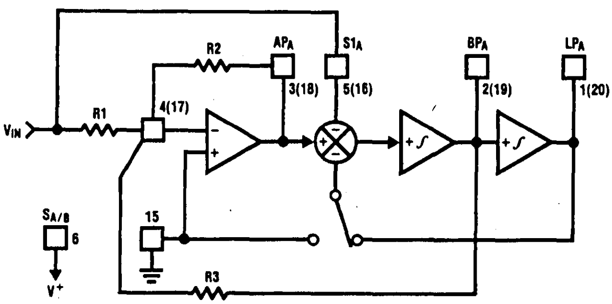

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FIGURE 9. MODE 4

Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 10*)

$$f_o = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1-R2/R4} \times \frac{R3}{R1}$$

$$H_{O_{z1}} = \text{gain at C.z output (as } f \rightarrow 0 \text{ Hz)} = \frac{R2(R4-R1)}{R1(R2+R4)}$$

$$H_{O_{z2}} = \text{gain at C.z output} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2} \right) = \frac{R2}{R1}$$

$$H_{OBP} = \left(\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = \left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, Hp, LP Filter (See *Figure 11*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 12*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP_1} = 1 (non-inverting)

$$H_{OLP_2} = -\frac{R3}{R2}$$

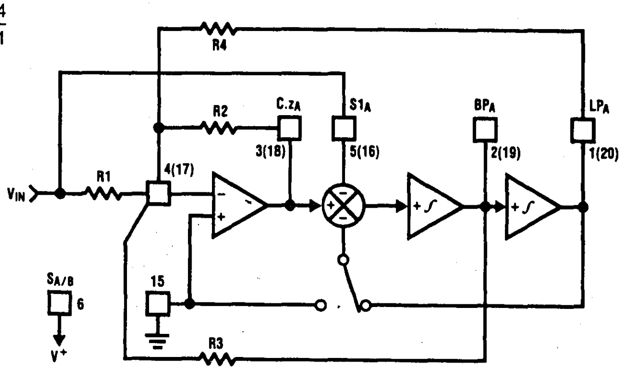

FIGURE 10. MODE 5

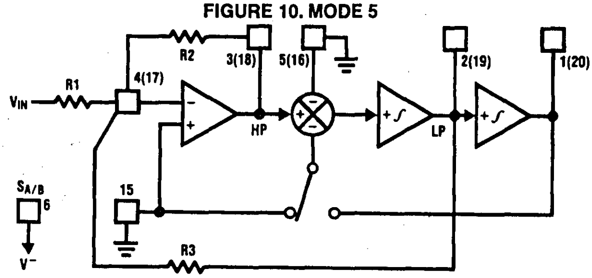

FIGURE 11. MODE 6a

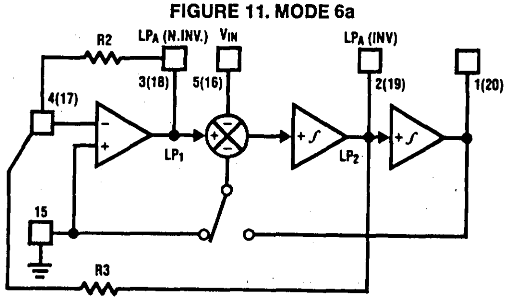

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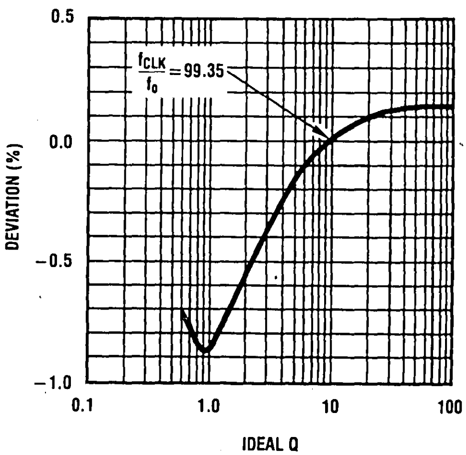
FIGURE 12. MODE 6b

Applications Information

HOW TO USE THE f_{CLK}/f_0 RATIO SPECIFICATION

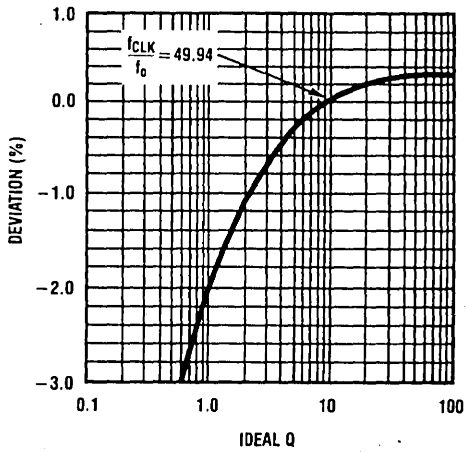
The MF10 is a switched capacitor filter designed to approximate the response of a 2nd order state variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled data filter is a good approximation to its continuous time equivalent. In the case of the MF10, this ratio is about 50:1 or 100:1. Nevertheless the filter's response must be examined in the z-domain in order to obtain the actual response. It can be shown that the clock frequency to center frequency ratio, f_{CLK}/f_0 and the quality factor, Q, deviate from their ideal values determined in the continuous time domain. These deviations are shown graphically in *Figures 13* and *14*. The ratio, f_{CLK}/f_0, is a function of the ideal Q and the largest errors occur for the lowest values of Q.

The curve for the f_{CLK}/f_0 ratio versus the ideal Q has been normalized for a Q of 10 which is the Q value used for the f_{CLK}/f_0 ratio testing of the MF10. At this point the f_{CLK}/f_0 ratio is 49.94 in the 50:1 mode and 99.35 in the 100:1 mode. These values are within a maximum tolerance of $\pm 0.6\%$ (MF10B) and $\pm 1.5\%$ (MF10C). The above tolerances hold for the entire range of Q's; in other words, at 50:1, an MF10B has a ratio of $49.94 \pm 0.6\%$ (Q = 10) and this ratio becomes ($49.44 \pm 0.6\%$) at Q = 2.1. If these small errors cannot be tolerated, the clock frequency or the resistor's ratio, in Mode 3 and Mode 2, can be adjusted accordingly.



TL/H/5645-9

FIGURE 13



TL/H/5645-08

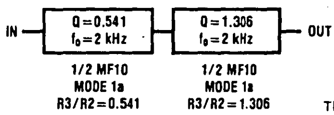
FIGURE 14

A SIMPLE AND INFORMATIVE FILTER DESIGN USING THE MF10

Example 1: Design a 4th order 2 kHz lowpass maximally flat (Butterworth filter). The overall gain of the filter is desired to be equal to 1V/V.

The 4th order filter can be built by cascading two 2nd order sections of (f_0, Q) equal to: Q = 0.541, f_0 = 2 kHz, Q = 1.306, f_0 = 2 kHz.

Due to the low Q values of the filter, the dynamics of the circuit are very good. Any of the modes of operation can be used but Mode 1a is the most simple:



TL/H/5645-10

FIGURE 15

Since for the first section the smallest resistor is R3, choose R3 > 5k. Assume R3 = 10k then R2 = 18.48k. For the second section choose R2 = 10k and then R3 = 13.06k. Both clock input pins (10, 11) can be tied together and then driven with a single external clock. If the approximate ratio $f_{CLK}/100$ is chosen (pin 12 is grounded), then with a 200 kHz clock, the cuftoff frequency, f_c, will be at 2 kHz with a 1.5% maximum error.

The filter schematic is shown in *Figure 16*.

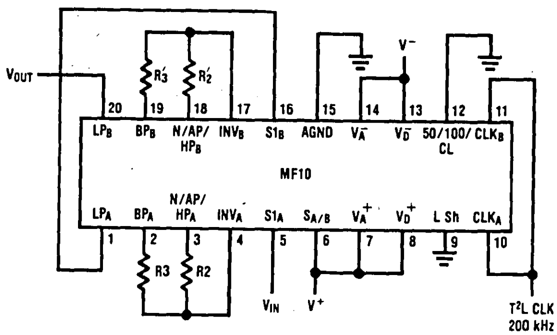


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FIGURE 16. 4th Order, 2 kHZ Lowpass Butterworth Filter

Applications Information (Continued)

With a ±5V supply, each output node of the IC (pins 1, 2, 3, 18, 19, 20) will swing to ±3.8V (MF10B) or ±3.2V (MF10C). The maximum gain of 1.306 occurs at pin 19 at $f_0 \approx 2$ kHz. The input voltage amplitude should be limited to less than 7.6 Vp-p/1.306 = 5.8 Vp-p. If the Q of 1.306 section of the MF10 precedes the Q of 0.541 section, the maximum gain is at pin 1. This gain can be calculated from the expression for H_{OP} given in Definition of Terms, and equals 1.41.

Getting Optimum Cutoff Frequency, f_c, Accuracy (if needed):

In the previous example, an approximate 100:1 ratio was assumed. The true f_{CLK}/f_0 ratio should be read from the curves, *Figures 13* and *14*. At 100:1 the normalized ratio to Q = 10 is: $f_{CLK}/f_0 = 99.35$. For Q's of 0.541 and 1.306 this ratio becomes 99.35 − 0.75% = 98.6. For a 2 kHz f_c, the clock frequency should be 2 kHz × 98.6 = 197.2 kHz.

With an MF10B and a 197.2 kHz clock, the maximum error on the 2 kHz cutoff frequency is ±0.6% as indicated in the specs.

If only a 200 kHz is available in Mode 1a, the true value of f_c and its maximum error is: 200 kHz/(98.6 ± 0.6%) = 2028 ∓ 0.6%.

If only a 200 kHz is available and there is need for a tight tolerance cutoff frequency, then Mode 3 should be used instead of Mode 1a. The resistor ratios are:

1st Section, Q = 0.541	**2nd Section, Q = 1.306**
R2/R4 = 0.972	R2/R4 = 0.972
R3/R2 = 0.548	R3/R2 = 1.324
R4/R1 = 1	R4/R1 = 1

MF10 OFFSETS

The switched capacitor integrators of the MF10 have higher equivalent input offset than the typical R, C integrator of a discrete active filter. These offsets are created by a parasitic charge injection from the switches into the integrating capacitors; they are temperature and clock frequency independent and their sign is shown to be consistent from part to part. The input offsets of the CMOS op amps also add to the overall offset, but their contribution is very small. *Figure 17* shows an equivalent circuit from where output DC offsets can be calculated.

V_{OS1} = 0 mV to ±10 mV

V_{OS2} = charge injected offset plus op amp offset $\cong -120$ mV to -170 mV (at 50:1)

V_{OS3} = charge injected offset plus op amp offset $\cong$ 100 mV to 150 mV (at 50:1)

The V_{OS2} and V_{OS3} numbers approximately double at 100:1.

Output Offsets

The DC offset at the BP output(s) of the MF10 is equal to the input offset of the lowpass switched capacitor integrator, V_{OS3}.

The DC offsets at the remaining outputs are roughly dependent upon the mode of operation and resistor ratios.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \|H_{OLP}\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

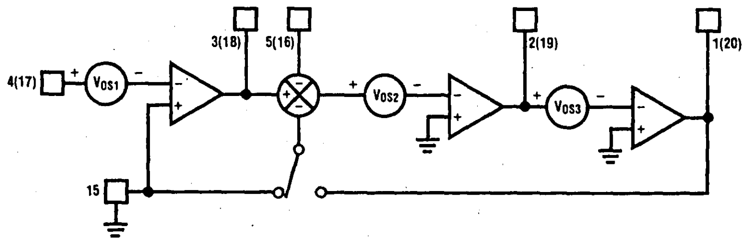

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FIGURE 17

Applications Information (Continued)

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} \pm 1\right) V_{OS1} \times \frac{1}{1+R2/R4} + V_{OS2}\frac{1}{1+R4/R2} - \frac{V_{OS3}}{Q\sqrt{1+R2/R4}};$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3}V_{OS3} + V_{OS2}\right) + \frac{R4}{R2}\left(1+\frac{R2}{R_p}\right)V_{OS1};\ R_p = R1//R3//R4$$

Mode 1a

$$V_{OS}(\text{N.INV.BP}) = \left(1+\frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS}(\text{INV.BP}) = V_{OS3}$$

$$V_{OS}(\text{LP}) = V_{OS}(\text{N.INV.BP}) - V_{OS2}$$

Comments on output DC offsets: For most applications, the outputs are AC coupled and the DC offsets are not bothersome unless large input voltage signals are applied to the filter. For instance, if the BP output is used and it is AC coupled, the remaining two outputs should not be allowed to saturate. If so, gain nonlinearities and f_o, Q errors will occur. For Mode 3 of operation a word of caution is necessary: by allowing small R2/R4 ratios and high Q, the LP output will exhibit a couple of volts of DC offset and an offset adjustment should be made.

An extreme example: Design a 1.76 kHz BP filter with a Q of 21 and a gain equal to unity. The MF10 will be driven with a 250 kHz clock, and it will be switched 50:1.

Resistor values: $\sqrt{\frac{R2}{R4}} = \frac{f_o}{f_{CLK}} \times 50 = 0.352;\ \frac{R2}{R4} = 0.124$

$\frac{R3}{R2} = 21 \times \frac{1}{0.353} = 59.63;\ \frac{R3}{R1} = 1$

Since R3/R2 is the highest resistor ratio, start with R2 = 10k, then R3 ≅ 600k, R1 ≅ 600k, R4 = 80k. Assuming $V_{OS1} = 2$ mV, $V_{OS2} = -150$ mV, $V_{OS3} = 150$ mV, the DC offset at the LP output is $V_{OS(LP)} = +1.2$V. The offset adjustment will be done by injecting a small amount of current into the inverting input of the first op amp, *Figure 18*. This will change the effect V_{OS1}, but the output DC offset of the HP and BP will remain unchanged.

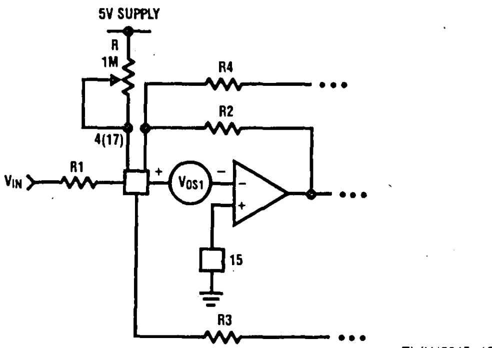


FIGURE 18. V_{OS} Adjust Scheme

Section 5

Telecommunications

5

Introduction

Telecommunications is a rapidly maturing field and has become an important new area for the application of semiconductor products.

With the advent of low-cost silicon electronics, major changes in telephone systems have been taking place. Just a few years ago, telecommunication circuits consisted of only a few products: pulse dialers and tone dialers. Today, with the emphasis on expanding the capacity of existing equipment, digital data is being transmitted across telephone lines. New telecommunications products such as filters, encoders/decoders (CODECs) and combined CODEC/filter chips (COMBOs) have been developed to meet these needs.

The new COMBO chips combine, on a single chip, the complete functions of both the PCM filter and the CODEC. In addition, they consume as little as 50 mW, and can also be put into a 1 mW standby mode.

Since all telephone systems must have auxiliary power sources in the event of loss of electrical power, the new circuits in these more complex systems must be especially geared toward power conservation. To meet this need, National chose microCMOS (a double poly CMOS process).

The resulting circuits not only consume very little power, but also exhibit greatly improved performance. The use of microCMOS has also produced smaller and more cost-effective die for telecommunications chips—not an easy thing to do, considering that these chips combine analog signal processing with digital circuitry.

National's early use of switched-capacitor filters and a microCMOS technology to meet the unique needs of the telecommunications industry has received industry-wide recognition. The company's technological leadership is acknowledged as having made major contributions to the development of the telecommunications field.

National Semiconductor

TP3020/TP3021 Monolithic CODECs

General Description

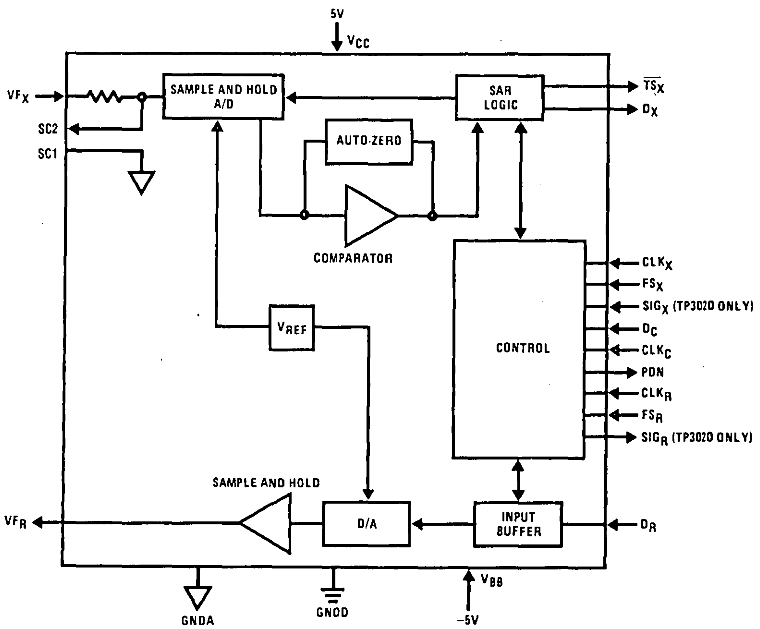
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



TL/H/5538-1

Absolute Maximum Ratings

Operating Temperature	−25°C to + 125°C
Storage Temperature	−65°C to + 150°C
V_{CC} with Respect to GNDD	7V
V_{BB} with Respect to GNDD	−7V
Voltage at Any Analog Input or Output	V_{BB} − 0.3V to V_{CC} + 0.3V
Voltage at Any Digital Input or Output	GNDD − 0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted $T_A = 0°C$ to 70°C, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$. Typical characteristics are specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$ and $T_A = 25°C$. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0 < V_{IN} < V_{CC}$	−10		10	μA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, $I_{OL} = 4.0$ mA SIG_R, $I_{OL} = 0.5$ mA $\overline{TS}_X$, $I_{OL} = 3.2$ mA, Open Drain PDN, $I_{OL} = 1.6$ mA			0.4 0.4 0.4 0.4	V V V V
V_{OH}	Output High Voltage	D_X, $I_{OH} = 6$ mA SIG_R, $I_{OH} = 0.6$ mA	2.4 2.4			V V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V < VF_R < 3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	D_R = PCM Zero Code (TP3020) or Alternating ± 1 Code (TP3021)	−25		25	mV
I_{IN}	Analog Input Bias Current	$V_{IN} = 0V$	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				160	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	0.4	mA
I_{BB0}	Standby Current, V_{BB}			0.03	0.1	mA
I_{CC1}	Operating Current, V_{CC}			4.5	8.0	mA
I_{BB1}	Operating Current, V_{BB}			4..5	8.0	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3020 and TP3021 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the TP3020/TP3021 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	$T = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$				
	TP3020, TP3021		−0.125		0.125	dB
	TP3020-1, TP3021-1		−0.175		0.175	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T = 0°C$ to 70°C	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	$T = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$				
	TP3020, TP3021		−0.325		−0.075	dB
	TP3020-1, TP3021-1		−0.375		−0.025	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T = 0°C$ to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0				
		0 dBm0 to 3 dBm0	−0.3		0.3	dB
		−40 dBm0 to 0 dBm0	−0.2		0.2	dB
		−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		−55 dBm0 to −50 dBm0	−1.0		1.0	dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0				
		0 dBm0 to 3 dBm0	−0.3		0.3	dB
		−40 dBm0 to 0 dBm0	−0.2		0.2	dB
		−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		−55 dBm0 to −50 dBm0	−1.0		1.0	dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level				
		−30 dBm0 to 0 dBm0	35			dBc
		−40 dBm0	29			dBc
		−45 dBm0	25			dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level				
		−30 dBm0 to 0 dBm0	35			dBc
		−40 dBm0	29			dBc
		−45 dBm0	25			dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			6	dBrnC0
N_X	Transmit Idle Channel Noise	TP3020, $VF_X = 0V$ (No Signaling)			13	dBrnC0
		TP3021, $VF_X = 0V$			−66*	dBrn0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			−47	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			−47	dB

AC Electrical Characteristics

(Continued) Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	50			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{CC} = 5.0 V_{DC} + 200 mVrms, F = 1.02 kHz	40			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	50			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 200 mVrms, f = = 1.02 kHz	45			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			−75	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V				
		TP3020			−70	dB
		TP3021			−65*	dB

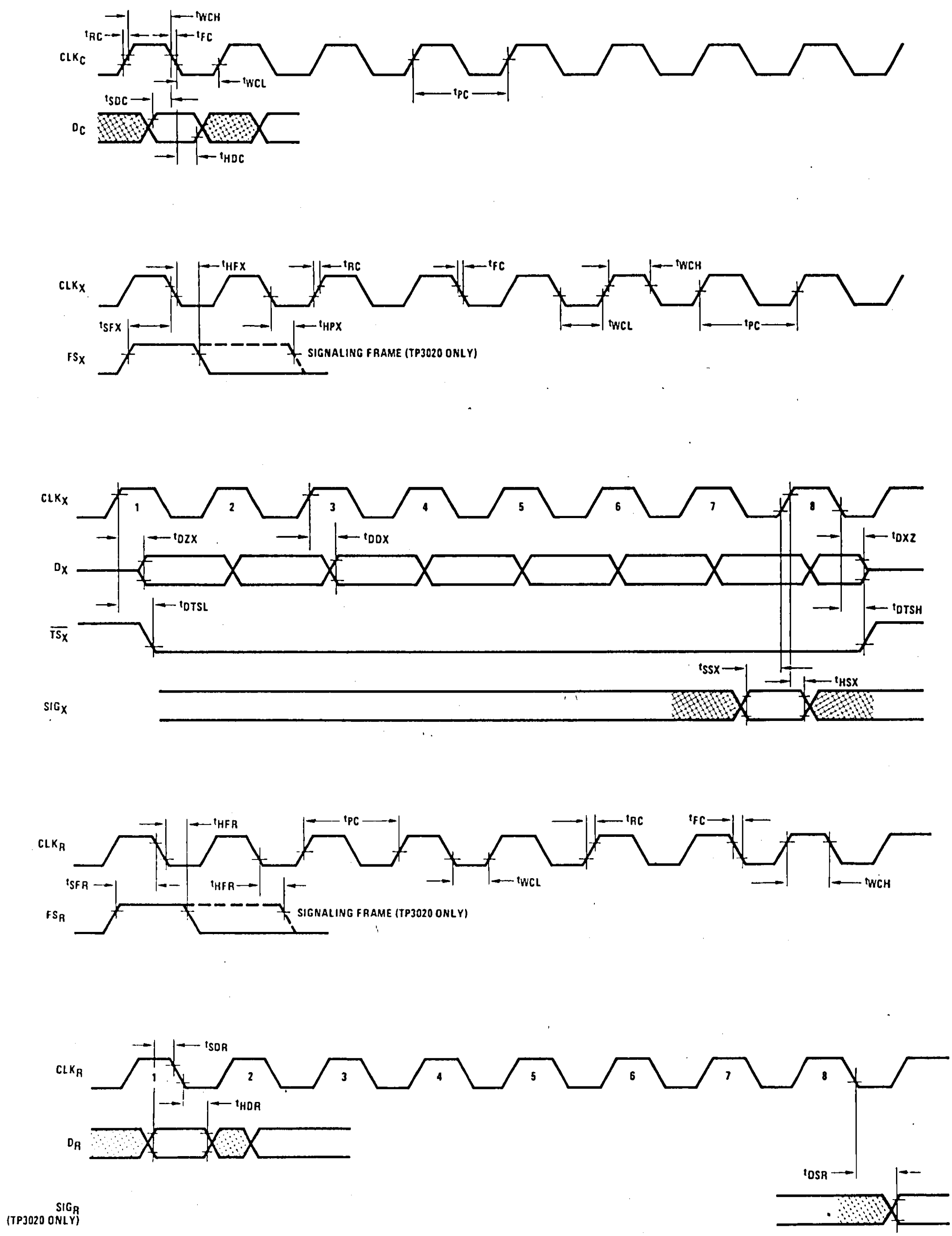
*Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specification

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0 ± 5%, V_{BB} = −5.0 ± 5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the Timing Waveforms.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	485			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	165			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	165			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			16	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			2	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		100			ns
t_{HDC}	Hold Time, CLK_C to DC		100			ns
t_{SFC}	Set-Up Time, FS_X or CLK_X		100			ns
t_{HFX}	Hold Time, CLK_X to FS_X		100			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	C_L = 150 pF	25		125	ns
t_{DDX}	Delay Time, CLK_X to D_X	C_L = 150 pF			125	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	C_L = 0 pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	$0 \leq C_L \leq 150$ pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	C_L = 0 pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		100			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		100			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		100			ns
t_{HFR}	Hold Time, CLK_R to FS_R		100			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		40			ns
t_{HDR}	Hold Time, CLK_R to D_R		30			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	C_L = 100 pF			300	ns

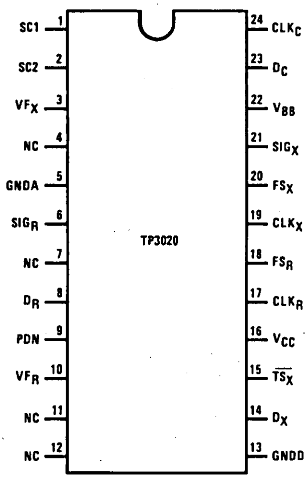
Timing Waveforms



TL/H/5538-2

Connection Diagrams

Dual-In-Line Package

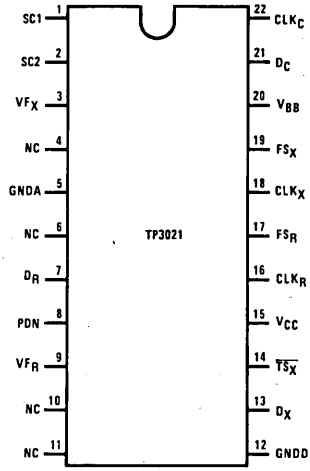


TOP VIEW

TL/H/5538-3

Order Number TP3020J, TP3020J-1
See NS Package J24A

Dual-In-Line Package



TOP VIEW

TL/H/5538-4

Order Number TP3021J, TP3021J-1
See NS Package J22A

Description of Pin Functions

TP3020

Pin No.	Name	Function
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Endures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output—SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.

TP3020 (Continued)

Pin No.	Name	Function
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial CM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE® bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V ($\pm$5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MH_z, 1.544 MH_z or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.

Description of Pin Functions (Continued)

TP3020 (Continued)

Pin No.	Name	Function
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	$-5V$ ($\pm 5\%$) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

TP3021

Pin No.	Name	Function
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the encoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.

TP3021 (Continued)

Pin No.	Name	Function
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE® bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	($5V \pm 5\%$) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz 1.544 MHz, or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	$-5V$ ($\pm 5\%$) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

Functional Description

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated, the TRI-STATE® PCM data output D_X is placed in the high impedance state and the receive signaling output of the TP3020, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the TP3020/TP3021 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μS or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3 − B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the TP3020/TP3021 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the TP3020/TP3021 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The TP3020 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "½" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μS later, resulting in an encoding delay of 125 μS. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μS to 67 μS.

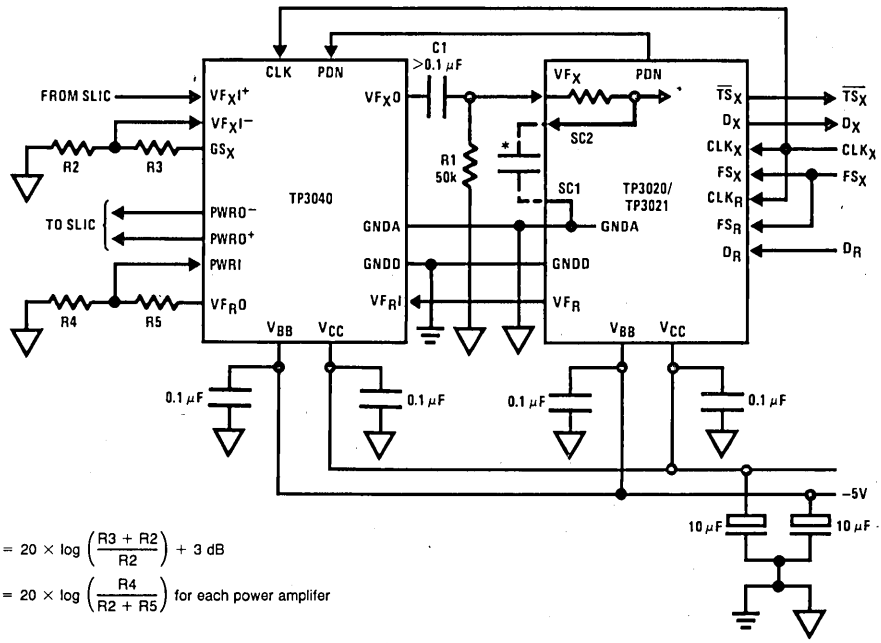
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μS for a 1.544 MHz system with an 8 kHz frame rate or 76 μS for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the TP3020/TP3021 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should not exceed 160 kΩ, and the product R1 × C1 should exceed 4 rms.

Typical Application



$$\text{XMT gain} = 20 \times \log \left(\frac{R3 + R2}{R2}\right) + 3\text{ dB}$$

$$\text{RCV gain} = 20 \times \log \left(\frac{R4}{R2 + R5}\right) \text{ for each power amplifer}$$

TL/H/5538-5

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3020/TP3021/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

*The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pins connect VF_X to this sample/hold capacitor (via a 300Ω resistor) to ensure gain compatibility. The TP3020/TP3021 itself does not require an external sample/hold capacitor.

National Semiconductor

microCMOS

TP3040/TP3040A PCM Monolithic Filter

General Description

The TP3040/TP3040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Exceeds all D3/D4 and CCITT specifications
- +5V, −5V power supplies
- Low power consumption:
  45 mW (0 dBm0 into 600Ω)
  30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block and Connection Diagrams

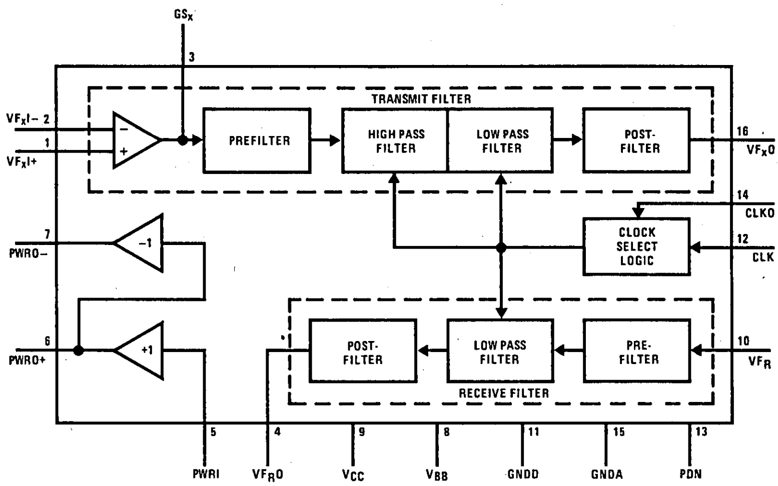
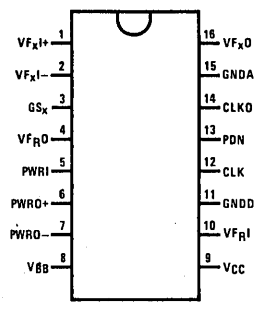


FIGURE 1

Dual-In-Line Package



TOP VIEW

Order Number TP3040J or TP3040AJ
See NS Package J16A

Order Number TP3040N or TP3040AN
See NS Package N16A

Absolute Maximum Ratings

Supply Voltages	±7V
Power Dissipation	1 W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−25°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, clock frequency is 2.048 MHz. Typical parameters are specified at $T_A = 25°C$, $V_{CC} = 5.0V$, $V_{BB} = -5.0V$. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	−10		10	μA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	−100			μA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC} - 0.5V$	−10		−0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		$V_{BB}+0.5$	V
V_{II0}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		$V_{CC}-0.5$		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_xI	Input Leakage Current, VF_xI	$V_{BB} \le VF_xI \le V_{CC}$	−100		100	nA
RI_xI	Input Resistance, VF_xI	$V_{BB} \le VF_xI \le V_{CC}$	10			MΩ
VOS_xI	Input Offset Voltage, VF_xI	$-2.5V \le V_{IN} \le +2.5V$	−20		20	mV
V_{CM}	Common-Mode Range, VF_xI		−2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \le V_{IN} \le 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
VO_xI	Output Voltage Swing, GS_x	$R_L \ge 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \ge 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC Electrical Characteristics

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with $VF_xI = 1.09$ Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-2.5V < V_{OUT} < 2.5V$ $-3.2V < V_{OUT} < 3.2V$	3 10			kΩ kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, $VF_xI+ = 0$ Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (TP3040A) f = 1 kHz (TP3040)	2.9 2.875	3.0 3.0	3.1 3.125	dB dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz (TP3040A)	−1.5		0	dB
		200 Hz (TP3040)	−1.5		0.05	dB
		300 Hz to 3 kHz (TP3040A)	−0.125		0.125	dB
		300 Hz to 3 kHz (TP3040)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, $R_L = 10k$			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3 $T_A = 0°C$ to $70°C$		3	6	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (TP3040A) f = 1 kHz (TP3040)	−0.1 −0.125	0 0	0.1 0.125	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (TP3040A) 300 Hz to 3.0 kHz (TP3040) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −0.125 −0.15 −0.35 −0.7		0.125 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, $R_L = 10k$			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_P+	Gain, PWRI to PWRO+	$R_L = 600\Omega$ Connected Between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 4)		1		V/V
GA_P-	Gain, PWRI to PWRO−			−1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level, Including Receive Filter	$V = 2.05$ Vrms, $R_L = 600\Omega$ (Notes 4, 5)	−0.1		0.1	dB
		$V = 1.75$ Vrms, $R_L = 300\Omega$ (Notes 4, 5)	−0.1		0.1	dB
S/D_P	Signal/Distortion	$V = 2.05$ Vrms, $R_L = 600\Omega$ (Notes 4, 5)			−45	dB
		$V = 1.75$ Vrms, $R_L = 300\Omega$ (Notes 4, 5)			−45	dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	−50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.

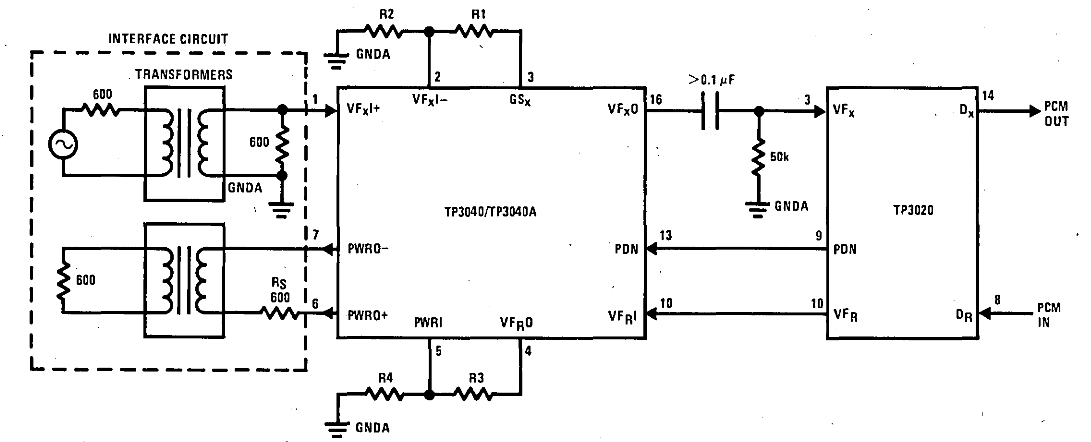
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

Note 3: The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.

Note 4: The 0 dBm0 level for the power amplifiers is load dependent. For $R_L = 600\Omega$ to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For $R_L = 300\Omega$ the 0 dBm0 level is 1.22 Vrms.

Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

Typical Application



Note 1: Transmit voltage gain $= \frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain), ($R1 + R2 \ge 10k$)

Note 2: Receive gain $= \frac{R4}{R3 + R4}$

($P3 + R4 \ge 10k$)

Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5 dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1 dBm across a 600Ω termination impedance.

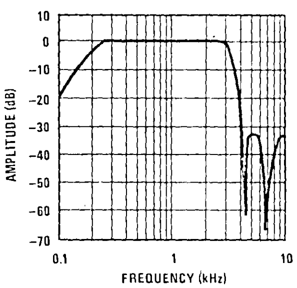
FIGURE 2

Description of Pin Functions

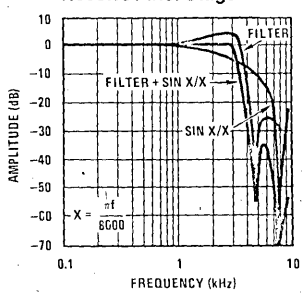
Pin No.	Name	Function
1	VF_XI+	The non-inverting input to the transmit filter stage.
2	VF_XI-	The inverting input to the transmit filter stage.
3	GS_X	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO−	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the TP3040/TP3040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** — **Connect CLK0 to:** 2048 kHz — V_{CC} 1544 kHz — GNDD 1536 kHz — V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_XO	The output of the transmit filter stage.

Typical Performance Characteristics

Transmit Filter Stage



Receive Filter Stage



Functional Description

The TP3040/TP3040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (*Figure 1*). A brief description of the circuit operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10 MΩ, a voltage gain of greater than 10,000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load in parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (*Figure 2*). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW–20 mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW. Connect PDN to GNDD for normal operation.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL - CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

Applications Information

Gain Adjust

Figure 2 shows the signal path interconnections between the TP3040/TP3040A and the TP3020 single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the TP3040/TP3040A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the TP3040/TP3040A filter can be used with the TP3000 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

National Semiconductor

PRELIMINARY

microCMOS

TP3051, TP3056 Monolithic Parallel Data Interface CMOS CODEC/FILTER Family

General Description

The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in *Figure 1,* and a parallel I/O data bus interface. The devices are fabricated on National's advanced double-poly CMOS process (microCMOS).

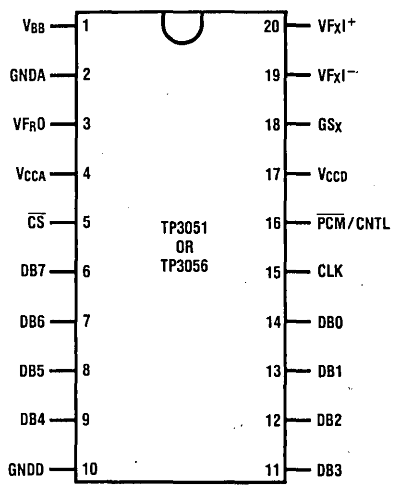
The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads. The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface CODEC/filters for bus-oriented systems. They are ideally suited for use with the TP3100 family of digital line interface controllers (DLIC) in switching system applications. The DLIC communicates with the main switch controller via integrated data, signaling and control channels, and provides local time-slot and space switching capability for up to 32 TP3051 or TP3056 CODECs.

Features

- Complete CODEC and filtering system including:
  - -Transmit high pass and low pass filtering
  - -Receive low pass filter with sin x/x correction
  - -Receive power amplifier
  - -Active RC noise filters
  - -μ-255 law COder and DECoder—TP3051
  - -A-law COder and DECoder—TP3056
  - -Internal precision voltage reference
  - -Internal auto-zero circuitry
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- High speed TRI-STATE® data bus
- 2 loopback test modes

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number TP3051J or TP3056J
See NS Package J20A

Block Diagram

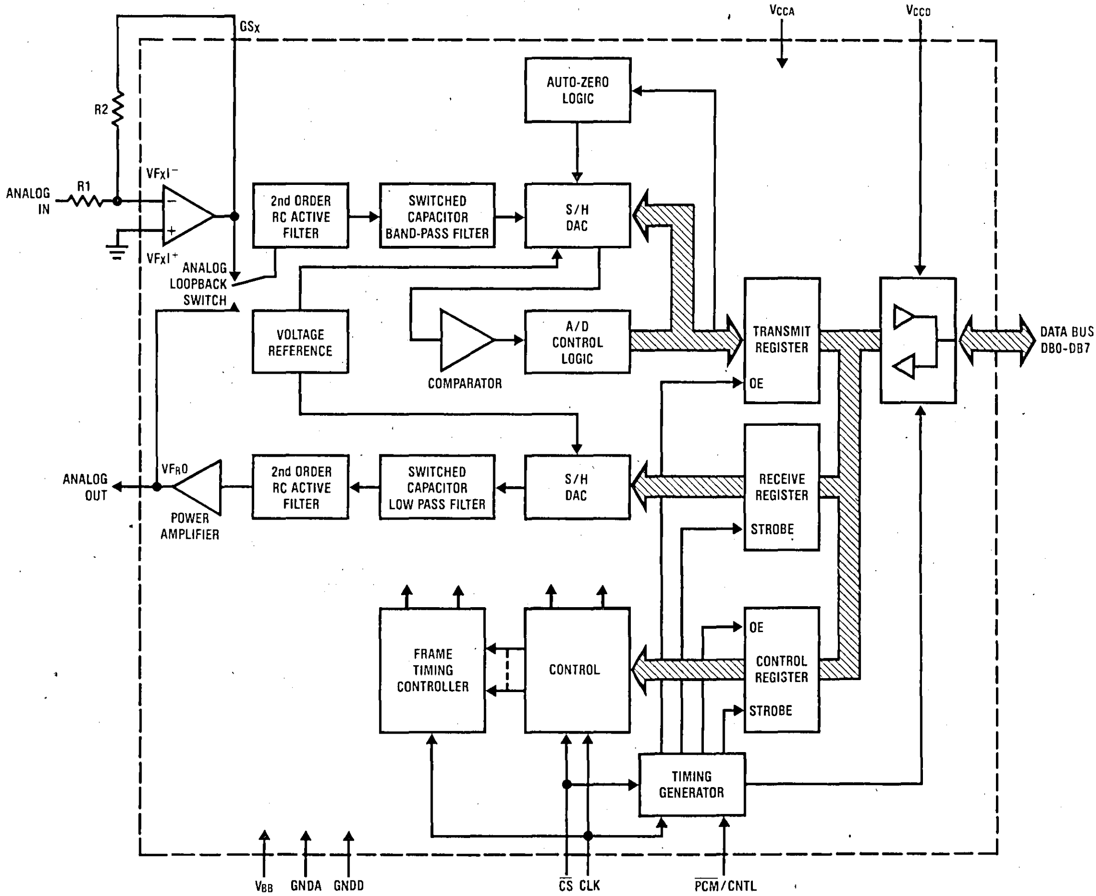


FIGURE 1. Parallel CODEC/Filter

Pin Description

Pin No.	Name	Function
1	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
2	GNDA	Analog ground. All analog signals are referenced to this pin.
3	VF_RO	Analog output of the receive power amplifier. This output can drive a 600Ω load to ±2.5V.
4	V_{CCA}	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5V \pm 5\%$. Must be connected to V_{CCD}.
5	$\overline{CS}$	Device chip select input which controls READ, WRITE and TRI-STATE operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
6	DB7	Bit 7 I/O on the data bus. The PCM LSB.
7	DB6	Bit 6 I/O on the data bus.
8	DB5	Bit 5 I/O on the data bus.
9	DB4	Bit 4 I/O on the data bus.
10	GNDD	Digital ground. All digital signals are referenced to this pin.
11	DB3	Bit 3 I/O on the data bus.
12	DB2	Bit 2 I/O on the data bus.
13	DB1	Bit 1 I/O on the data bus.
14	DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.
15	CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.

Pin Description (Continued)

Pin No.	Name	Function
16	$\overline{\text{PCM}}$/CNTL	This control input determines whether the information on the data bus is PCM data or control data.
17	V_{CCD}	Positive power supply pin for the bus drivers. $V_{CCD} = 5V \pm 5\%$. Must be connected to V_{CCA}.
18	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
19	VF_XI^-	Inverting input of the transmit input amplifier.
20	VF_XI^+	Non-inverting input of the transmit input amplifier.

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table I and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{\text{WRITE}}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in *Figure 4.*

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the CODEC/filter and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0-DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The TP3051, TP3056 is powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

TABLE I. CONTROL BIT FUNCTIONS

Control Bits	Function
C0, C1	Select Clock Frequency **C0 C1 Frequency** 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2, C3	Digital and Analog Loopback **C2 C3 Mode** 1 X digital loopback 0 1 analog loopback 0 0 normal
C4	Power-Down/Power-Up 1 = power-down 0 = power-up
C5	TP3051 — Don't care TP3056 1 = A-law without even bit inversion 0 = A-law with even bit inversion

TABLE I. CONTROL BIT FUNCTIONS (Continued)

Control Bits	Function
C6–C7	Don't care

DATA BUS NOMENCLATURE

The normal order for serial PCM transmission is sign bit first, whereas the normal order for serial data is LSB first. For compatibility with the TP3110/TP3120 DLIC, the parallel data bus is defined as follows:

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{\text{CS}}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If $\overline{\text{PCM}}$/CNTL is low during the falling $\overline{\text{CS}}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame; i.e., at an 8 kHz rate.

If $\overline{\text{PCM}}$/CNTL is high during the falling $\overline{\text{CS}}$ transition, the bus data is latched into the control register. This does not affect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{\text{CS}}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated onto the bus, depending on the level of $\overline{\text{PCM}}$/CNTL at the $\overline{\text{CS}}$ transition. If $\overline{\text{PCM}}$/CNTL is low during the $\overline{\text{CS}}$ falling transition, the transmit register data is written to the bus. An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame; i.e., at an 8 kHz rate.

If $\overline{\text{PCM}}$/CNTL is high during the $\overline{\text{CS}}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the TP3051 and TP3056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select
   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits

Functional Description (Continued)

C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback
   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the TP3051, TP3056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.
3. Analog Loopback
   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.
4. Power-Down/Power-Up
   The TP3051, TP3056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 powers-up the device.

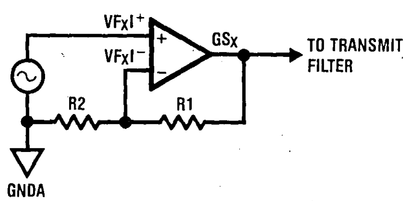
TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 2*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (TP3051) or A-law (TP3056) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

DECODER AND RECEIVE FILTER SECTION

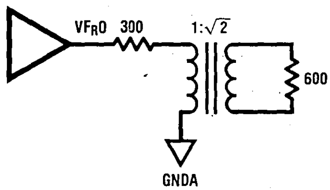
The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (TP3056) or μ-law (TP3051) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600Ω load to a level of 7.2 dBm. The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.



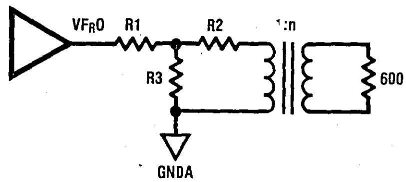
Non-inverting transmit gain $= 20 \log_{10} \left(\frac{R1 + R2}{R2}\right)$

Set gain to provide peak overload level $= t_{MAX}$ at GS_X (see Transmission Characteristics)

FIGURE 2. Transmit Gain Adjustment



Maximum output power = 7.2 dBm total, 4.2 dBm to the load.



See Applications Information for attenuator design guide.

FIGURE 3. Receive Gain Adjustment

Absolute Maximum Ratings

GNDD to GNDA	± 0.3V
V_{CCA} or V_{CCD} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at Any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GNDD − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, $T_A = 0°C$ to 70°C; typical characteristics specified at nominal supply voltages, $T_A = 25°C$; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	DB0–DB7, $I_L = 2.5$ mA			0.4	V
V_{OH}	Output High Voltage	DB0–DB7, $I_H = -2.5$ mA	2.4			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	$V_{IH} \le V_{IN} \le V_{CC}$	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	−10		10	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	−200		200	nA
R_IXA	Input Resistance	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	$R_L = 10$ kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	5000			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
RECEIVE POWER AMPLIFIER (ALL DEVICES)						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	600			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
I_{CC0}	Power-Down Current			0.5	1.5	mA
I_{BB0}	Power-Down Current			0.05	0.3	mA
I_{CC1}	Active Current			6.0	9.0	mA
I_{BB1}	Active Current			6.0	9.0	mA

Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock		760		ns
t_{WCH}	Width of Clock High		330		ns
t_{WCL}	Width of Clock Low		330		ns
t_{RC}	Rise Time of Clock			50	ns
t_{FC}	Fall Time of Clock			50	ns
t_{SCS}	Set-Up Time of CLK High or Low		100		ns
t_{HCS}	Hold Time from $\overline{CS}$ Low to CLK		100		ns
t_{WCS}	Width of Chip Select		100		ns
t_{SPCM}	Set-Up Time of PCM/CNTL		0		ns
t_{HPCM}	Hold Time of PCM/CNTL		100		ns
t_{SDI}	Set-Up Time of Data In		50		ns
t_{HDI}	Hold Time of Data In		20		ns
t_{DDO}	Delay Time to Data Out Valid	$C_L = 0$ pF to 200 pF	90	260	ns
t_{DDZ}	Delay Time to Data Output Disabled	$C_L = 0$ pF to 200 pF	20	80	ns

Switching Time Waveforms

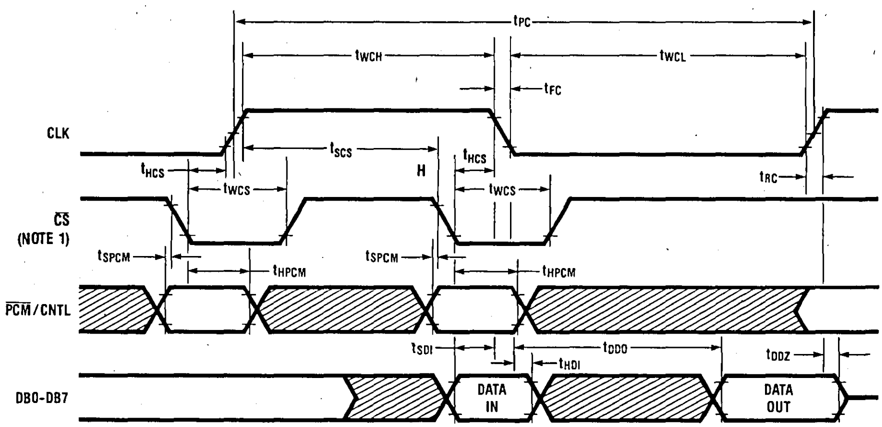


FIGURE 4. Timing Waveforms for TP3051, TP3056

Note 1: This diagram shows that READ and WRITE $\overline{CS}$ pulses may occur on consecutive half-cycles of CLK, although this is not a restriction. READ and WRITE $\overline{CS}$ pulses must each occur at an 8 kHz rate.

Transmission Characteristics (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
	0 dBm0	TP3051		1.2276		Vrms
		TP3056		1.2276		Vrms
t_{MAX}	Maximum Overload Level	TP3051 (+3.17 dBm0)		2.501		V_{DC}
		TP3056 (+3.14 dBm0)		2.492		V_{DC}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CCA} = V_{CCD} = 5.0V$, $V_{BB} = -5.0V$ Input at GS_X = 0 dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz			−40	dB
		f = 50 Hz			−30	dB
		f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz-3000 Hz	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	dB
		f = 3400 Hz	−0.7		0	dB
		f = 4000 Hz			−14	dB
		f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			−32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Test Method Reference Level = −10 dBm0				
		VF_XI^+ = −40 dBm0 to +3 dBm0	−0.2		0.2	dB
		VF_XI^+ = −50 dBm0 to −40 dBm0	−0.4		0.4	dB
		VF_XI^+ = −55 dBm0 to −50 dBm0	−1.2		1.2	dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CCA} = V_{CCD} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	dB
		f = 3400 Hz	−0.7		0	dB
		f = 4000 Hz			−14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded −10 dBm0 Signal				
		PCM Level = −40 dBm0 to +3 dBm0	−0.2		0.2	dB
		PCM Level = −50 dBm0 to −40 dBm0	−0.4		0.4	dB
		PCM Level = −55 dBm0 to −50 dBm0	−1.2		1.2	dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz-600 Hz		195	220	μs
		f = 600 Hz-800 Hz		120	145	μs
		f = 800 Hz-1000 Hz		50	75	μs
		f = 1000 Hz-1600 Hz		20	40	μs
		f = 1600 Hz-2600 Hz		55	75	μs
		f = 2600 Hz-2800 Hz		80	105	μs
		f = 2800 Hz-3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz-1000 Hz	−40	−25		μs
		f = 1000 Hz-1600 Hz	−30	−20		μs
		f = 1600 Hz-2600 Hz		70	90	μs
		f = 2600 Hz-2800 Hz		100	125	μs
		f = 2800 Hz-3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3051, $VF_XI^+ = 0V$		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3056, $VF_XI^+ = 0V$		−74	−69 (Note1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3051, PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3056, PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0V$			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_XI^+ = 0V$, $V_{CCA} = V_{CCD} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 kHz-50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 kHz-50 kHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz-4000 Hz	40			dBC
		f = 4 kHz-25 kHz	40			dBC
		f = 25 kHz-50 kHz	36			dBC
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz-4000 Hz	40			dBC
		f = 4 kHz-25 kHz	40			dBC
		f = 25 kHz-50 kHz	36			dBC
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz-3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz-7600 Hz			−32	dB
		7600 Hz-8400 Hz			−40	dB
		8400 Hz-100,000 Hz			−32	dB

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X	Signal to Total Distortion	Sinusoidal Test Method				
STD_R	Transmit or Receive Half-Channel	Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to −30 dBm0	36			dBC
		= −40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= −55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			−41	dB
CROSSTALK						
$CT_{X\text{-}R}$	Transmit to Receive Crosstalk 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz at 0 dBm0 Steady PCM Receive Code		−90	−75	dB
$CT_{R\text{-}X}$	Receive to Transmit Crosstalk 0 dBm0 Receive Level	f = 300 Hz–3400 Hz		−90	−70 (Note 2)	dB

Note 1: Measured by extrapolation from the distortion test result.

Note 2: $CT_{R\text{-}X}$ is measured with a −40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT DATA BUS OUTPUT

	TP3051 μ-Law	TP3056 True A-Law, C5 = 0 (Includes Even Bit Inversion)
	MSB LSB	MSB LSB
V_{IN} = + Full-Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} = − Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0
	Not Applicable (C5 is Don't Care)	**Sign + Magnitude A-Law, C5 = 1 (Before Even Bit Inversion)**
V_{IN} = + Full-Scale		1 1 1 1 1 1 1 1
V_{IN} = 0V		1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
V_{IN} = − Full-Scale		0 1 1 1 1 1 1 1

Applications Information

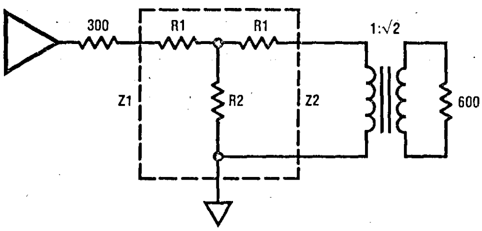
POWER SUPPLIES

While the pins of the TP3051 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each CODEC/filter, not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{BB}.

For best performance, the ground point of each CODEC/filter on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

Where: $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

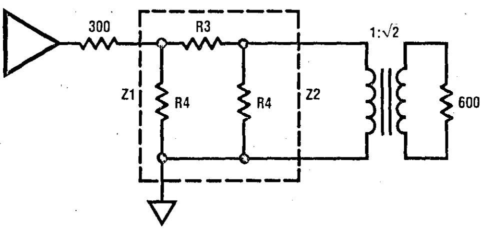
$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC} \bullet Z_{OC}}$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



$$R3 = \sqrt{\frac{Z1.Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the CODEC and filter circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the CODEC/filter at the point where the 0.1 μF decoupling capacitor is connected.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

TABLE II. ATTENUATOR TABLES FOR Z1 = Z2 = 300Ω (ALL VALUES IN Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Note: See Applications Brief 13 for further details.

Typical Applications

The benefits of a CODEC/filter with a parallel data bus, rather than the usual serial port, are illustrated in *Figure 5*. This shows a 16-channel line card in which the TP3051, TP3056 CODEC/filters share the data bus interface to a TP3110/TP3120 digital line interface controller. The DLIC can access up to 128 channels on the serial backplane, providing fully non-blocking time and space switching capability with optional redundancy. In conjunction with a local microprocessor, typically from the INS8048 family, a standard HDLC control channel can be assigned, providing secure message capability between the line card and the system control processor. The local microprocessor can also collect and process line status and signaling information, off-loading these tasks from the main processor. A prioritized vectored interrupt scheme is used for data transfers between the microprocessor and DLIC.

System flexibility can be further enhanced by adding 2 additional bits per frame to the PCM data, operating the DLIC with 80 Kb/s channels rather than 64 Kb/s channels.

Another application of the T3051, TP3056 CODEC/filters is in the all-digital telephone. The analog and digital loop-back test modes are particularly useful, enabling the switching system to verify the integrity of virtually the complete channel. The transmit op amp can be set for gains in excess of 20 dB, enabling a simple AC connection to an electret microphone (with integral FET buffer) to be made. A receive transducer with an impedance not less than 600Ω can be driven directly by the receive amplifier, with a resistive network providing gain adjustment and sidetone. Low impedance transducers require an audio matching transformer.

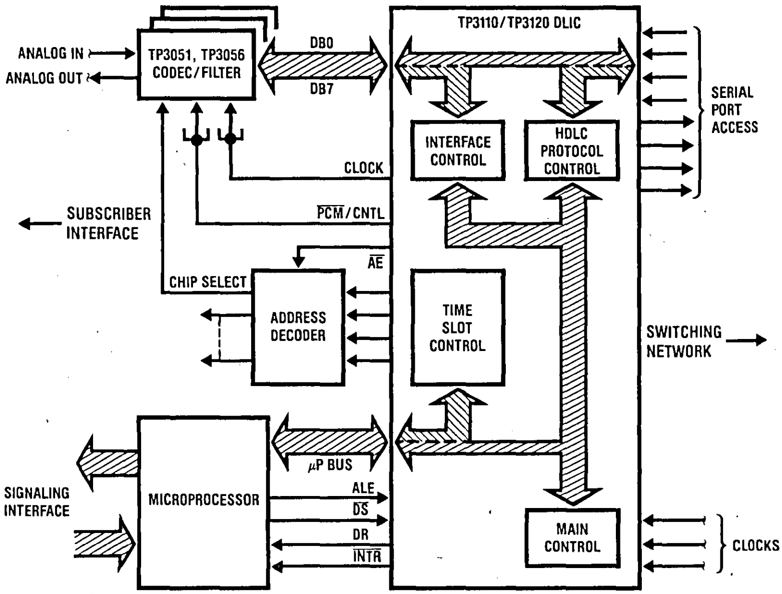


FIGURE 5. Typical 16-Channel Line Card

National Semiconductor

TP3052, TP3053, TP3054, TP3057 Monolithic Serial Interface CMOS CODEC/FILTER Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

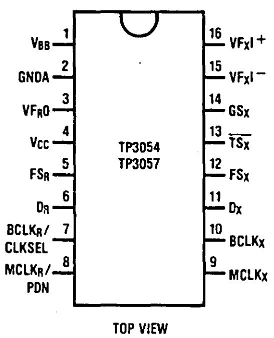
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

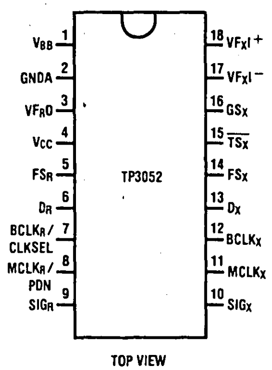
Connection Diagrams

Dual-In-Line Package



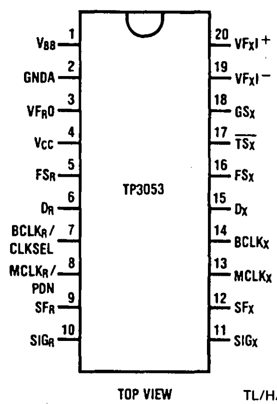
Order Number TP3054J or TP3057J
NS Package Number J16A

Dual-In-Line Package



Order Number TP3052J
NS Package Number J18A

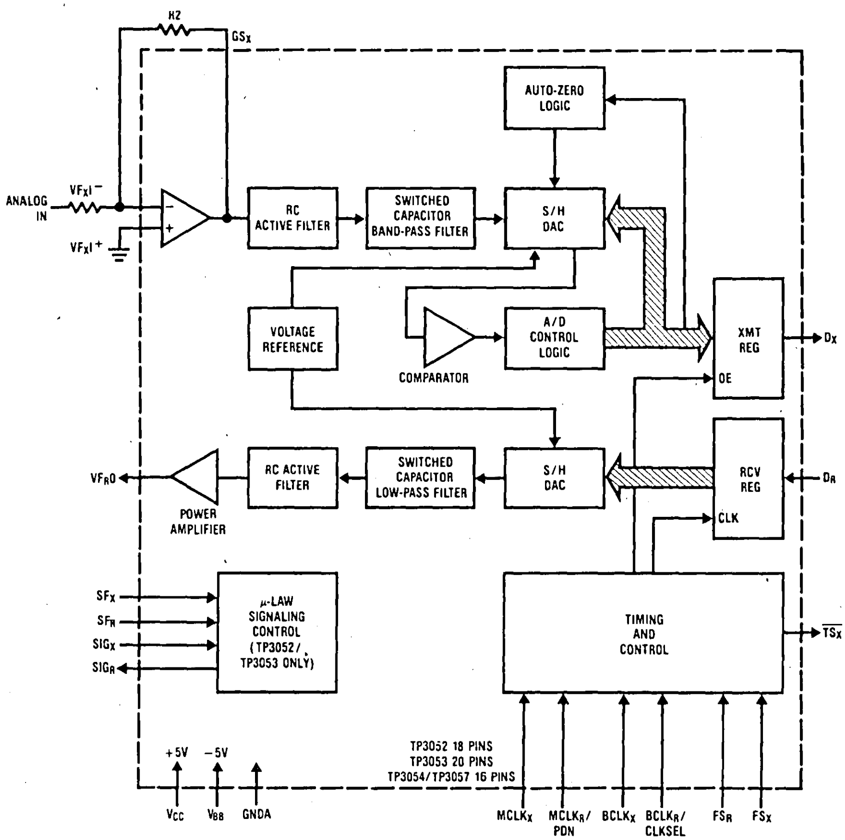
Dual-In-Line Package



TL/H/5510-1

Order Number TP3053J
NS Package Number J20A

Block Diagram



TL/H/5510-2

FIGURE 1

Pin Description

TP3052 Pin No.	TP3053 Pin No.	TP3054 TP3057 Pin No.	Name	Function
1	1	1	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
2	2	2	GNDA	Analog ground. All signals are referenced to this pin.
3	3	3	VF_RO	Analog output of the receive filter.
4	4	4	V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
5	5	5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
6	6	6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	7	7	$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
8	8	8	$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Pin Description (Continued)

TP3052 Pin No.	TP3053 Pin No.	TP3054 TP3057 Pin No.	Name	Function
—	9	—	SF_R	When high during FS_R, this input indicates a receive signal frame.
9	10	—	SIG_R	The eighth bit of the PCM data appears at this output after each receive signaling frame.
10	11	—	SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
—	12	—	SF_X	When high during FS_X, this input indicates a transmit signaling frame.
11	13	9	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
14	16	12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
12	14	10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
13	15	11	D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
15	17	13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	18	14	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
17	19	15	VF_XI^-	Inverting input of the transmit input amplifier.
18	20	16	VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE 1. SELECTION OF MASTER CLOCK FREQUENCIES

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Functional Description (Continued)

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse (the same as the TP5116A family of CODECs). Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A-type) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ-law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "½" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μS (due to the transmit filter) plus 125 μS (due to encoding delay), which totals 290 μS. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μS later the decoder DAC output is updated. The total decoder delay is ~ 10 μS (decoder update) plus 110 μS (filter delay) plus 62.5 μS (½ frame), which gives approximately 180 μS.

Absolute Maximum Ratings

V_{CC} to GNDA 7V
V_{BB} to GNDA −7V
Voltage at any Analog Input or Output $V_{CC}+0.3V$ to $V_{BB}-0.3V$
Voltage at any Digital Input or Output $V_{CC}+0.3V$ to GNDA−0.3V
Operating Temperature Range −25°C to + 125°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics

Unless otherwise noted: $V_{CC}=5.0V\pm5\%$, $V_{BB}=-5V\pm5\%$, GNDA=0V, T_A=0°C to 70°C; typical characteristics specified at $V_{CC}=5.0V$, $V_{BB}=-5.0V$, T_A=25°C;all signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L=3.2 mA SIG_R, I_L=1.0 mA $\overline{TS_X}$, I_L=3.2 mA, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	D_X, I_H=−3.2 mA SIG_R, I_H=−1.0 mA	2.4 2.4			V V
I_{IL}	Input Low Current	GNDA≤V_{IN}≤V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	V_{IH}≤V_{IN}≤V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA≤V_O≤V_{CC}	−10		10	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	−2.5V≤V≤+2.5V, VF_XI^+ or VF_XI^-	−200		200	nA
R_IXA	Input Resistance	−2.5V≤V≤+2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L≤10 kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO= ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current			0.5	1.5	mA
$I_{BB}0$	Power-Down Current			0.05	0.3	mA
$I_{CC}1$	Active Current			6.0	9.0	mA
$I_{BB}1$	Active Current			6.0	9.0	mA

Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100			ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	$V_{IH} = 2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL} = 0.6V$	160			ns
t_{RB}	Rise Time of Bit Clock	$t_{PB} = 488$ ns			50	ns
t_{FB}	Fall Time of Bit Clock	$t_{PB} = 488$ ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	$C_L = 0$ pF to 150 pF	20		165	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	TP3053 Only	60			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	TP3053 Only	60			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052 and TP3053	100			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052 and TP3053	50			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{DFSSG}	Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	Load = 50 pF plus 2 LSTTL Loads			300	ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	TP3053 Only	100			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

Timing Diagrams

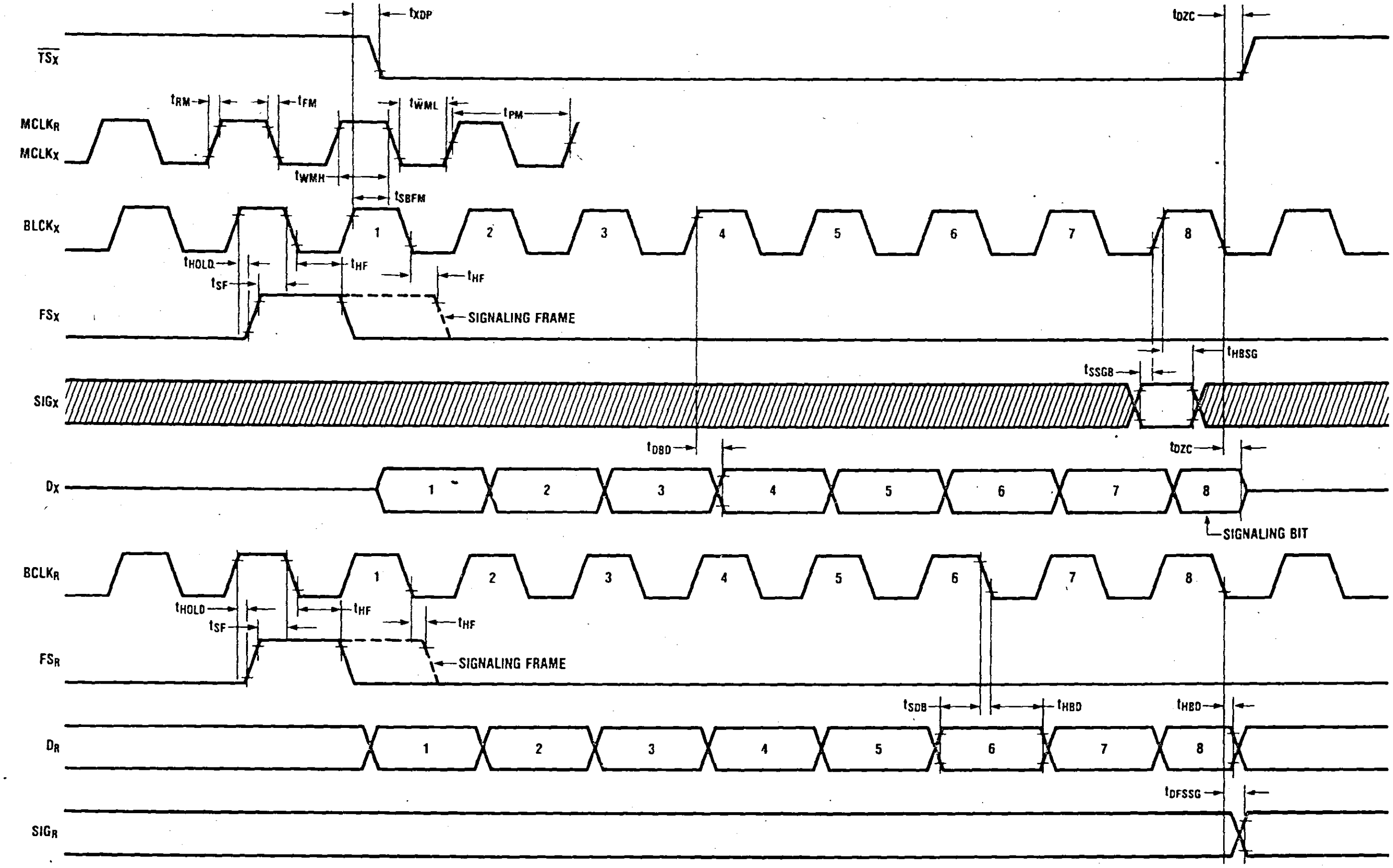
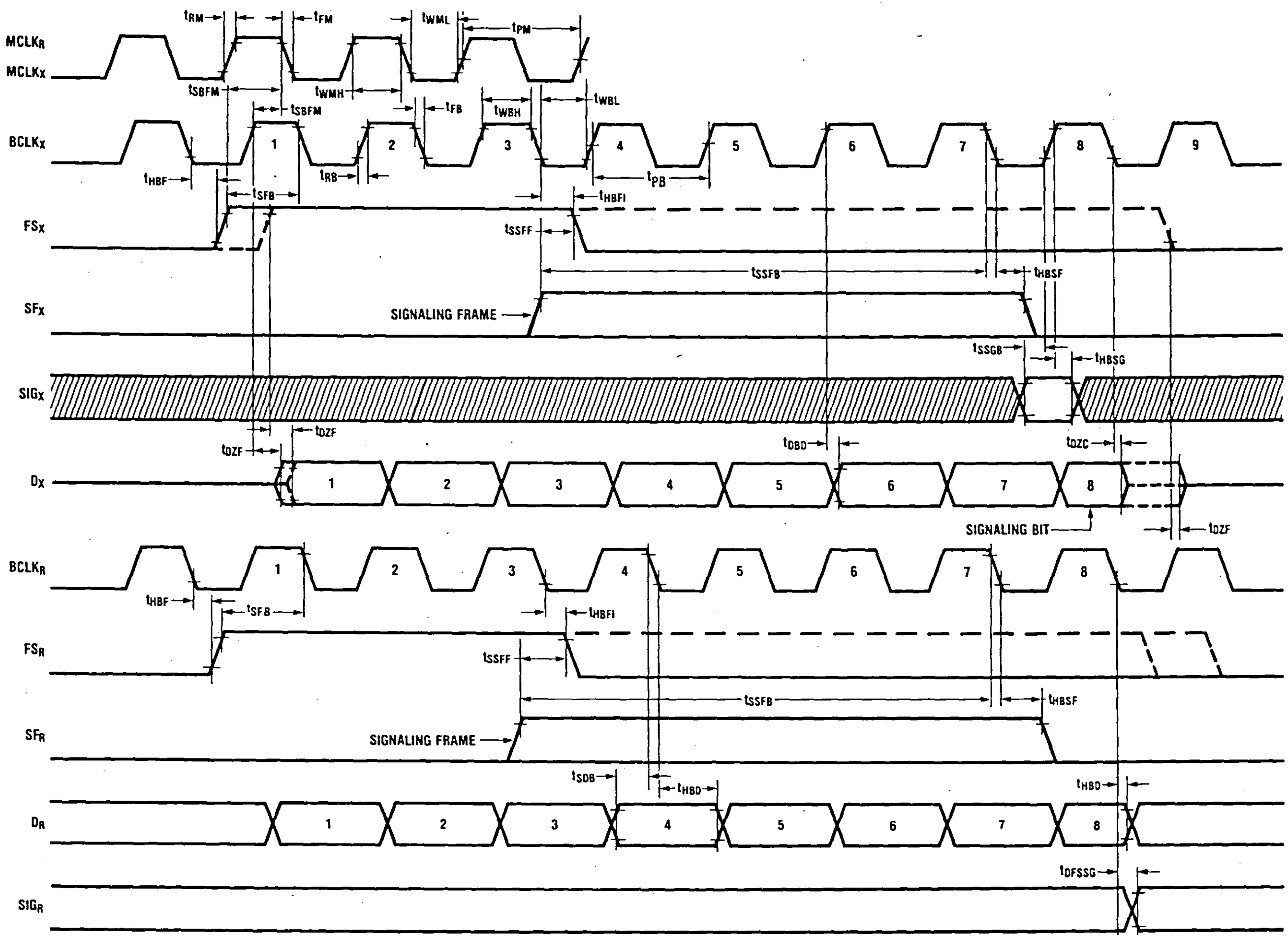


FIGURE 2. Short Frame Sync Timing

Timing Diagrams (Continued)



TL/H/5510–4

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
		0 dBm0				
		TP3052, TP3053, TP3054		1.2276		Vrms
		TP3057		1.2276		Vrms
t_{MAX}		Max Overload Level				
		TP3052, TP3053, TP3054 (3.17 dBm0)		2.501		V_{PK}
		TP3057 (3.14 dBm0)		2.492		V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input at GS_X = 0 dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz			−40	dB
		f = 50 Hz			−30	dB
		f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz − 3000 Hz	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	dB
		f = 3400 Hz	−0.7		0	dB
		f = 4000 Hz			−14	dB
		f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			−32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0				
		VF_XI+ = −40 dBm0 to +3 dBm0	−0.2		0.2	dB
		VF_XI+ = −50 dBm0 to −40 dBm0	−0.4		0.4	dB
		VF_XI+ = −55 dBm0 to −50 dBm0	−1.2		1.2	dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	dB
		f = 3400 Hz	−0.7		0	dB
		f = 4000 Hz			−14	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded—10 dBm0 Signal				
		PCM Level = −40 dBm0 to + 3 dBm0	−0.2		0.2	dB
		PCM Level = −50 dBm0 to −40 dBm0	−0.4		0.4	dB
		PCM Level = −55 dBm0 to −50 dBm0	−1.2		1.2	dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	µS
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	µS
		f = 600 Hz–800 Hz		120	145	µS
		f = 800 Hz–1000 Hz		50	75	µS
		f = 1000 Hz–1600 Hz		20	40	µS
		f = 1600 Hz–2600 Hz		55	75	µS
		f = 2600 Hz–2800 Hz		80	105	µS
		f = 2800 Hz–3000 Hz		130	155	µS
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	µS
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		µS
		f = 1000 Hz–1600 Hz	−30	−20		µS
		f = 1600 Hz–2600 Hz		70	90	µS
		f = 2600 Hz–2800 Hz		100	125	µS
		f = 2800 Hz–3000 Hz		145	175	µS
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054 $VF_XI^+ = 0V$		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057 $VF_XI^+ = 0V$		−74	−69 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3052, TP3053, TP3054 PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 kHz–50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 kHz–50 kHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	40			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	40			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			−32	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−32	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method				
		Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to −30 dBm0	36			dBC
		= −40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= −55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $VF_X^+ = -4$ dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			−41	dB
CROSSTALK						
$CT_{X\text{-}R}$	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Steady PCM Code		−90	−75	dB
$CT_{R\text{-}X}$	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, $VF_XI = 0V$		−90	−70 (Note 2)	dB

Note 1: Measured by extrapolation from the distortion test result.

Note 2: $CT_{R\text{-}X}$ is measured with a -40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ-Law	TP3057 A-Law (Includes Even Bit Inversion)
V_{IN} (at GS_X) = + Full-Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = − Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

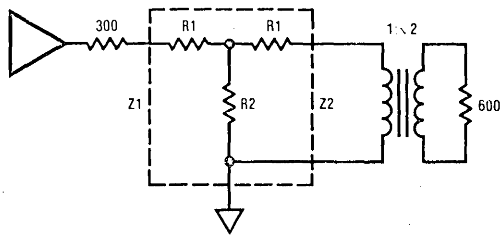
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

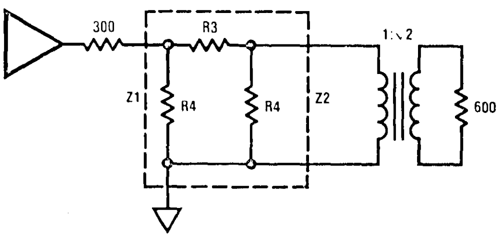
$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC} \bullet Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



$$R3 = \sqrt{\frac{Z1.Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

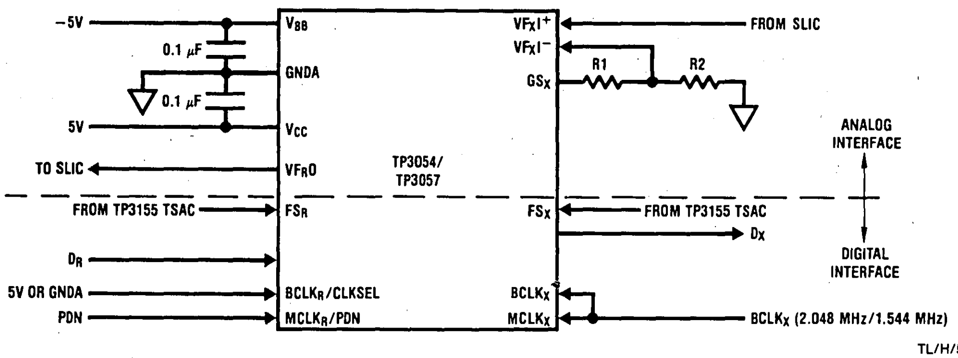
Note: See Applications Brief 13 for further details.

Applications Information (Continued)

TABLE II. ATTENTUATOR TABLES FOR Z1 = Z2 = 300Ω (ALL VALUES IN Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



Note 1: XMIT gain $= 20 \times \log \left(\frac{R1+R2}{R2}\right)$, $(R1+R2) > 10\ K\Omega$.

FIGURE 4

National Semiconductor

PRELIMINARY

TP3064, TP3067 Monolithic Serial Interface CMOS CODEC/FILTER Combos

General Description

The TP3064 (μ-law) and TP3067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the TP3050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and $\overline{TS_X}$ output.

Features

- Complete CODEC and filtering system including:
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - μ-law or A-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
  - Receive push-pull power amplifiers
- μ-law—TP3064
- A-law—TP3067
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

5

Block Diagram

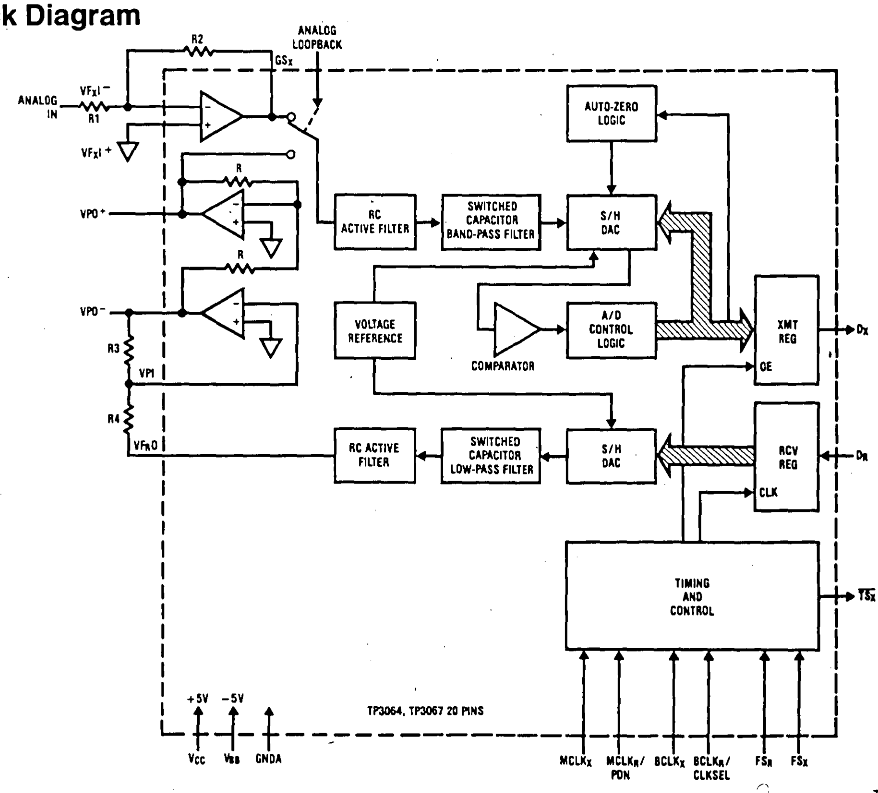


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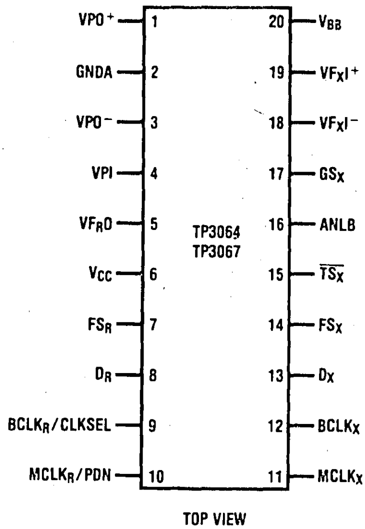
FIGURE 1

Connection Diagram

Dual-In-Line Package



TL/H/5070-2

Order Number TP3064J, TP3067J
See NS Package J20A

Pin Description

TP3064 TP3067 Pin No.	Name	Function
1	VPO+	The non-inverted output of the receive power amplifier.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VPO−	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
7	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
8	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
9	$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
10	$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Pin Description (Continued)

TP3064 TP3067 Pin No.	Name	Function
11	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
12	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
13	D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
14	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
18	VF_XI^-	Inverting input of the transmit input amplifier.
19	VF_XI^+	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X, VF_RO, VPO^- and VPO^+ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BLCK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. SELECTION OF MASTER CLOCK FREQUENCIES

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3067	TP3064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHZ	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.544 MHz

Functional Description (Continued)

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3067, or 1.536 MHZ, 1.544 MHz for the TP3064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse (the same as the TP5116A family of CODECs). Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2.* With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A-type) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3.* Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 5.* The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3064) or A-law (TP3067) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

ENCODING FORMAT AT D_X OUTPUT

	TP3064 μ-Law								TP3067 A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Functional Description (Continued)

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3067) or μ-law (TP3064) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5V peak output signal from the receive filter up to ±3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}:1$ turns ratio, as shown in *Figure 2*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12 mW of power.

Absolute Maximum Ratings

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC}+0.3V to V_{BB}−0.3V
Voltage at any Digital Input or Output	V_{CC}+0.3V to GNDA−0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise noted: V_{CC}=5.0V±5%, V_{BB}=−5V±5%, GNDA=0V, T_A=0°C to 70°C; typical characteristics specified at V_{CC}=5.0V, V_{BB}=−5.0V, T_A=25°C; all signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current			0.5	1.5	mA
$I_{BB}0$	Power-Down Current			0.05	0.3	mA
$I_{CC}1$	Active Current	Power Amplifiers Active, VPI=0V		7.0	10.0	mA
$I_{BB}1$	Active Current	Power Amplifiers Active, VPI=0V		7.0	10.0	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L=3.2 mA SIG_R, I_L=1.0 mA $\overline{TS_X}$, I_L=3.2 mA, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	D_X, I_H=−3.2 mA SIG_R, I_H=−1.0 mA	2.4 2.4			V V
I_{IL}	Input Low Current	GNDA≤V_{IN}≤V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	V_{IH}≤V_{IN}≤V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA≤V_O≤V_{CC}	−10		10	μA

Electrical Characteristics (Continued)

Unless otherwise noted: $V_{CC}=5.0V \pm 5\%$, $V_{BB}=-5V \pm 5\%$, GNDA=0V, $T_A=0°C$ to 70°C; typical characteristics specified at $V_{CC}=5.0V$, $V_{BB}=-5.0V$, $T_A=25°C$; all signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	−200		200	nA
R_IXA	Input Resistance	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \ge 10$ kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	5000			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	10			kΩ
C_LRF	Load Capacitance	VF_RO to GNDA			25	pF
VOS_RO	Output DC Offset Voltage	VF_RO to GNDA	−200		200	mV
ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)						
IPI	Input Leakage Current	$-1.0V \le VPI \le 1.0V$	−100		100	nA
RIPI	Input Resistance	$-1.0V \le VPI \le 1.0V$	10			MΩ
VIOS	Input Offset Voltage		−25		25	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO^+ or VPO^-		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance	$R_L \ge 1500\Omega$ } VPO^+ or $R_L = 600\Omega$ } VPO^- to $R_L = 300\Omega$ } GNDA			100 500 1000	pF pF pF
$GA_P{}^+$	Gain, VPO^- to VPO^+	$R_L = 300\Omega$ VPO^+ to GNDA Level at $VPO^- = 1.77$ Vrms (+3 dBm0)		−1		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO^- Connected to VPI 0 kHz−4 kHz 0 kHz−50 kHz	 60 36			 dB dB

Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100			ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	$V_{IH} = 2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL} = 0.6V$	160			ns
t_{RB}	Rise Time of Bit Clock	$t_{PB} = 488$ ns			50	ns
t_{FB}	Fall Time of Bit Clock	$t_{PB} = 488$ ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	$C_L = 0$ pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{DFSSG}	Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	Load = 50 pF plus 2 LSTTL Loads			300	ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

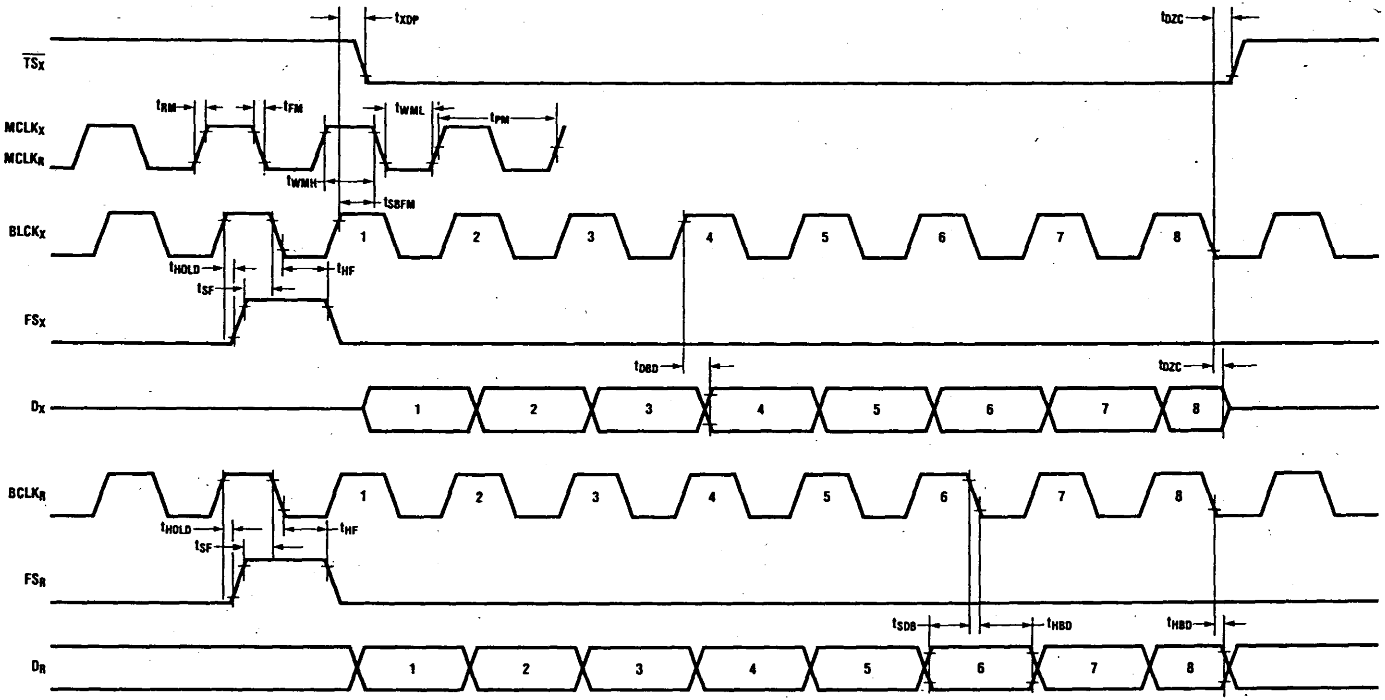


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FIGURE 2. Short Frame Sync Timing

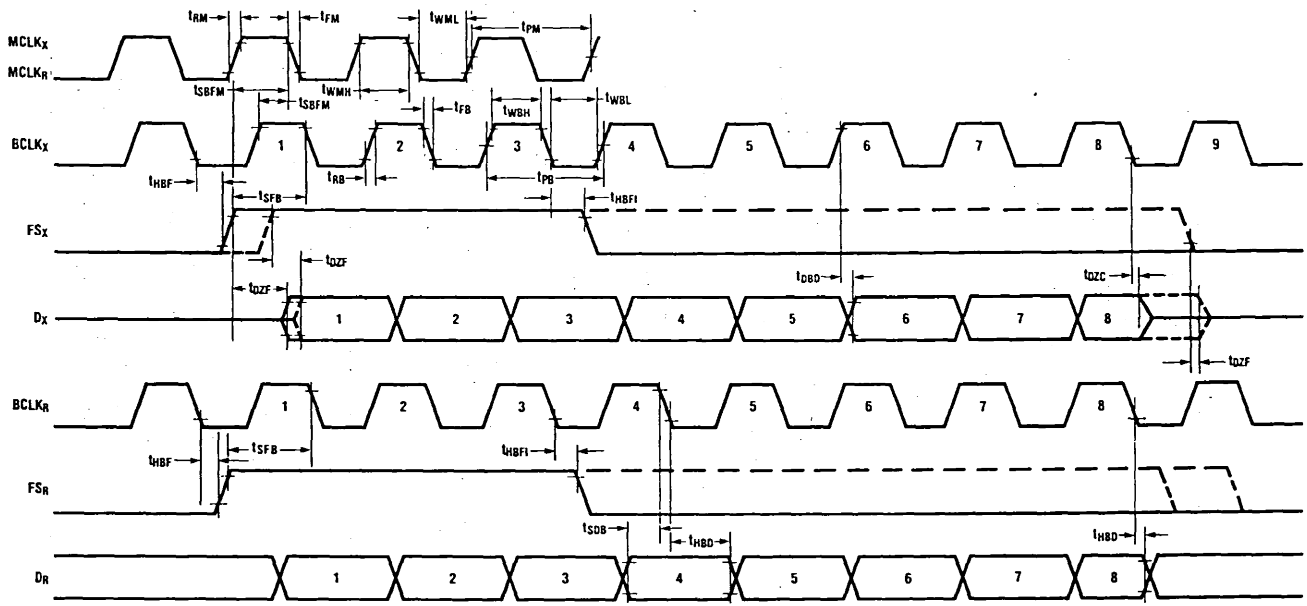

FIGURE 3. Long Frame Sync Timing

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Transmission Characteristics (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0 TP3064 TP3067		 1.2276 1.2276		 Vrms Vrms
t_{MAX}		Max Transmit Overload Level TP3064 (3.17 dBm0) TP3067 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input at $GS_X = 0$ dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz-3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 $VF_XI+ = -40$ dBm0 to +3 dBm0 $VF_XI+ = -50$ dBm0 to −40 dBm0 $VF_XI+ = -55$ dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±01.	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded - 10 dBm0 Signal PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Filter Output at VF_RO	RL = 10 kΩ	−2.5		2.5	V

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz f = 600 Hz − 800 Hz f = 800 Hz − 1000 Hz f = 1000 Hz − 1600 Hz f = 1600 Hz − 2600 Hz f = 2600 Hz − 2800 Hz f = 2800 Hz − 3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1000 Hz f = 1000 Hz − 1600 Hz f = 1600 Hz − 2600 Hz f = 2600 Hz − 2800 Hz f = 2800 Hz − 3000 Hz	−40 −30	−25 −20 70 100 145	 90 125 175	μs μs μs μs μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3064 $VF_XI^+ = 0V$		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3067 $VF_XI^+ = 0V$		−74	−69 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3064 PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3067 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 kHz − 50 kHz	 40			 dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 kHz − 50 kHz	 40			 dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 Hz − 4000 Hz f = 4 kHz − 25 kHz f = 25 kHz − 50 kHz	 40 40 36			 dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 Hz − 4000 Hz f = 4 kHz − 25 kHz f = 25 kHz − 50 kHz	 40 40 36			 dBC dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz − 3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO 4600 Hz-7600 Hz 7600 Hz-8400 Hz 8400 Hz-100,000 Hz			 −32 −40 −32	 dB dB dB

Transmission Characteristics (Continued)

(All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} - 5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X	Signal to Total Distortion	Sinusoidal Test Method				
STD_R	Transmit or Receive Half-Channel	Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to −30 dBm0	36			dBC
		= −40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= −55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz			−41	dB
CROSSTALK						
$CT_{X\text{-}R}$	Transmit to Receive Crosstalk	f = 300 Hz−3000 Hz D_R = Steady PCM Code		−90	−75	dB
$CT_{R\text{-}X}$	Receive to Transmit Crosstalk	f = 300 Hz−3000 Hz, VF_XI = 0V		−90	−70 (Note 2)	dB
POWER AMPLIFIERS						
V_{OL}	Maximum 0 dBm0 Level for Better than ±0.1 dB Linearity Over the Range −10 dBm0 to +3 dBm0	Balanced Load, R_L Connected Between VPO^+ and VPO^-				
		$R_L = 600\Omega$	3.3			Vrms
		$R_L = 1200\Omega$	3.5			Vrms
		$R_L = 30\ k\Omega$	4.0			Vrms
S/D_P	Signal/Distortion	$R_L = 600\Omega$, 0 dBm0	50			dB

Note 1: Measured by extrapolation from the distortion test result.

Note 2: $CT_{R\text{-}X}$ is measured with a −40 dBm0 activating signal applied at VF_XI^+.

Applications Information

POWER SUPPLIES

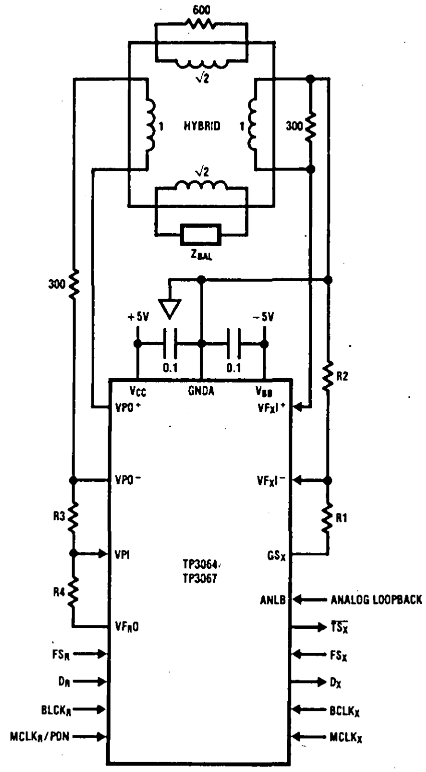
While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in start formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Note: See Applications Brief 13 for further details.

Typical Asynchronous Application



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Note 1: Transmit gain $= 20 \times \log \left(\frac{R1+R2}{R2}\right)$, $(R1+R2) \geq 10\ k\Omega$

Note 2: Receive gain $= 20 \times \log \left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 2

National Semiconductor

PRELIMINARY

TP3155 Time Slot Assignment Circuit

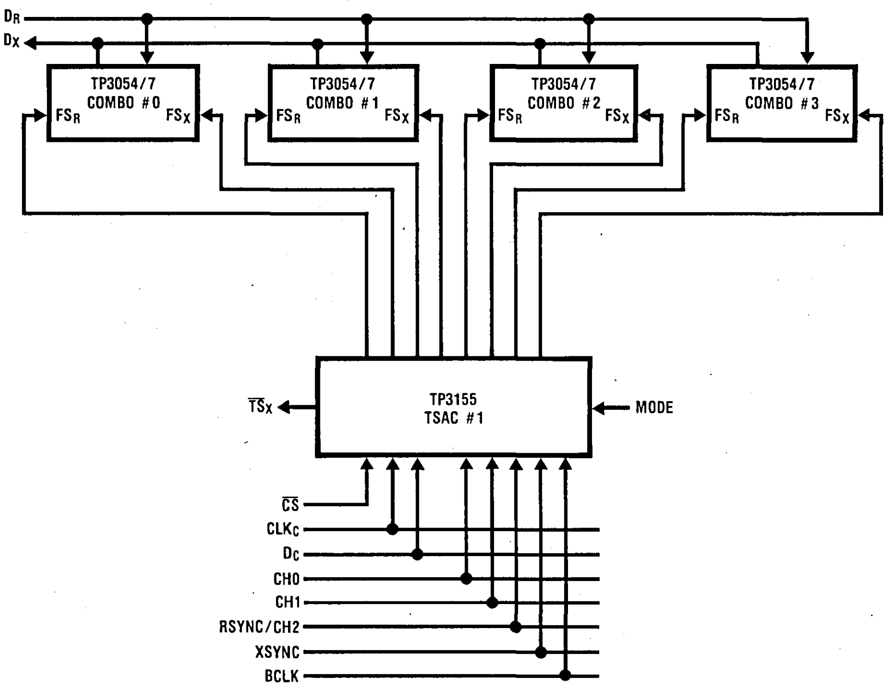
General Description

The TP3155 is a monolithic CMOS logic circuit designed to generate transmit and receive frame synchronization pulses for 4 PCM CODEC/Filters. Each frame sync pulse may be independently assigned to a time slot in a frame of up to 64 time slots. Assignments are controlled by loading in an 8-bit word via a simple serial interface port. This control interface is compatible with that used on the TP3020/TP3021 and 2910/2911 CODECs, enabling an easy upgrade to combo CODEC/Filters to be made.

Features

- Controls 4 CODEC/Filters
- Independent transmit and receive time slot assignments
- 8-channel unidirectional mode
- Up to 64 time slots per frame
- 4.096 MHz maximum clock rate
- Serial control interface compatible with TP3020/TP3021 CODECs
- TTL and CMOS compatible inputs
- 5 mW, 5V operation

Typical Application



TL/H/5118-1

Absolute Maximum Ratings

V_{CC} Relative to GND	7V
Voltage at Any Input or Output	V_{CC} + 0.3V to GND − 0.3V
Operating Temperature Range (Ambient)	−40°C to +70°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

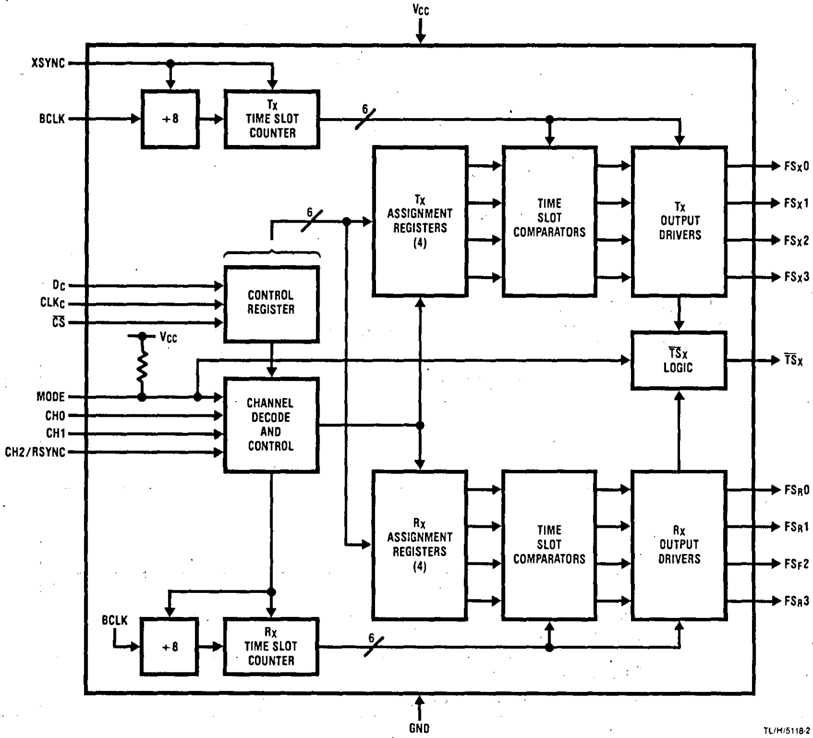
Unless otherwise noted, V_{CC} = 4.75V to 5.25V and ambient temperature is 0°C to 70°C.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		2.2			V
V_{IL}, Logic Low				0.6	V
Input Currents					
All Inputs Except MODE	$V_{IL} < V_{IN} < V_{IH}$	−1		1	μA
MODE	$V_{IL} < V_{IN} < V_{IH}$	−100		100	μA
Output Voltage Levels					
V_{OH}, Logic High	FS_X and FS_R Outputs, I_{OH} = 3 mA	2.4			V
V_{OL}, Logic Low	FS_X, FS_R and $\overline{TS}_X$ Outputs, I_{OL} = 3 mA			0.4	V
Power Dissipation Operating Current	BCLK = 4.096 MHz, All Outputs Open-Circuit		1	1.5	mA

Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock	BCLK, CLK_C	240		ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	BCLK, CLK_C		50	ns
t_{WCH}	Width of Clock High	BCLK, CLK_C	50		ns
t_{WCL}	Width of Clock Low	BCLK, CLK_C	50		ns
t_{SDC}	Set-Up Time from D_C to CLK_C		30		ns
t_{HCD}	Hold Time from CLK_C to D_C		50		ns
t_{SCC}	Set-Up Time from $\overline{CS}$ to CLK_C		0		ns
t_{HCCL}	Hold Time from CLK_C to $\overline{CS}$ Low		0		ns
t_{HCCH}	Hold Time from CLK_C to $\overline{CS}$ High		50		ns
t_{SCHC}	Set-Up Time from Channel Select to CLK_C		30		ns
t_{HCHC}	Hold Time from Channel Select to CLK_C		50		ns
t_{RS}, t_{FS}	Rise and Fall Time of XSYNC, RSYNC			50	ns
t_{DBF}	Delay Time from BCLK Low to $FS_{X/R}$ 0-3 High or Low	C_L = 50 pF		50	ns
t_{HSYNC}	Hold Time from BCLK to Frame Sync		50	8 Cycles of BCLK	ns
t_{SSYNC}	Set-Up Time from Frame Sync to BCLK		30		ns
t_{DTL}	Delay to $\overline{TS}_X$ Low	C_L = 100 pF		140	ns
t_{DTH}	Delay to $\overline{TS}_X$ Off		30	100	ns

Block Diagram



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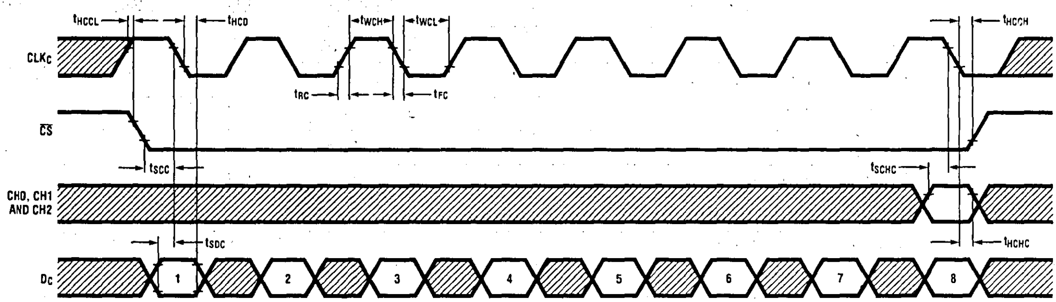
Timing Diagrams

Control Interface



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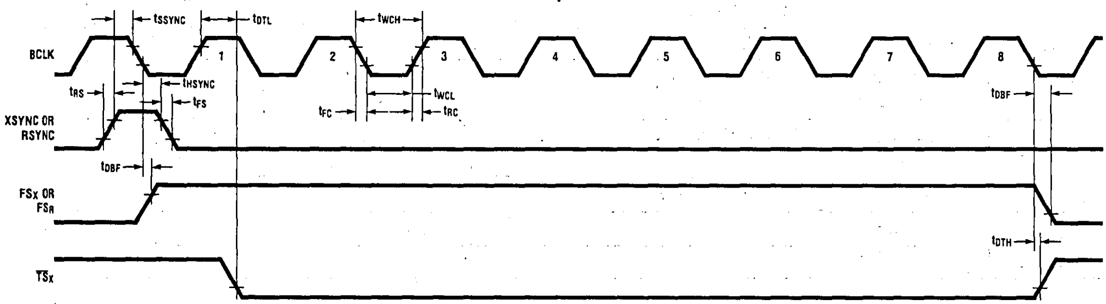
Output



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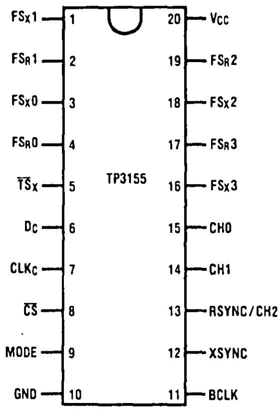
Connection Diagram

Dual-In-Line Package



TOP VIEW TL/H/5118-5

Pin Descriptions

Pin Number	Name	Description
1	FS_X1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
2	FS_R1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
3	FS_X0	A transmit frame sync output similar to pin 1.
4	FS_R0	A receive frame sync output similar to pin 2.
5	$\overline{TS}_X$	An open-drain N-channel output which is normally high impedance but pulls low during any active transmit time slot.
6	D_C	The input for an 8-bit serial control word. $\overline{X}$ is the first bit clocked in.
7	CLK_C	The clock input for the control interface.
8	$\overline{CS}$	The active-low chip select for the control interface.
9	MODE	The mode select input. When left open-circuit or connected to V_{CC}, mode 1 is selected, and when connected to GND, mode 2 is selected.
10	GND	The 0V ground connection to the device.
11	BCLK	The bit clock input, which should run at the same rate as that for the CODEC/Filter combos.
12	XSYNC	The transmit TS0 sync pulse input. Must be synchronous with BCLK.
13	RSYNC/CH2	The function of this input is determined by the MODE input (pin 9). In mode 1 this is the receive TS0 sync pulse, RSYNC, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
14	CH1	The input for the next significant bit of the channel select word.
15	CH0	The input for the LSB of the channel select word, which defines the frame sync output affected by the following control word.
16	FS_X3	A transmit frame sync output similar to pin 1.
17	FS_R3	A receive frame sync output similar to pin 2.
18	FS_X2	A transmit frame sync output similar to pin 1.
19	FS_R2	A receive frame sync output similar to pin 2.
20	V_{CC}	The positive supply to the device. 5V ± 10% (± 5% for 4 MHz operation).

Functional Description

OPERATING MODES

The TP3155 control interface requires an 8-bit serial control word which is compatible with that for the TP3020/TP3021 and 2910/2911 CODECs. Two bits, $\overline{X}$ and $\overline{R}$, define which of the two groups of frame sync outputs, FS_X0 to FS_X3 or FS_R0 to FS_R3, is affected by the control word, and a 6-bit assignment field specifies the selected time slot, from 0 to 63. A frame sync output is active-high for one time slot, which is always 8 cycles of BCLK. A frame may consist of any number of time slots up to 64.

Two modes of operation are available. Mode 1 is for systems requiring different time slot assignments for the transmit and receive direction of each channel. In this case, pin 15 is the RSYNC input which defines the start of each receive frame, and the four outputs, FS_R0–FS_R3, are assigned with respect to RSYNC. The XSYNC input defines the start of each transmit frame and outputs FS_X0–FS_X3 are assigned with respect to XSYNC. XSYNC may have any phase relationship with RSYNC. Inputs CH0 and CH1 select the channel, from 0 to 3 (see Table Ia). Mode 1 is selected by leaving pin 9 (MODE) open-circuit or connecting it to V_{CC}.

Mode 2 provides the option of assigning all 8 frame sync outputs with respect to the XSYNC input. This makes the TP3155 TSAC useful for either an 8-channel unidirectional controller or for systems in which the transmit and receive directions of each channel are always assigned to the same time slot as the other, i.e., the FS_X and FS_R inputs on the combo CODEC/Filter are hard-wired together. In this case, logical selection of the channel to be assigned is made via inputs CH0, CH1 and CH2 (see Table Ib). Mode 2 is selected by connecting pin 9 (MODE) to GND.

POWER-UP INITIALIZATION

During power-up, all frame sync outputs, FS_X0–FS_X3 and FS_R0–FS_R3, are inhibited and held low. No outputs will go active until a valid time slot assignment is made.

LOADING CONTROL DATA

During the loading of control data, the binary code for the selected channel must be set on inputs CH0 and CH1 (and CH2 in mode 2), see Tables 1a and 1b.

Control data is clocked into the D_C input on the falling edges of CLK_C while $\overline{CS}$ is low.

Alternatively, $\overline{CS}$ may be connected to GND and an externally gated burst of 8 positive CLK_C pulses used to shift in control data on D_C. CLK_C must stay low at all other times.

In either case the shifting of control data may overlap an XSYNC or RSYNC pulse, but must be completed in less than one frame period. A new time slot assignment is only transferred to the selected assignment register and frame sync output at the start of the second frame (either transmit or receive, as appropriate) after $\overline{CS}$ goes low.

TIME SLOT COUNTER OPERATION

At the start of TS0 of each transmit frame, defined by the first falling edge of BCLK after XSYNC goes high, the transmit time slot counter is reset to 000000 and begins to increment once every 8 cycles of BCLK. Each count is compared with the 4 transmit assignment registers and, on finding a match, a frame sync pulse is generated at that FS_X output.

Similarly, the first falling edge of BCLK after RSYNC goes high defines the start of receive TS0, and outputs FS_R0–FS_R3 are generated with respect to TS0 when the receive time slot counter matches the appropriate receive assignment register.

$\overline{TS}_X$ OUTPUT

In mode 1 (separate transmit and receive assignments), this output pulls low whenever any FS_X output pulse is being generated. In mode 2, this output pulls low whenever any FS_X or FS_R output is being generated. At all other times it is open-circuit, allowing the $\overline{TS}_X$ outputs of a number of TSACs to be wire-ANDed together with a common pull-up resistor. This signal can be used to control the TRI-STATE® enable input of a line driver to buffer the transmit PCM bus from the CODEC/Filters to the backplane.

TABLE 1a. CONTROL MODE 1 (TP3020/TP3021 COMPATIBLE)

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into the D_C input.

Control Data Format

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

CH1	CH0	Channel Selected
0	0	Assign to FS_X0 and/or FS_R0
0	1	Assign to FS_X1 and/or FS_R1
1	0	Assign to FS_X2 and/or FS_R2
1	1	Assign to FS_X3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE 1b. CONTROL MODE 2

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	Assign time slot to selected output
1	0	Assign time slot to selected output
1	1	Disable selected output

Applications Information

A combination of the TP3155 TSAC and any CODEC/Filter combo from the TP3052/3/4/7 or TP3064/7 series will result in data timing as shown in *Figure 1*. Although the FS_X output pulse goes high before BCLK goes high, the D_X output of the combo remains in the TRI-STATE mode until both are high. The eighth bit period is shortened to prevent a bus clash, just as it is on the TP3020/1 CODECs.

Alternatively, eight full-length bits can be obtained by inverting the BCLK to the combo devices, thereby aligning rising edges of BCLK and $FS_{X/R}$.

Figure 2 shows the digital interconnections of a typical line card application.

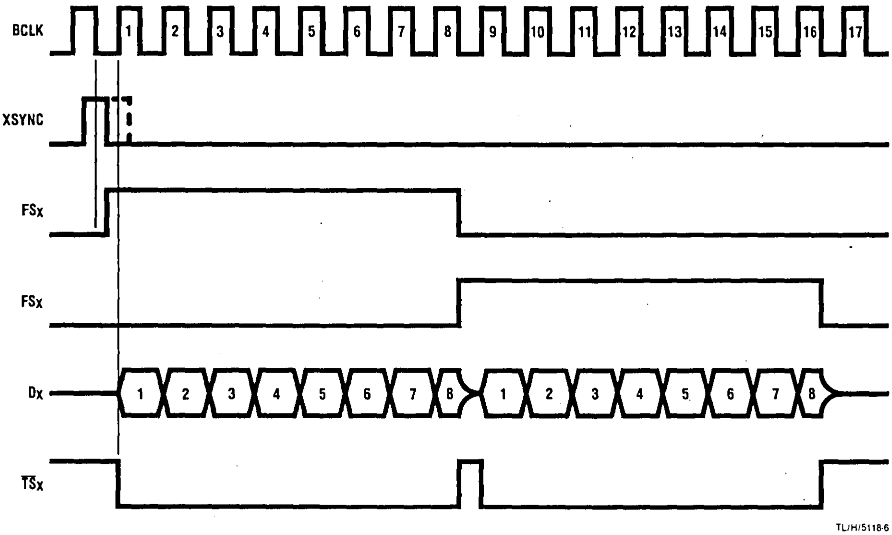


FIGURE 1. Transmit Data Timing

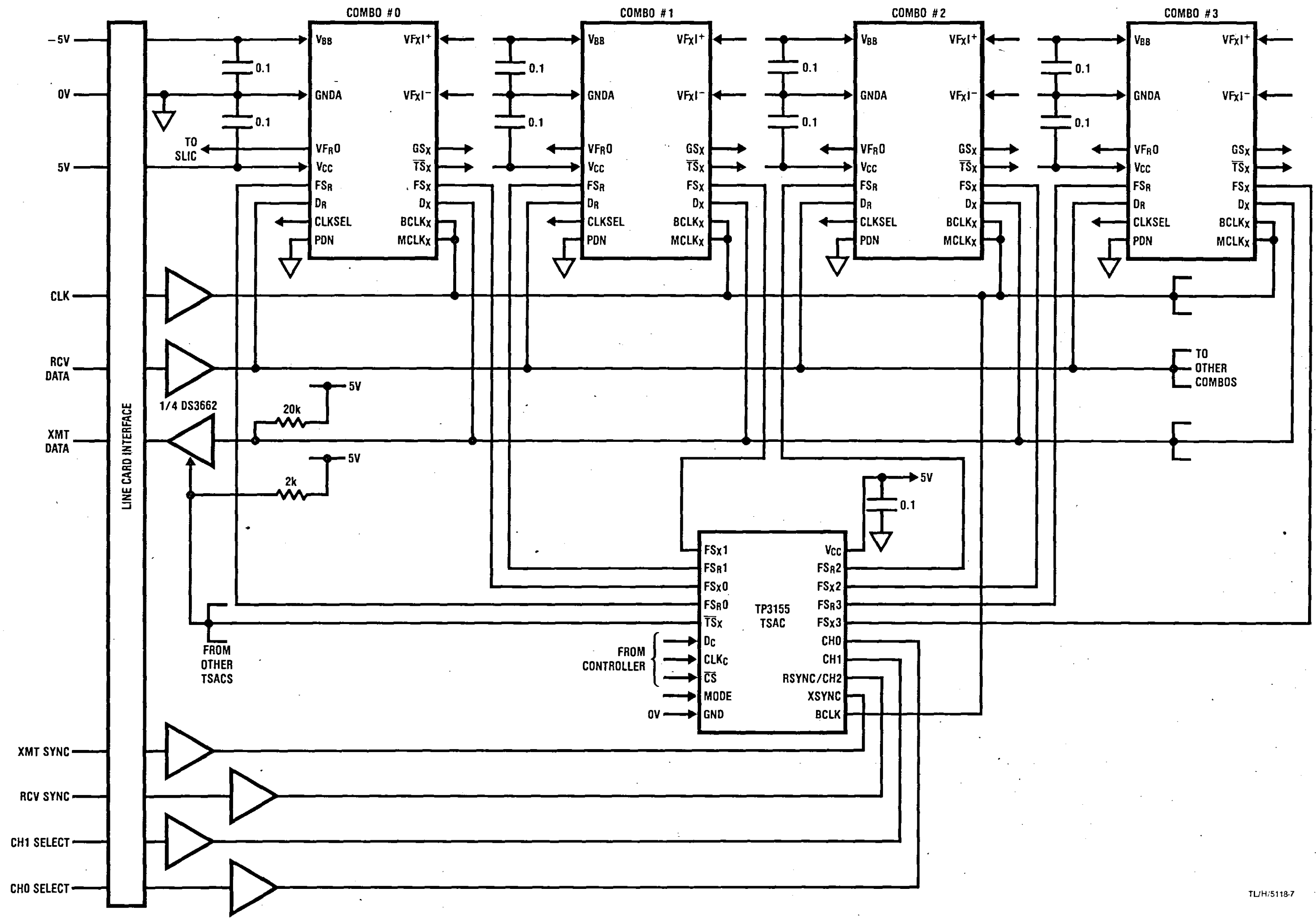


FIGURE 2. Digital Interconnections on a Typical Synchronous Line Card

TP3310, TP3311, TP3320, TP3321 Monolithic Reversible 1200-600/150-75-5 Bit/s CMOS FSK MODEM Family

General Description

The TP3320 and TP3321 are general purpose monolithic FSK (frequency shift-keyed) MODEMs implemented with National's advanced double-poly CMOS process (P^2CMOS^{TM}). They are capable of generating and receiving frequency modulated signals at data rates up to 1200 bit/s on voice-grade telephone lines. The TP3320 and TP3321 are offered in a 20-pin package capable of operating half-duplex with a backward channel on two-wire lines or full-duplex on four-wire lines according to three pin selectable standards:

—CCITT V23 at 1200 bit/s, with backward channel at 75 or 150 bit/s.
—CCITT V23 at 600 bit/s, with backward channel at 75 or 150 bit/s.
—BELL 202 at 1200 bit/s, with backward channel at 5 or 150 bit/s.

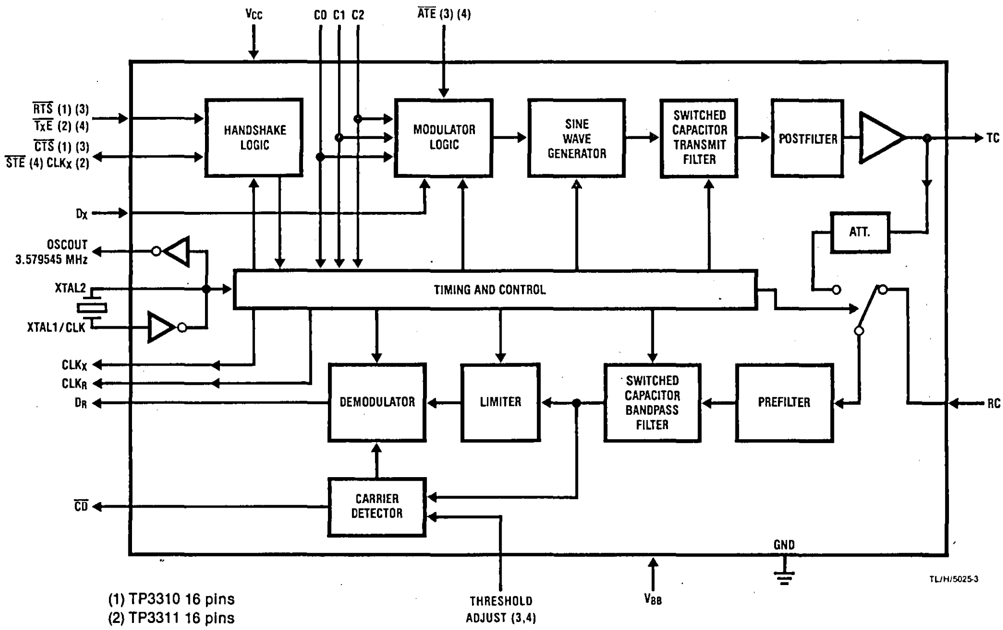
All filtering functions required for frequency generation, out-of-band noise rejection and demodulation are performed by on-chip switched capacitor filters. Internal frequencies are generated from an inexpensive 3.579545 MHz TV color-burst crystal reference.

The TP3310 and TP3311 are 16-pin versions of the TP3320 optimized for low cost applications.

Features

- BELL 202(s) compatible
  0–1200 bit/s with 0–5 or 150 bit/s backward channel
  900 Hz soft carrier turn-off tone
  2025 Hz answer tone
- CCITT V23 compatible
  0–1200 bit/s with 0–75 or 150 bit/s backward channel
  0–600 bit/s with 0–75 or 150 bit/s backward channel
  2100 Hz answer tone
- Half-duplex operation on two-wire lines
- Full-duplex 1200 or 600 bit/s operation on four-wire lines
- Low operating power: 90 mW (typical)
- Low standby power: 2 mW (typical)
- ±5V operation
- On-chip switched capacitor transmit and receive filters
- Uses 3.579545 MHz TV color-burst crystal
- Optimized UART interface
- Loopback test mode
- RS232C-type handshake signals
- TTL and CMOS compatible

Block Diagram



(1) TP3310 16 pins
(2) TP3311 16 pins
(3) TP3320 20 pins
(4) TP3321 20 pins

FIGURE 1

Absolute Maximum Ratings

Operating Temperature Range	−25°C to 80°C
Storage Temperature Range	−65°C to +150°C
V_{CC} with Respect to GND	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GND	−7V
Voltage at Digital Inputs ($\overline{RTS}$, $\overline{T_XE}$, $\overline{ATE}$, D_X)	V_{CC} + 0.3V to GND − 0.3V
Voltage at Any Other Input	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Output	V_{CC} + 0.3V to GND − 0.3V
Voltage at Any Analog Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Output Short-Circuit Duration	Continuous
Power Dissipation	1W/package
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise noted: V_{CC} = 5.0V ± 5%, V_{BB} = −5.0V ± 5%, GND = 0V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C; all digital and analog signals are referenced to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	$\overline{CTS}$, $\overline{CD}$, CLK_X, CLK_R, DR I_L = 1.0 mA OSCOUT I_L = 1.0 mA			0.4 0.4	V V
V_{OH}	Output High Voltage	$\overline{CTS}$, $\overline{CD}$, CLK_X, CLK_R, DR OSCOUT	2.4 2.4			V V
I_{IL}	Input Low Current	GND ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	−10		10	μA
POWER DISSIPATION						
$I_{CC}0$	Power-Down Current			0.2		mA
$I_{BB}0$	Power-Down Current			0.2		mA
$I_{CC}1$	Active Current	R_{LXA} ≥ 10 kΩ		10		mA
$I_{BB}1$	Active Current	R_{LXA} ≥ 10 kΩ		5		mA
ANALOG INTERFACE—TRANSMIT CARRIER OUTPUT (TC)						
R_{OXA}	Output Dynamic Resistance			1		Ω
R_{LXA}	Load Resistance	V_{OXA} = ±2.19V	600			Ω
C_{LXA}	Load Capacitance				500	pF
V_{OXA}	Transmit Level	R_L = 600Ω	 5.5	±2.19	 6.5	Vp dBm/600Ω
V_{OSX}	Output Offset Voltage		−100		+100	mV
ANALOG INTERFACE—RECEIVE CARRIER INPUT (RC)						
I_{IRA}	Input Leakage Current	V_{BB} ≤ V_{IRA} ≤ V_{CC}	−1.0		−1.0	μA
R_{IRA}	Input Resistance		100			kΩ
V_{IRA}	Receive Signal Level Range				−6 548	dBm/600Ω mVp

Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Crystal Frequency	Note 1		3.579545		MHz
$1/t_{OSC}$	OSCOUT Frequency			3.579545		MHz
t_{RM}	Rise Time OSCOUT Output	$C_L = 50$ pF, 1 LSTTL Load			55	ns
t_{FM}	Fall Time OSCOUT Output	$C_L = 50$ pF, 1 LSTTL Load			40	ns
t_R	Rise Time CLK_X, CLK_R	$C_L = 50$ pF, 1 LSTTL Load			120	ns
t_F	Fall Time CLK_X, CLK_R	$C_L = 50$ pF, 1 LSTTL Load			80	ns
t_{RDX}	Rise Time Receive Data Output (D_R)	$C_L = 50$ pF, 1 LSTTL Load			120	ns
t_{FDX}	Fall Time Receive Data Output (D_R)	$C_L = 50$ pF, 1 LSTTL Load			80	ns
t_{PWNS}	Set-Up Time from C1 Valid to C2 Low	Power-Down/Power-Up Transition (*Figure 4*)	300			ns
t_{PWNH}	Hold Time from C2 Low to C1 Invalid	Power-Down/Power-Up Transition	300			ns
t_{TCE}	Delay Time from $\overline{RTS}$, $\overline{TXE}$, or $\overline{ATE}$ Low to Transmit Carrier Enabled	(*Figure 5*)		0.1		ms
t_{TCD}	Delay Time from $\overline{RTS}$, $\overline{TXE}$, or $\overline{ATE}$ High to Transmit Carrier Disabled			0.1		ms
FORWARD CHANNEL						
t_{CTSLF}	Delay Time from $\overline{RTS}$ Low to $\overline{CTS}$ Low	(*Figure 5*) BR = 1200 or 600 Bit/s		33.3		ms
t_{CTSHF}	Delay Time from $\overline{RTS}$ High to $\overline{CTS}$ High			0.1		ms
t_{CDONF}	Carrier Detector Acquisition Time	1300 Hz Tone		15		ms
t_{CDOFFF}	Carrier Detector Release Time			12		ms
BACKWARD CHANNEL						
t_{CTSLB}	Delay Time from $\overline{RTS}$ Low to $\overline{CTS}$ Low	(*Figure 5*) BR = 5 or 75 Bit/s BR = 150 Bit/s		133 66.7		ms ms
t_{CTSHB}	Delay Time from $\overline{RTS}$ High to $\overline{CTS}$ High			0.1		ms
t_{CDONB}	Carrier Detector Acquisition Time	390 Hz Tone		50		ms
t_{CDOFFB}	Carrier Detector Release Time			48		ms

Note 1: Crystal parameters $R_S \leq 150\Omega$, $L = 100$ mH, $C_M = 0.02$ pF, $C_h = 5$ pF.

TABLE I. CARRIER FREQUENCY ACCURACY

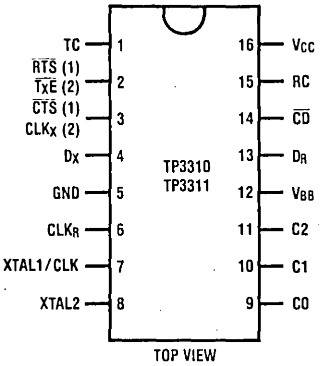
		Standard FSK Frequency (Hz)		Output Frequency Using 3.579545 MHz Crystal (Hz)	% Deviation from Standard
CCITT V23	1200 bit/s	FH1	1300	1300.71	0.05
		FH0	2100	2100.67	0.03
	600 bit/s	FH1	1300	1300.71	0.05
		FH0	1700	1701.30	0.08
	75 bit/s	FL1	390	389.76	−0.06
		FL0	450	450.14	0.03
BELL 202	1200 bit/s	FH1	1200	1199.58	−0.04
		FH0	2200	2204.15	0.19
	150 bit/s	FL1	390	389.76	−0.06
		FL0	490	490.08	0.02
	5 bit/s	FL1	387	389.76	0.71
		FL0	—	—	—
	Answer Tone		2025	2024.63	−0.02
	Soft Carrier Turn-Off Tone		900	900.29	0.03

Transmission Performance

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
D_{tX}	Maximum Delay from Transmit Data Input (D_X) to Transmit Carrier Frequency Change					4	μs
E_{OX}	Out-of-Band Energy Referred to Carrier Level	F ≥ 3.4 kHz (see *Figure 3*)				−40	dB
		F ≥ 8 kHz				−60	dB
RECEIVER							
S_R	Input Signal Level					−6	dBm/600Ω
Th_{CD}	Carrier Detect Threshold	−THRESHOLD ADJUST = V_{CC} (+5V)	ON			−43	dBm
			OFF	−48			dBm
		−THRESHOLD ADJUST = GND (0V)	ON			−38	dBm
		(TP3320/TP3321)	OFF	−43			dBm
		−THRESHOLD ADJUST = V_{BB} (−5V)	ON			−33	dBm
		(TP3320/TP3321)	OFF	−38			dBm
H_{CD}	Carrier Detect Hysteresis	Measured from Th_{CD} ON to Th_{CD} OFF		2		5	dB
FORWARD CHANNEL							
ID_F	Peak Intersymbol Distortion (Isochronous ± Bias)	Back-to-Back Over Input Signal Range −6 dBm to −43 dBm 511-Bit Test Pattern	BR = 1200 Bit/s		10		%
			BR = 600 Bit/s		6		%
BER_F	Bit Error Rate	Back-to-Back over a Flat Line with Additive 300 Hz – 3400 Hz Flat Noise— Receive Signal Level: −6 dBm to −43 dBm 511-Bit Test Pattern	S/N = 7 dB		10^{-3}		
			S/N = 10 dB		10^{-5}		
BACKWARD CHANNEL							
ID_B	Peak Intersymbol Distortion (Isochronous ± Bias)	Back-to-Back Over Input Signal Range −6 dBm to −43 dBm 511-Bit Test Pattern	BR = 150 Bit/s		6		%
			BR = 75 Bit/s		6		%
BER_B	Bit Error Rate	Back-to-Back over a Flat Line with Additive 300 Hz – 3400 Hz Flat Noise— Receive Signal Level: −6 dBm to −43 dBm 511-Bit Test Pattern	S/N = −2 dB		10^{-3}		
			S/N = 1 dB		10^{-5}		

Connection Diagrams

Dual-In-Line Package



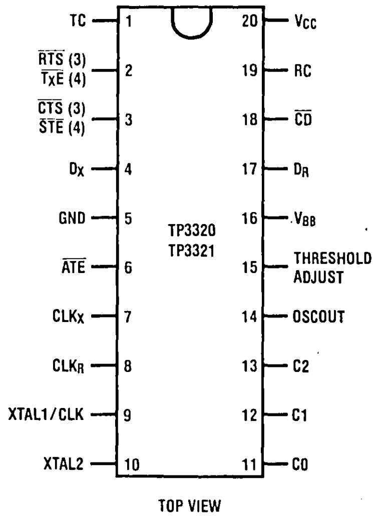
TL/H/5025-1

(1) TP3310
(2) TP3311

Order Number TP3310J or TP3311J
NS Package Number J16A

Order Number TP3310N or TP3311N
NS Package Number N16A

Dual-In-Line Package



TL/H/5025-2

(3) TP3320
(4) TP3321

Order Number TP3320J or TP3321J
NS Package Number J20A

Functional Description

POWER-UP AND INITIALIZATION

When power is first applied, power-on reset circuitry initializes the MODEM and places it into the power-up mode. In applications where transmission toward the telephone line is not continuous, and where power consumption needs to be low, the MODEM can be powered down using control inputs C1 and C2. (See *Figure 4*.)

In the power-down mode, all nonessential circuits are deactivated, and analog output TC is grounded. Outputs D_R, $\overline{CTS}$ and $\overline{CD}$ are put in a high impedance state. External clocks OSCOUT, CLK_X and CLK_R remain in a low impedance high or low state.

TRANSMITTER

The transmitter consists of a digitally controlled frequency modulator followed by a transmit switched capacitor filter and a postfilter (*Figure 1*). It converts the digital information received from a UART or from a DTE into a frequency modulated sine-wave (*Figure 2*). The output power amplifier can directly drive a transformer or DAA coupler to the telephone line.

In order to avoid generating unwanted frequency components and to minimize bit length distortion, the modulator maintains phase continuity when switching between the two carrier frequencies.

The transmit filter and the postfilter attenuate any unwanted frequency created by the modulation process, so that the level of spurious out-of-band signals transmitted to the telephone line is maintained below the limits of FCC and CCITT specifications (see *Figure 3*).

The frequency assignments for the three standards are also shown in *Figure 3* and in Table II. The telephone channel bandwidth is divided into a forward channel on which transmission occurs at 1200 bit/s or 600 bit/s, and a backward channel on which transmission is at a lower rate: 75 bit/s for the CCITT V23 standard and 5 or 150 bit/s for the BELL 202 standard.

On a two-wire line, the only operating mode is half-duplex with split baud rates: when the MODEM transmits at 1200 bit/s or 600 bit/s on the forward channel, it receives at 150 bit/s, 75 bit/s or 5 bit/s on the backward channel; when it transmits at 150 bit/s, 75 bit/s or 5 bit/s on the backward channel, it receives at 1200 bit/s or 600 bit/s on the forward channel.

On a four-wire line, the MODEM can also operate in full-duplex mode at 600 bit/s or 1200 bit/s in both directions.

Table II shows how to program control inputs C0, C1 and C2 to select the standard and the operating mode.

Functional Description (Continued)

$\overline{\text{RTS}}$/$\overline{\text{CTS}}$ DELAY

TP3310/TP3320: When the request to send input ($\overline{\text{RTS}}$-pin 2) is asserted low by the DTE (data terminal equipment), the MODEM enables the transmit carrier output and prepares itself to transmit data. After a fixed delay has been timed out (t_{CTSLF} or t_{CTSLB} according to the channel processed by the transmitter), it pulls down pin 3 ($\overline{\text{CTS}}$) in order to indicate to the DTE that it is ready to transmit data—data input D_X remains internally clamped to mark (logical 1) as long as $\overline{\text{CTS}}$ (clear to send) is high.

TP3311/TP3321: These devices do not provide an internal delay before the carrier can be modulated. When input $\overline{\text{TXE}}$ is pulled low by the DTE the MODEM enables the TC output directly. The carrier frequency is immediately determined by the data at input D_X. Any delay required to allow the remote MODEM to acquire the carrier must be provided externally.

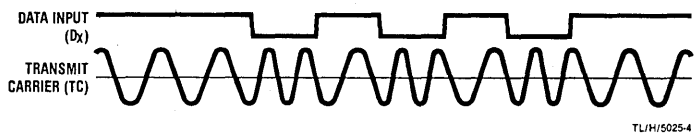
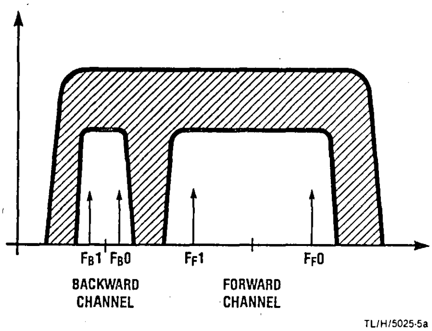


FIGURE 2. Transmitted Signal



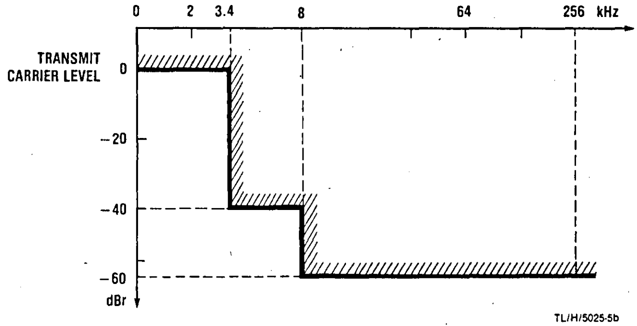


FIGURE 3. Frequency Assignments

Maximum Level of Out-of-Band Energy, Relative to the Unmodulated Transmit Carrier Level

TABLE II. OPERATING MODE AND STANDARD SELECTION

Operating Mode	C2	C1	C0	Standard	Modulation Speed (Bauds) XMT	Modulation Speed (Bauds) RCV	XMT Freq (Hz) 1	XMT Freq (Hz) 0	RCV Freq (Hz) 1	RCV Freq (Hz) 0	CLK_X Freq (×16 Hz)	CLK_R Freq (×16 Hz)
NORMAL	GND	GND	GND	CCITT V23 1200 bit/s	1200	75/150*	1300	2100	390	450/490*	1200	75/150*
		V_{CC}	GND		75/150*	1200	390	450/490*	1300	2100	75/150*	1200
		V_{BB}	GND		1200	1200	1300	2100	1300	2100	1200	1200
		GND	V_{CC}	CCITT V23 600 bit/s	600	75/150*	1300	1700	390	450/490*	600	75/150*
		V_{CC}	V_{CC}		75/150*	600	390	450/490*	1300	1700	75/150*	600
		V_{BB}	V_{CC}		600	600	1300	1700	1300	1700	600	600
		GND	V_{BB}	BELL 202 Mode 1	1200	5	1200	2200	387	0	1200	75
		V_{CC}	V_{BB}		5	1200	387	0	1200	2200	75	1200
		V_{BB}	V_{BB}		1200	1200	1200	2200	1200	2200	1200	1200
	V_{CC}	V_{BB}	GND	BELL 202 Mode 2	150	1200	390	490	1200	2200	150	1200
		V_{BB}	V_{CC}		1200	150	1200	2200	390	490	1200	150
SELF-TEST	V_{CC}	GND	GND	CCITT V23 1200 bit/s	1200	1200	1300	2100	1300	2100	1200	1200
		V_{CC}	GND		75/150*	75/150*	390	450/490*	390	450/490*	75/150*	75/150*
		GND	V_{CC}	CCITT V23 600 bit/s	600	600	1300	1700	1300	1700	600	600
		V_{CC}	V_{CC}		75/150*	75/150*	390	450/490*	390	450/490*	75/150*	75/150*
		GND	V_{BB}	BELL 202	1200	1200	1200	2200	1200	2200	1200	1200
		V_{CC}	V_{BB}		5	5	387	0	387	0	75	75
		V_{BB}	V_{BB}		1200	1200	1200	2200	1200	2200	1200	1200

*TP3320 or TP3321 only. 75 Bauds and 450 Hz are selected when $\overline{\text{ATE}}$ is low (GND). 150 Bauds and 490 Hz are selected when $\overline{\text{ATE}}$ is high (V_{CC}).

Functional Description (Continued)

RECEIVE FILTERS

The signal delivered by the hybrid to the receive carrier input is a mixture of transmitted signal, received signal and noise, with a level in the range from −48 dBm/600Ω to −6 dBm/600Ω.

An antialias filter is inserted at the input of the receive section to remove any high frequency noise component before sampling occurs.

Depending on the operating mode, the receive switched capacitor band-pass filter selects the frequency band of the main channel or of the backward channel. It rejects out-of-band transmission noise components and undesirable adjacent channel echo signals which can be fed from the transmit section into the receive section when the MODEM operates on a two-wire line. Equalization is included in order to assure low bit error rate and low bit length distortion when connected to a telephone line.

At the input to the demodulator, a limiter and an associated auto-zero circuit remove any amplitude modulation and any offset which could bias the demodulator toward a 1 or a 0 output. The demodulator converts the FSK modulated signal back into digital data at the D_R output.

CARRIER DETECTOR

The carrier detector monitors the level of the receive signal. To prevent transmission of erroneous data toward the data terminal, receive data output D_R is clamped to 1 when the carrier falls below the receive threshold level. Whenever valid signals are being received at the input of the demodulator and are acceptable for demodulation, output pin $\overline{CD}$ is pulled down and the D_R output is enabled. A delay is timed out before the carrier received or carrier lost signal changes $\overline{CD}$ to provide immunity against noise bursts. The MODEM also provides at least 2 dB of hysteresis between the carrier ON and the carrier OFF thresholds. These thresholds are normally ON by −43 dBm and OFF by −48 dBm for switched telephone network operation; but two additional sensitivities (−33 dBm/−38 dBm or −38 dBm/−43 dBm) can also be selected when the TP3320 or the TP3321 is used through digital control input THRESHOLD ADJUST.

SOFT CARRIER TURN-OFF (BELL 202 STANDARD)

When $\overline{RTS}$ is turned off at the end of a message, transients may occur and cause erroneous data to be received at a remote MODEM. To prevent this spurious effect, the transmitting MODEM can generate a 900 Hz soft carrier turn-off tone at the end of the message, under external control (TP3320 and TP3321 only).

On the TP3320, the soft carrier turn-off tone is controlled by $\overline{ATE}$ (pin 6—active low) and $\overline{RTS}$ (pin 2). On the TP3321, it is controlled by $\overline{STE}$ (pin 3—active low).

BAUD RATE CLOCKS

The TP3320, the TP3321 and the TP3311 provide two baud rate clocks, CLK_X and CLK_R, which can be used to synchronize the transmit and the receive sections of a UART. The frequency of each of these clocks (75 × 16 Hz, 150 × 16 Hz, 600 × 16 Hz or 1200 × 16 Hz) is internally adjusted so that it corresponds to the baud rate for the associated direction. When 5 baud is selected, the frequency becomes 75 × 16 Hz.

Only one of the baud rate clocks (CLK_R) is available on the TP3310.

OSCILLATOR OUTPUT (TP3320 or TP3321)

The buffered master clock (3.579545 MHz) is made available at output OSCOUT. It can be used as a clock for a DTMF tone generator or for a microprocessor. The oscillator runs continuously while the MODEM is powered up.

SELF-TEST

The self-test mode allows the user or the DTE to verify that the MODEM operates properly. It can be selected by control inputs C0, C1 and C2, as shown in Table II. In the self-test mode, the transmit carrier output is looped back to the receive carrier input through an internal attenuator while still providing the modulated carrier to output pin TC. The receive filters and the demodulator are configured to process the same channel as the transmit section. Transmitted signals are still controlled by C0, C1 and by data input D_X. Baud rate clocks CLK_X and CLK_R provide the same baud rate to the transmit and the receive sections of an external UART (75 × 16 Hz, 150 × 16 Hz, 600 × 16 Hz or 1200 × 16 Hz).

POWER-DOWN/POWER-UP

To power-down the MODEM, C1 must be set to a low (GND) level and a falling edge applied at C2. To power-up the MODEM, C1 must be set to a high (V_{CC}) level and a falling edge applied at C2 (see *Figure 4*).

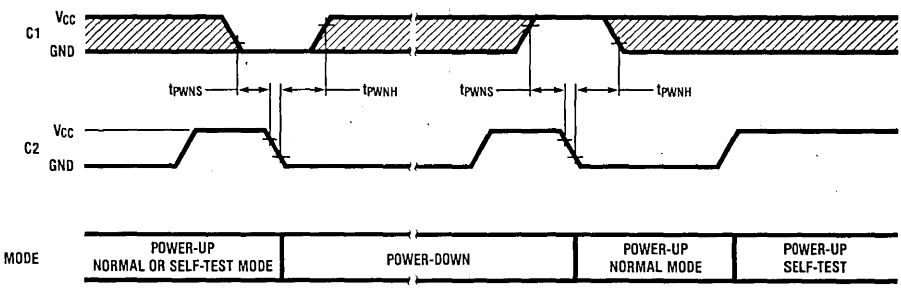


FIGURE 4. Power-Down/Power-Up Sequence

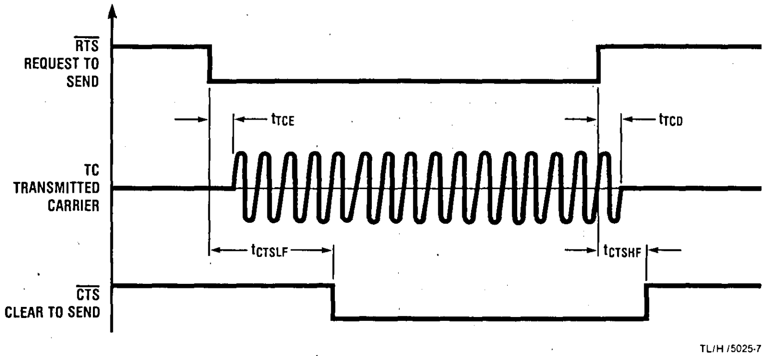
Pin Descriptions

TP3310 TP3311 Pin No.	TP3320 TP3321 Pin No.	Name	Function
1	1	TC	Transmit carrier output of the modulator. The nominal level of the FSK modulated carrier is 6 dBm into a 600Ω load (2.19V peak).
2	2	$\overline{RTS}$	TP3310/TP3320 only. Request To Send input. When this pin is asserted low by the DTE, the MODEM enables the transmit carrier output and prepares itself to transmit data. After a fixed delay has been timed out, it pulls down pin 3 ($\overline{CTS}$) in order to indicate to the DTE that it is ready to transmit data.
		$\overline{TXE}$	TP3311/TP3321 only. Transmit Carrier Enable input—active low.
3	3	$\overline{CTS}$	TP3310/TP3320 only. Clear to send output from the MODEM to the DTE—a low level on this pin indicates that the MODEM is ready to transmit data.
		CLK_X	TP3311 only. Transmit baud rate clock output.
		$\overline{STE}$	TP3321 only. Soft carrier turn-off tone enable input—active low.
4	4	D_X	Transmit data input. This pin accepts serial binary data from the DTE.
5	5	GND	This pin should be connected to ground. All digital and analog signals are referenced to this input.
—	6	$\overline{ATE}$	This is a dual function control pin. When the MODEM operates in BELL 202 modes 1 or 2 (see Table II), this pin becomes the Answer Tone Enable control input of an internal tone generator. The tone level at TC output is 6 dBm into 600Ω (2.19V peak). —When $\overline{ATE}$ is pulled low while $\overline{RTS}$ is low, a 2025 Hz answer tone is transmitted. —When $\overline{ATE}$ is pulled low while $\overline{RTS}$ is high, a 900 Hz soft carrier turn-off tone is transmitted. When the MODEM operates in the CCITT V23 mode this pin becomes the backward channel bit-rate control. —When $\overline{ATE}$ is low, 75 bit/s is selected. —When $\overline{ATE}$ is high, 150 bit/s is selected (see Table II).
3 (TP3311 only)	7	CLK_X	This output provides a TTL compatible clock signal which can be used to synchronize the transmit section of a UART. The clock frequency is 16 times the baud rate of the transmit section (1200 × 16 Hz, 600 × 16 Hz, 150 × 16 Hz or 75 × 16 Hz, depending on the operating mode). In 5 baud mode this frequency is 75 × 16 Hz.

Pin Descriptions (Continued)

TP3310 TP3311 Pin No.	TP3320 TP3321 Pin No.	Name	Function
6	8	CLK_R	This output provides a TTL compatible clock signal which can be used to synchronize the receive section of a UART. The clock frequency is 16 times the baud rate of the receive section (75 × 16 Hz, 150 × 16 Hz, 600 × 16 Hz or 1200 × 16 Hz, depending on the operating mode). When in 5 bauds the frequency is 75 × 16 Hz.
7	9	XTAL1/ CLK	On-chip oscillator input—XTAL1/CLK is the input of a high gain amplifier/inverter which oscillates when it is connected to an external 3.579545 MHz TV color-burst crystal. No other external components are necessary. An external 3.579545 MHz clock signal can be applied to input XTAL1/CLK.
8	10	XTAL2	Output of the on-chip oscillator high gain inverter.
9	11	C0	This input, C1 and C2 select the mode and standard in which the MODEM operates. Table II summarizes the various operating modes.
10	12	C1	This input, C0 and C2 select the mode and standard in which the MODEM operates. Table II summarizes the various operating modes.
11	13	C2	This input, C0 and C1 select the mode and standard in which the MODEM operates. Table II summarizes the various operating modes.
—	14	OSCOUT	Buffered master clock output (3.579545 MHz).
—	15	THRESHOLD ADJUST	This digital input selects the sensitivity of the carrier detector, see Transmission Performance.
12	16	V_{BB}	Negative power supply pin. The recommended input is $-5V \pm 5\%$.
13	17	D_R	Receive data output of the demodulator. The demodulated data is delivered to the DTE through this pin. In order to avoid transmission of erroneous data toward the data terminal, an internal switch clamps D_R to 1 when the carrier level falls below the receive threshold level.
14	18	$\overline{CD}$	Carrier Detect output. This output pin is pulled down whenever valid signals are being received at the analog input of the MODEM (RC) and are acceptable for demodulation.
15	19	RC	Receive Carrier input to the MODEM. The FSK modulated signal received from the telephone line is applied to this pin. The input level dynamic range is from -6 dBm/600Ω to -48 dBm/600Ω.
16	20	V_{CC}	Positive power supply pin. The recommended input is $5V \pm 5\%$.

Timing Diagrams



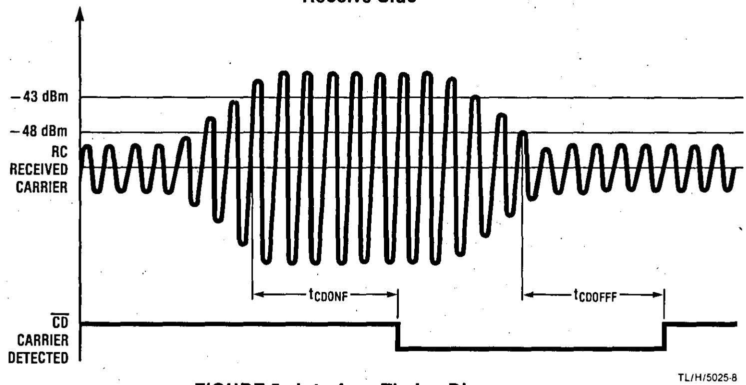


FIGURE 5. Interface Timing Diagrams

Applications Information

To realize a low cost data terminal, the MODEM can be interfaced with a UART and a microprocessor as shown in *Figures 6 and 7.* The operating mode is controlled by the microprocessor. No external baud rate generator is needed.

An active hybrid with level adjust may be realized by two operational amplifiers and a few resistors. This arrangement enables the MODEM to transmit over one channel while receiving data from the adjacent channel. No external filtering is normally necessary. A 150 pF capacitor can be connected across R2 in *Figure 7* to provide an additional 10 dB rejection above 50 kHz if required.

The transmit level can be adjusted by resistor R1. The maximum level allowed on the telephone line by most telephone companies is 0 dBm/600Ω. The transmit level is usually made adjustable between 0 dBm/600Ω and −12 dBm/600Ω. Table III gives the correspondence between the transmit level and the programming resistor value.

TABLE III

Transmit Level dBm/600Ω	Programming Resistor R1 kΩ
0	47
−1	53
−2	59
−3	66
−4	75
−5	84
−6	94
−7	105
−8	118
−9	130
−10	150
−11	167
−12	187

Typical Applications

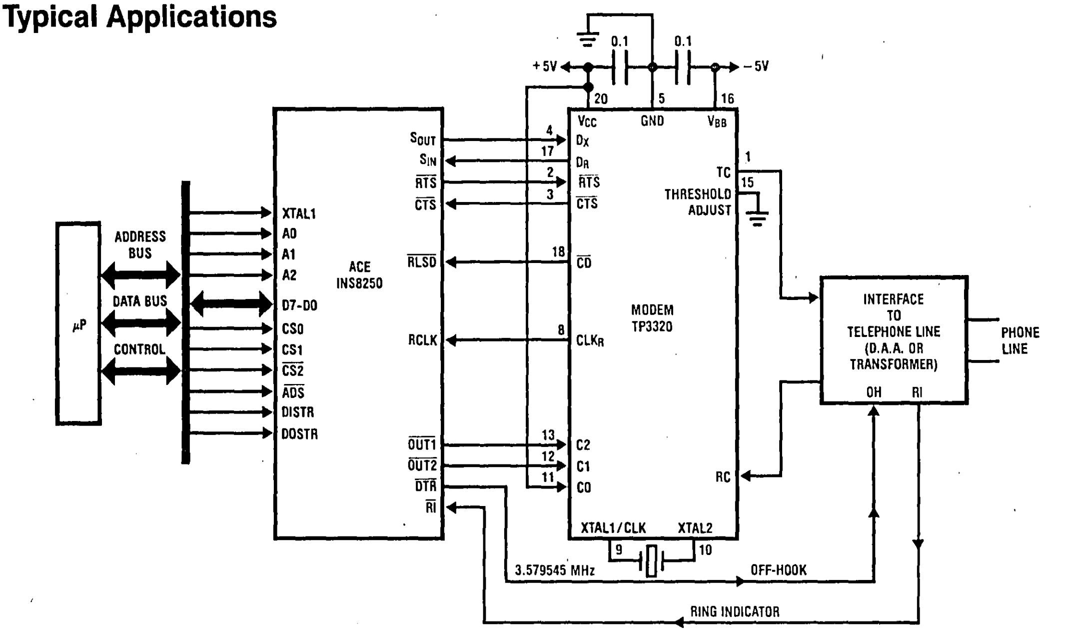


FIGURE 6. Interfacing the TP3320 with a Microprocessor

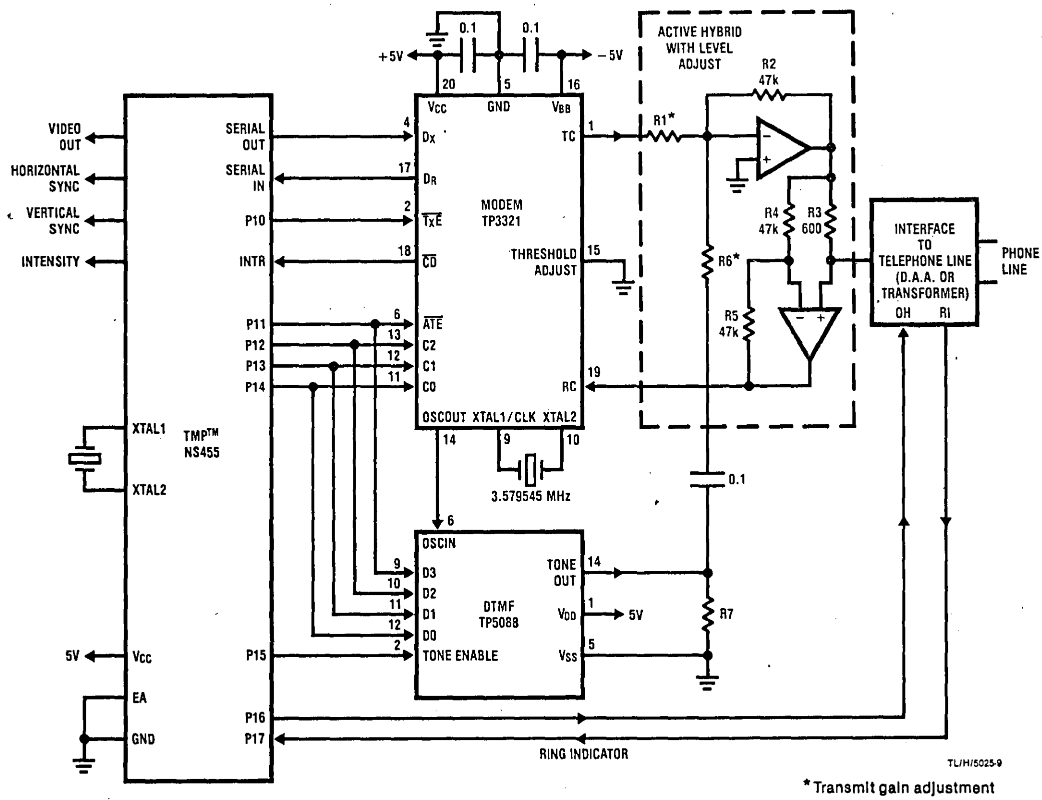


FIGURE 7. Interfacing the TP3321 and a Tone Generator with the NS455 Terminal Management Processor (The TMP includes a UART with split baud rate capability.)

National Semiconductor

PRELIMINARY

TP5087/TP5092/TP5094/TP5380 DTMF (TOUCH-TONE®) Generators

General Description

These Tone Dialers are low threshold voltage, field-implanted, metal gate CMOS integrated circuits. The devices interface directly to a standard telephone keypad and generate all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A MUTE OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 2.5V-10V operation when generating tones (TP5380)
- 2V operation of keyscan and MUTE logic
- Powered directly from telephone line
- Interfaces with standard single-contact or 2-of-8 telephone keypad
- Static sensing of key closures
- On-chip 3.579545 MHz crystal-controlled oscillator
- On-chip regulation of tone amplitudes
- High group and low group tones generated and mixed internally
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram

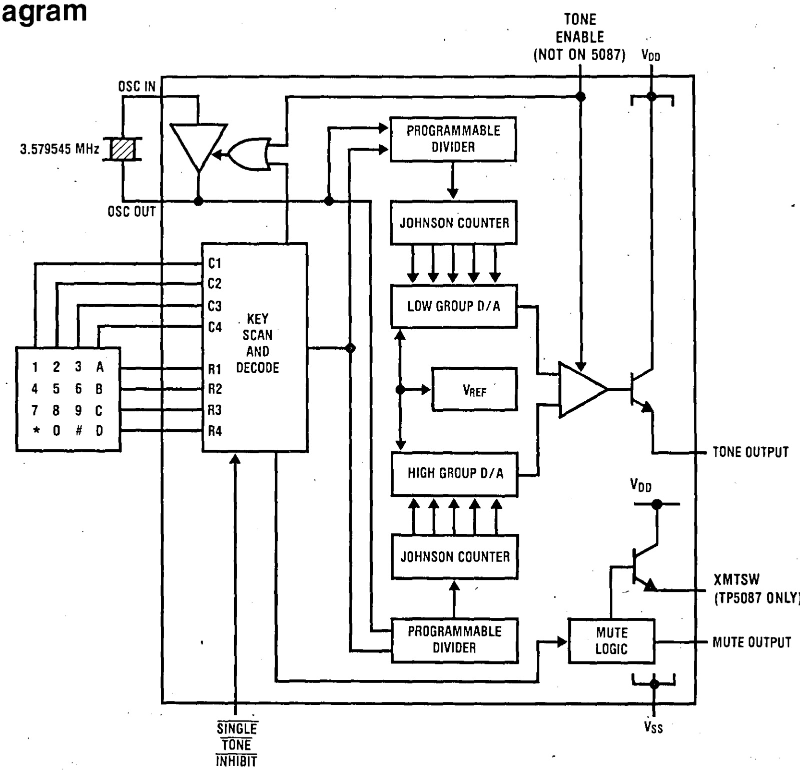


FIGURE 1. TP5087 Family

Absolute Maximum Ratings

Supply Voltage ($V_{DD}-V_{SS}$)	15V
Maximum Voltage at Any Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Operating Temperature	−30°C to +60°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

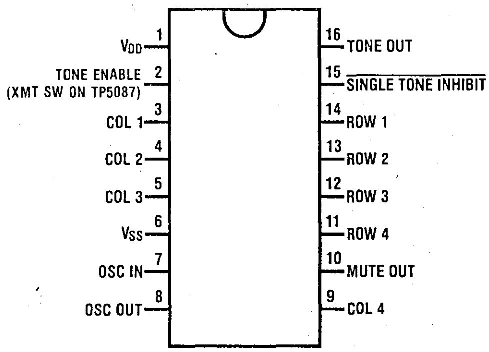
Electrical Characteristics T_A within operating temperature range, $3.5V < V_{DD} < 10V$ unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
TP5087, TP5092, TP5094						
Minimum Supply Voltage Swing, $V_{DD\,(min)}$		Generating Tones			3.5	V
Output Amplitudes		$R_L=240\Omega$				
Low Group	TP5087, TP5094			400		mVrms
	TP5092			450		mVrms
High Group	TP5087, TP5094			540		mVrms
	TP5092			620		mVrms
Mean Output DC Offset, V_{OS}		$V_D=3.5V$		1.3		V
		$V_{DD}=10V$		4.6		V
TP5380						
Minimum Supply Voltage Swing, $V_{DD\,(min)}$		Generating Tones			2.5	V
Output Amplitudes		$R_L=100\Omega$				
Low Group				170		mVrms
High Group				230		mVrms
Mean Output DC Offset, V_{OS}		$V_{DD}=2.5V$		0.7		V
		$V_{DD}=10V$		2.5		V
ALL PARTS						
Minimum Supply Voltage for Keysense and MUTE Logic Functions					2	V
Operating Current						
Idle		$R_L=$ open,		20		μA
Generating Tones		$V_{DD}=3.5V$		2		mA
Input Pull-Up Resistors						
COLUMN and ROW (Pull-Down)				40		kΩ
SINGLE TONE INHIBIT				50		kΩ
TONE ENABLE				50		kΩ
MUTE OUT Sink Current (COLUMN and ROW Inactive)		$V_{DD}=3V$, $V_o=0.5V$	0.5			mA
MUTE OUT Source Current (COLUMN and ROW Active)		$V_{DD}=3V$, $V_o=2.5V$	0.5			mA
High Group Pre-Emphasis			2.4	2.7	3.0	dB
Dual Tone/Total Harmonic Distortion Ratio		1 MHz Bandwidth	22			dB
Start-Up Time (to 90% Amplitude)		$V_{DD}\geq 4V$, $R_L\geq 150\Omega$		2	5	ms

Note 1: Crystal Specifications: Parallel Resonant, $R_S\leq 150\Omega$, L = 100 mH, $C_0=5$ pF, $C_1=0.02$ pF.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number TP5087N, TP5092N, TP5094N or TP5380N
See NS Package N16A

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically to ensure no modulation of the line when tones are not being generated. A valid key closure activates the MUTE output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

Pin Descriptions

V_{DD} (Pin 1): The positive voltage supply to the device, referenced to V_{SS}. The collectors of the TONE OUT, and XMT SW transistors are also connected to this pin.

V_{SS} (Pin 6): This is the negative voltage supply.

OSCILLATOR (Pins 7 and 8): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when both COLUMN inputs and ROW inputs are sensed sequentially with no valid input having been detected. The oscillator is also stopped when the TONE ENABLE input is pulled to logic low.

ROW and COLUMN Inputs (Pins 3, 4, 5, 9, 11, 12, 13, 14): When no key is pushed, pull-up resistors are active on COLUMN inputs and pull-down resistors are active on ROW inputs. Column latches are ON and ready to store column key closures. After a key is pushed, the row pull-down resistors cause a negative-true on COLUMN inputs which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.

TONE ENABLE Input (Pin 2): The TONE ENABLE input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When this input is at logic low, the device will be in the inactive mode, tone output will be at an open circuit state.

XMT SW Output (Pin 2 of TP5087 only): With no key inputs, this output is pulled high by the open emitter of an NPN transistor. Any key entry turns off this transistor by pulling its base to V_{SS}.

MUTE Output (Pin 10): The MUTE output is a conventional CMOS output that sinks current to V_{SS} with no valid input and sources current from V_{DD} when a valid key input is sensed. The MUTE output will switch regardless of the state of the $\overline{\text{SINGLE TONE INHIBIT}}$ input.

$\overline{\text{SINGLE TONE INHIBIT}}$ Input (Pin 15): The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-up resistor to V_{DD}, and when left open or tied to V_{DD}, single or dual tones may be generated in accordance with Table II. When forced to V_{SS}, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

TONE OUT (Pin 16): This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current.

Applications Information

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sine-wave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion, while increasing the source impedance of the device as seen from its power supply terminals. Note that the DTMF generator is a current source which modulates its own supply terminals in a conventional telephone application.

TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

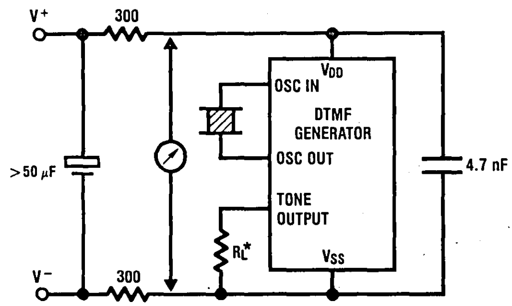
TABLE II. FUNCTIONAL TRUTH TABLE

$\overline{\text{SINGLE TONE INHIBIT}}$	TONE ENABLE	ROW	COLUMN	Tones Low	Tones High	MUTE
X	0	X	X	0V	0V	0
X	X	O/C	O/C	0V	0V	0
X	1	One	One	f_L	f_H	1
1	1	2 or More	One	—	f_H	1
1	1	One	2 or More	f_L	—	1
1	1	2 or More	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	One	V_{OS}	V_{OS}	1
0	1	One	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	2 or More	V_{OS}	V_{OS}	1

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.

Note 3: TONE ENABLE and $\overline{\text{SINGLE TONE INHIBIT}}$ have internal pull-up resistors.



* Adjust R_L for desired tone amplitudes.

FIGURE 2. Amplitude and Distortion Measurements for Conventional Telephone Applications

National Semiconductor

PRELIMINARY

TP5088 DTMF Generator for Binary Data

General Description

This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. 4-bit binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, data is latched into the device and the selected tone pair from the standard DTMF frequencies is generated. An open-drain N-channel transistor provides a MUTE output during tone generation.

Features

- 2.5V–15V operation
- Direct microprocessor interface
- Binary data inputs with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Better than 0.64% frequency accuracy
- High group pre-emphasis
- Low harmonic distortion
- MUTE output interfaces to speech network
- Low power idle mode

Block Diagram

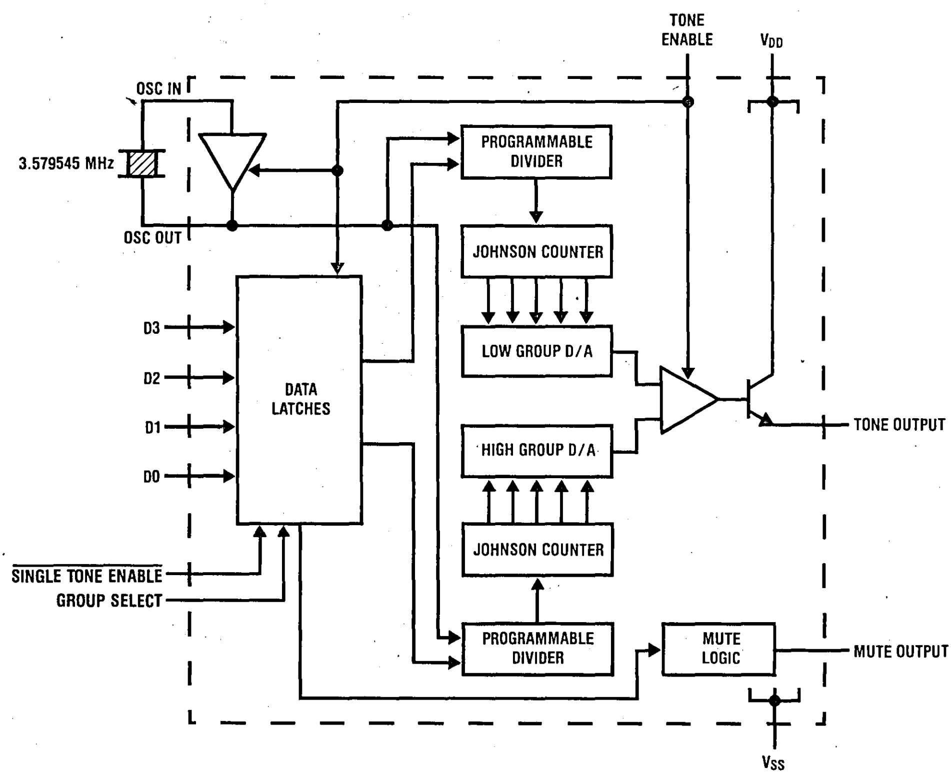


FIGURE 1

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	15V	Operating Temperature, T_A	−30°C to +60°C
$\overline{\text{MUTE}}$ Voltage	15V	Storage Temperature	−55°C to +150°C
Maximum Voltage at Any Other Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$	Maximum Power Dissipation	500 mW

Electrical Characteristics

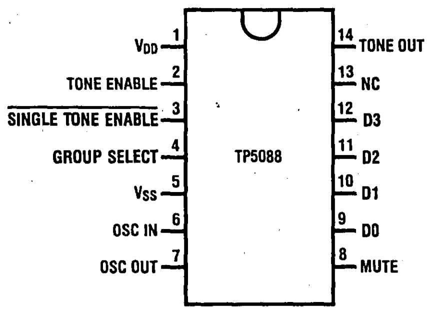
T_A within operating temperature range, $V_{SS}=0V$, $3V < V_{DD} < 10V$ unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	Generating Tones	3		12	V
Supply Voltage for Data Input, TONE ENABLE and MUTE Logic Functions		2.25		12	V
Operating Current					
Idle	$R_L = 10\ k\Omega$, D0–D3 Open		100		μA
Generating Tones	$V_{DD}=5V$		2		mA
Input Pull-Up Resistance					
D0–D3			100		kΩ
TONE ENABLE			50		kΩ
MUTE OUT Sink Current (TONE ENABLE High)	$V_{DD}=3V$ $V_o=0.5V$	0.5			mA
MUTE OUT Leakage Current (TONE ENABLE Low)	$V_{DD}=3V$ $V_o=0V$		1		μA
Output Amplitudes	$R_L=100\Omega$				
Low Group			170		mVrms
High Group			230		mVrms
Mean Output DC Offset	$V_{DD}=2.5V$		1.0		V
	$V_{DD}=10V$		3.0		V
High Group Pre-Emphasis			2.7		dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth	20			dB
Start-Up Time (to 90% Amplitude), t_{OSC}			4		ms
Data Set-Up Time, t_S (*Figure 2*)	$V_{DD}=2V$	300			ns
Data Hold Time, t_H		300			ns

Note 1: Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, $L = 100$ mH, $C_0 = 5$ pF, $C_1 = 0.02$ pF.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number TP5088N
See NS Package N14A

Functional Description

With the TONE ENABLE pin pulled high, the device is in a low power idle mode, with the oscillator inhibited and the output transistor turned off. Data on inputs D0–D3 is ignored until a rising transition on TONE ENABLE. Data meeting the timing specifications is latched in, the oscillator and output stage are enabled, and tone generation begins. The decoded data sets the high group and low group programmable counters to the appropriate divide ratios. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}.

Table I shows the accuracies of the tone output frequencies and Table II is the Functional Truth Table.

TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	697	694.8	−0.32
	770	770.1	+0.02
	852	852.4	+0.03
	941	940.0	−0.11
High Group f_H	1209	1206.0	−0.24
	1336	1331.7	−0.32
	1477	1486.5	+0.64
	1633	1639.0	+0.37

Pin Descriptions

V_{DD} (Pin 1): This is the positive supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is also connected to this pin.

V_{SS} (Pin 5): This is the negative voltage supply.

Oscillator (Pins 6 and 7): All tone generation timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 6 and 7. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator is stopped when the TONE ENABLE input is pulled to logic low.

TONE ENABLE Input (Pin 2): This input has an internal pull-up resistor. When TONE ENABLE is pulled to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on TONE ENABLE latches in data from D0–D3. The oscillator starts, and tone generation continues until TONE ENABLE is pulled low again.

MUTE (Pin 8): This output is an open-drain N-channel device that sinks current to V_{SS} when TONE ENABLE is low and no tones are being generated. The device turns off when TONE ENABLE is high.

D3, D2, D1, D0 (Pins 9, 10, 11, 12): These are the inputs for binary-coded data, which is latched in on the rising edge of TONE ENABLE. Data must meet the timing specifications of *Figure 2*. At all other times these inputs are ignored and may be multiplexed with other system functions.

TONE OUT (Pin 14): This output is the open emitter of an NPN transistor, the collector of which is connected internally to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group tones superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

TABLE II. FUNCTIONAL TRUTH TABLE

Keyboard Equivalent	Data Inputs D3	D2	D1	D0	TONE ENABLE	TONES OUT f_L (Hz)	f_H (Hz)	MUTE
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	↑	697	1209	O/C
2	0	0	1	0	↑	697	1336	O/C
3	0	0	1	1	↑	697	1477	O/C
4	0	1	0	0	↑	770	1209	O/C
5	0	1	0	1	↑	770	1336	O/C
6	0	1	1	0	↑	770	1477	O/C
7	0	1	1	1	↑	852	1209	O/C
8	1	0	0	0	↑	852	1336	O/C
9	1	0	0	1	↑	852	1477	O/C
0	1	0	1	0	↑	941	1336	O/C
*	1	0	1	1	↑	941	1209	O/C
#	1	1	0	0	↑	941	1477	O/C
A	1	1	0	1	↑	697	1633	O/C
B	1	1	1	0	↑	770	1633	O/C
C	1	1	1	1	↑	852	1633	O/C
D	0	0	0	0	↑	941	1633	O/C

Timing Diagram

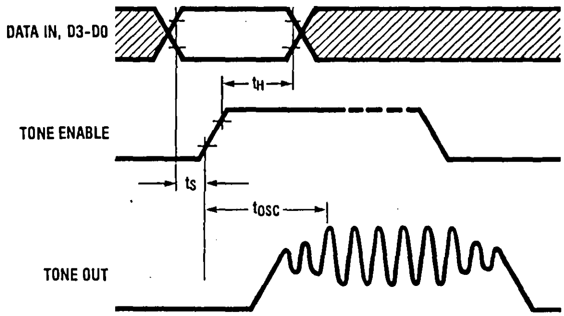


FIGURE 2

Typical Application

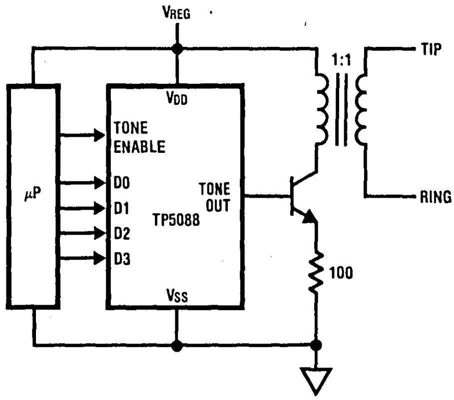


FIGURE 3

National Semiconductor

PRELIMINARY

TP5089 DTMF (TOUCH-TONE®) Generator

General Description

The TP5089 is a low threshold voltage, field-implanted, metal gate CMOS integrated circuit. It interfaces directly to a standard telephone keypad and generates all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A $\overline{\text{MUTE}}$ OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 3V–10V operation when generating tones
- 2V operation of keyscan and $\overline{\text{MUTE}}$ logic
- Static sensing of key closures or logic inputs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Output amplitudes proportional to supply voltage
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram

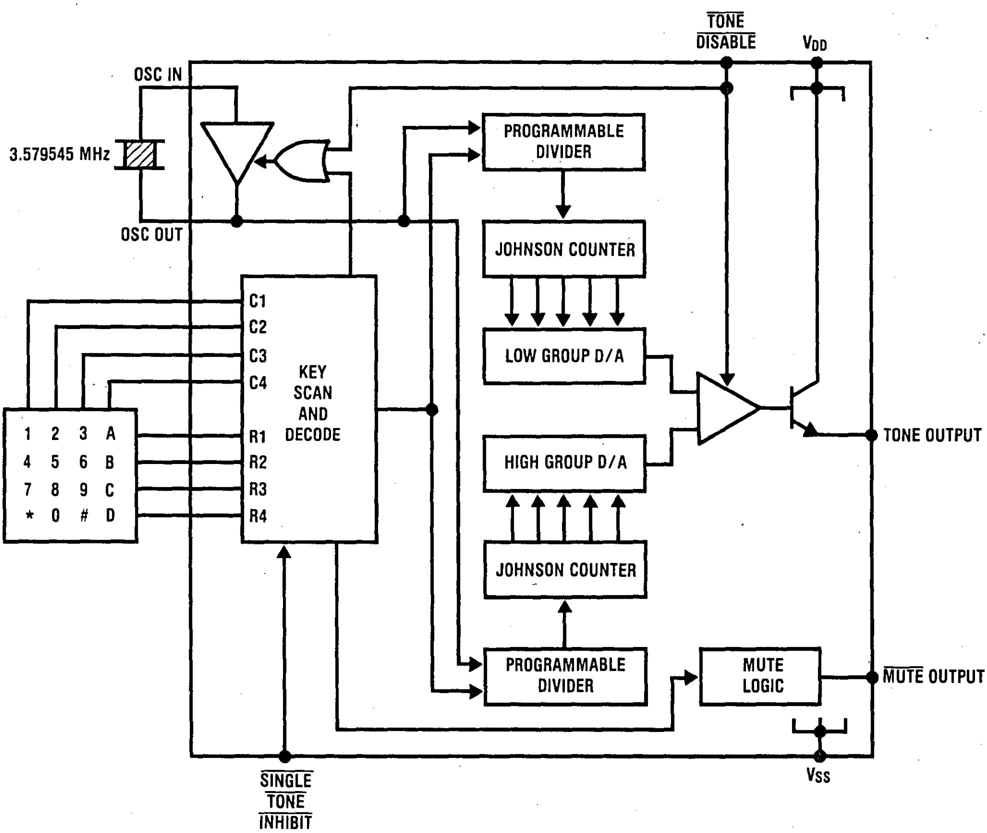


FIGURE 1

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	15V
Maximum Voltage at Any Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Operating Temperature	$-30°C$ to $+60°C$
Storage Temperature	$-55°C$ to $+150°C$
Maximum Power Dissipation	500 mW

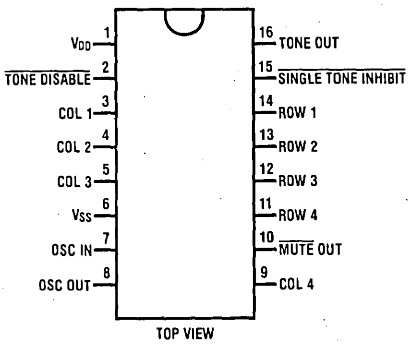
Electrical Characteristics T_A within operating temperature range, $3V < V_{DD} < 10V$ unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage for Keysense and $\overline{\text{MUTE}}$ Logic Functions				2	V
Operating Current					
Idle	$R_L = 10\ k\Omega$		20		μA
Generating Tones	$V_{DD} = 5V$		2		mA
Input Resistors					
COLUMN and ROW (Pull-Up)			40		kΩ
$\overline{\text{SINGLE TONE INHIBIT}}$ (Pull-Down)			50		kΩ
$\overline{\text{TONE DISABLE}}$ (Pull-Up)			50		kΩ
$\overline{\text{MUTE}}$ OUT Sink Current (COLUMN and ROW Active)	$V_{DD} = 3V$, $V_o = 0.5V$	0.5			mA
Output Amplitudes	$R_L = 240\Omega$				
Low Group	$V_{DD} = 3V$		250		mVrms
	$V_{DD} = 10V$		850		mVrms
High Group	$V_{DD} = 3V$		315		mVrms
	$V_{DD} = 10V$		1000		mVrms
Mean Output DC Offset	$V_{DD} = 3V$		1.2		V
	$V_{DD} = 10V$		4.2		V
High Group Pre-Emphasis		2.4	2.7	3.0	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth	22			dB
Start-Up Time (to 90% Amplitude)			3	5	ms

Note 1: Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

Connection Diagram

Dual-In-Line Package



Order Number TP5089N
See NS Package N16A

Pin Descriptions

V_{DD} (Pin 1): This is the positive voltage supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is connected to this pin.

V_{SS} (Pin 6): This is the negative voltage supply.

OSCILLATOR (Pins 7 and 8): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545- MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when column inputs are sensed with no valid input having been detected. The oscillator is also stopped when the $\overline{\text{TONE DISABLE}}$ input is pulled to logic low.

Row and Column Inputs (Pins 3, 4, 5, 9, 11, 12, 13, 14): When no key is pushed, pull-up resistors are active on row and column inputs. A key closure is recognized when a single row and a single column are connected to V_{SS}, which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.

Pin Descriptions (Continued)

$\overline{\text{TONE DISABLE}}$ Input (Pin 2): The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, TONE OUTPUT will be at an open circuit state.

$\overline{\text{MUTE}}$ Output (Pin 10): The $\overline{\text{MUTE}}$ output is an open-drain N-channel device that sinks current to V_{SS} with any key input and is open when no key input is sensed. The $\overline{\text{MUTE}}$ output will switch regardless of the state of the $\overline{\text{SINGLE TONE INHIBIT}}$ input.

$\overline{\text{SINGLE TONE INHIBIT}}$ Input (Pin 15): The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-down resistor to V_{SS}, and when left open or tied to V_{SS} any input condition that would normally result in a single tone will now result in no tone, with all other functions operating normally. When tied to V_{DD}, single or dual tones may be generated, see Table II.

TONE OUT (Pin 16): This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current.

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sine-wave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion.

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically to ensure no modulation of the line when tones are not being generated. Any key closure activates the $\overline{\text{MUTE}}$ output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

The amplitude of the output tones is directly proportional to the device supply voltage.

TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

TABLE II. FUNCTIONAL TRUTH TABLE

$\overline{\text{SINGLE TONE INHIBIT}}$	$\overline{\text{TONE DISABLE}}$	ROW	COLUMN	Tones Low	Tones High	$\overline{\text{MUTE}}$
X	O	X	X	0V	0V	0
X	X	O/C	O/C	0V	0V	0
X	1	One	One	f_L	f_H	1
1	1	2 or More	One	—	f_H	1
1	1	One	2 or More	f_L	—	1
1	1	2 or More	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	One	V_{OS}	V_{OS}	1
0	1	One	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	2 or More	V_{OS}	V_{OS}	1

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.

Functional Description (Continued)

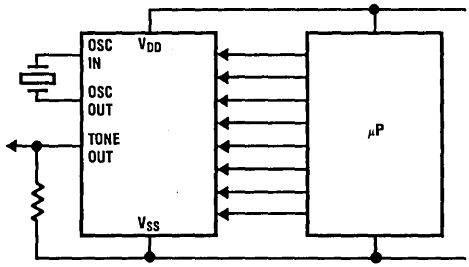


FIGURE 2. Typical Application

National Semiconductor

microCMOS

TP5116A, TP5156A Monolithic CODECs

General Description

The TP5116A and TP5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP5116A is intended for μ-law applications and the TP5156A is for A-law applications.

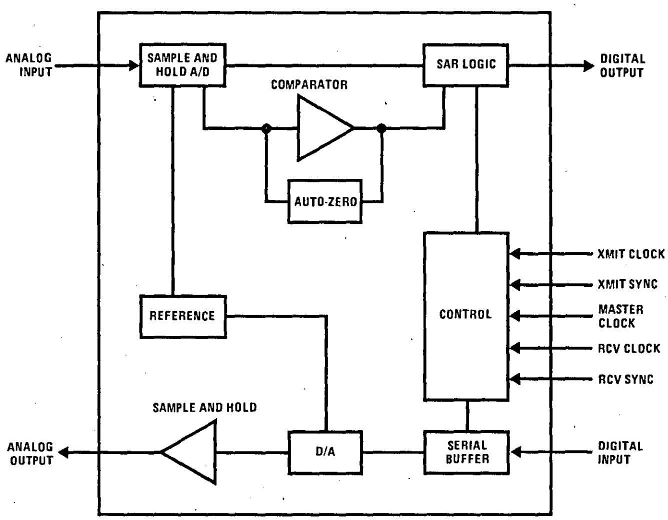
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

All devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

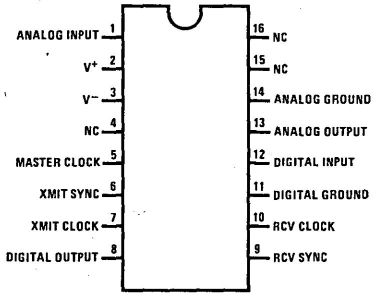
- Low operation power — 40 mW typical
- ±5V operation
- TTL compatible digital interface
- Precision voltage reference on-chip
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP5116A—μ-law coding (sign plus magnitude format)
- TP5156A—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number TP5116AJ or TP5156AJ
See NS Package J16S

Absolute Maximum Ratings

Operating Temperature	−25°C to +125°C
Storage Temperature	−65°C to +150°C
V^+ with Respect to DIGITAL GROUND	7V
V^+ with Respect to V^-	14V
V^- with Respect to DIGITAL GROUND	−7V
Voltage at Any Analog Input or Output	V^--0.3V to V^+ +0.3V
Voltage at Any Digital Input or Output	GNDD−0.3V to V^+ +0.3V

DC Electrical Characteristics

Unless otherwise noted T_A=0°C to 70°C, V^+ =5.0V ±5%, V^- = −5.0V ±5%. Typical characteristics are specified at V^+ =5.0V, V^- = −5.0V and T_A=25°C. All digital signals are referenced to DIGITAL GROUND. All analog signals are referenced to ANALOG GROUND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0V<V_{IN}<V^+$	−10		10	μA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	I_{OL}=3.2 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}=6 mA	2.4			V
ANALOG INTERFACE						
Z_I	Analog Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2			kΩ
	Output Impedance at Analog Output			10	20	Ω
	Analog Input Bias Current	V_{IN}=0V	−0.1		0.1	μA
C1	DC Blocking Time Constant		4.0			ms
	DC Blocking Capacitor		0.1			μF
	Input Bias Resistor				50	kΩ
ER DISSIPATION						
	Operating Current, V_{CC}			3.5	8.0	mA
	Operating Current, V_{BB}			3.5	8.0	mA

Electrical Characteristics

ss otherwise noted, T_A=25°C, V^+ =5.0V, V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL T is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are x corrected.

ool	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP5116A is 1.227 Vrms and 1.231 Vrms for the TP5156A. The resulting nominal overload level is 2.5V peak for all devices. All gain measurements for the encode and decode portions of the devices are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	T_A=25°C, V^+ =5V, V^- = −5V	−0.125		0.125	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A=0°C to 70°C	−0.05		0.05	dB

AC Electrical Characteristics (Continued)

Unless otherwise noted, $T_A = 25°C$, $V^+ = 5.0V$, $V^- = -5.0V$. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$	−0.125		0.125	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V^+ = 5V \pm 5\%$, $V^- = -5V \pm 5\%$	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 35 29 25			 d c c
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 35 29 25			 (((
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			8	dI
N_X	Transmit Idle Channel Noise	Tp5116A, $VF_X = 0V$ (No Signaling) TP5156A, $VF_X = 0V$			13 −66	dI dI
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, $V_{CC} = 5.0 V_{DC}$ + 200 mVrms, f = 1.02 kHz	50			
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, $V_{CC} = 5.0 V_{DC}$ + 200 mVrms, f = 1.02 kHz	40			
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, $V_{BB} = -5.0 V_{DC}$ + 200 mVrms, f = 1.02 kHz	50			
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, $V_{BB} = -5.0 V_{DC}$ + 200 mVrms, f = 1.02 kHz	45			dL
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			−75	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V TP5116A TP5156A			 −70 −65 (Note 1)	 dB dB

Note 1: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

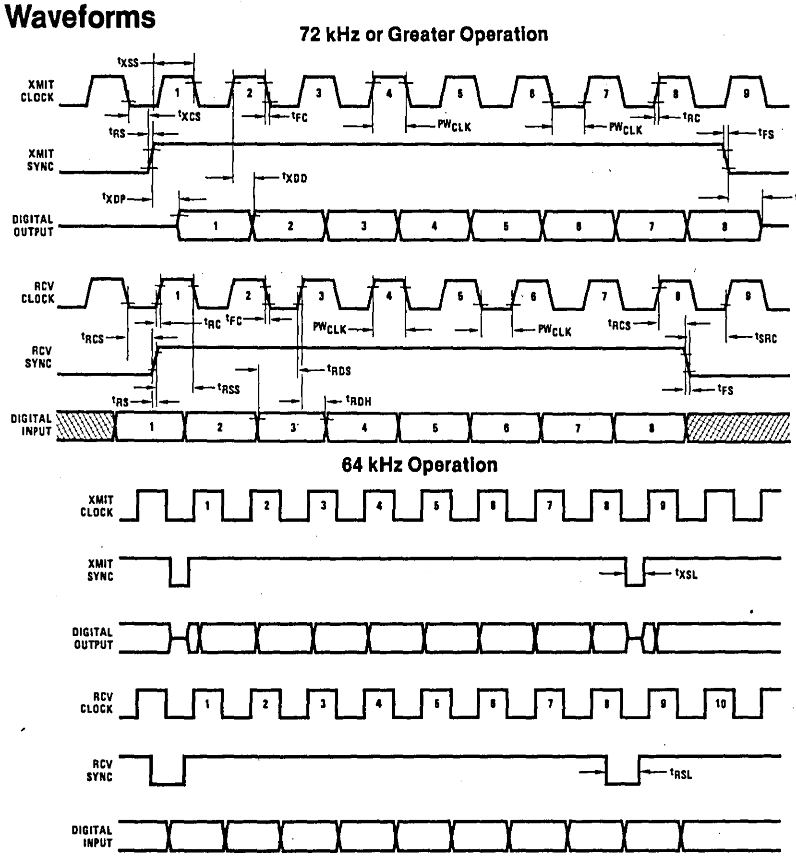
Timing Specifications

Unless otherwise noted, $T_A = 0°C$ to $70°C$, $V^+ = +5V \pm 5\%$, $V^- = -5V \pm 5\%$. All digital signals are referenced to DIGITAL GROUND and are measured at V_{IH} and V_{IL} as indicated in the Timing Waveforms.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_M	MASTER CLOCK Frequency		1.5	2.048	2.1	MHz
F_X, F_R	XMIT, RCV CLOCK Frequency		0.064	2.048	2.1	MHz
PW_{CLK}	Clock Pulse Width	MASTER, XMIT, RCV CLOCKS	150			ns
t_{RC}, t_{FC}	Clock Rise and Fall Time	MASTER, XMIT, RCV CLOCKS			50	ns
t_{RS}, t_{FS}	Sync Pulse Rise and Fall Time	RCV, XMIT SYNC			50	ns
t_{RCS}, t_{XCS}	Clock to Sync Delay	RCV, XMIT	0			ns
t_{XSS}	XMIT SYNC Set-Up Time		150			ns
t_{XDD}	XMIT Data Delay	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDP}	XMIT Data Present	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDT}	XMIT Data TRI-STATE®				150	ns
t_{SRC}	RCV CLOCK to RCV SYNC Delay		0			ns
t_{RDS}	RCV Data Set-Up Time		0			ns
t_{RSS}	RCV SYNC Set-Up Time		150			ns
t_{RDH}	RCV Data Hold Time		100			ns
t_{XSL}	XMIT SYNC Low Time	64 kHz Operation	300			ns
t_{RSL}	RCV SYNC Low Time	64 kHz Operation	17			(Note 1)

Note 1: RCV SYNC must remain low for 17 cycles of MASTER CLOCK.

Timing Waveforms



Description of Pin Functions

Pin No.	Name	Function
1	ANALOG INPUT	ANALOG INPUT to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
2	V^+	5V (±5%) input.
3	V^-	−5V (±5%) input.
4	NC	Unused.
5	MASTER CLOCK	MASTER CLOCK input used to operate the internal encode and decode sequencers. Should be 1.536 MHz, 1.544 MHz or 2.048 MHz.
6	XMIT SYNC	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight XMIT CLOCK cycles wide.
7	XMIT CLOCK	Transmit bit clock input used to shift out the PCM data on DIGITAL OUTPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with RCV CLOCK.
8	DIGITAL OUTPUT	Serial PCM TRI-STATE® output from encoder. During the encoder time slot, the PCM code for the previous sample of ANALOG INPUT is shifted out, most significant bit first, on the rising edge of XMIT CLOCK.
9	RCV SYNC	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight RCV CLOCK cycles wide.
10	RCV CLOCK	Receive bit clock input used to shift in the PCM data on DIGITAL INPUT. May operate from 64 kHz to 2048 MHz. May be asynchronous with XMIT CLOCK.
11	DIGITAL GROUND	All digital levels referenced to the DIGITAL GROUND pin.
12	DIGITAL INPUT	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DIGITAL INPUT, most significant bit first, on the rising edge of RCV CLOCK.
13	ANALOG OUTPUT	ANALOG OUTPUT from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
14	ANALOG GROUND	All analog signals are referenced to the ANALOG GROUND pin.
15	NC	Not connected.
16	NC	Not connected.

ENCODING FORMAT AT DIGITAL OUTPUT

	TP5116A Sign + Magnitude	TP5156A A-Law (Includes Even Bit Inversion)
V_{IN} = + Full-Scale	1 1 1 1 1 1 1 1	1 0 1 0 1 0 1 0
V_{IN} = 0V	1 0 0 0 0 0 0 0	1 1 0 1 0 1 0 1
	0 0 0 0 0 0 0 0	0 1 0 1 0 1 0 1
V_{IN} = − Full-Scale	0 1 1 1 1 1 1 1	0 0 1 0 1 0 1 0

Functional Description

Approximately 4 μs after the rising edge of the XMIT SYNC pulse, the voltage present on the ANALOG INPUT is sampled and the process of encoding that sample into a PCM code is begun. Simultaneously, the 8-bit PCM code corresponding to the previous sample is shifted out of the DIGITAL OUTPUT, MSB first, on the rising edge of the next eight cycles of the XMIT CLOCK. When XMIT SYNC (which is normally eight XMIT CLOCK cycles long) goes low, the TRI-STATE® DIGITAL OUTPUT is returned to the high impedance state. On the TP5116A, the PCM code is in a μ-law sign plus magnitude format. The TP5156A uses the standard A-law coding.

An 8-bit PCM code is shifted into DIGITAL INPUT on the rising edge of the first eight RCV CLOCK pulses after RCV SYNC goes high. RCV SYNC is nominally eight RCV CLOCK cycles wide. Approximately 15 μs after RCV SYNC goes low, the ANALOG OUTPUT is updated to the voltage corresponding to the PCM input code.

All encoding and decoding operations are run off the MASTER CLOCK. MASTER CLOCK should be in the range of 1.536 MHz to 2.048 MHz and must be synchronous with XMIT CLOCK. The XMIT and RCV CLOCK may vary from 64 kHz to 2.048 MHz.

Encoding Delay

The encoding process begins immediately at the beginning of the encode time slot and is concluded no later than 18 time slots later. In normal applications, the PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz MASTER CLOCK, the FS rate could be increased to 15 kHz, reducing the delay from 125 μs to 67 μs.

Functional Description (Continued)

Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 MASTER CLOCK cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or, 81 μs for a 1.544 MHz system with an 8 kHz frame rate or, 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

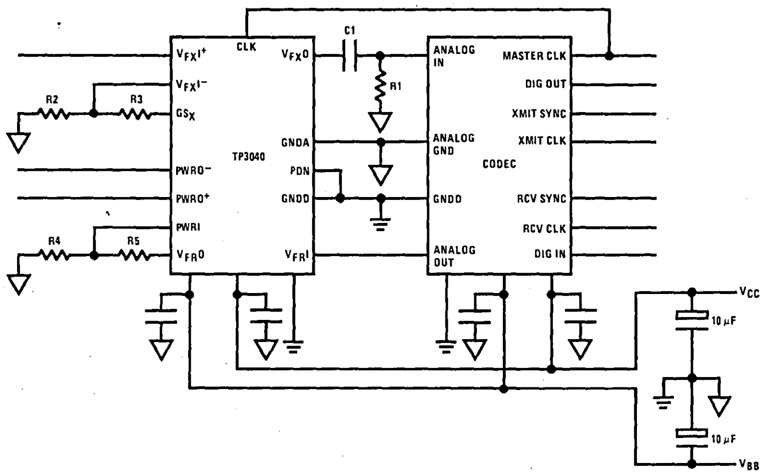
Typical Application

A typical application of these CODECs used in conjunction with the TP3040 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1 × C1 should exceed 4 ms.

$$\text{XMIT GAIN} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\,\text{dB}$$

$$\text{RCV GAIN} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of these CODECs, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. For card insertion into a hot connector, care should be taken to insure that GNDA and GNDD are contacted prior to V_{CC} and V_{BB}.



National Semiconductor

PRELIMINARY

microCMOS

TP5600, TP5605, TP5610, TP5615 Ten-Number Repertory Pulse Dialers

General Description

The TP5600, TP5605, TP5610, TP5615 are monolithic integrated circuits built using National's advanced P^2CMOS process (double poly-silicon gate CMOS). They provide all logic necessary to convert keypad inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory provides storage for nine telephone numbers plus the last number dialed, each up to 16 digits in length. The simple control scheme needs only 2 key entries to store a number or initiate automatic dialing of a stored number. This control scheme is the same as that used on the TP5650 repertory DTMF generator so that no user re-education is necessary when converting from pulse to tone dialing. For PBX applications, the first 1 or 2 digits may be overwritten to obtain a second dial tone prior to automatic dialing. Two outputs are provided to control pulsing of the telephone line and muting of the receiver. The low voltage and low current requirements of this device allow direct telephone line powered operation for dialing. A small battery is recommended for on-hook memory retention.

Features

- 2V, 150 μA telephone-line powered operation
- 1 μA memory retention current
- Stores and auto-dials ten 16-digit numbers
- Last-number-redial included
- Scratchpad (number storage without dialing)
- Control key scheme—same as TP5650 DTMF repertory dialer
- 2-digit overwrite for PBX access codes
- Voltage regulator on-chip
- Single-contact or negative-common key inputs
- TP5600, TP5605 for pulsing loop in shunt with speech network
- TP5610, TP5615 for pulsing loop in series with speech network
- TP5600, TP5610 pin compatible with TP50981/2 pulse dialers; ceramic resonator oscillator
- TP5605, TP5615 have RC oscillator and IDP select

Block Diagram

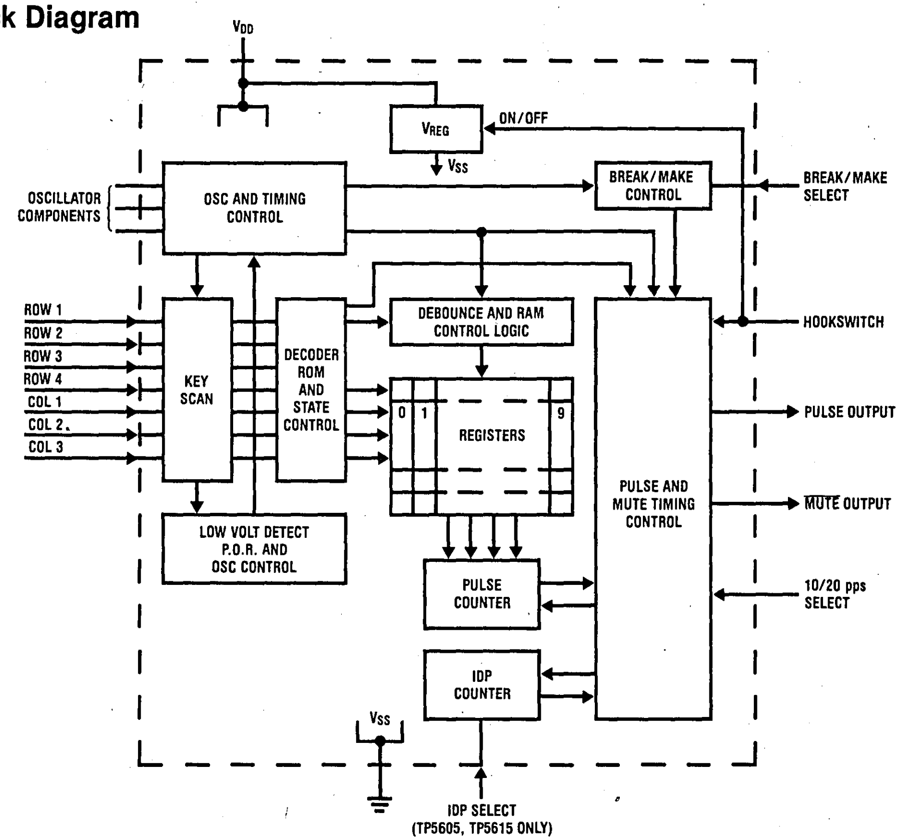


FIGURE 1

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}-V_{SS})	6V
Voltage on Any Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature (T_A)	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation (25°C)	500 mW

DC Electrical Characteristics

T_A within operating temperature range, $2V < V_{DD} - V_{SS} < 5V$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Operating Current, I_{DD}	V_{DD} = 2V (Note 1) V_{DD} = 5V (Note 1)	 1		150 	μA mA
Regulator Voltage	I_{DD} = 150 μA		3.5		V
Memory Retention Current	On-Hook, V_{DD} = 2V			1	μA
PULSE Sink Current	V_{DD} = 2V, V_{OUT} = 0.5V	50			μA
PULSE Source Current	V_{DD} = 2V, V_{OUT} = 1.5V	150			μA
MUTE Sink Current	V_{DD} = 2V, V_{OUT} = 0.5V	50			μA
MUTE Source Current	V_{DD} = 2V, V_{OUT} = 1.5V	150			μA
Logic '0' Level Input		V_{SS}		0.2 V_{DD}	
Logic '1' Level Input		0.8 V_{DD}		V_{DD}	
Keyscan Pull-Up Resistance			100		kΩ
Keyscan Pull-Down Resistance			4		kΩ
Keypad Contact Resistance				1	kΩ
Keypad Capacitance				30	pF
HOOKSWITCH Pull-Up Resistance			100		kΩ
ıput Leakage Current B/M SELECT, IDP SELECT, 0/20 pps SELECT	$V_{SS} < V_{IN} < V_{DD}$		0.1		μA

Electrical Characteristics

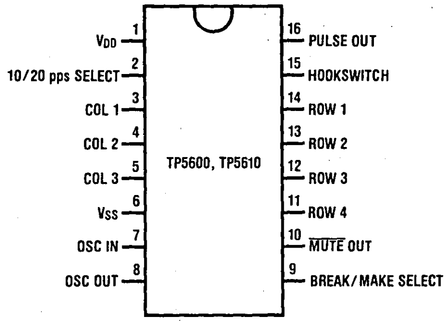
ithin operating temperature range, $2V < V_{DD} - V_{SS} < 5V$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
)0, TP5610 cillator Frequency	*Figure 3* Component Values		480		kHz
)5, TP5615 cillator Frequency	*Figure 4* Component Values		16		kHz
lator Stability	Internal Regulator Connected, 150 μA < I_{DD} < 300 μA	−3		3	%
arts					
eypad Debounce Time	OSC IN = Nominal Frequency	9		12	ms
Key Closure Time		25			ms
Oscillator Start-Up Time	V_{DD} = 2V		5		ms
Pulse Rate			10		pps
BREAK Time, t_B	BREAK/MAKE = V_{DD} BREAK/MAKE = V_{SS}		60 66		ms ms

Note 1: Off-hook, HOOKSWITCH pin connected to V_{SS}, all outputs open.

Connection Diagrams

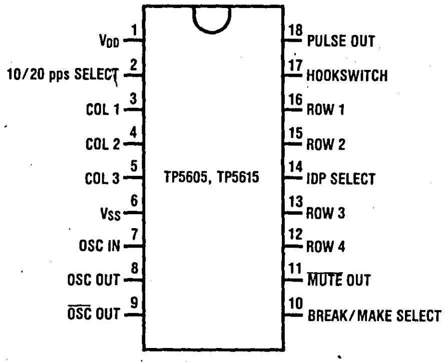
Dual-In-Line Package



TOP VIEW

Order Number TP5600N or TP5610N
See NS Package N16A

Dual-In-Line Package



TOP VIEW

Order Number TP5605N or TP5615N
See NS Package N18A

Pin Descriptions

V_{DD} (pin 1): This is the positive supply to the device and is referenced to V_{SS} (pin 6). An active zener regulator is connected on-chip between V_{DD} and V_{SS} (see pin 6), and the device is intended to be powered from a current-limited source. This regulator is turned off and effectively disconnected when the device is in the on-hook state in order to minimize current consumption. Power-on reset and low voltage detect circuits ensure correct operation following power-up or reduction of the on-hook supply voltage below that required to retain stored data.

Keypad Inputs: A valid key entry is defined as either connecting a single row to a single column or connecting V_{SS} simultaneously to a single row and a single column. This allows direct interface to an inexpensive single-contact (form A) keypad, the standard 2-of-7 keypad with negative-common, or logic-generated inputs.

V_{SS} (pin 6): This is the negative supply.

OSC IN, OSC OUT (pins 7, 8 on TP5600, TP5610 only): The device contains an on-chip oscillator circuit designed to work with a ceramic resonator at 480 kHz in anti-resonant mode. 2 external capacitors are required, typically 100 pF each *(Figure 3)*. The circuit may also be driven with an external 480 kHz source on OSC IN.

OSC IN, OSC OUT, $\overline{\text{OSC}}$ OUT (pins 7, 8 and 9 on TP5605, TP5615 only): The device includes a stable on-chip oscillator circuit designed to work with the component values shown in *Figure 4*. The circuit may also be driven with an external 16 kHz source on OSC IN (pin 7).

On all devices, the oscillator runs only while the device is scanning the keypad and/or timing storage or outpulsing functions.

BREAK/MAKE SELECT: The BREAK/MAKE ratio is selected by connecting this pin as follows (no pull-up resistor is provided):

Input to BREAK/MAKE Pin	PULSE Output	
	BREAK	MAKE
V_{DD}	60%	40%
V_{SS}	66%	34%

$\overline{\text{MUTE}}$ OUT: This is an open-drain n-channel output designed to drive a simple interface circuit to mute the receiver during outpulsing. See the timing diagram for further details.

HOOKSWITCH: This input has a 100 kΩ internal pull-up resistor to V_{DD}. Allowing this pin to float, or connecting a V_{DD} level puts the circuit in the on-hook, low power idl mode. It also turns off the active zener regulator.

Connecting this pin to V_{SS} puts the circuit in the off-h mode, ready to accept key inputs and generate outp ing. It also turns on the zener regulator to limit the volt across the device. See Applications Information for ther information.

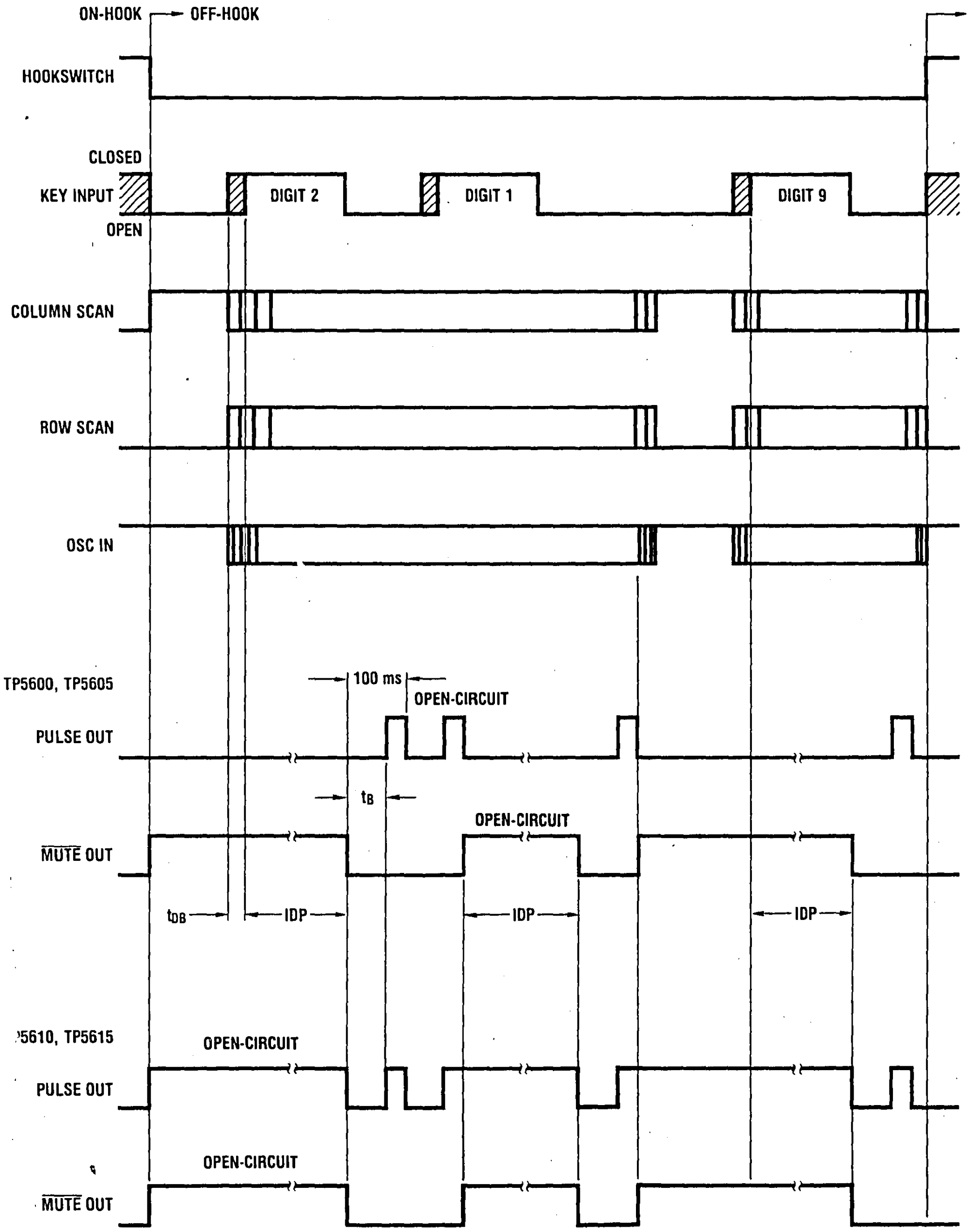
PULSE OUT: This is an open-drain n-channel o designed to drive a simple interface circuit to pulse the phone line with the correct BREAK/MAKE ratio, IDP ti and pulse rate.

IDP SELECT (TP5605, TP5615 only): The Inter-D Pause period is selected by connecting this pin as fo (no pull-up resistor is provided):

Input to IDP Pin	IDP Period
V_{DD}	825 ms
V_{SS}	525 ms

10/20 pps SELECT (pin 2): For normal 10 pps dialing, c nect this pin to V_{SS}. Connecting this pin to V_{DD} doubles t rate of all PULSE OUT and $\overline{\text{MUTE}}$ OUT timing. No pull-up resistor is provided.

Timing Diagram



Note 1: PPP is a pre-pulsing pause equal to 1 MAKE period.

Note 2: A mask option of $\overline{\text{MUTE}}$ continuously active low during the IDP is available (TP5610, TP5615 only).

FIGURE 2

Functional Description

The timebase for this family of repertory dialers is derived from an on-chip oscillator connected as shown in *Figure 3 or 4.* In the on-hook condition, the oscillator is stopped and all keypad inputs inhibited. After going off-hook, the oscillator remains off and the keypad inputs go to a static sensing mode. Upon sensing a single key closure, the oscillator starts, and the row and column inputs are alternately scanned at a 500 Hz rate. When a key closure remains valid for the required debounce time, the key is interpreted in accordance with Table I. During manual dialing, valid digit keys are entered into the last-number-dialed register (register 0) in sequence and outpulsed at the nominal 10 pps rate. A manually dialed number may be entered rapidly and may exceed 16 digits without limit, provided no more than 15 digits remain to be outpulsed. Automatic dialing is inhibited, however, if an attempt is made to store more than 16 digits in that register. When no further digits remain to be outpulsed, the oscillator stops and key inputs return to the static sensing mode awaiting further keys or a return to the on-hook condition.

TABLE I. CONTROL SCHEME

Function	Control Sequence
Dial and store in register 0	$D_1 \ldots D_x$
No dial, store in register N only	$* \; N \; D_1 \ldots D_x$
Scratchpad	$\ldots D_x * N \; D_1 \ldots D_y$
Copy last number to register N	$\ldots D_x (\downarrow \uparrow) * N \downarrow$
Auto-dial register N	# N
Last number redial.	# 0
PBX access	$\uparrow (D_1)(D_2)$ # 0 or N

Note 1: N is a long-term storage register numbered from 1–9. D is a digit.
Note 2: $\uparrow$ indicates on-hook to off-hook, $\downarrow$ indicates off-hook to on-hook.
Note 3: Entries in brackets may be omitted.

NUMBER STORAGE

Telephone numbers are stored in 10 registers, numbered 0–9. Register contents can only be modified while off-hook. Register 0 always stores the last number which was manually dialed, and remains unchanged during automatic dialing. Numbers for long-term storage in registers 1–9 are entered by *, then N and then the telephone number, where N is the register number. Other registers can be successively modified by entering a new *, N followed by the telephone number. Once a * key is entered, no further outpulsing is possible until after an on-hook reset on the HOOKSWITCH pin. This facilitates the Scratchpad feature, whereby a number can be stored in a register without outpulsing during a conversation. The last number dialed manually is copied from register 0 to any of the long-term storage registers by entering *, N.

An attempt to store more than 16 digits in a register will set an overflow flag to inhibit automatic dialing from that register. The flag is reset following the next *, N entry to re-program that register.

DIALING

Automatic dialing of the telephone number stored in any register is initiated by entering #, then N. The keypad is then locked out until completion of outpulsing, after which further manual or automatic dialing is permitted.

For PBX applications, a 1 or 2-digit access code may be entered prior to a #, N code. These access digits overwrite the previously stored digits at the start of register 0, the last-number-dialed register. The user then waits for a second dial-tone before automatically dialing the required number. Note that if a 2-digit access code is entered followed by #, 0, register 0 is automatically dialed from location 3 onwards. Either a 1 or 2-digit access code followed by #, N, however, automatically dials register N from location 1 onwards. This allows the most flexible use of registers 1–9. Thus, it is not necessary to store access codes in registers 1–9, either manually or by copying the last number dialed.

Applications Information

The TP5600 and TP5605 PULSE output is designed to drive a pulsing loop circuit in shunt with the speech network, as shown in *Figure 3.* During outpulsing, the MUTE circuit is turned off to isolate the speech network from the line. Q2 and Q3 conduct during MAKE periods, R1 adjusts telephone pulsing resistance. Q2 and Q3 turn off during BREAK periods, loop current is then only the supply current to the device. Q1 provides a current source of 200 μA minimum to ensure that the device will have an adequate supply voltage.

The TP5610 and TP5615 PULSE output is designed for a series pulsing loop, as shown in *Figure 4.* In this case, the MUTE circuit isolates only the receiver, so that current flows through the speech network while outpulsing MAKE periods. Q3 cuts off this current during BREAK periods.

The on-hook current required for the device to retain dat is low enough to allow this current to be drawn from tl telephone line in certain applications. In this case, it is ε visable to add an external protection zener dio specified for very low leakage, as the internal regulato turned off when the HOOKSWITCH pin goes high. A leakage decoupling capacitor should also be specifie

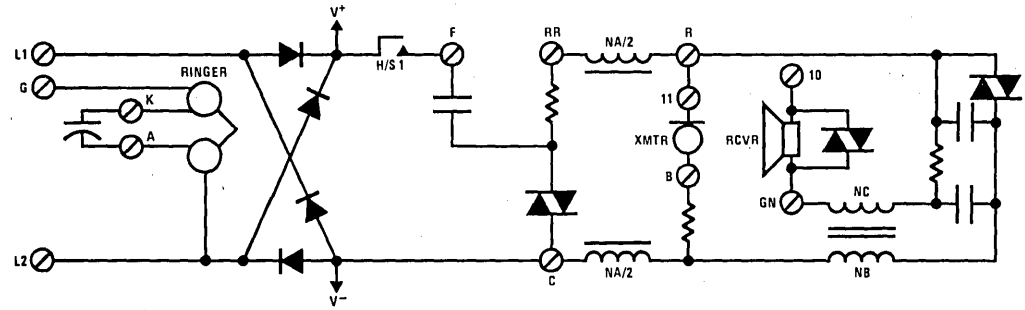
To protect stored data in the event of reduced line volt (caused by an off-hook extension telephone, for exam a small back-up battery is recommended, as show *Figures 3 and 4.* The voltage regulator is turned off in on-hook state to minimize battery current consumpti

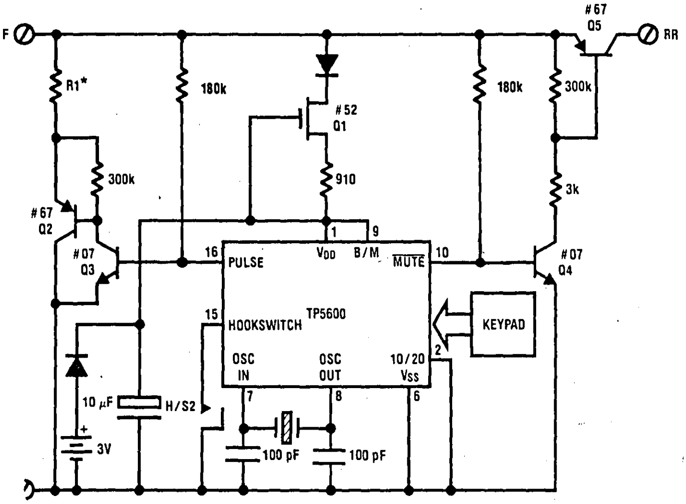
To protect the device against over-voltage during the t sition to off-hook, the HOOKSWITCH contacts shoulc sequenced so that H/S2 closes before H/S1, thus conn ing the on-chip regulator before the line power. Alter tively an external zener diode can be used.

Ceramic resonators for the TP5600, TP5610 oscillator c cuits can be obtained from various companies includin muRata, Toko, Vernitron and Radio Materials Corporation. The anti-resonant frequency, f_a, should be 480 kHz. Note that resonators are often referred to by their resonant frequency, f_r, which is typically 15 kHz–25 kHz lower than f_a. Consult manufacturers' data for specifications and tolerances.

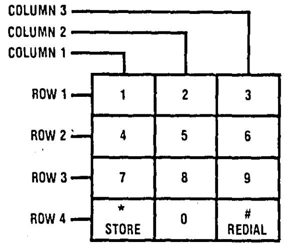
Applications Information (Continued)

Typical Speech Network





Keypad Matrix



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licates National Semiconductor Discrete process number.

FIGURE 3. TP5600 Shunt Dialer Application

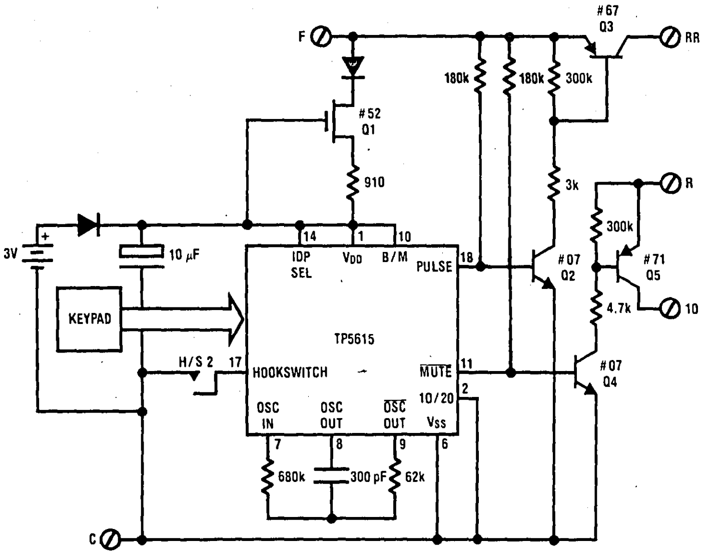


FIGURE 4. TP5615 Series Dialer Application

National Semiconductor

PRELIMINARY

TP5650, TP5660 Ten-Number Repertory DTMF Generators

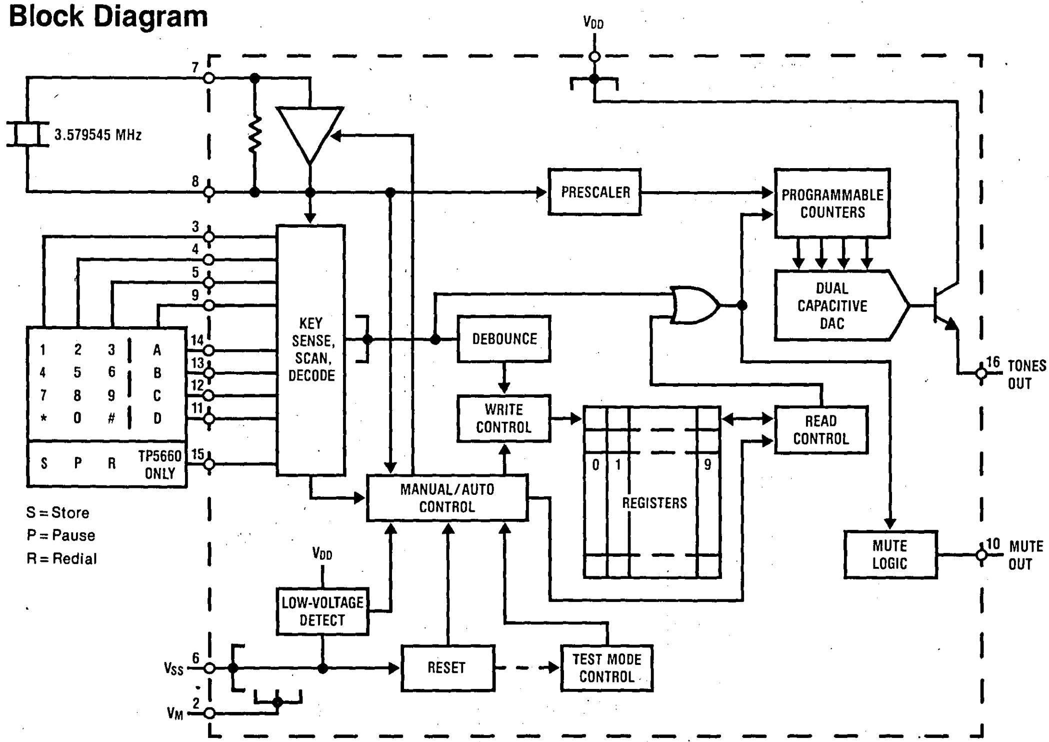
General Description

The TP5650 and TP5660 are monolithic integrated circuits built using National's advanced P²CMOS™ process (double poly-silicon gate CMOS). They interface directly to a telephone keypad and generate all 16 standard dual-tone multi-frequency pairs required in tone dialing systems. An on-chip memory provides storage for nine telephone numbers plus the last number dialed, each up to 16 digits in length. The simple control scheme needs only 2 key entries to store a number or initiate automatic dialing of a stored number. This control scheme is the same as that used on the TP5600 family of repertory pulse dialers so that no user re-education is necessary when converting from pulse to tone dialing. The tone synthesizers are locked to an inexpensive 3.579545 MHz crystal for high accuracy. A MUTE OUT logic signal, which changes state when any key is depressed, is also provided. The low voltage and low current requirements of this device allow direct telephone line powered operation. A small battery is recommended for on-hook memory retention.

Features

- 2.5V–12V operation when generating tones
- 2V operation of keyscan and MUTE logic
- 1 μA memory retention current
- Stores and auto-dials ten 16-digit numbers
- Last-number-redial included
- Scratchpad (number storage without dialing)
- TP5650 control key scheme same as TP5600 repertory pulse dialer
- TP5660 has 14 keys—separate Store, Redial, and Pause
- 2-digit overwrite for PBX access codes
- 3.579545 MHz crystal-controlled oscillator
- Low harmonic distortion
- Single-contact or negative-common (2-of-8) key inputs

Block Diagram



TL/H/5474-1

FIGURE 1

Absolute Maximum Ratings

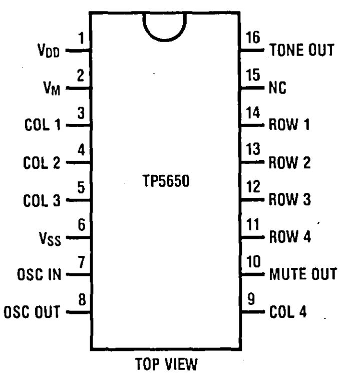
Supply Voltages ($V_{DD} - V_{SS}$) and ($V_{DD} - V_M$)	13V
Maximum Voltage at Any Other Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature (T_A)	−30°C to +60°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics 2.5V < V_{DD} < 10V, unless otherwise specified, T_A within operating temperature range

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage Swing	Generating Tones			2.5	V
Minimum Memory Retention Voltage				2	V
Supply Current, I_{DD}					
Idle	V_{DD} = 2.5V,		20		µA
Generating Tones	R_L = Open		1		mA
Battery Current, I_M	On-Hook, V_{SS} Open		2		µA
MUTE OUT Sink Current	V_{DD} = 2.5V, V_O = 0.5V	0.2			mA
MUTE OUT Source Current	V_{DD} = 2.5V, V_O = 1.5V	0.2			mA
TONE OUT Amplitudes	R_L = 100Ω				
Low Group	V_{DD} = 2.5V		175		mVrms
	V_D = 10V		190		mVrms
High Group	V_{DD} = 2.5V		225		mVrms
	V_{DD} = 10V		240		mVrms
High Group Pre-Emphasis			2		dB
Mean DC Offset at TONE OUT	Generating Tones				
	V_{DD} = 2.5V		0.7		V
	V_{DD} = 10V		4.2		V
al Tone/Total Harmonic ,tortion Ratio	1 MHz Bandwidth	20			dB
't-Up Time (to 90% Amplitude)	Manual Dialing			5	ms
ɜs-On Duration	Automatic Dialing		75		ms
ɜs-Off Duration	Automatic Dialing		75		ms
ɹmn and Row Resistors			50		kΩ

1: Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \le 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

nnection Diagrams



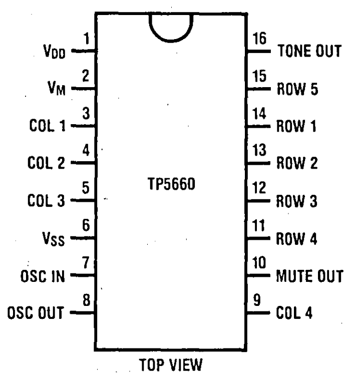


FIGURE 2

Order Number TP5650N or TP5660N
NS Package Number N16A

Pin Descriptions

V_{DD} (pin 1): The positive supply to the device, referenced to V_{SS}. A power-on reset circuit ensures correct operation following initial power-up.

V_M (pin 2): The negative terminal of the back-up battery for on-hook memory retention. A low-voltage detect circuit prevents misoperation of the circuit in the event of a reduction in the on-hook supply voltage below that required to retain stored data.

COLUMN and ROW Scans (pins 3, 4, 5, 9, 11, 12, 13, 14 plus pin 15 on TP5650 only): When no key is closed, pull-up resistors are active on COLUMN inputs and pull-down resistors are active on ROW inputs. After a key is closed the ROW pull-down resistors cause a negative-true on COLUMN inputs, which starts the oscillator and initiates tone generation.

V_{SS} (pin 6): The negative supply to the device in the off-hook state. An open-circuit on this pin while back-up power is maintained on V_M will reset the circuit.

OSC IN, OSC OUT (pins 7 and 8): All logic and tone generator timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) must be connected between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when automatic tone generation is completed or there are no key closures.

MUTE OUT (pin 10): This is a CMOS output which sinks current to V_{SS} when no tones are being generated and sources current from V_{DD} when tones are being generated.

TONE OUT (pin 10): This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

Functional Description

In the on-hook state, with power maintained for memory retention, the oscillator is stopped, the output transistor is pulled off and all keypad inputs are inhibited. After going off-hook, the oscillator remains off and the key inputs go to a static sensing mode. A single key closure activates the MUTE OUTPUT and starts the oscillator and keyscan. A valid digit key sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two sine-weighted-capacitor D/A converters through a series of 28 equal-duration steps per sine-wave cycle. An on-chip voltage reference ensures good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

Key inputs which are digits for manual dialing are not debounced prior to tone generation. Keys are debounced prior to being accepted as digits to be stored or as control keys (Table II). Upon completion of a manually or automatically dialed number, the oscillator stops and key inputs return to the static sensing mode awaiting further keys or a return to the on-hook state.

TABLE I. OUTPUT FREQUENCY ACCURACY

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Out Frequency	% Deviation from Standard
LOW	ROW 1	697	694.8	−0.32
GROUP	ROW 2	770	770.1	+0.02
f_L	ROW 3	852	852.4	+0.03
	ROW 4	941	940.0	−0.11
HIGH	COL 1	1209	1206.0	−0.24
GROUP	COL 2	1336	1331.7	−0.32
f_H	COL 3	1477	1486.5	+0.64
	COL 4	1633	1639.0	+0.37

TABLE II. CONTROL SCHEME

Function	Control Sequence
Dial and Store in Register 0	$\uparrow D_1 \ldots D_x$
No Dial, Store in Register N Only	$\uparrow$ S N $D_1 \ldots D_x$
Scratchpad	$\uparrow D_1 \ldots D_x$ S N $D_1 \ldots D_y$
Copy Last Number to Register N	$\ldots D_x (\downarrow \uparrow)$ S N $\downarrow$
Auto-Dial Register N	$\uparrow$ R N
Last Number Redial	$\uparrow$ R 0
PBX Access	$\uparrow (D_1) (D_2)$ R 0 or N
* Tones	* (TP5660) ** (TP5650) Note 1
# Tones	# (TP5660) ## (TP5650) Note 2

Note 1: * key is also STORE key S on TP5650

Note 2: # key is also REDIAL key R on TP5650

Note 3: N is a long-term storage register numbered from 1–9

Note 4: $\uparrow$ indicates on-hook to off-hook, $\downarrow$ indicates off-hook to on-hook

Note 5: Entries in brackets may be omitted

NUMBER STORAGE

S (for store) and R (for redial) entries refer to TP5660 c * is shown in brackets to replace S and # is show brackets to replace R on the TP5650 only.

Telephone numbers are stored in 10 registers, numb 0–9. Register 0 always stores the last number which manually dialed, and remains unchanged during . matic dialing. Register contents can only be mod while off-hook.

Numbers are stored in long-term registers 1–9 by ent S (*), then N and then the telephone number, where the register number. Other registers can be succes modified by entering a new S (*), N, followed by the phone number. Once an S (*) key is entered, no fu digit tone outputs are possible until after an on-hook This facilitates the Scratchpad feature, whereby a nu can be stored in a register without tone outputs du conversation. The last number dialed manually ca copied from register 0 to any of the long-term stc registers by entering S (*), N, then going on-hook.

An attempt to store more than 16 digits in a register wil an overflow flag to inhibit automatic dialing from t register. The flag is reset following the next S (*), N entry re-program that register.

DIALING

In the manual dialing mode (i.e., direct dialing from the keypad), tone pairs are generated for the duration of a valid key closure.

Automatic dialing of the number stored in register N is initiated by entering R (#) followed by N. The correct tone

Functional Description (Continued)

pairs are generated in alternate bursts of tones-on, tones-off until the end of the stored number. During this time, the keypad is locked out until completion of dialing, following which further manual or automatic dialing is permitted.

For PBX applications a 1 or 2-digit access code may be entered prior to the R (#), N code. These access digits overwrite the previously-stored digits at the start of register 0, the last-number-dialed register. The user then waits for a second dial tone before entering R (#), N to automatically dial the stored number.

Note that if a 2-digit access code is entered followed by R (#), 0, register 0 is automatically dialed from location 3 onwards. Entering either a 1 or 2-digit access code followed by R (#), N, automatically dials register N from location 1 onwards. This allows the most flexible use of registers 1-9. Note that access codes should not be entered into registers 1-9, either manually or by copying the last number dialed.

PAUSE

This key (on the TP5660 only) allows the user to enter a pause at a point in the dialing sequence where an outside dial tone from a PABX is required. A pause may be entered in any register either during manual dialing or scratchpad storage. Then, during automatic dialing of that number, the stored pause will halt dialing. On hearing the outside dial tone the REDIAL key must be entered to continue automatic dialing.

Applications Information

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sinewave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion, while increasing the source impedance of the device as seen from its power supply terminal. Note that the DTMF generator is a current source which modulates its own supply terminals in a conventional telephone application.

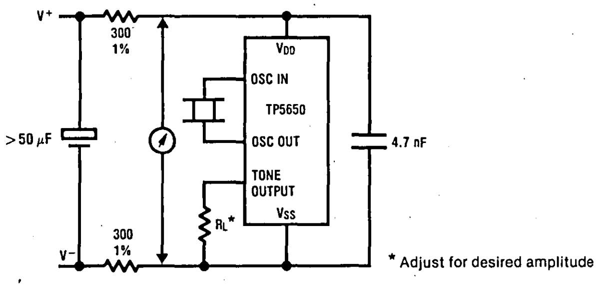


FIGURE 3. Amplitude and Distortion Measurement Circuit

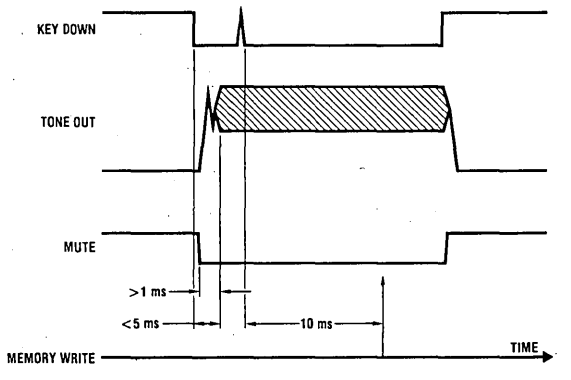


FIGURE 4a. Manual Timing

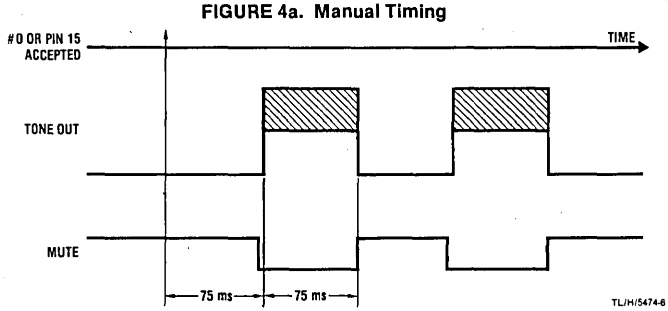
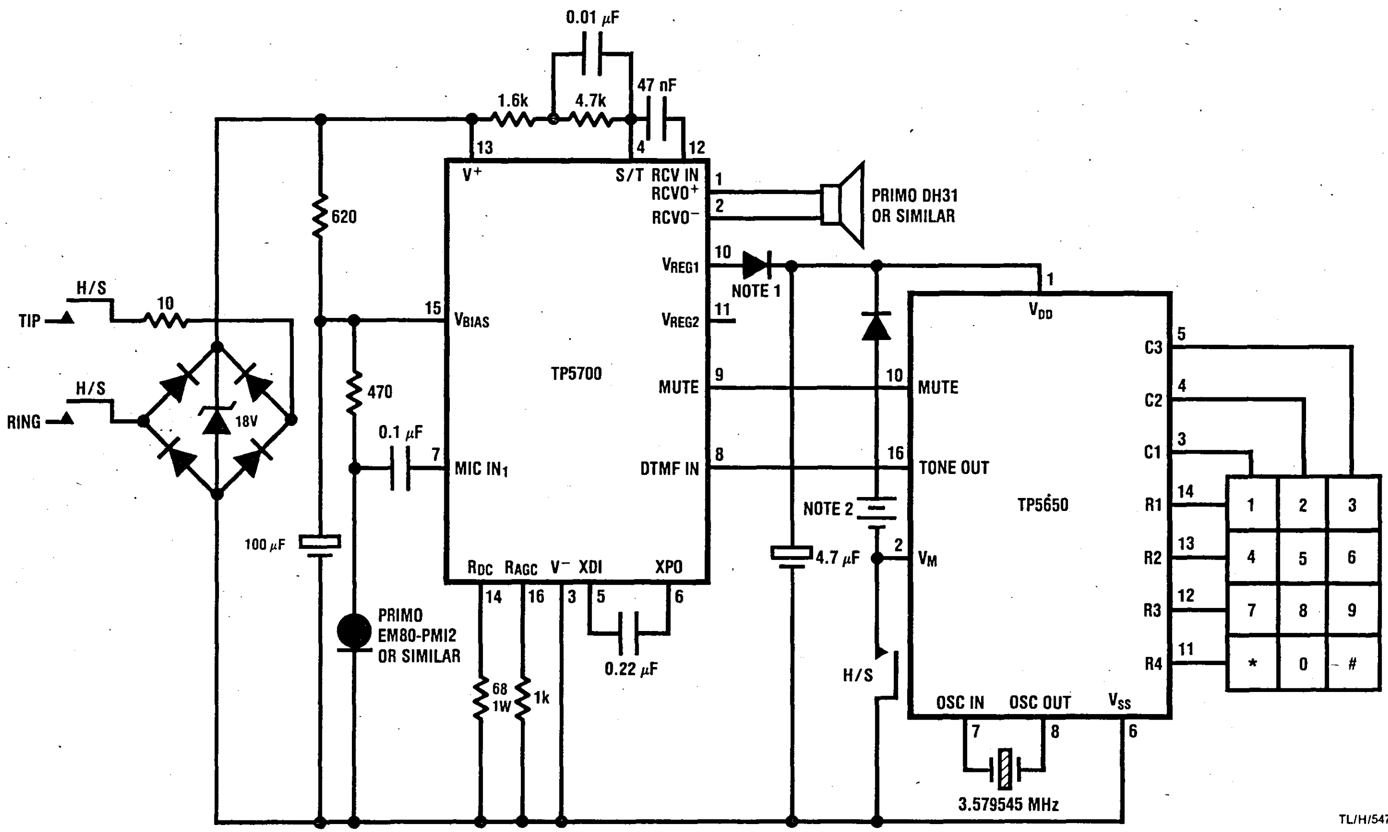


FIGURE 4b. Auto-Redial Timing

Typical Application TP5650



TL/H/5474-7

Note 1: Must be low voltage drop diode (e.g., Schottky).

Note 2: 2.7V-3.1V.

TP5700 Telephone Speech Circuit

National Semiconductor

TP50981/TP50981A, TP50982/TP50982A, TP50985/TP50985A Push Button Pulse Dialer Circuits

General Description

This family of monolithic CMOS circuits provides all logic necessary to convert keyboard inputs into a series of pulses simulating rotary telephone dialing. An on-chip memory capable of storing up to 17 digits allows keyboard entries to be made at rates comparable to those of tone-dialing telephones and provides one-key redial of the last number dialed. The keyboard inputs interface directly to a standard 2-of-7 keypad with positive-common or an inexpensive form A-type keyboard. Two outputs, one for pulsing the telephone line and one to mute the receiver, are provided along with pin selectable Break/Make ratios and an on-chip voltage regulator. The low voltage and low current requirements of these devices allow direct telephone line powered operation.

Features

- TP50981/TP50981A, TP50985/TP50985A for pulsing loop in shunt with speech network
- TP50982/TP50982A for pulsing loop in series with speech network
- 1.7V, 150 µA operation TP50981A, TP50982A and TP50985A
- Single-contact or positive-common key inputs
- Break/Make ratio pin selectable
- On-chip voltage regulator
- On-chip oscillator using 480 kHz ceramic resonator
- Scratchpad (new number storage without dialing) on TP50985/TP50985A
- 10/20 pps option on TP50985/TP50985A

Block Diagram

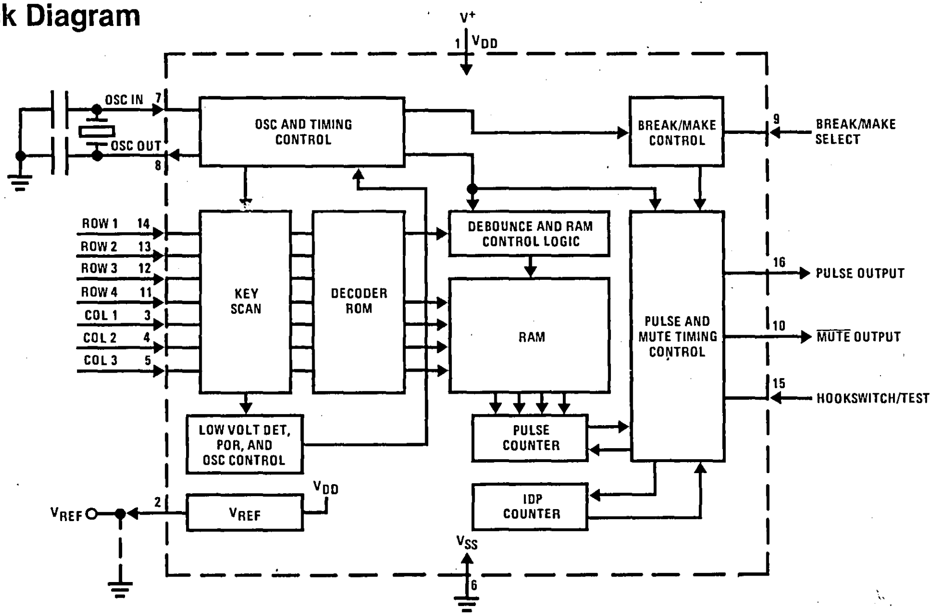
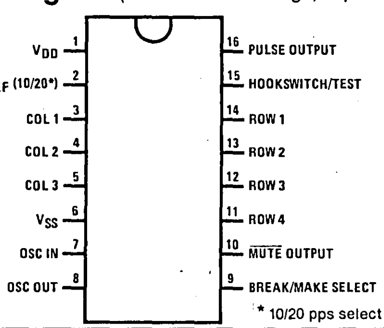


FIGURE 1

Connection Diagram (Dual-In-Line Package, Top View)



* 10/20 pps select input on TP50985/TP50985A

Order Number TP50981N, TP50981AN, TP50982N, TP50982AN, TP50985N or TP50985AN
See NS Package N16A

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}-V_{SS})	6.0V
Voltage on Any Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation (25°C)	500 mW

DC Electrical Characteristics

T_A within operating temperature range, V_{DD} min ≤ V_{DD} ≤ 5.0V, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Min DC Supply Voltage					
TP50981, TP50982, TP50985	Pin 1 Ref. Pin 6	2.5			V
TP50981A, TP50982A, TP50985A		1.7			V
Memory Retention Current	V_{DD} = 1.7V, Notes 1 and 2		0.5	1.0	μA
DC Operating Current	Off-Hook, Valid Key, V_{REF} Tied to V_{SS}		100	150	μA
V_{REF} Sink Current	V_{DD} = 5.0V	1.0			mA
$\overline{\text{MUTE}}$ Sink Current	V_{DD} = V_{DD} Min, V_o = 0.5V	0.5	2.0		mA
PULSE Sink Current	V_{DD} = V_{DD} Min, V_o = 0.5V	1.0	4.0		mA
$\overline{\text{MUTE}}$ and PULSE Leakage	V_{DD} = 5.0V, V_O = 5.0V		0.001	1.0	μA
Keyboard Contact Resistance				1.0	kΩ
Keyboard Capacitance				30	pF
Logic '0' Level Input		V_{SS}		0.2 V_{DD}	V
Logic '1' Level Input		0.8 V_{DD}		V_{DD}	V
Keyboard Pull-Up Resistance			4.0		kΩ
Keyboard Pull-Down Resistance			100		kΩ
HOOKSWITCH Pull-Up Resistance			100		kΩ

Note 1: On-hook mode, V_{REF} tied to V_{SS}, all outputs open.

Note 2: Power-on reset and low-voltage-detect circuits inhibit the redial function if the supply voltage falls below V_{DD} Min.

AC Electrical Characteristics

T_A within operating temperature range, V_{DD} min ≤ V_{DD} ≤ 5.0V, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	Anti-Resonant Mode		480		kHz
Keyboard Debounce Time	OSC IN = 480 kHz	9		11	ms
Oscillator Start-Up Time	V_{DD} = V_{DD} Min		5.0		ms
Pulse Rate			10.0		pps
Break Time	Pin 9 @ V_{DD}		61.0		ms
	Pin 9 @ V_{SS}		67.0		ms
Interdigit Pause			800		ms

Functional Description

The time base for this family of pulse dialers is derived from a 480 kHz ceramic resonator in anti-resonant mode. In the on-hook condition, the oscillator is stopped and all keyboard row and column inputs are forced to V_{DD} which inhibits any key closures from effecting the circuit. After going off-hook the oscillator remains off and the keyboard inputs go to a static sensing mode. Upon sensing a single key closure, the oscillator starts, and the row and column inputs are alternately scanned at a 500 Hz rate. When the circuit senses a valid key closure for the required debounce time, the key is written into memory and outpulsing begins for that key. Further valid keys are entered in sequence, provided that no more than 17 digits remain to be outpulsed. If no further key is entered, following the IDP the oscillator will stop and the key inputs will return to the static sensing mode awaiting further keys or a return to the on-hook condition. By maintaining power to the device while on-hook, the last number dialed (up to 17 digits) is stored in the memory. On going off-hook (HOOKSWITCH goes to V_{SS}) the stored number can be automatically redialed by entering either * or # as the first key (TP50981/TP50981A and TP50982/TP50982A). Entry of any digit as the first key following off-hook clears the redial memory and enters digits in sequence, starting at location 1.

The * key on the TP50985/TP50985A is redefined to provide entry to the Scratchpad feature. This mode allows the outpulsing memory to be overwritten with a new telephone number without that number being outpulsed. Scratchpad mode can be entered directly after going ff-hook or during a conversation by keying * followed by) next desired number. The new number can only be out- lsed by returning on-hook, then off-hook followed by the ey, which will redial the last number as normal.

TP50985/TP50985A also enables the user to select an)ut pulse rate of either 10 pps by connecting pin 2 to ınd or 20 pps by connecting pin 2 to V_{DD}. On this ver- V_{REF} is connected to V_{SS} internally.

Descriptions

)in 1): This is the positive supply to the device and is ›nced to V_{SS} (pin 6). The voltage on this pin must be d to less than 6V either externally or by current- ıg the supply to the on-chip voltage regulator. In the umber-stored mode a minimum of 1 μA of supply cur- ..ıı must be available to this pin while on-hook.

V_{REF} (pin 2): In normal applications, this pin is tied to V_{SS} (pin 6) which enables the on-chip voltage regulator circuit. When V_{REF} is tied to V_{SS}, the voltage regulator will provide a current sink from V_{DD} to V_{SS} of a minimum of 1 mA with V_{DD} equal to 5V.

KEYBOARD INPUTS (pins 3, 4, 5, 11, 12, 13, and 14): A valid key entry is defined as either connecting a single row to a single column or connecting V_{DD} simultaneously to a single row and a single column. This allows direct interface to an inexpensive single-contact (form A) keyboard, the standard 2-of-7 keyboard with positive-common, or logic-generated inputs.

In the on-hook condition [HOOKSWITCH/TEST (pin 15) connected to V_{DD}] the keyboard inputs are disabled and pulled high. Upon entering the off-hook condition the keyboard inputs go to a static sensing mode until a key closure is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. The key must then remain valid continuously for the specified debounce time before the circuit will accept and decode it and begin outpulsing.

V_{SS} (pin 6): This is the negative supply.

OSCILLATOR IN, OUT (pins 7, 8): The device contains an on-chip oscillator circuit designed to work with a 480 kHz ceramic resonator (anti-resonant mode) and 2 external capacitors, normally 100 pF. A 1 MΩ resistor is included on-chip for good oscillator stability. The circuit may also be driven with an external 480 kHz source on OSCILLATOR IN (pin 7).

BREAK/MAKE SELECT (pin 9): The Break/Make ratio is selected by connecting pin 9 to either V_{DD} or V_{SS}. Table I indicates the available ratios.

TABLE I. BREAK/MAKE SELECT

Input to BREAK/MAKE (pin 9)	PULSE OUTPUT Break	Make
V_{DD}	61%	39%
V_{SS}	67%	33%

$\overline{\text{MUTE}}$ (pin 10): This pin is the output of an open-drain N-channel transistor. It drives a simple interface circuit to mute the receiver during outpulsing. See the timing diagram and application notes for further information concerning this output.

HOOKSWITCH/TEST (pin 15): This input has a 100 kΩ internal pull-up resistor to V_{DD}. Allowing this pin to float, or connecting a V_{DD} level puts the circuit in the on-hook idle mode.

With this pin connected to V_{SS} the circuit is in the off-hook mode and will accept keyboard inputs, and outpulse them at the normal 10 pps rate. When the outpulsing is complete, the oscillator stops and waits for further key inputs. If, however, pin 15 is taken to V_{DD} while the circuit is still outpulsing the remaining digits will be outpulsed at 100 times the normal rate (BREAK/MAKE becomes 50%). This allows for rapid testing of the device and also provides a means for resetting the circuit if power to the device is maintained while on-hook. (Note: Taking the worst-case of 17 zeros remaining to be outpulsed, this operation could take 300 ms to complete. Therefore, to ensure that the circuit has been properly reset, pin 15 should remain at V_{DD} for more than 300 ms before entering a new number.)

PULSE OUTPUT (pin 16): The pulse output consists of an open-drain N-channel transistor. It is intended to drive a transistor interface circuit to pulse the telephone line with the correct Break/Make ratio, IDP timing, and pulse rate. On the TP50981/TP50981A, TP50985/TP50985A this output is normally low and pulses high. On the TP50982/TP50982A the output is normally high and pulses low. See *Figure 2* for further details of the timing differences between the parts.

Timing Diagram

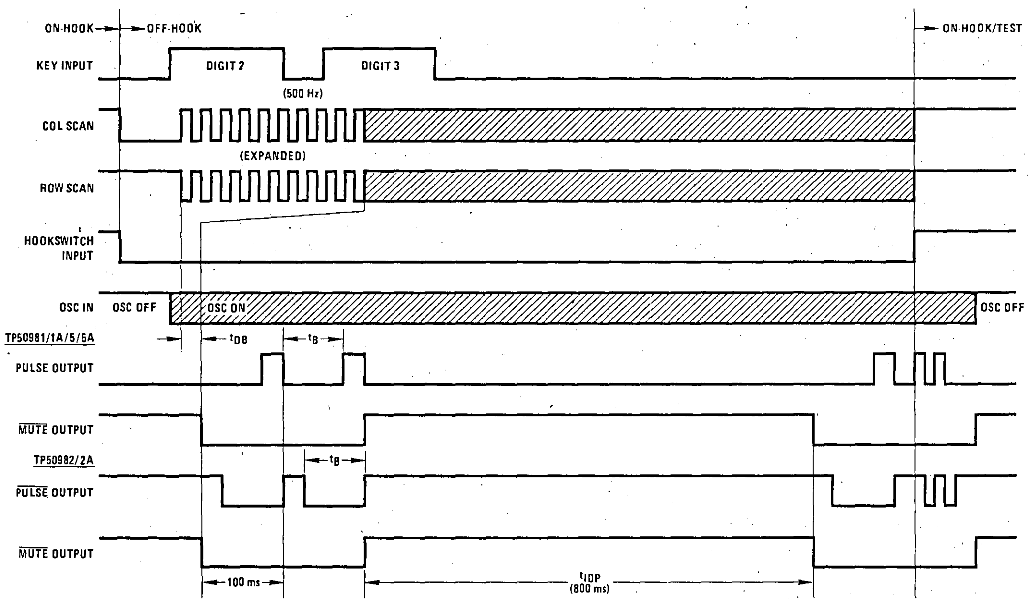


FIGURE 2

Applications Information

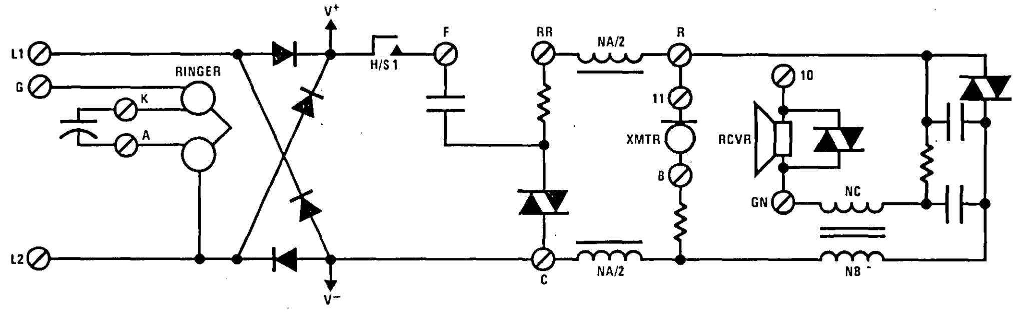
The TP50981/TP50981A, TP50985/TP50985A PULSE output is designed to drive a pulsing loop circuit in shunt with the speech network, as shown in *Figure 3.* During outpulsing the MUTE circuit is turned off to isolate the speech network from the line. VT2 and VT3 conduct during MAKE periods, R1 adjusts telephone pulsing resistance. VT2 and VT3 turn off during BREAK periods, loop current is then the sum of the device supply current, plus R2 and R3 currents. These currents should be designed to meet the system maximum BREAK current specification, where applicable. The on-chip voltage regulator enables the device to be fed from a current-limited supply of 150 μA minimum, as shown in *Figure 3.*

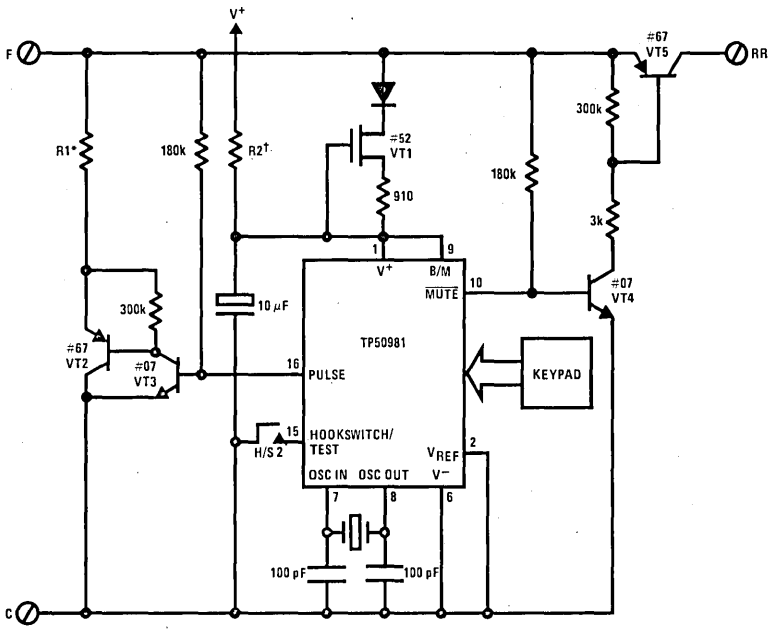
The TP50982/TP50982A PULSE output is designed for a series pulsing loop, as shown in *Figure 4.* In this case the MUTE circuit isolates only the receiver, so that current flows through the speech network while outpulsing MAKE periods. VT3 cuts off this current during BREAK periods.

To take maximum advantage of the low current consumption of the TP50981A, TP50982A, TP50985A in the on-hook, last-number-stored mode, all other current paths must be minimized. These include leakage of the decoupling capacitor C1, and reverse leakage of current through the current source, which could flow to ground via the transistor interface circuits and speech network. If on-hook current is drawn from the telephone line, reverse leakage of the two back-biased diodes in the rectifier bridge must also be considered. Virtually the full station battery voltage may appear across these diodes in the on-hook condition of *Figures 3 and 4,* hence the diodes should be specified for minimum leakage current at 50V reverse bias and maximum operating temperature.

Ceramic resonators for the oscillator circuit can be obtained from various companies including muRata, Toko, Vernitron and Radio Materials Corporation. The anti-resonant frequency, f_a, should be 480 kHz. Note that resonators are often referred to by their resonant frequency, f_r, which is typically 15 kHz–25 kHz lower than f_a. Consult manufacturers' data for specifications and tolerances.

Applications Information (Continued)





*R1 typically 150Ω.
†R2 = 20M for TP50981, TP50985; R2 = 50M for TP50981A, TP50985A.
# indicates National Semiconductor Discrete process number.

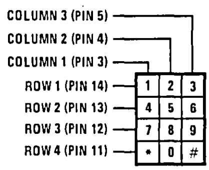
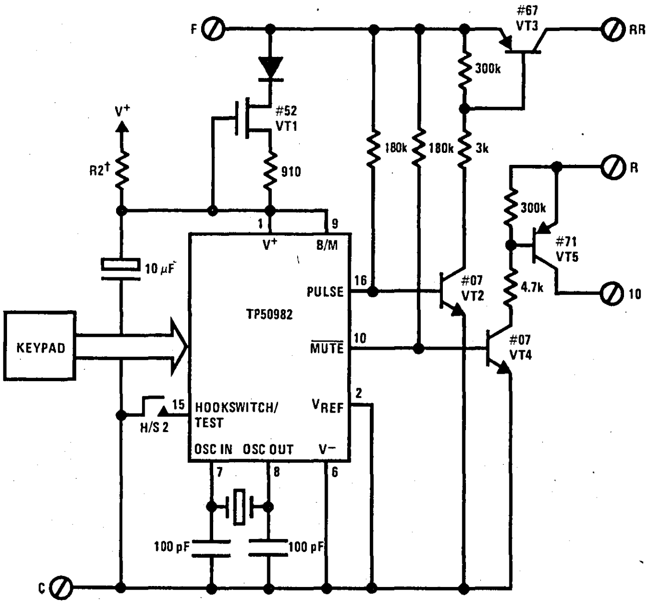


FIGURE 3. TP50981, TP50985 Shunt Dialer Application

Applications Information (Continued)



†R2 = 20M for TP50982, R2 = 50M for TP50982A

FIGURE 4. TP50982 Series Dialer Application

National Semiconductor

TP53130 DTMF (TOUCH TONE®) Generator with Binary Data and Keypad Interface

General Description

The TP53130 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that generates all dual tone multi-frequency (DTMF) pairs required in tone-dialing systems. The 8 audio output frequencies are generated from an on-chip 3.579545 MHz master oscillator. No external components other than the crystal are required for the oscillator. The TP53130 can be powered directly from telephone lines over wide range loop conditions. The device can interface directly to an inexpensive single-contact calculator type keyboard or a standard telephone 2-of-8 keypad *(Figure 4)*. The TP53130 is also capable of accepting binary code inputs for micro-processor-controlled systems applications.

Features

- 3V–15V operating voltage
- On-chip 3.579545 MHz crystal-controlled oscillator
- Tone accuracy better than ±1% without tuning
- Interface with standard 2-of-8 telephone keypad
- Interface with single-contact low cost keypad
- Input signals can be in binary code
- Multi-key lockout with/without single tone capability
- On-chip high band and low band tone generators and mixer
- High band pre-emphasis
- Low harmonic distortion
- Open emitter-follower low impedance output
- Separate receiver mute and transmitter mute switch outputs
- Powered directly from the telephone line

Block Diagram

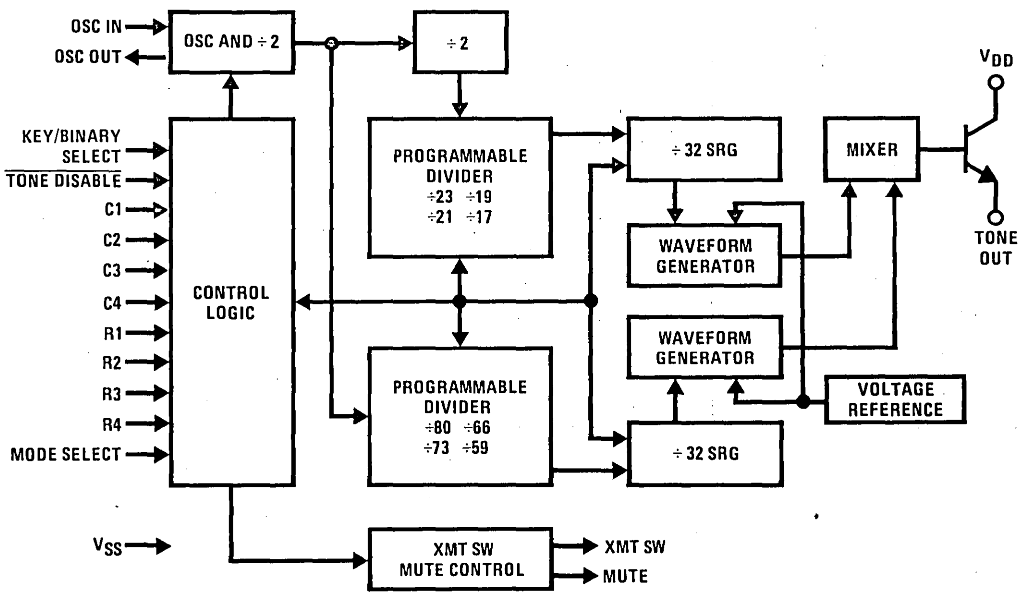


FIGURE 1

Absolute Maximum Ratings

Voltage at Any Pin Except XMT SW and MUTE	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Voltage at XMT SW and MUTE Pins	$V_{SS}-0.3V$ to 15V
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−65°C to +150°C
V_{DD}-V_{SS}	15V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating temperature range, $3V \leq V_{DD} \leq 8V$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Pull-Up Resistor					
Column and Row Inputs		25	50	90	kΩ
Key/Binary Select		200	650	1000	kΩ
$\overline{\text{Mode Select}}$		200	650	1000	kΩ
Tone Disable		200	650	1000	kΩ
Input Pull-Down Resistor					
Column and Row Inputs	$V_{DD}=3V$	650			Ω
	$V_{DD}=8V$	200			Ω
Input Voltage Levels					
Logical "1"		80% of V_{DD}		V_{DD}	V
Logical "0"		V_{SS}		20% of V_{DD}	V
Operating Frequency			3.579545		MHz
Output Voltage Swing at Tone Output					
Low Band Alone	$R_L > 150\Omega$		820		mVp-
High Band Alone	$R_L > 150\Omega$		1000		mVp
Harmonic Distortion	$R_L > 150\Omega$			−20	dB
Tone Frequency Deviation				1.0	%
Typical Application Output Level V_L (See *Figure 5*)	$20 < I_L < 100$ mA				
Low Band Tone	$R_L = 150\Omega$		−6		d
High Band Tone	$R_L = 150\Omega$		−4		d
THD	$f \leq 20$ kHz		4		[illegible]
Output Currents	$V_{DD}=3V$				
XMT SW/MUTE	$V_{OUT}=2V$	3			r
Idle Current	$R_L=\infty$, $V_{DD}=8.0V$ (No Key Depressed)			1	r
Operating Current	$R_L=\infty$, $V_{DD}=3.5V$			2	[illegible]
Key Down to Tone Outputting Time (Debounce)			3	4	ms
DC Output	Tone Disable = 0		TRI-STATE®		

Connection Diagram

Dual-In-Line Package

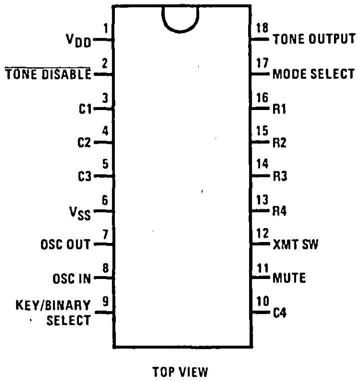


FIGURE 2

Order Number TP53130N
See NS Package N18A

Functional Description

A functional block diagram of the TP53130 is shown in *Figure 1*, and connection diagram is shown in *Figure 2*. The TP53130 can be operated in the Keyboard Interface Mode and can also be operated in the Binary Interface Mode depending on the logic level at the Key/Binary Select input. In either mode, the device will digitally synthesize the high and low band sine waves of DTMF signaling, when valid signals are applied to row and/or column inputs. The sum of the two sine waves is then provided at the Tone output.

Tone Disable: This input has an internal pull-up resistor. When this input is open or at logical high (V_{DD}), the XMT SW and MUTE outputs will deliver valid output signals in response to the proper input signals. When Tone Disable at logical low (V_{SS}), the device will be in the inactive mode. ne output will go to an open circuit state, XMT SW and)TE outputs will sink current through on-chip N-channel vices and the crystal oscillator will be disabled.

/Binary Select: When this input is open or at logical h (V_{DD}), the device will interface a keyboard. (See Table I.) en Key/Binary Select is low (V_{SS}), the device will accept ry inputs on the row signal input lines. (See Table II.)

cillator: Tone generation and internal timing are dependent on the accurate operation of the crystal oscillator. The oscillator inverter/amplifier and all necessary bias networks are included on-chip. The only external component is a 3.579545 MHz crystal. It should be connected to the device as shown in the typical application diagram *(Figure 5)*. The oscillator is not running unless a valid input signal is applied to the device. The oscillator is also disabled when Tone Disable is tied to logic low (V_{SS}). This feature will prevent RF modulation on the telephone line.

Single Tone Capability: This is a desirable feature for initial testing. With the device operating in the Keypad Interface Mode, operation of multiple keys in different rows and columns will not generate output tones. However, operation of two or more keys in the same row or column will generate the proper tone for that row or column. During multiple key operation, the XMT SW and MUTE outputs will not change state more than once. With the device operating in the Binary Interface Mode, a logical low at the column 1 input will inhibit the high band tone output while a logical low at the column 2 input will inhibit the low band tone output. (See Table I.) Logical low inputs on both column inputs 1 and 2 will disable the device the same way as the Tone Disable input will when set to logical low.

Mode Select: This input has an internal pull-up resistor. When open or at logical high, single tone outputs are allowed. When this input is at logical low, single tone outputs are prohibited. XMT SW and MUTE outputs will stay high during a multiple key depression input.

Tone Output: Dual-tone output frequencies are generated in response to valid input signals to the device. (See Table III.) Each frequency is synthesized with 32 steps of approximation for low harmonic distortion. The amplitudes of the low and high frequency tones are constant and independent of operating voltages. When tone outputs are present, the Tone output will be the composite of the AC signal superimposed on a DC offset. The DC offset is approximately 1/2 V_{DD}. When no tones are present at the Tone output pin, the pin will be open circuit.

XMT SW (Transmitter Switch) and MUTE Outputs: In the idle state (no key depressed, no signal interface inputs and Tone Disable at a logical low) both the XMT SW and MUTE outputs will sink current to V_{SS} through on-chip transistors. In the active state, these outputs will source current from V_{DD} whenever valid output tones are generated. The MUTE output activates before the XMT SW output as shown in *Figure 3*.

Signal Inputs (Row and Column Inputs): An input scan technique is used so that the device can directly interface either 2-of-8 keypads with common switch arrangements or the single contact X-Y keypads when Key/Binary Select is open circuit. (See *Figure 4*.)

Functional Description (Continued)

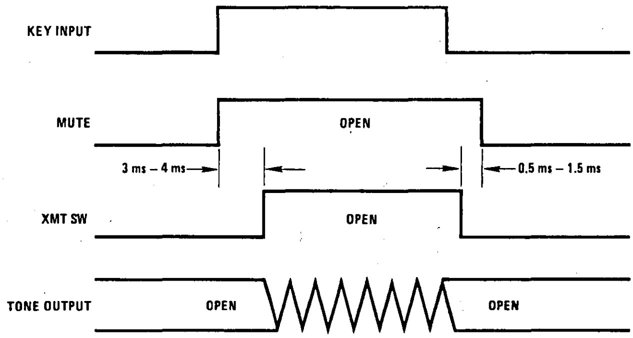


FIGURE 3. Timing Diagram of MUTE and XMT SW in Relation to Key Input and Tone Output

TABLE I. FUNCTIONAL TRUTH TABLE (WITH "MODE SELECT" OPEN)

Key/Binary Select	Tone Disable	Row	Column	Tone Output		XMT SW	MUTE
				Low Band	High Band		
X	0	X	X	0	0	0	0
1	1	One	One	f_L	f_H	1	1
1	1	One	Two or More	f_L	0	1	1
1	1	Two or More	One	0	f_H	1	1
1	1	Two or More	Two or More	0	0	0	0
0	1	Binary	Open	f_L	f_H	1	1
0	1	Binary	C1 = 0	f_L	0	1	1
0	1	Binary	C2 = 0	0	f_H	1	1
0	1	X	C1 and C2 = 0	0	0	0	0

TABLE II. FUNCTIONAL TRUTH TABLE FOR BINARY INTERFACE

Keyboard Inputs	Binary Inputs						Frequencies Generated	
	C1	C2	R1	R2	R3	R4	f_L (Hz)	f_H (Hz)
1	Open	Open	0	0	0	1	697	1209
2	Open	Open	0	0	1	0	697	1336
3	Open	Open	0	0	1	1	697	1477
4	Open	Open	0	1	0	0	770	1209
5	Open	Open	0	1	0	1	770	1336
6	Open	Open	0	1	1	0	770	1477
7	Open	Open	0	1	1	1	852	1209
8	Open	Open	1	0	0	0	852	1336
9	Open	Open	1	0	0	1	852	1477
0	Open	Open	1	0	1	0	941	1336
*	Open	Open	1	0	1	1	941	1209
#	Open	Open	1	1	0	0	941	1477
A	Open	Open	1	1	0	1	697	1633
B	Open	Open	1	1	1	0	770	1633
C	Open	Open	1	1	1	1	852	1633
D	Open	Open	0	0	0	0	941	1633
	0	Open	Valid				f_L	—
	Open	0	Binary				—	f_H
	0	0	Inputs				1/2 V_{DD}	1/2 V_{DD}

Functional Description (Continued)

TABLE III. OUTPUT FREQUENCIES

Inputs	Desired Freq. (Hz)		Actual Frequency (Hz)	Percent Deviation
	f_L	f_H		
R1	697		699.1	0.306
R2	770		766.2	−0.497
R3	852		847.4	−0.536
R4	941		948.0	0.741
C1		1209	1215.9	0.569
C2		1336	1331.7	−0.324
C3		1477	1471.9	−0.35
C4		1633	1645.0	0.736

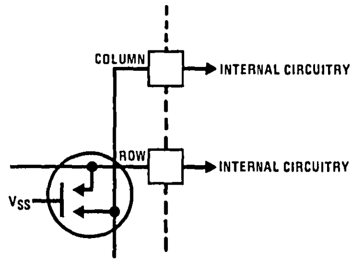


FIGURE 4a. Standard Dual Contact Telephone Key

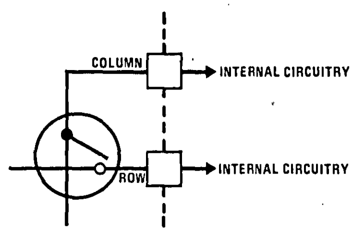
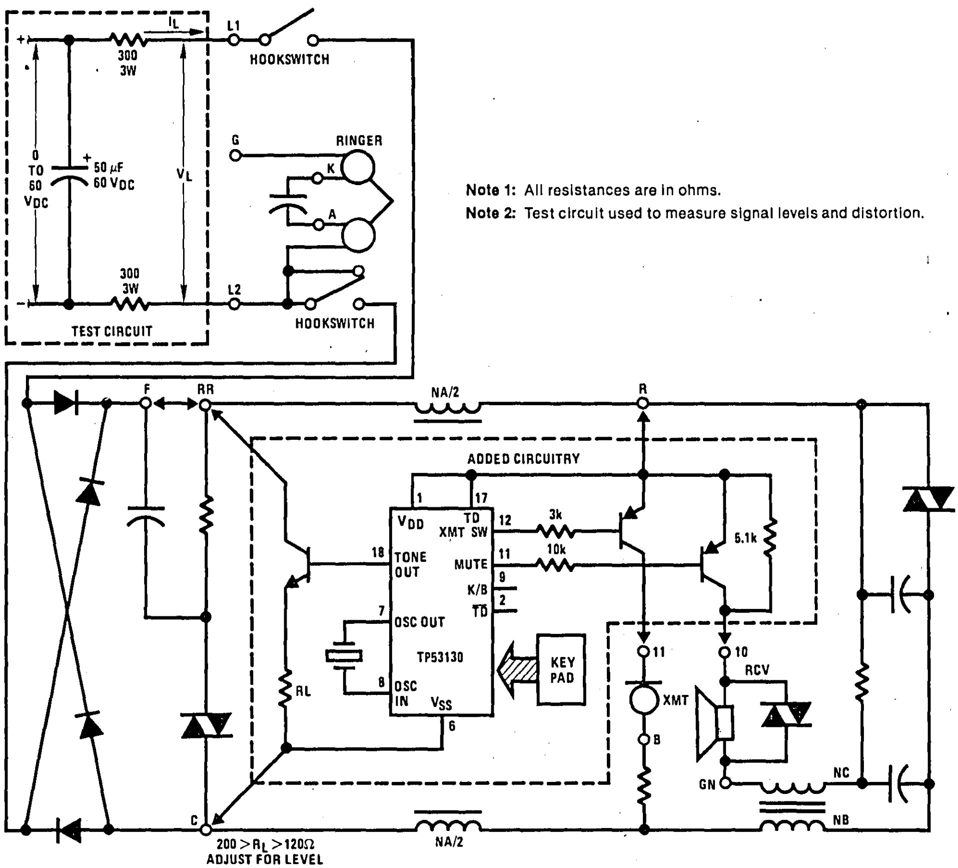


FIGURE 4b. Single Contact Key

Typical Application



Note 1: All resistances are in ohms.

Note 2: Test circuit used to measure signal levels and distortion.

FIGURE 5

National Semiconductor

TP53190 Push-Button Pulse Dialer

General Description

The TP53190 is a low threshold voltage, ion implanted, metal-gate CMOS integrated circuit that provides all the logic required to convert a push-button input into a series of pulses suitable for simulating a telephone rotary dial. The circuit works with both calculator type keypad (single-contact) or standard 2-of-7 type keypad. An inexpensive ceramic resonator is used as a frequency reference. When not actually outpulsing, or if there are no keypad entries, the TP53190 consumes only microamperes of current and does not allow any internal oscillators to run.

The TP53190 contains a 16-digit first-in—first-out memory that allows the user to enter digits faster than they are outpulsed. Numbers up to 16 digits may be dialed. After 16 digits have been entered, no more entries will be accepted. The outpulsing rate can be externally selected as either 10 pps or 20 pps. An interdigit pause of 4, 6, 8 or 10 times the dial pulse period is also externally selectable. The break/make ratio (ratio of the time the line is broken to the time the line is looped during outpulsing) is externally selectable to 1/1, 1.5/1, 1.6/1 or 2/1. A mute output is provided to mute receiver noise during outpulsing. No muting occurs during the inter-digit pause, thereby allowing the user to hear any busy or invalid condition arising during the call. The TP53190 provides a pacifier tone of 632 Hz every time a key is depressed. The last number entered may be redialed by use of the # key.

Features

- Powered directly from the telephone line
- Uses standard calculator type keypad or 2-of-7 type keypad
- Uses inexpensive ceramic resonator for a frequency reference
- Pin-selectable outpulsing rate
- Pin-selectable interdigit pause
- Pin-selectable break/make ratio
- 632 Hz pacifier tone
- Redial of last number
- 2 digit overwrite for PABX access

Block and Connection Diagrams

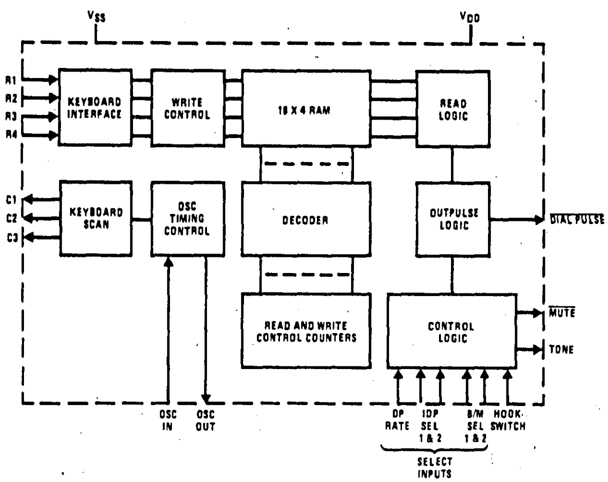


FIGURE 1

Dual-In-Line Package

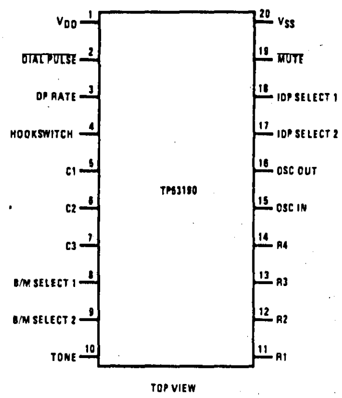


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FIGURE 2

Order Number TP53190
See NS Package N20A

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS}-0.3$ to $V_{DD}+0.3V$
Current into $\overline{DP}$ for Voltages Exceeding V_{DD}	$\leq 500\ \mu A$
Operating Temperature Range	−30°C to +70°C
Storage Temperature Range	−40°C to +70°C
$V_{DD}-V_{SS}$	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Voltage Range

V_{SS} = GND, V_{DD} = 2.5V min, 5.5V max

Electrical Characteristics

V_{SS} = GND, $2.5V \leq V_{DD} \leq 5.5V$, $-30°C \leq T_A \leq +70°C$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Output Current Levels:					
$\overline{\text{Dial Pulse}}$					
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=0.7V$	500			μA
$\overline{\text{Mute}}$					
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=0.7V$	500			μA
Tone					
Logical "1"	$V_{DD}=3V$, $V_{OUT}=2.75V$	4			μA
Logical "0"	$V_{DD}=3V$, $V_{OUT}=0.25V$	4			μA
C1—C3					
Logical "1"	$V_{DD}=3V$, $V_{OUT}=2.75V$	1			μA
Logical "0"	$V_{DD}=3V$, $V_{OUT}=0.25V$	18			μA
Keypad Resistance				1	kΩ
Operating Current	$V_{DD}=3V$				
	Quiescent			1	μA
	Oscillating			300	μA
Outpulsing Frequency	Osc = 488 kHz	9.5		10.5	Hz
Input Leakages:					
Pins 3, 8, 9, 17, 18	$V_{DD}=5.5V$, $V_{IN}=V_{SS}$			5	μA
Pins 11, 12, 13, 14	$V_{DD}=5.5V$, $V_{IN}=V_{SS}$			30	μA
Pin 4 (Hookswitch)	$V_{DD}=5.5V$, $V_{IN}=V_{SS}$			1	μA
Pins 3, 8, 9, 17, 18	$V_{DD}=5.5V$, $V_{IN}=V_{DD}$			1	μA
Pins 11, 12, 13, 14	$V_{DD}=5.5V$, $V_{IN}=V_{DD}$			1	μA
Pin 4 (Hookswitch)	$V_{DD}=5.5V$, $V_{IN}=V_{DD}$			5	μA

Functional Description

A block diagram of the TP53190 integrated circuit is shown in *Figure 1* and a package connection diagram is shown in *Figure 2.*

Oscillator (Pins 15 and 16): The precision time base of the TP53190 pulse dialer is provided by an internal oscillator circuit which utilizes an inexpensive ceramic resonator as a frequency reference. Two external capacitors, as shown in *Figure 3*, are needed to load the resonator to operate in the anti-resonant mode. A 455 kHz series resonance ceramic resonator will result in a frequency of oscillation of 480 kHz. Ceramic resonators are available from Vernitron Corporation, Murata Corporation, and Radio Materials Company. Frequency stability of ±5% can be maintained for all devices over the voltage and temperature ranges. When the circuit is not outpulsing, or no keys are depressed, the oscillator will be shut down to eliminate noise and minimize dissipation.

Keypad (Pins 5–7 and 11–14): Three column scan output pins and four row input pins are provided to utilize a standard single-contact keypad or 2-of-7 type keypad (*Figure 4).* A valid key closure is recorded when a single row (R_X input) is connected to a single column (C_X output) or when a single row and a single column are brought to V_{SS}. Key closures are protected from contact bounce for 6 ms. Roll-over keyboard inputs will be considered valid.

5

Functional Description (Continued)

Dial Pulse Output (Pin 2): The Dial Pulse output drives an external bipolar transistor that sequentially opens (breaks) the telephone loop a number of times equal to the input digit selected. For example, key 5 will generate 5 loop current breaks. The Dial Pulse output is an open drain transistor that sinks current only during a break.

Break/Make Select (Pins 8–9): The break/make ratio of the TP53190 can be externally selected by the 2 break/make select pins to be 1/1, 1.5/1, 1.6/1 or 2/1. This allows applications in a wide variety of telephone systems (Table I).

DP Rate Select (Pin 3): The dial pulse rate select input is used to select an outpulsing rate of either 10 pps or 20 pps (Table II).

IDP Select (Pins 17 and 18): The IDP select inputs are used to select an interdigit separation of 400 ms, 600 ms, 800 ms or 1000 ms when the outpulsing rate is 10 pps; and 200 ms, 300 ms, 400 ms, or 500 ms when the outpulsing rate is 20 pps (Table III)

Mute (Pin 19): The Mute output is used to drive an external bipolar transistor that is used to mute the receiver during the outpulse period. The Mute output is an open drain transistor that only sinks current while muting. System timing between key closure, mute and dial pulse are shown in the timing diagram in *Figure 5.* For initial key entries, and subsequent key entries made 1 IDP period after the last digit has been outpulsed, mute will occur 1 IDP period before outpulsing begins.

For key entries made during outpulsing, or during an IDP, there will be a pre-dial mute of 100 ms when the outpulsing rate is 10 pps, and a pre-dial mute of 50 ms when the outpulsing rate is 20 pps. The post-dial mute is 50 ms when the outpulsing rate is 10 pps and 25 ms when the outpulsing rate is 20 pps.

Tone (Pin 10): The TP53190 provides a pacifier tone output to provide audio feedback to the user that a key has been depressed. The output is a 632 Hz tone that can be capacitively coupled in to the telephone receiver.

Redial: This feature allows the user to automatically dial the last number that was dialed. This is accomplished by pushing the # key on the next dial attempt. The number to be redialed may be 3 to 16 digits long. If an access code is required, as in a PBX system, up to 2 digits may be entered before the dial tone is established and the redial key is pushed to automatically dial the remainder of the number. To maintain memory information, power must be present to the part while in the ON-HOOK condition. To detect the ON-HOOK condition, the hookswitch input (pin 4) must be left floating. Hookswitch is used to reset the internal control circuitry and memory pointers. To detect the OFF-hook condition, hookswitch must be at a logical "1". An example of the redial operation is shown below.

	Key Inputs	Outpulses	Memory
First Try	85P4087375000	854087375000	854087375000
Second Try	85P#	854087375000	854087375000
Third Try	85P#	854087375000	854087375000

Note: P indicates a user pause

TABLE I

Break/Make Ratio		
B/M	**Select 1**	**Select 2**
1.5/1	0	0
2/1	0	1
1/1	1	0
1.6/1	1	1

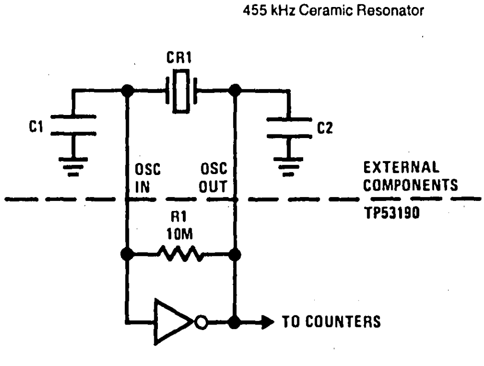
TABLE II

Dial Pulse Rate	
pps	**SELECT**
10	0
20	1

TABLE III

Interdigital Pause			
IDP Length	**Dial Pulse Rate**	**Select 1**	**Select 2**
800 ms	10 pps	0	0
400 ms	20 pps	0	0
1000 ms	10 pps	0	1
500 ms	20 pps	0	1
400 ms	10 pps	1	0
200 ms	20 pps	1	0
600 ms	10 pps	1	1
300 ms	20 pps	1	1

Functional Description (Continued)



C1 = C2 = 80 pF

FIGURE 3

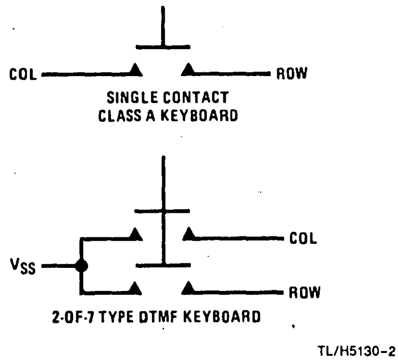
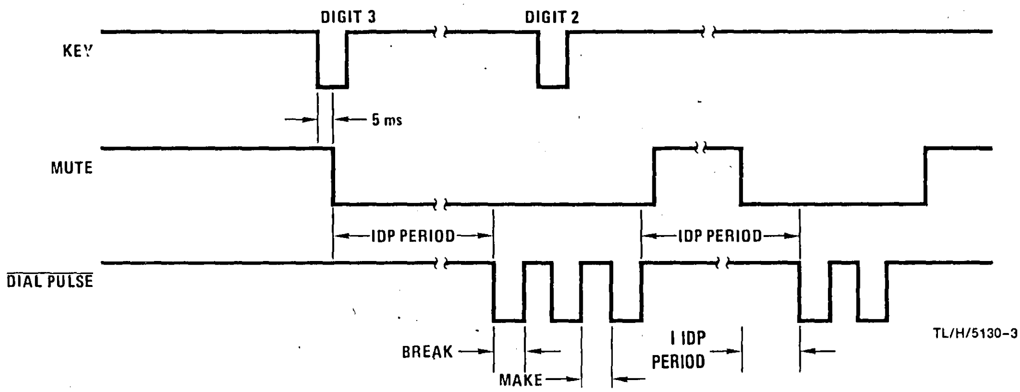
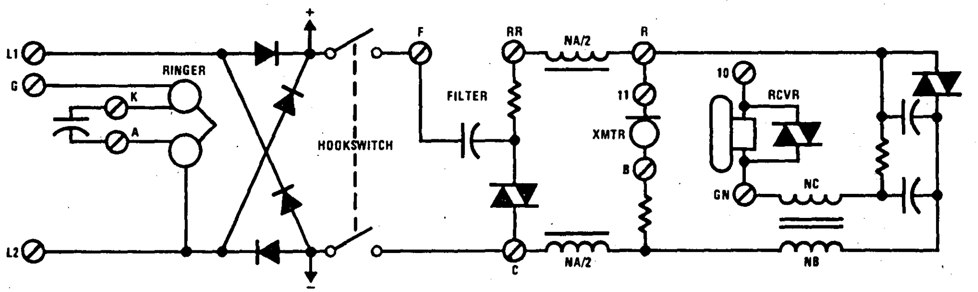


FIGURE 4

Output Timing Waveforms



Functional Description (Continued)



Note 1: All resistances in ohms and capacitances in μF unless otherwise noted.

Note 2: DP Rate, B/M and IDP select pins must be tied to the appropriate logic level for desired operation.

Note 3: Diode, bridge must be added to telephone set.

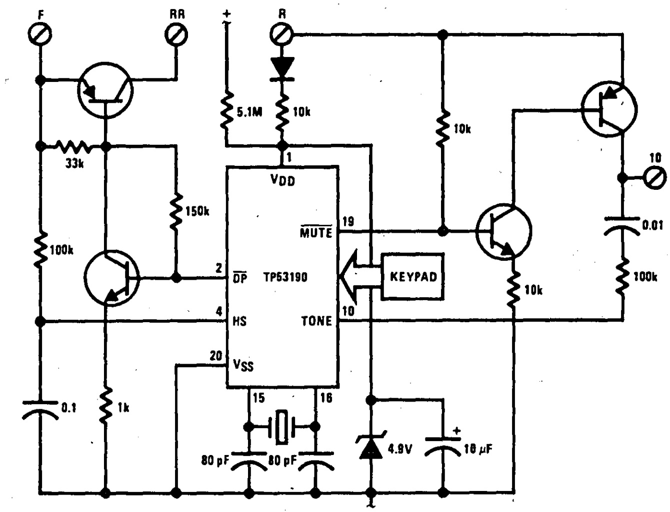


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FIGURE 6. Using the TP53190 Pulse Dialer with Redial Option

Section 6

Converters

6

Introduction

For data conversion products, digital-to-analog converters (DACs) and analog-to-digital converters (A/Ds), CMOS offers many advantages. The first is the low-cost high-performance analog switch that is easily achieved: the CMOS transmission gate. These switches are useful in DACs and have allowed a breakthrough in the design of A/Ds.

ANALOG-TO-DIGITAL CONVERTERS

The comparator is the key to an A/D. It must be fast with a fraction of an LSB voltage overdrive, exhibit no hysteresis and no oscillations in the linear region, and have high noise immunity.

A new sampled-data comparator has solved these performance problems and also provides many additional features—for example, true differential analog voltage inputs, useful reference voltage options and even incorporation of the analog multiplexer within the A/D.

REALIZING THE COMPARATOR FUNCTION

To realize the comparator function, National uses a cascade of capacitor-coupled CMOS logic inverters and switches as shown in *Figure 6-1*.

The differential input voltages are converted to weighted input charges by scaling the value used for each input capacitor (C1 and C2). These input charges are balanced at the input charge summing-node ($\Delta Q1 = \Delta Q2$ at balance, or $\Delta V1 \times C1 = \Delta V2 \times C2$).

The differential input voltage feature of the sampled-data comparator allows us to borrow the old, low-cost engraving trick that is used in the manufacture of drafting scales (*Figure 6-2*).

Most of the scale has only major divisions engraved, with only one section subdivided by higher resolution engravings. This, of course, reduces the engraving costs, but requires a differential measurement to be made because zero is no longer at the end of the scale. This is the basic idea of the differential DAC (DDAC), allowing National to reduce the number of circuit components (and their associated die area) and get the same overall resolution at a lower cost.

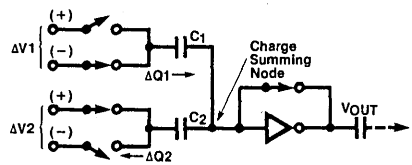


FIGURE 6-1. The Sampled-Data Comparator

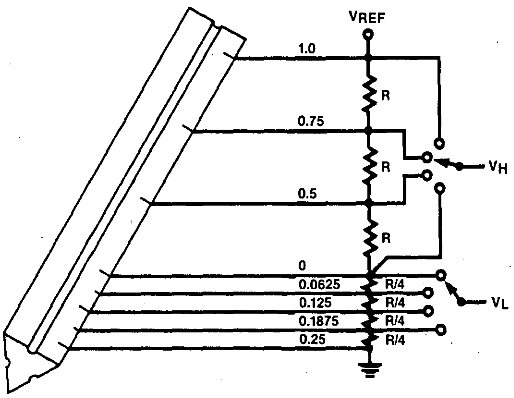


FIGURE 6-2. The Differential DAC (DDAC) Concept

Sharing the ladder makes use of all of the tap voltages that are provided by the DDAC a second time to provide four additional bits of resolution as shown in *Figure 6-3.*

The proper reduction in the significance of these last four bits is achieved by scaling down the value of the input capacitor for this 4-LSB (least significant bit) group by a factor of sixteen.

INCORPORATING AN ANALOG MULTIPLEXER

An analog multiplexer (MUX) can be easily incorporated into this A/D circuitry by adding extra switches, all of which are connected to a common analog input capacitor. Logic circuitry controls which switches are cycled, and therefore selects the analog channel that will be converted. Both the particular analog channel and either a single-ended or a differential conversion is selected by a configuration word that the CPU presents to the A/D prior to each conversion.

A wide range of CMOS A/D products is available from 8 bits to 10 bits of resolution and in serial and parallel data formats. The lowest cost A/D is an 8-bit serial product that fits in an 8-pin miniDIP. A half-flash 8-bit A/D that converts in as little as 1.2 μs is also available and a new 8-bit A/D that allows the CPU to load the on-chip DAC directly is provided for limit-testing applications.

DIGITAL-TO-ANALOG CONVERTERS

The switches available in the CMOS processes allow the realization of low power drain DACs as shown in *Figure 6-4.*

This multiplying DAC (MDAC) uses an R-2R resistor ladder and N-channel current-mode switches. Silicon-chromium thin-film resistors are used for the ladder, so the reference voltage (V_{REF}) for this DAC can be of either polarity since there are no parasitic diodes associated with thin-film resistors.

These DACs appear like a memory location to a μP. Decoding the address bus provides the chip select ($\overline{CS}$) signal and the digital code on the data bus is read by the MDAC when the write strobe ($\overline{WR}$) falls. For the 10-bit and 12-bit MDACs, package pin options are provided which allow the data to be accepted in one write cycle or in two bytes.

A broad product offering exists, from 8 bits to 12 bits, with or without input data latches. These MDACs make use of double data latches: one holds the code that is providing the analog output while the other allows 10-bit or 12-bit words to be assembled from an 8-bit data bus. Even the 8-bit MDACs use double latches to allow writing new data to a number of DACs and then simultaneously updating all of these DACs.

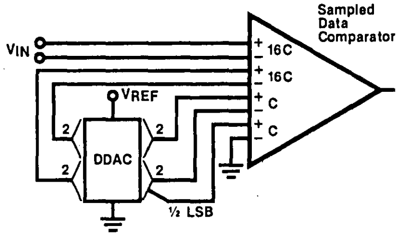


FIGURE 6-3. Increasing from 4 Bits to 8 Bits in an A/D

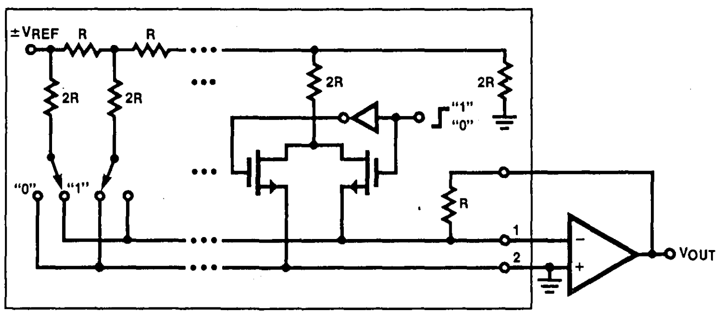


FIGURE 6.4. The CMOS MDAC

6

National Semiconductor

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

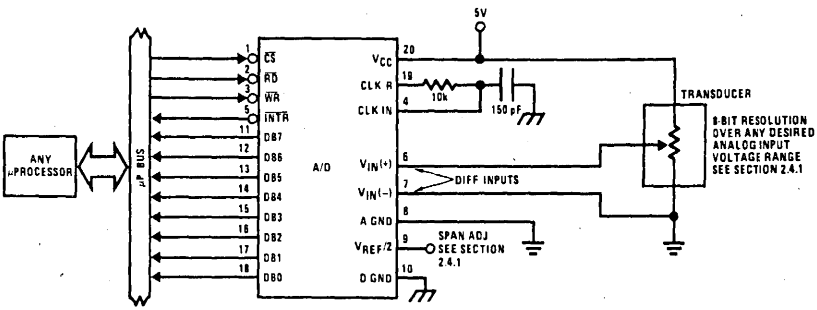
- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

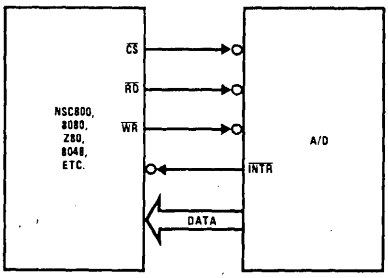
- Resolution 8 bits
- Total error ±1/4 LSB, ±1/2 LSB and ±1 LSB
- Conversion time 100 μs

6

Typical Applications



8080 Interface



TL/H/5671-1

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±1/4 LSB		
ADC0802		±1/2 LSB	
ADC0803	±1/2 LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02LD	$-55°C \leq T_A \leq +125°C$
ADC0801/02/03/04LCD	$-40°C \leq T_A \leq +85°C$
ADC0801/02/03/05LCN	$-40°C \leq T_A \leq +85°C$
ADC0804LCN	$0°C \leq T_A \leq +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 1.0	8.0 1.3		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd-0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 V_{DC}, f_{CLK}=640 kHz			8770	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$=0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

Electrical Characteristics

The following specifications apply for V_{CC} = $5V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 μA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 μA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = "1" ADC0801/02/03/05 ADC0804 (Note 9)		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

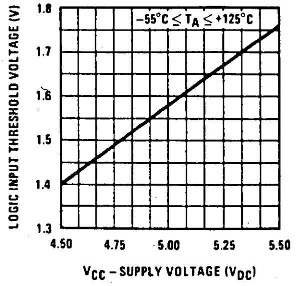
Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

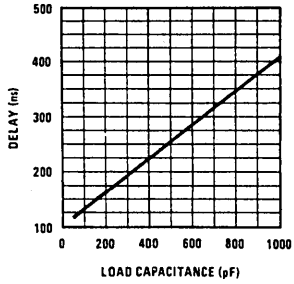
Note 9: For ADC0804LCD typical value of $V_{REF}/2$ input resistance is 8 kΩ and of I_{CC} is 1.1 mA.

Typical Performance Characteristics

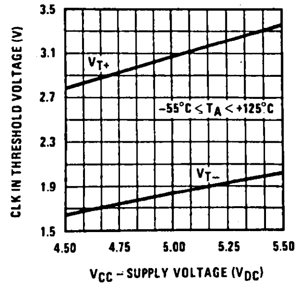
Logic Input Threshold Voltage vs. Supply Voltage



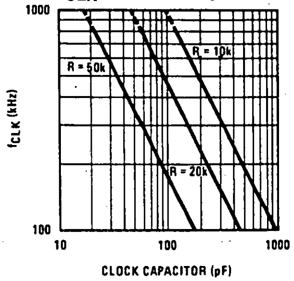
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



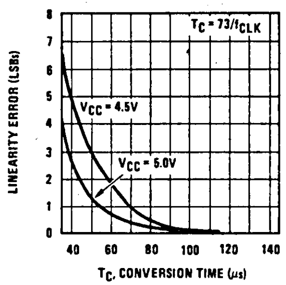
CLK IN Schmitt Trip Levels vs. Supply Voltage



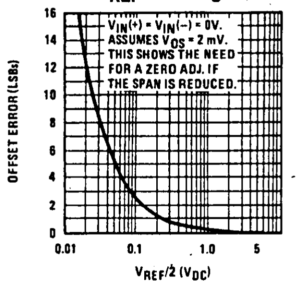
f_{CLK} vs. Clock Capacitor



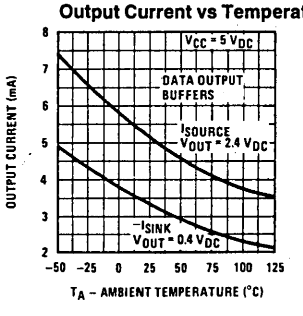
Full-Scale Error vs Conversion Time



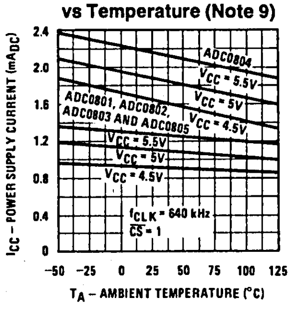
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



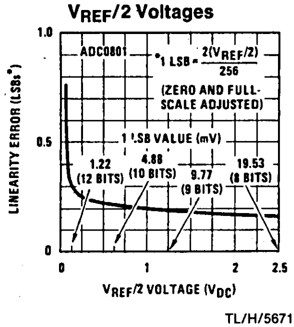
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

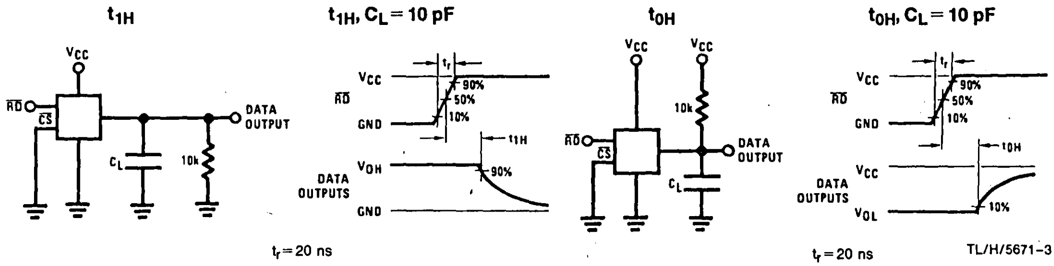


Linearity Error at Low $V_{REF}/2$ Voltages



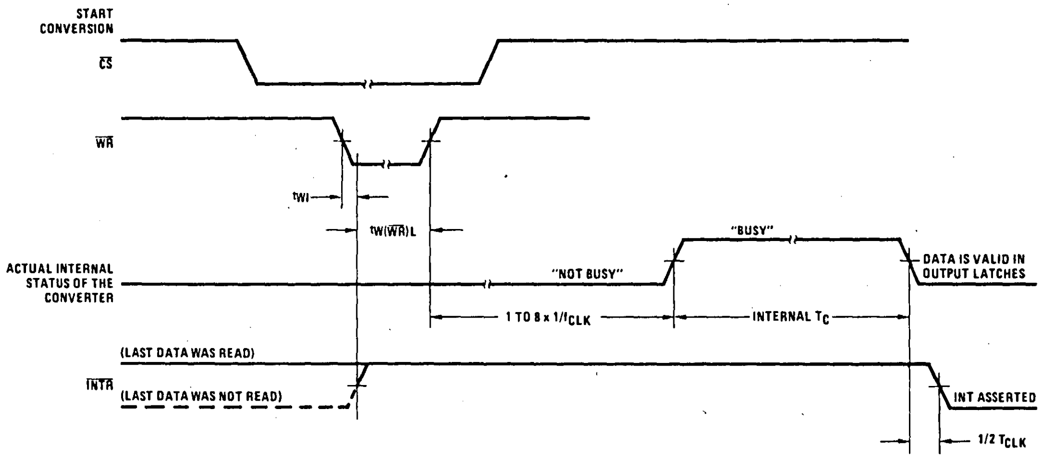
TL/H/5671–2

TRI-STATE Test Circuits and Waveforms

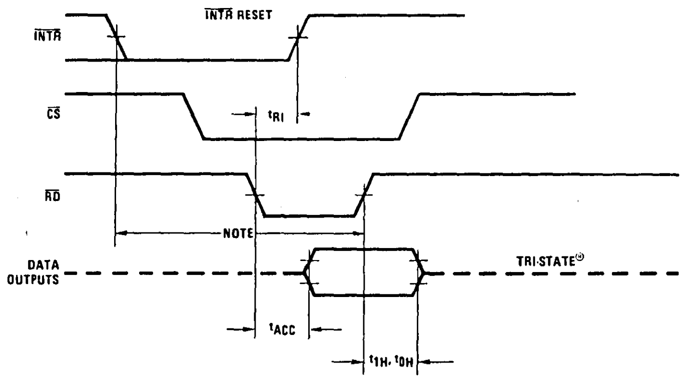


TL/H/5671-3

Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{\text{INTR}}$

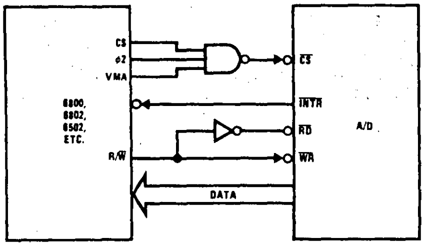


TL/H/5671-4

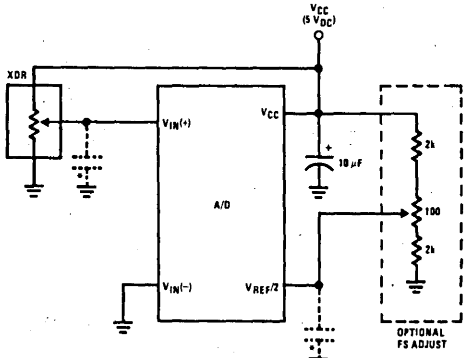
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{\text{INTR}}$.

Typical Applications (Continued)

6800 Interface

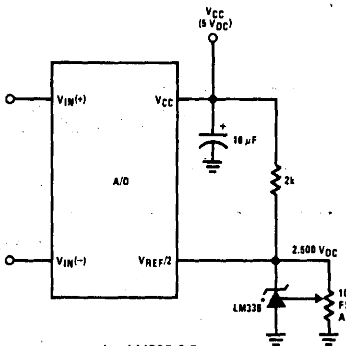


Ratiometric with Full-Scale Adjust



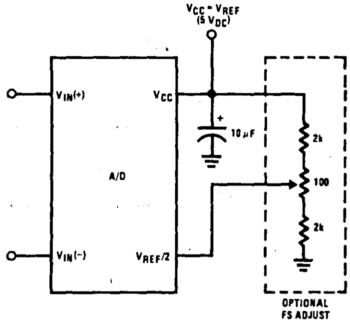
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

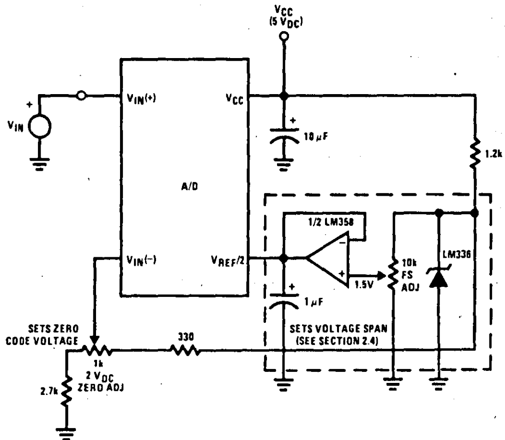


*For low power, see also LM385-2.5

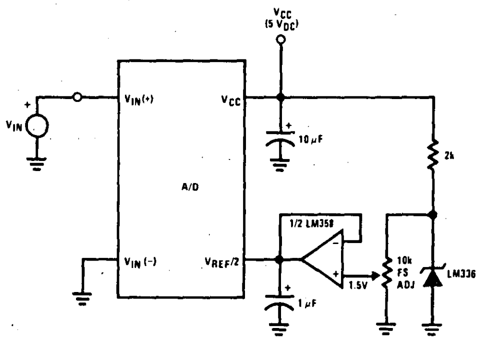
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



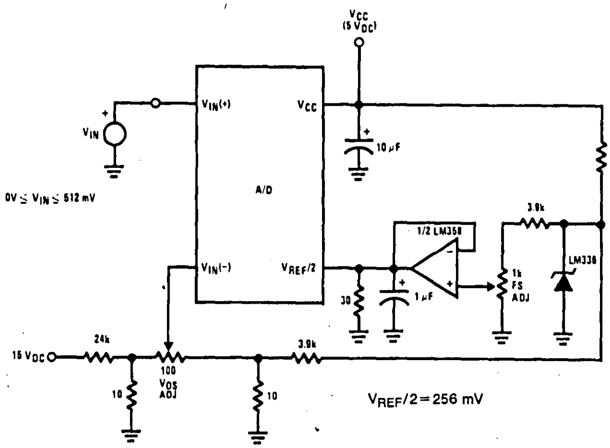
Span Adjust: $0V \leq V_{IN} \leq 3V$



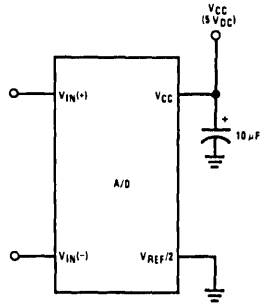
TL/H/5671–5

Typical Applications (Continued)

Directly Converting a Low-Level Signal



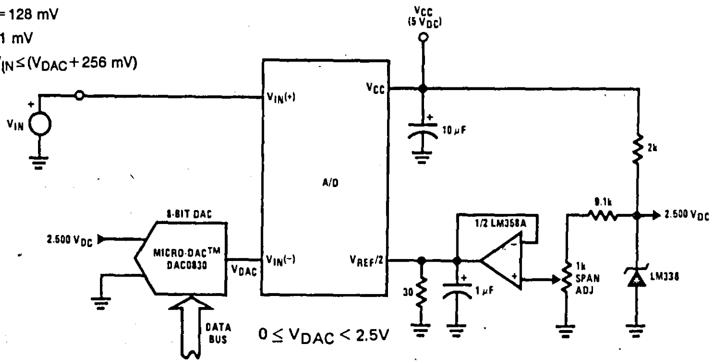
A µP Interfaced Comparator



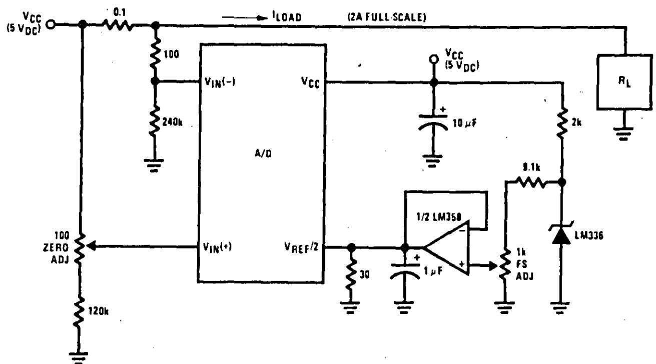
For: $V_{IN}(+) > V_{IN}(-)$
Output $= FF_{HEX}$
For: $V_{IN}(+) < V_{IN}(-)$
Output $= 00_{HEX}$

1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \le V_{IN} \le (V_{DAC} + 256$ mV)



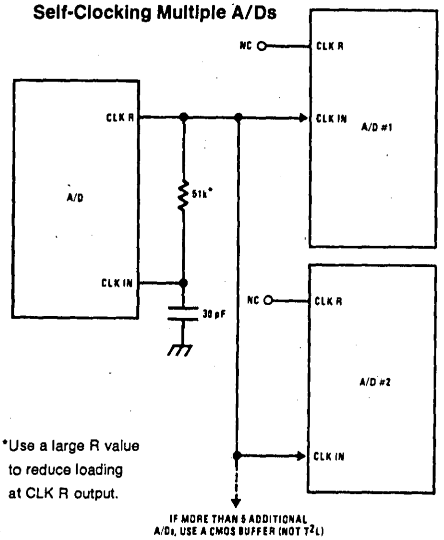
Digitizing a Current Flow



TL/H/5671-6

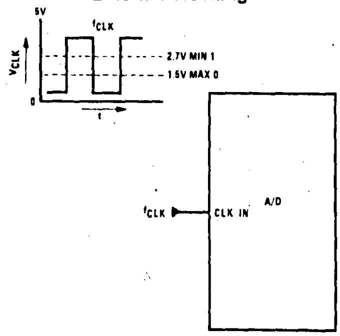
Typical Applications (Continued)

Self-Clocking Multiple A/Ds



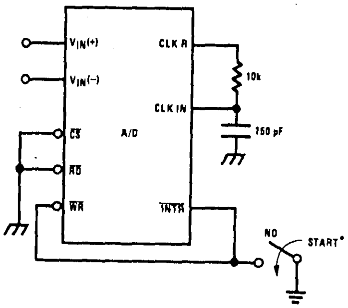
*Use a large R value to reduce loading at CLK R output.

External Clocking



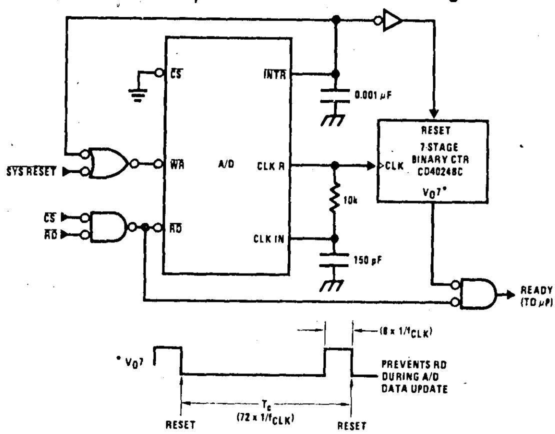
100 kHz $\leq f_{CLK} \leq$ 1460 kHz

Self-Clocking in Free-Running Mode

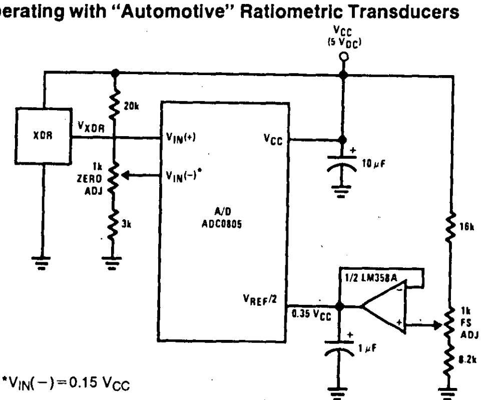


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

μP Interface for Free-Running A/D



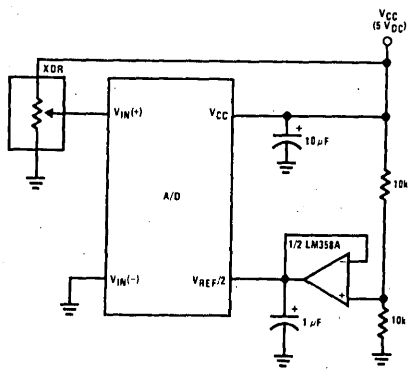
Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq$ 85% of V_{CC}

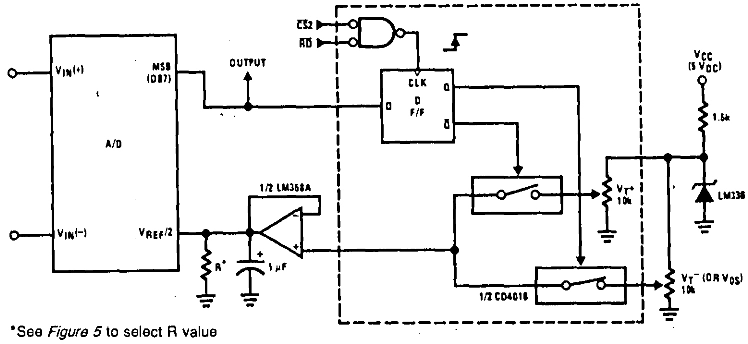
Ratiometric with $V_{REF}/2$ Forced



TL/H/5671-7

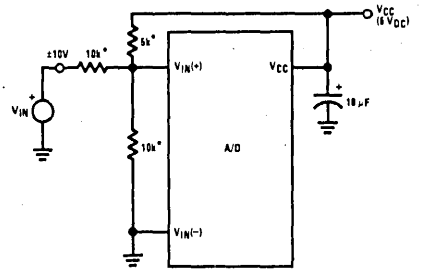
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

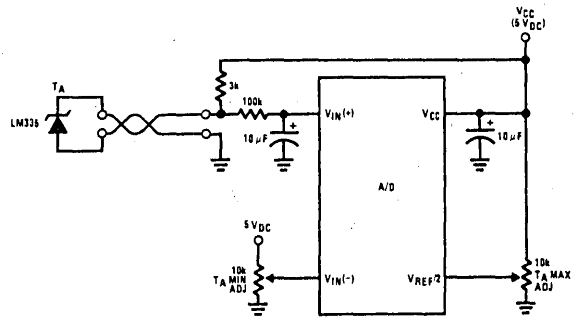


*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Handling ± 10V Analog Inputs

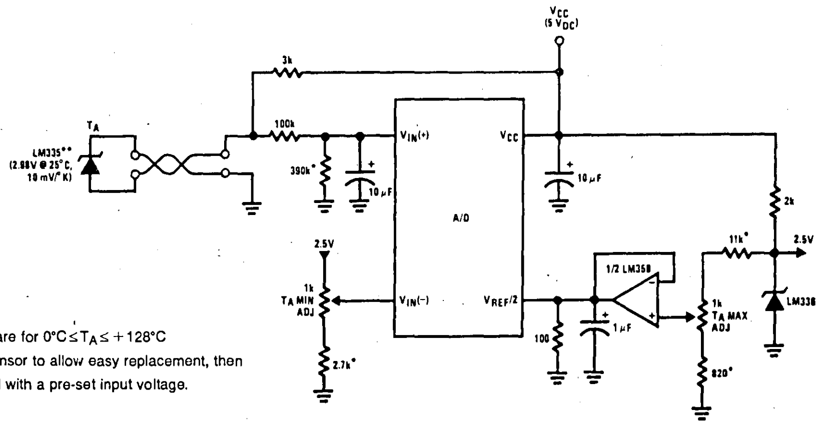


Low-Cost, μP Interfaced, Temperature-to-Digital Converter



*Beckman Instruments #694-3-R10K resistor array

μP Interfaced Temperature-to-Digital Converter



*Circuit values shown are for 0°C ≤ T_A ≤ +128°C
**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

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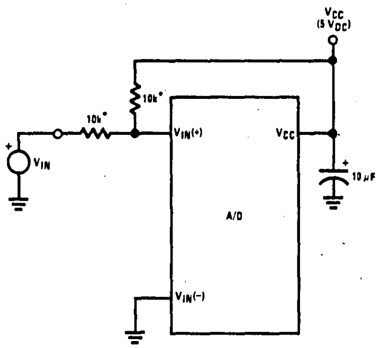
6

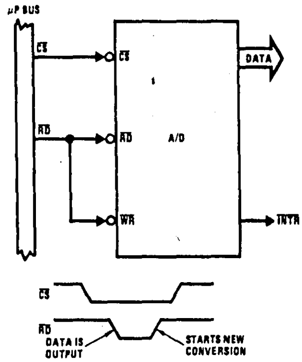
Typical Applications (Continued)

Handling ±5V Analog Inputs

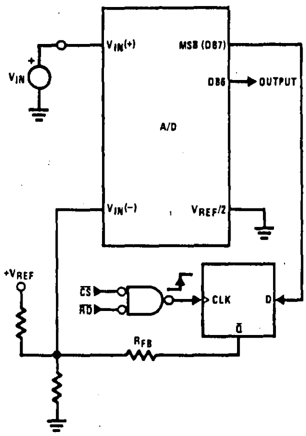


*Beckman Instruments #694-3-R10K resistor array

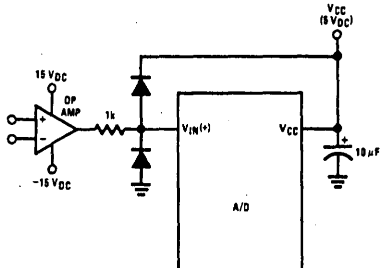
Read-Only Interface



μP Interfaced Comparator with Hysteresis

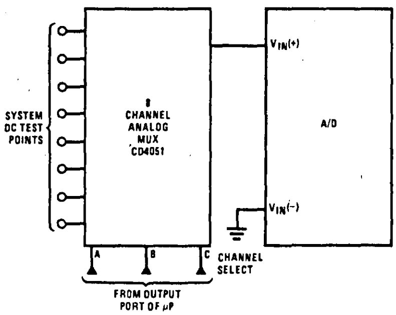


Protecting the Input

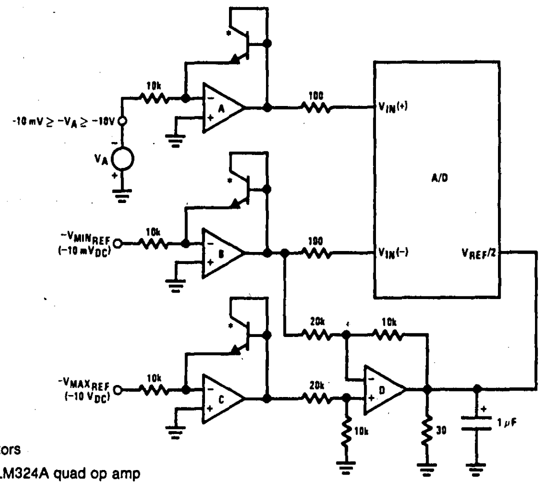


Diodes are 1N914

Analog Self-Test for a System



A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors

A, B, C, D = LM324A quad op amp

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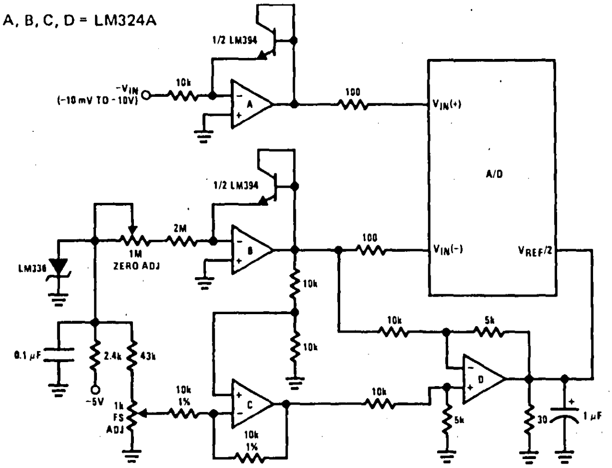
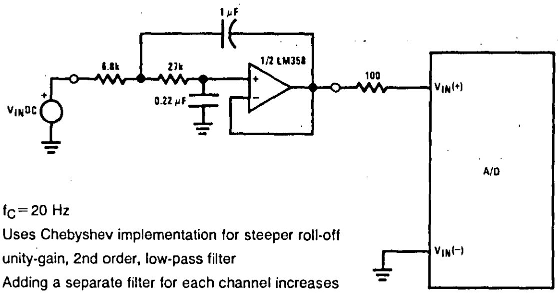
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A

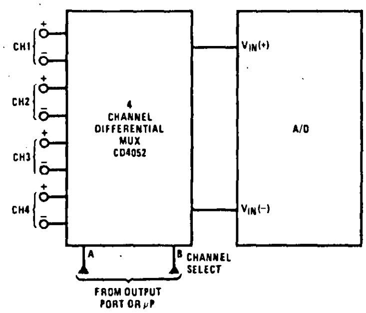


Noise Filtering the Analog Input

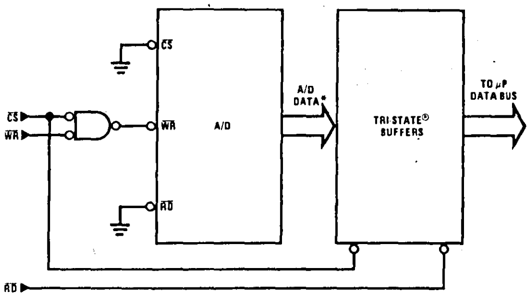


$f_C = 20$ Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

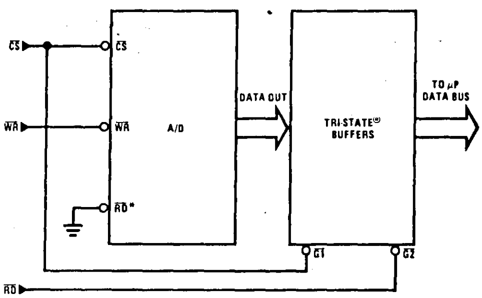


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus



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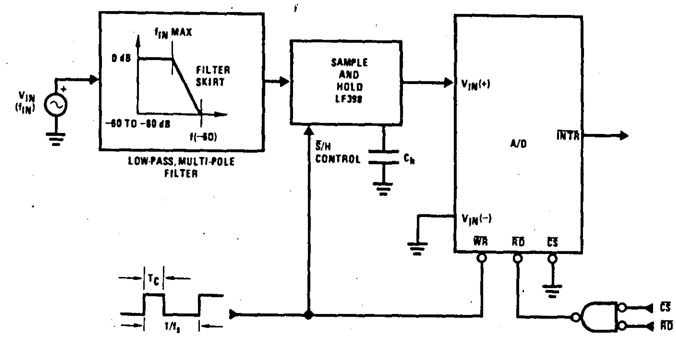
*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

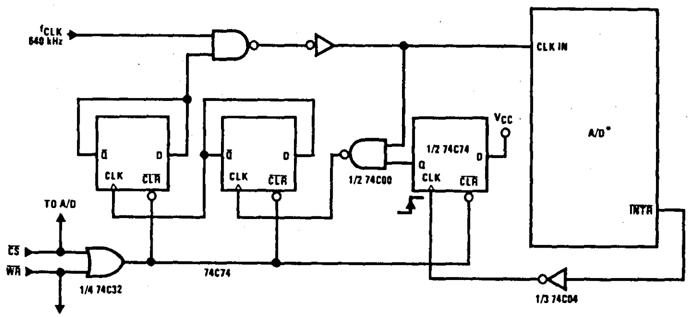
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

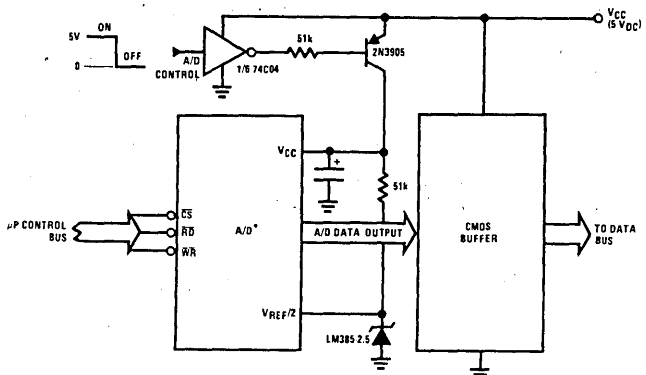
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



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*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

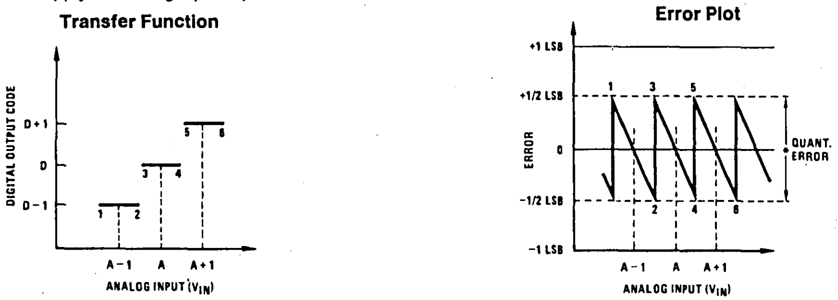
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

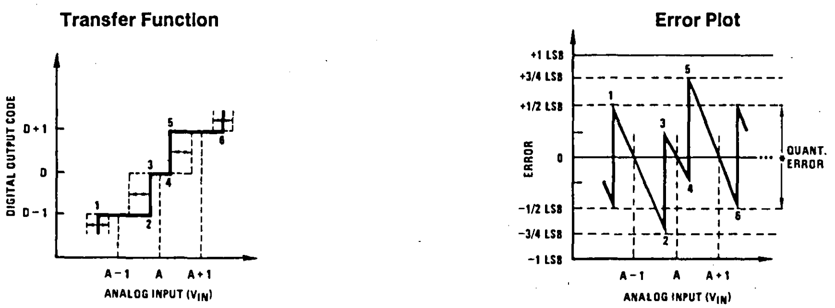
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

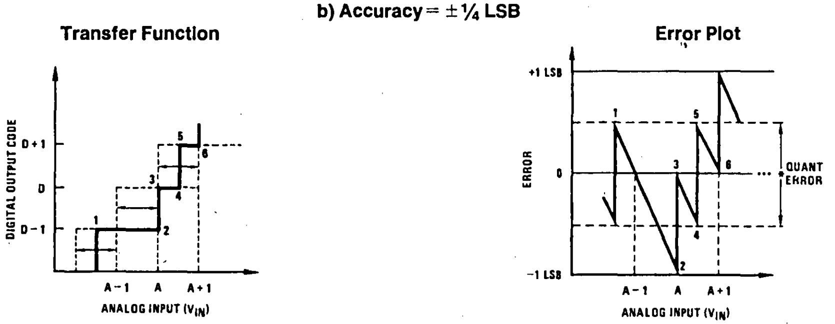
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB A Perfect A/D



b) Accuracy = ±¼ LSB



c) Accuracy = ±½ LSB

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FIGURE 1. Clarifying the Error Specs of an A/D Converter

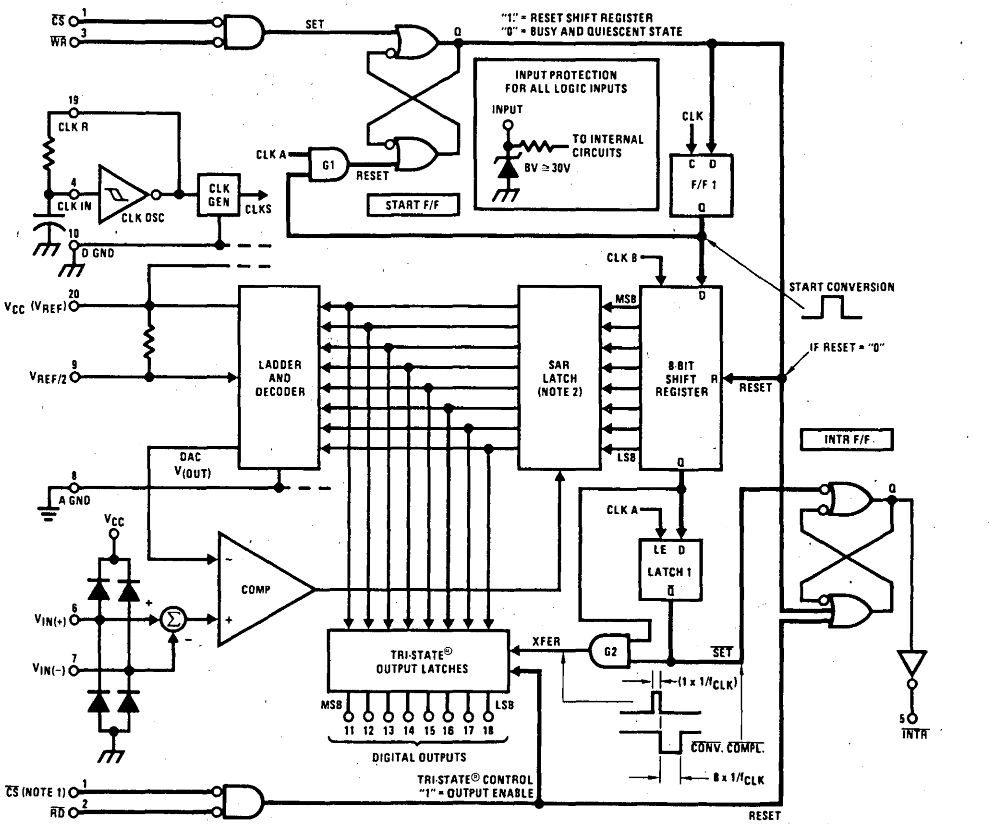
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{\text{INTR}}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{\text{INTR}}$ to the $\overline{\text{WR}}$ input with $\overline{\text{CS}}=0$. To insure start-up under all possible conditions, an external $\overline{\text{WR}}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{\text{WR}}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{\text{CS}}$ input and $\overline{\text{WR}}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{\text{CS}}$ and $\overline{\text{WR}}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{\text{WR}}$ or $\overline{\text{CS}}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



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Note 1: $\overline{\text{CS}}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{\text{INTR}}$ input signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ both held low), the $\overline{\text{INTR}}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{\text{INTR}}$ pin tied to $\overline{\text{WR}}$ and $\overline{\text{CS}}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{\text{Q}}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\text{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{\text{WR}}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\text{RD}}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)\,(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}\,(f_{CLK})]}{(2\pi f_{cm})\,(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\,(640 \times 10^3)}{(6.28)\,(60)\,(4.5)}$$

which gives

$V_P \cong 1.9V.$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

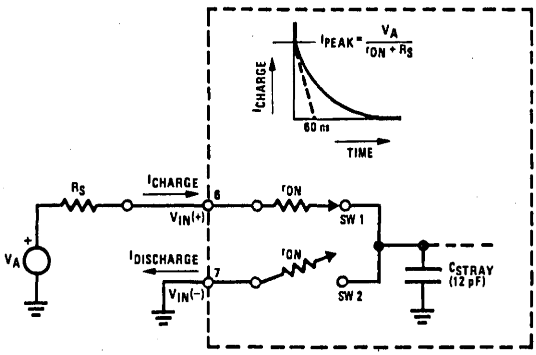
An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



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r_{ON} of SW 1 and SW 2 $\cong$ 5 kΩ

$\tau = r_{ON}\,C_{STRAY} \cong 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source which is applied to the $V_{IN}(+)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents could exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\leq$ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\leq$ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

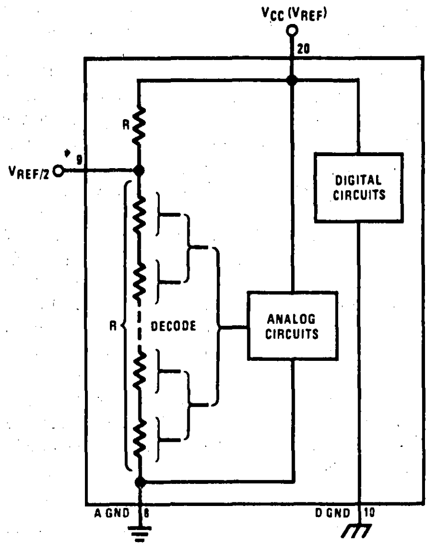
2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

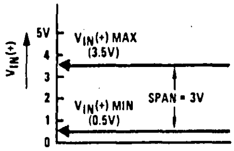


TL/H/5671-15

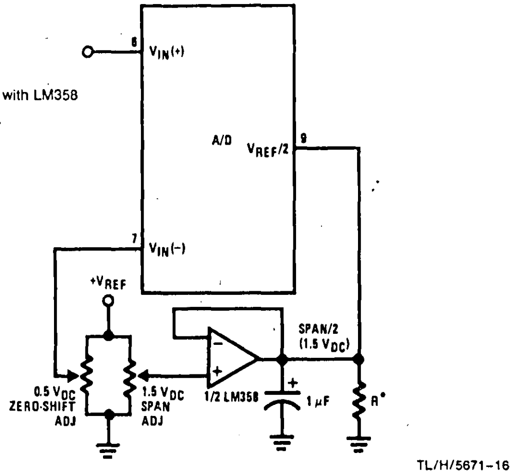
FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage which is applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2 making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.



a) Analog Input Signal Example



b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ± 10 mV_{DC} will cause conversion errors of ± 1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) is available which has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V (−) input and applying a small magnitude positive voltage to the V (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500$ V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code which is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

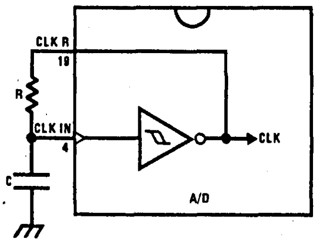
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\ RC}$$

$R \cong 10\ k\Omega$

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FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power T^2L buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard T^2L buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output also simple remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to insure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky is recommended such as the DM74LS240 series) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7.*

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the decoded voltages which are obtained from the column: Input voltage value for a 2.560 $V_{REF}/2$ of both the MS and the LS groups, the value of the digital display can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

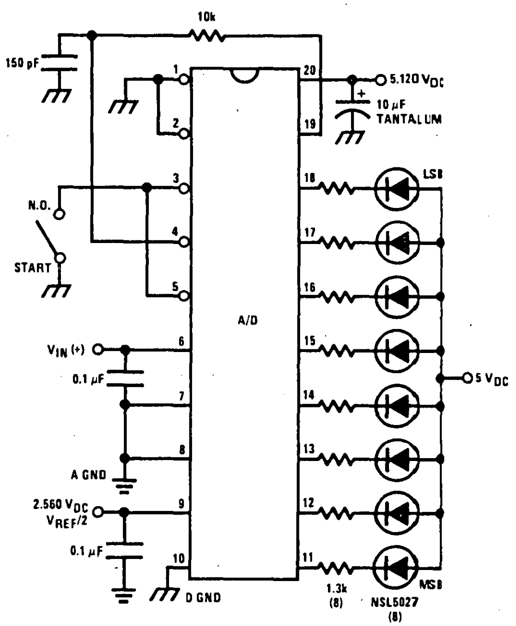

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FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in 2 ditigal words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be elminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A−C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10.*

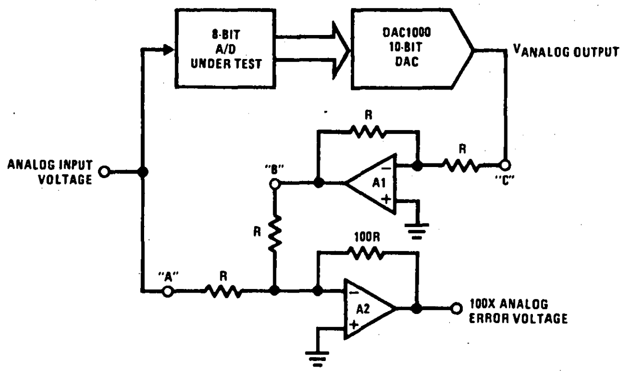

FIGURE 8. A/D Tester with Analog Error Output

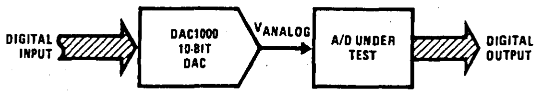

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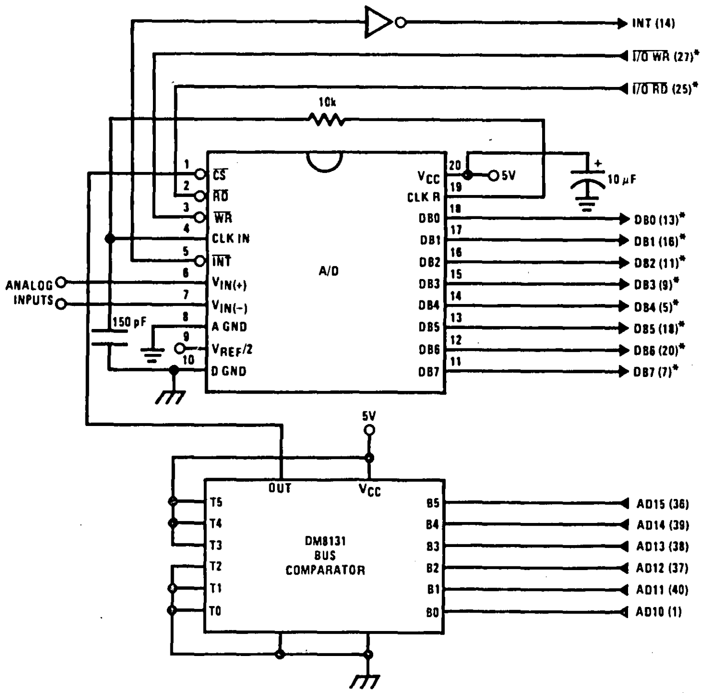
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2/880	0.180
8	1 0 0 0	1/2	1/32	2/560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1/280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*Display Output = VMS Group + VLS Group



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Note 1: *Pin numbers for the INS8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801-INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801-INS8080A CPU INTERFACE

```
0038   C3 00 03   RST 7:      JMP    LD DATA
  •        •         •
  •        •         •
0100   21 00 02   START:      LXI H 0200H      ; HL pair will point to
                                               ; data storage locations
0103   31 00 04   RETURN:     LXI SP 0400H     ; Initialize stack pointer (Note 1)
0106   7D                     MOV A, L         ; Test # of bytes entered
0107   FE 0F                  CPI 0F H         ; If # = 16. JMP to
0109   CA 13 01               JZ CONT          ; user program
010C   D3 E0                  OUT E0 H         ; Start A/D
010E   FB                     EI               ; Enable interrupt
010F   00         LOOP:       NOP              ; Loop until end of
0110   C3 0F 01               JMP LOOP         ; conversion
0113       •      CONT:         •
  •        •         •          •
  •        •      (User program to  •
  •        •      process data)     •
  •        •         •          •
  •        •         •          •
0300   DB E0      LD DATA:    IN E0 H          ; Load data into accumulator
0302   77                     MOV M, A         ; Store data
0303   23                     INX H            ; Increment storage pointer
0304   C3 03 01               JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{\text{CS}}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{\text{CS}}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{INT}}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

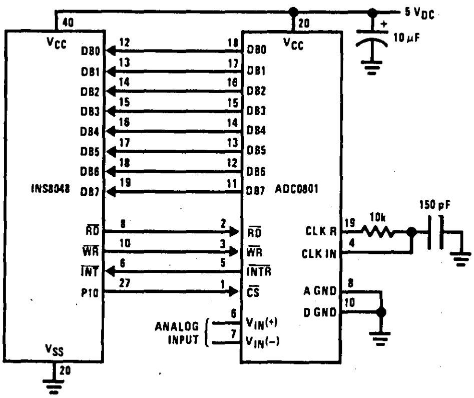

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                JMP     10H          ; Program starts at addr 10
                     ORG     3H
04 50                JMP     50H          ; Interrupt jump vector
                     ORG     10H          ; Main program
99 FE                ANL     P1, #0FEH    ; Chip select
81                   MOVX    A, @R1       ; Read in the 1st data
                                          ; to reset the intr
89 01    START:      ORL     P1, #1       ; Set port pin high
B8 20                MOV     R0, #20H     ; Data address
B9 FF                MOV     R1, #0FFH    ; Dummy address
BA 10                MOV     R2, #10H     ; Counter for 16 bytes
23 FF    AGAIN:      MOV     A, #0FFH     ; Set ACC for intr loop
99 FE                ANL     P1, #0FEH    ; Send CS (bit 0 of P1)
91                   MOVX    @R1, A       ; Send WR out
05                   EN      I            ; Enable interrupt
96 21    LOOP:       JNZ     LOOP         ; Wait for interrupt
EA 1B                DJNZ    R2, AGAIN    ; If 16 bytes are read
00                   NOP                  ; go to user's program
00                   NOP
                     ORG     50H
81       INDATA:     MOVX    A, @R1       ; Input data, CS still low
A0                   MOV     @R0, A       ; Store in memory
18                   INC     R0           ; Increment storage counter
89 01                ORL     P1, #1       ; Reset CS signal
27                   CLR     A            ; Clear ACC to get out of
93                   RETR                 ; the interrupt loop
```

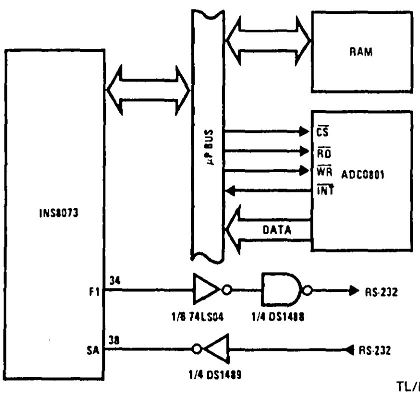

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FIGURE 12. INS8073 Interface

SAMPLE PROGRAM FOR *FIGURE 12* — INS8073 INTERFACE

```
100  C = 16                        ; REM C is the 16 bytes counter
110  D = #13D0                     ; REM D points to data address
120  @ #3000 = A                   ; REM start A/D
130  A = STAT AND #20              ; REM wait until interrupt
140  IF A <> 0 THEN GO TO 130      ; REM from A/D
150  @ D = @ #3000                 ; REM input converted data
160  D = D + 1                     ; REM increment data address
170  C = C - 1                     ; REM check counter
180  IF C > 0 THEN GO TO 120       ; REM if 16 data have been read
190  RETURN                        ; REM return to main program
```

4.1.3 INS8073 Interface

The INS8073 allows users to program directly in Tiny Basic. DS1488/1489 driver/receiver chips are used for level buffering to communicate via RS-232. (For a detailed description of the INS8073 and the Tiny Basic, see INS8073 data sheet.) The ADC0801 is mapped into the memory space of the 8073 system (see *Figure 12*). A RAM of 1k bytes is provided in which the first 256 bytes are used by the Tiny Basic micro-interpreter. Address 3000 (Hex) is assigned to the A/D and the 16 converted data bytes are stored at external RAM locations from 13D0 to 13DF (Hex). STAT function is used to examine the interrupt signal from the A/D. A sample Tiny Basic subroutine is given in the sample program for *Figure 12* — INS8073 Interface.

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

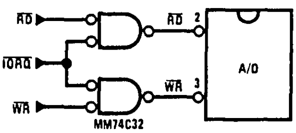

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FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives doe not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4.5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine essentially performs the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

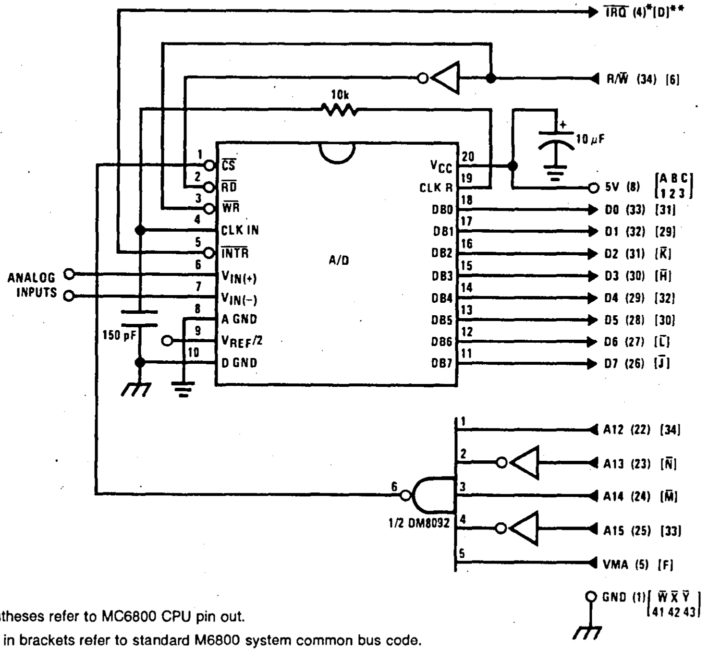
A sample interface program equivalent to the previous one, is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor which is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

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FIGURE 14. ADC0801-MC6800 CPU Interface

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010   DF 36      DATAIN   STX    TEMP2     ; Save contents of X
0012   CE 00 2C            LDX    #$002C    ; Upon IRQ low CPU
0015   FF FF F8            STX    $FFF8     ; jumps to 002C
0018   B7 50 00            STAA   $5000     ; Start ADC0801
001B   0E                  CLI
001C   3E         CONVRT   WAI              ; Wait for interrupt
001D   DE 34               LDX    TEMP1
001F   8C 02 0F            CPX    #$020F    ; Is final data stored?
0022   27 14               BEQ    ENDP
0024   B7 50 00            STAA   $5000     ; Restarts ADC0801
0027   08                  INX
0028   DF 34               STX    TEMP1
002A   20 F0               BRA    CONVRT
002C   DE 34      INTRPT   LDX    TEMP1
002E   B6 50 00            LDAA   $5000     ; Read data
0031   A7 00               STAA   X         ; Store it at X
0033   3B                  RTI
0034   02 00      TEMP1    FDB    $0200     ; Starting address for
                                            ; data storage
0036   00 00      TEMP2    FDB    $0000
0038   CE 02 00   ENDP     LDX    #$0200    ; Reinitialize TEMP1
003B   DF 34               STX    TEMP1
003D   DE 36               LDX    TEMP2
003F   39                  RTS              ; Return from subroutine
                                            ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

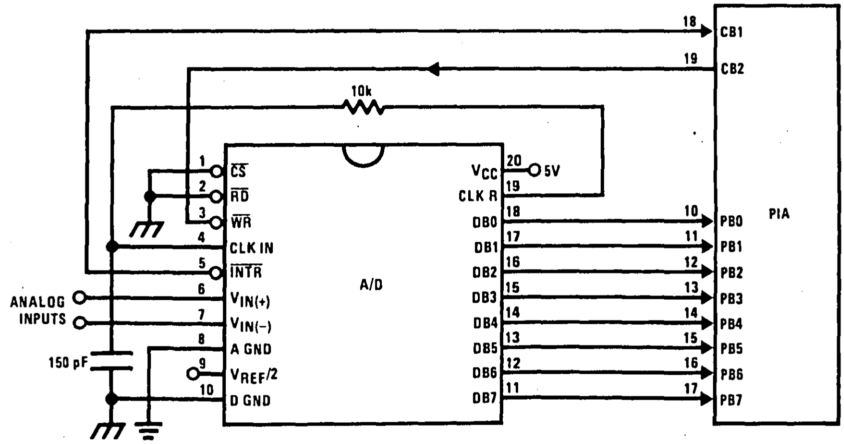

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FIGURE 15. ADC0801–MC6820 PIA Interface

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010   CE 00 38   DATAIN   LDX    #$0038   ; Upon IRQ low CPU
0013   FF FF F8            STX    $FFF8    ; jumps to 0038
0016   B6 80 06            LDAA   PIAORB   ; Clear possible IRQ flags
0019   4F                  CLRA
001A   B7 80 07            STAA   PIACRB
001D   B7 80 06            STAA   PIAORB   ; Set Port B as input
0020   0E                  CLI
0021   C6 34               LDAB   #$34
0023   86 3D               LDAA   #$3D
0025   F7 80 07   CONVRT   STAB   PIACRB   ; Starts ADC0801
0028   B7 80 07            STAA   PIACRB
002B   3E                  WAI             ; Wait for interrupt
002C   DE 40               LDX    TEMP1
002E   8C 02 0F            CPX    #$020F   ; Is final data stored?
0031   27 0F               BEQ    ENDP
0033   08                  INX
0034   DF 40               STX    TEMP1
0036   20 ED               BRA    CONVRT
0038   DE 40      INTRPT   LDX    TEMP1
003A   B6 80 06            LDAA   PIAORB   ; Read data in
003D   A7 00               STAA   X        ; Store it at X
003F   3B                  RTI
0040   02 00      TEMP1    FDB    $0200    ; Starting address for
                                           ; data storage
0042   CE 02 00   ENDP     LDX    #$0200   ; Reinitialize TEMP1
0045   DF 40               STX    TEMP1
0047   39                  RTS             ; Return from subroutine
                  PIAORB   EQU    $8006    ; To user's program
                  PIACRB   EQU    $8007
```

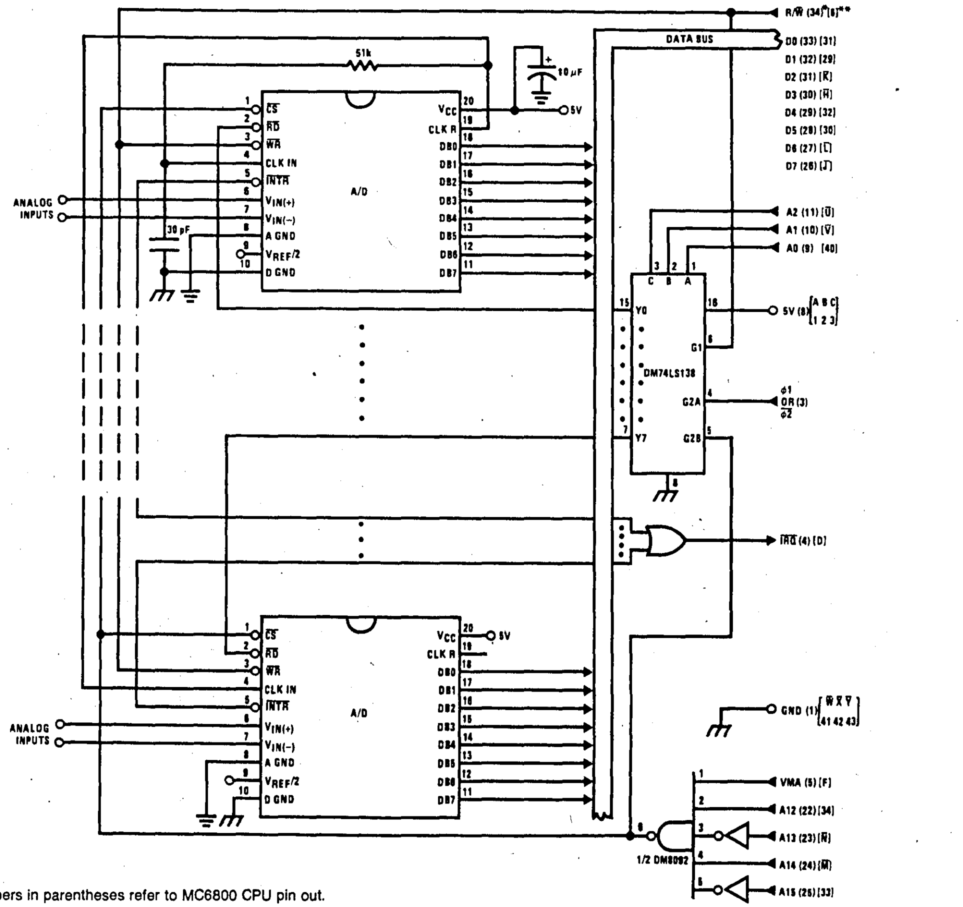
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

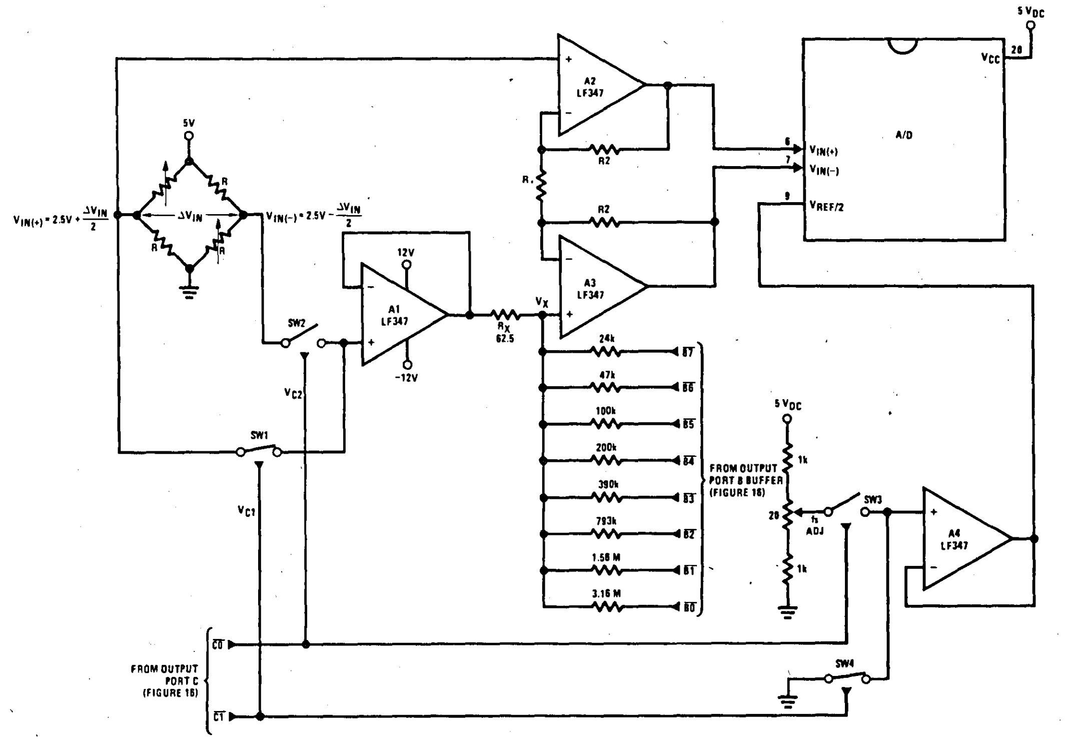
$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by insuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown. V_X can move ±12 mV with a resolution of 50 μV which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels which drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 1: R2 = 49.5 R1

Note 2: Switches are CD4066BC CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

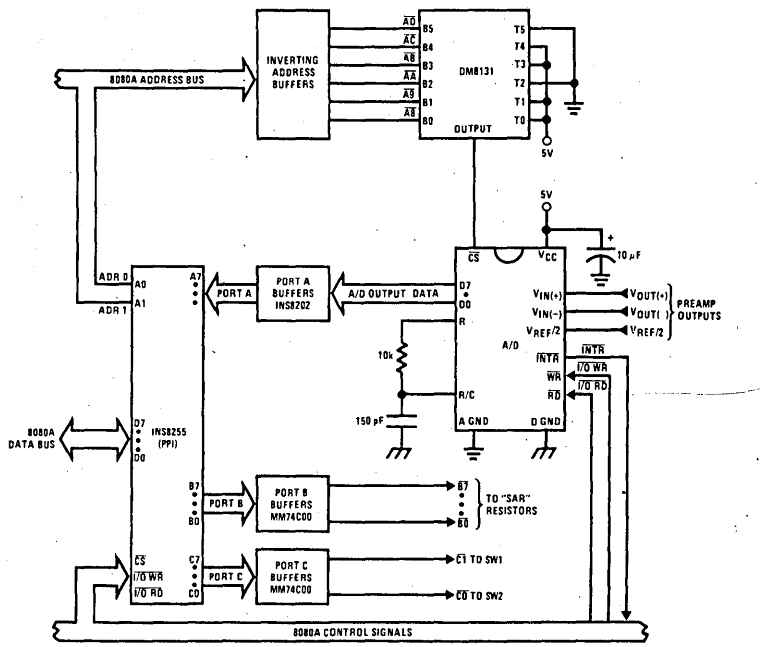


FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

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A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

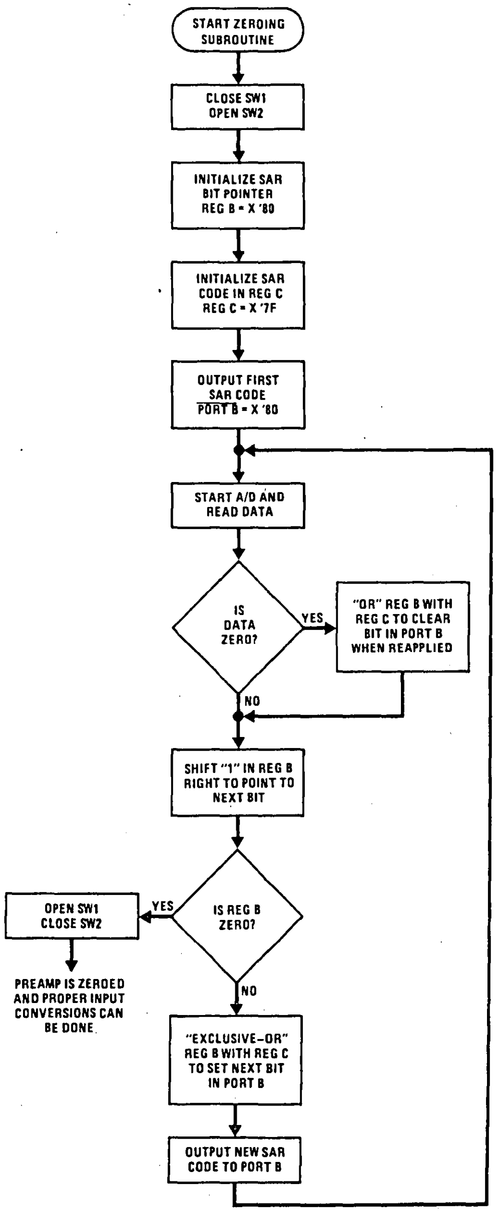

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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90    MVI 90
3D02  D3E7    Out Control Port                                ; Program PPI
3D04  2601    MVI H 01          Auto-Zero Subroutine
3D06  7C      MOV A,H
3D07  D3E6    OUT C                                           ; Close SW1 open SW2
3D09  0680    MVI B 80                                        ; Initialize SAR bit pointer
3D0B  3E7F    MVI A 7F                                        ; Initialize SAR code
3D0D  4F      MOV C,A           Return
3D0E  D3E5    OUT B                                           ; Port B = SAR code
3D10  31AA3D  LXI SP 3DAA       Start                         ; Dimension stack pointer
3D13  D3E4    OUT A                                           ; Start A/D
3D15  FB      IE
3D16  00      NOP               Loop                          ; Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D           Auto-Zero
3D1B  C600    ADI 00
3D1D  CA2D3D  JZ Set C                                        ; Test A/D output data for zero
3D20  78      MOV A,B           Shift B
3D21  F600    ORI 00                                          ; Clear carry
3D23  1F      RAR                                             ; Shift "1" in B right one place
3D24  FE00    CPI 00                                          ; Is B zero? If yes last
3D26  CA373D  JZ Done                                         ; approximation has been made
3D29  47      MOV B,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C           Set C
3D2E  B0      ORA B                                           ; Set bit in C that is in same
3D2F  4F      MOV C,A                                         ; position as "1" in B
3D30  C3203D  JMP Shift B
3D33  A9      XRA C             New C                         ; Clear bit in C that is in
3D34  C30D3D  JMP Return                                      ; same position as "1" in B
3D37  47      MOV B,A           Done                          ; then output new SAR code.
3D38  7C      MOV A,H                                         ; Open SW1, close SW2 then
3D39  EE03    XRI 03                                          ; proceed with program. Preamp
3D3B  D3E6    OUT C                                           ; is now zeroed.
3D3D          •                 Normal
              •
              •
              Program for processing
              proper data values
3C3D  DBE4    IN A              Read A/D Subroutine           ; Read A/D data
3C3F  EEFF    XRI FF                                          ; Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                                         ; Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                                          ; in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

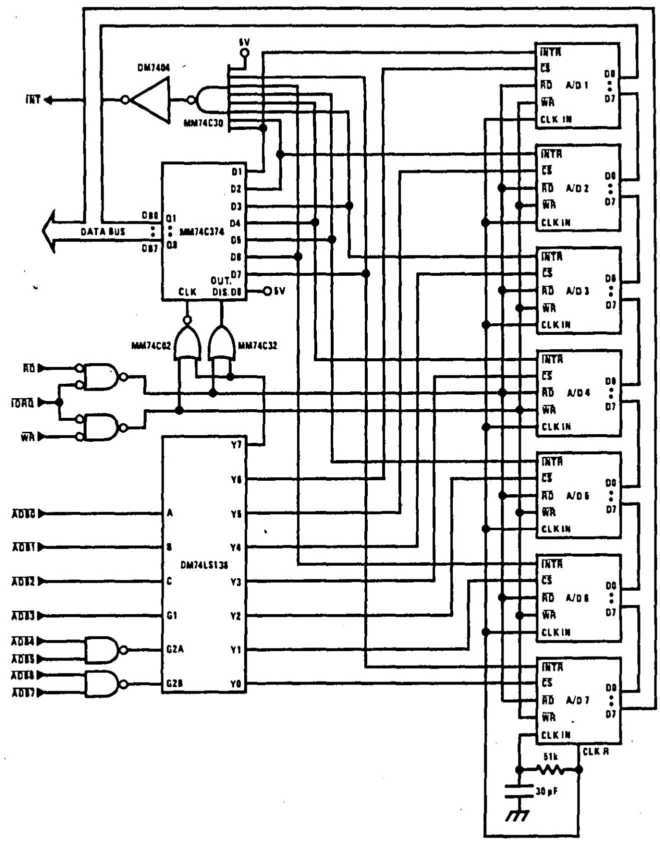

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FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

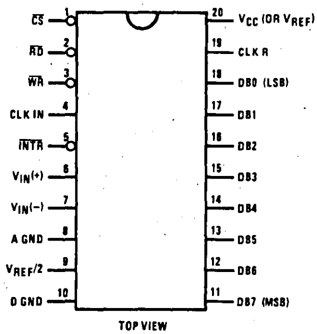
LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL), X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B,A	; Save the status word.
0045	79	TEST	LD A,C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X08	; been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP, TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL),A	; Store the data
005A	2C		INC L	
005B	71		LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP, NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program

Ordering Information

TEMPERATURE RANGE		0°C TO 70°C	−40°C TO +85°C	−40°C TO +85°C	−55°C TO +125°C
ERROR	± 1/4 Bit Adjusted		ADC0801LCN	ADC0801LCD	ADC0801LD
	± 1/2 Bit Unadjusted		ADC0802LCN	ADC0802LCD	ADC0802LD
	± 1/2 Bit Adjusted		ADC0803LCN	ADC0803LCD	
	± 1 Bit Unadjusted	ADC0804LCN	ADC0805LCN	ADC0804LCD	
PACKAGE OUTLINE		N20A-MOLDED DIP		D20A-CAVITY DIP	D20A-CAVITY DIP

Connection Diagram

ADC080X
Dual-In-Line Package



TL/H/5671-30

ADC0808, ADC0809 8-Bit µP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

Features

- Resolution—8-bits
- Total unadjusted error—±½ LSB and ±1 LSB
- No missing codes
- Conversion time—100 µS
- Single supply—5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption—15 mW
- Latched TRI-STATE® output

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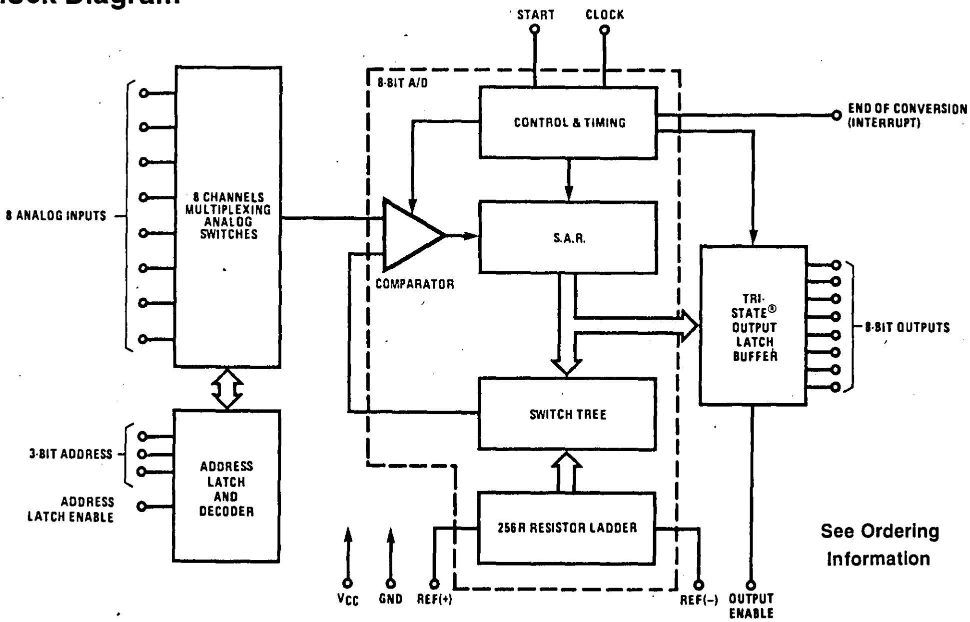
Block Diagram



See Ordering Information

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Absolute Maximum Ratings
(Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	$-0.3V$ to $(V_{CC}+0.3V)$
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	$-0.3V$ to $+15V$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation at $T_A=25°C$	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	$-55°C \le T_A \le +125°C$
ADC0808CCJ, ADC0808CCN, ADC0809CCN	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: $V_{CC}=5$ $V_{DC}=V_{REF+}$, $V_{REF(-)}=GND$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_{CLK}=640$ kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			$\pm 1/2$	LSB
	(Note 5)	T_{MIN} to T_{MAX}			$\pm 3/4$	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			± 1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			$\pm 1\frac{1}{4}$	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		$V_{CC}+0.10$	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2$-0.1	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	$f_c=640$ kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=5V$, $T_A=25°C$		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=0$, $T_A=25°C$	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	−1.0			μA
I_{CC}	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6\ mA$			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2\ mA$			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = 5V$ $V_O = 0$	 −3		3	μA μA

Electrical Characteristics

Timing Specifications $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μS
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8+2 μS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

6

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE C	ADDRESS LINE B	ADDRESS LINE A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached $+\frac{1}{2}$ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

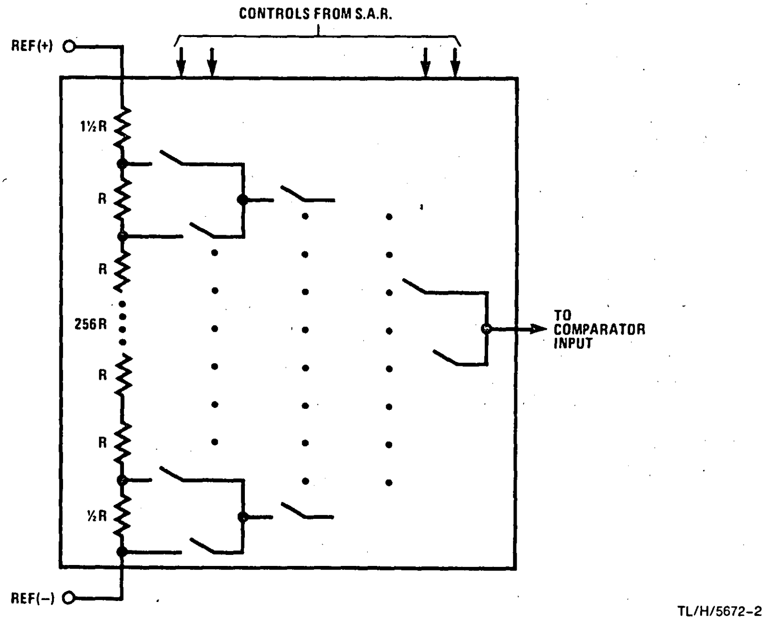


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed throught a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

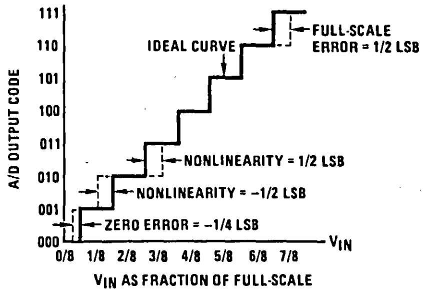


FIGURE 2. 3-Bit A/D Transfer Curve

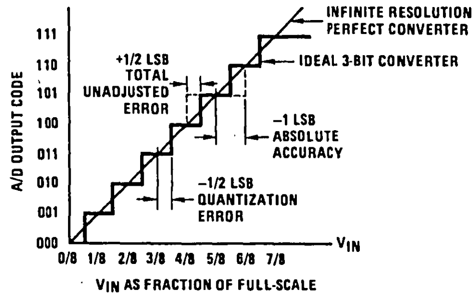
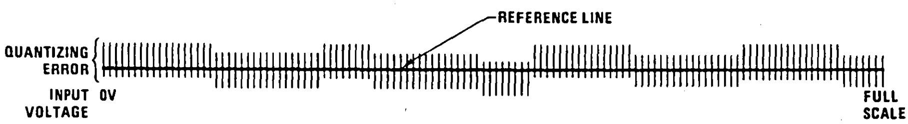


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

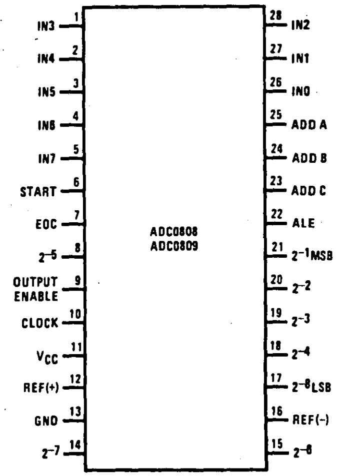


TL/H/5672–3

FIGURE 4. Typical Error Curve

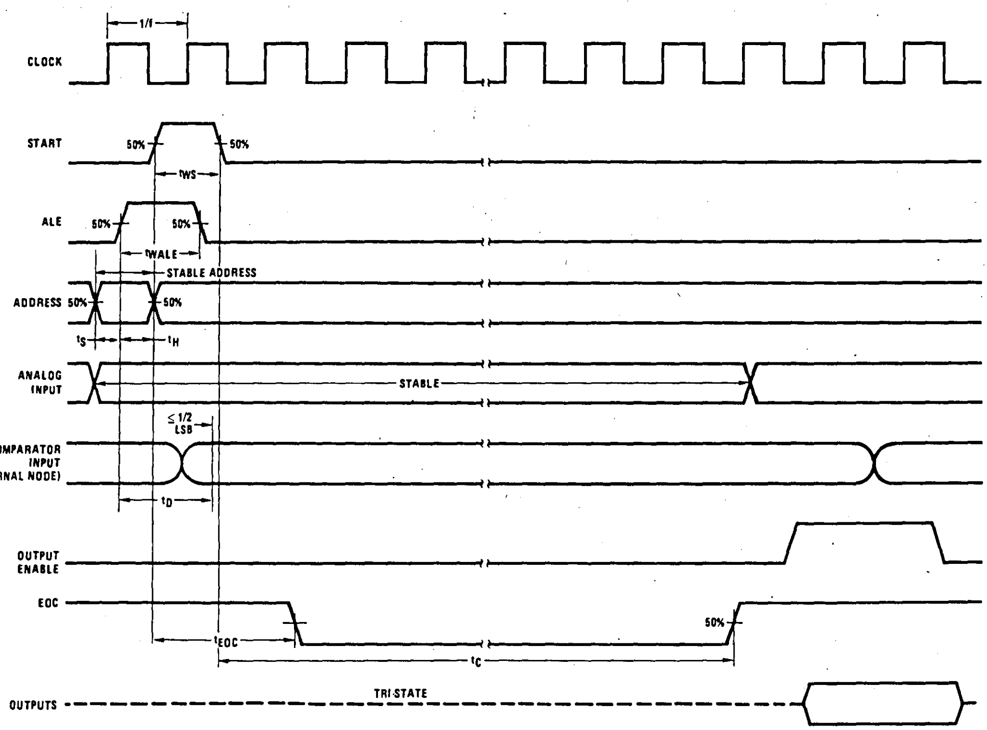
Connection Diagram

Dual-In-Line Package



TOP VIEW

Timing Diagram



TL/H/5672–4

Typical Performance Characteristics

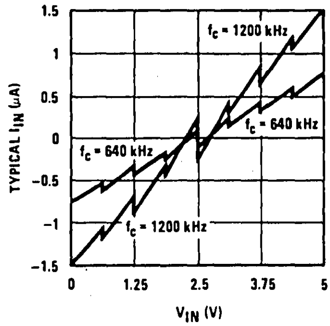


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

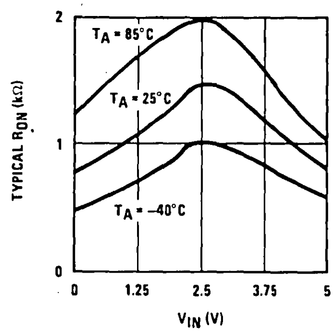


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FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

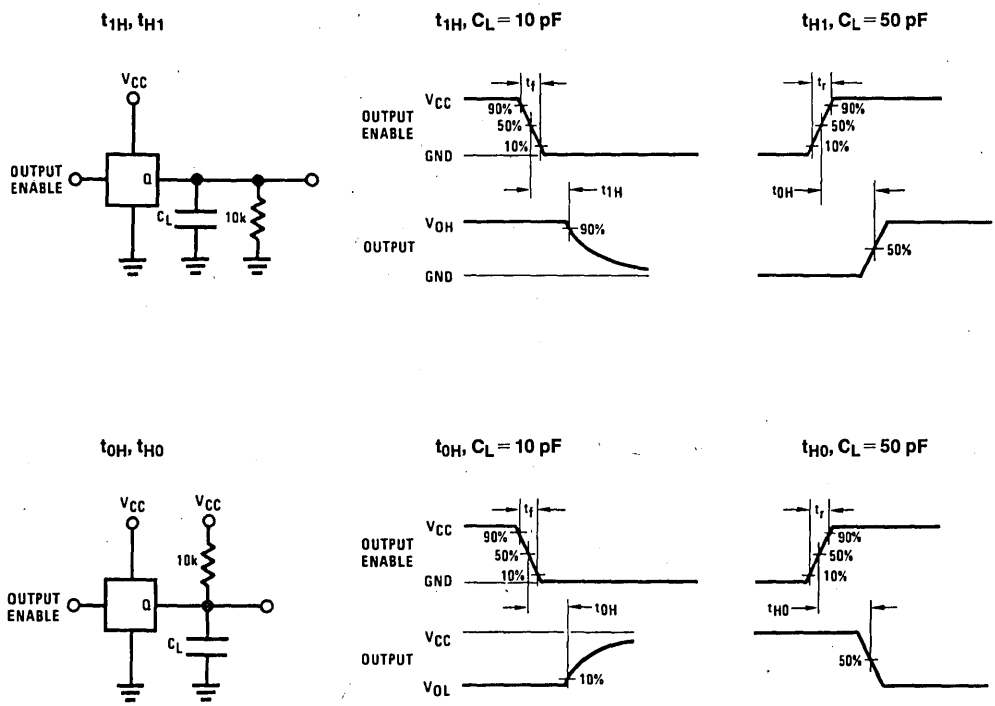

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FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \tag{1}$$

V_{IN} = Input voltage into the ADC0808

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

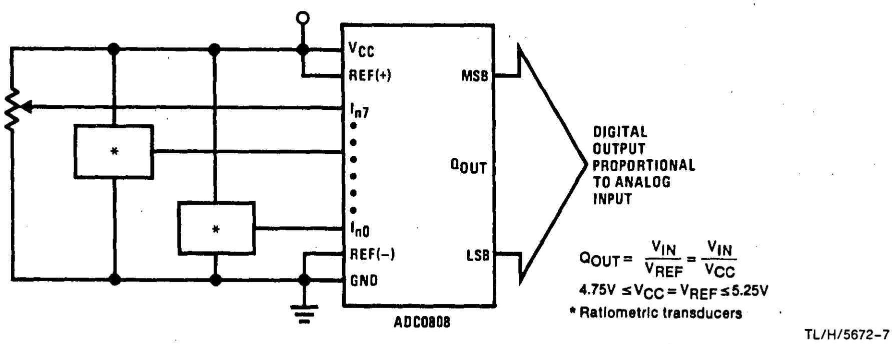

FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

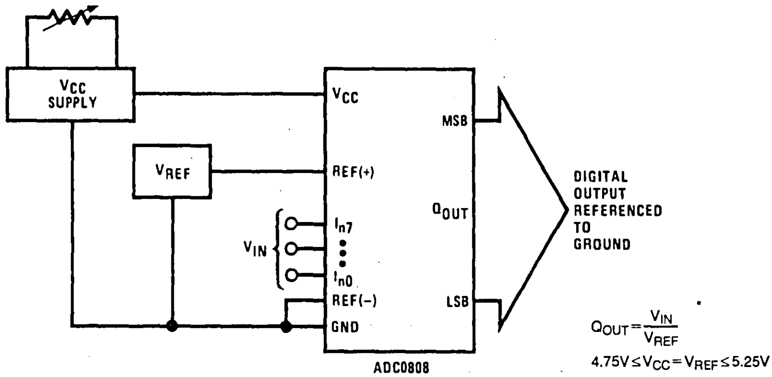

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

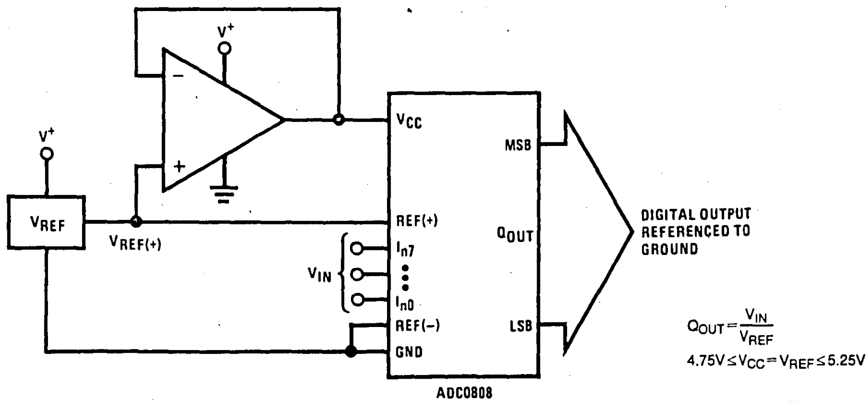

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FIGURE 11: Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

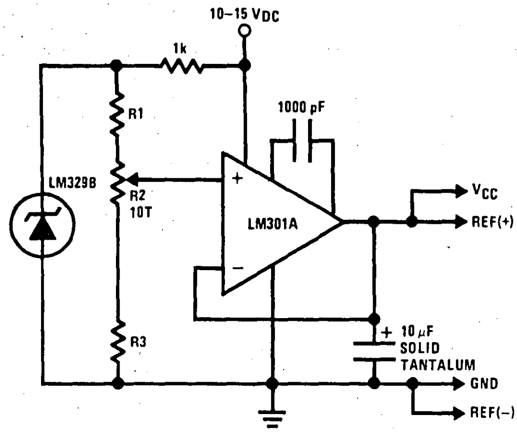

FIGURE 12. Typical Reference and Supply Circuit

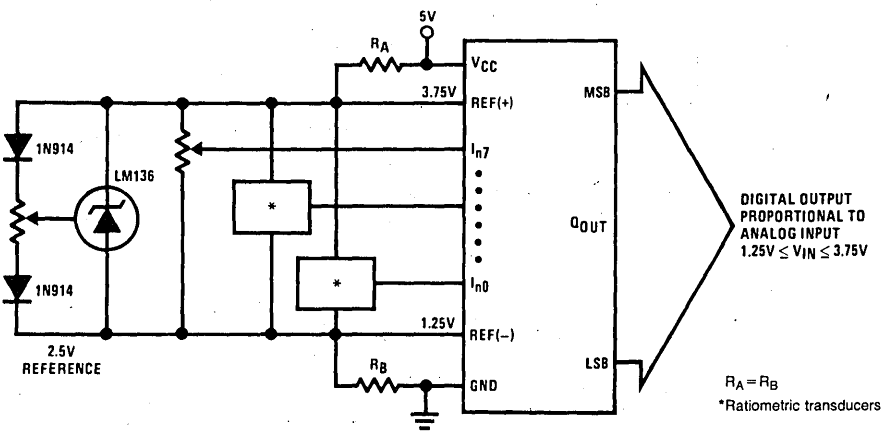

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FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN}=\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}+\frac{1}{512}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN}\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N=\frac{V_{IN}-V_{REF(-)}}{V_{REF(+)}-V_{REF(-)}}\times 256\pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

$V_{REF(+)}$ = Voltage at Ref(+)

$V_{REF(-)}$ = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 ANALOG COMPARATOR INPUTS

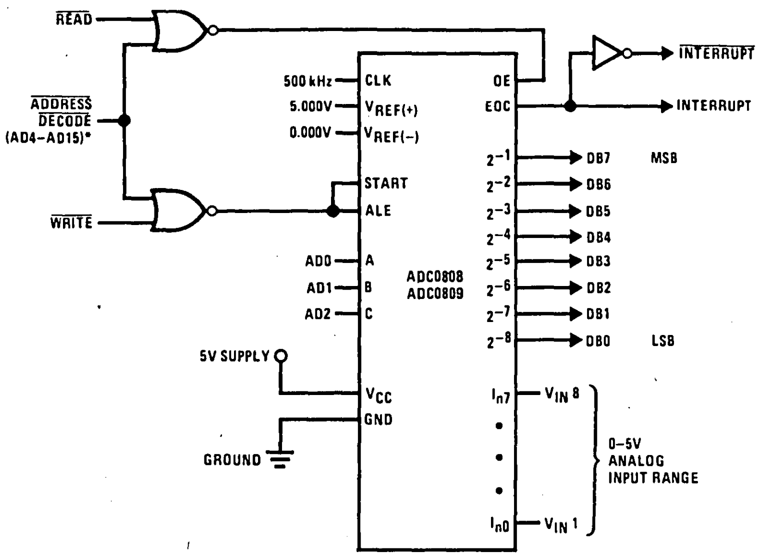
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



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*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ2•R/W	VMA•ϕ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	±½ Bit Unadjusted	ADC0808CCN	ADC0808CCJ	ADC0808CJ
	±1 Bit Unadjusted	ADC0809CCN		
Package Outline		N28A Molded DIP	J28A Hermetic DIP	J28A Hermetic DIP

National Semiconductor

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

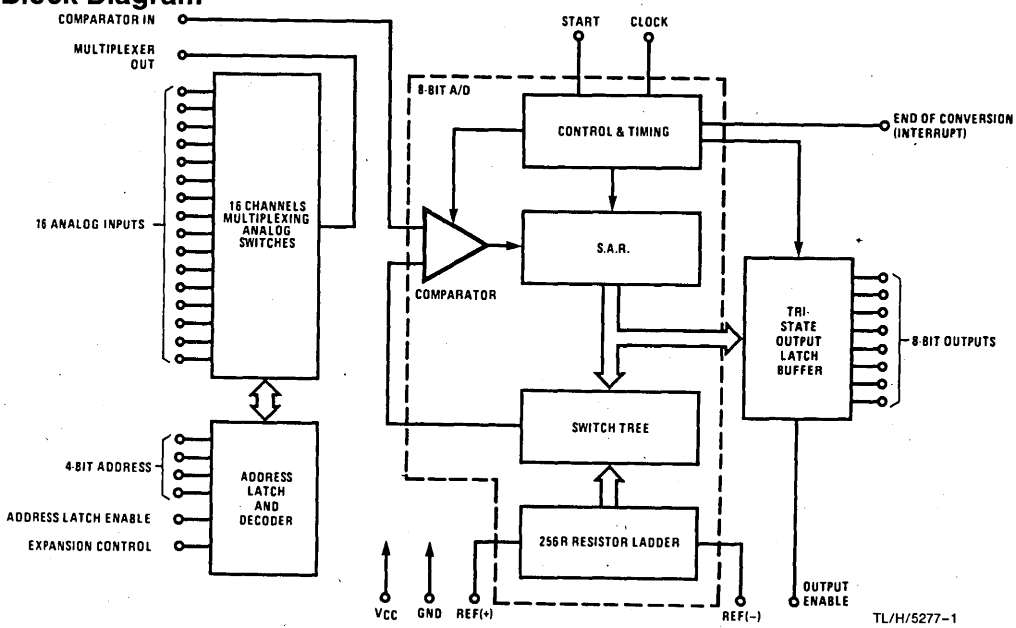
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

Features

- Resolution—8-bits
- Total unadjusted error—$\pm\frac{1}{2}$ LSB and $\pm$ 1 LSB
- No missing codes
- Conversion time—100 μS
- Single supply—5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption—15 mW
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC} (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	$-0.3V$ to $(V_{CC}+0.3V)$
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	$-0.3V$ to 15V
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0816CJ	$-55°C \leq T_A + 125°C$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	$-40°C \leq T_A \leq +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: $V_{CC}=5\ V_{DC}=V_{REF(+)}$, $V_{REF(-)}=GND$, $V_{IN}=V_{COMPARATOR\ IN}$, $T_{MIN} \leq T_{MAX}$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter		Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			$\pm 1/2$ $\pm 3/4$	LSB LSB
	ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			± 1 $\pm 1\frac{1}{4}$	LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4)V(+) or V(−)	GND−0.10		$V_{CC}+0.10$	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	$f_c=640$ kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_A \leq +125°C$ unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN $4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) $T_A=25°C$, $R_L=10k$ $T_A=85°C$ $T_A=125°C$		1.5	3 6 9	kΩ kΩ kΩ
ΔR_{ON}	ΔON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L=10k$		75		Ω
I_{OFF+}	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=5V$, $T_A=25°C$ T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=0$, $T_A=25°C$ T_{MIN} to T_{Max}	−200 −1.0			nA μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	−1.0			μA
I_{CC}	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ—4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted. ADC0816CCJ, ADC0816CCN, ADC0817CCN—4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O −360 μA, T_A = 85°C I_O = −300 μA, T_A = 125°C	V_{CC} − 0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	V_O = V_{CC} V_O = 0	 −3.0		3.0	μA μA

Electrical Characteristics

Timing Specifications: V_{CC} = $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = GND, t_r = t_f = 20 ns and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)* (Note 7)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time from ALE	R_S = 0Ω *(Figure 5)*		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L = 50 pF, R_L = 10k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L = 10 pF, R_L = 10k *(Figure 8)*		125	250	ns
t_C	Conversion Time	f_c = 640 kHz, *(Figure 5)* (Note 8)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs (Note 8)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3.* None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13.*

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: If start pulse is asynchronous with converter clock the minimum start pulse width is 8 clock periods plus 2 μS.

Note 8: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1

Selected Analog Channel	Address Line D	C	B	A	Expansion Control
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

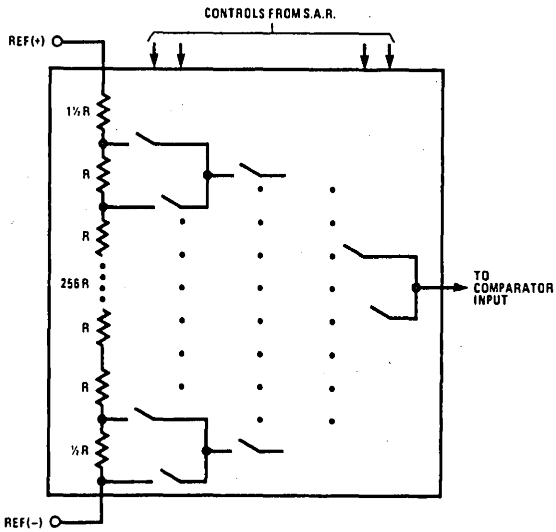
CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + ½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.



TL/H/5277-2

FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

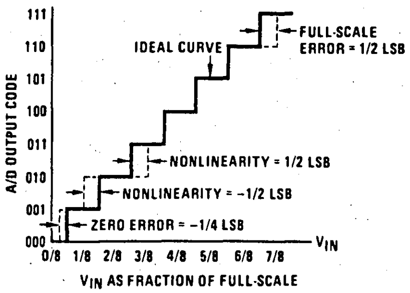
The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ulimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

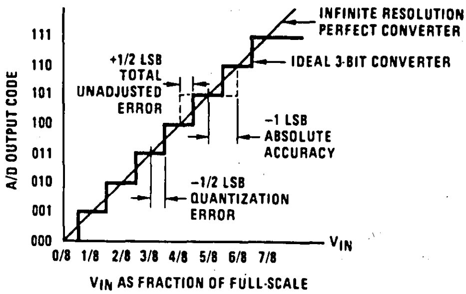
The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.



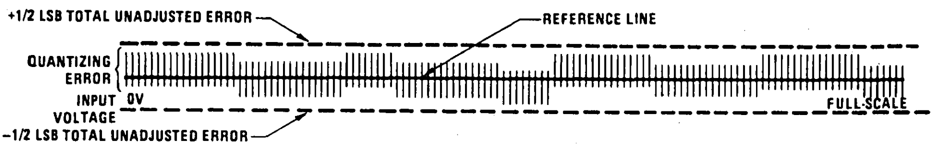
TL/H/5277-3

FIGURE 2. 3-Bit A/D Transfer Curve



TL/H/5277-4

FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

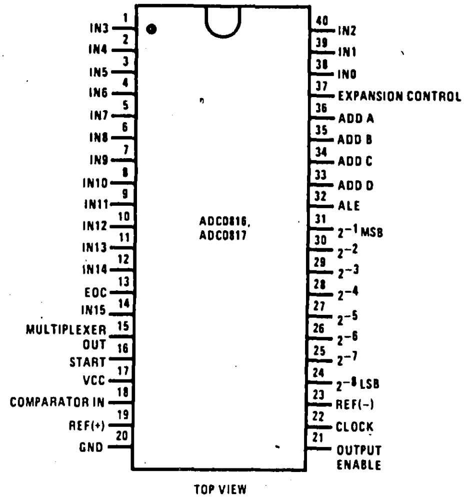


TL/H/5277-5

FIGURE 4. Typical Error Curve

Connection Diagram

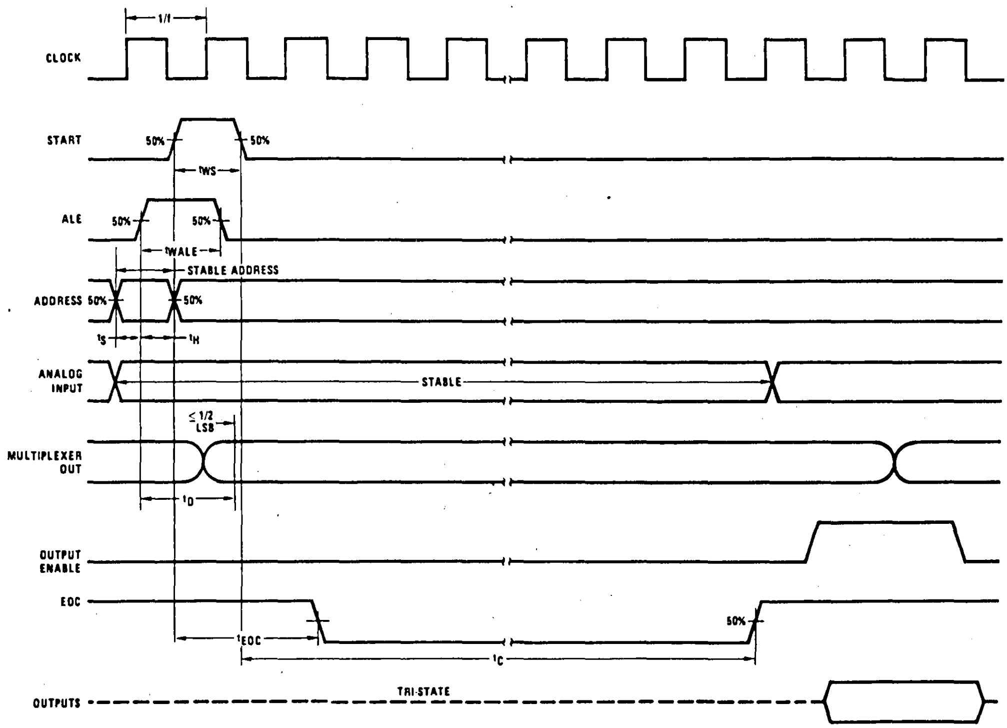
Dual-In-Package



TL/H/5277-6

See Ordering Information

Timing Diagram



TL/H/5277-7

FIGURE 5

Typical Performance Characteristics

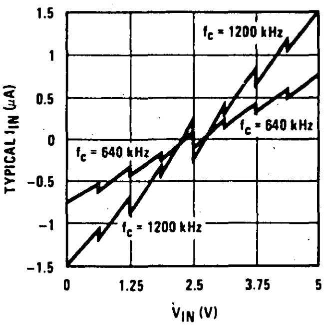
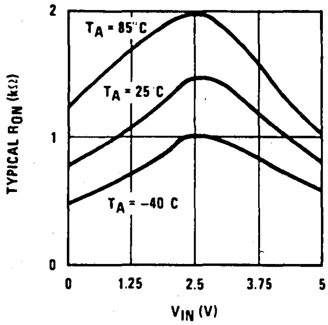


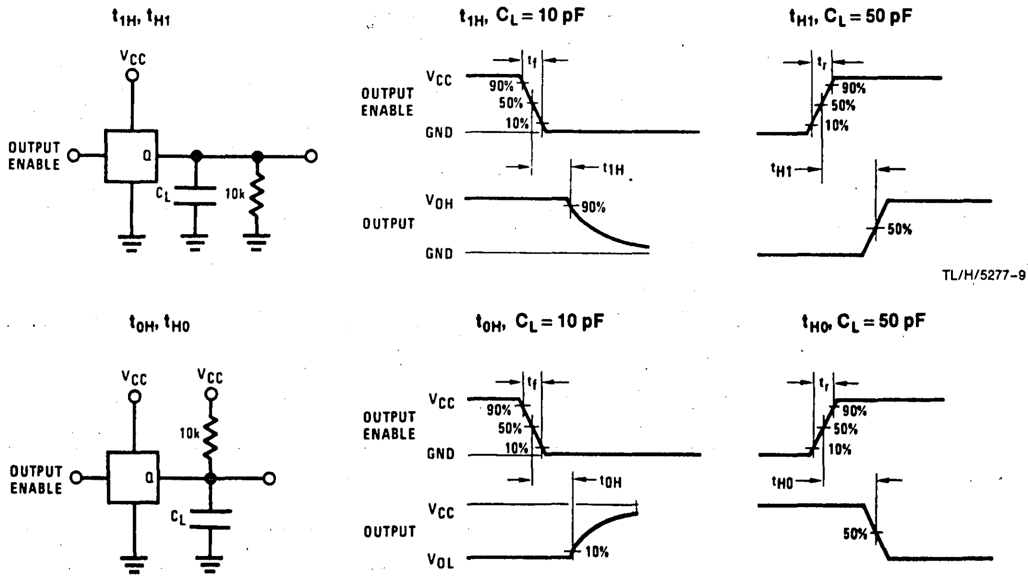
FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)



TL/H/5277-8

FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE Test Circuits and Timing Diagrams



TL/H/5277-9

TL/H/5277-10

FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches These limitations are automaticaly satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

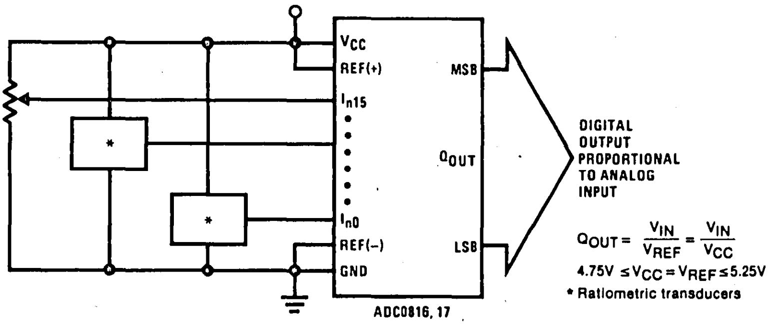


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground references system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the millliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.

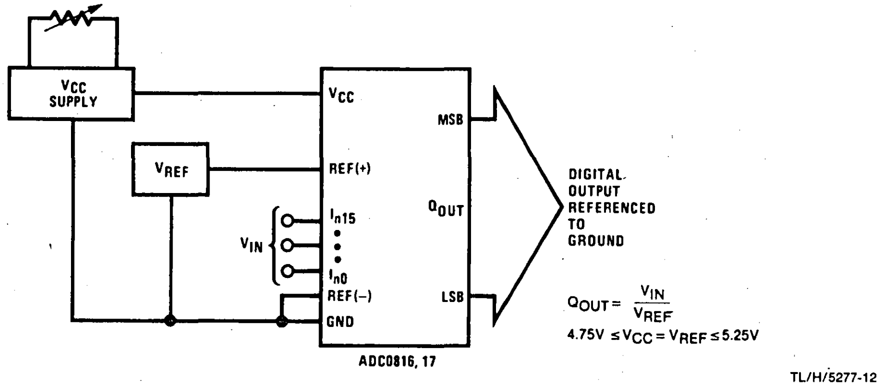


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

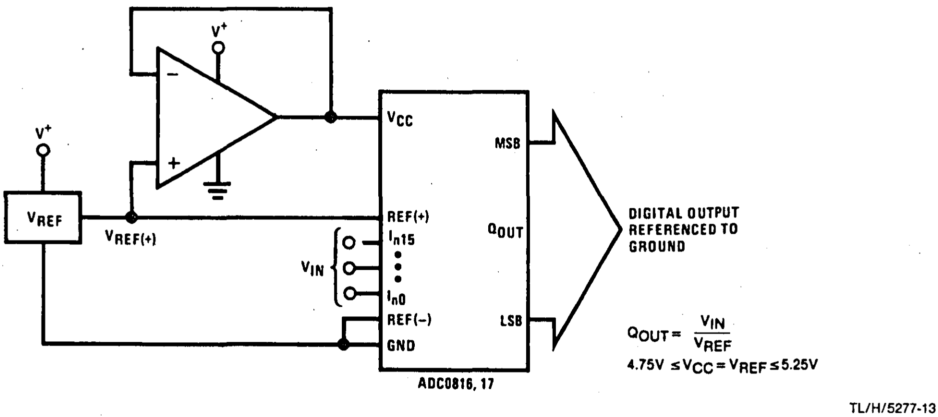


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

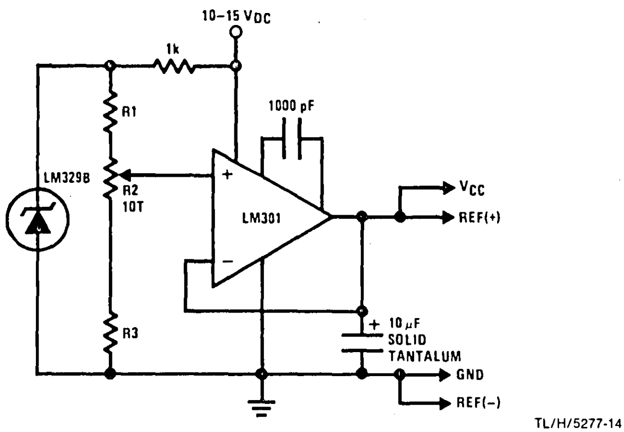


FIGURE 12. Typical Reference and Supply Circuit

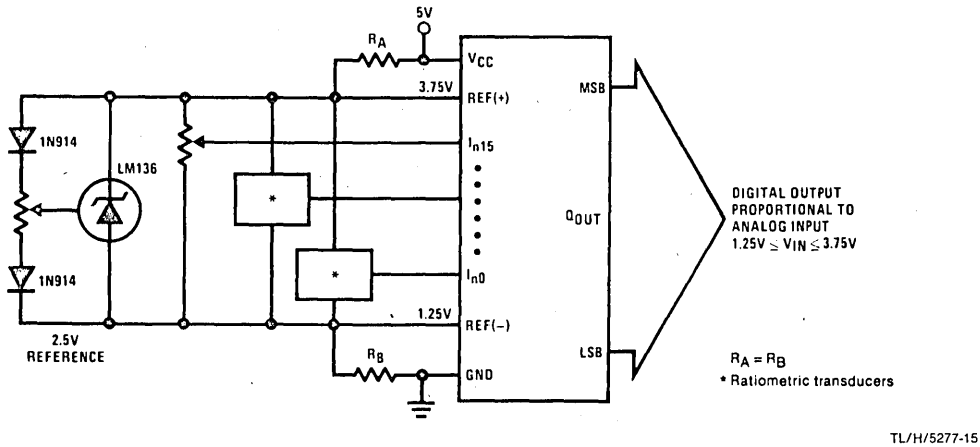


FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \qquad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right] + V_{REF(-)} \qquad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \qquad (4)$$

where: V_{IN} = Voltage at comparator input

V_{REF} = Voltage at Ref(+)

V_{REF} = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF}(+) \div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

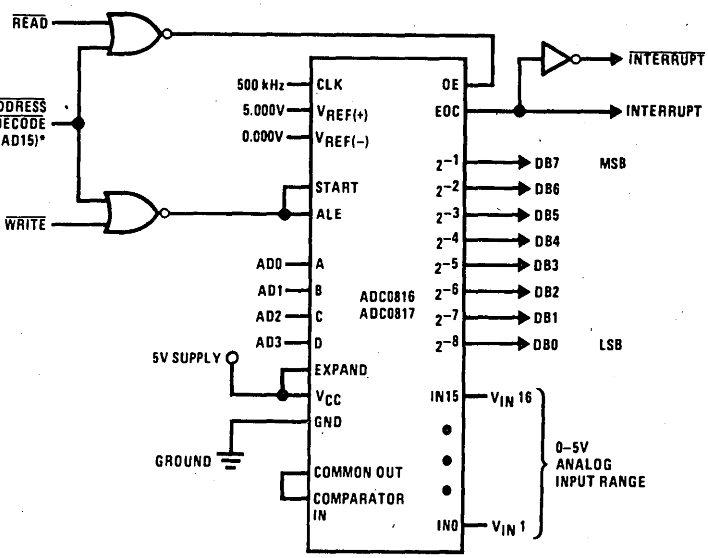
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application



TL/H/5277-16

*Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ 2•R/W	VMA•Q_2•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to + 125°C
Error	±½ Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	±1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

National Semiconductor

microCMOS

ADC0820 8-Bit High Speed µP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 µs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/µs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

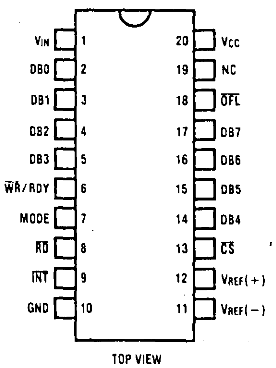
- Resolution — 8 Bits
- Conversion Time — 2.5 µs Max (RD Mode); 1.5 µs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/µs converted without external sample-and-hold to 8 bits
- Low Power — 75 mW Max
- Total Unadjusted Error — ± ½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3″ standard width 20-pin DIP

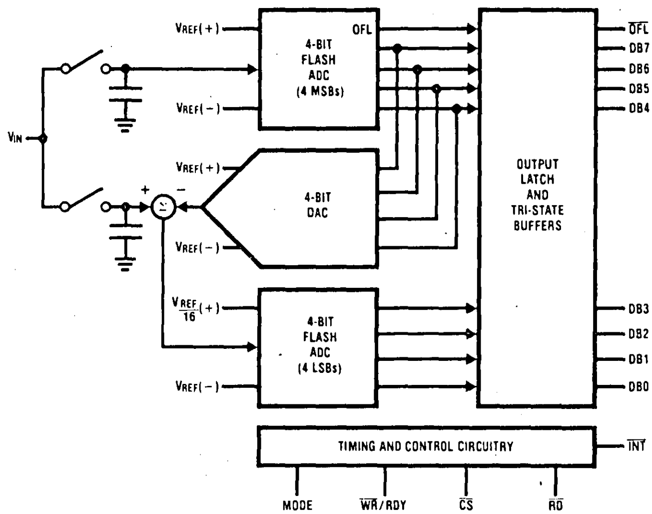
Connection Diagram

Dual-In-Line



TL/H/5501-1

Functional Diagram



TL/H/5501-2

FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	10V
Logic Control Inputs	−0.2V to V_{CC} +0.2V
Voltage at Other Inputs and Output	−0.2V to V_{CC} +0.2V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0820BD, ADC0820CD	$-55°C \le T_A \le +125°C$
ADC0820BCD, ADC0820CCD	$-40°C \le T_A \le +85°C$
ADC0820BCN, ADC0820CCN	$0°C \le T_A \le 70°C$
V_{CC} Range	4.5V to 8V

Converter Characteristics

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = 5V, $V_{REF}(+)$ = 5V, and $V_{REF}(-)$ = GND unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	ADC0820BD, ADC0820CD ADC0820BCD, ADC0820CCD Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	ADC0820BCN, ADC0820CCN Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Limit Units
Resolution			**8**			8	**8**	Bits
Total Unadjusted Error (Note 3)	ADC0820BD, BCD		**±½**					LSB
	ADC0820BCN					±½	**±½**	LSB
	ADC0820CD, CCD		**±1**					LSB
	ADC0820CCN					±1	**±1**	LSB
Minimum Reference Resistance		2.3	**1.25**		2.3	1.4	**1.25**	kΩ
Maximum Reference Resistance		2.3	**6**		2.3	5.3	**6**	kΩ
Maximum $V_{REF}(+)$ Input Voltage			**V_{CC}**			V_{CC}	**V_{CC}**	V
Minimum $V_{REF}(-)$ Input Voltage			**GND**			GND	**GND**	V
Minimum $V_{REF}(+)$ Input Voltage			**$V_{REF}(-)$**			$V_{REF}(-)$	**$V_{REF}(-)$**	V
Maximum $V_{REF}(-)$ Input Voltage			**$V_{REF}(+)$**			$V_{REF}(+)$	**$V_{REF}(+)$**	V
Maximum V_{IN} Input Voltage			**V_{CC}+0.1**			V_{CC}+0.1	**V_{CC}+0.1**	V
Minimum V_{IN} Input Voltage			**GND−0.1**			GND−0.1	**GND−0.1**	V
Maximum Analog Input Leakage Current	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC}		**3**			0.3	**3**	μA
	V_{IN} = GND		**−3**			−0.3	**−3**	μA
Power Supply Sensitivity	V_{CC} = 5V ± 5%	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB

Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	−55°C to +125°C
Error	±1/2 LSB Unadjusted	ADC0820BCN	ADC0820BCD	ADC0820BD
	±1 LSB Unadjusted	ADC0820CCN	ADC0820CCD	ADC0820CD
Package Outline		N20A—Molded DIP	D20A—Cavity DIP	D20A—Cavity DIP

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A=T_J=25°C$.

Parameter	Conditions		ADC0820BD, ADC0820CD ADC0820BCD, ADC0820CCD Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	ADC0820BCN, ADC0820CCN Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Limit Units
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC}=5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**2.0**			2.0	**2.0**	V
		Mode		**3.5**			3.5	**3.5**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC}=4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**0.8**			0.8	**0.8**	V
		Mode		**1.5**			1.5	**1.5**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)}=5V$; $\overline{CS}$, $\overline{RD}$		0.005	**1**		0.005		**1**	µA
	$V_{IN(1)}=5V$; $\overline{WR}$		0.1	**3**		0.1	0.3	**3**	µA
	$V_{IN(1)}=5V$; Mode		50	**200**		50	170	**200**	µA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)}=0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	**−1**		−0.005		**−1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC}=4.75V$, $I_{OUT}=-360$ µA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**2.4**			2.8	**2.4**	V
	$V_{CC}=4.75V$, $I_{OUT}=-10$ µA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$V_{CC}=4.75V$, $I_{OUT}=1.6$ mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current	$V_{OUT}=5V$; DB0–DB7, RDY		0.1	**3**		0.1	0.3	**3**	µA
	$V_{OUT}=0V$; DB0–DB7, RDY		−0.1	**−3**		−0.1	−0.3	**−3**	µA
I_{SOURCE}, Output Source Current	$V_{OUT}=0V$; DB0–DB7, $\overline{OFL}$		−12	**−6**		−12	−7.2	**−6**	mA
	$\overline{INT}$		−9	**−4.5**		−9	−5.3	**−4.5**	mA
I_{SINK}, Output Sink Current	$V_{OUT}=5V$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	**7**		14	8.4	**7**	mA
I_{CC}, Supply Current	$\overline{CS}=\overline{WR}=\overline{RD}=0$		7.5	**15**		7.5	13	**15**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0, *Figure 2*	1.6		2.5	µs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0, *Figure 2*	$t_{CRD}+20$		$t_{CRD}+50$	ns
t_{CWR-RD}, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; t_{WR} = 600 ns, $t_{RD}=600$ ns; *Figures 3a* and *3b*			1.52	µs
t_{WR}, Write Time	Min	Pin 7 = V_{CC}; *Figures 3a* and *3b*		600		ns
	Max	(Note 4) See Graph	50			µs
t_{RD}, Read Time	Min	Pin 7 = V_{CC}; *Figures 3a* and *3b* (Note 4) See Graph		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD}<t_I$; *Figure 3a* $C_L=15$ pF	190		280	ns
		$C_L=100$ pF	210		320	ns
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD}>t_I$; *Figure 3b* $C_L=15$ pF	70		120	ns
		$C_L=100$ pF	90		150	ns

AC Electrical Characteristics (Continued) The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_I, Internal Comparison Time	Pin 7 = V_{CC}; *Figures 3b* and *4* $C_L=50$ pF	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L=1k$, $C_L=10$ pF	100		200	ns
t_{INTL}, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = V_{CC}, $C_L=50$ pF $t_{RD}>t_I$; *Figure 3b* $t_{RD}<t_I$; *Figure 3a*	 $t_{RD}+200$		 t_I $t_{RD}+290$	 ns ns
t_{INTH}, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	*Figures 2, 3a* and *3b* $C_L=50$ pF	125		225	ns
t_{INTHWR}, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	*Figure 4*, $C_L=50$ pF	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY	*Figure 2*, $C_L=50$ pF, Pin 7 = 0	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid	*Figure 4*	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7 = V_{CC}, $t_{RD}<t_I$ *Figure 3a*	200		290	ns
t_P, Delay from End of Conversion to Next Conversion	*Figures 2, 3a, 3b* and *4* (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/μs
C_{VIN}, Analog Input Capacitance		45			pF
C_{OUT}, Logic Output Capacitance		5			pF
C_{IN}, Logic Input Capacitance		5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RP} graphs.

Note 5: The voltage at these pins should never go higher than V_{CC} nor lower than GND.

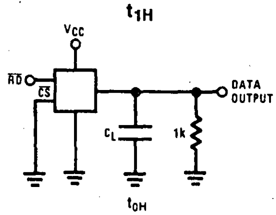
Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

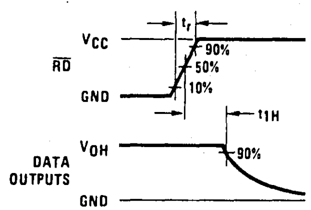
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/5501-3

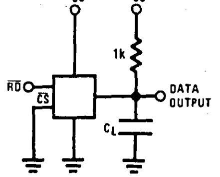
t_{1H}, $C_L=10$ pF



$t_r=20$ ns

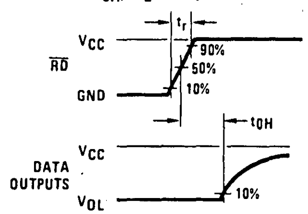
TL/H/5501-4

t_{0H}



TL/H/5501-5

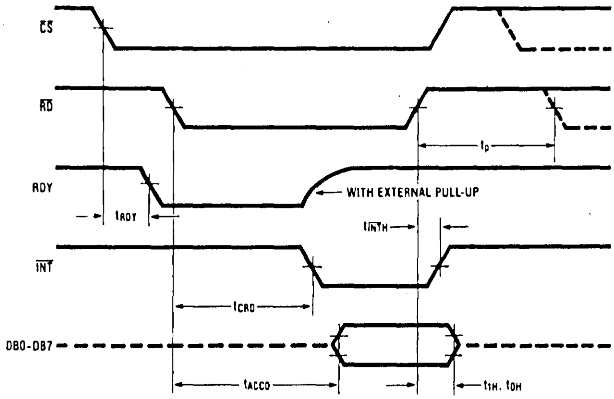
t_{0H}, $C_L=10$ pF



$t_r=20$ ns

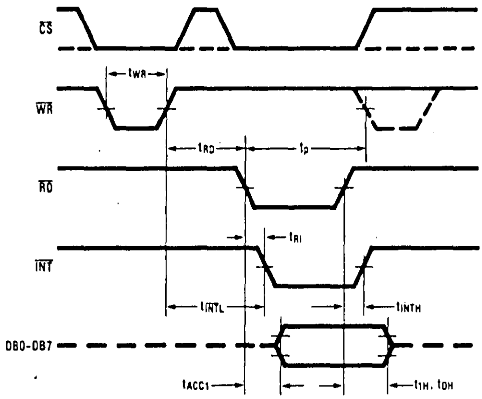
TL/H/5501-6

Timing Diagrams



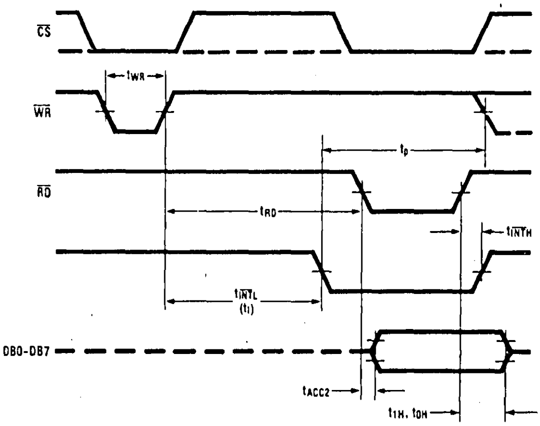
TL/H/5501-7

FIGURE 2. RD Mode (Pin 7 is Low)



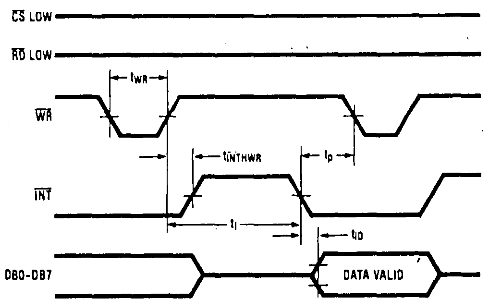
TL/H/5501-8

FIGURE 3a. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)



TL/H/5501-9

FIGURE 3b. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)



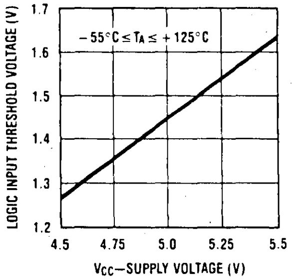
TL/H/5501-10

FIGURE 4. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

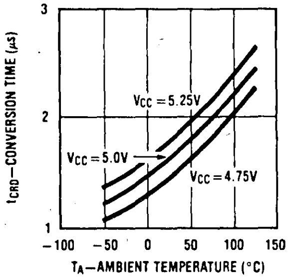
6

Typical Performance Characteristics

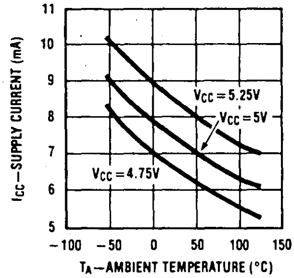
Logic Input Threshold Voltage vs Supply Voltage



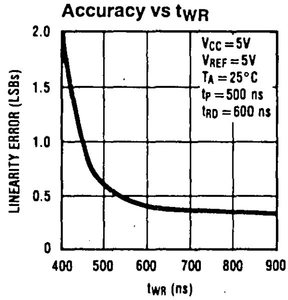
Conversion Time (RD Mode) vs Temperature



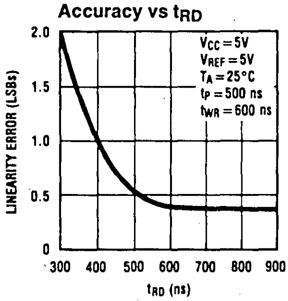
Power Supply Current vs Temperature (not including reference ladder)



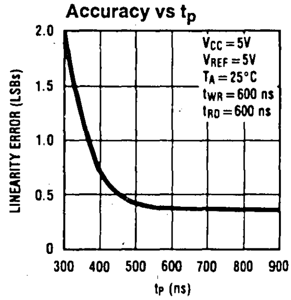
Accuracy vs t_{WR}



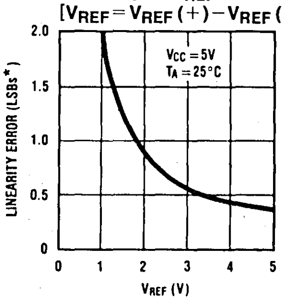
Accuracy vs t_{RD}



Accuracy vs t_P

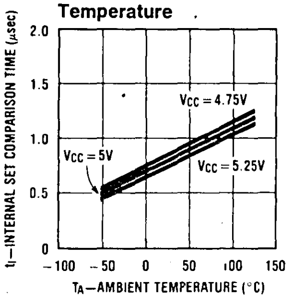


Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]

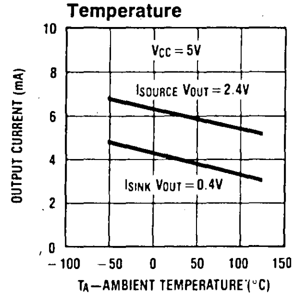


*1 LSB = $\frac{V_{REF}}{256}$

t_I, Internal Time Delay vs Temperature



Output Current vs Temperature



TL/H/5501-11

Description of Pin Functions

Pin	Name	Function
1	V_{IN}	Analog input; range $= GND \le V_{IN} \le V_{CC}$
2	DB0	TRI-STATE data output—bit 0 (LSB)
3	DB1	TRI-STATE data output—bit 1
4	DB2	TRI-STATE data output—bit 2
5	DB3	TRI-STATE data output—bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** **$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800 ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see *Figures 3a* and *3b*). **RD Mode** **RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see *Figure 2*).
7	Mode	**Mode:** Mode selection input—it is internally tied to GND through a 50 μA current source. **RD Mode:** When mode is low **WR-RD Mode:** When mode is high
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ low, the TRI-STATE data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes low (see *Figure 4*). $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_I, ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see *Figures 3a* and *3b*). **RD Mode** With $\overline{CS}$ low, the conversion will start with $\overline{RD}$ going low, also $\overline{RD}$ will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and $\overline{INT}$ going low indicates the completion of the conversion (see *Figure 2*).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go low, ~800 ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see *Figure 3b*); or $\overline{INT}$ will go low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes low prior to the 800 ns time out (see *Figure 3a*). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figures 3a* and *3b*). **RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figure 2*).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \le V_{REF}(-) \le V_{REF}(+)$ (Note 5)
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \le V_{REF}(+) \le V_{CC}$ (Note 5)
13	$\overline{CS}$	$\overline{CS}$ must be low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	TRI-STATE data output—bit 4
15	DB5	TRI-STATE data output—bit 5
16	DB6	TRI-STATE data output—bit 6
17	DB7	TRI-STATE data output—bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—If the analog input is higher than the $V_{REF}(+)$, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit).
19	NC	No connection
20	V_{CC}	Power supply voltage

1.0 Functional Description

1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (*Figure 1*). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled-data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

1.2 THE SAMPLED-DATA COMPARATOR

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (*Figure 5*). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (*Figure 5a*) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_B, approximately 1.2V). In the second cycle (*Figure 5b*), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_B') becomes

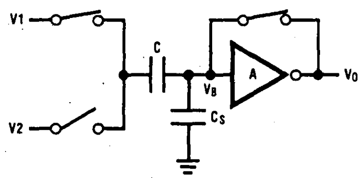
$$V_B - (V1 - V2)\frac{C}{C + C_S}$$

and the output will go high or low depending on the sign of $V_B' - V_B$.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (*Figure 6*), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (*Figure 7*). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.



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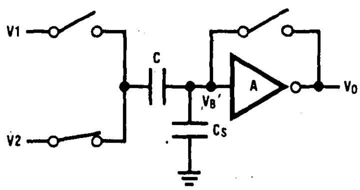
- $V_O = V_B$
- V on C $= V1 - V_B$
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

FIGURE 5a. Zeroing Phase



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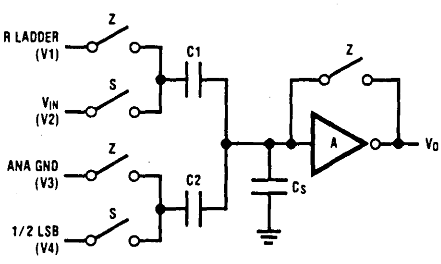
- $V_B' - V_B = (V2 - V1)\frac{C}{C + C_S}$
- $V_O' = \frac{-A}{C + C_S}[CV2 - CV1]$
- V_O' is dependent on $V2 - V1$

FIGURE 5b. Compare Phase

FIGURE 5. Sampled-Data Comparator



$$V_O = \frac{-A}{C1 + C2 + C_S}[C1(V2 - V1) + C2(V4 - V3)]$$
$$= \frac{-A}{C1 + C2 + C_S}[\Delta Q_{C1} + \Delta Q_{C2}]$$

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FIGURE 6. ADC0820 Comparator (from MS Flash ADC)

Detailed Block Diagram

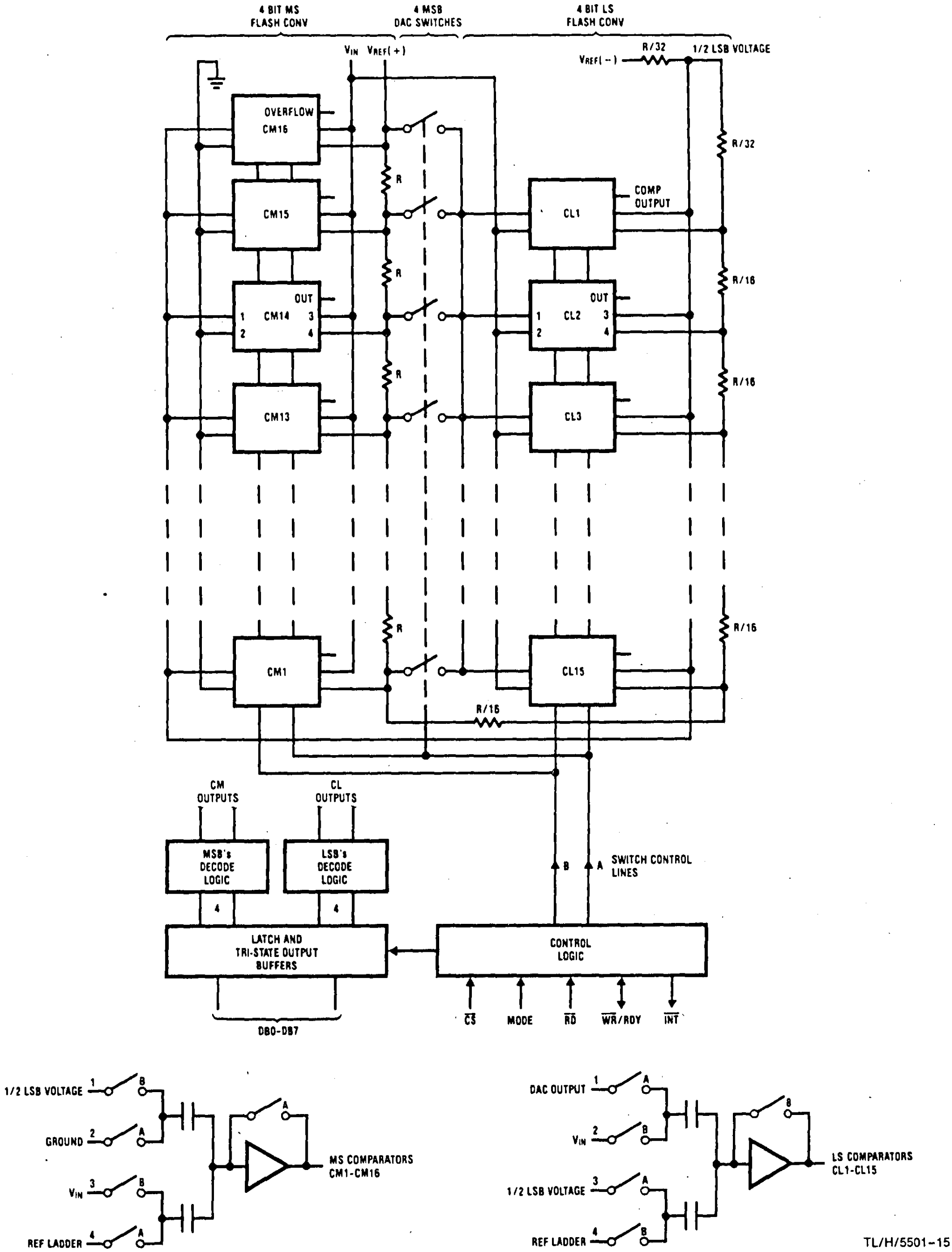

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FIGURE 7

When a typical conversion is started, the $\overline{WR}$ line is brought low. At this instant the MS comparators go from zeroing to comparison mode (*Figure 8*). When $\overline{WR}$ is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the $\overline{RD}$ line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When $\overline{RD}$ goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is low. In RD mode, sampling occurs during the first 800 ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

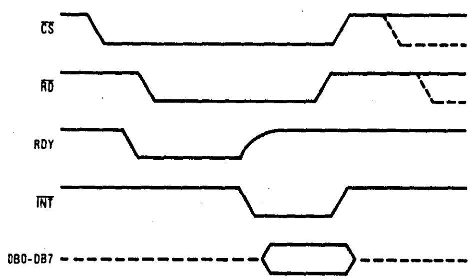
1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ low until output data appears. An $\overline{INT}$ line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

RD Mode (Pin 7 Is Low)



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When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for $\overline{INT}$ to go low before reading the conversion result (*Figure B*). $\overline{INT}$ will typically go low 800 ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 600 ns (*Figure A*). If this is done, $\overline{INT}$ will immediately go low and data will appear at the outputs.

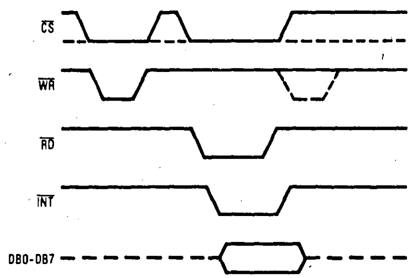

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FIGURE A. WR-RD Mode (Pin 7 Is High and $t_{RD} < t_I$)

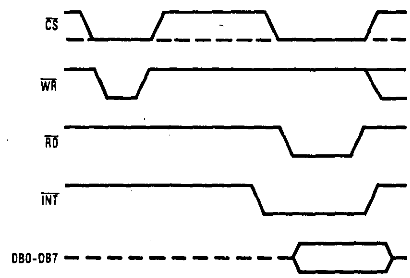

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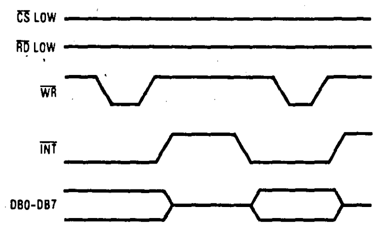
FIGURE B. WR-RD Mode (Pin 7 Is High and $t_{RD} > t_I$)

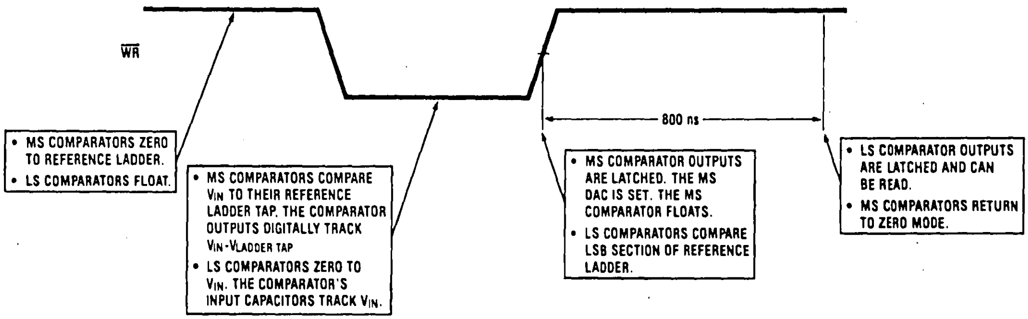
Stand-Alone

For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800 ns following $\overline{WR}$'s rising edge.

WR-RD Mode (Pin 7 Is High) Stand-Alone Operation



TL/H/5501-19



Note: MS means most significant
LS means least significant

FIGURE 8. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50 μs. When the MS flash ADC's sampled-data comparators (Section 1.2) are in comparison mode ($\overline{WR}$ is low), the input capacitors (C, *Figure 6*) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_P, *Figures 2, 3a, 3b,* and *4*) is 500 ns.

2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF}=V_{REF}(+)-V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF}=2V$ then 1 LSB=7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. *Figure 9* shows some of the configurations that are possible.

2.2 INPUT CURRENT

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in *Figure 10a*. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in *Figure 10b*. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be 1.5 kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

6

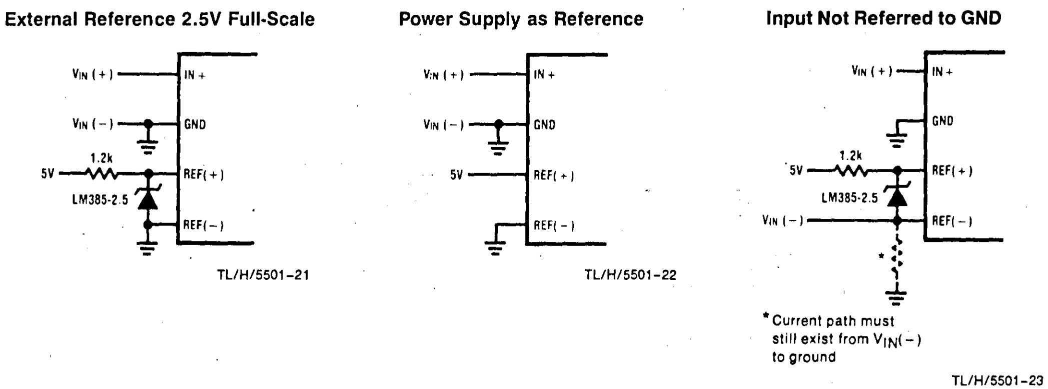


FIGURE 9. Analog Input Options

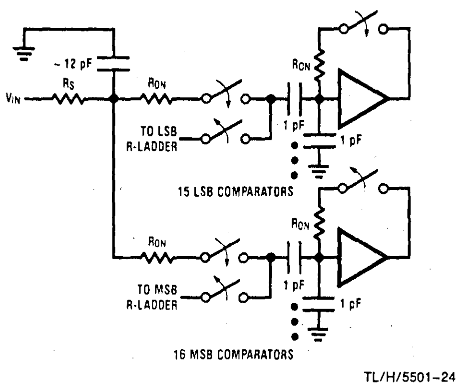


FIGURE 10a

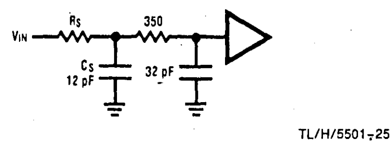


FIGURE 10b

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

2.4 INHERENT SAMPLE-HOLD

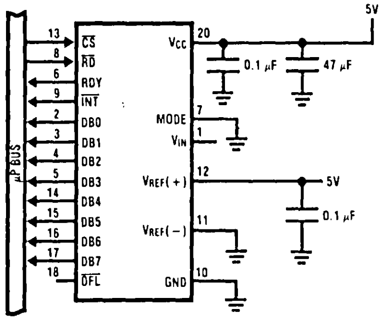
Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 μs, the time through which V_{IN} must be 1/2 LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of $\overline{WR}$ (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 μs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.

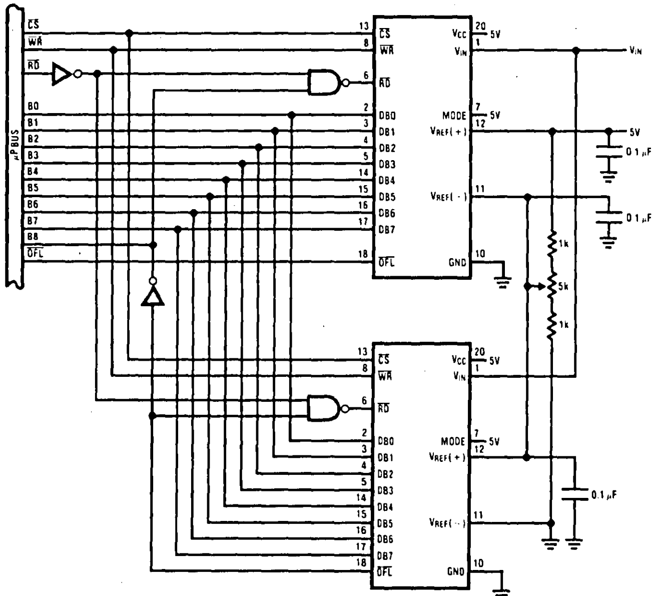
3.0 Typical Applications

8-Bit Resolution Configuration



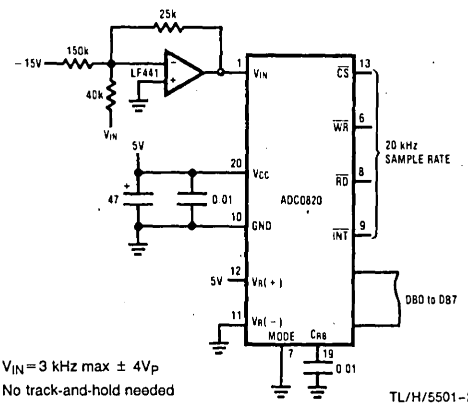
TL/H/5501-26

9-Bit Resolution Configuration



TL/H/5501-27

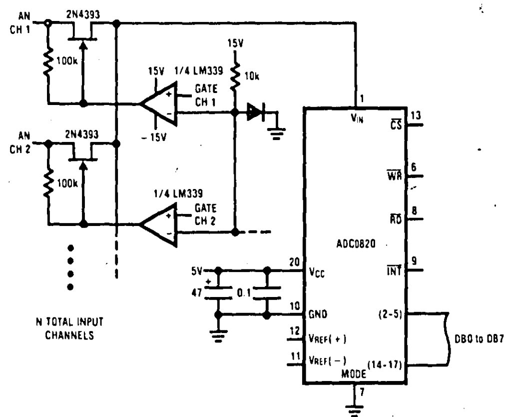
Telecom A/D Converter



- V_{IN} = 3 kHz max ± $4V_P$
- No track-and-hold needed
- Low power consumption

TL/H/5501-28

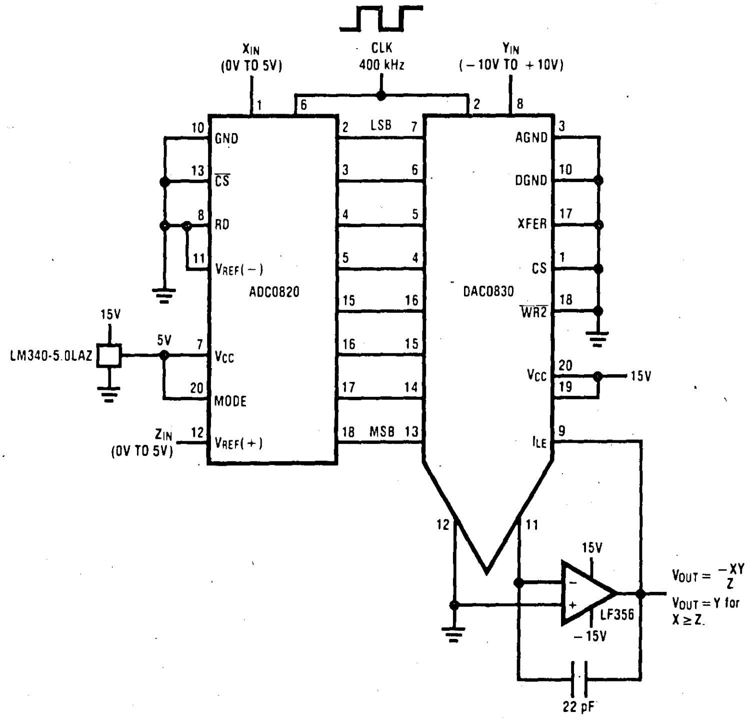
Multiple Input Channels



TL/H/5501-29

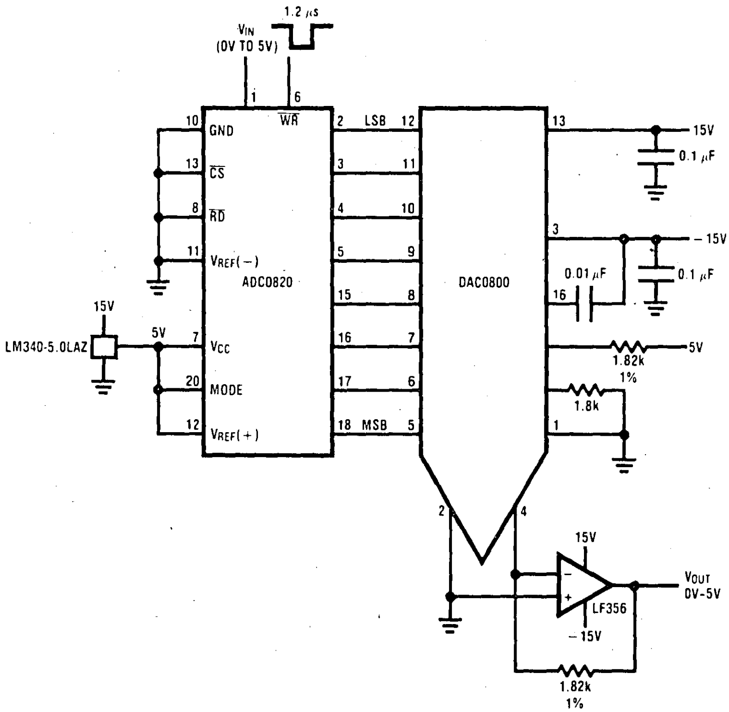
3.0 Typical Applications (Continued)

8-Bit 2-Quadrant Analog Multiplier



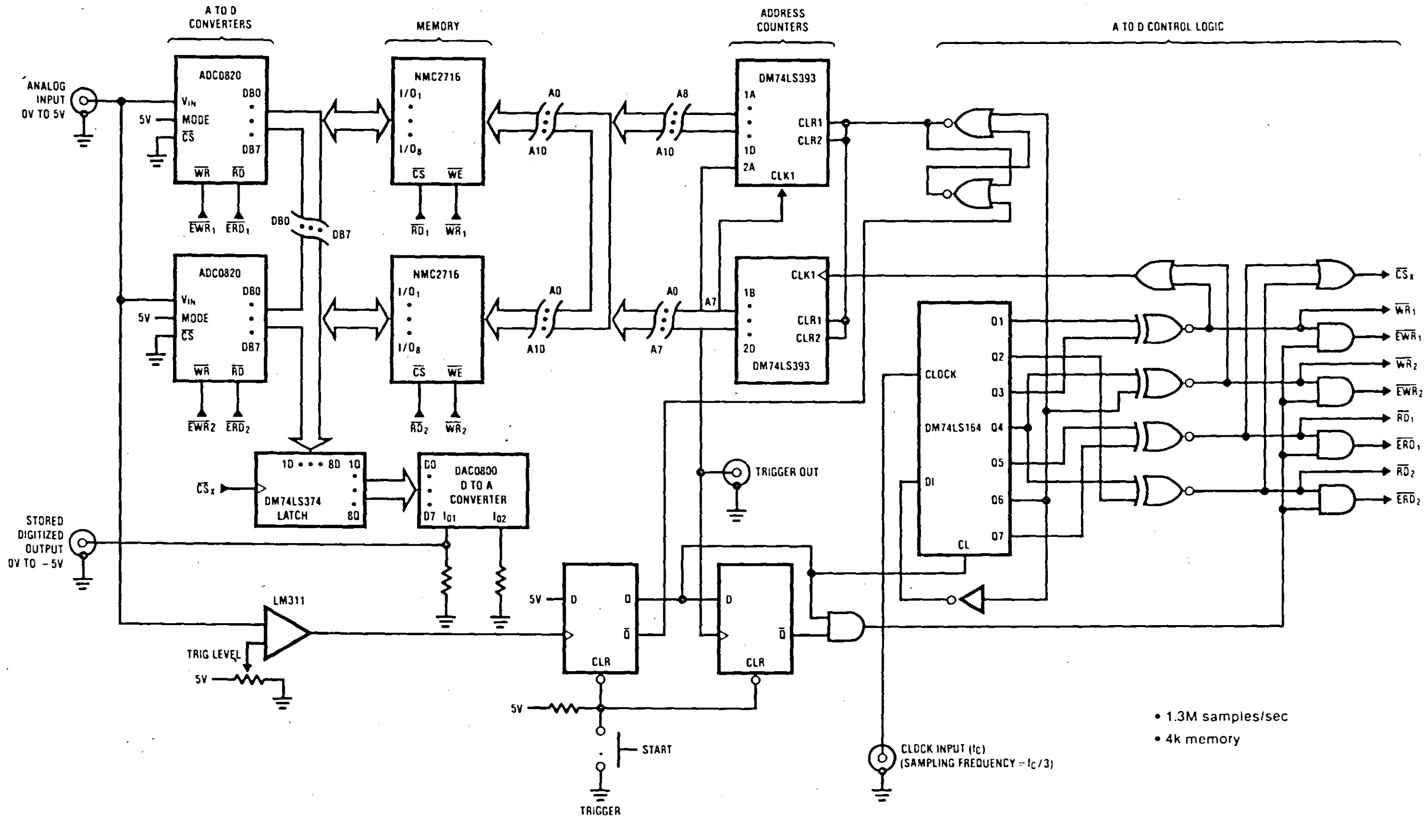
TL/H/5501-30

Fast Infinite Sample-and-Hold



TL/H/5501-31

Digital Waveform Recorder



- 1.3M samples/sec
- 4k memory

TL/H/5501–32

National Semiconductor

ADC0829 μP Compatible 8-Bit A/D with 11-Channel MUX/Digital Input

General Description

The ADC0829 is an 8-bit successive approximation A/D converter with an 11-channel multiplexer of which six can be used as digital inputs, as well as, analog inputs.

This A/D is designed to operate from the μP data bus using a single 5V supply.

Channel selection, conversion control, software configuration and bus interface logic are all contained on this monolithic CMOS device.

This device contains three 16-bit registers which are accessed via double byte instructions. The control register is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 8-bit I/O port as input or output, and provides information for the 8-bit output register.

The conversion results register is a read only register which contains the current status and most recent conversion results. The discrete input register is also a read only register which contains the four address bits of the selected channel, and the six discrete inputs which are connected to the analog multiplexer.

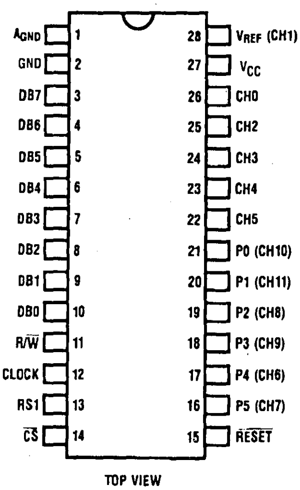
Key Specification

- Resolution — 8 Bits
- Total Unadjusted Error — ±½ LSB and ±1 LSB
- Conversion Time — 256 μS
- Single Supply — $5V_{DC}$
- Low Power — 50 mW

Features

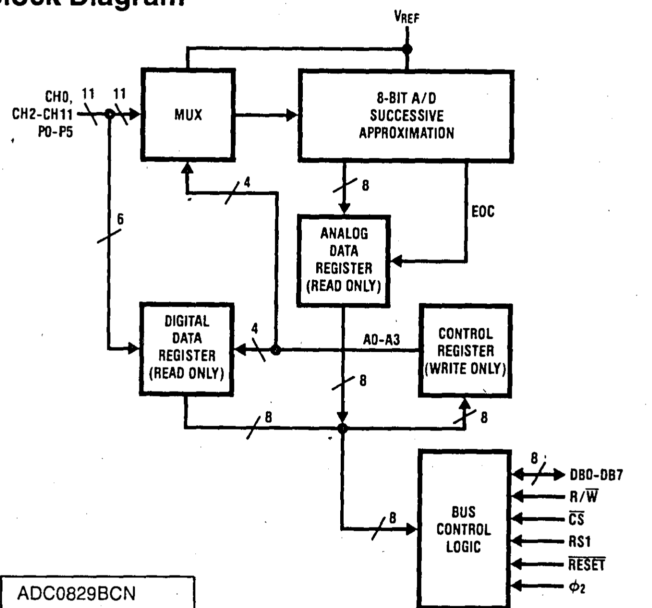
- No missing codes
- Operates ratiometrically or with analog span adjusted voltage reference
- 11-Channel multiplexer with latched control logic of which six can be used as digital inputs
- Easy interface to all microprocessors or operates "stand alone"
- 0 to 5V analog input range with single 5V supply
- T^2 L/MOS input/output compatible
- No zero or full scale adjusts required
- Standard 28-pin DIP
- Temperature range −40°C to +85°C

Connection Diagram



TL/F/5508-1

Block Diagram



TL/F/5508-2

Ordering Information

Error	± ½ Bit Unadjusted	ADC0829BCN
	± 1 Bit Unadjusted	ADC0829CCN
Package Outline		N28B

Absolute Maximum Ratings

(Notes 1 and 2)

Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	$-0.3V$ to V_{CC} + 0.3V
Analog Inputs	$-0.3V$ to V_{CC} + 0.3V
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	
Lead Temperature (Soldering, 10 seconds)	300°C
Input Current Per Pin	±5 mA
Package	+20 mA

Operating Ratings (Notes 1 and 2)

Supply Voltage, V_{CC}	4.75 V_{DC} to 5.5 V_{DC}
Temperature Range	−40°C to + 85°C

Converter and Multiplexer Electrical Characteristics

V_{CC} = 5V_{DC} = $V_{REF}(+)$, $V_{REF}(-)$ = GND, SCLK ϕ_2 = 1.048 MHz, −40°C ≤ T_A + 85°C unless otherwise noted.

Parameter	Conditions		Min	Typ (Notes)	Max	Units
Total Unadjusted Error; (Note 3)						
ADC0829BCN	V_{REF} Forced to 5.000 V_{DC}				±½	LSB
ADC0829CCN	V_{REF} Forced to 5.000 V_{DC}				±1	LSB
Reference Input Resistance			1.0	4.5		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)		GND-0.10		V_{CC}+0.10	V
$V_{REF}(+)$ Voltage, Top of Ladder	Measured at REF(+)			V_{CC}	V_{CC}+0.01	V
$\frac{V_{REF}(+) + V_{REF}(-)}{2}$ Voltage, Center of Ladder			$V_{CC/2}$−0.1	$V_{CC/2}$	$V_{CC/2}$+0.01	V
$V_{REF}(-)$ Voltage, Bottom of Ladder	Measured at REF(−)		−0.1	0		V
I_{OFF}, Off Channel Leakage Current (Note 6)	ON Channel = 5V	ADC0829BCN			±400	nA
	OFF Channel = 0V	ADC0829CCN			±1	μA
I_{ON}, On Channel Leakage Current (Note 6)	ON Channel = 0V	ADC0829BCN			±400	nA
	OFF Channel = 5V	ADC0829CCN			±1	μA

AC Characteristics

V_{CC} = $V_{REF}(+)$ = 5V, t_r = t_f = 20 ns and T_A = 25°C (Note 7) unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
$t_{CYC}(\phi_2)$, ϕ_2 Clock Cycle Time ($1/f_{\phi 2}$)		0.943		10.0	μs
$PW_H(\phi_2)$, ϕ_2 Clock Pulse Width, High		440			ns
$PW_L(\phi_2)$, ϕ_2 Clock Pulse Width, Low		410			ns
$t_r(\phi_2)$, ϕ_2 Rise Time				25	ns
$t_f(\phi_2)$, ϕ_2 Fall Time				30	ns
t_{AS}, Address Set Up Time	RS1, R/$\overline{W}$, $\overline{CS}$	145			ns
t_{DDR}, Data Delay (Read)	DB0-DB7			335	ns
t_{DSW}, Data Delay Setup (Write)	DB0-DB7	185			ns
t_{AH}, Address Hold Time	RS1, R/$\overline{W}$, $\overline{CE}$	20			ns
t_{DHW}, Input Data Hold Time	DB0-DB7	20			ns
t_{DHR}, Output Data Hold Time	DB0-DB7	10			ns
Analog Channel Settling Time		32			Clocks
t_c, Conversion Time		256			Clocks

6

Digital and DC Characteristics V_{CC} = 4.5V to 5.5V and $-40°C \le T_A \le 85°C$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Bus Control Inputs (R/$\overline{W}$, ENABLE $\overline{RESET}$, RS1, $\overline{CS}$) and Peripheral Inputs (P0-P5)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{IN}, Input Leakage Current				±1	μA
ϕ_2 CLOCK INPUT					
$V_{IN}(1)$, Logical "1" Input Voltage		$V_{CC}-0.8$			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.4	V
Data Bus (DB0-DB7)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{OUT}, TRI-STATE® Output Current	V_{OUT} = 0V			−10	μA
	V_{OUT} = 5V			10	μA
$V_{OUT}(1)$, Logical "1" Output Voltage	I_{OUT} = −1.6 mA	2.4			V
$V_{OUT}(0)$, Logical "0" Output Voltage	I_{OUT} = 1.6 mA			0.4	V
Power Supply Requirements					
I_{CC}, Supply Current				10	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

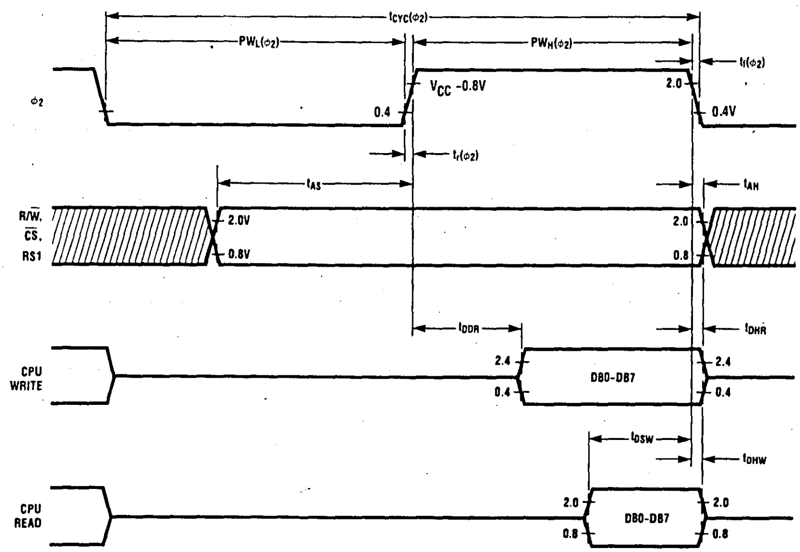
Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.90 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Off channel leakage current is measured after the channel selection.

Note 7: The temperature coefficient is 0.3%/°C.

Timing Diagram



TL/F/5508-3

Pin Description

ANALOG AND DIGITAL INPUTS

CH0, CH2-CH5—These are dedicated analog inputs. They are fed directly to the internal 12 to 1 multiplexer which feeds the A/D converter.

P0-P5/CH6-CH11—These 6 pins are dual purpose and may be used as either TTL compatible digital inputs, or analog inputs. When used as digital inputs they may be read via the discrete input register. When they are used as analog inputs they function like CH-0, CH2-5.

MICROPROCESSOR INTERFACE SIGNALS

DB0-DB7—The bi-directional data lines for the data bus connect to the μP's main data bus to enable data transfer to and from the μP. DB0-DB7 remain in a high impedance state unless the ADC0829 is read.

ϕ_2 Clock—This signal is used for two purposes. First it synchronizes data transfer in and out of the ADC. Second, it is the master clock for the A/D converter logic and all other timing signals are derived from it.

R/$\overline{\text{W}}$—The read/write pin controls the direction of data transfer on D0-D7.

$\overline{\text{RESET}}$—A low on this pin forces the ADC0829 into a known state. The start bit is cleared, Channel CH0 is selected and the internal byte counter is reset to the MS Byte. The A/D data register is not reset. Reset must be held low for at least three clocks.

$\overline{\text{CS}}$—Chip Select must be low in order for data transfer between the ADC0829 and the μP to occur.

RS1—The Register Select pin is used to address the internal registers.

POWER SUPPLY PINS

V_{CC}—This is the positive 5V supply pin. It powers the digital load and the sample data comparator. Care should be exercised to ensure that supply noise on this pin is adequately filtered, by using a bypass capacitor from V_{CC} to D_{GND}.

D_{GND}—Digital ground should be connected to the systems digital ground.

V_{REF} and A_{GND}—The positive reference pin attaches to the top of the 256R resistor ladder and sets the full scale conversion voltage value. The A_{GND} connects to the bottom of the ladder. The conversion result is ratiometric to V_{REF} - A_{GND} and hence both V_{REF} and A_{GND} should be noise free. Ideally the V_{REF} and A_{GND} should be single point connected to the analog transducer's supply. The V_{REF} and A_{GND} voltages typically are 5V and Ground but they may be varied so long as $(V_{REF}\text{-}A_{GND})/2 = V_{CC}/2 \pm 0.1V$.

Functional Description

1.0 CONTROL LOGIC

The Control Logic interprets the microprocessor control signals and decodes these signals to perform the actual functions of selecting, reading, writing, enabling the outputs, etc.

2.0 STATE DESCRIPTIONS

There are three internal states within the A/D converter: the NO OP state; the sample state; and the converting state.

The NO OP state is a stable state since the external stimulus (e.g. start conversion signal) is needed for a state transition.

The first transient state is sampling the input. The first 32 clocks of the conversion are used for acquiring the channel; this settling time allows any transients to decay before conversion begins. The second transient state is the actual conversion. The conversion is completed in 256 clocks and the conversion results register is updated. The converter then returns to the stable NO OP state awaiting further instructions.

The device has no comparator bias current and draws minimal power during the NO OP state.

3.0 INITIALIZATION

The device is initialized by an active low on $\overline{\text{RESET}}$. All outputs are initialized to the inactive state and the converter placed in its NO OP state. The data register is not affected by $\overline{\text{RESET}}$. System TRI-STATE outputs are initialized to the high impedance state.

4.0 CONVERSION CONTROL

The program normally initiates a conversion cycle with a double write command. (See control word format.) The control word selects a channel, configures the peripheral I/O, and provides peripheral data information. The conversion is initiated by setting the SC bit in the control word high.

The converter then resets the start conversion bit and begins the conversion cycle.

When the conversion is complete and the new conversion results transferred to the data register, the status bit is set. The status bit is not reset when the conversion status is read. A full double byte write into the control word will reset the status bit, or a low level at master $\overline{\text{RESET}}$.

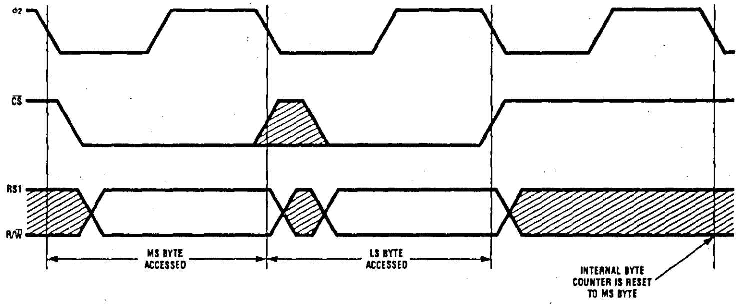
If a new conversion command occurs during a conversion, the conversion is aborted and a new channel acquisition phase will immediately begin.

5.0 CONTROL STRUCTURE

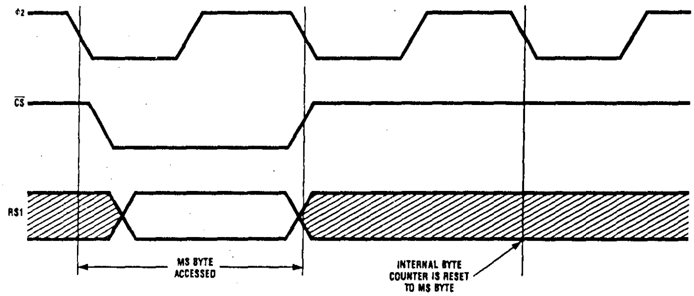
The control logic continually monitors the control bus waiting for $\overline{\text{CS}}$ to go low and ϕ_2 to go high. When this condition occurs, the internal decoder, which has already selected the proper function, activitates.

The byte counter will always select the most significant (MS) half first, and the least significant (LS) half second. Single byte instructions will always access the MSB portion of any word. After a single byte instruction the byte counter will return to the MSB portion of a word when $\overline{\text{CS}}$ is high for a full clock cycle. A 16-bit read or write is accomplished by using a 16-bit load or store instruction which transfers each byte on consecutive clock cycles. This timing is shown in *Figure 1*. A single byte instruction is especially useful for reading the status bit during a polled interrupt. *Figure 2* shows the basic A/D conversion timing sequence and flow.

Functional Description (Continued)

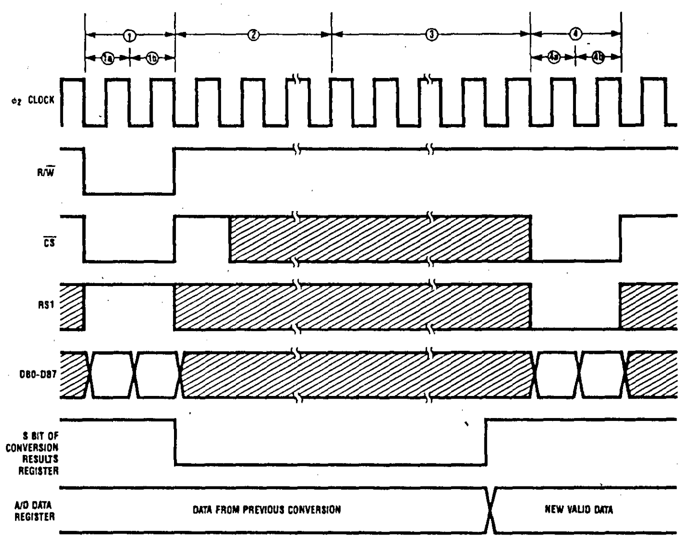


Timing for a Typical μP 16 Byte Access



TL/F/5508-4

FIGURE 1. Timing for a Typical μP 8 Byte Access



1. START CONVERSION
   a. SET SC BIT TO A 1
   b. LOAD ADDRESS
2. ANALOG INPUT SETTLING TIME ALLOWS INTERNAL MULTIPLEXER TO SELECT A CHANNEL AND STABILIZE (~32 CLOCKS).
3. A/D CONVERSION TIME (~256 CLOCKS)
4. READ END OF CONVERSION DATA
   a. EOC BIT READ IF A 1 CONVERSION COMPLETE.
   b. A/D DATA REGISTER READ. IF EOC = 1, THEN NEW VALID DATA.

TL/F/5508-5

FIGURE 2. A/D Conversion Timing Sequence

Functional Description (Continued)

6.0 WORD FORMAT

6.1 Control Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
X	X	X	X	X	X	X	(LSB) SC	X	X	X	X	A3 CH3	A2 CH2	A1 CH1	A0 CH0

X:	Don't Care
SC:	Start Conversion
	1 = Start new conversion
	0 = Do not start new conversion
CH3-CH0:	Channel Address
Hex Value	Definition
0	Select CH0
1	Select $V_{ref}(+)$
2-5	Select Channels CH2-CH5
6-9	Undefined
A-F	Select CH7-CH10

6.2 Conversion Results Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
S	0	0	0	0	0	0	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

S:	Status
	1 = Data is valid (conversion complete)
	0 = Data is not valid
C_7-C_0:	8 bit converted result

6.3 Discrete Input Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
P5	P4	P3	P2	P1	P0	CH3	CH2	CH1	CH0	0	0	0	0	0	0

CH3-CH0:	Status of channel address
P5-P0:	Status of P5-P0 interpreted as discrete digital inputs

ADU ADDRESS SELECTION

CSO*	R/W	RSI	Description
1	X	X	Do not respond
0	0	0	Write NO OP
0	0	1	Write Control Word
0	1	0	Read Conversion Results
0	1	1	Read Discrete Inputs

Note: All words are transferred as two 8-bit bytes, MSB transferred first LSB transferred second.

7.0 ANALOG TO DIGITAL CONVERTER

The ADC0829 A/D Converter is composed of three major sections: the successive approximation register (SAR); the 256R ladder and analog decoder; and the sample-data comparator.

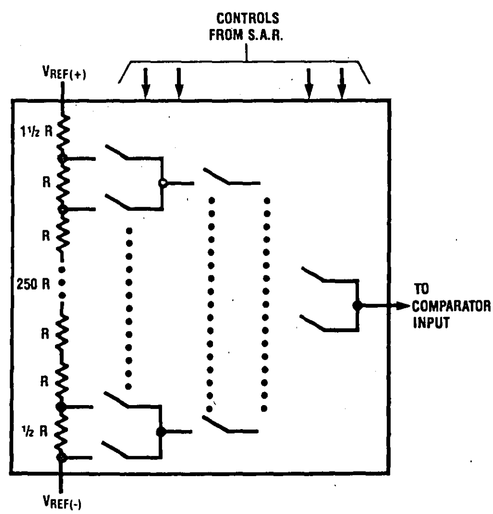
7.1 Successive Approximation

The analog signal at the A/D input is compared eight times to various ladder voltages to determine which of the 256 voltages in the ladder most closely approximates the input voltage. This stochastic technique is accomplished by converging on the proper tap in the ladder by simple iterative convergence. There are nine posting registers in the SAR which contain the position of the bit being tested and eight latching registers which remember if the comparison was high or low. Starting with the MSB and continuing downward each bit is set high by the posting register. The analog tree decoder selects the corresponding tap in the ladder and the A/D input is compared to that voltage. If the comparison is positive the latch remains set, so higher voltages in the ladder are checked next. If the comparison is negative the bit is reset so lower ladder voltages are sought.

After all eight comparisons are made, the contents of the latching register are transferred to a data register, thus the A/D can perform a new conversion while the previous results remain available.

7.2 256R Ladder

The ladder is a very accurate voltage divider which divides the reference voltage into 256 equal steps. Special consideration was given to the ladder terminations at each end, and also the center, to ensure consistent and accurate voltage steps. The use of a 256R ladder guarantees monotonicity since only a single voltage gradient across the ladder exists. Shorted or unequal resistors in the ladder may cause non-uniform steps but cannot cause a nonmonotonic response so often fatal in closed loop system applications. (See *Figure 3*.)



TL/F/5508-6

FIGURE 3. Resistor Ladder and Switch Tree

Functional Description (Continued)

Actually of the 256 resistors in the ladder, 254 have the same value while the end point resistors are equal to 1-1/2R and 1/2R. This ensures the system output characteristic is symmetrical with the zero and full scale points of its input to output, or transfer curve.

The tree decoder routes the 256 voltages from the ladder to a single point at the comparator input. This allows comparisons between the A/D input and any voltage the SAR directs the decoder to route to the comparator.

Since the ladder is dependent upon only the matching of resistors, the voltages it generates are very stable with temperature and have excellent repeatability and long term drift.

8.0 MULTIPLEXER

8.1 Analog Inputs

The analog multiplexer selects one of 11 channels and directs them to the input of the A/D converter. The multiplexer was designed to minimize the effects of leakage currents and multiplexer output capacitance.

Special input protection is used to prevent damage from static voltages or voltages exceeding the specified range from −0.3V to V_{CC}+0.3V. However, normal precautions are recommended to avoid such situations whenever possible.

8.2 Digital Inputs

Six of the analog inputs can also be used as digital inputs to sense TTL voltage levels. Care must be taken when these inputs are interpreted since TTL levels may not always be present.

8.3 A/D Comparator

Probably the most important section of the A/D converter is the comparator since the comparator's offset voltage and stability determine the converter's ultimate accuracy. The low voltage offset of the chopper-stabilized comparator of this converter optimizes performance by minimizing temperature dependent input offset errors as well as drift.

The dc signal appearing at the amplifier input is converted to an ac signal, amplified by an ac amplifier and restored to a dc signal. The drift of the comparator is minimized since the drift signal is a dc component blocked by the ac amplifier.

The comparator has very high input impedance to dc voltages since it looks like a capacitor. Because the comparator is chopping the dc voltages at the input, the difference between the A/D input voltage and ladder voltage appears on the comparator's input capacitor. The input voltage difference, chopping frequency, and comparator input capacitor causes a CVF current. The CVF current is a small bias current which will not produce any error when the A/D input is connected to a low impedance voltage source. If the voltage source has an output impedance of less than 10k, the error is still insignificant since the bias current exponentially decays.

Adding a capacitor to the input of the comparator integrates the exponential charging current converting it into dc bias current. (See Figure 1.) Two main considerations on the integration capacitor are charge sharing with a filter capacitor and settling time.

9.0 BUS INTERFACE

The ADC0829 communicates to the microprocessor through an 8-bit I/O port. The I/O port is composed of a TTL to CMOS buffer and a TRI-STATE output driver.

The TTL to CMOS Buffer translates the TTL voltage levels into CMOS levels very rapidly and is quite stable with supply and temperature. The buffer has a small amount of hysteresis (about 100 mV) to improve both noise immunity and internal rise and fall times.

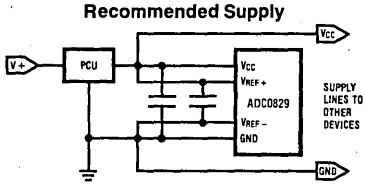
The TRI-STATE bus driver is a bipolar and N-channel pair that easily drive the bus capacitance. Since the bus drivers collectively can sink or source a quarter of an amp total, a non-overlap circuit is used which guarantees that only one of the two drive transistors is on at a time.

Since this output drives the bus capacitance, even the non-overlapping circuit cannot prevent noise on V_{CC}. The amount of noise depends on the V_{CC} current used to charge the bus capacitance.

The external filter capacitor on V_{CC} provides some of the transient current while the bus is being driven. A capacitor with good ac characteristics and low series resistance is a good choice to prevent V_{CC} transients from affecting accuracy.

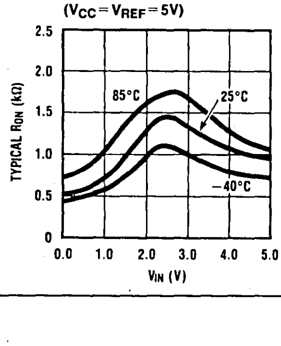
Application Information

Recommended Supply



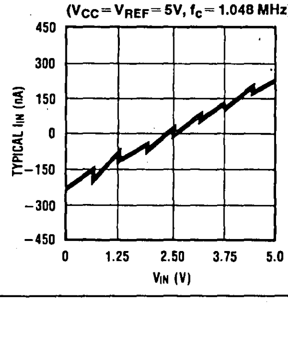
TL/F/5508-7

Multiplexer R_{ON} vs V_{IN} ($V_{CC}=V_{REF}=5V$)



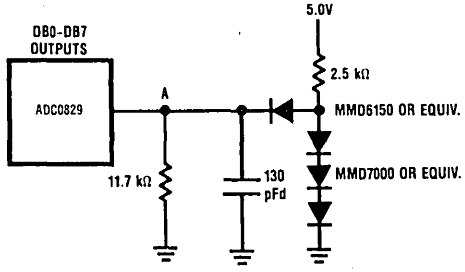
TL/F/5508-8

Comparator I_{IN} vs V_{IN} ($V_{CC}=V_{REF}=5V$, $f_c=1.048$ MHz)



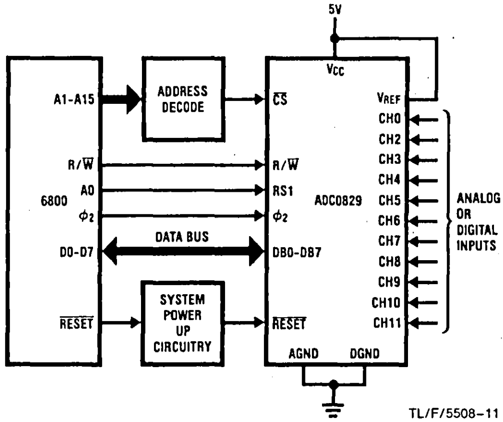
TL/F/5508-9

Data Bus Test Circuit



TL/F/5508-10

Typical Application



TL/F/5508-11

National Semiconductor

ADC0831, ADC0832, ADC0834 and ADC0838 (COP431, COP432, COP434 and COP438) 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

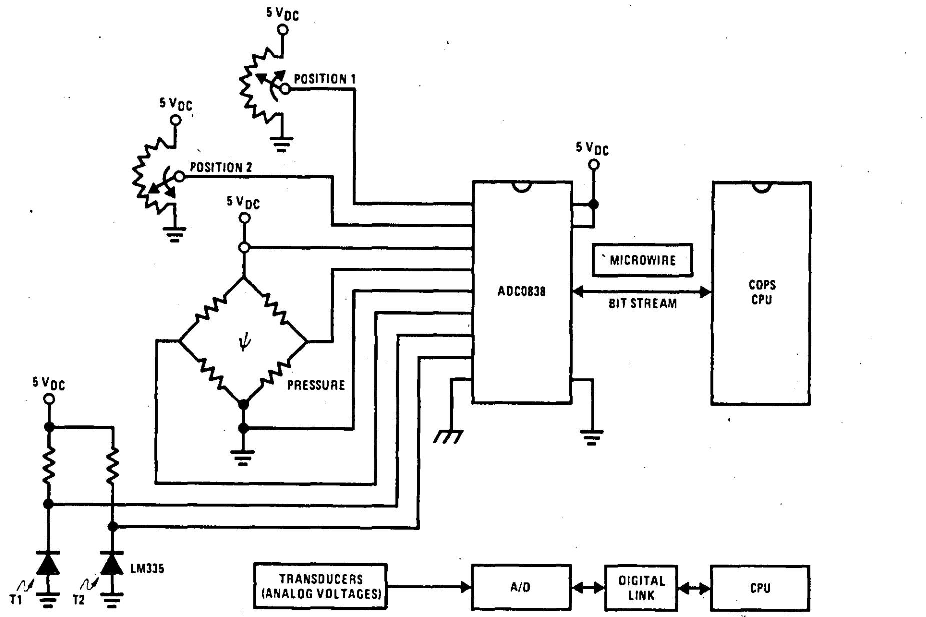
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3″ standard width, 8-, 14- or 20-pin DIP package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 μs

Typical Application



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Absolute Maximum Ratings

(Notes 1 and 2)

Current into V+	10 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to +15V
Analog Inputs	−0.3V to V_{CC} +0.3V
Input Current per Pin	±5 mA
Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0831BJ, ADC0832BJ, ADC0834BJ, ADC0838BJ	−55°C to +125°C
ADC0831BCJ, ADC0831CCJ, ADC0832BCJ, ADC0832CCJ, ADC0834BCJ, ADC0834CCJ, ADC0838BCJ, ADC0838CCJ	−40°C to +85°C
ADC0831BCN, ADC0831CCN, ADC0832BCN, ADC0832CCN, ADC0834BCN, ADC0834CCN, ADC0838BCN, ADC0838CCN	−0°C to +70°C

Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V+ = 5V, and f_{CLK} = 250 kHz unless otherwise specified. Boldface limits apply from T_{MIN} to T_{MAX}; all other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC083_BJ ADC083_BCJ ADC083_CCJ			ADC083_BCN ADC083_CCN			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	V_{REF} = 5.00 V_{DC} (Note 4)							
ADC083_BCN						±½	**±½**	LSB
ADC083_BJ ADC083_BCJ			**±½**					LSB
ADC083_CCN						±1	**±1**	LSB
ADC083_CCJ			**±1**					LSB
Minimum Reference Input Resistance		2.4	**1.2**		2.4	1.9	**1.2**	kΩ
Maximum Reference Input Resistance		2.4	**6.0**		2.4		**6.0**	kΩ
Maximum Common-Mode Input (Note 5)			**V_{CC} +0.05**			V_{CC} +0.05	**V_{CC} +0.05**	V
Minimum Common-Mode Input (Note 5)			**GND −0.05**			GND −0.05	**GND −0.05**	V
DC Common-Mode Error		±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity	V_{CC} = 5V ±5%	±1/16	**±⅛**		±1/16	±⅛	**±⅛**	LSB
I_{OFF}, Off Channel Leakage Current (Note 6)	On Channel = 5V Off Channel = 0V		**−1**			−0.05	**−1**	μA
	On Channel = 0V Off Channel = 5V		**1**			0.05	**1**	μA
I_{ON}, On Channel Leakage Current (Note 6)	On Channel = 0V Off Channel = 5V		**−1**			−0.20	**−1**	μA
	On Channel = 5V Off Channel = 0V		**1**			0.20	**1**	μA

Converter and Multiplexer Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V+ = 5V$, and $f_{CLK} = 250$ kHz unless otherwise specified. Boldface limits apply from T_{MIN} to T_{MAX}; all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	ADC083_BJ ADC083_BCJ ADC083_CCJ			ADC083_BCN ADC083_CCN			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC} = 5.25V$		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC} = 4.75V$		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN} = 5.0V$	0.005	**1**		0.005		**1**	µA
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN} = 0V$	−0.005	**−1**		−0.005		**−1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**			 2.8 4.6	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	µA µA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT} = V_{CC}$	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		1	**2.5**		1		**2.5**	mA
ADC0832	Includes Ladder Current	3	**7.2**		3		**7.2**	mA

AC Characteristics

The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20$ ns and 25°C unless otherwise specified.

Parameter		Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 7)	Min				40	%
	Max				60	%
t_{SET-UP}, CS Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{CSPW}, Minimum $\overline{CS}$ High Internal			35		120	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 8)		$C_L = 100$ pF Data MSB First Data LSB First	 650 250		 1500 600	 ns ns
t_{1H}, t_{0H},—Rising Edge of CS to Data Output and SARS Hi-Z		$C_L = 10$ pF, $R_L = 10k$ (see TRI-STATE® Test Circuits)	125		250	ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: An internal zener diode exists from V_{CC} to GND on the V^+ and V_{CC} inputs. The breakdown of these zeners is approximately 7V. The V^+ zener is intended to operate as a shunt regulator and connects to the V_{CC} via a diode. When using this regulator to power the A/D, this diode guarantees the V_{CC} input to be operating below the zener voltage (7V–0.6V). It is recommended that a series resistor be used to limit the maximum current into the V^+ input.

Note 4: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 5: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

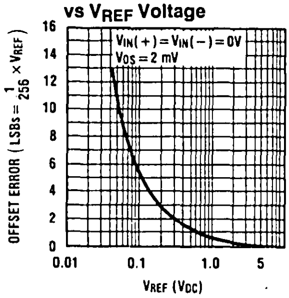
Note 6: Leakage current is measured with the clock not switching.

Note 7: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 μs.

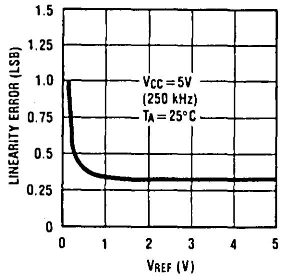
Note 8: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Typical Performance Characteristics

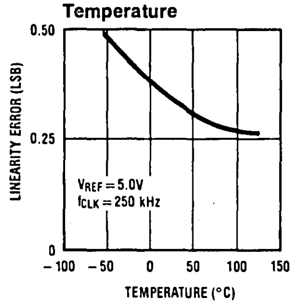
Unadjusted Offset Error vs V_{REF} Voltage



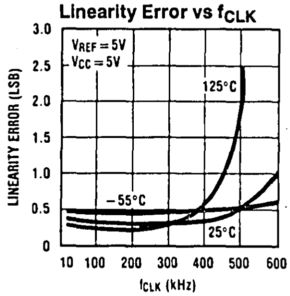
Linearity Error vs V_{REF} Voltage



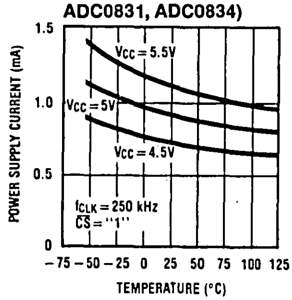
Linearity Error vs Temperature



Linearity Error vs f_{CLK}

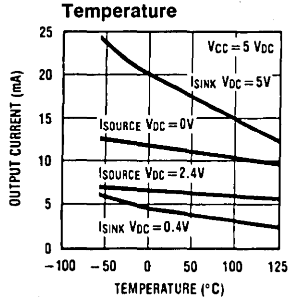


Power Supply Current vs Temperature (ADC0838, ADC0831, ADC0834)

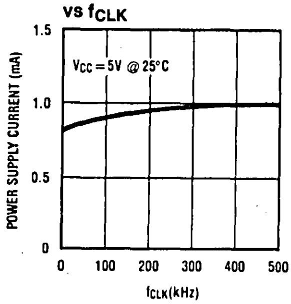


Note: For ADC0832 and I_{REF}

Output Current vs Temperature



Power Supply Current vs f_{CLK}



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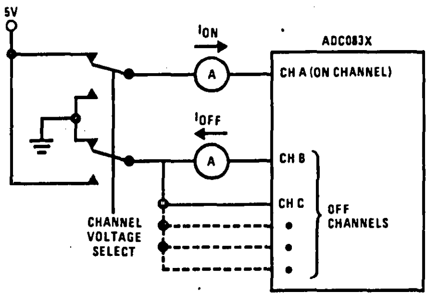
Leakage Current Test Circuit



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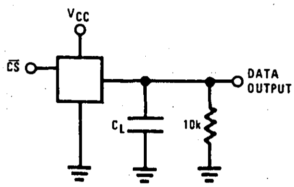
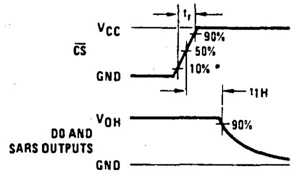
TRI-STATE Test Circuits and Waveforms

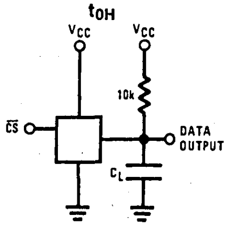
t_{1H}



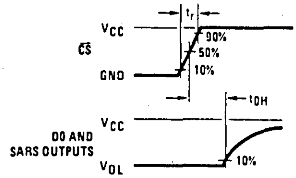
t_{1H}, $C_L = 10$ pF



t_{0H}

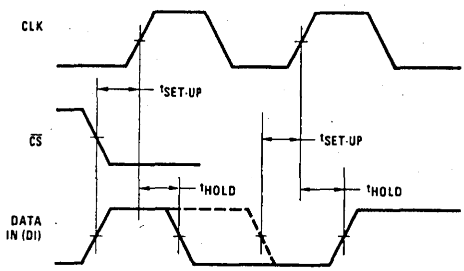


t_{0H}, $C_L = 10$ pF

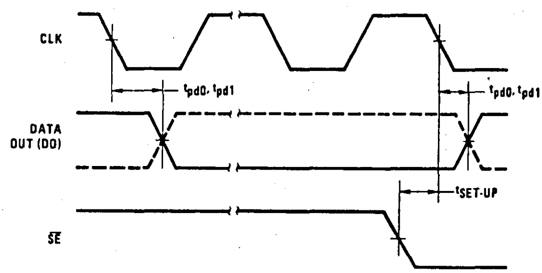


Timing Diagrams

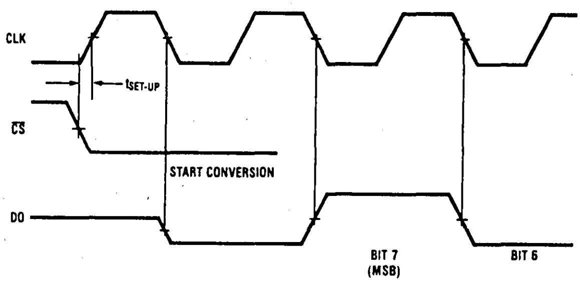
Data Input Timing



Data Output Timing



ADC0831 Start Conversion Timing



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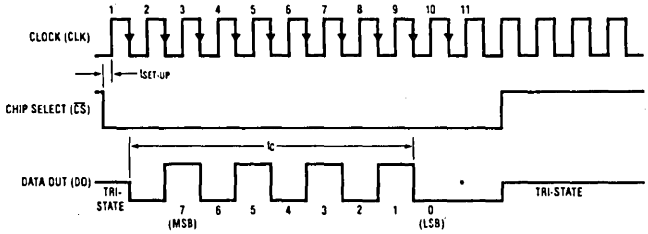
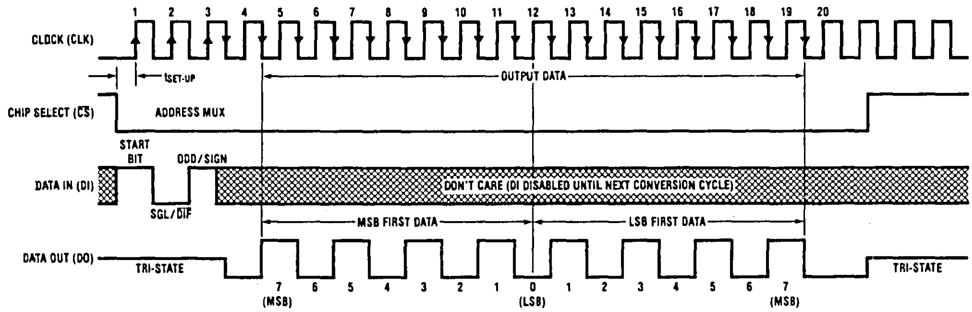
Timing Diagrams (Continued)

ADC0831 Timing

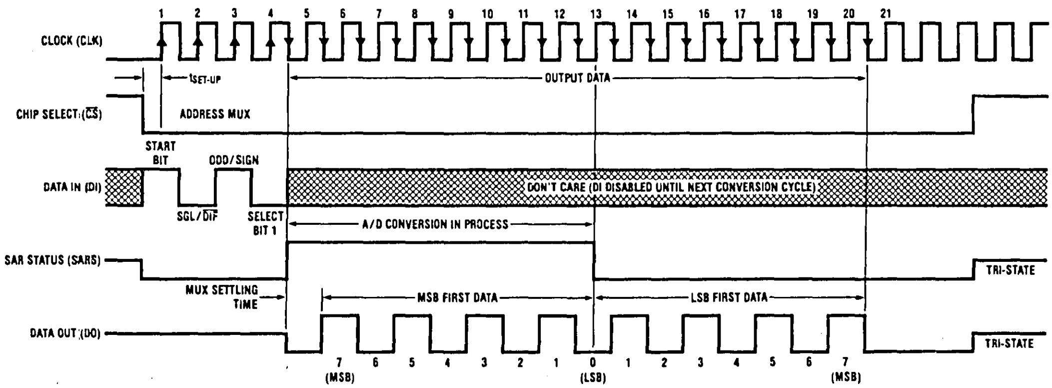


*LSB first output not available on ADC0831

ADC0832 Timing



ADC0834 Timing



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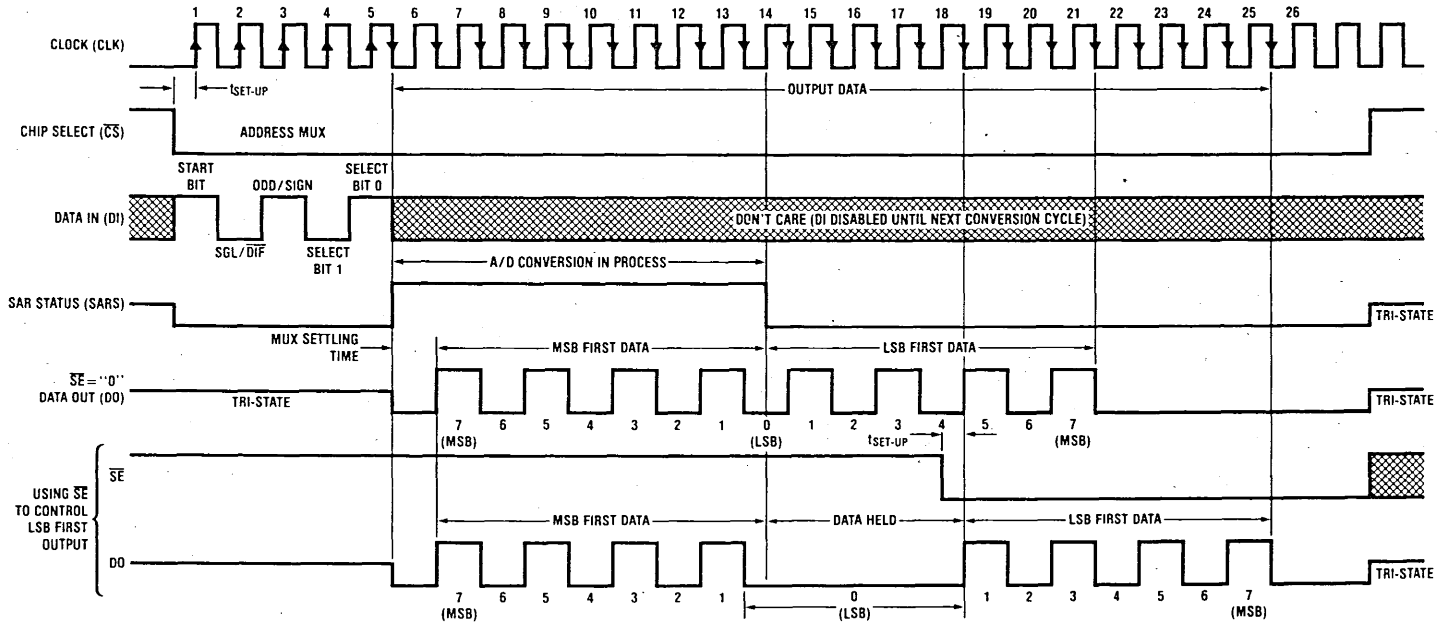
Timing Diagrams (Continued)

ADC0838 Timing



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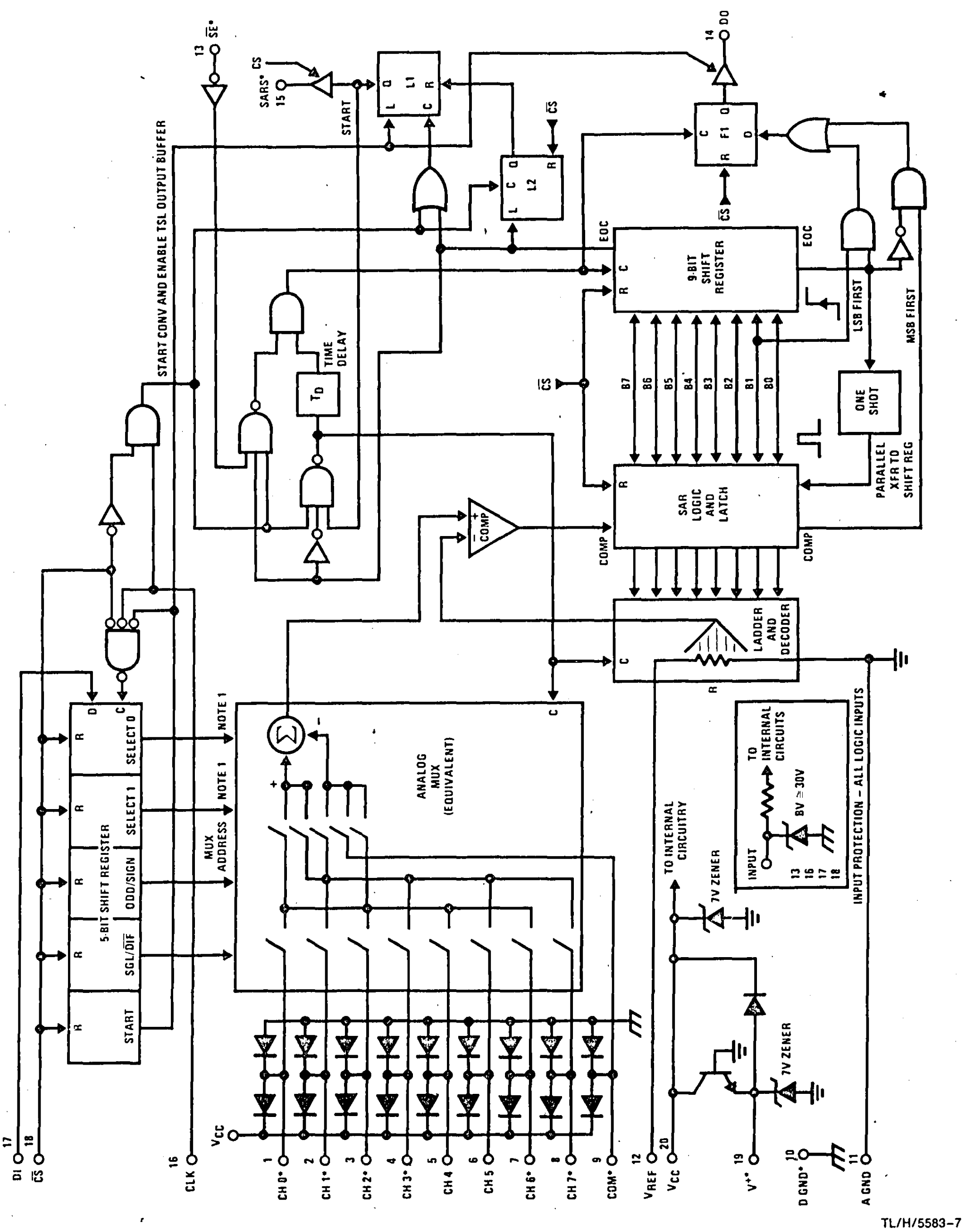
*Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC0838 Functional Block Diagram



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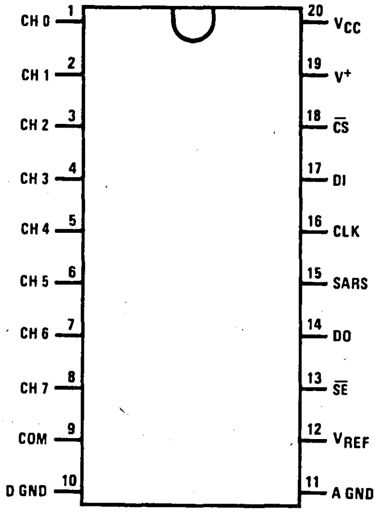
*Some of these functions/pins are not available with other options.

Note 1: For the ADC0834, D1 is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832, DI is input directly to the DI input of ODD/SIGN. SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

Connection Diagrams

ADC0838 8-Channel MUX

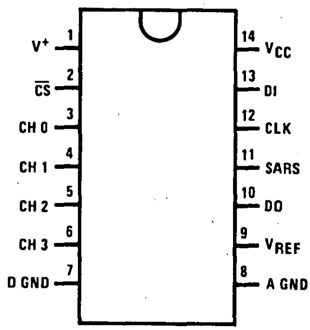
Dual-In-Line Package



TOP VIEW

ADC0834 4-Channel MUX

Dual-In-Line Package

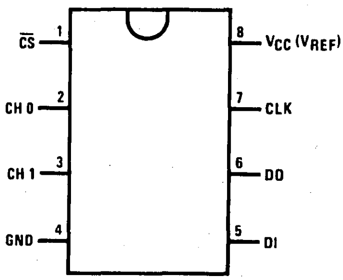


TOP VIEW

COM internally connected to A GND

ADC0832 2-Channel MUX

Dual-In-Line Package



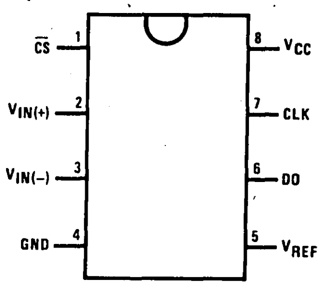
TOP VIEW

COM internally connected to GND.

V_{REF} internally connected to V_{CC}.

ADC0831 Single Differential Input

Dual-In-Line Package



TOP VIEW

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Applications

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter through the DI line (because the ADC0831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing).

The common input line on the ADC0838 can be used for a pseudo-differential input. In this mode, the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where all of the analog circuitry may be biased up to a potential other than ground and the output signals are all relative to this potential.

TABLE 1. MULTIPLEXER/PACKAGE OPTIONS

Part Number	Alternate Part Number	Number of Analog Channels		Number of Package Pins
		Single-Ended	Differential	
ADC0831	COP431	1	1	8
ADC0832	COP432	2	1	8
ADC0834	COP434	4	2	14
ADC0838	COP438	8	4	20

Applications (Continued)

TABLE II. MUX ADDRESSING: ADC0838

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/$\overline{DIF}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
SGL/$\overline{DIF}$	ODD/SIGN	SELECT		0		1		2		3	
		1	0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

TABLE III. MUX ADDRESSING: ADC0834

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE IV. MUX ADDRESSING: ADC0832

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel #	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

Applications (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.

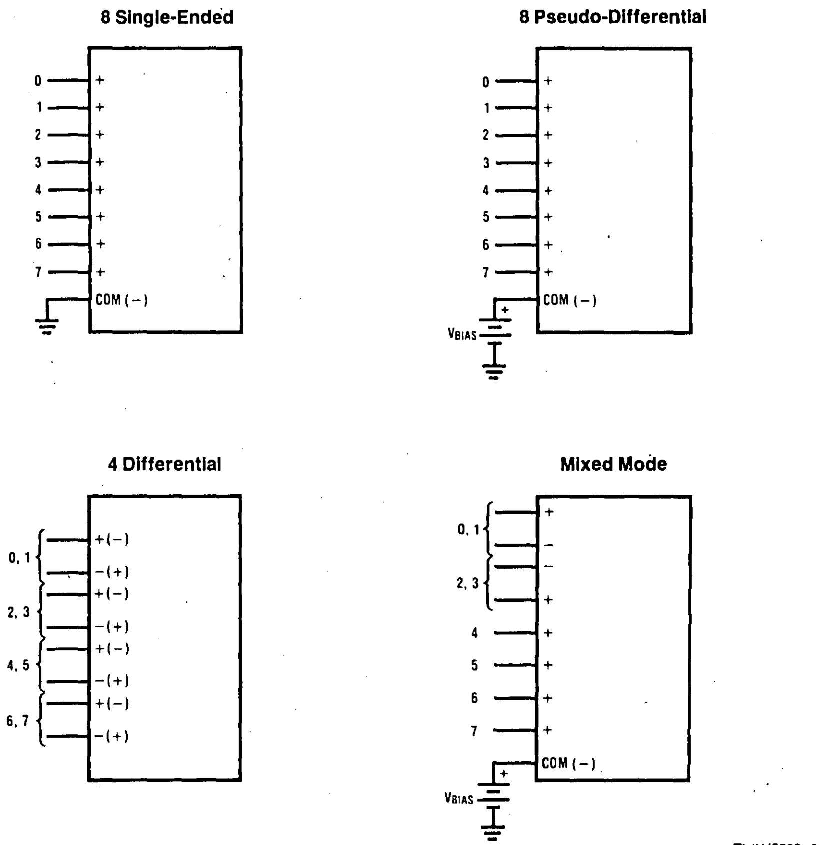


FIGURE 1. Analog Input Multiplexer Options for the ADC0838

Applications (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1 full clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods, the conversion is completed and the SAR status line returns low to indicate this.

8. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. All 8 bits of the result are stored in an output shift register. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. On the ADC0838 the $\overline{SE}$ line is brought out and if held high, the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low, the data is then clocked out LSB first. The ADC0831 is an exception in that its data is only output in MSB first format.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

All of the logic inputs can be taken to 15V independent of the magnitude of the supply voltage, V_{CC}.

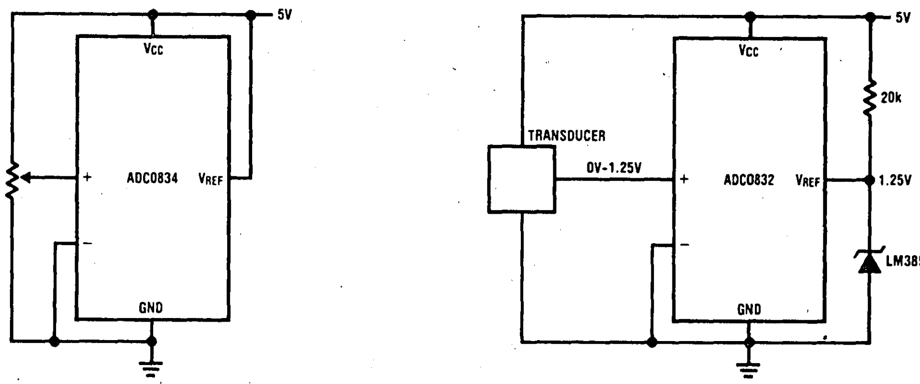
3.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 2.4 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC0832). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/256).



a) Ratiometric   b) Absolute with a Reduced Span

FIGURE 2. Reference Examples

Applications (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{peak}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{peak} is its peak voltage value

and f_{CLK}, is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error ($\approx$5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

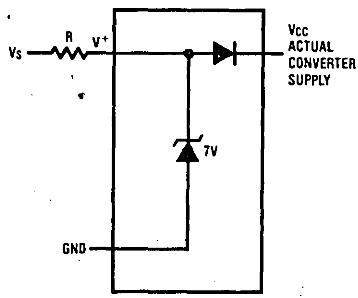
V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0838 and ADC0834 is the inclusion of a 6.8V zener diode connected from the V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3*.



TL/H/5583-11

FIGURE 3. An On-Chip Shunt Regulator Diode

6

Applications (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4 and 5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 6 and 7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D (~3 mA) and the relatively high clock frequencies used (typically in the range of 10k–400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of 7V. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V+ pin.

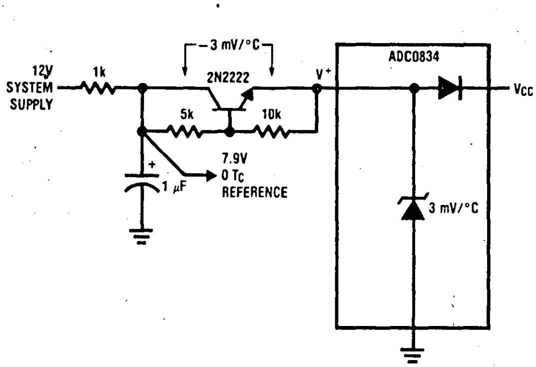


FIGURE 4. Operating with a Temperature Compensated Reference

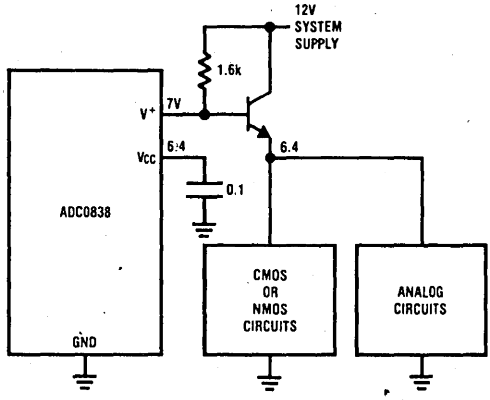


FIGURE 5. Using the A/D as the System Supply Regulator

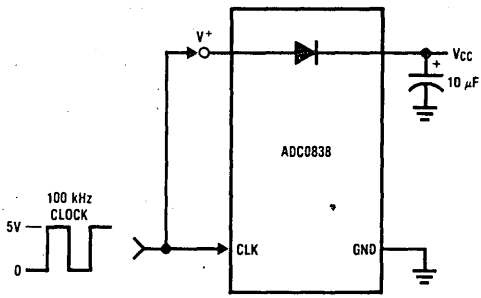


FIGURE 6. Generating V_{CC} from the Converter Clock

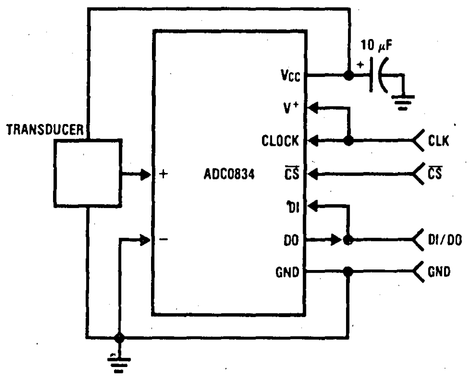


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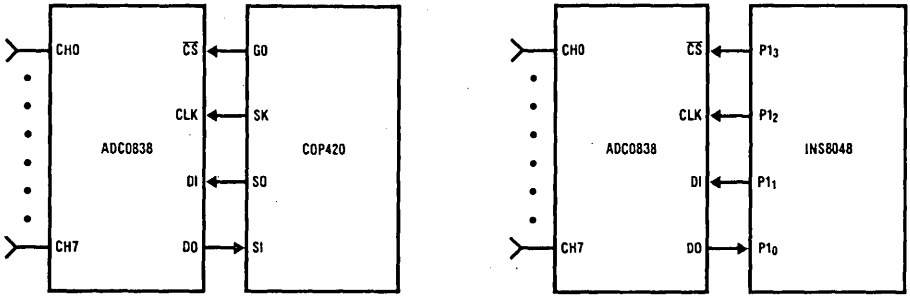
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



TL/H/5583-13

COP CODING EXAMPLE

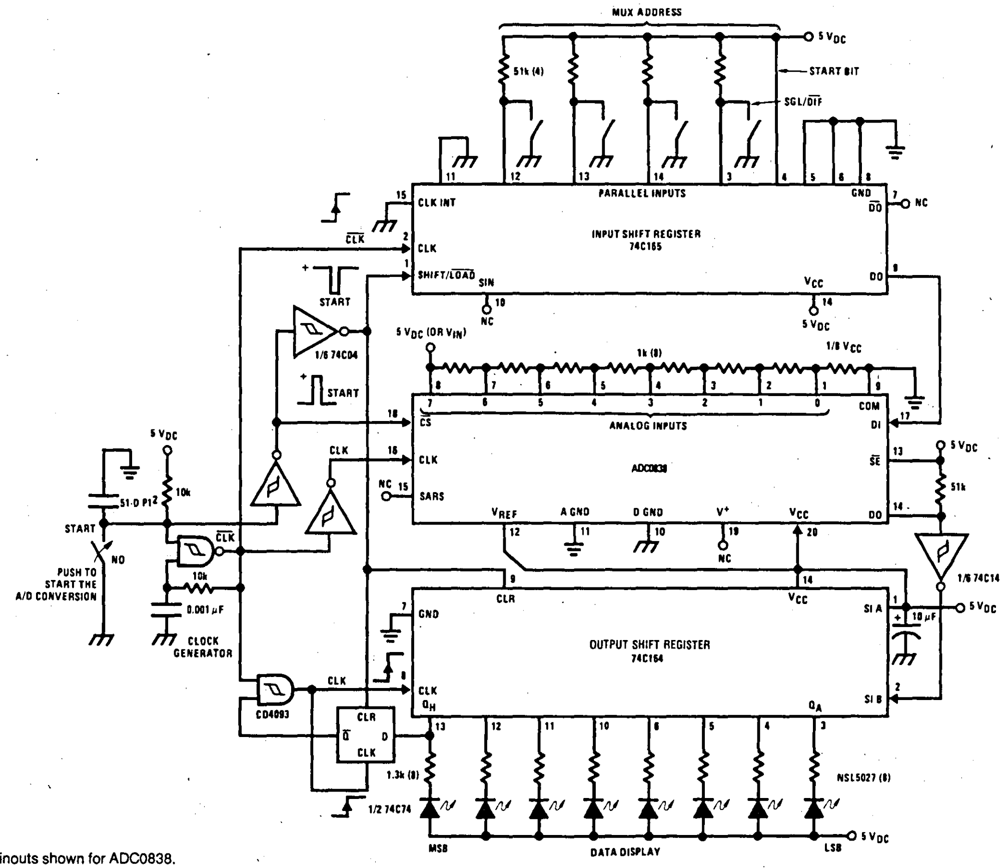
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑ 8 INSTRUCTIONS ↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

	Mnemonic		Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

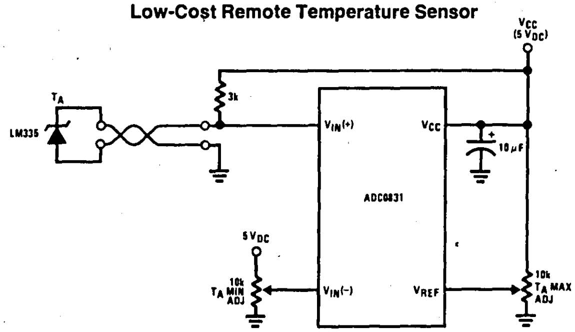
Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0838 Evaluation



*Pinouts shown for ADC0838.
For all other products tie to
pin functions as shown.

Low-Cost Remote Temperature Sensor



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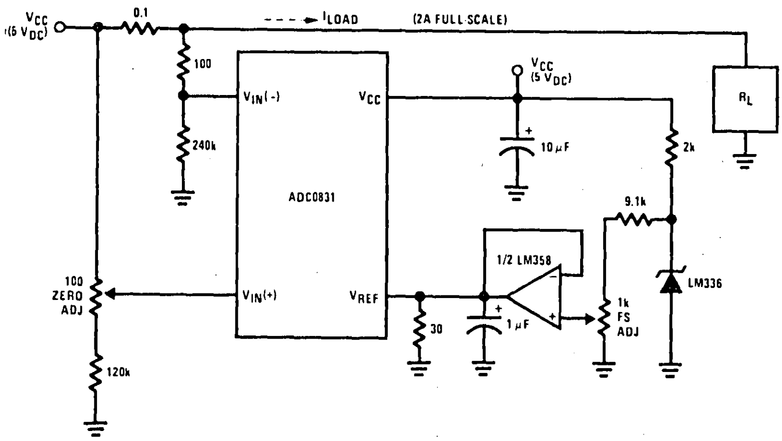
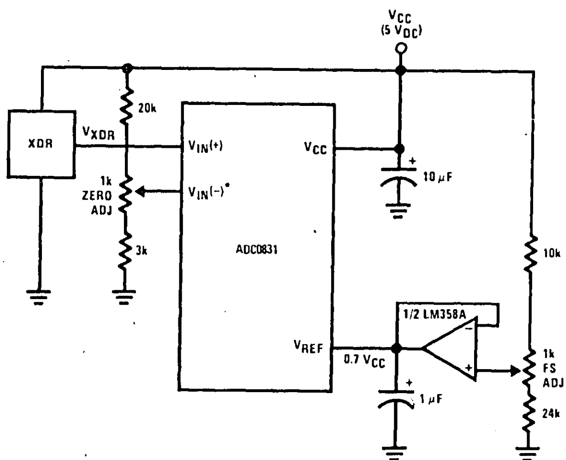
Applications (Continued)

Digitizing a Current Flow



Operating with Ratiometric Transducers

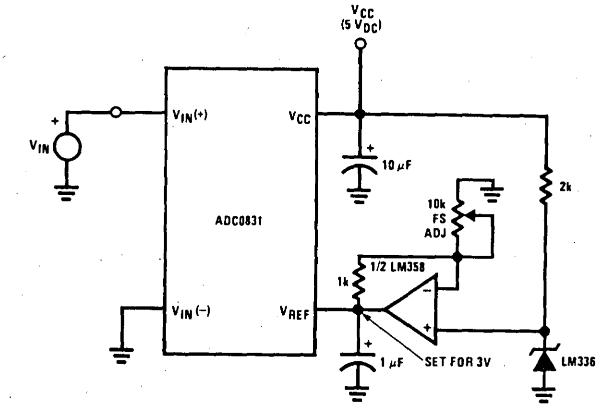


TL/H/5583–15

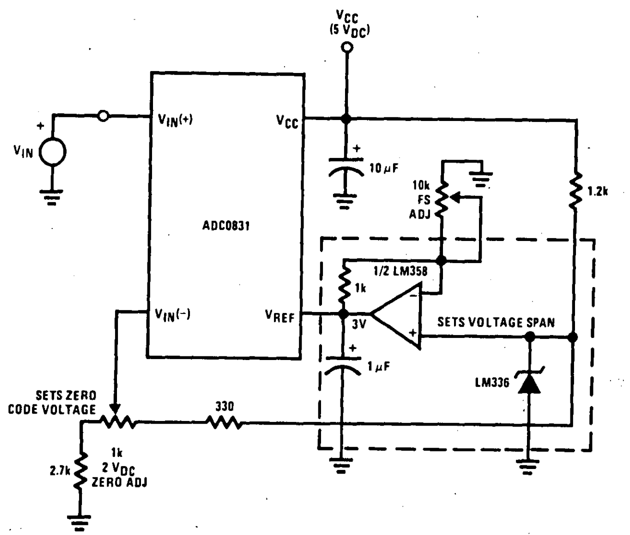
* $V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Applications (Continued)

Span Adjust: $0V \le V_{IN} \le 3V$



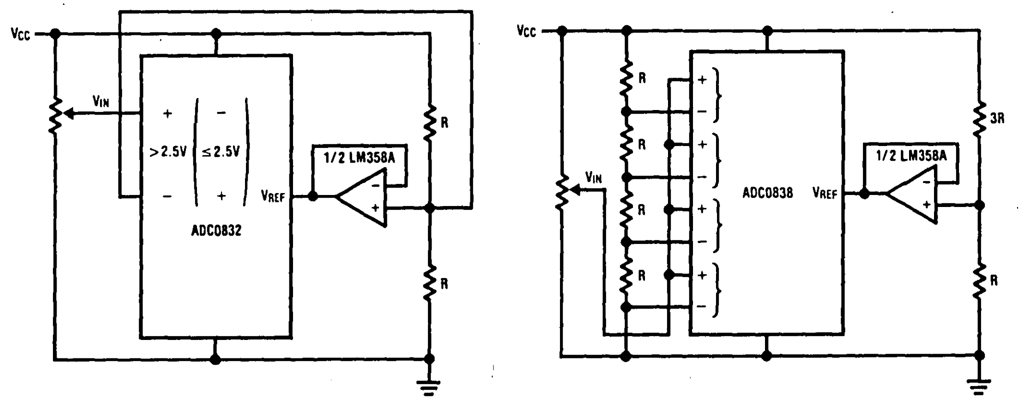
Zero-Shift and Span Adjust: $2V \le V_{IN} \le 5V$



TL/H/5583-16

Applications (Continued)

Obtaining Higher Resolution



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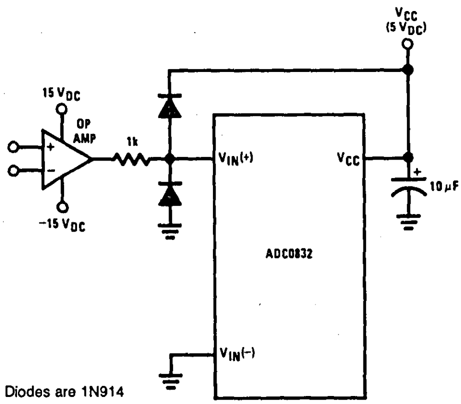
Controller performs a routine to determine which input polarity (9-bit example) or which channel pair (10-bit example) provides a non-zero output code. This information provides the extra bits.

a) 9-Bit A/D

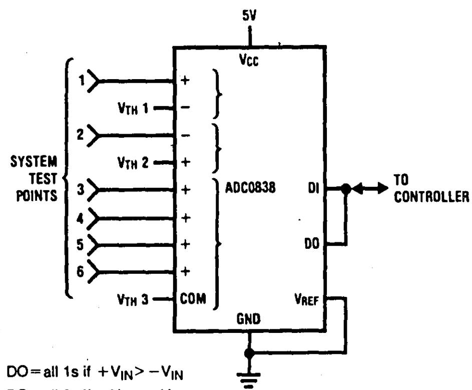
b)10-Bit A/D

Protecting the Input



Diodes are 1N914

High Accuracy Comparators



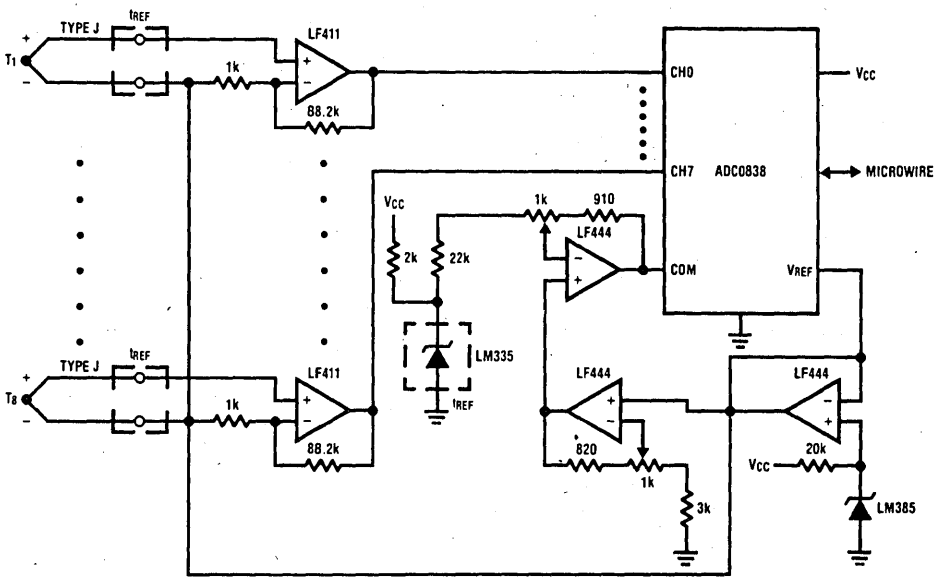
DO = all 1s if $+V_{IN} > -V_{IN}$

DO = all 0s if $+V_{IN} < -V_{IN}$

TL/H/5583-18

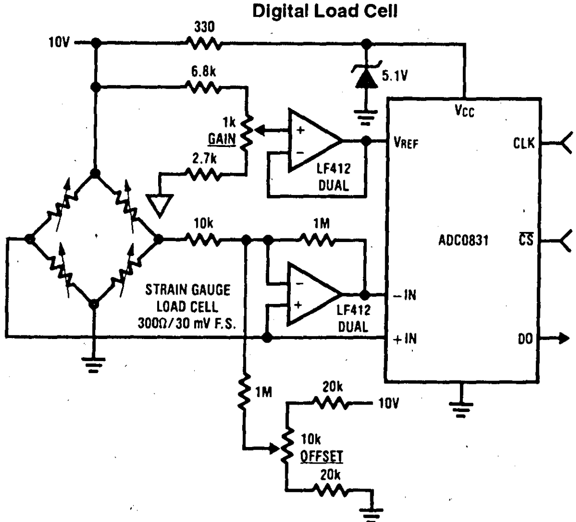
Applications (Continued)

Convert 8 Thermocouples with only One Cold-Junction Compensator



Uses the pseudo-differential mode to keep the differential inputs constant with changes in reference temperature (T_{REF}).

Digital Load Cell

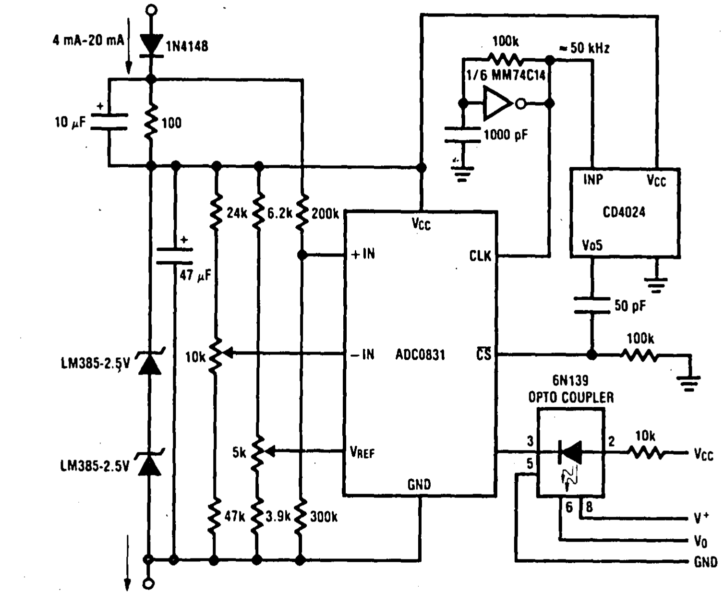


TL/H/5583-19

- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

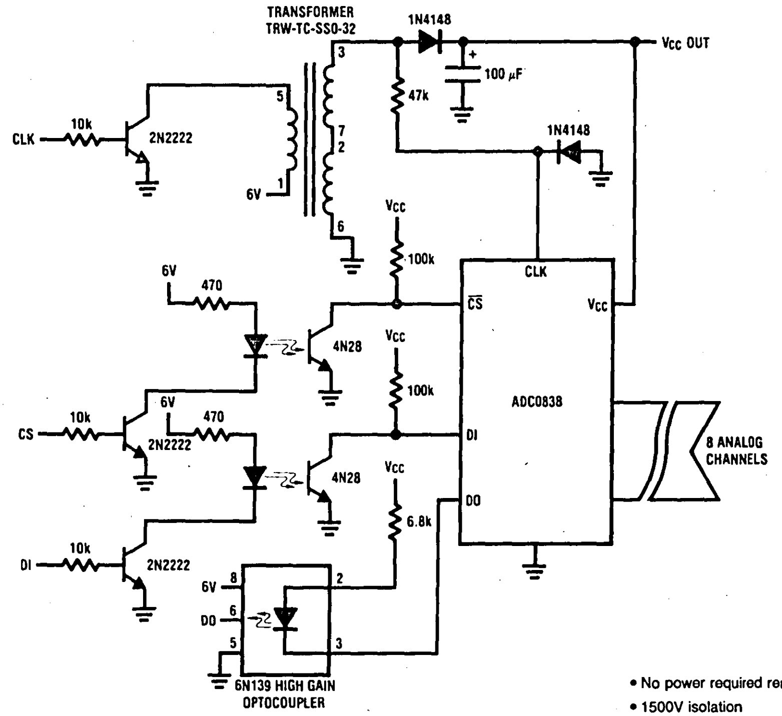
Applications (Continued)

4 mA–20 mA Current Loop Converter



- All power supplied by loop
- 1500V isolation at output

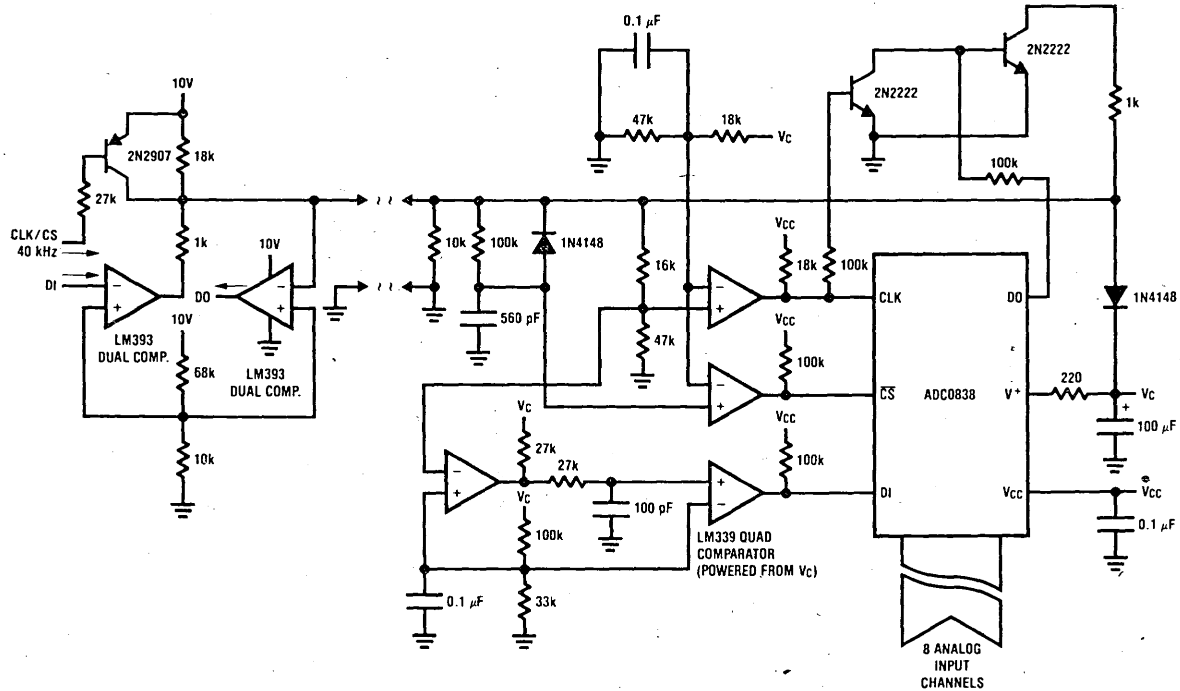
Isolated Data Converter



TL/H/5583-20

- No power required remotely
- 1500V isolation

Two Wire Interface for 8 Channels

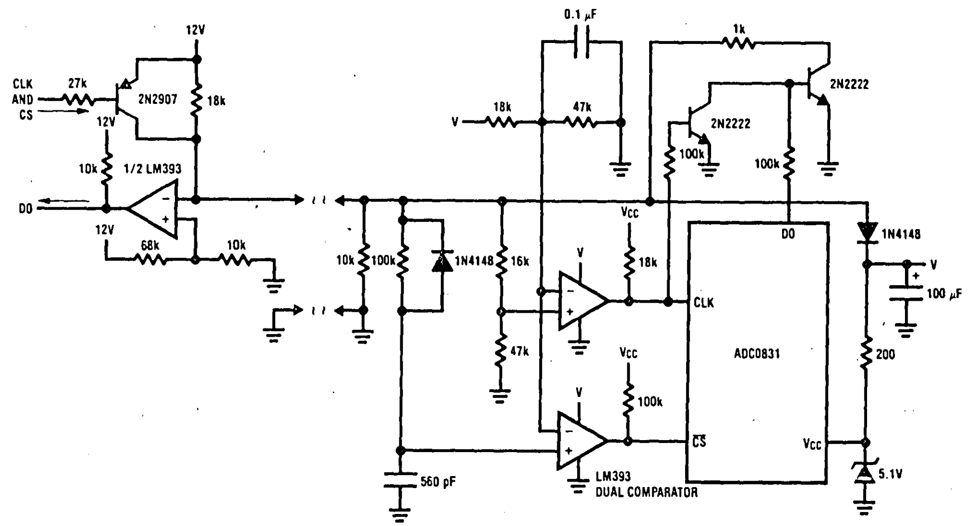


- No additional connections
- $\overline{CS}$ derived from extended high on CLK line > 100 µs
- Timing arranged for 40 kHz, could be changed up or down by component change
- 10% CLK frequency change without component change OK

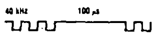
TL/H/5583–21

Applications (Continued)

Two Wire 1-Channel Interface



- Simpler version of 8-channel
- $\overline{CS}$ derived from long CLK pulse



TL/H/5583-22

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831BJ ADC0831CJ ADC0831BCN (COP431BN)	1	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C −0°C to +70°C
ADC0831CCJ ADC0831CCN (COP431CN)		±1	Hermetic (J) Molded (N)	−40°C to +85°C −0°C to +70°C
ADC0832BJ ADC0832BCJ ADC0832BCN (COP432BN)	2	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C −0°C to +70°C
ADC0832CCJ ADC0832CCN (COP432CN)		±1	Hermetic (J) Molded (N)	−40°C to +85°C −0°C to +70°C
ADC0834BJ ADC0834BJ ADC0834BCN (COP434BN)	4	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C −0°C to +70°C
ADC0834CCJ ADC0834CCN (COP434CN)		±1	Hermetic (J) Molded (N)	−40°C to +85°C −0°C to +70°C
ADC0838BJ ADC0838BCJ ADC0838BCN (COP438BN)	8	±½	Hermetic (J) Hermetic (J) Molded (N)	−55°C to +125°C −40°C to +85°C −0°C to +70°C
ADC0838CCJ ADC0838CCN (COP438CN)		±1	Hermetic (J) Molded (N)	−40°C to +85°C −0°C to +70°C

See NS Packages J08A, J14A, J20A, N08E, N14A, N20A

National Semiconductor

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Key Specifications

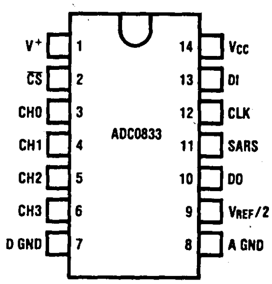
■ Resolution	8 Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	$5V_{DC}$
■ Low Power	25 mW
■ Conversion Time	32 μs

Features

- NSC MICROWIRE compatible-direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3″ standard width 14-pin DIP package

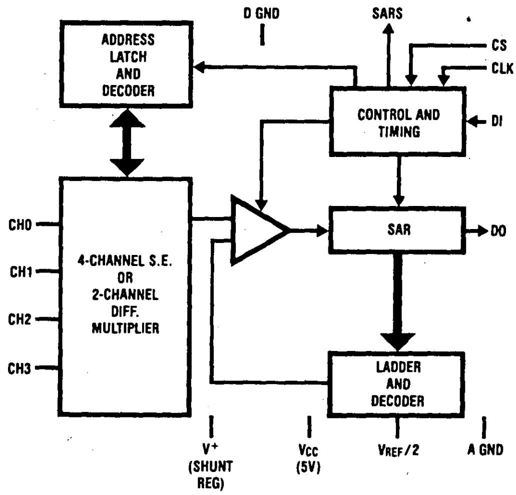
Connection Diagram

Dual-In-Line Package



TOP VIEW

Functional Diagram



TL/H/5607-1

Absolute Maximum Ratings

(Notes 1 and 2)

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to + 15V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin	±5mA
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0833BJ, ADC0833CJ	$-55°C \leq T_A \leq 125°C$
ADC0833BCJ, ADC0833CCJ	$-40°C \leq T_A \leq 85°C$
ADC0833BCN, ADC0833CCN	$0°C \leq T_A \leq 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = V+ = 5V$, $f_{CLK} = 250$ kHz unless otherwise specified. Boldface limits apply from t_{MIN} to t_{MAX}; all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error	$V_{REF}/2$ Forced to 2.500 V_{DC}				
ADC0833BCN			±½	±½	LSB
ADC0883BJ, BCJ			±½		LSB
ADC0833CCN			±1	**±1**	LSB
ADC0833CJ, CCJ			±1		LSB
Minimum Total Ladder Resistance (Note 7)					
ADC0833BCJ/CCJ/BJ/CJ		4.8	**2.2**		kΩ
ADC0833BCN/CCN		4.8	2.2	**2.2**	kΩ
Maximum Total Ladder Resistance (Note7)					
ADC0833BCJ/CCJ/BJ/CJ		4.8	**8.2**		kΩ
ADC0833BCN/CCN		4.8	8.2	**8.2**	kΩ
Minimum Common-Mode Input Range (Note 8)	All MUX Inputs and COM Input				
ADC0833BCJ/CCJ/BJ/CJ			**GND−0.05**		V
ADC0833BCN/CCN			GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input Range (Note 8)	All MUX Inputs and COM Input				
ADC0833BCJ/CCJ/BJ/CJ			**V_{CC}+0.05**		V
ADC0833BCN/CCN			V_{CC}+0.05	**V_{CC}+0.05**	V
DC Common-Mode Error					
ADC0833BCJ/CCJ/BJ/CJ		±1/16	±¼		LSB
ADC0833BCN/CCN		±1/16	±¼	±¼	LSB
Power Supply Sensitivity	V_{CC} = 5V ± 5%				
ADC0833BCJ/CCJ/BJ/CJ		±1/16	±⅛		LSB
ADC0833BCN/CCN		±1/16	±⅛	±⅛	LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V				
ADC0833BCJ/CCJ/BJ/CJ			**−1**		µA
			−50		nA
ADC0833BCN/CCN				**−1**	µA
			−50		nA
	On Channel = 0V, Off Channel = 5V				
ADC0833BCJ/CCJ/BJ/CJ			**−1**		µA
			−50		nA
ADC0833BCN/CCN				**−1**	µA
			−50		nA

Electrical Characteristics

(Continued) The following specifications apply for $V_{CC} = V^{+} = 5V$, $f_{CLK} = 250$ kHz unless otherwise specified. Boldface limits apply from t_{MIN} to t_{MAX}; all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V				
ADC083BCJ/CCJ/BJ/CJ			**−1**		μA
			−200		nA
ADC0833BCN/CCN				**−1**	μA
			−200		nA
	On Channel = 0V, Off Channel = 5V				
ADC083BCJ/CCJ/BJ/CJ			**−1**		μA
			−200		nA
ADC0833BCN/CCN				**−1**	μA
			−200		nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$				
ADC0833BCJ/CCJ/BJ/CJ			**2.0**		V
ADC0833BCN/CCN			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ			**0.8**		V
ADC0833BCN/CCN			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$				
ADC0833BCJ/CCJ/BJ/CJ		0.005	**1**		μA
ADC0833BCN/CCN		0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$				
ADC0833BCJ/CCJ/BJ/CJ		−0.005	**−1**		μA
ADC0833BCN/CCN		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ	$I_{OUT} = -360\mu A$		**2.4**		V
ADC0833BCN/CCN			2.4	**2.4**	V
ADC0833BCJ/CCJ/BJ/CJ	$I_{OUT} = -10\mu A$		**4.5**		V
ADC0833BCN/CCN4.54			4.5	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6mA$, $V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ			**0.4**		V
ADC0833BCN/CCN			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (DO, SARS)					
ADC0833BCJ/CCJ/BJ/CJ	$V_{OUT} = 0.4V$	−0.1	**−3**		μA
ADC0833BCN/CCN		−0.1	−3	**−3**	μA
ADC0833BCJ/CCJ/BJ/CJ	$V_{OUT} = 5V$	0.1	**3**		μA
ADC0833BCN/CCN		0.1	3	**3**	μA
I_{SOURCE}	V_{OUT} Short to GND				
ADC0833BCJ/CCJ/BJ/CJ		14	**7.5**		mA
ADC0833BCN/CCN		14	7.5	**7.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}				
ADC0833BCJ/CCJ/BJ/CJ		16	**9.0**		mA
ADC0833BCN/CCN		16	9.0	**9.0**	mA

Electrical Characteristics (Continued) The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz unless otherwise specified. Boldface limits apply from t_{MIN} to t_{MAX}; all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
I_{CC}, Supply Current (Note 3)	$V_{REF}/2$ Open Circuit				
ADC0833BCJ/CCJ/BJ/CJ		2	**5**		mA
ADC0833BCN/CCN		2	5	**5**	mA
I^+, Current into V^+ (Note 3)					
ADC0833BCJ/CCJ/BJ/CJ			**10**		mA
ADC0833BCN/CCN			10	**10**	mA

AC Characteristics $t_r = t_f = 20$ ns

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
f_{CLK}, Clock Frequency	Min		10		kHz
	Max			400	kHz
T_C, Conversion Time	Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 10)	Min			40	%
	Max			60	%
t_{SET-UP}, CS Falling Edge or Data Input Valid to CLK Rising Edge				250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge				90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 11)	$C_L = 100$ pF				
	Data MSB First	650		1500	ns
	Data LSB First	250		600	ns
t_{1H}, T_{OH}—Rising Edge of CS to Data Output and SARS Hi-Z	$C_L = 10$ pF, $R_L = 10k$ (see TRI-STATE Test Circuits)	125		250	ns
C_{IN}, Capacitance of Logic Input		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: An internal zener diode exists from V_{CC} to GND on the V^+ and the V_{CC} inputs. The breakdown of these zeners is approximately 7V. The V^+ zener is intended to operate as a shunt regulator and connects to the V_{CC} via a diode. When using this regulator to power the A/D, this diode guarantees the V_{CC} input to be operating below the zener voltage (7V-0.6V). It is recommended that a series resistor be used to limit the maximum current into the V^+ input.

Note 4: Typicals are at 25°C and represent most likely parametric norm.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: See Applications, section 3.0.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

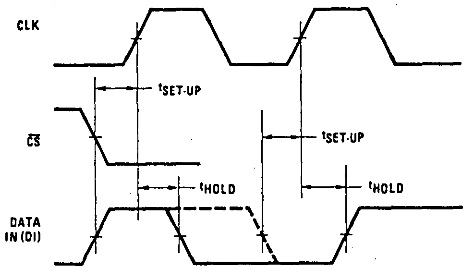
Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 1 μs.

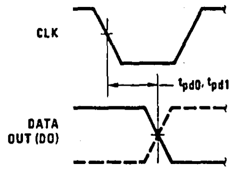
Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Timing Diagrams

Data Input Timing

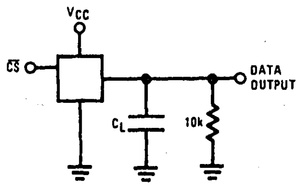


Data Output Timing

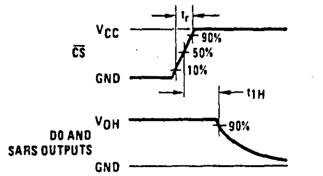


TRI-STATE Test Circuits and Waveforms

t_{1H}

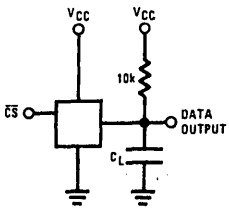


t_{1H}, $C_L = 10$ pF

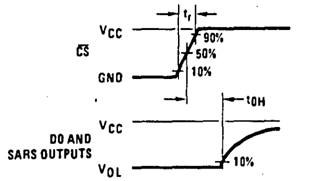


$t_r = 20$ ns

t_{0H}

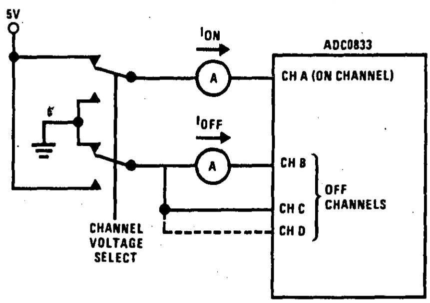


t_{0H}, $C_L = 10$ pF



$t_r = 20$ ns

Leakage Current Test Circuit



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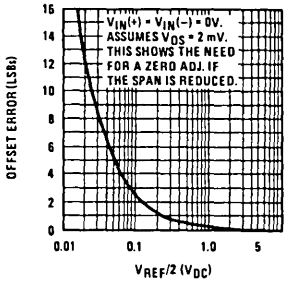
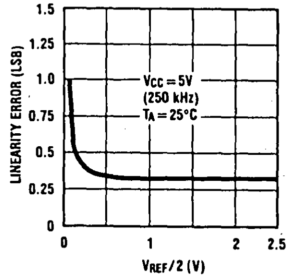
Typical Performance Characteristics

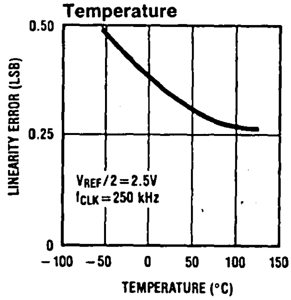
Effect of Unadjusted Offset Error vs $V_{REF}/2$ Voltage



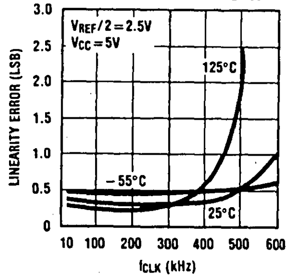
Linearity Error vs V_{REF} Voltage



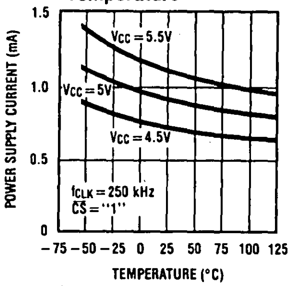
Linearity Error vs Temperature



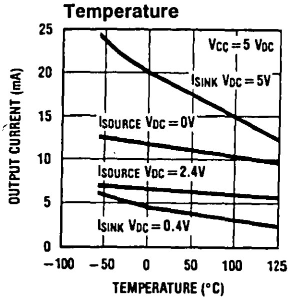
Linearity Error vs f_{CLK}



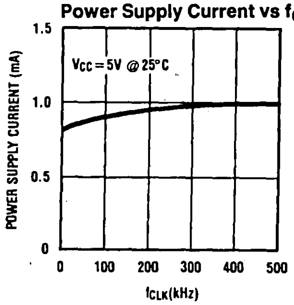
Power Supply Current vs Temperature



Output Current vs Temperature



Power Supply Current vs f_{CLK}



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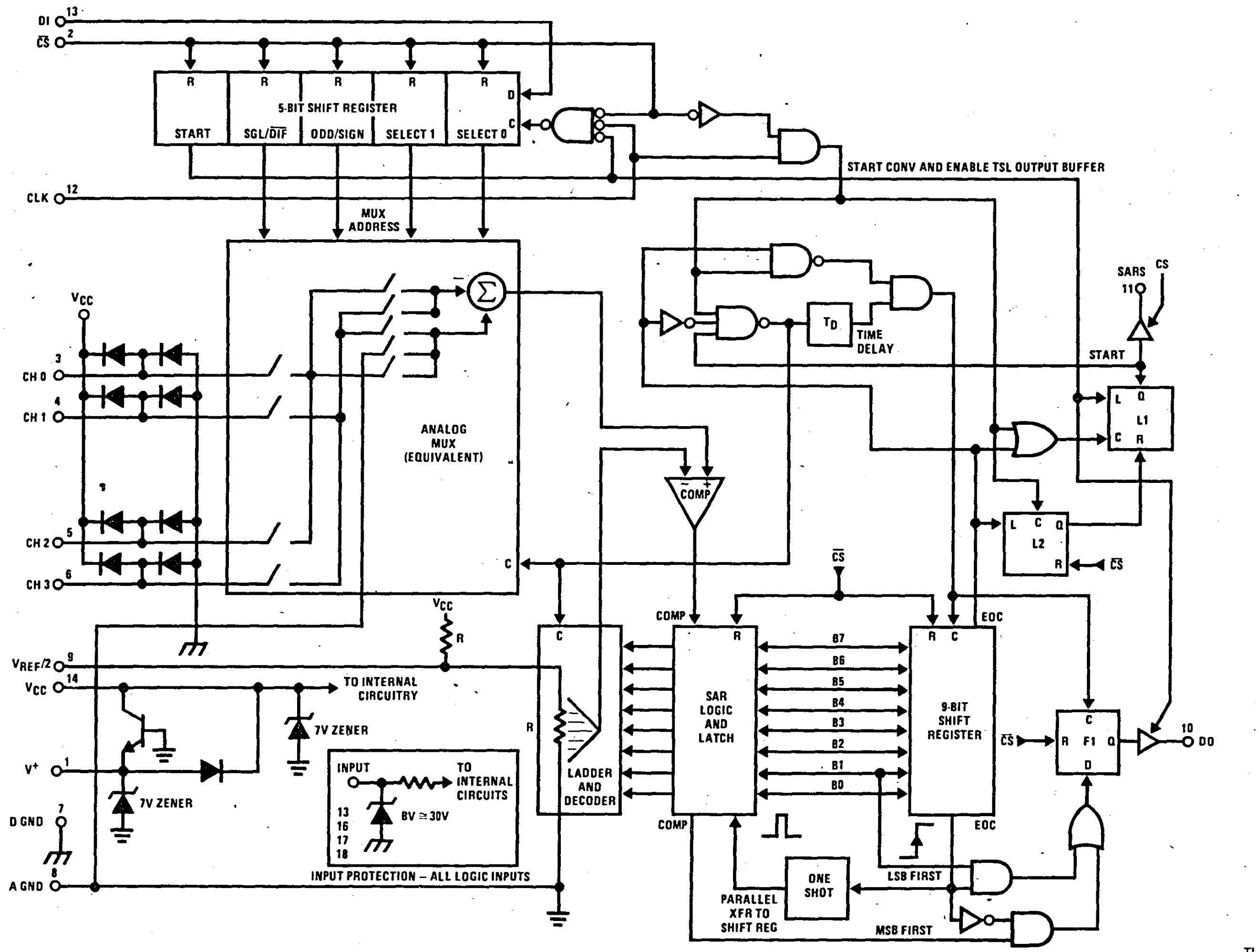
ADC0833 Functional Block Diagram



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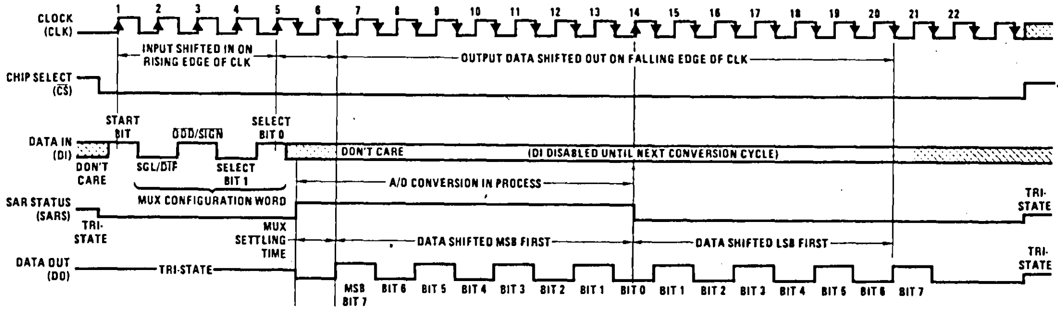
Functional Timing Diagram



TL/H/5607-5

Applications

1.0 MULTIPLEXER ADDRESSING

The design of the ADC0833 utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended (ground referred) or differential inputs. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a differential pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following table. The MUX address is shifted into the converter through the DI line.

TABLE I. MUX ADDRESSING

Single-Ended MUX Mode

Address				Channel #			
SGL/$\overline{DIF}$	$\overline{ODD}$/SIGN	SELECT 1	SELECT 0	0	1	2	3
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

COM is internally ties to a GND

Differential MUX Mode

Address				Channel #			
SGL/$\overline{DIF}$	$\overline{ODD}$/SIGN	SELECT 1	SELECT 0	0	1	2	3
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

6

Applications (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50mV above V_{CC}(typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor;transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagram and Functional Block Diagram and to follow a complete conversion sequence.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 4 bits to be the MUX assignment word.

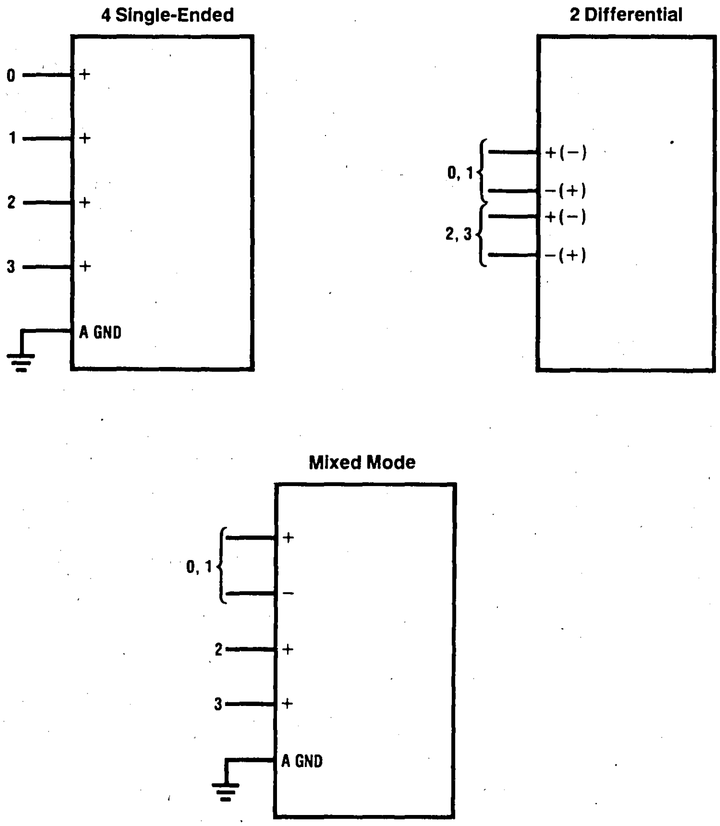


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FIGURE 1. Analog Input Multiplexer Options for the ADC08333

Applications (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1 full clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods, the conversion is completed and the SAB status line returns low to indicate this.

8. If the programmer prefers, the data can be read in an LSB first format. All 8 bits of the result are stored in an output shift register. The conversion result, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

All of the logic inputs can be taken to 15V independent of the magnitude of the supply voltage, V_{CC}.

3.0 REFERENCE CONSIDERATIONS

The ADC0833 is intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, an ADC0834 is a pin-for-pin compatible alternative.

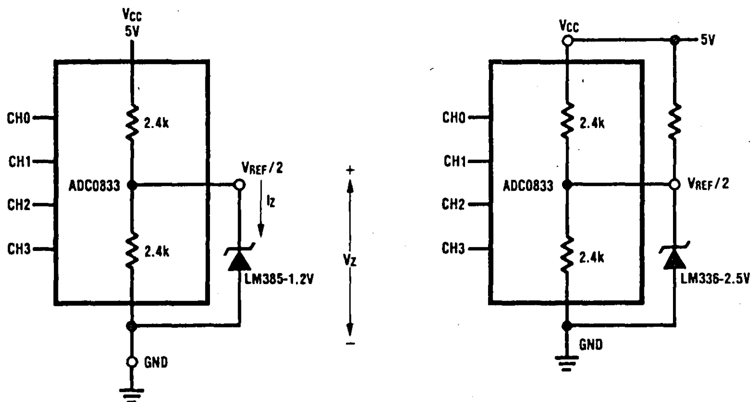
The voltage applied to the $V_{REF}/2$ pin defines the voltage span of the analog input [the difference between $V_{IN}(+)$ and $V_{IN}(-)$] over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+" input and "−" input is approximately *twice* the voltage at the $V_{REF}/2$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The LM385 and LM336 reference diodes are good low current devices to use with these converters. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256\left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)}\right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF}/2$ is the voltage from pin 9 to ground.

The $V_{REF}/2$ pin is the center point of a two resistor divider (each resistor is 2.4 kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors. As shown in *Figure 2,* a reference diode with a voltage less than $V_{CC}/2$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF}/2$ can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



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$V_{FULL\text{-}SCALE} \cong 2.4V$ $\qquad$ $V_{FULL\text{-}SCALE} \cong 5.0V$

Note: No external biasing resistor needed if $V_Z < \frac{V_{CC}}{2}$ and $I_Z \min < \frac{V_{CC}/2 - V_Z}{1.2\,k\Omega}$

FIGURE 2. Reference Biasing Examples

Applications (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{peak}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the %clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ± 1 μA over temperature will create a 1 mV inut error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input as this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transaction.

The full-scale adjustment should be made [with the proper $V_{In}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ fs\ adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The $V_{REF}/2$ voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0833 is the inclusion of a 7V zener diode connected from the V^+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3.*

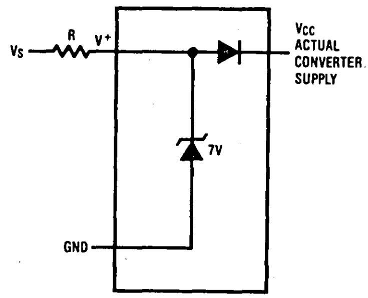

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FIGURE 3. An On-Chip Shunt Regulator Diode

Applications (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4* and *5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 6* and *7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D (~3 mA) and the relatively high clock frequencies used (typically in the range of 10k-400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of 7V. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V+ pin.

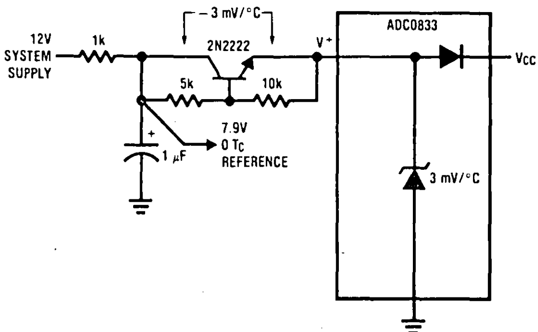

FIGURE 4. Operating with a Temperature Compensated Reference

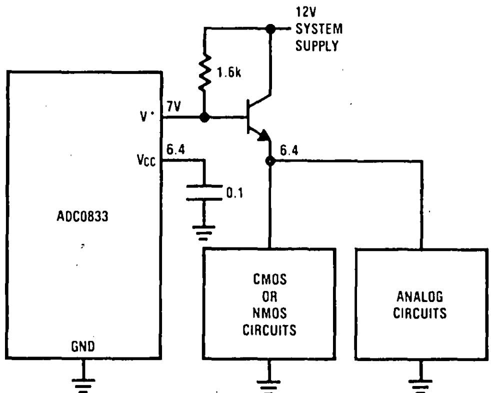

FIGURE 5. Using the A/D as the System Supply Regulator

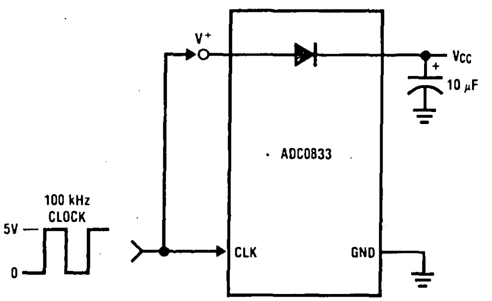

FIGURE 6. Generally V_{CC} from the Converter Clock

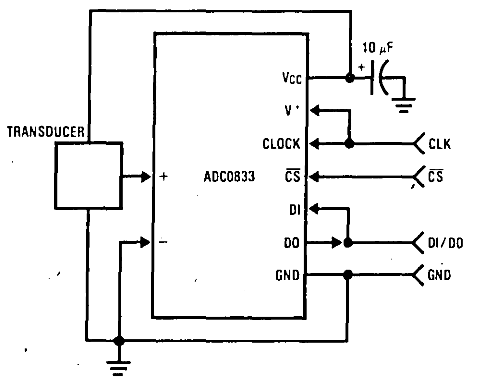

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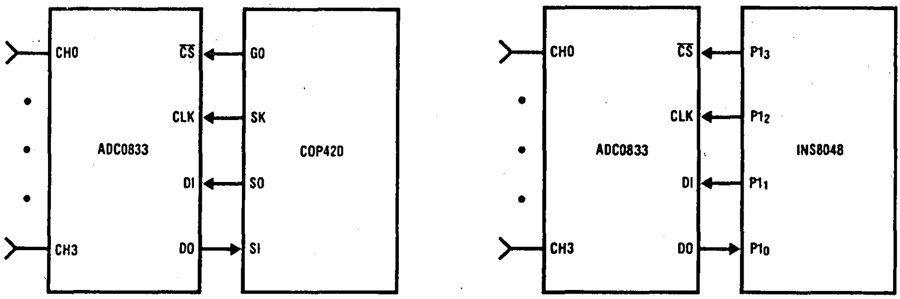
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

6

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



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COP CODING EXAMPLE

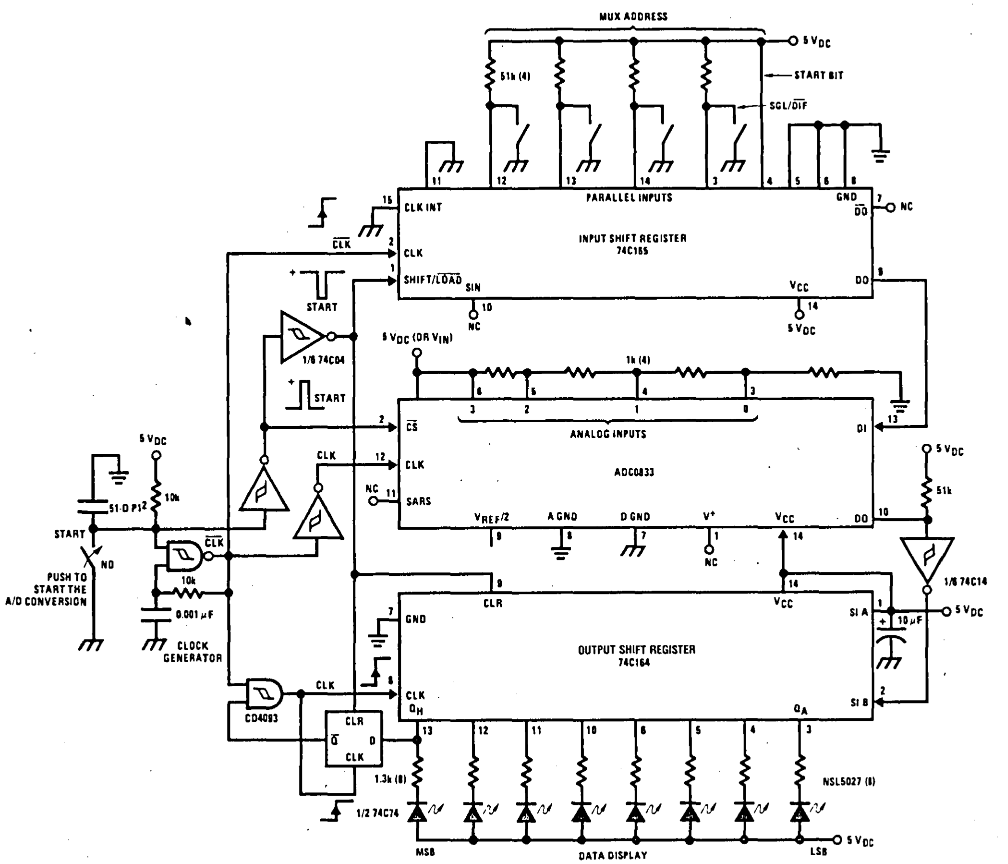
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑ 8 INSTRUCTIONS ↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

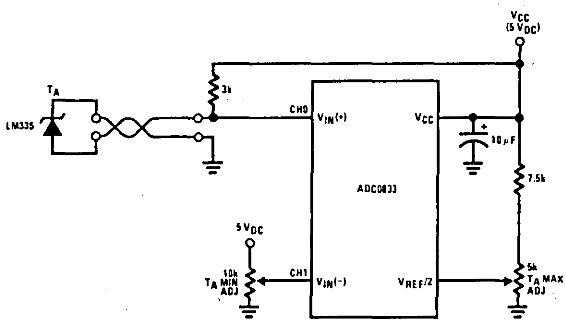
	Mnemonic		Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0833 Evaluation



Low Cost Remote Temperature Sensor



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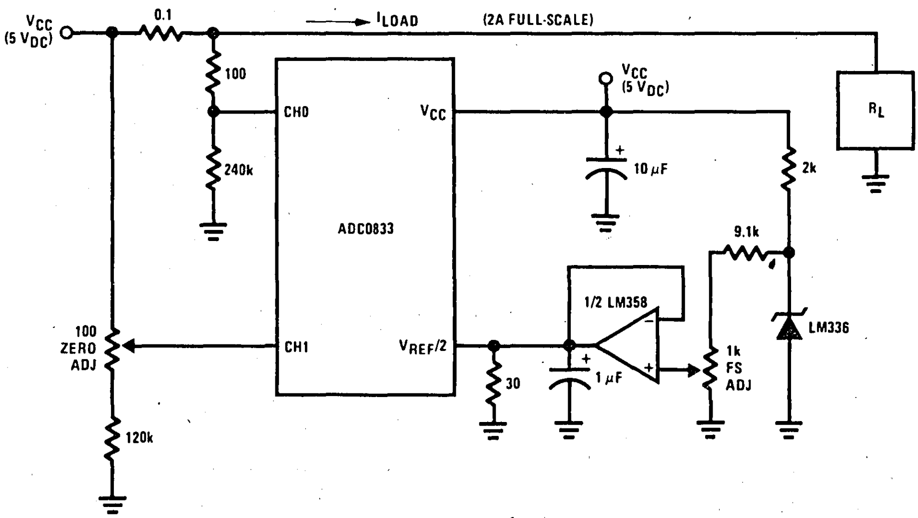
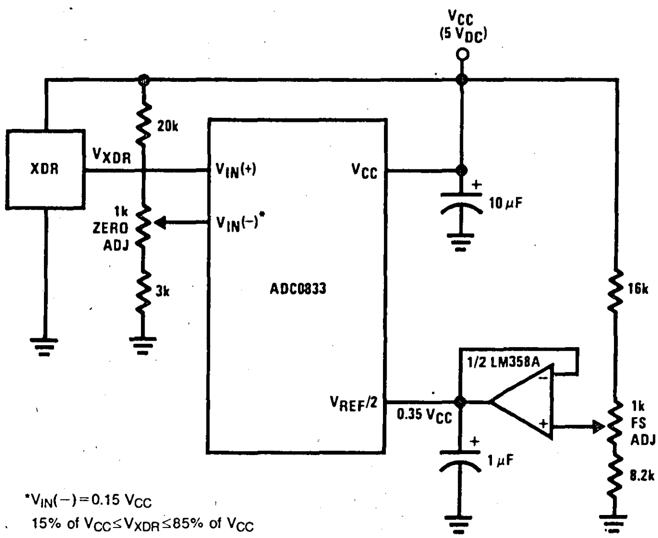
6

Applications (Continued)

Digitizing a Current Flow



Operating with Automotive Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

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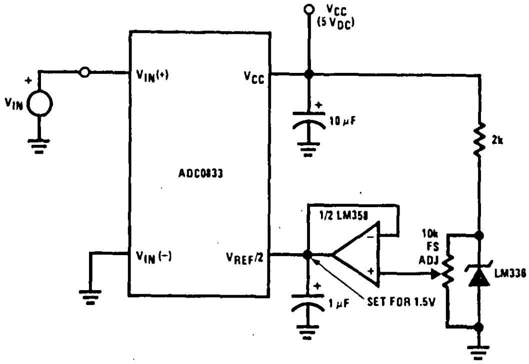
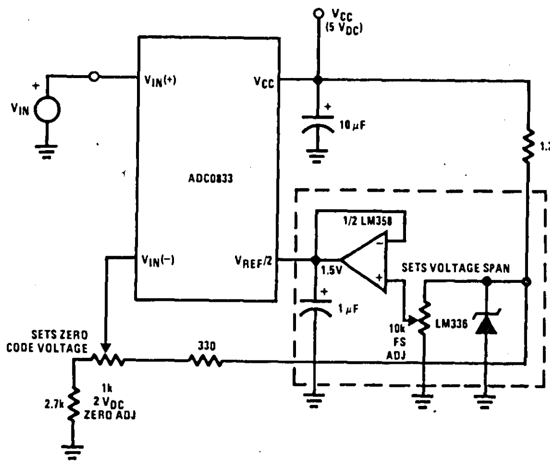
Applications (Continued)

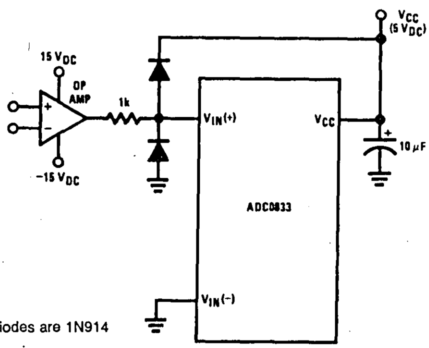
Span Adjust: 0V ≤ V_{IN} ≤ 3V



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

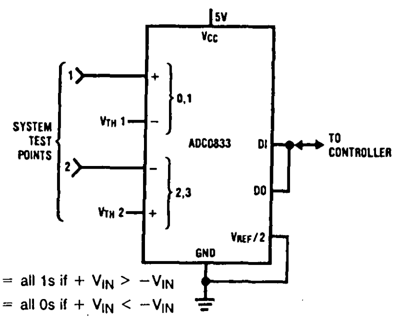


Protecting the Input



Diodes are 1N914

High Accuracy Comparators



DO = all 1s if + V_{IN} > $-V_{IN}$

DO = all 0s if + V_{IN} < $-V_{IN}$

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For additional application ideas, refer to the data sheet for the ADC0831 family of serial data converters.

Ordering Information

Part Number	Temperature Range	Total Unadjusted Error
ADC0833BCJ	−40°C to +85°C	±1//2 LSB
ADC0833BCN	0°C to +70°C	
ADC0833BJ	−55°C to +125°C	
ADC0833CCJ	−40°C to +85°C	±1 LSB
ADC0833CCN	0°C to +70°C	
ADC0833CJ	−55°C to +125°C	

National Semiconductor

ADC0844 8-Bit µP Compatible A/D Converter with 4-Channel Multiplexer

General Description

The ADC0844 is a CMOS 8-bit successive approximation A/D converter with a versatile analog input multiplexer. The 4-channel multiplexer can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common-mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

This A/D is designed to operate from the control bus of the NSC800™ and the wide variety of 8080 µP derivatives. TRI-STATE® output latches that directly drive the data bus permit this A/D to be configured as a memory location or as an I/O device to the microprocessor with no interface logic necessary.

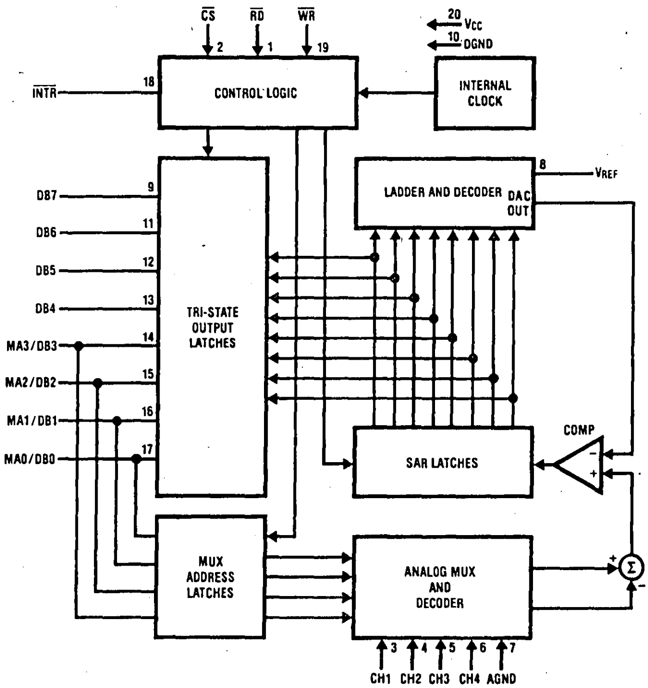
Features

- Compatible with 8080 µP derivatives—no interface logic needed
- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- T^2L/MOS input/output compatible
- 0.3″ standard width 20-pin DIP

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	10 mW
■ Conversion Time	40 µS

Block and Connection Diagrams



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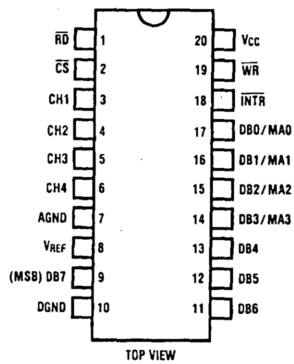
Dual-In-Line Package



TL/H/5016-2

See Ordering Information

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	6.5V
Voltage	
Logic Control Inputs	−0.3V to +15V
At Other Inputs and Outputs	−0.3V to V_{CC}+0.3V
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0844BCN, ADC0844CCN	0°C ≤ T_A ≤ 70°C
ADC0844BCJ, ADC0844CCJ	−40°C ≤ T_A ≤ 85°C
ADC0844BJ, ADC0844CJ	−55°C ≤ T_A ≤ 125°C

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_j = 25°C.

Parameter	Conditions	ADC0844BJ, ADC0844BCJ ADC0844CJ, ADC0844CCJ			ADC0844BCN, ADC0844CCN			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	V_{REF} = 5.00 V_{DC} (Note 3)							
ADC0844BCN						±½	±½	LSB
ADC0844BJ, BCJ			**±½**					LSB
ADC0844CCN						±1	±1	LSB
ADC0844CJ, CCJ			**±1**					LSB
Minimum Reference Input Resistance		2.4	**1.1**		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance		2.4	**4.1**		2.4	3.8	**4.1**	kΩ
Maximum Common-Mode Input Range	(Note 4)		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Range	(Note 4)		**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Differential Mode	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity	V_{CC} = 5V±5%	±1/16	**±⅛**		±1/16	±⅛	**±⅛**	LSB
Off Channel Leakage Current	(Note 8) On Channel = 5V, Off Channel = 0V		**−1**			−0.1	**−1**	μA
	On Channel = 0V, Off Channel = 5V		**1**			0.1	**1**	μA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN} = 5.0V	0.005	**1**		0.005		**1**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	**−1**		−0.005		**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.5**			2.8 4.6	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	**−3** **3**		−0.01 0..01	−0.3 0.3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SNK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	**2.5**		1	2.3	**2.5**	mA

AC Characteristics

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Units
t_C, Maximum Conversion Time (See Graph)		30	40		µS
$t_{W(\overline{WR})}$, Minimum $\overline{WR}$ Pulse Width	(Note 9)	50		150	ns
t_{ACC}, Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF (Note 9)	145		225	ns
t_{1H}, t_{0H}, TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (Note 9)	125		200	ns
t_{WI}, t_{RI}, Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$	(Note 9)	200		400	ns
t_{DS}, Minimum Data Set-Up Time	(Note 9)	50		100	ns
t_{DH}, Minimum Data Hold Time	(Note 9)	0		50	ns
C_{IN}, Capacitance of Logic Inputs		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Guaranteed and 100% production tested.

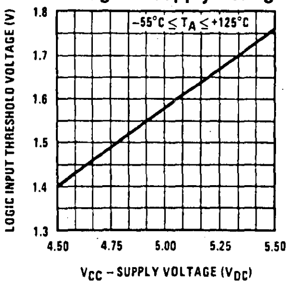
Note 7: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 8: Off channel leakage current is measured after the channel selection.

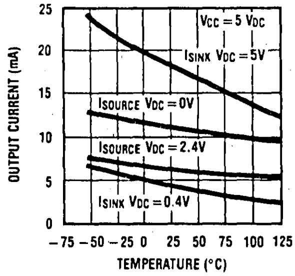
Note 9: The temperature coefficient is 0.3%/°C.

Typical Performance Characteristics

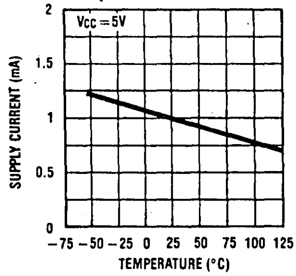
Logic Input Threshold Voltage vs Supply Voltage



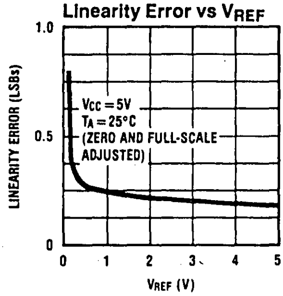
Output Current vs Temperature



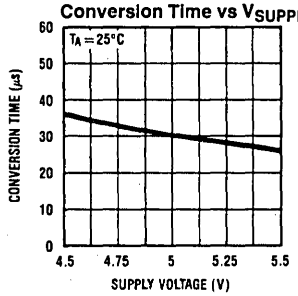
Power Supply Current vs Temperature



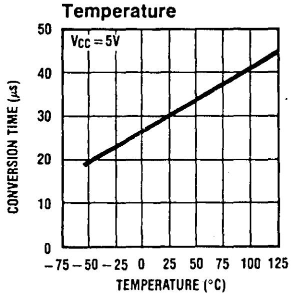
Linearity Error vs V_{REF}



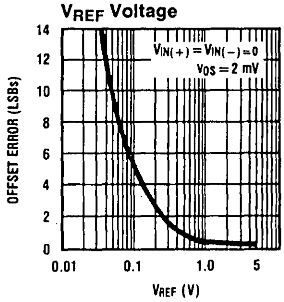
Conversion Time vs V_{SUPPLY}



Conversion Time vs Temperature



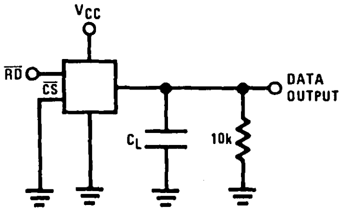
Unadjusted Offset Error vs V_{REF} Voltage



TL/H/5016–3

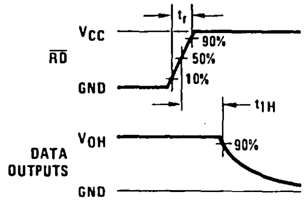
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/5016-4

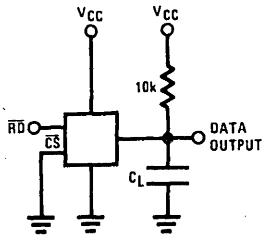
t_{1H}, $C_L = 10$ pF



TL/H/5016-5

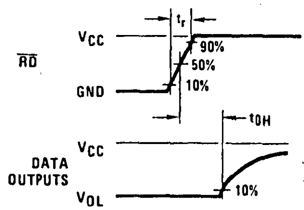
$t_r = 20$ ns

t_{0H}



TL/H/5016-6

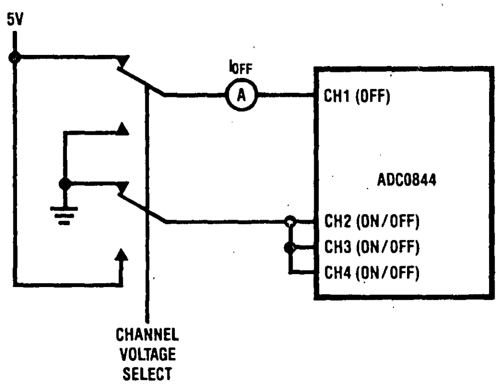
t_{0H}, C_L 10 pF



TL/H/5016-7

$t_r = 20$ ns

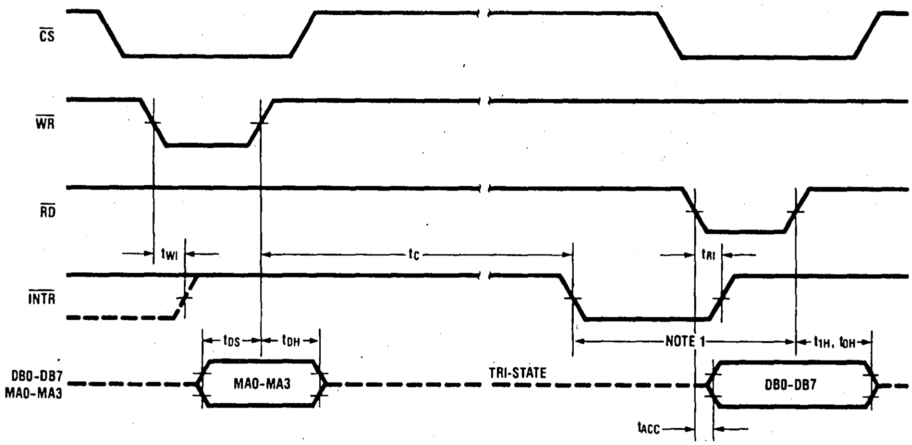
Leakage Current Test Circuit



TL/H/5016-8

Timing Diagrams

Programming New Channel Configuration and Starting a Conversion



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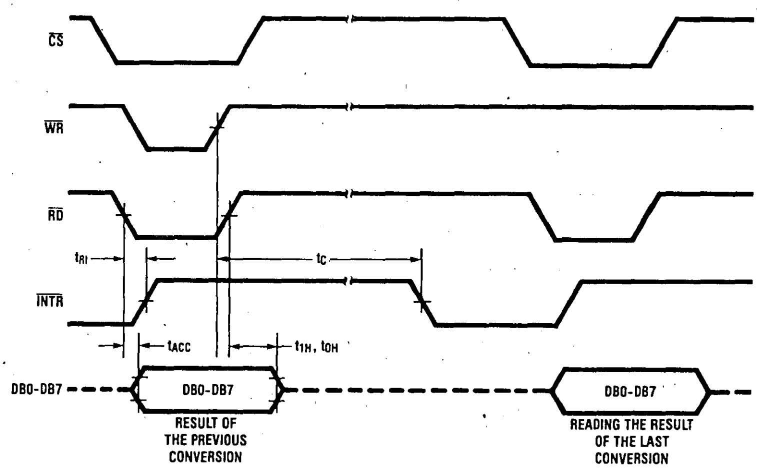
Note 1: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of $\overline{\text{INTR}}$.

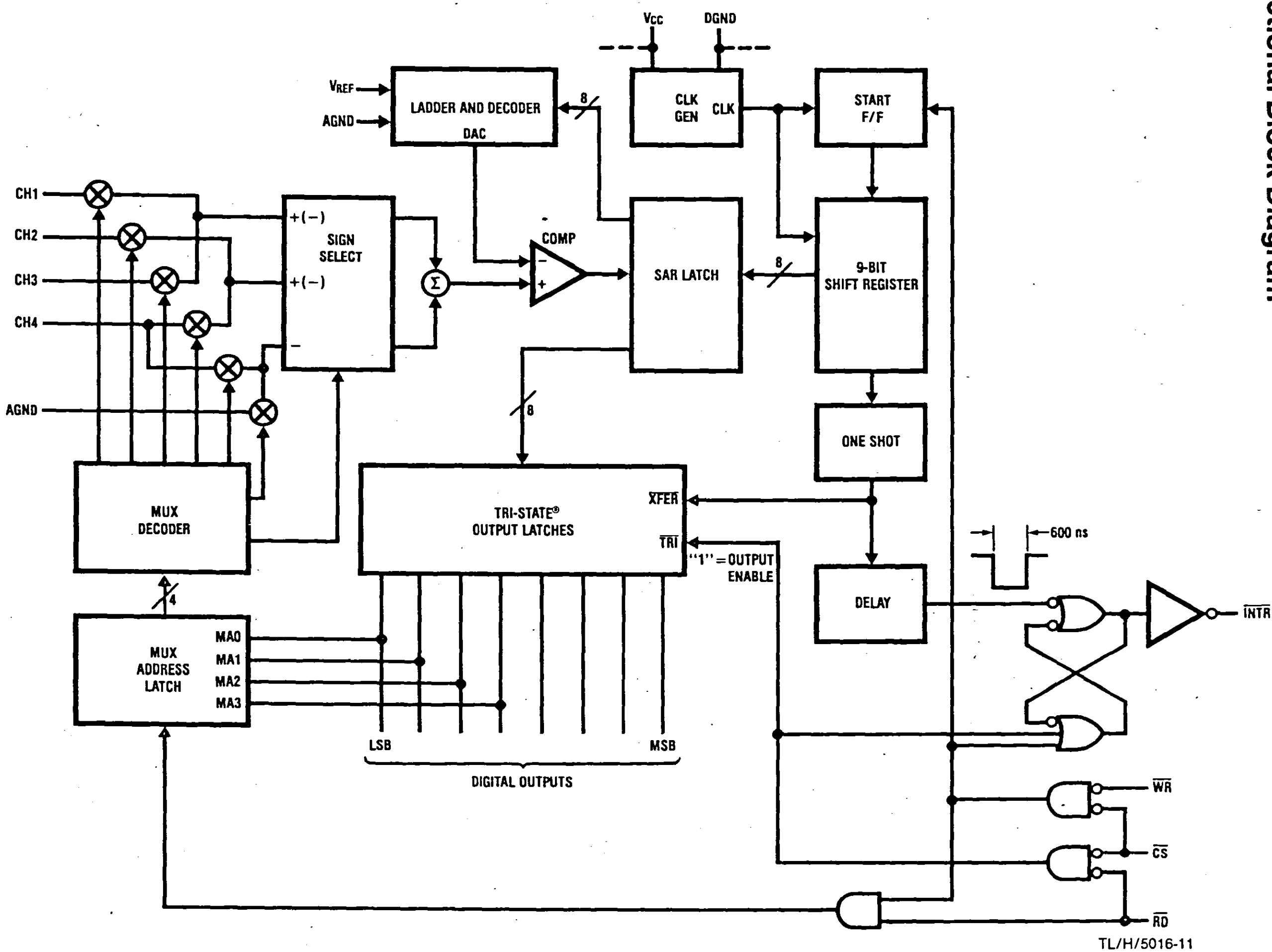
Note 2: MA stands for MUX address.

Using the Previously Selected Channel Configuration and Starting a Conversion



TL/H/5016-10

Functional Block Diagram



TL/H/5016-11

Functional Description

The ADC0844 contains a 4-channel analog multiplexer (MUX) which can be configured in a single-ended, differential, or pseudo-differential mode (Table 1). The specific mode is selected by loading the MUX address latch with the proper address. Inputs to the MUX address latch (MA0-MA3) are common with data bus lines (DB0-DB3) and are enabled when the $\overline{RD}$ line is high. A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$, with $\overline{RD}$ high, strobes the data on the MA0/DB0-MA3/DB3 inputs into the MUX address latch to select a new input configuration and start a conversion. If the $\overline{RD}$ line is held low during the entire low period of $\overline{WR}$ the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ($t_C \leq 40\ \mu S$), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and outputs the conversion result on the data lines (DB0-DB7).

Applications Information

1.0 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sample-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

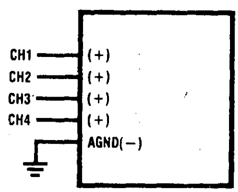
A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-

TABLE 1. ADC0844 MUX ADDRESSING

MUX Address				$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel #					MUX Mode
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND	
X	L	L	L	L		H	+	−				Differential
X	L	L	H	L	⊔	H	−	+				
X	L	H	L	L		H			+	−		
X	L	H	H	L		H			−	+		
L	H	L	L	L		H	+				−	Single-Ended
L	H	L	H	L	⊔	H		+			−	
L	H	H	L	L		H			+		−	
L	H	H	H	L		H				+	−	
H	H	L	L	L		H	+			−		Pseudo-Differential
H	H	L	H	L	⊔	H		+		−		
H	H	H	L	L		H			+	−		
X	X	X	X	L	⊔	L	Previous Channel Configuration					

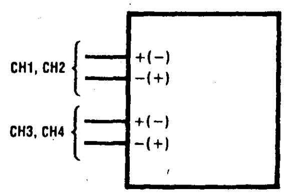
X = don't care

4 Single-Ended



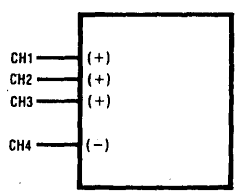
TL/H/5016-12

2 Differential



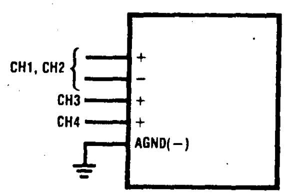
TL/H/5016-13

3 Pseudo-Differential



TL/H/5016-14

Combined



TL/H/5016-15

FIGURE 1. Analog Input Multiplexer Options

Applications Information (Continued)

ended, or pseudo-differential (*Figure 1*). In the differential mode, the channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1-CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1-CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 2.4 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 2a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 2b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

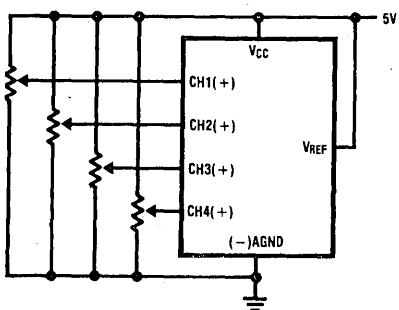
$$V_{ERROR(MAX)} = V_{peak}\,(2\pi\,f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, Vpeak is its peak voltage value and t_C is the conversion time.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

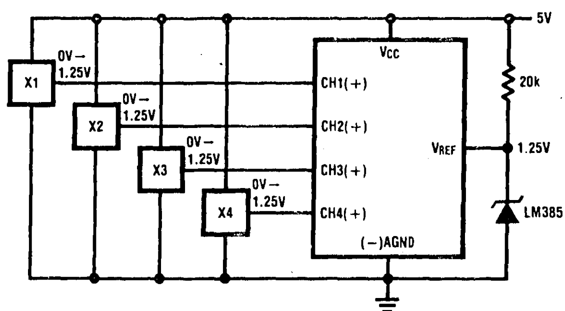
3.2 Input Current

Due to the sampling nature of the analog inputs short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.



TL/H/5016-16

a) Ratiometric



TL/H/5016-17

b) Absolute with a Reduce Span

FIGURE 2. Referencing Examples

Applications Information (Continued)

3.3 Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of ± 1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

4.0 OPTIONAL ADJUSTMENTS

4.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This is useful for either differential or pseudo-differential modes of input channel configuration.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}).

4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (+) voltage applied] by forcing a voltage to the $V_{IN}(-)$ input which is given by:

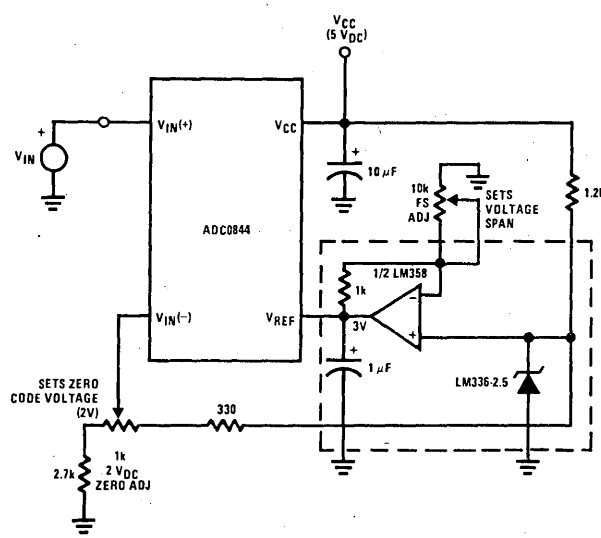
$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

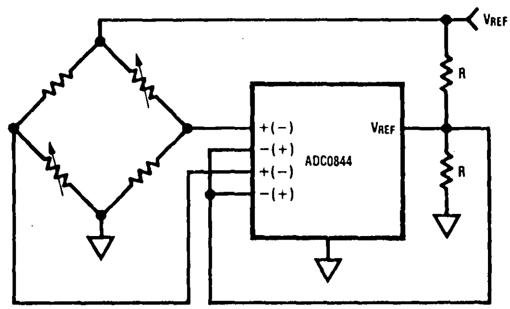
Zero-Shift and Span Adjust (2V ≤ V_{IN} ≤ 5V)



TL/H/5016-18

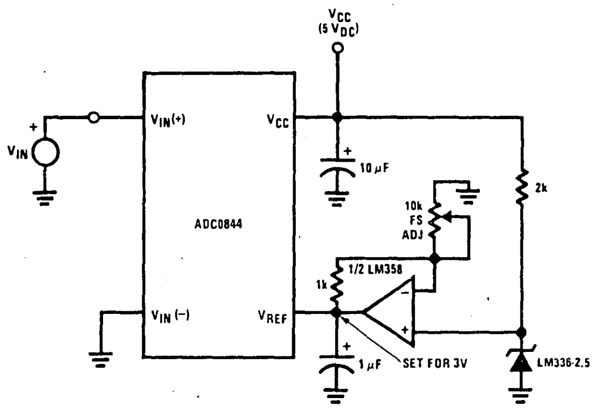
Applications Information (Continued)

Differential Voltage Input 9-Bit A/D



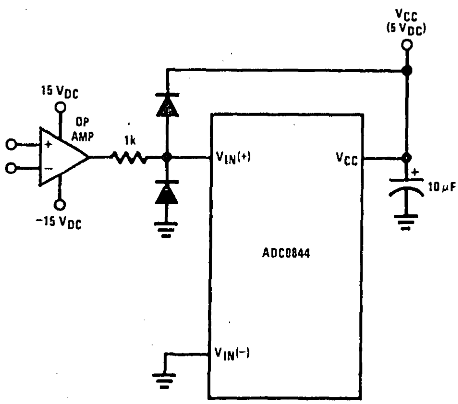
TL/H/5016-19

Span Adjust 0V ≤ V_{IN} ≤ 3V



TL/H/5016-20

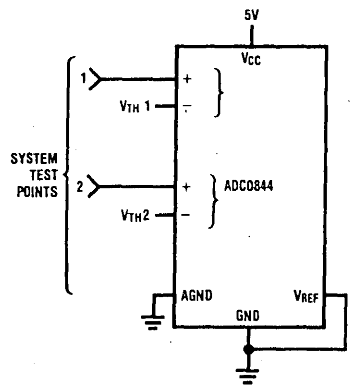
Protecting the Input



TL/H/5016-21

Diodes are 1N914

High Accuracy Comparators



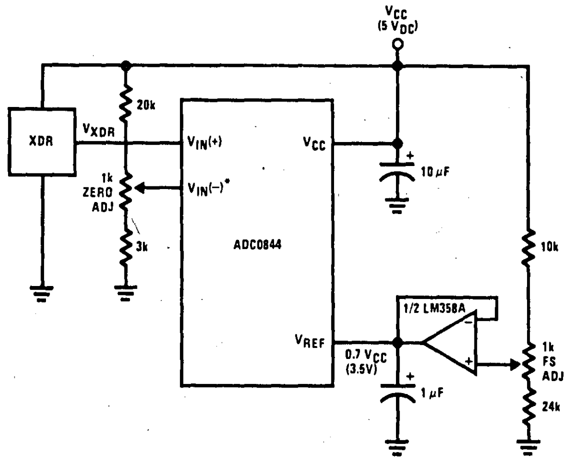
TL/H/5016-22

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$

DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

Applications Information (Continued)

Operating with Automotive Ratiometric Transducers

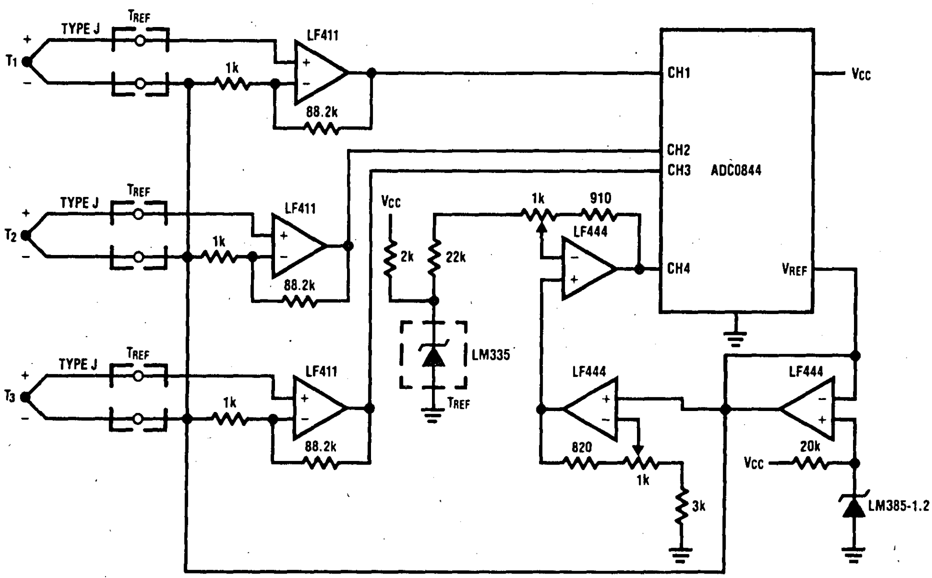


TL/H/5016-23

$^{*}V_{IN}(-) = 0.15\ V_{CC}$

$15\%\ of\ V_{CC} \le V_{XDR} \le 85\%\ of\ V_{CC}$

Converting 3 Thermocouples with only One Cold-Junction Compensator

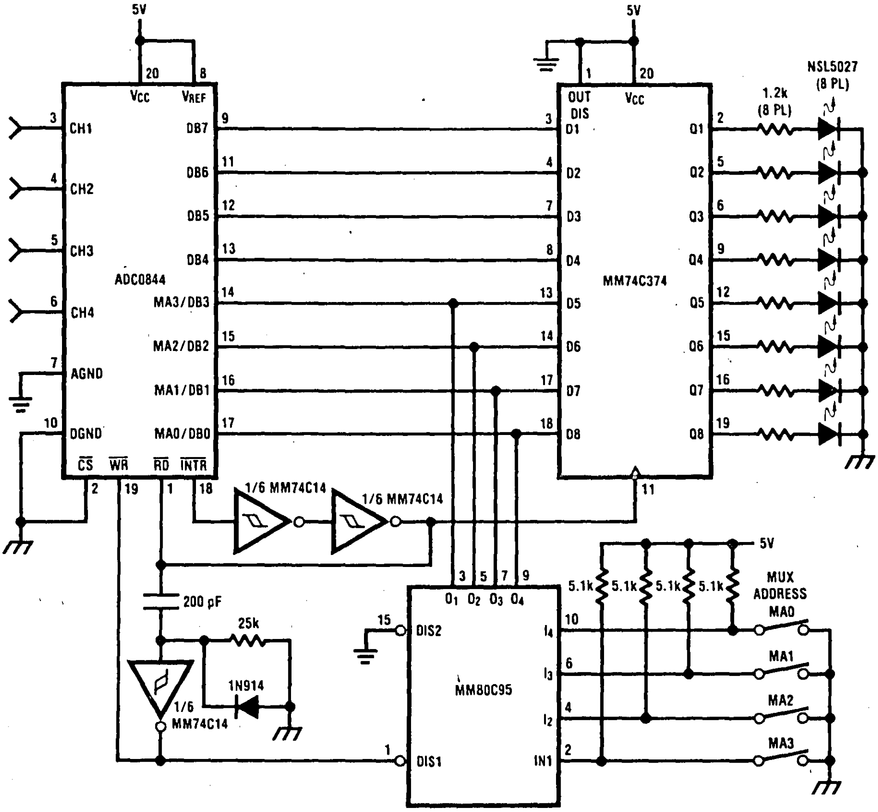


TL/H/5016-24

Uses the pseudo-differential mode to keep the differential inputs constant with changes in reference temperature (T_{REF}).

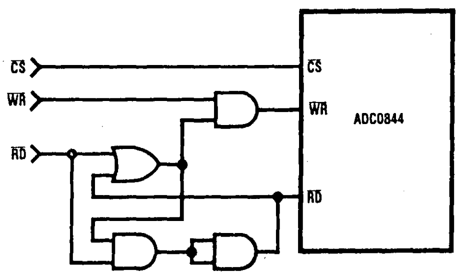
Applications Information (Continued)

A Stand Alone Circuit



TL/H/5016-25

Start a Conversion without Updating the Channel Configuration



TL/H/5016-26

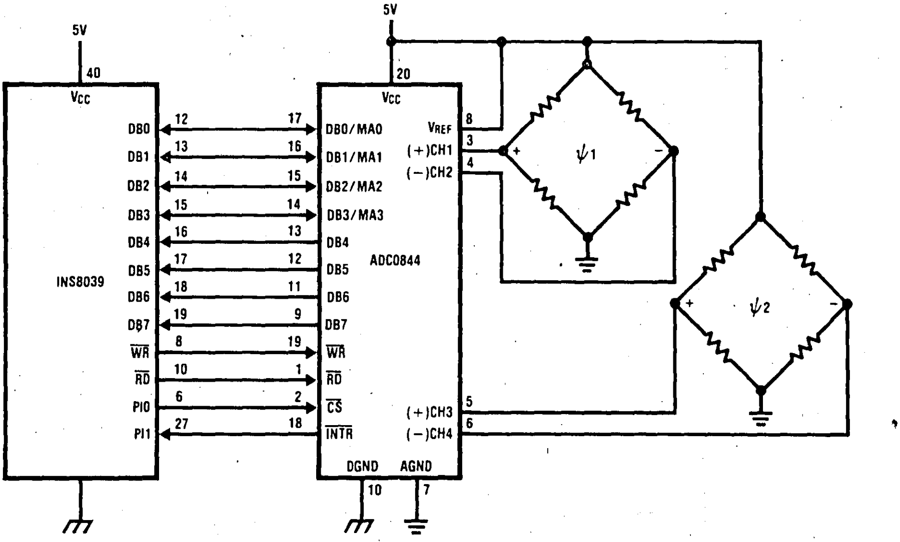
$\overline{CS}$•$\overline{WR}$ will update the channel configuration and start a conversion.

$\overline{CS}$•$\overline{RD}$ will read the conversion data and start a new conversion without updating the channel configuration.

Waiting for the end of this conversion is not necessary. A $\overline{CS}$•$\overline{WR}$ can immediately follow the $\overline{CS}$•$\overline{RD}$.

Applications Information (Continued)

ADC0844—INS8039 Interface



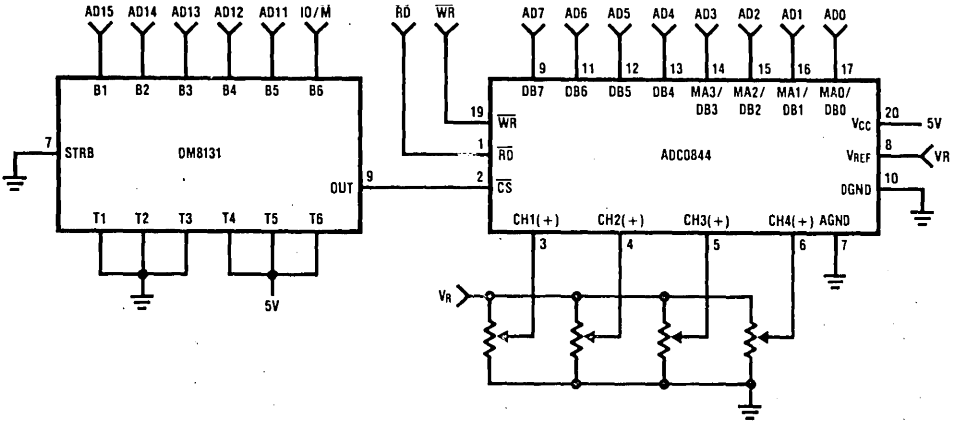
TL/H/5016-27

SAMPLE PROGRAM FOR ADC0844—INS8039 INTERFACE CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

```
                                ORG     0H
0000    04 10                   JMP     BEGIN        ;START PROGRAM AT ADDR 10
                                ORG     10H          ;MAIN PROGRAM
0010    B9 FF       BEGIN:      MOV     R1,#0FFH     ;LOAD R1 WITH A UNUSED ADDR
                                                     ;LOCATION
0012    B8 20                   MOV     R0#20H       ;A/D DATA ADDRESS
0014    89 FF                   ORL     P1,#0FFH     ;SET PORT 1 OUTPUTS HIGH
0016    23 00                   MOV     A,00H        ;LOAD THE ACC WITH A/D MUX DATA
                                                     ;CH1 AND CH2 DIFFERENTIAL
0018    14 50                   CALL    CONV         ;CALL THE CONVERSION SUBROUTINE
001A    23 02                   MOV     A,#02H       ;LOAD THE ACC WITH A/D MUX DATA
                                                     ;CH3 AND CH4 DIFFERENTIAL
001C    18                      INC     R0           ;INCREMENT THE A/D DATA ADDRESS
001D    14 50                   CALL    CONV         ;CALL THE CONVERSION SUBROUTINE

                                ;CONTINUE MAIN PROGRAM

                                ;CONVERSION SUBROUTINE
                                ;ENTRY:ACC—A/D MUX DATA
                                ;EXIT: ACC—CONVERTED DATA

                                ORG     50H
0050    99 FE       CONV:       ANL     P1,#0FEH     ;CHIP SELECT THE A/D
0052    91                      MOVX    @R1,A        ;LOAD A/D MUX & START CONVERSION
0053    09          LOOP:       IN      A,P1         ;INPUT INTR STATE
0054    32 53                   JB1     LOOP         ;IF INTR = 1 GOTO LOOP
0056    81                      MOVX    A,@R1        ;IF INTR = 0 INPUT A/D DATA
0057    89 01                   ORL     P1 &01H      ;CLEAR THE A/D CHIP SELECT
0059    A0                      MOV     @R0,A        ;STORE THE A/D DATA
005A    83                      RET                  ;RETURN TO MAIN PROGRAM
```

Applications Information (Continued)

I/O Interface to NSC800



TL/H/5016-28

SAMPLE PROGRAM FOR ADC0844—NSC800 INTERFACE

```
0008                 NCONV      EQU    8
000F                 DEL        EQU    15              ;DELAY 50 µsec CONVERSION
001F                 CS         EQU    1FH             ;THE BOARD ADDRESS
3C00                 ADDTA      EQU    003CH           ;START OF RAM FOR A/D
                                                       ;DATA
0000'   0B 0A 09     MUXDTA:    DB     0BH,0AH,09H     ;MUX DATA
0003'   08                      DB     08H
0004'   0E 1F        START:     LD     C,CS
0006'   06 08                   LD     B,NCONV
0008'   21 0000'                LD     HL,MUXDTA
000B'   11 003C                 LD     DE,ADDTA
000E'   ED A3        STCONV:    OUTI                   ;LOAD A/D'S MUX DATA
                                                       ;AND START A CONVERSION
0010'   EB                      EX     DE,HL           ;HL=RAM ADDRESS FOR THE
                                                       ;A/D DATA
0011'   3E 0F                   LD     A,DEL
0013'   3D           WAIT:      DEC    A               ;WAIT 50 µsec FOR THE
0014'   C2 0013'                JP     NZ,WAIT         ;CONVERSION TO FINISH
0017'   ED A2                   INI                    ;STORE THE A/D'S DATA
                                                       ;CONVERTED ALL INPUTS?
0019'   EB                      EX     DE,HL
001A'   C2 000E'                JP     NZ,STCONV       ;IF NOT GOTO STCONV

                                END
```

Note: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH4 a conversion is started, then a 50 µS wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.

Ordering Information

Temperature Range	0°C to 70°C	−40°C to +85°C	−55°C to +125°C
±½ LSB Unadjusted	ADC0844BCN	ADC0844BCJ	ADC0844BJ
±1 LSB Unadjusted	ADC0844CCN	ADC0844CCJ	ADC0844CJ
Package Outline	N20A—Molded DIP	J20A—CERDIP	J20A—CERDIP

National Semiconductor

PRELIMINARY

ADC1001, ADC1021 10-Bit μP Compatible A/D Converters

General Description

The ADC1001 and ADC1021 are CMOS, 10-bit successive approximation A/D converters. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

The 24-pin ADC1021 outputs 10 bits parallel and is intended for interface to a 16-bit data bus.

A differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 10 bits of resolution.

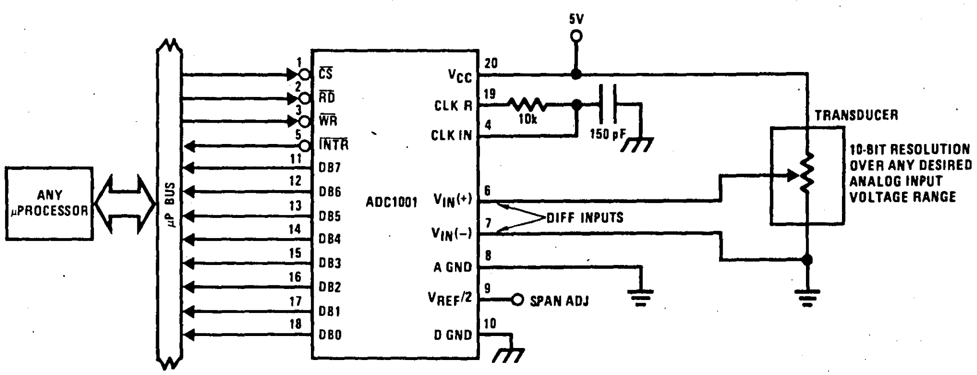
Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D
- Compatible with NSC800 and 8080 μP derivatives—no interfacing logic needed—access time 170 ns
- Easily interfaced to 6800 μP derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3″ standard width 20-pin DIP package or 24 pins with 10-bit parallel output

Key Specifications

- Resolution: 10 bits
- Linearity error: ±1 LSB
- Conversion time: 200μS

Typical Application



TL/H/5675-1

Ordering Information

Temperature Range	0°C to + 70°C		−40°C to +85°C	
Order Number	ADC1001CCD-1	ADC1021CCD-1	ADC1001CCD	ADC1021CCD
Package Outline	D20A	D24C	D20A	D24C

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Logic Control Inputs	−0.3V to +18V
Voltage at Other Inputs and Outputs	−0.3V to (V_{CC}+0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1001CCD	$-40°C \le T_A \le +85°C$
ADC1021CCD	
ADC1001CCD-1	$0°C \le T_A \le +70°C$
ADC1021CCD-1	
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Converter Characteristics

Converter Specifications: V_{CC}=5 V_{DC}, $V_{REF}/2$=2.500 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=410 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC1001C, ADC1021C: Linearity Error Zero Error Full-Scale Error				 ±1 ±2 ±2	 LSB LSB LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	3.2	5.2		KΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/8		LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC}±5% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/8		LSB

AC Electrical Characteristics

Timing Specifications: V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

	Parameter	Conditions	Min	Typ	Max	Units
T_c	Conversion Time	(Note 5) f_{CLK}=410 kHz	82 200		89 217	$1/f_{CLK}$ μS
f_{CLK}	Clock Frequency	(Note 8)	100		1260	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 V_{DC}, f_{CLK}=410 kHz			4600	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$=0 V_{DC} (Note 6)	150			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		170	300	ns
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
t_{1rs}	$\overline{INTR}$ to 1st Read Set-Up Time		550	400		ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5\ V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except CLK IN)	$V_{CC}=5.25\ V_{DC}$	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except CLK IN)	$V_{CC}=4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN}=5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" input Current (All Inputs)	$V_{IN}=0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN						
V_T+	CLK IN Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
OUTPUTS AND $\overline{INTR}$						
$V_{OUT}(0)$	Logical "0" Output Voltage	$I_{OUT}=1.6$ mA, $V_{CC}=4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-360\ \mu A$, $V_{CC}=4.75\ V_{DC}$ $I_O=-10\ \mu A$, $V_{CC}=4.75\ V_{DC}$	2.4 4.5			V_{DC} V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT}=0.4\ V_{DC}$ $V_{OUT}=5\ V_{DC}$		0.1 0.1	−100 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to GND, $T_A=25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A=25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	$f_{CLK}=410$ kHz, $V_{REF}/2=$ NC, $T_A=25°C$ and $\overline{CS}=1$		1.5	2.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be all zeros. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near fullscale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 1*.

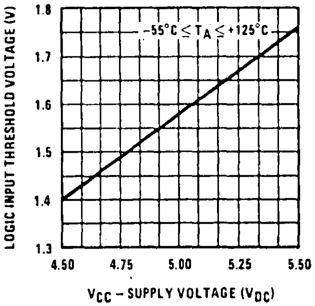
Note 6: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).

Note 7: All typical values are for $T_A=25°C$.

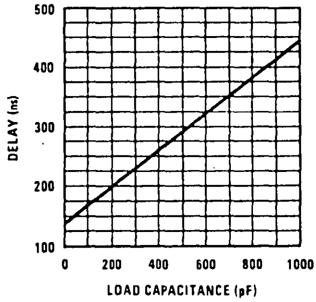
Note 8: Accuracy is guaranteed at $f_{CLK}=410$ kHz. At higher clock frequencies accuracy can degrade.

Typical Performance Characteristics

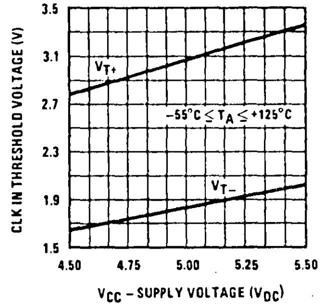
Logic Input Threshold Voltage vs Supply Voltage



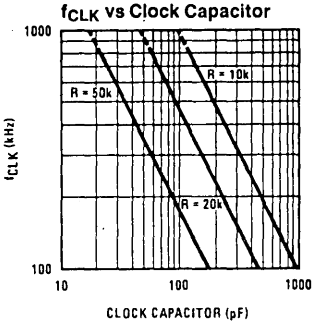
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



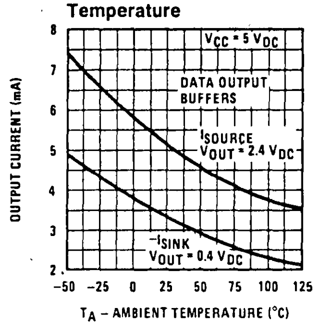
CLK IN Schmitt Trip Levels vs Supply Voltage



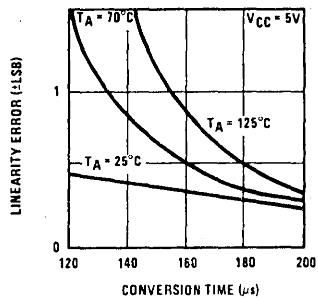
f_{CLK} vs Clock Capacitor



Output Current vs Temperature



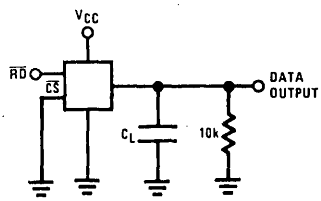
Typical Linearity Error vs Conversion Time



TL/H/5675–2

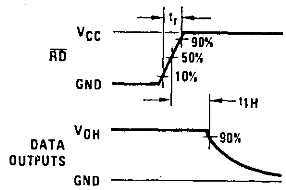
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/5675–3

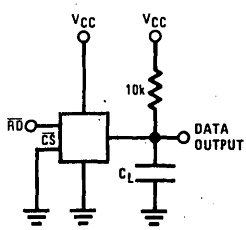
t_{1H}, C_L = 10 pF



TL/H/5675–4

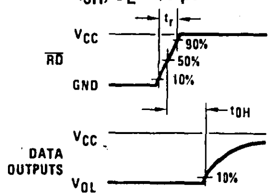
t_r = 20 ns

t_{0H}



TL/H/5675–5

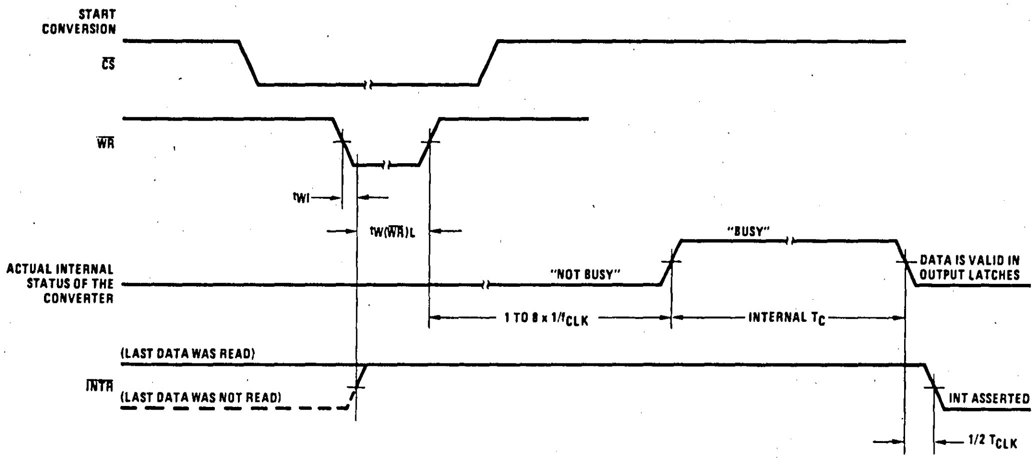
t_{0H}, C_L = 10 pF



TL/H/5675–6

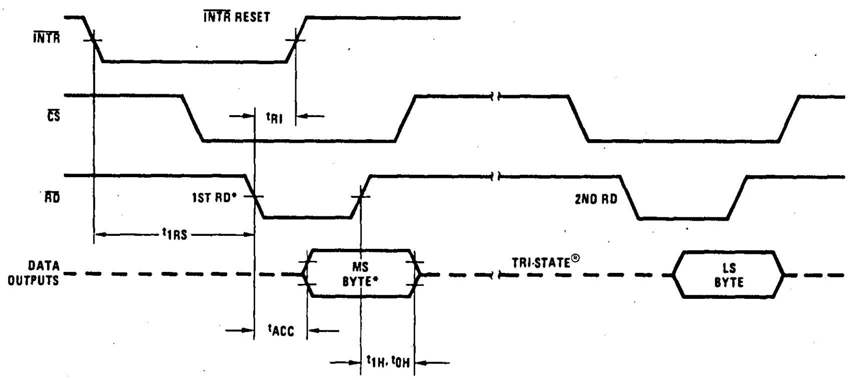
t_r = 20 ns

Timing Diagrams



TL/H/5675-7

Output Enable and Reset $\overline{INTR}$



TL/H/5675-8

*The 24-pin ADC1021 outputs all 10 bits on each RD.

Note: All timing is measured from the 50% voltage points.

BYTE SEQUENCING FOR THE 20-PIN ADC1001

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Functional Description

The ADC1001, ADC1021 are mechanized using an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network, are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog difference input voltage [$V_{IN}(+)-V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ inut with $\overline{CS}=0$. To insure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 1*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, which allows the conversion process to continue. If the set signal were to still be present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When this XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

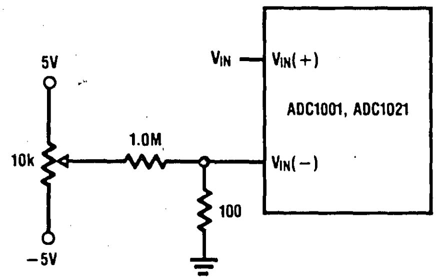
Note that this $\overline{SET}$ control of the INTR F/F remains low for aproximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

Zero and Full-Scale Adjustment

Zero error can be adjusted as shown in *Figure 2*. $V_{IN}(+)$ is forced to +2.5 mV (+½ LSB) and the potentiometer is adjusted until the digital output code changes from 00 0000 0000 to 00 0000 0001.

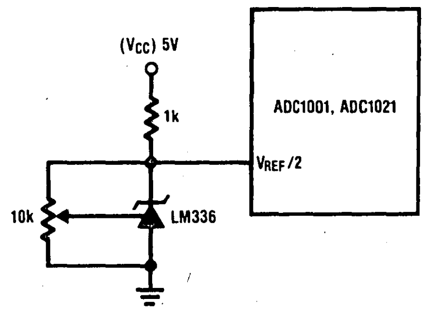
Full-scale is adjusted as shown in *Figure 3*, with the $V_{REF}/2$ input. With $V_{IN}(+)$ forced to the desired full-scale voltage less 1½ LSBs ($V_{FS}-1½$ LSBs), $V_{REF}/2$ is adjusted until the digital output code changes from 11 1111 1110 to 11 1111 1111.



TL/H/5675-9

NOTE: $V_{IN}(-)$ should be biased so that $V_{IN}(-) \geq -0.05V$ when potentiometer wiper is set at most negative voltage position.

FIGURE 2. Zero Adjust Circuit

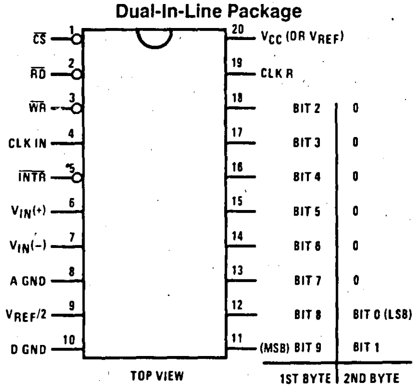


TL/H/5675-10

FIGURE 3. Full-Scale Adjust

Connection Diagrams

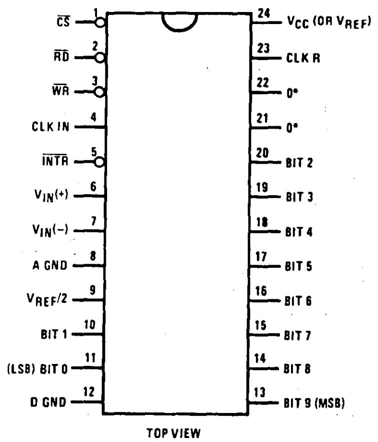
ADC1001 (for an 8-bit data bus)
Dual-In-Line Package



TL/H/5675–11

See Ordering Information

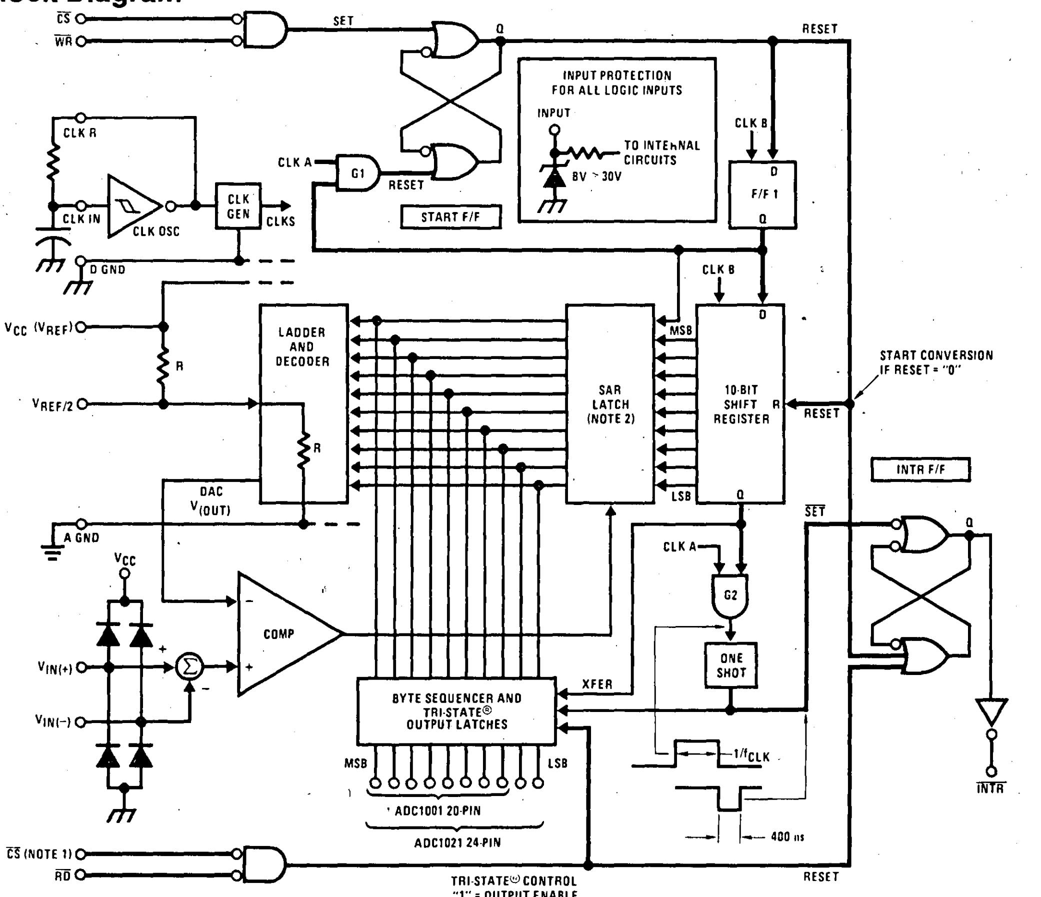
ADC1021 (for all 10-bit outputs in parallel)
Dual-In-Line Package



TL/H/5675–12

*TRI-STATE® output buffers which output 0 during $\overline{RD}$.

Block Diagram



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

TL/H/5675–13

FIGURE 1

National Semiconductor

PRELIMINARY

ADC3511 3½-Digit Microprocessor Compatible A/D Converter
ADC3711 3¾-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

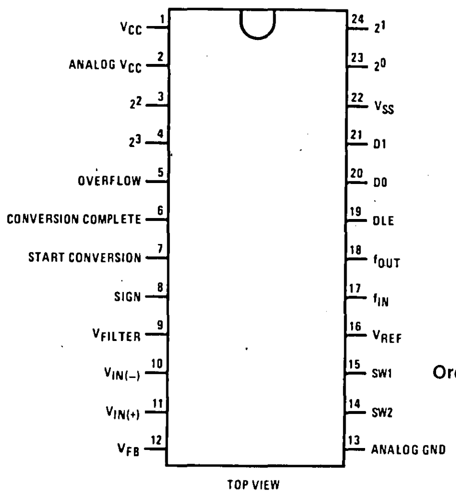
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



Order Number ADC3511CCN or ADC3711CCN
NS Package N24A

TL/H/5678-1

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A=25°C$	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics ADC3511CC, ADC3711CC

$4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$, unless otherwise specified.

	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		$V_{CC}-0.6$			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except 2^0, 2^1, 2^2, 2^3)	$I_O=360\mu A$	$V_{CC}-0.4$			V
$V_{OUT(1)}$	Logical "1" Output Voltage (2^0, 2^1, 2^2, 2^3)	$I_O=360\mu A$	$V_{CC}-1.0$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	$V_{IN}=V_{CC}$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	$V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

$V_{CC}=5V$; $T_A=25°C$, $C_L=50$ pF; $t_r=t_f=20$ ns; unless otherwise specified.

	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC ADC3711CC		f_{IN}/64,512 f_{IN}/129,024		conversions/sec conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to 2^0, 2^1, 2^2, 2^3	DLE=0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to 2^0, 2^1, 2^2, 2^3			2.0	5.0	μs
$t_{SET\text{-}UP}$	Set-Up Time D0, D1, to DLE	$t_{HOLD}=0$ ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

Converter Characteristics ADC3511CC, ADC3711CC $4.75 \le V_{CC} \le 5.25V$; $-40°C \le T_A \le +85°C$, $f_c = 5$ conv./sec (ADC3511CC); 2.5 conv./sec (ADC3711CC); unless otherwise specified.

	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
	Non-Linearity	$V_{IN} = 0-2V$ Full Scale $V_{IN} = 0-200$ mV Full Scale	−0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		−1		+0	Counts
	Offset Error	$V_{IN} = 0V$	−0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		−0		+0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	$T_A = 25°C$	−5	±1	+5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

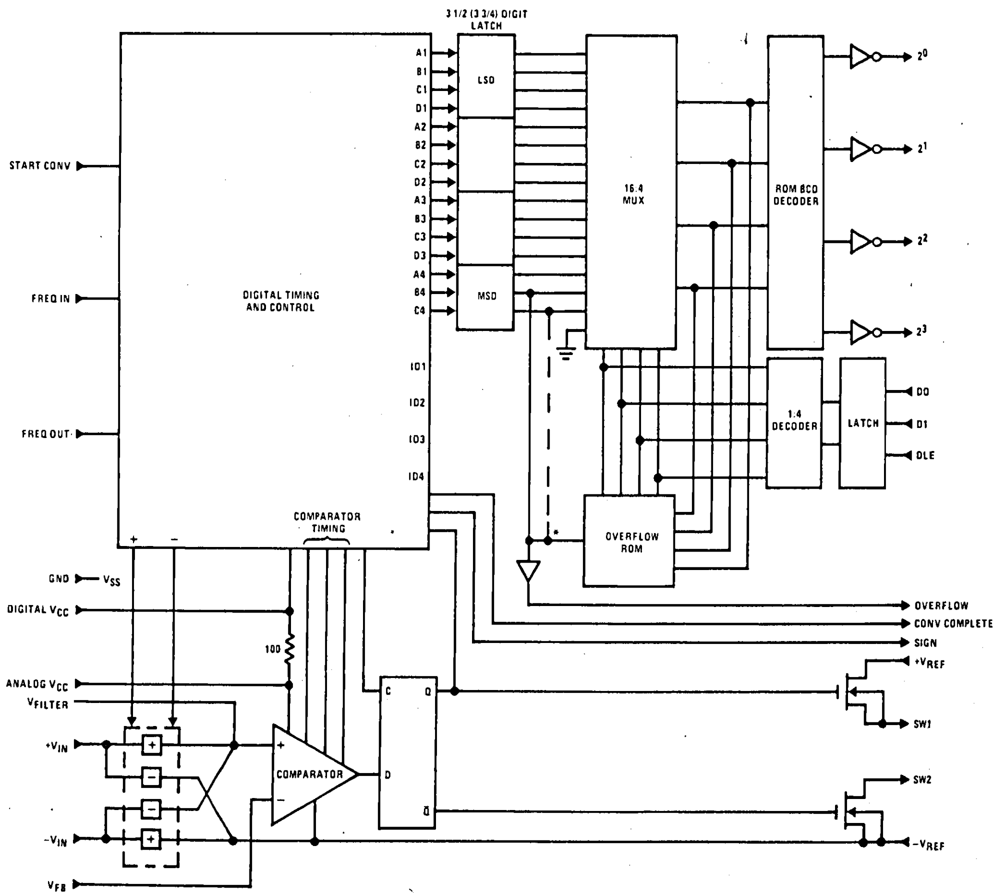
Note 2: All typicals are given for $T_A = 25°C$.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = ½ count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Block Diagram

ADC3511 3 ½-Digit A/D (*ADC3711 3 ¾-Digit A/D)



TL/H/5678-2

Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT}=V_{REF}$ and if Q is at a low level $V_{OUT}=0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\frac{t_{ON}}{t_{ON}+t_{OFF}} = V_{REF}\text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB}=V_{REF}\text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN}=V_{FB}=V_{REF}\text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

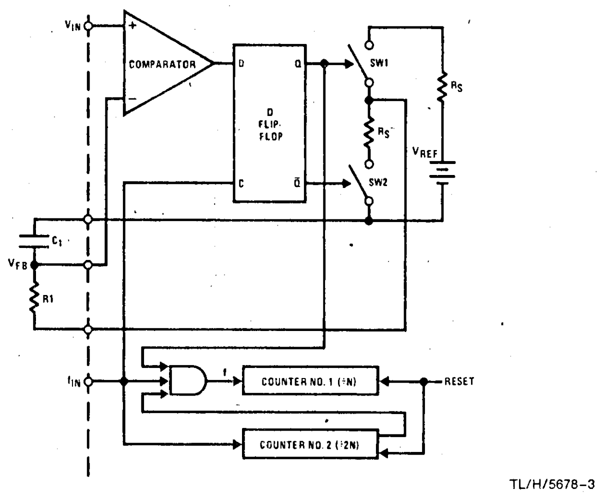
$$f=\text{(duty cycle)}\times(f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)}\times(f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}}\times N$$

For the ADC3511 N=2000.

For the ADC3711 N=4000.



$V_{IN}=V_{FB}=V_{REF}\times$(duty cycle)

$f=$(duty cycle)$\times f_{IN}$

$$\text{Count in counter no. 1} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)}\times f_{IN}}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}}\times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 × $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to $64 \times 1/f_{IN}$ on the ADC3511, or $128 \times 1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 × $1/f_{IN}$ (129,024 × $1/f_{IN}$ for the ADC3711) and the minimum time is 256 × $1/f_{IN}$ (512 × $1/f_{IN}$) for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

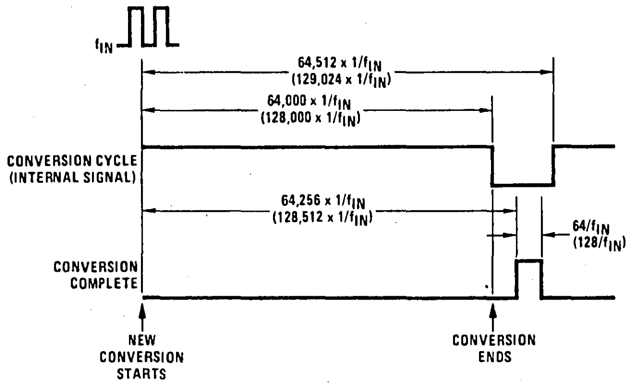


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

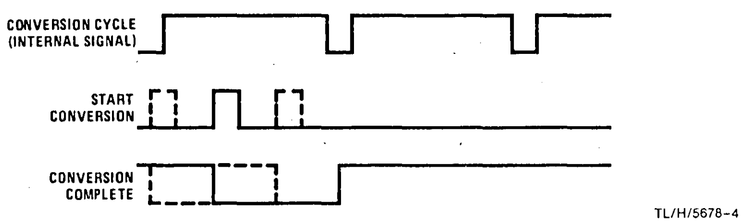


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = Low logic level
H = High logic level
X = Irrelevant logic level

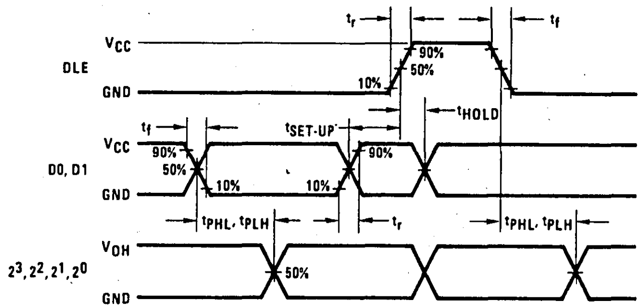
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



TL/H/5678-5

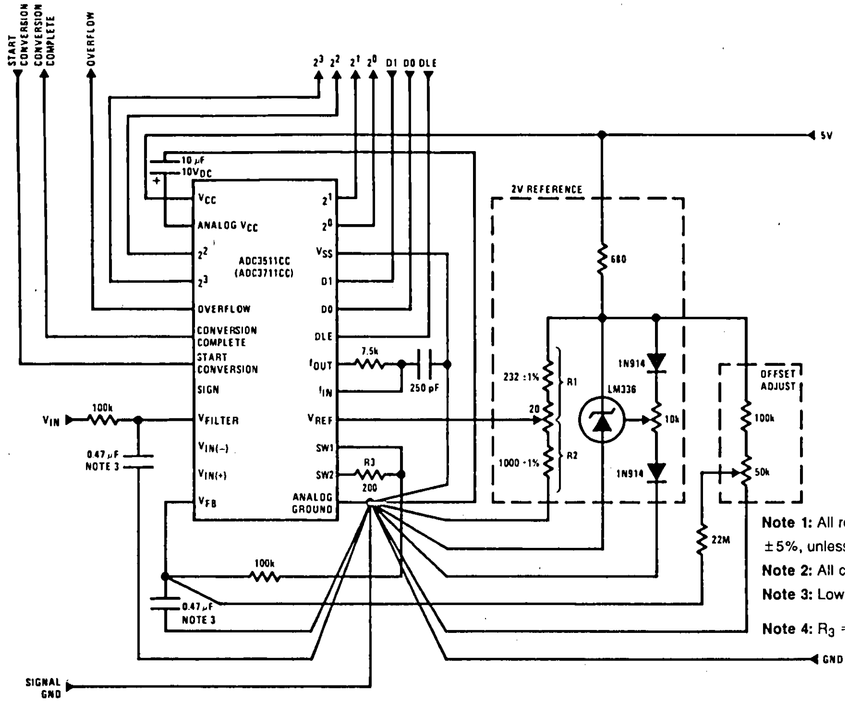
Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6*.

Figures 5 and *6* show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error ($1.0 \times 10^{-9}A \times 100\ k\Omega = 0.1\ mV$). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

Typical Applications (Continued)



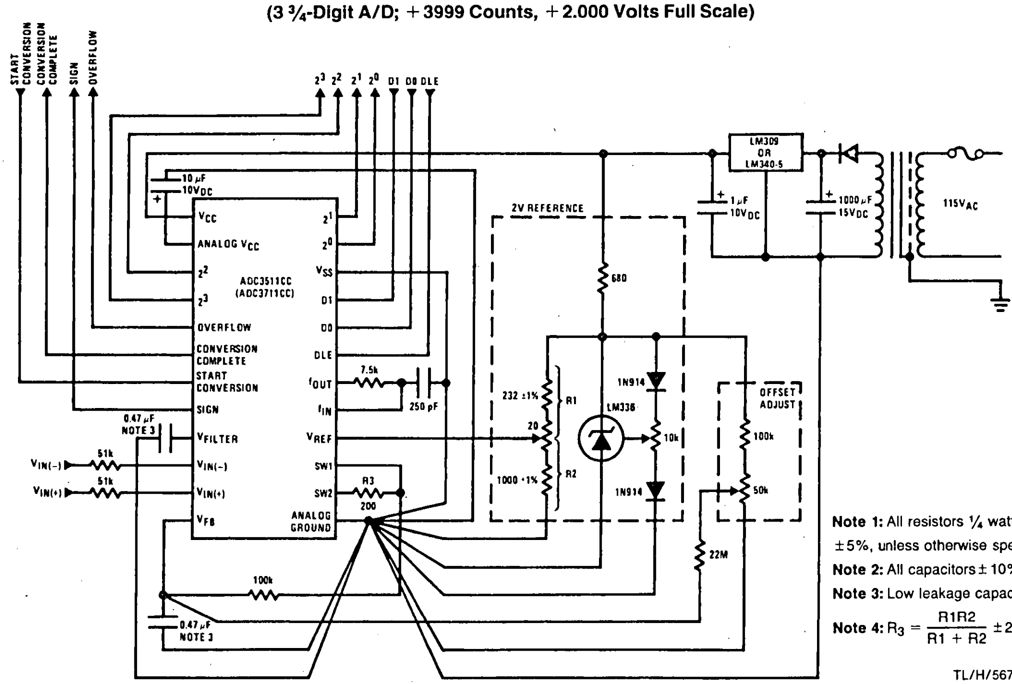
Note 1: All resistors ¼ watt, and ±5%, unless otherwise specified.

Note 2: All capacitors ± 10%.

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega$.

FIGURE 4. 3 ½-Digit A/D; + 1999 Counts, + 2.000 Volts Full Scale (3 ¾-Digit A/D; + 3999 Counts, + 2.000 Volts Full Scale)



Note 1: All resistors ¼ watt, and ±5%, unless otherwise specified.

Note 2: All capacitors ± 10%.

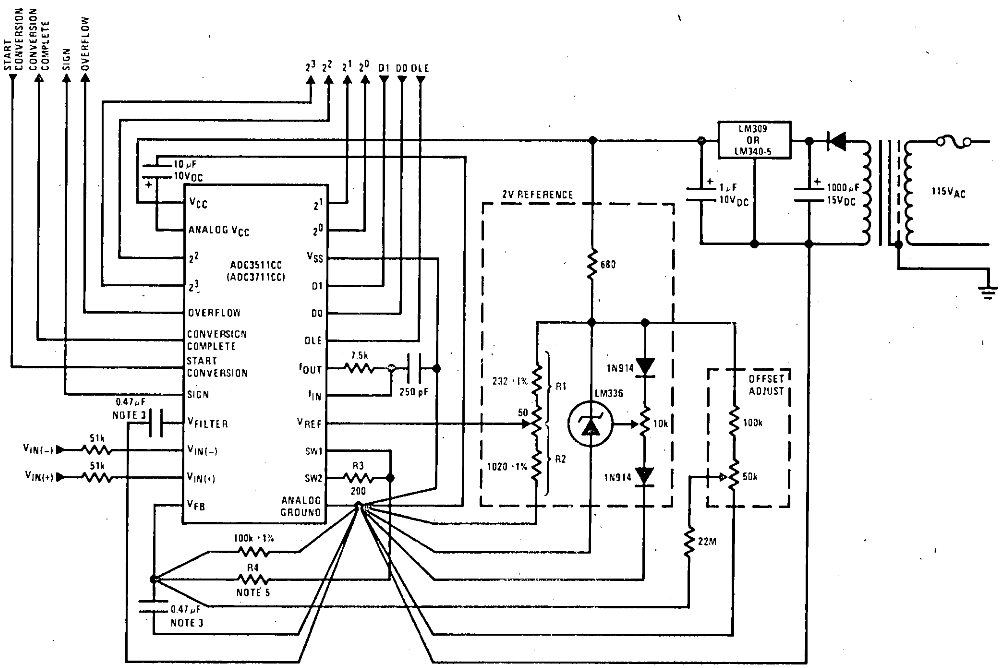
Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega$.

TL/H/5678-6

FIGURE 5. 3 ½-Digit A/D; ± 1999 Counts, ± 2.000 Volts Full Scale (3 ¾-Digit A/D; ± 3999 Counts, ± 2.000 Volts Full Scale)

Typical Applications (Continued)



TL/H/5678-7

Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.

Note 2: All capacitors ±10%

Note 3: Low leakage capacitor.

Note 4: $R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega$

Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.
R4 = 400k ±1% for the ADC3711CC, 400.0 mV Full-Scale.

FIGURE 6. 3 1/2-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale (3 3/4-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)

National Semiconductor

ADD3501 3½ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3501 (MM74C935-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

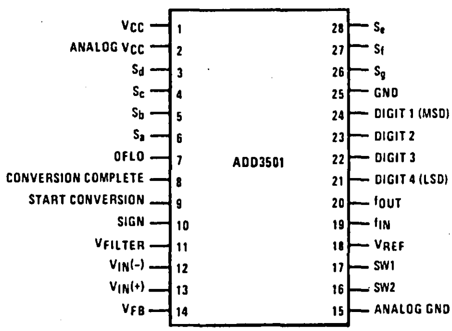
Features

- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed - 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange Indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram



TL/H/5681–1

Order Number ADD3501CCN
See NS Package N28B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A=25°C$	800mW
derate at $\theta_{JA(MAX)}=125°C/Watt$ above $T_A=25°C$	
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$

Electrical Characteristics ADD3501

$4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$, unless otherwise specified.

Parameter		Conditions	Min	Typ(2)	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs except Digit Outputs)	$I_O=1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O=0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O=50$ mA@$T_J=25°C$ $V_{CC}=5V$ $I_O=30$ mA@$T_J=100°C$	$V_{CC}-1.6$ $V_{CC}-1.6$	$V_{CC}-1.3$ $V_{CC}-1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs except Segment Outputs)	$I_O=500\mu A$ (Digit Outputs) $I_O=360\mu A$ (Conv. Complete, +/−, Oflo Outputs)	$V_{CC}-0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT}=1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN}=1.5V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN}=0V$	-1.0			μA
I_{CC}	Supply Current Oscillator Frequency	Segments and Digits Open		0.5 0.6/RC	10	mA kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/64,512$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/256$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for $T_A = 25°C$.

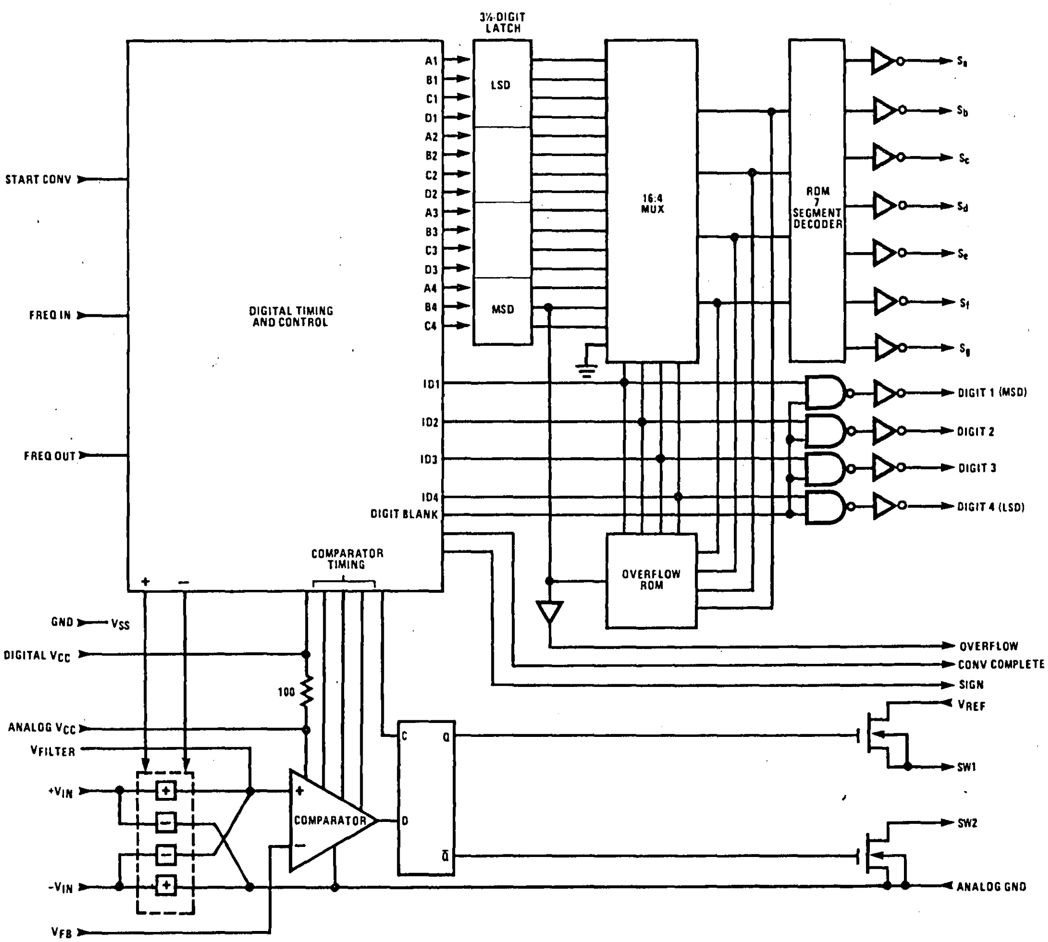
Electrical Characteristics ADD3501

$t_C = 5$ conversions/second, $0°C \leq T_A \leq 70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Non-Linearity	$V_{IN} = 0-2V$ Full Scale $V_{IN} = 0-200mV$ Full Scale	−0.05	±0.025	+0.05	% of full scale
Quantization Error		−1		+0	counts
Offset Error, $V_{IN} = 0V$		−0.5	+1.5	+3	mV
Rollover Error		−0		+0	counts
Analog Input Current	$T_A = 25°C$	−5	±0.5	+5	nA
($V_{IN}+$, $V_{IN}-$)					

Block Diagram

ADD3501 3½-Digit DVM Block Diagram



TL/H/5681-2

Theory of Operation

A schematic for the analog loop is shown in *Figure 1*. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\left(\frac{T_{ON}}{T_{ON}+T_{OFF}}\right) = V_{REF}(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

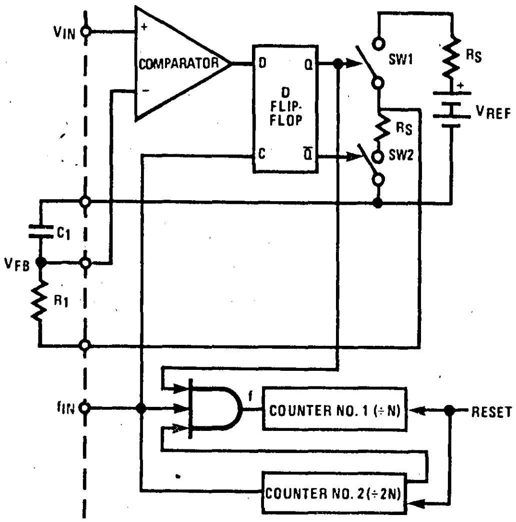
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3501, $N = 2000$.

Schematic Diagram



TL/H/5681-3

$$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$$

$$f = (\text{duty cycle}) \times f_{IN}$$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{In}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in *Figure 2*, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to $64,512 \times 1/f_{IN}$.

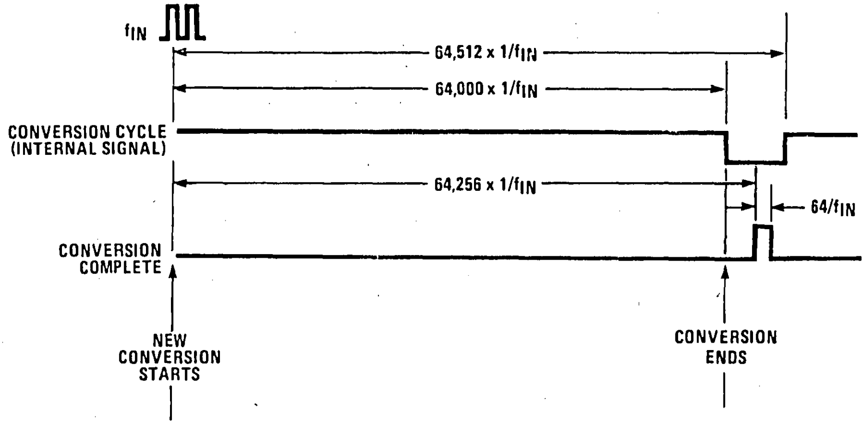
The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to $64 \times 1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3501 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3*, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is $64,512 \times 1/f_{IN}$ and the minimum time is $256 \times 1/f_{IN}$.

Timing Waveforms



TL/H/5681-4

Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

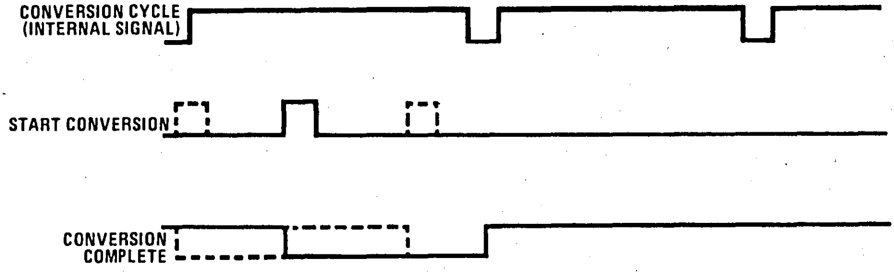


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3501 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3501 to minimize these problems but poor printed circuit layout can negate these features.

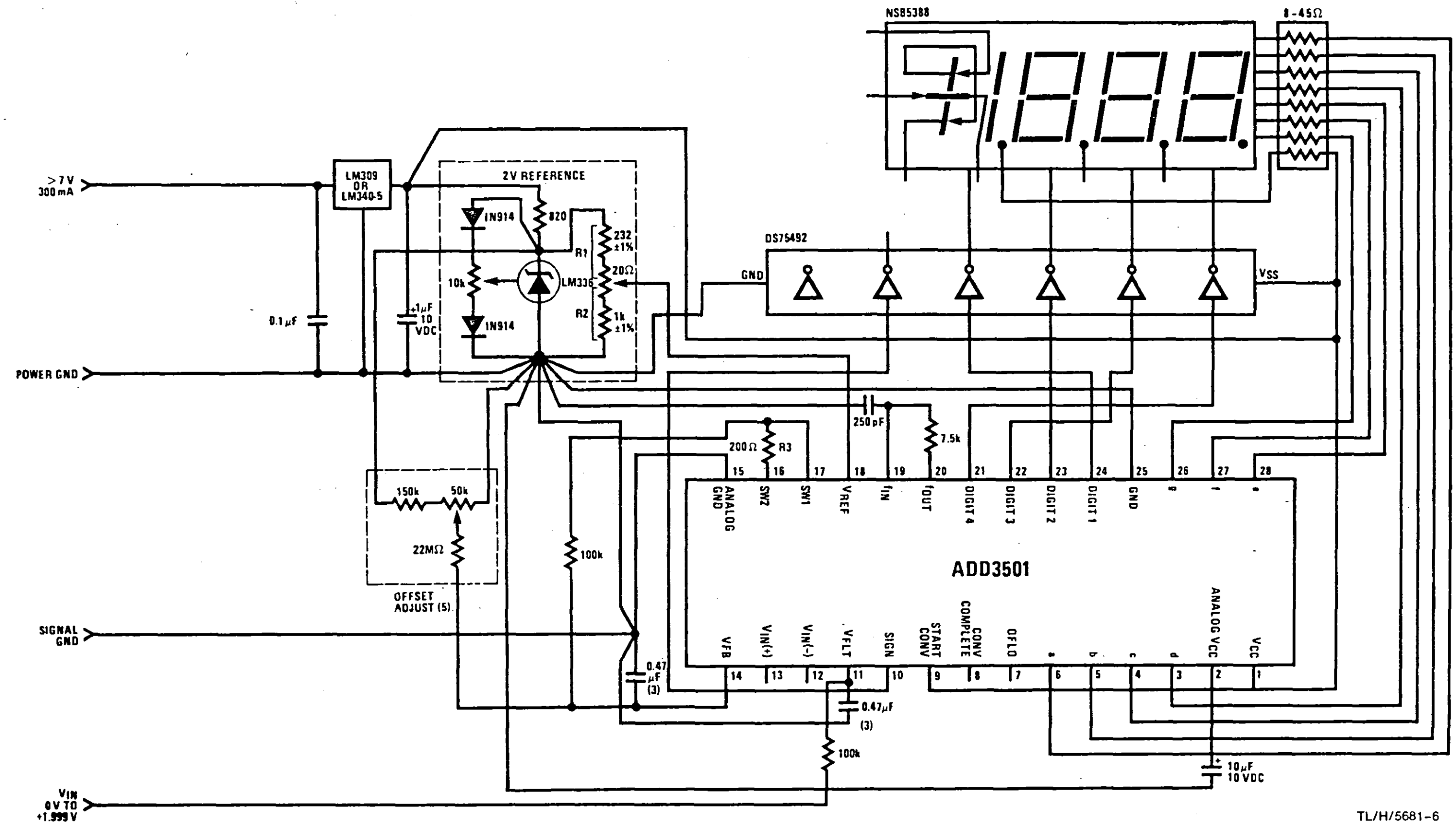
Figures 4, 5, and *6* show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators both function well and are shown in *Figures 4, 5,* and *6.* Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0V to 1.999V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or − (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in *Figure 6.*

Figures 5 and *6* show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

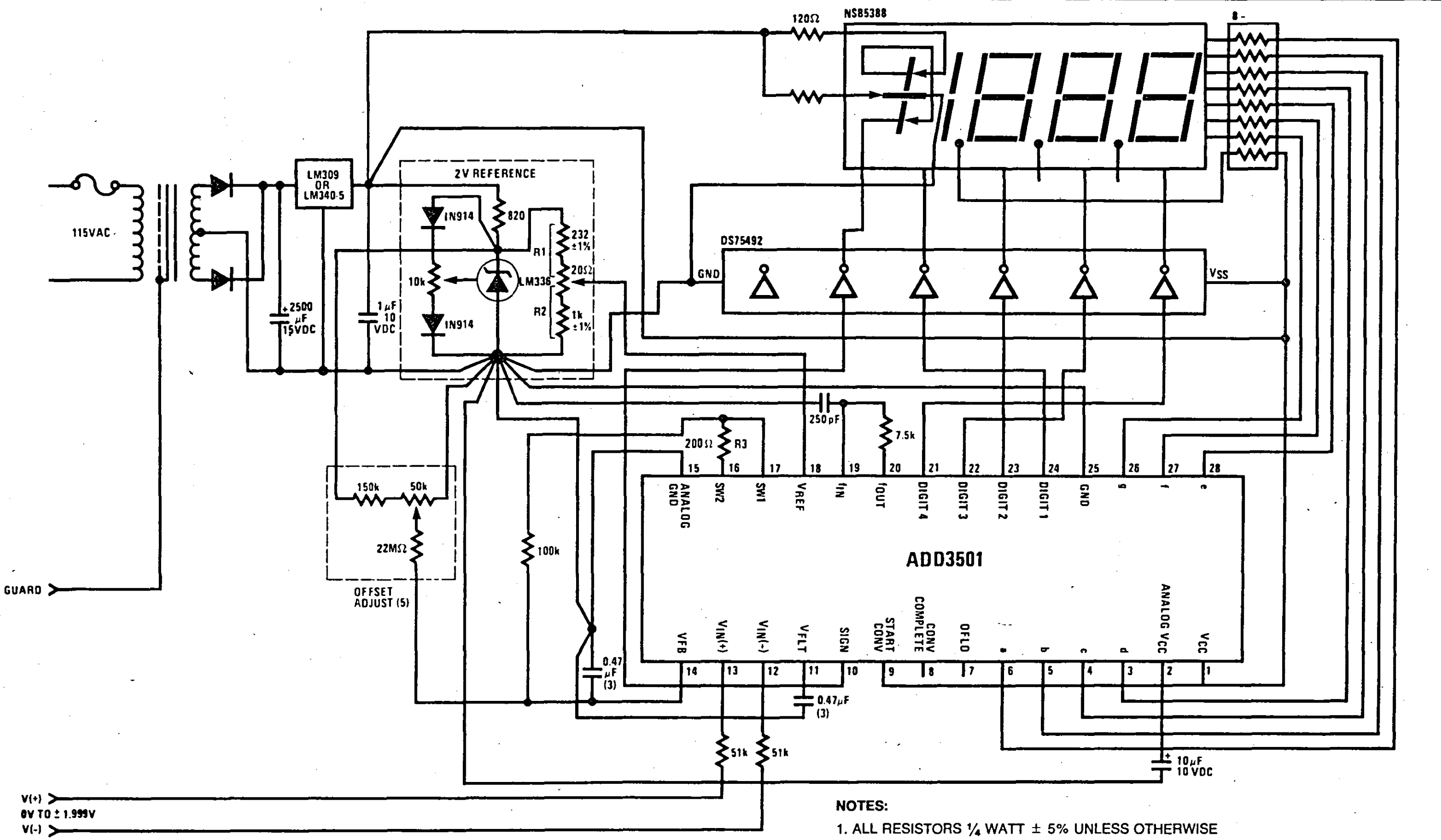
The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0nA of leakage current will cause 0.1mV error ($1.0 \times 10^{-9}A \times 100k\Omega = 0.1mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$

Figure 4. 3½-Digit DPM, + 1.999 Volts Full Scale

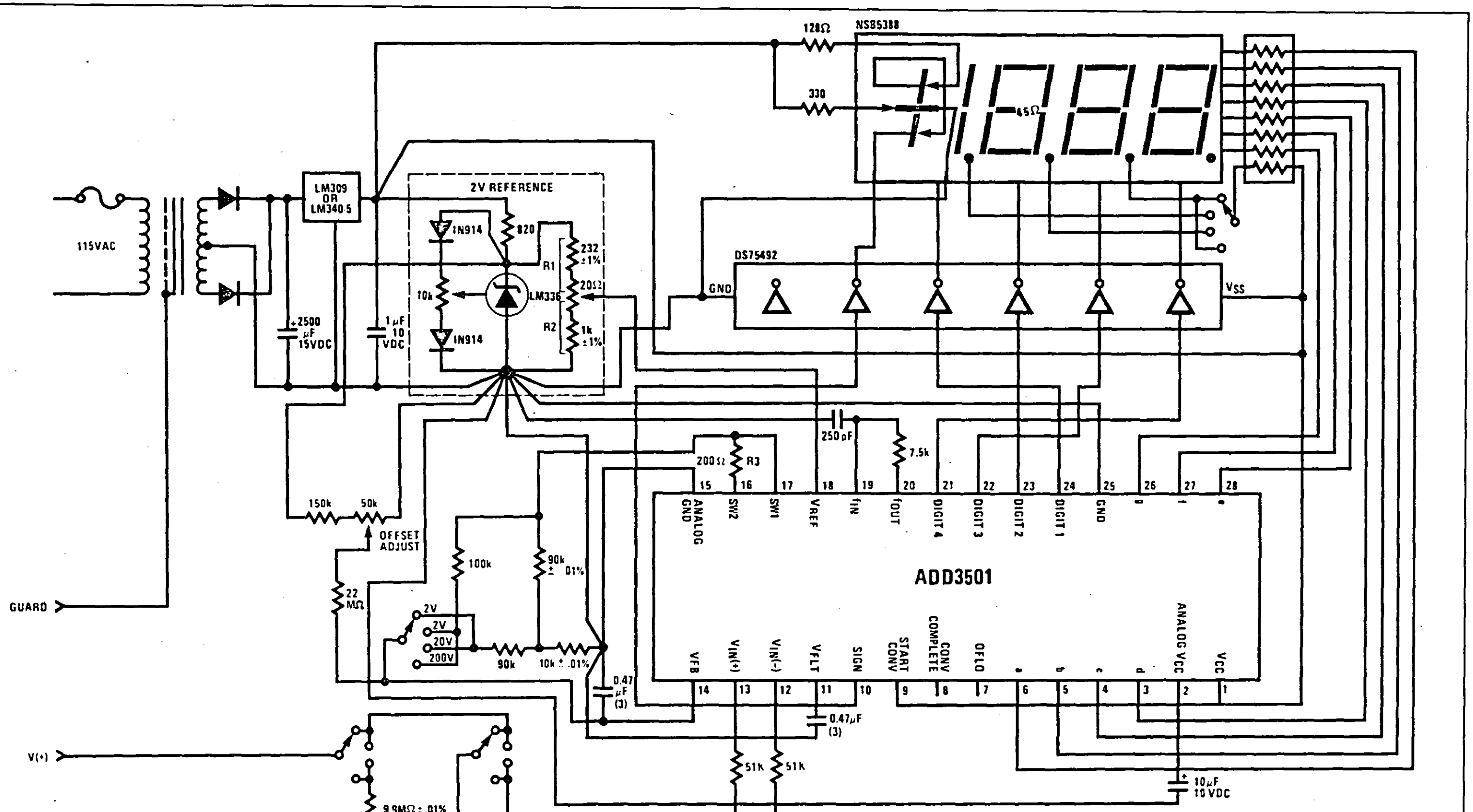


NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

TL/H/5681–7

Figure 5. 3½-Digit DPM, ± 1.999 Volts Full Scale



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

TL/H/5681-8

Figure 6. 3½-Digit DVM, Four Decade, ±0.2V, ±2V, ±20V and ±200V Full Scale

National Semiconductor

ADD3701 $3\frac{3}{4}$ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

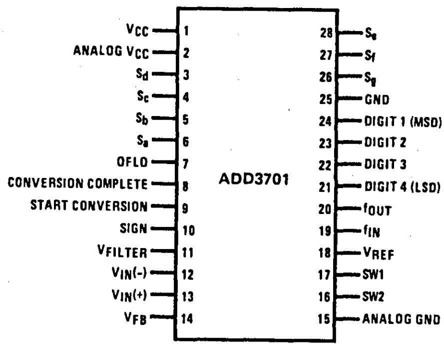
Features

- Operates from single 5V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram



TL/H/5682-1

Order Number ADD3701CCN
See NS Package N28B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin except Start Conversion	$-0.3V$ to $V_{CC}+0.3V$
Voltage at Start Conversion	$-0.3V$ to $+15.0V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A=25°C$	800mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$

Electrical Characteristics ADD3701

$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$, unless otherwise specified.

Parameter		Conditions	Min	Typ[2]	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs Except Digital Outputs)	$I_O=1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O=0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O=50$ mA @ $T_J=25°C$ $V_{CC}=5V$ $I_O=30$ mA @ $T_J=100°C$	$V_{CC}-1.6$ $V_{CC}-1.6$	$V_{CC}-1.3$ $V_{CC}-1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	$I_O=500$ µA (Digit Outputs) $I_O=360$ µA (Conv. Complete, +/−, OFLO Outputs)	$V_{CC}-0.4$			V
I_{SOURCE}	Output Source Current (Digital Outputs)	$V_{OUT}=1.0$ V	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN}=15V$			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN}=0V$	−1.0			µA
I_{CC}	Supply Current Oscillator Frequency	Segments and Digits Open		0.5 0.6/RC	10	mA kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/129{,}024$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/512$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		seconds
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for $T_A=25°C$.

Note 3: Full scale = 4000 counts; therefore 0.025% of full scale = 1 count and 0.05% of full scale = 2 counts.

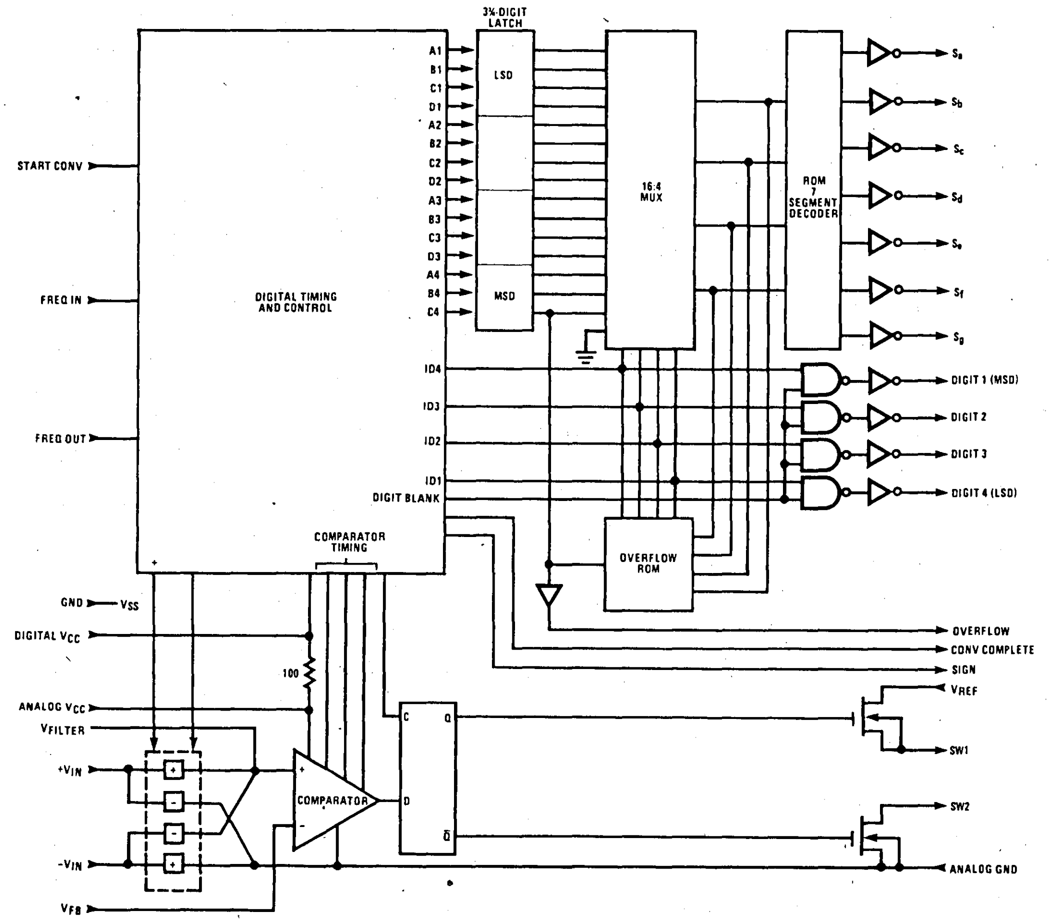
Note 4: For 2.000 Volts full scale, 1 mV = 2 counts.

Electrical Characteristics ADD3701

$t_C = 2.5$ conversions/second, $0°C \leq T_A \leq +70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ[2]	Max	Units
Non-Linearity of Output	$V_{IN} = 0 - 2V$ Full Scale	−0.05	±0.025	±0.05	% full scale
Reading	$V_{IN} = 0 - 200$ mV Full Scale				(Note 3)
Quantization Error		−1		+0	counts
Offset Error, $V_{IN} = 0V$		−0.5	+1.5	+3	mV (Note 4)
Rollover Error		−0		+0	counts
Analog Input Current ($V_{IN}+$, $V_{IN}-$)	$T_A = 25°C$	−5	±1	+5	nA

Block Diagram



TL/H/5682-2

ADD3701 3¾-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times \text{(clock)}$$

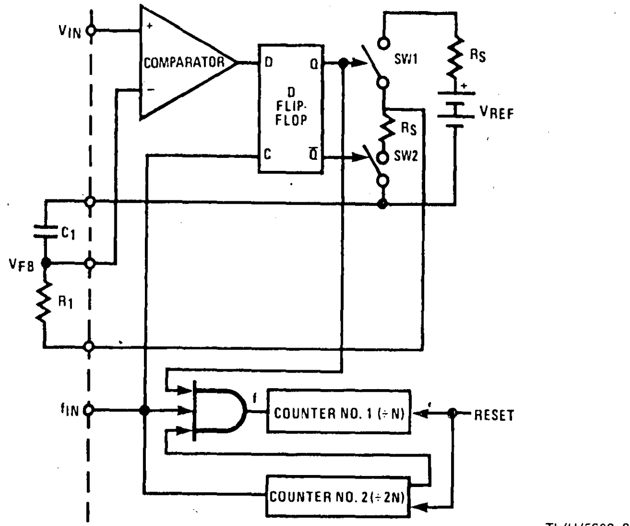
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{\text{(clock)}/N} = \frac{\text{(duty cycle)} \times \text{(clock)}}{\text{(clock)}/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3701 N = 4000.

Schematic Diagram



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in *Figure 2*, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 129,024 × $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 128 × $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3701 is always continuously converting the analog voltage present at its input. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3*, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 129,024 × $1/f_{IN}$ and the minimum time is 512 × $1/f_{IN}$.

Timing Waveforms

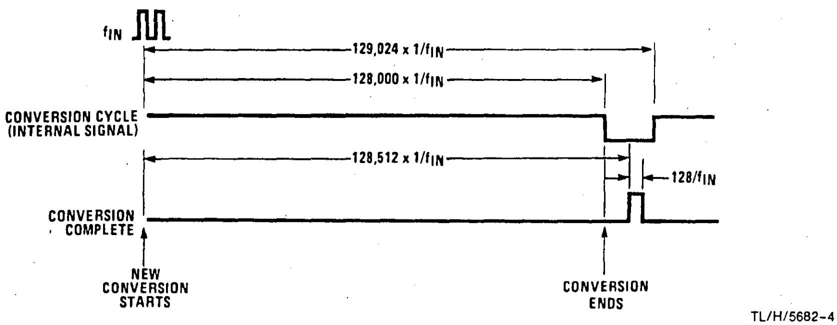


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation

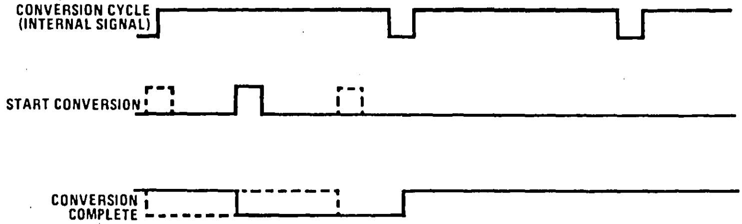


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3701 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3701 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and *6* show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

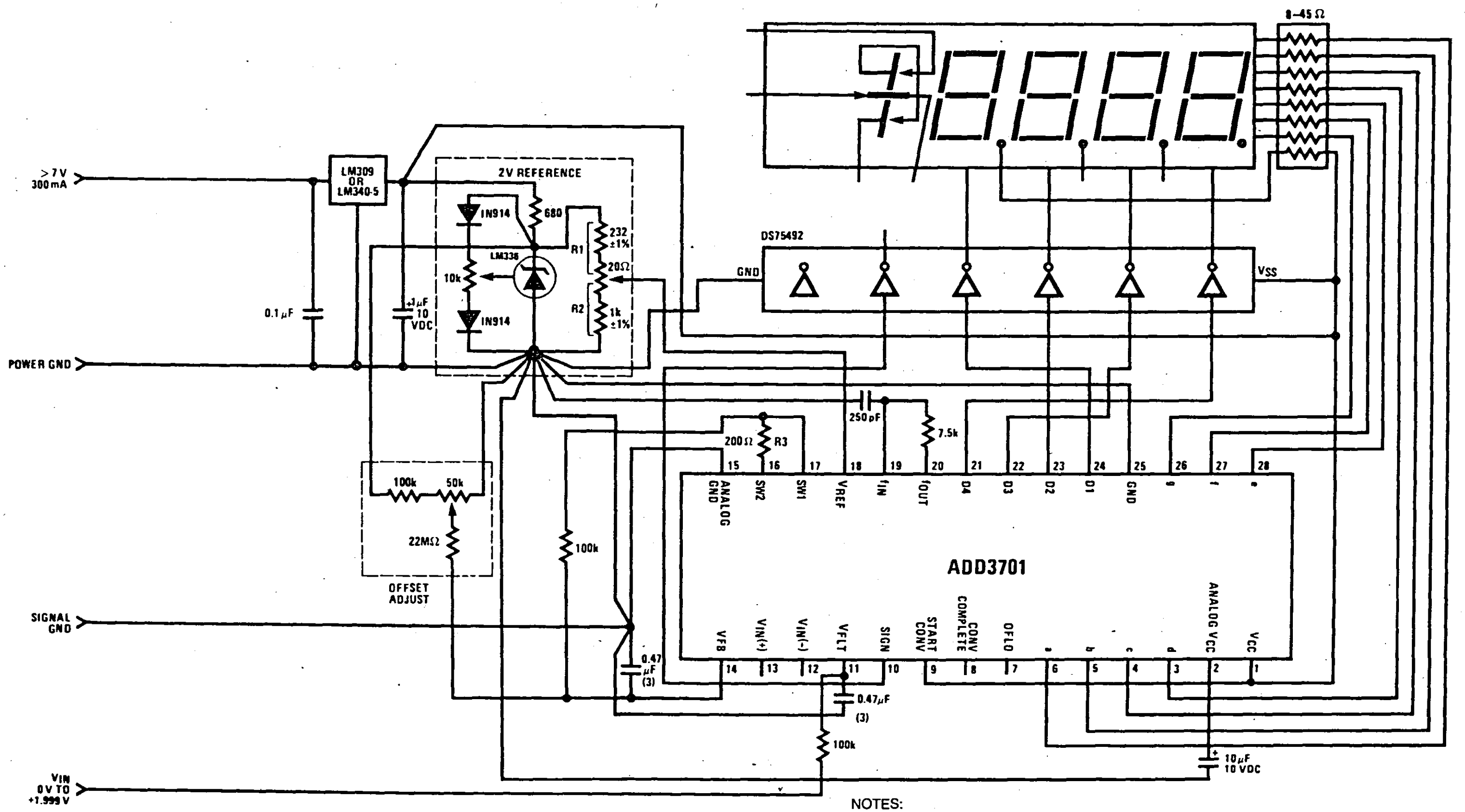
To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators all function well and are shown in *Figures 4, 5,* and *6*. Adding more filtering than is shown will in general increase the jitter rather than decrease it.

The most important characteristics of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0 to +3.999 counts operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or − (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in *Figure 5*.

Figures 5 and *6* show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error (1.0×10^{-9}A $\times$ 100 kΩ = 0.1 mV). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ±10%
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R3 \pm 25\Omega$

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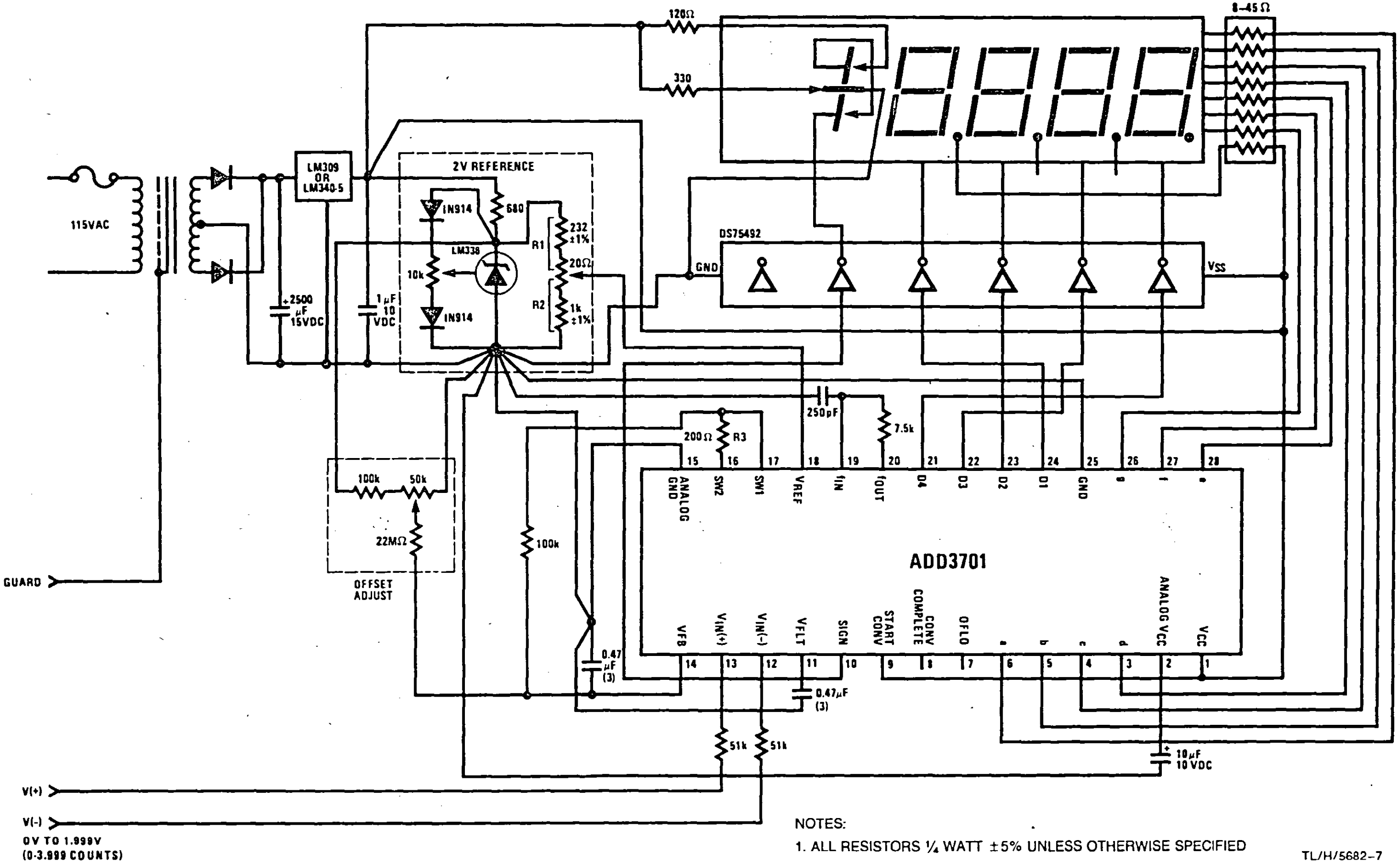
Figure 4. 3¾-Digital DPM, +3.999 Count Full Scale



NOTES:

1. ALL RESISTORS ¼ WATT ±5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$.

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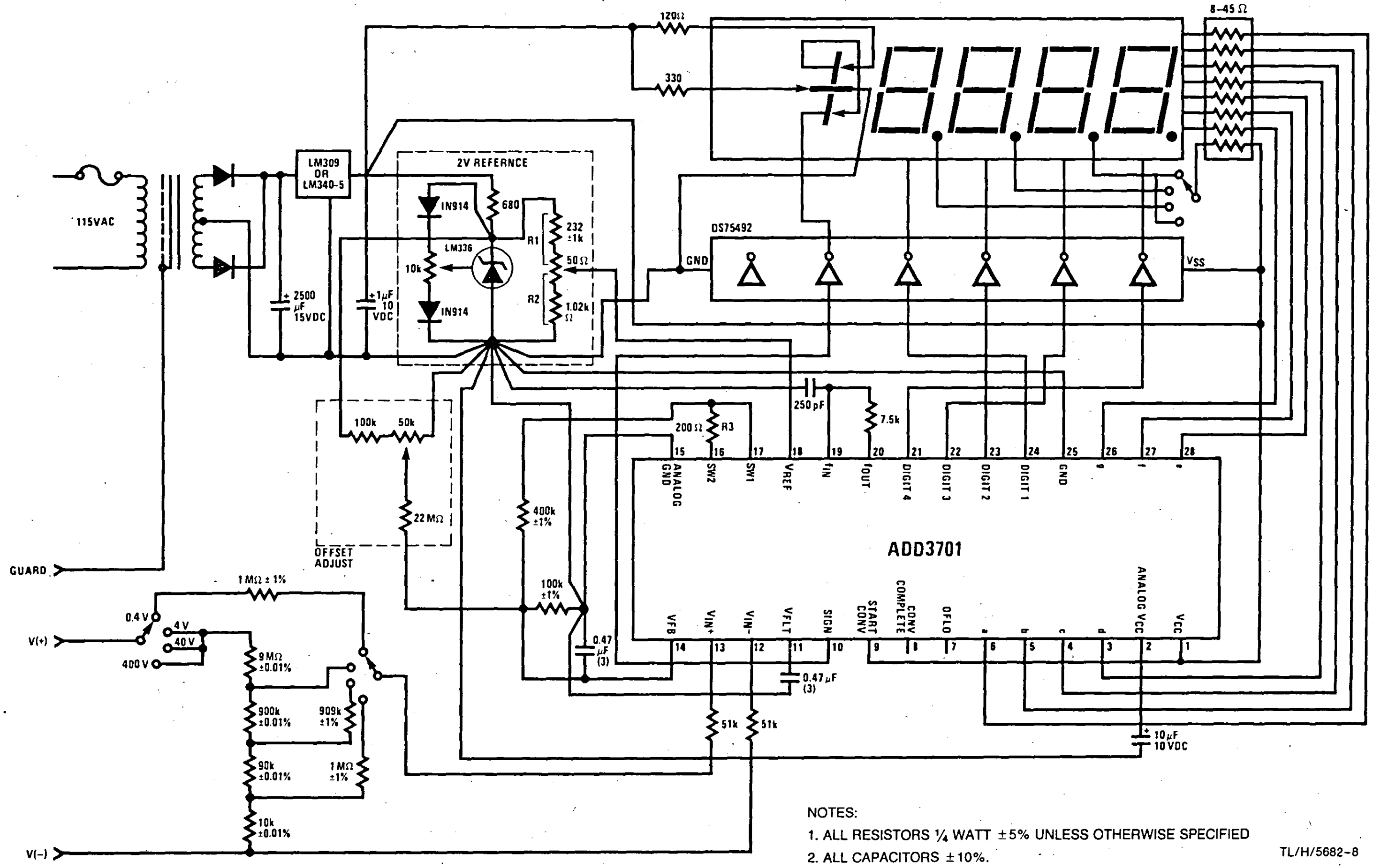
Figure 5. 3¾-Digit DPM, ±3.999 Counts Full Scale



NOTES:

1. ALL RESISTORS ¼ WATT ±5% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$.

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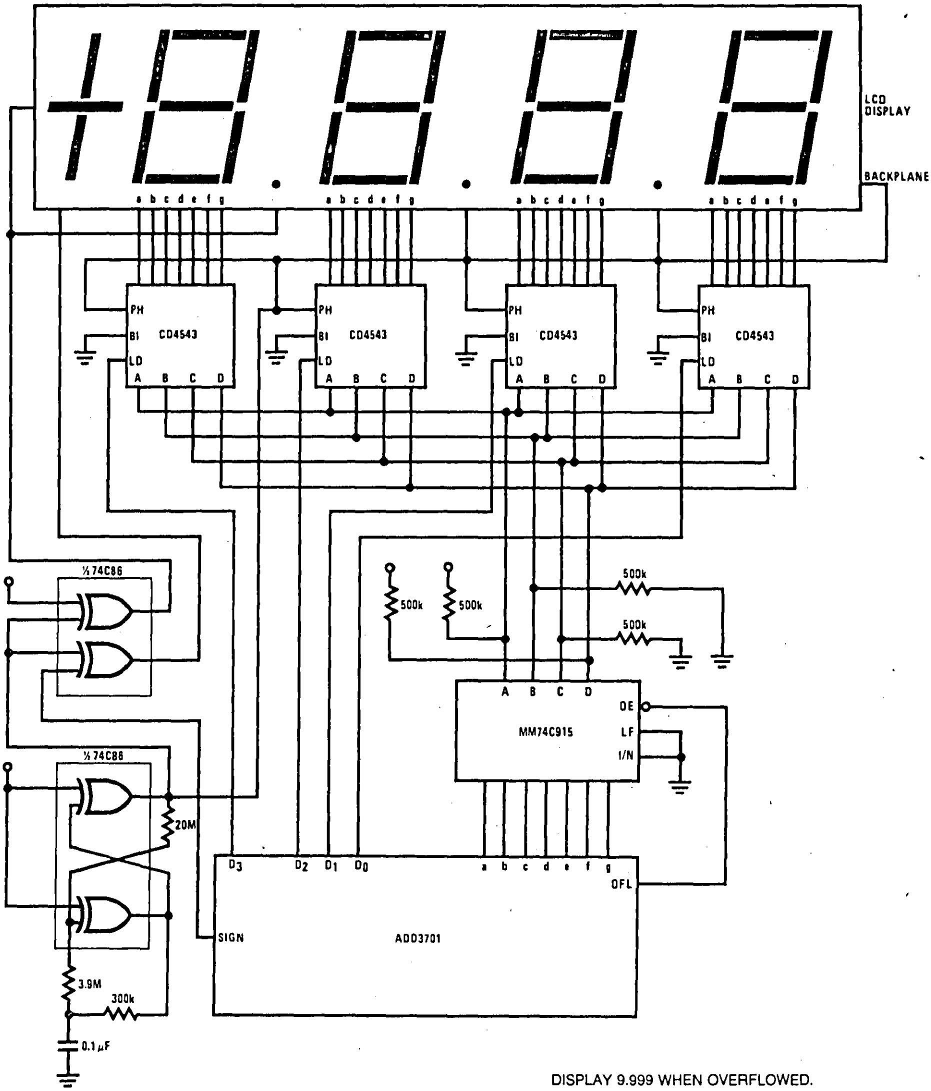
Figure 6. 3¾-Digit DVM, Four Decade, ±0.4V, ±4V, ±40V, and ±400V Full Scale



DISPLAY 9.999 WHEN OVERFLOWED.
ALL DIGITS CAN ALSO BE BLANKED AT OVERFLOW BY TYING OFL TO B1 ON THE CD4543s.

TL/H/5682-9

Figure 7. ADD3701 Driving Liquid Crystal Display

National Semiconductor

DAC0830/DAC0831/DAC0832
8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

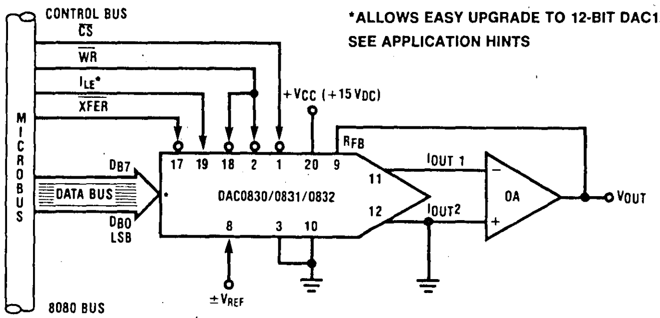
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired

Key Specifications

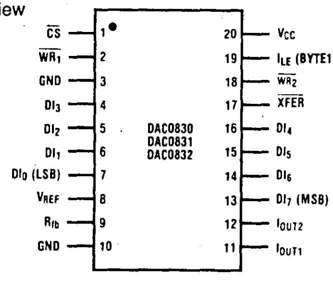
■ Current settling time	1 μs
■ Resolution	8-bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application



*ALLOWS EASY UPGRADE TO 12-BIT DAC1230, SEE APPLICATION HINTS

Connection Diagram Top View



†THIS IS NECESSARY FOR THE 12-BIT DAC1230 SERIES TO PERMIT INTERCHANGING FROM AN 8-BIT TO A 12-BIT DAC WITH **NO PC BOARD CHANGES AND NO SOFTWARE CHANGES**, SEE APPLICATIONS SECTION.

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Order Numbers DAC0830, DAC0831, DAC0832
See NS Packages D20A and N20A

Absolute Maximum Ratings

(Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65°C to +150°C
Package dissipation at T_A = 25°C (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead temperature (soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCD' suffix	−40°C to +85°C
Part numbers with 'LD' suffix	−55°C to +125°C
Voltage at any digital input	V_{CC} TO GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC} unless otherwise noted. Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$. For all other limits T_A = 25°C.

Parameter	Conditions	See Note	V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%			V_{CC} = 5 V_{DC} ±5%			Limit Units
			Typ.	Tested Limit (Note 5)	Design Limit (Note 6)	Typ.	Tested Limit (Note 5)	Design Limit (Note 6)	
Converter Characteristics									
Resolution			8	8		8	8		bits
Linearity Error Max.	Zero and full scale adjusted	4, 7							
	$-10V \le V_{REF} \le +10V$	8							
	DAC0830LD & LCD			**0.05**			**0.05**		% FSR
	DAC0832LD & LCD			**0.2**			**0.2**		% FSR
	DAC0830LCN			0.05	**0.05**		0.05	**0.05**	% FSR
	DAC0831LCN			0.1	**0.1**		0.1	**0.1**	% FSR
	DAC0832LCN			0.2	**0.2**		0.2	**0.2**	% FSR
Differential Nonlinearity Max.	Zero and full scale adjusted	4, 7							
	$-10V \le V_{REF} \le +10V$	8							
	DAC0830LD & LCD			**0.1**			**0.1**		% FSR
	DAC0832LD & LCD			**0.4**			**0.4**		% FSR
	DAC0830LCN			0.1	**0.1**		0.1	**0.1**	% FSR
	DAC0831LCN			0.2	**0.2**		0.2	**0.2**	% FSR
	DAC0832LCN			0.4	**0.4**		0.4	**0.4**	% FSR
Monotonicity	$-10V \le V_{REF}$ LD & LCD	4, 7		**8**			**8**		bits
	$\le +10V$ LCN			8	**8**		8	**8**	bits
Gain Error Max.	Using Internal R_{fb} $-10V \le V_{REF} \le +10V$	7	±0.2	±1		±0.2	±1		% FS
Gain Error Tempco Max.	Using internal R_{fb}		**0.0002**		**0.0006**	**0.0002**		**0.0006**	% FS/°C
Power Supply Rejection	All digital inputs latched high								% FSR/V
	V_{CC} = 14.5V to 15.5V		0.0002						
	11.5V to 12.5V		0.0006						
	4.5V to 5.5V					0.0130			
Reference Input Max.			15	20		15	20		kΩ
Reference Input Min.			15	10		15	10		kΩ
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All data inputs latched low	9	3			3			mVp-p
Output Leakage Current Max. I_{OUT1}	All data inputs latched low LD & LCD	10		**100**			**100**		nA
	LCN			50	**100**		50	**100**	nA
Output Leakage Current Max. I_{OUT2}	All data inputs latched high LD & LCD			**100**			**100**		nA
	LCN			50	**100**		50	**100**	nA
Output Capacitance I_{OUT1}	All data inputs latched low		45			45			pF
Output Capacitance I_{OUT2}			115			115			pF
Output Capacitance I_{OUT1}	All data inputs latched high		130			130			pF
Output Capacitance I_{OUT2}			30			30			pF

Electrical Characteristics (Continued) $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted. Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$. For all other limits $T_A = 25°C$.

Parameter		Conditions	See Note	$V_{CC} = 12\ V_{DC} \pm 5\%$ to $15\ V_{DC} \pm 5\%$			$V_{CC} = 5\ V_{DC} \pm 5\%$			Limit Units
				Typ.	Tested Limit (Note 5)	Design Limit (Note 6)	Typ.	Tested Limit (Note 5)	Design Limit (Note 6)	
Digital and DC Characteristics										
Digital Input Voltages	Max.	Logic Low LD LCD LCN			**0.8** **0.8** 1.0	 **0.8**		**0.6** **0.8** 1.0	 **0.8**	V_{DC}
	Min.	Logic High LD & LCD LCN			**2.0** 1.9	 **2.0**		**2.0** 1.9	 **2.0**	V_{DC}
Digital input Currents	Max.	Digital inputs <0.8V LD & LCD LCN		−50	**−200** 160	 **−200**	−50	**−200** −160	 **−200**	μA_{DC}
		Digital inputs>2.0V LD & LCD LCN		0.1	**+10** +8	 **+10**	0.1	**+10** +8	 **+10**	μA_{DC}
Supply Current Drain	Max.	LD & LCD LCN		1.2	**2.0** 1.7	 **2.0**	1.2	**2.0** 1.7	 **2.0**	mA
AC Characteristics										
t_S	Current Setting Time	$V_{IL} = 0V$, $V_{IH} = 5V$		1.0			1.0			μs
t_W	Write and XFER Pulse Width Min.	$V_{IL} = 0V$, $V_{IH} = 5V$	11	100 **180**		320 **320**	375 **500**		600 **900**	ns
t_{DS}	Data Setup Time Min.	$V_{IL} = 0V$, $V_{IH} = 5V$		100 **180**		320 **320**	375 **500**		600 **900**	ns
t_{DH}	Data Hold Time Min.	$V_{IL} = 0V$, $V_{IH} = 5V$		**10**		**50**	**10**		**50**	ns
t_{CS}	Control Setup Time Min.	$V_{IL} = 0V$, $V_{IH} = 5V$		110 **200**		320 **320**	400 **500**		650 **900**	ns
t_{CH}	Control Hold Time Min.	$V_{IL} = 0V$, $V_{IH} = 5V$				**10**			**10**	ns

Note 1: "*Absolute Maximum Ratings*" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "*Absolute Maximum*" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Max. T_J for the D suffix package is 150°C with $\theta_{JA} = 80°C/W$. Max. T_J for the N suffix package is 125°C with $\theta_{JA} = 120°C/W$.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

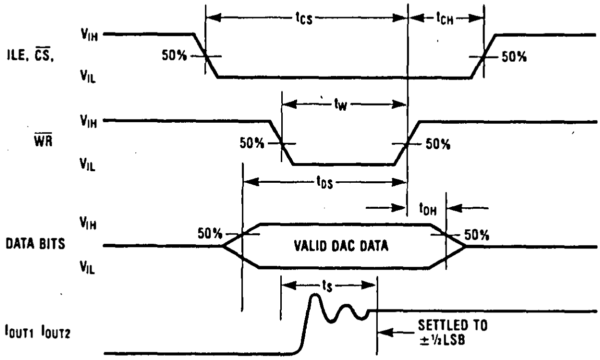
Note 8: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)". This guarantees that after performing a zero and full scale adjustment (see Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating, the feedthrough is typically 6mV.

Note 10: A 100nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(100 \times 10^{-9} \times 20 \times 10^3) \times 100/10$ which is 0.02% of FS.

Note 11: The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Switching Waveform



TL/H/5608-2

Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{CS}$: **Chip Select** (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: **Input Latch Enable** (active high). The ILE in combination with $\overline{CS}$ enables $\overline{WR_1}$.

$\overline{WR_1}$: **Write 1.** The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch—$\overline{CS}$ and $\overline{WR_1}$ must be low while ILE is high.

$\overline{WR_2}$: **Write 2** (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: **Transfer control signal** (active low). The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0-DI_7: **Digital Inputs.** DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: **DAC Current Output 1.** I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: **DAC Current Output 2.** I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1}+I_{OUT2}$ = constant (I full scale for a fixed reference voltage).

R_{fb}: **Feedback Resistor.** The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: **Reference Voltage Input.** This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: **Digital Supply Voltage.** This is the power supply pin for the part. V_{CC} can be from +5 to +15V_{DC}. Operation is optimum for +15V_{DC}.

GND: The pin 10 voltage must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications. Any difference of potential (V_{OS} pin 10) will result in a linearity change of

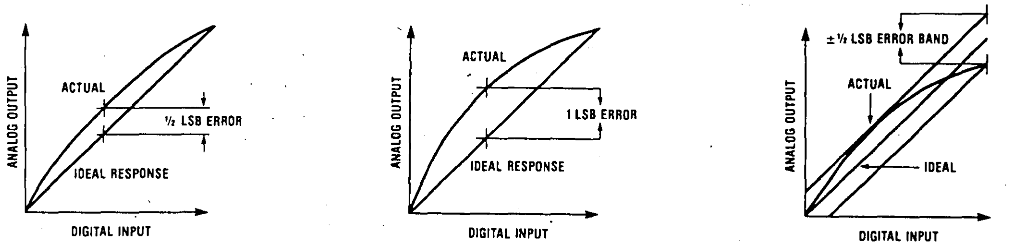
$$\frac{V_{OS}\text{ pin 10}}{3V_{REF}}$$

For example, if V_{REF} = 10V and pin 10 is 9mV offset from I_{OUT1} and I_{OUT2} the linearity change will be 0.03%.

Pin 3 can be offset ±100mV with no linearity change, but the logic input threshold will shift.

6

Linearity Error



TL/H/5608-3

a) End point test after zero and fs adj.

b) Best straight line

c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within $\pm\frac{1}{2}$LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is $V_{REF} - 1$LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 39mV = 9.961V$. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

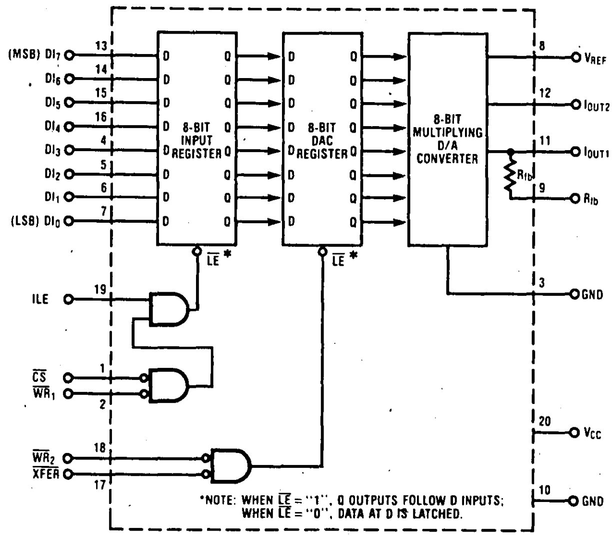


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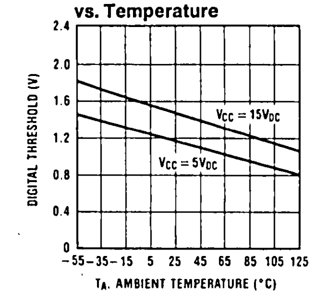
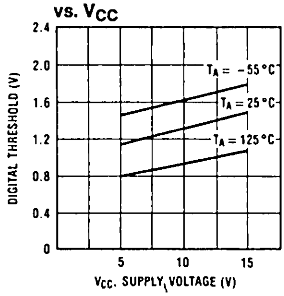
FIGURE 1. DAC0830 Functional Diagram

Typical Performance Characteristics

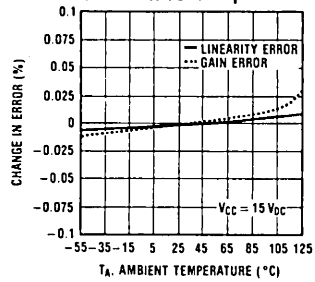
Digital Input Threshold vs. Temperature



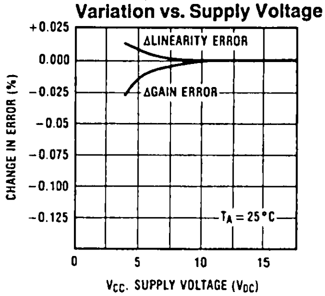
Digital Input Threshold vs. V_{CC}



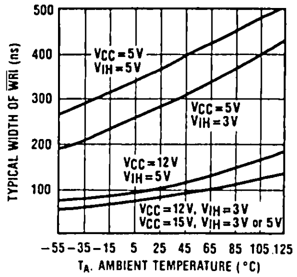
Gain and Linearity Error Variation vs. Temperature



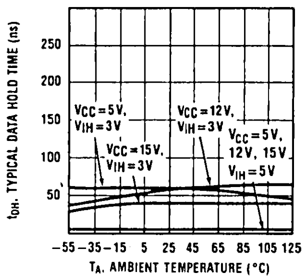
Gain and Linearity Error Variation vs. Supply Voltage



Write Pulse Width



Data Hold Time



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DAC0830 Series Application Hints

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte μP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0 = "1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in section 1.1).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 DIGITAL CONSIDERATIONS

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

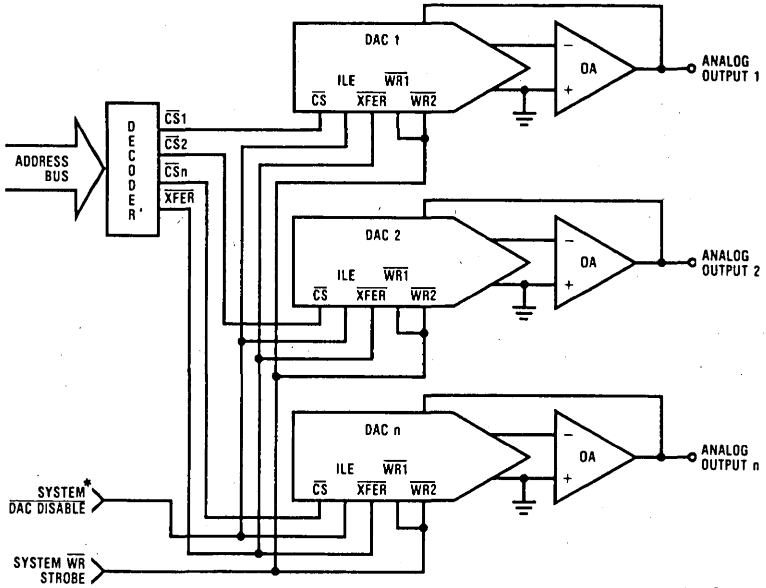
The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write-only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{CS}$ pin and a second for the DAC latch which is controlled by the $\overline{XFER}$ line. If more than one DAC is being driven, *Figure 2*, the $\overline{CS}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{XFER}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, *Figure 3*.

It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{XFER}$ command.

DAC0830 Series Application Hints (Continued)



*TIE TO LOGIC 1 IF NOT NEEDED (SEE SEC. 1.1).

FIGURE 2. Controlling Mutiple DACs

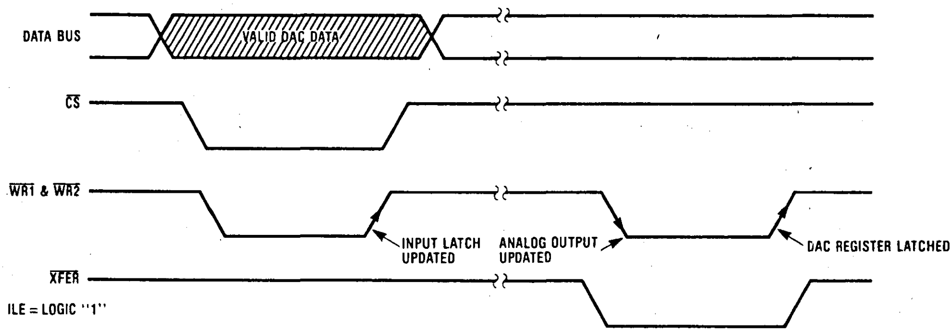


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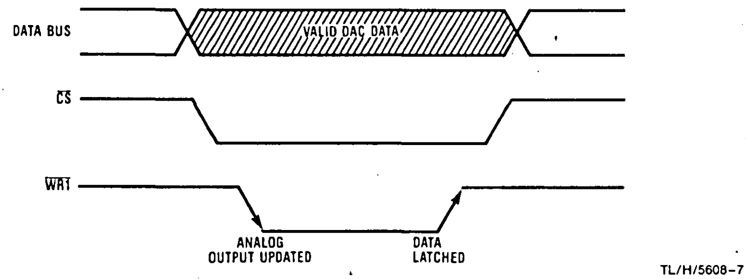
FIGURE 3.

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{CS}$ signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

DAC0830 Series Application Hints (Continued)



ILE = LOGIC "1"; $\overline{WR2}$ and $\overline{XFER}$ GROUNDED

FIGURE 4.

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughout to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in *Figure 4*.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR_1}$ low to update the DAC with $\overline{CS}$, $\overline{WR_2}$ and $\overline{XFER}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR_1}$, $\overline{WR_2}$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 900 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 180ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 50ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulsewidth. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 5* for an exemplary system which provides a 250ns $\overline{WR}$ strobe time with a data hold time of less than 10ns.

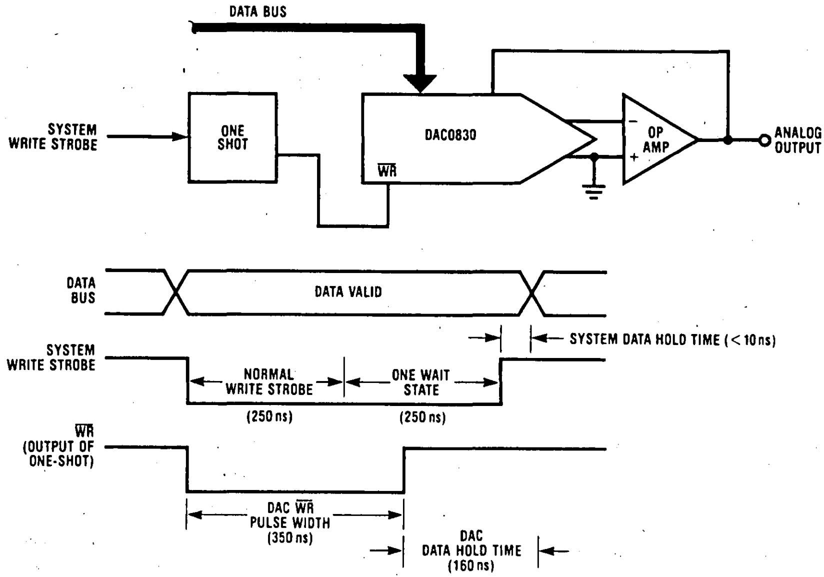
The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulsewidth is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (*Figure 8*) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

DAC0830 Series Application Hints (Continued)



TL/H/5608-8

FIGURE 5. Accommodating a High Speed System

2.0 ANALOG CONSIDERATIONS

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\ k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\ k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, *Figure 6*, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in *Figure 6*. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With V_{REF} = +10V every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 7*.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15 kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

DAC0830 Series Application Hints (Continued)

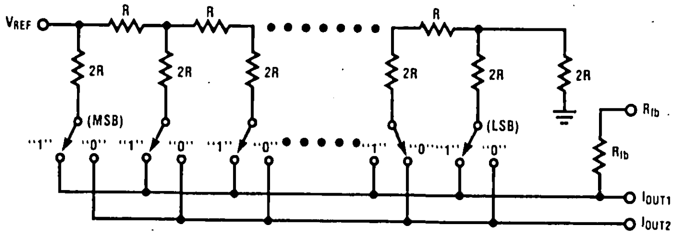


FIGURE 6.

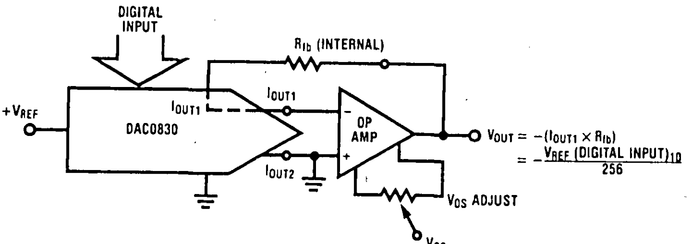


FIGURE 7.

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2.3 Op Amp Considerations

The op amp used in *Figure 7* should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 8*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

2.4 Bipolar Output Voltage with a Fixed Reference

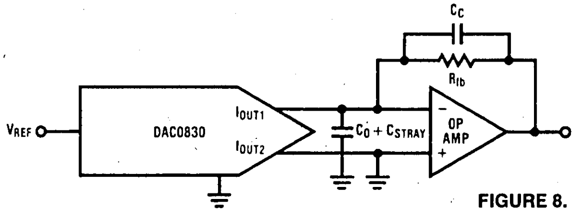
The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm$Digital Code$= \mp V_{OUT}$. This circuit is shown in *Figure 9*.

This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DACs. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking tempco. Two of the four available 10 kΩ resistors can be paralleled to form R in *Figure 9* and the other two can be used independently as the resistances labeled 2R.

2.5 Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

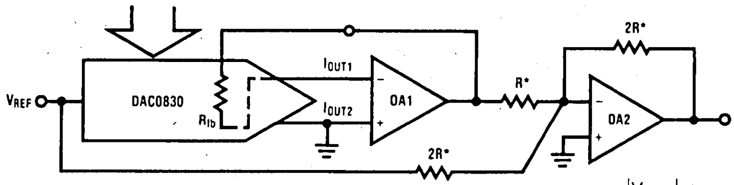
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (*Figure 7*) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.



OP AMP	C_C	t_s (O TO FULL SCALE)
LF356	22 pF	4 μs
LF351	22 pF	5 μs
LF357*	10 pF	2 μs

*2.4 kΩ RESISTOR ADDED FROM – INPUT TO GROUND TO INSURE STABILITY

FIGURE 8.



$$V_{OUT} = V_{REF} \frac{(\text{DIGITAL CODE} - 128)}{128}$$

$$1\ \text{LSB} = \frac{|V_{REF}|}{128}$$

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*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

INPUT CODE	IDEAL V_{OUT}	
MSB ....LSB	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	-1 LSB	$+1$ LSB
0 0 1 1 1 1 1 1	$-\frac{\lvert V_{REF}\rvert}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0 0 0 0 0 0 0 0	$-\lvert V_{REF}\rvert$	$+\lvert V_{REF}\rvert$

FIGURE 9.

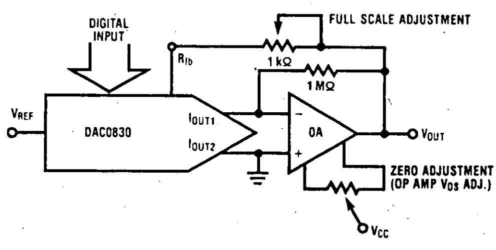
2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in *Figure 10* to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error tempco by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in *Figure 10*, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error tempco would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Using the DAC0830 in a Voltage Switching Configuration

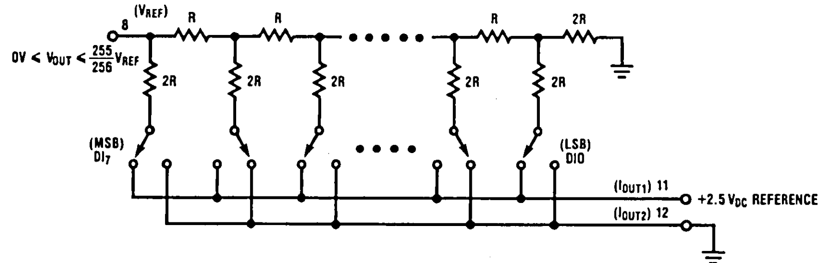
The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in *Figure 11*.



TL/H/5608-11

FIGURE 10. Adding Full-Scale Adjustment

DAC0830 Series Application Hints (Continued)

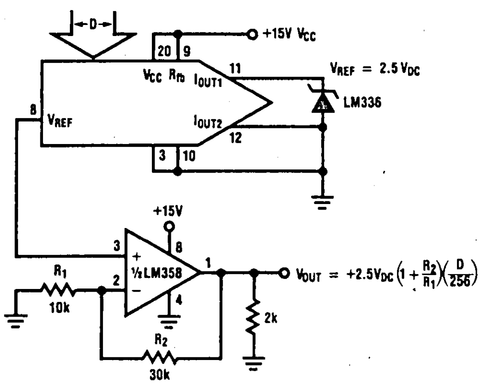


TL/H/5608-12

FIGURE 11. Voltage Mode Switching

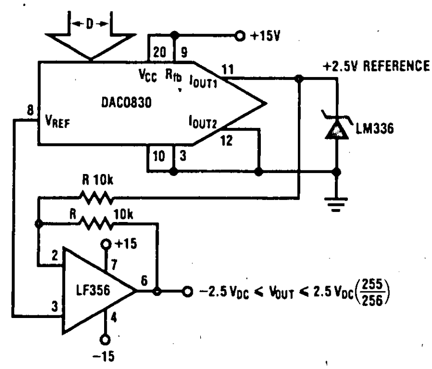
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in *Figures 12, 13, 14* and *15*.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drive requirements of the ladder switches. To insure that all 8 switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions insure less than 0.1% linearity and gain error change. *Figures 16, 17* and *18* characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.



- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

FIGURE 12. Single Supply DAC



TL/H/5608-13

- $V_{OUT} = 2.5V\left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 μs

FIGURE 13. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

DAC0830 Series Application Hints (Continued)

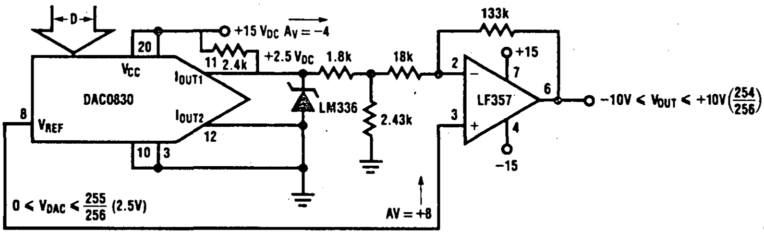
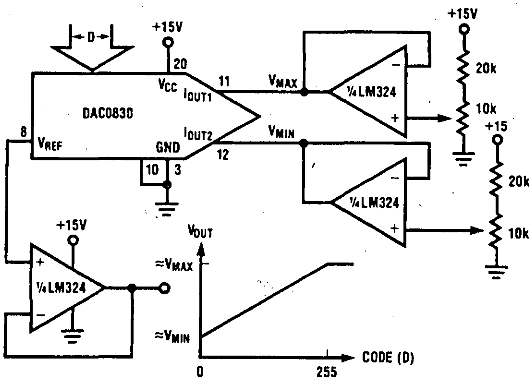


FIGURE 14. Bipolar Output with Increased Output Voltage Swing



TL/H/5608-14

- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be $\leq +5VDC$ and $\geq 0V$.
- Incremental Output Step $= \frac{1}{256}(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}V_{MIN}$

FIGURE 15. Single Supply DAC with Level Shift and Span-Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage

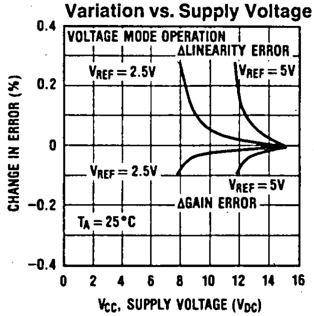


FIGURE 16.

Gain and Linearity Error Variation vs. Reference Voltage

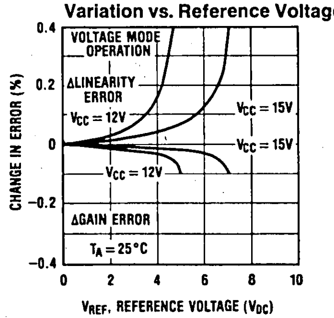
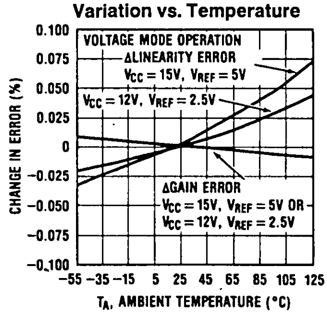


FIGURE 17.

Note: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

Gain and Linearity Error Variation vs. Temperature



TL/H/5608-15

FIGURE 18.

DAC0830 Series Application Hints (Continued)

2.8 Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DACs.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

3.0 GENERAL APPLICATION IDEAS

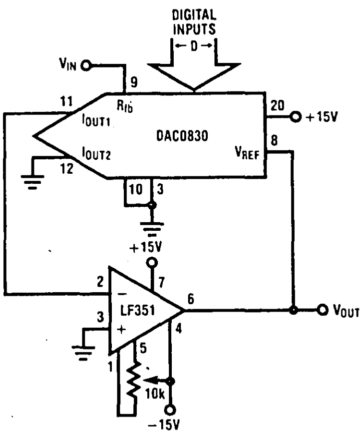
The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input Pin 13 MSB							Pin 7 LSB	D Decimal Equivalent
1	1	1	1	1	1	1	1	255
1	0	0	0	0	0	0	0	128
0	0	0	1	0	0	0	0	16
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0

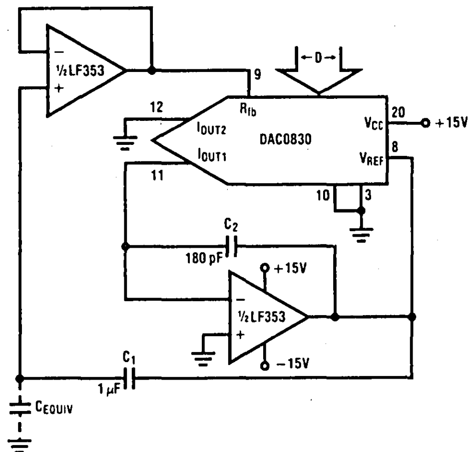
Applications

DAC Controlled Amplifier (Volume Control)



- $V_{OUT} = \dfrac{-V_{IN}(256)}{D}$
- When D = 0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the −input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.

Capacitance Multiplier

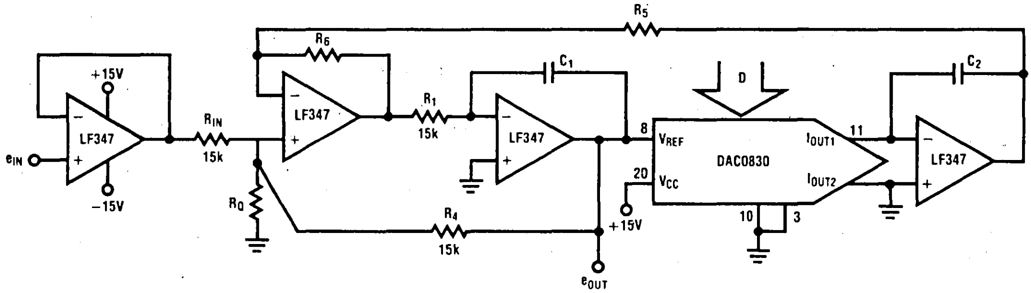


TL/H/5608-16

- $C_{EQUIV} = C_1\left(1 + \dfrac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\dfrac{V_{O\,MAX}\,(\text{op amp})}{1 + \dfrac{256}{D}}$
- C_2 is used to improve settling time of op amp.

Applications (Continued)

Variable f_O, Variable Q_O, Constant BW Bandpass Filter

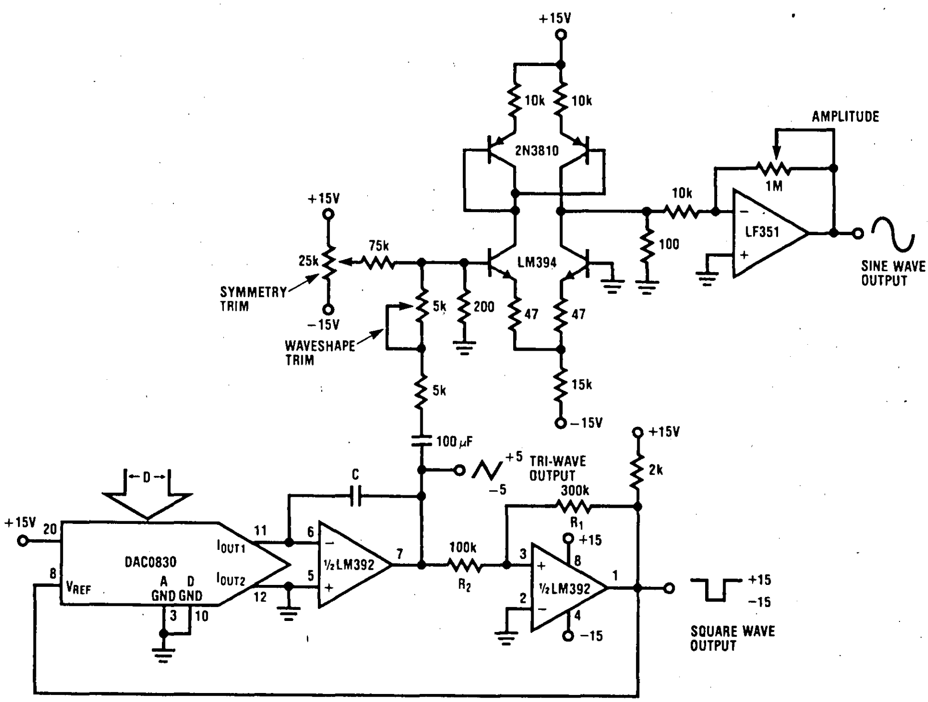


TL/H/5608–17

- $f_O = \dfrac{\sqrt{\frac{KD}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\dfrac{KD(2R_Q + R_1)}{256\, R_Q(K+1)}}$; $3dbBW = \dfrac{R_Q(K+1)}{2\pi R_1 C(2R_Q + R_1)}$

  where $G_1 = C_2 = C$; $K = \dfrac{R_6}{R_5}$ and $R_1 = R$ of DAC = 15k
- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is $\approx$ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be $\leq$200 kHz.

DAC Controlled Function Generator

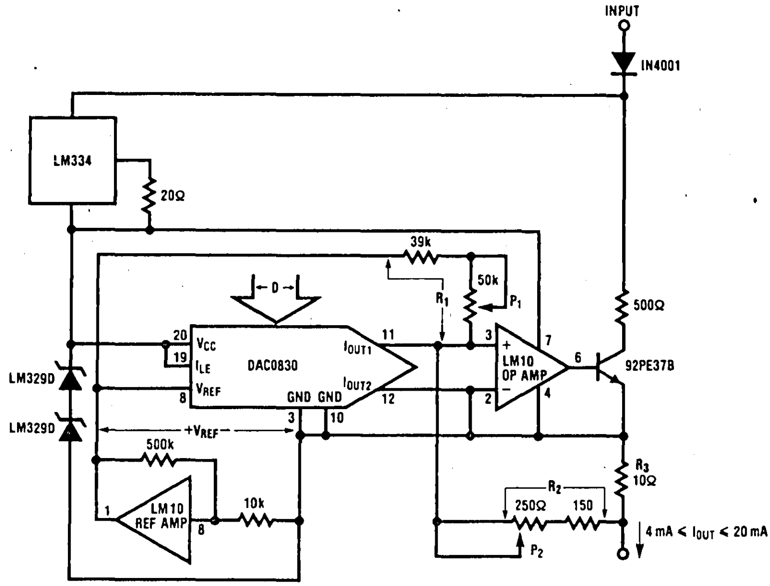


TL/H/5608–18

- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \dfrac{D}{256(20k)C}$ for $V_{OMAX} = V_{OMIN}$ of square wave output and $R_2 = 3\ R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave-shape for minimum sine wave distortion.

Applications (Continued)

Two Terminal Floating 4 to 20 mA Current Loop Controller

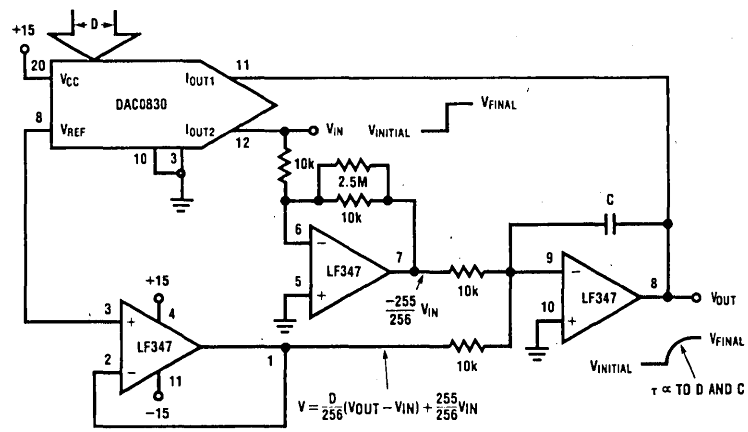


TL/H/5608-19

$$I_{OUT} = V_{REF}\left[\frac{1}{R_1} + \frac{D}{256\,R_{fb}}\right]\left[1 + \frac{R_2}{R_3}\right]$$

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D=0) to 19.94 mA (for D=255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).

DAC Controlled Exponential Time Response



TL/H/5608-20

- Output responds exponentially to input changes and automatically stops when $V_{OUT} = V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See section 2.7)

National Semiconductor

DAC1000, DAC1001, DAC1002, DAC1006, DAC1007, DAC1008 μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1000/1/2 and DAC1006/7/8 are advanced CMOS/Si-Cr 10-, 9- and 8-bit accurate multiplying DACs which are designed to interface directly with the 8080, 8048, 8085, Z-80 and other popular microprocessors. These DACs appear as a memory location or an I/O port to the μP and no interfacing logic is needed.

These devices, combined with an external amplifier and voltage reference, can be used as standard D/A converters; and they are very attractive for multiplying applications (such as digitally controlled gain blocks) since their linearity error is essentially independent of the voltage reference. They become equally attractive in audio signal processing equipment as audio gain controls or as programmable attenuators which marry high quality audio signal processing to digitally based systems under microprocessor control.

All of these DACs are double buffered. They can load all 10 bits or two 8-bit bytes and the data format can be either right justified or left justified. The analog section of these DACs is essentially the same as that of the DAC1020.

The DAC1000 series are the 10-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC's). For applications requiring other resolutions, the DAC0830 series (8 bits) and the DAC1208 and DAC1230 (12 bits) are available alternatives.

Part #	Accuracy (bits)	Pin	Description
DAC1000	10	24	Has all logic features
DAC1001	9		
DAC1002	8		
DAC1006	10	20	For left-justified data
DAC1007	9		
DAC1008	8		

Features

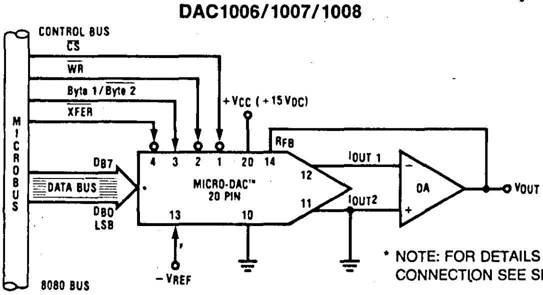
- Uses easy to adjust END POINT specs, NOT BEST STRAIGHT LINE FIT
- Low power consumption
- Direct interface to all popular microprocessors.
- Integrated thin film on CMOS structure
- Double-buffered, single-buffered or flow through digital data inputs.
- Loads two 8-bit bytes or a single 10-bit word.
- Logic inputs which meet T^2L voltage level specs (1.4V logic threshold).
- Works with ±10V reference—full 4-quadrant multiplication.
- Operates STAND ALONE (without μP) if desired.
- Available in 0.3″ standard 20-pin and 0.6″ 24-pin package.
- Differential non-linearity selection available as special order.

Key Specifications

- Output Current Settling Time — 500 ns
- Resolution — 100 bits
- Linearity — 10, 9, and 8 bits (guaranteed over temp.)
- Gain Tempco — −0.0003% of FS/°C
- Low Power Dissipation (including ladder) — 20 mW
- Single Power Supply — 5 to 15 V_{DC}

Typical Application

DAC1006/1007/1008



* NOTE: FOR DETAILS OF BUS CONNECTION SEE SECTION 6.0

TL/H/5688–1

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65°C to +150°C
Package dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−10 mV to V_{CC}
Lead temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCD' suffix	−40°C to +85°C
Part numbers with 'LD' suffix	−55°C to +125°C
Voltage at any digital input	V_{CC} to GND

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted

Parameter	Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$			$V_{CC} = 5V_{DC} \pm 5\%$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution					10			10	bits
Linearity Error	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1000 and 1006				0.05			0.05	% of FSR
	DAC1001 and 1007				0.1			0.1	% of FSR
	DAC1002 and 1008				0.2			0.2	% of FSR
Differential Nonlinearity	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1000 and 1006				0.1			0.1	% of FSR
	DAC1001 and 1007				0.2			0.2	% of FSR
	DAC1002 and 1008				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1000 and 1006		10			10			bits
	DAC1001 and 1007		9			9			bits
	DAC1002 and 1008		8			8			bits
Gain Error	Using internal R_{fb} $-10V \le V_{REF} \le +10V$	5	−1.0	±0.3	1.0	−1.0	±0.3	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6							
	Using internal R_{fb}	9		−0.0003	−0.001		−0.0006	−0.002	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	$V_{CC} = 14.5V$ to 15.5V			0.003	0.008				% FSR/V
	11.5V to 12.5V			0.004	0.010				% FSR/V
	4.75V to 5.25V						0.033	0.10	% FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	$V_{REF} = 20V_{p\text{-}p}$, f = 100 kHz								
	All data inputs latched low								
	D Package			130			130		$mV_{p\text{-}p}$
	N Package			90			90		$mV_{p\text{-}p}$
Output Capacitance I_{OUT1}	All data inputs			60			60		pF
I_{OUT2}	latched low			250			250		pF
I_{OUT1}	All data inputs			250			250		pF
I_{OUT2}	latched high			60			60		pF
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$	6		0.5	2.0		0.5	2.0	mA
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$	6							
I_{OUT1}	All data inputs latched low	10			200			200	nA
I_{OUT2}	All data inputs latched high				200			200	nA
Digital Input Voltages	$T_{MIN} \le T_A \le T_{MAX}$	6							
	Low level								
	LD suffix				0.8			0.6	V_{DC}
	LCD or LCN suffix				0.8			0.8	V_{DC}
	High level (all parts)		2.0			2.0			V_{DC}

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted

Parameter	Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$			$V_{CC} = 5V_{DC} \pm 5\%$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$	6							
	Digital inputs $<0.8V$			−40	−150		−40	−150	μA_{DC}
	Digital inputs $>2.0V$			1.0	+10		1.0	+10	μA_{DC}
Current Settling Time t_S	$V_{IL} = 0V$, $V_{IH} = 5V$			500			500		ns
Write and $\overline{XFER}$ Pulse Width t_W	$V_{IL} = 0V$, $V_{IH} = 5V$,								
	$T_A = 25°C$	8	150	60		320	200		ns
	$T_{MIN} \le T_A \le T_{MAX}$	9	320	100		500	250		ns
Data Set Up Time t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$,								
	$T_A = 25°C$	9	150	80		320	170		ns
	$T_{MIN} \le T_A \le T_{MAX}$		320	120		500	250		ns
Data Hold Time t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$								
	$T_A = 25°C$	9	200	100		320	220		ns
	$T_{MIN} \le T_A \le T_{MAX}$		250	120		500	320		ns
Control Set Up Time t_{CS}	$V_{IL} = 0V$, $V_{IL} = 5V$,								
	$T_A = 25°C$	9	150	60		320	180		ns
	$T_{MIN} \le T_A \le T_{MAX}$		320	100		500	260		ns
Control Hold Time t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$,								
	$T_A = 25°C$	9	10	0		10	0		ns
	$T_{MIN} \le T_A \le T_{MAX}$		10	0		10	0		ns

Note 1: *"Absolute Maximum Ratings"* are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these *"Absolute Maximum"* limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 6: $T_{MIN} = 0°C$ and $T_{MAX} = 70°C$ for "LCN" suffix parts.
$T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.
$T_{MIN} = 55°C$ and $T_{MAX} = 125°C$ for "LD" suffix parts.

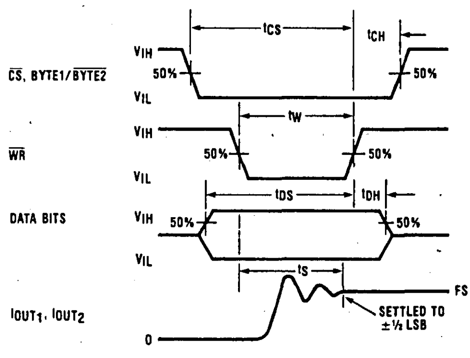
Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC1000 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 1024 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: Guaranteed by design but not tested.

Note 10: A 200 nA leakage current with $R_{fb} = 20K$ and $V_{REF} = 10V$ corresponds to a zero error of $(200 \times 10^{-9} \times 20 \times 10^3) \times 100 \div 10$ which is 0.04% of FS.

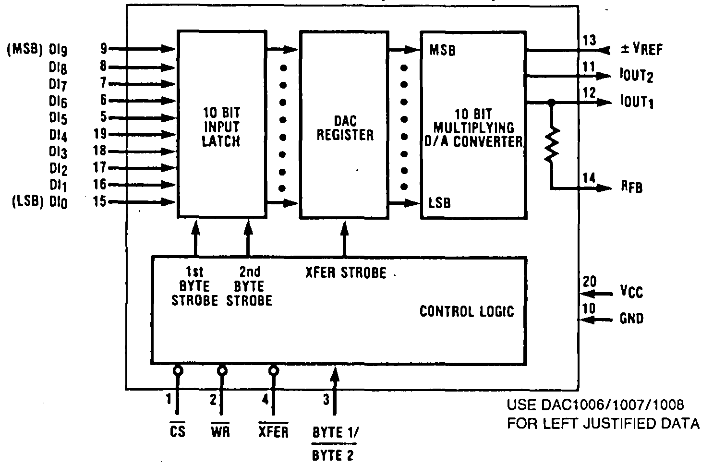
Switching Waveforms



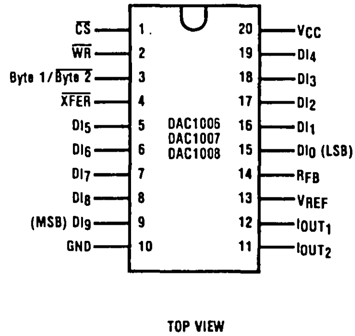
TL/H/5688-2

Block and Connection Diagrams (Continued)

DAC1006/1007/1008 (20-Pin Parts)

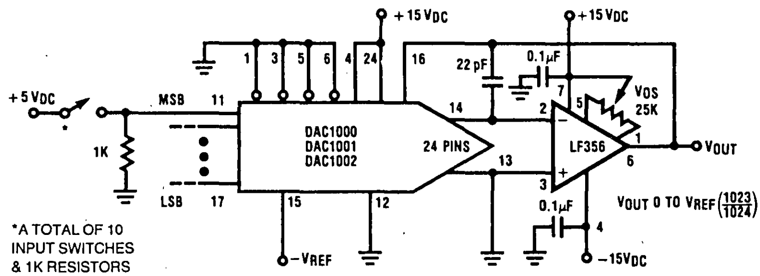


DAC1006/1007/1008
(20-Pin Parts)



TL/H/5688-5

DAC1000/1001/1002—Simple Hookup for a "Quick Look"

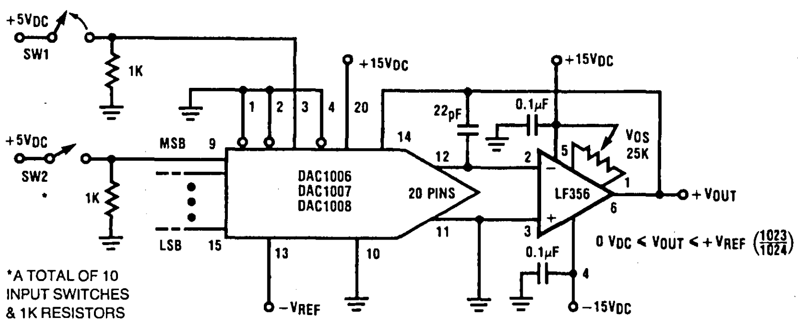


TL/H/5688-6

Notes:

1. For $V_{REF} = -10.240\ V_{DC}$ the output voltage steps are approximately 10 mV each.
2. Operation is set up for flow through—no latching of digital input data.
3. Single point ground is strongly recommended.

DAC1006/1007/1008—Simple Hookup for a "Quick Look"



TL/H/5688-7

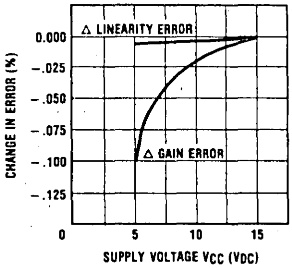
Notes:

1. For $V_{REF} = -10.240\ V_{DC}$ the output voltage steps are approximately 10 mV each.
2. SW1 is a normally closed switch. While SW1 is closed, the DAC register is latched and new data can be loaded into the input latch via the 10 SW2 switches.

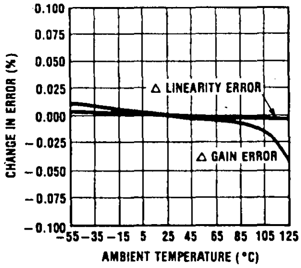
When SW1 is momentarily opened the new data is transferred from the input latch to the DAC register and is latched when SW1 again closes.

Typical Performance Characteristics

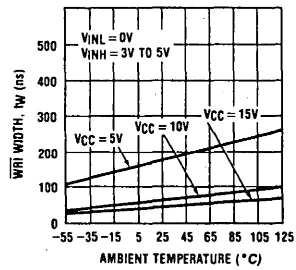
Errors vs. Supply Voltage



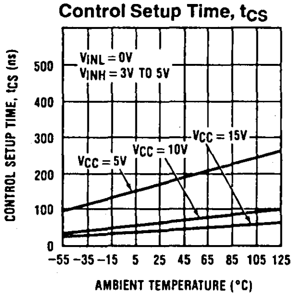
Errors vs. Temperature



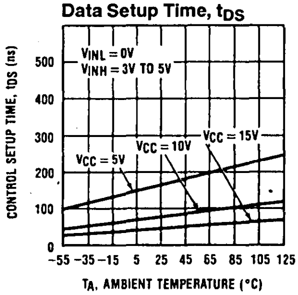
Write Width, t_W



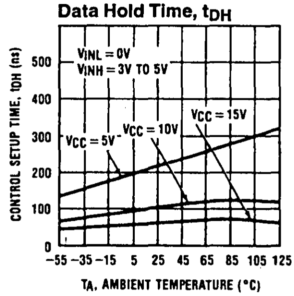
Control Setup Time, t_{CS}



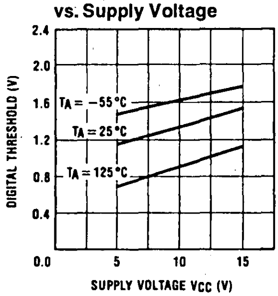
Data Setup Time, t_{DS}



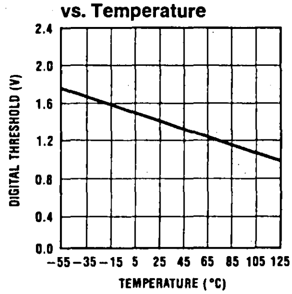
Data Hold Time, t_{DH}



Digital Threshold vs. Supply Voltage



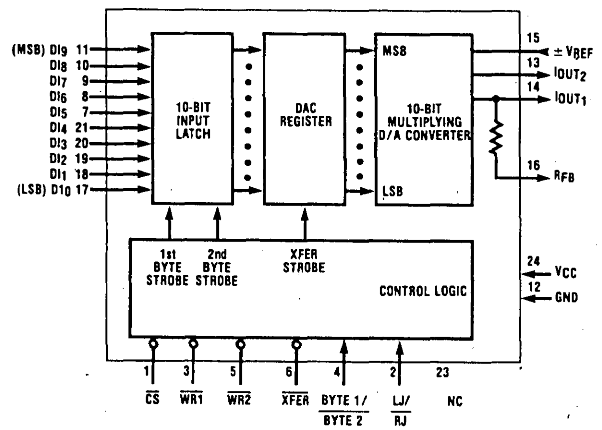
Digital Input Threshold vs. Temperature



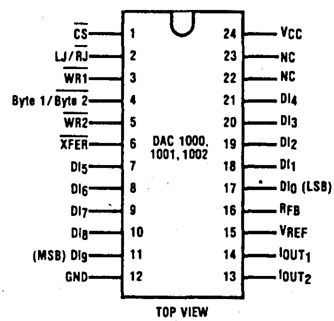
TL/H/5688–3

Block and Connection Diagrams

DAC1000/1001/1002 (24-Pin Parts)



DAC1000/1001/1002 (24-Pin Parts)



See Ordering Information

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1.0 DEFINITION OF PACKAGE PINOUTS

1.1 Control Signals (All control signals are level actuated.)

$\overline{CS}$: Chip Select — active low, it will enable $\overline{WR}$ (DAC1003-1008) or WR_1 (DAC1000-1002).

$\overline{WR}$ or $\overline{WR_1}$: Write — The active low $\overline{WR}$ (or $\overline{WR_1}$ — DAC1000-1002) is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR}$ (or $\overline{WR_1}$) is high. The 10-bit input latch is split into two latches; one holds 8 bits and the other holds 2 bits. The Byte1/$\overline{\text{Byte2}}$ control pin is used to select both input latches when Byte1/$\overline{\text{Byte2}}$ = 1 or to overwrite the 2-bit input latch when in the low state.

$\overline{WR_2}$: Extra Write (DAC1000-1002) — The active low $\overline{WR_2}$ is used to load the data from the input latch to the DAC register while $\overline{XFER}$ is low. The data in the DAC register is latched when WR_2 is high.

Byte1/$\overline{\text{Byte2}}$: Byte Sequence Control — When this control is high, all ten locations of the input latch are enabled. When low, only two locations of the input latch are enabled and these two locations are overwritten on the second byte write. On the DAC1006, 1007, and 1008, the Byte1/$\overline{\text{Byte2}}$ must be low to transfer the 10-bit data in the input latch to the DAC register.

$\overline{XFER}$: Transfer Control Signal, active low — This signal, in combination with others, is used to transfer the 10-bit data which is available in the input latch to the DAC register — see timing diagrams.

LJ/$\overline{RJ}$: Left Justify/Right Justify (DAC1000-1002) — When LJ/$\overline{RJ}$ is high the part is set up for left justified (fractional) data format. (DAC1006-1008 have this done internally.) When LJ/$\overline{RJ}$ is low, the part is set up for right justified (integer) data.

1.2 Other Pin Functions

DI_i (i = 0 to 9): Digital Inputs — DI_0 is the least significant bit (LSB) and DI_9 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1 — I_{OUT1} is a maximum for a digital input code of all 1s and is zero for a digital input code of all 0s.

I_{OUT2}: DAC Current Output 2 — I_{OUT2} is a constant minus I_{OUT1}, or

$$I_{OUT1} + I_{OUT2} = \frac{1023\ V_{REF}}{1024\ R}$$

where R ≅ 15 kΩ.

R_{FB}: Feedback Resistor — This is provided on the IC chip for use as the shunt feedback resistor when an external op amp is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) because it matches the resistors used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input — This is the connection for the external precision voltage source which drives the R-2R ladder. V_{REF} can range from −10 to +10 volts. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage — This is the power supply pin for the part. V_{CC} can be from +5 to +15 V_{DC}. Operation is optimum for +15V. The input threshold voltages are nearly independent of V_{CC}. (See Typical Performance Characteristics and Description in Section 3.0, T^2L compatible logic inputs.)

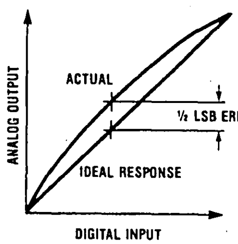
GND: Ground — the ground pin for the part.

1.3 Definition of Terms

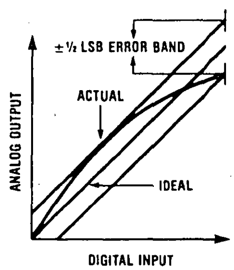
Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC1000 has 2^{10} or 1024 steps and therefore has 10-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the "best straight line" test (b) used by other suppliers are illustrated below. The "best straight line" requires a special zero and FS adjustment for each part, which is almost impossible for user to determine. The "end point test" uses a standard zero and FS adjustment procedure and is a much more stringent test for DAC linearity.



a. End Point Test After Zero and FS Adj.



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b. Best Straight Line

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within $\pm 1/2$ LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1000 series, full-scale is $V_{REF}-1$ LSB. For $V_{REF}=-10V$ and unipolar operation, $V_{FULL\text{-}SCALE}=10.0000V\ -9.8mV=9.9902V$. Full-scale error is adjustable to zero.

Monotonicity: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 10-bit DAC with 10-bit monotonicity will produce an increasing analog output when all 10 digital inputs are exercised. A 10-bit DAC with 9-bit monotonicity will be monotonic when only the most significant 9 bits are exercised. Similarly, 8-bit monotonicity is guaranteed when only the most significant 8 bits are exercised.

2.0 DOUBLE BUFFERING

These DACs are double-buffered, microprocessor compatible versions of the DAC1020 10-bit multiplying DAC. The addition of the buffers for the digital input data not only allows for storage of this data, but also provides a way to assemble the 10-bit input data word from two write cycles when using an 8-bit data bus. Thus, the next data update for the DAC output can be made with the complete new set of 10-bit data. Further, the double buffering allows many DACs in a system to store current data and also the next data. The updating of the new data for each DAC is also not time critical. When all DACs are updated, a common strobe signal can then be used to cause all DACs to switch to their new analog output levels.

3.0 T²L COMPATIBLE LOGIC INPUTS

To guarantee T²L voltage compatibility of the logic inputs, a novel bipolar (NPN) regulator circuit is used. This makes the input logic thresholds equal to the forward drop of two diodes (and also matches the temperature variation) as occurs naturally in T²L. The basic circuit is shown in *Figure 1*. A curve of digital input threshold as a function of power supply voltage is shown in the Typical Performance Characteristics section.

4.0 APPLICATION HINTS

The DC stability of the V_{REF} source is the most important factor to maintain accuracy of the DAC over time and temperature changes. A good single point ground for the analog signals is next in importance.

These MICRO-DAC converters are CMOS products and reasonable care should be exercised in handling them prior to final mounting on a PC board The digital inputs are protected, but permanent damage may occur if the part is subjected to high electrostatic fields. Store unused parts in conductive foam or anti-static rails.

4.1 Power Supply Sequencing & Decoupling

Some IC amplifiers draw excessive current from the Analog inputs to V− when the supplies are first turned on. To prevent damage to the DAC — an external Schottky diode connected from I_{OUT1} or I_{OUT2} to ground may be required to prevent destructive currents in I_{OUT1} or I_{OUT2}. If an LM741 or LF356 is used — these diodes are not required.

The standard power supply decoupling capacitors which are used for the op amp are adequate for the DAC.

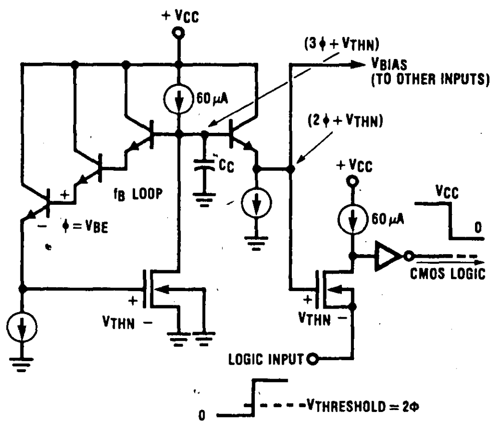

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FIGURE 1. Basic Logic Threshold Loop

4.2 Op Amp Bias Current & Input Leads

The op amp bias current (I_B) CAN CAUSE DC ERRORS. BI-FET™ op amps have very low bias current, and therefore the error introduced is negligible. BI-FET op amps are strongly recommended for these DACs.

The distance from the I_{OUT1} pin of the DAC to the inverting input of the op amp should be kept as short as possible to prevent inadvertent noise pickup.

5.0 ANALOG APPLICATIONS

The analog section of these DACs uses an R-2R ladder which can be operated both in the current switching mode and in the voltage switching mode.

The major product changes (compared with the DAC1020) have been made in the digital functioning of the DAC. The analog functioning is reviewed here for completeness. For additional analog applications, such as multipliers, attenuators, digitally controlled amplifiers and low frequency sine wave oscillators, refer to the DAC1020 data sheet. Some basic circuit ideas are presented in this section in addition to complete applications circuits.

5.1 Operation in Current Switching Mode

The analog circuitry, *Figure 2*, consists of a silicon-chromium (Si-Cr) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there is no parasitic diode connected to the V_{REF} pin as would exist if diffused resistors were used. The reference voltage input (V_{REF}) can therefore range from −10V to +10V.

The digital input code to the DAC simply controls the position of the SPDT current switches, SW0 to SW9. A logical 1 digital input causes the current switch to steer the available ladder current to the I_{OUT1} output pin. These MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

5.1.1 Providing a Unipolar Output Voltage with the DAC in the Current Switching Mode

A voltage output is provided by making use of an external op amp as a current-to-voltage converter. The idea is to use the internal feedback resistor, R_{FB}, from the output of the op amp to the inverting (−) input. Now, when current is entered at this inverting input, the feedback action of the op amp keeps that input at ground potential. This causes the applied input current to be diverted to the feedback resistor. The output voltage of the op amp is forced to a voltage given by:

$$V_{OUT} = -(I_{OUT1} \times R_{FB})$$

Notice that the sign of the output voltage depends on the direction of current flow through the feedback resistor.

In current switching mode applications, both current output pins (I_{OUT1} and I_{OUT2}) should be operated at 0 V_{DC}. This is accomplished as shown in *Figure 3*. The capacitor, C_C, is used to compensate for the output capacitance of the DAC and the input capacitance of the op amp. The required feedback resistor, R_{FB}, is available on the chip (one end is internally tied to I_{OUT1}) and must be used since an external resistor will not provide the needed matching and temperature tracking. This circuit can therefore be simplified as

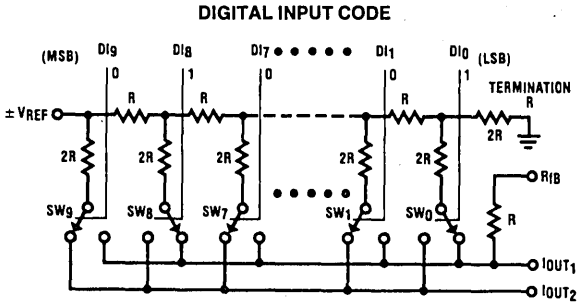

FIGURE 2. Current Mode Switching

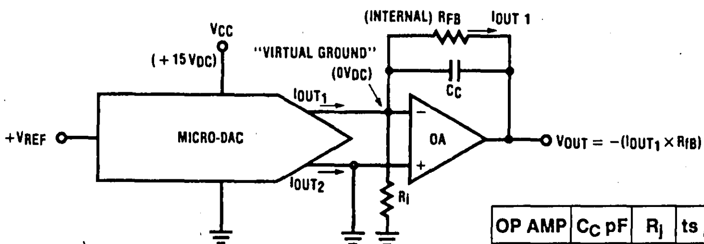

FIGURE 3. Converting I_{OUT} to V_{OUT}

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OP AMP	C_C pF	R_i	ts µS
LF356	22	∞	3
LF351	24	∞	4
LF357	10	2.4k	1.5

shown in *Figure 4*, where the sign of the reference voltage has been changed to provide a positive output voltage. Note that the output current, I_{OUT1}, now flows through the R_{FB} pin.

5.1.2 Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

The addition of a second op amp to the circuit of *Figure 4* can be used to generate a bipolar output voltage from a fixed reference voltage *Figure 5*. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize the full four-quadrant multiplication.

The applied digital word is offset binary which includes a code to output zero volts without the need of a large valued resistor common to existing bipolar multiplying DAC circuits. Offset binary code can be derived from 2's complement data (most common for signed processor arithmetic) by inverting the state of the MSB in either software or hardware. After doing this the output then responds in accordance to the following expression:

$$V_O = V_{REF} \times \frac{D}{512}$$

where V_{REF} can be positive or negative and D is the signed decimal equivalent of the 2's complement processor data. ($-512 \le D \le +511$ or $1000000000 \le D \le 0111111111$). If the applied digital input is interpreted as the decimal equivalent of a true binary word, V_{OUT} can be found by:

$$V_O = V_{REF}\left(\frac{D-512}{512}\right) \qquad 0 \le D \le 1023$$

With this configuration, only the offset voltage of amplifier 1 need be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp has no effect on linearity. It presents a constant output voltage error and should be nulled only if absolute accuracy is needed. Another advantage of this configuration is that the values of the external resistors required do not have to match the value of the internal DAC resistors; they need only to match and temperature track each other.

A thin film 4 resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four available 10 kΩ resistor can be paralleled to form R in *Figure 5* and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

2's Comp. (Decimal)	2's Comp. (Binary)	Applied Digital Input	Applied True Binary (Decimal)	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
+511	0111111111	1111111111	1023	$V_{REF}-1$ LSB	$-\lvert V_{REF}\rvert+1$ LSB
+256	0100000000	1100000000	768	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
0	0000000000	1000000000	512	0	0
−1	1111111111	0111111111	511	−1 LSB	+1 LSB
−256	1100000000	0100000000	256	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
−512	1000000000	0000000000	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

with: $1\text{ LSB} = \frac{\lvert V_{REF}\rvert}{512}$

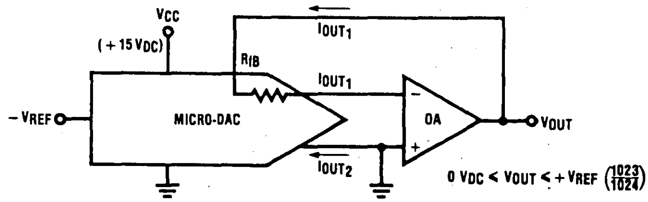

FIGURE 4. Providing a Unipolar Output Voltage

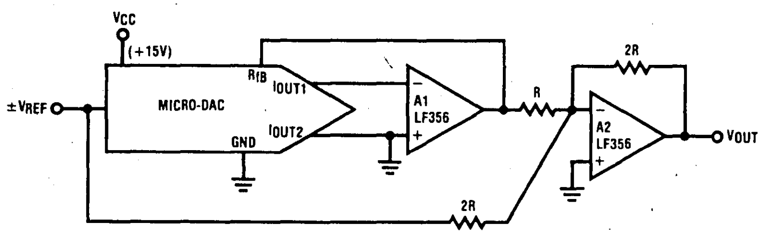

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FIGURE 5. Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

5.2 Analog Operation in the Voltage Switching Mode

Some useful application circuits result if the R-2R ladder is operated in the voltage switching mode. There are two very important things to remember when using the DAC in the voltage mode. The reference voltage (+V) must always be positive since there are parasitic diodes to ground on the I_{OUT1} pin which would turn on if the reference voltage went negative. To maintain a degradation of linearity less than ±0.005%, keep $+V \leq 3\ V_{DC}$ and V_{CC} at least 10V more positive than +V. *Figures 6* and *7* show these errors for the voltage switching mode. This operation appears unusual, since a reference voltage (+V) is applied to the I_{OUT1} pin and the voltage output is the V_{REF} pin. This basic idea is shown in *Figure 8.*

This V_{OUT} range can be scaled by use of a non-inverting gain stage as shown in *Figure 9.*

Notice that this is unipolar operation since all voltages are positive. A bipolar output voltage can be obtained by using a single op amp as shown in *Figure 10.* For a digital input code of all zeros, the output voltage from the V_{REF} pin is zero volts. The external op amp now has a single input of +V and is operating with a gain of −1 to this input. The output of the op amp therefore will be at −V for a digital input of all zeros. As the digital code increases, the output voltage at the V_{REF} pin increases.

Notice that the gain of the op amp to voltages which are applied to the (+) input is +2 and the gain to voltages which are applied to the input resistor, R, is −1. The output voltage of the op amp depends on both of these inputs and is given by:

$$V_{OUT} = (+V)(-1) + V_{REF}(+2)$$

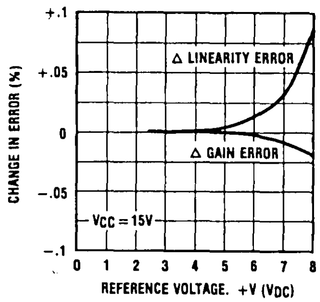

FIGURE 6.

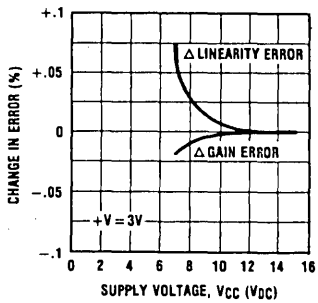

FIGURE 7.

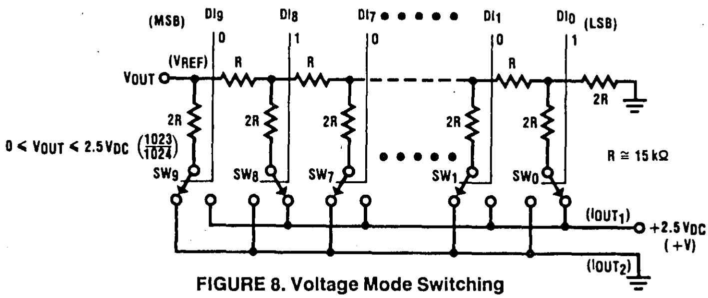

FIGURE 8. Voltage Mode Switching

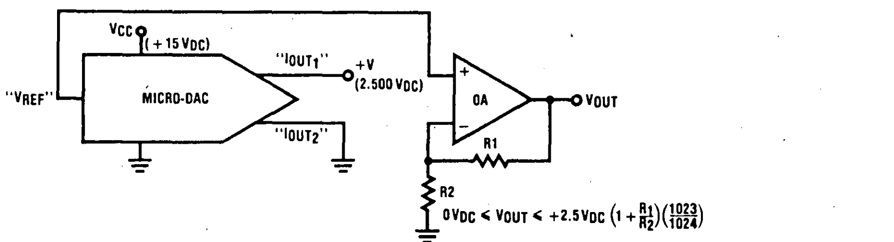

FIGURE 9. Amplifying the Voltage Mode Output (Single Supply Operation)

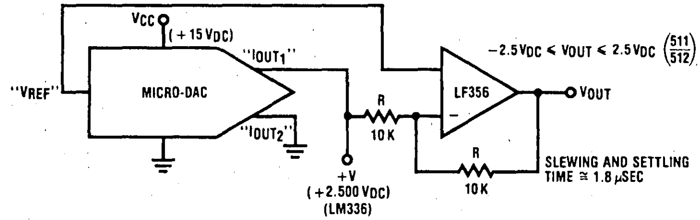

FIGURE 10. Providing a Bipolar Output Voltage with a Single Op Amp

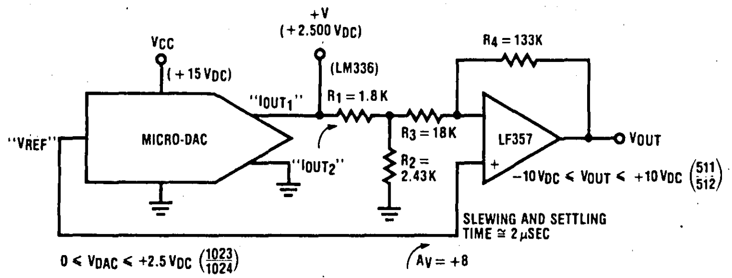

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FIGURE 11. Increasing the Output Voltage Swing

The output voltage swing can be expanded by adding 2 resistors to *Figure 10* as shown in *Figure 11*. These added resistors are used to attenuate the +V voltage. The overall gain, $A_V(-)$, from the +V terminal to the output of the op amp determines the most negative output voltage, $-4(+V)$ (when the V_{REF} voltage at the + input of the op amp is zero) with the component values shown. The complete dynamic range of V_{OUT} is provided by the gain from the (+) input of the op amp. As the voltage at the V_{REF} pin ranges from 0V to +V(1023/1024) the output of the op amp will range from -10 V_{DC} to +10V (1023/1024) when using a +V voltage of +2.500 V_{DC}. The 2.5 V_{DC} reference voltage can be easily developed by using the LM336 zener which can be biased through the R_{FB} internal resistor, connected to V_{CC}.

5.3 Op Amp V_{OS} Adjust (Zero Adjust) for Current Switching Mode

Proper operation of the ladder requires that all of the 2R legs always go to exactly 0 V_{DC} (ground). Therefore offset voltage, V_{OS}, of the external op amp cannot be tolerated as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear the 1 mV is 0.01% of the 10V reference! High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part. To prevent this source of error, the V_{OS} of the op amp has to be initially zeroed. This is the "zero adjust" of the DAC calibration sequence and should be done first.

If the V_{OS} is to be adjusted there are a few points to consider. Note that no "dc balancing" resistance should be used in the grounded positive input lead of the op amp. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET op amps makes them ideal for use in DAC current to voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force $I_{OUT}=0$ mA. A 1 kΩ resistor can be temporarily connected from the inverting input to ground to provide a dc gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense.

5.4 Full-Scale Adjust

The full-scale adjust procedure depends on the application circuit and whether the DAC is operated in the current switching mode or in the voltage switching mode. Techniques are given below for all of the possible application circuits.

5.4.1 Current Switching with Unipolar Output Voltage

After doing a "zero adjust," set all of the digital input levels HIGH and adjust the magnitude of V_{REF} for

$$V_{OUT} = -(\text{ideal } V_{REF}) \frac{1023}{1024}$$

This completes the DAC calibration.

5.4.2 Current Switching with Bipolar Output Voltage

The circuit of *Figure 12* shows the 3 adjustments needed. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adj." for zero volts at the inverting input (pin 2) of OA1. Next, with a code of all zeros still applied, adjust "−FS adj.", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+FS adj." for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. The addition of the 200Ω resistor in series with the V_{REF} pin of the DAC is to force the circuit gain error from the DAC to be negative. This insures that adding resistance to R_{fb}, with the 500Ω pot, will always compensate the gain error of the DAC.

5.4.3 Voltage Switching with a Unipolar Output Voltage

Refer to the circuit of *Figure 13* and set all digital inputs LOW. Trim the "zero adj." for $V_{OUT} = 0\ V_{DC} \pm 1$ mV. Then set all digital inputs HIGH and trim the "FS Adj." for:

$$V_{OUT} = (+V)\left(1 + \frac{R_1}{R_2}\right)\frac{1023}{1024}$$

5.4.4 Voltage Switching with a Bipolar Output Voltage

Refer to *Figure 14* and set all digital inputs LOW. Trim the "−FS Adj." for $V_{OUT} = -2.5\ V_{DC}$. Then set all digital inputs HIGH and trim the "+FS Adj." for $V_{OUT} = +2.5$ (511/512) V_{DC}. Test the zero by setting the MS digital input HIGH and all the rest LOW. Adjust V_{OS} of amp #3, if necessary, and recheck the full-scale values.

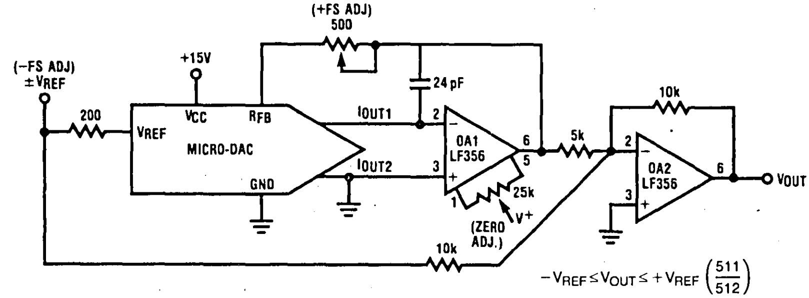

FIGURE 12. Full Scale Adjust — Current Switching with Bipolar Output Voltage

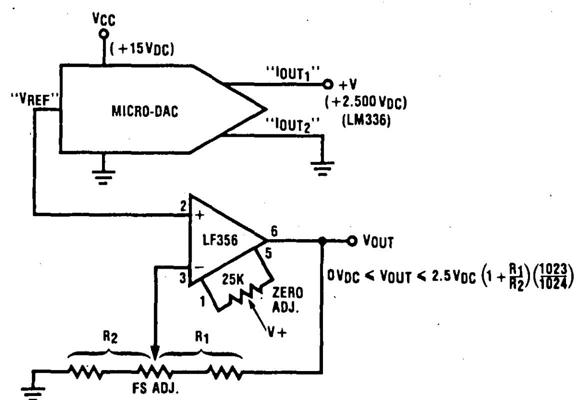

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FIGURE 13. Full Scale Adjust — Unipolar Output Voltage

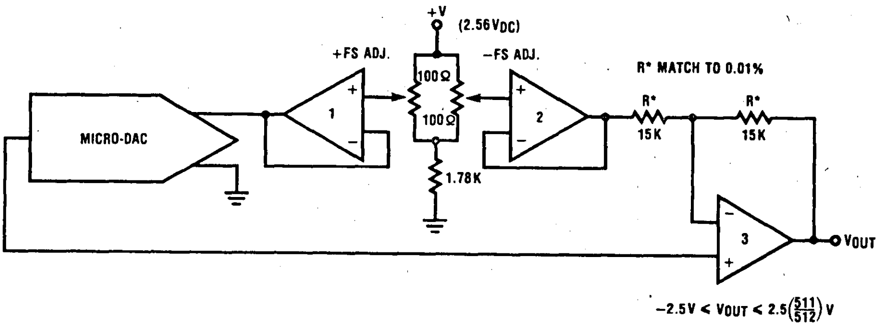

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FIGURE 14. Voltage Switching with a Bipolar Output Voltage

6.0 DIGITAL CONTROL DESCRIPTION

The DAC1000 series of products can be used in a wide variety of operating modes. Most of the options are shown in Table 1. Also shown in this table are the section numbers of this data sheet where each of the operating modes is discussed. For example, if your main interest in interfacing to a μP with an 8-bit data bus you will be directed to Section 6.1.0.

The first consideration is "will the DAC be interfaced to a μP with an 8-bit or a 16-bit data bus or used in the stand-alone mode?" For the 8-bit data bus, a second selection is made on how the 2nd digital data buffer (the DAC Latch) is updated by a transfer from the 1st digital data buffer (the Input Latch). Three options are provided: 1) an automatic transfer when the 2nd data byte is written to the DAC, 2) a transfer which is under the control of the μP and can include more than one DAC in a simultaneous transfer, or 3) a transfer which is under the control of external logic. Further, the data format can be either left justified or right justified.

When interfacing to a μP with a 16-bit data bus only two selections are available: 1) operating the DAC with a single digital data buffer (the transfer of one DAC does not have to be synchronized with any other DACs in the system), or 2) operating with a double digital data buffer for simultaneous transfer, or updating, of more than one DAC.

For operating without a μP in the stand alone mode, three options are provided: 1) using only a single digital data buffer, 2) using both digital data buffers — "double buffered," or 3) allowing the input digital data to "flow through" to provide the analog output without the use of any data latches.

To reduce the required reading, only the applicable sections of 6.1 through 6.4 need be considered.

6.1 Interfacing to an 8-Bit Data Bus

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations which depend upon two basic data format and protocol decisions:

1. Is the data to be left justified (considered as fractional binary data with the binary point to the left) or right justified (considered as binary weighted data with the binary point to the right)?
2. Which byte will be transferred first, the most significant byte (MS byte) or the least significant byte (LS byte)?

Table 1.

Operating Mode	Automatic Transfer			μP Control Transfer			External Transfer		
Data Bus	Section	Figure No. (24-Pin)	Figure No. (20-Pin)	Section	Figure No. (24-Pin)	Figure No. (20-Pin)	Section	Figure No. (24-Pin)	Figure No. (20-Pin)
8-Bit Data Bus (6.1.0)									
Right Justified (6.1.1)	6.2.1	16		6.2.2	16		6.2.3	16	
Left Justified (6.1.2)	6.2.1	17	18	6.2.2	17	18	6.2.3	17	18
16-Bit Data Bus (6.3.0)	Single Buffered			Double Buffered			Flow Through		
	6.3.1	19	20	6.3.2	19	20	Not Applicable		
Stand Alone (6.4.0)	Single Buffered			Double Buffered			Flow Through		
	6.4.1	19	20	6.4.2	19	20	6.4.3	19	NA

These data possibilities are shown in *Figure 15.* Note that the justification of data depends on how the 10-bit data word is located within the 16-bit data source (CPU) register. In either case, there is a surplus of 6 bits and these are shown as "don't care" terms ("×") in this figure.

All of these DACs load 10 bits on the 1st write cycle. A particular set of 2 bits is then overwritten on the 2nd write cycle, depending on the justification of the data. This requires the 1st write cycle to contain the LS or LO Byte data group for all right justified data options. For all left justified data options, the 1st write cycle must contain the MS or Hi Byte data group.

6.1.1 Providing for Optional Data Format

The DAC1000/1/2 (24-pin parts) can be used for either data formatting by tying the LJ/$\overline{\text{RJ}}$ pin either high or low, respectively. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in *Figure 16* for the right justified data operation. *Figure 17* is for left justified data.

6.1.2 For Left Justified Data

For applications which require left justified data, DAC1006-1008 (20-pin parts) can be used. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in *Figure 18.* These parts require the MS or Hi Byte data group to be transferred on the 1st write cycle.

6.2 Controlling Data Transfer for an 8-Bit Data Bus

Three operating modes are possible for controlling the transfer of data from the Input Latch to the DAC Register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the 2nd write cycle. This is recommended when the exact timing of the changes of the DAC analog output are not critical. This typically happens where each DAC is operating individually in a system and the analog updating of one DAC is not required to be synchronized to any other DAC. For synchronized DAC updating, two options are provided: μP control via a common $\overline{\text{XFER}}$ strobe or external update timing control via an external strobe. The details of these options are now shown.

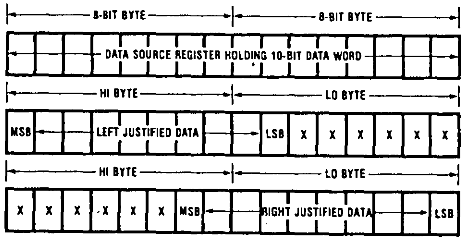
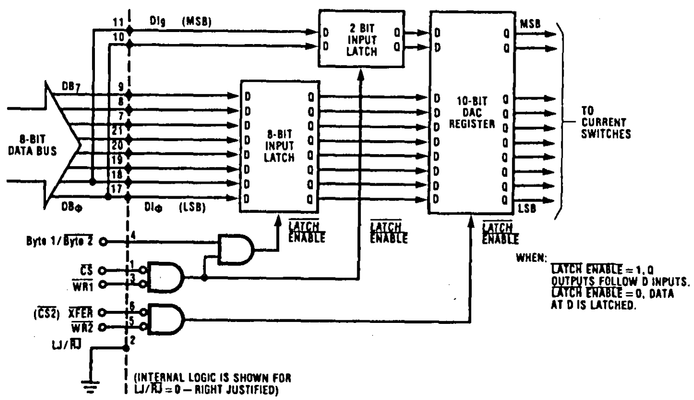


FIGURE 15. Fitting a 10-Bit Data Word into 16 Available Bit Locations

DAC1000/1001/1002 (24-Pin Parts)



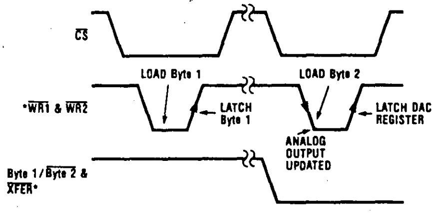
TL/H/5688-16

FIGURE 16. Input Connections and Controls for DAC1000-1002 Right Justified Data Option

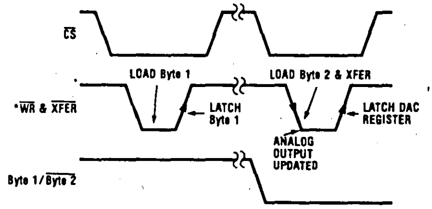
6.2.1 Automatic Transfer

This makes use of a double byte (double precision) write. The first byte (8 bits) is strobed into the input latch and the second byte causes a simultaneous strobe of the two remaining bits into the input latch and also the transfer of the complete 10-bit word from the input latch to the DAC register. This is shown in the following timing diagrams; the point in time where the analog output is updated is also indicated on these diagrams.

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



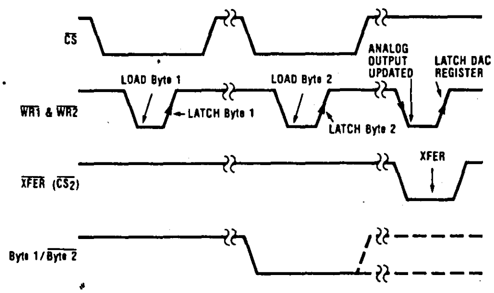
TL/H/5688-18

*SIGNIFIES CONTROL INPUTS WHICH ARE DRIVEN IN PARALLEL

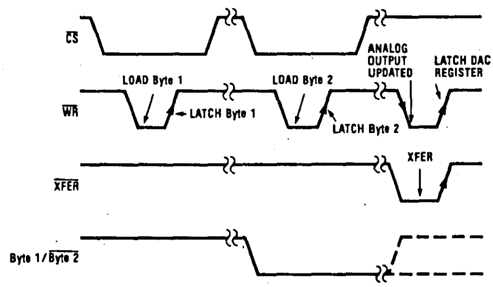
6.2.2 Transfer Using μP Write Stroke

The input latch is loaded with the first two write strobes. The $\overline{XFER}$ signal is provided by external logic, as shown below, to cause the transfer to be accomplished on a third write strobe. This is shown in the following diagrams:

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



WHERE THE XFER CONTROL CAN BE GENERATED BY USING A SECOND CHIP SELECT AS:

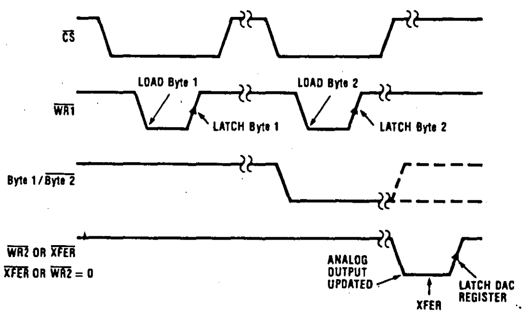
AND THE BYTE CONTROL CAN BE DERIVED FROM THE ADDRESS BUS SIGNALS.

TL/H/5688-19

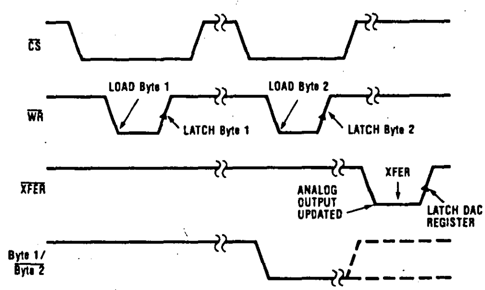
6.2.3 Transfer Using an External Strobe

This is similar to the previous operation except the $\overline{XFER}$ signal is not provided by the μP. The timing diagram for this is:

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



TL/H/5688-20

DAC1000/1001/1002 (24-Pin Parts)

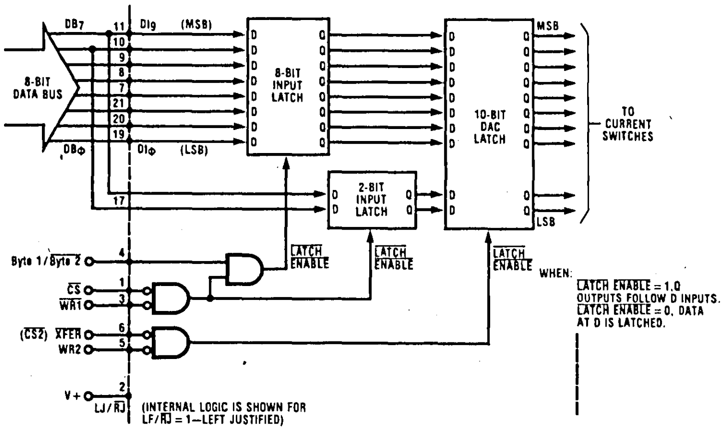
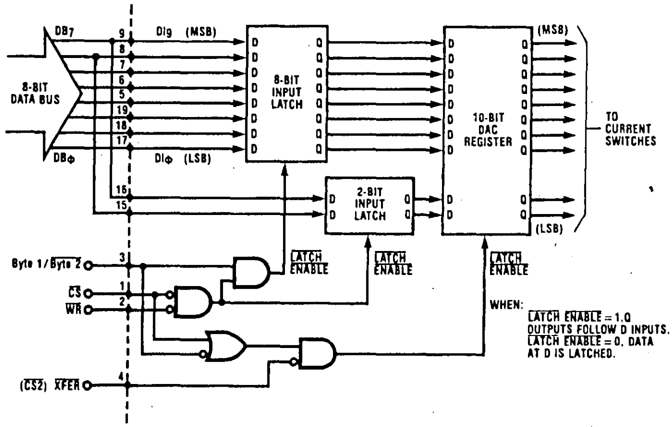


FIGURE 17. Input Connections and Controls for DAC1000–1002 Left Justified Data Option

DAC1006/1007/1008 (20-Pin Parts for Left Justified Data)



TL/H/5688–17

FIGURE 18. Input Connections and Controls for DAC1006/1007/1008 Left Justified Data

6.3 Interfacing to a 16-Bit Data Bus

The interface to a 16-bit data bus is easily handled by connecting to 10 of the available bus lines. This allows a wiring selected right justified or left justified data format. This is shown in the connection diagrams of *Figures 19* and *20*, where the use of DB6 to DB15 gives left justified data operation. Note that any part number can be used and the Byte1/$\overline{\text{Byte2}}$ control should be wired Hi.

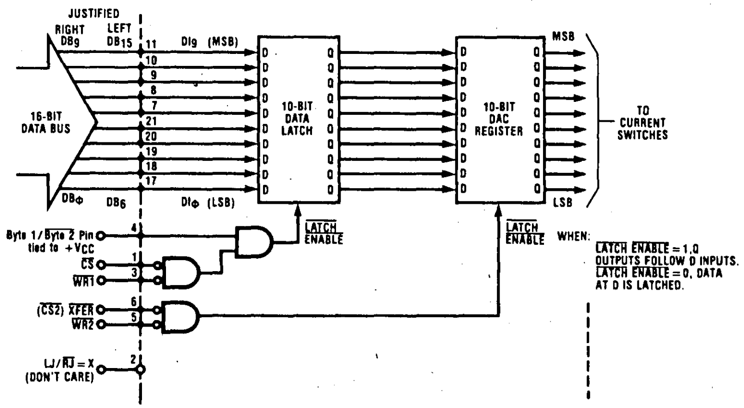
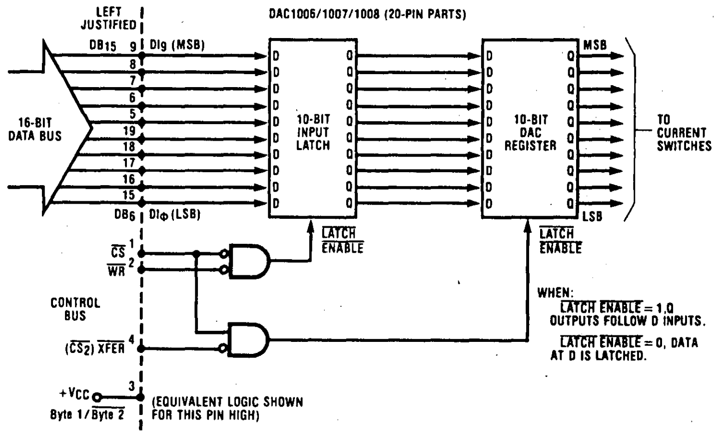


FIGURE 19. Input Connections and Logic for DAC1000–1002 with 16-Bit Data Bus



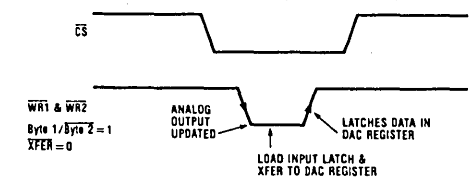
TL/H/5688–21

FIGURE 20. Input Connections and Logic for DAC1006/1007/1008 with 16-Bit Data Bus

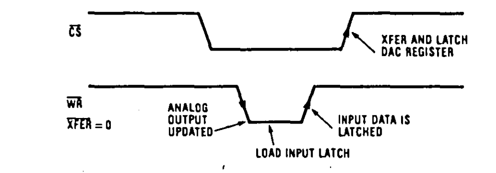
Three operating modes are possible: flow through, single buffered, or double buffered. The timing diagrams for these are shown below:

6.3.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts)

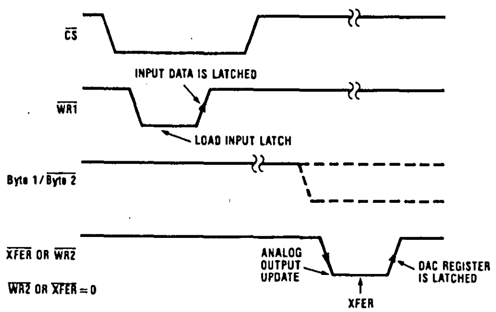


DAC1006/1007/1008 (20-Pin Parts)

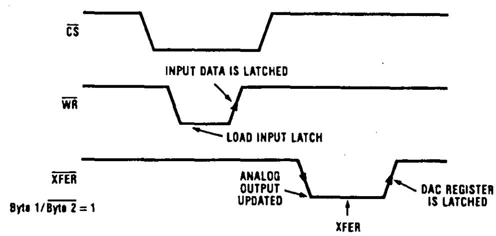


6.3.2 Double Buffered

DAC 1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)



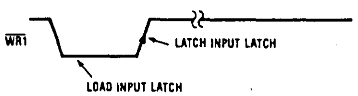
TL/H/5688-22

6.4 Stand Alone Operation

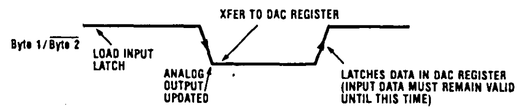
For applications for a DAC which are not under μP control (stand alone) there are two basic operating modes, single buffered and double buffered. The timing diagrams for these are shown below:

6.4.1 Single Buffered

DAC1000/1001/1002 (24-Pin Parts)

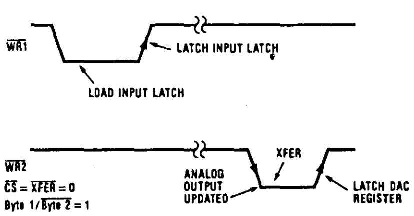


DAC1006/1007/1008 (20-Pin Parts)

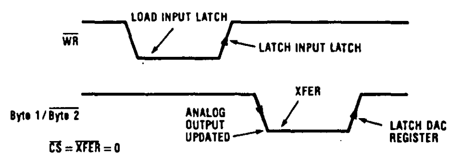


6.4.2 Double Buffered

DAC1000/1001/1002 (24-Pin Parts)



DAC1006/1007/1008 (20-Pin Parts)*



TL/H/5688-23

*For a connection diagram of this operating mode use *Figure 18* for the Logic and *Figure 20* for the Data Input connections.

6.4.3 Flow Through

This operating mode causes the 10-bit input word to directly create the DAC output without any latching involved.

DAC1000/1001/1002 (24-Pin Parts)

$\overline{WR1} = \overline{WR2} = \overline{CS} = \overline{XFER} = 0$

Byte 1/$\overline{\text{Byte 2}} = 1$

7.0 MICROPROCESSOR INTERFACE

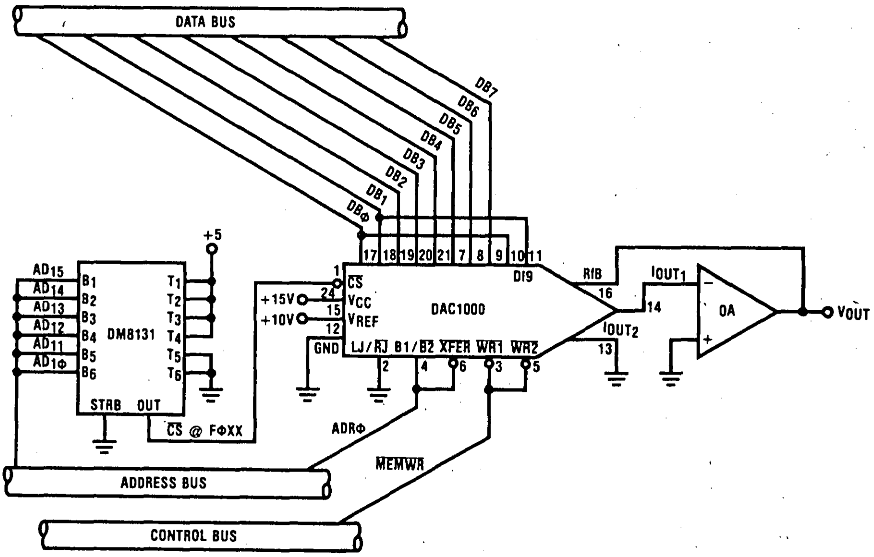
The logic functions of the DAC1000 family have been oriented towards an ease of interface with all popular μPs. The following sections discuss in detail a few useful interface schemes.

7.1 DAC1001/1/2 to INS8080A Interface

Figure 21 illustrates the simplicity of interfacing the DAC1000 to an INS8080A based microprocessor system.

The circuit will perform an automatic transfer of the 10 bits of output data from the CPU to the DAC register as outlined in Section 6.2.1, "Controlling Data Transfer for an 8-Bit Data Bus."

Since a double byte write is necessary to control the DAC with the INS8080A, a possible instruction to achieve this is a PUSH of a register pair onto a "stack" in memory. The 16-bit register pair word will contain the 10 bits of the eventual DAC input data in the proper sequence to conform to both



TL/H/5688-24

NOTE: DOUBLE BYTE STORES CAN BE USED.
e.g. THE INSTRUCTION SHLD FΦΦ1 STORES THE L REG INTO B1 AND THE H REG INTO B2 AND TRANSFERS THE RESULT TO THE DAC REGISTER. THE OPERAND OF THE SHLD INSTRUCTION MUST BE AN ODD ADDRESS FOR PROPER TRANSFER.

FIGURE 21. Interfacing the DAC1000 to the INS8080A CPU Group

the requirements of the DAC (with regard to right or left justified data) and the implementation of the PUSH instruction which will output the higher order byte of the register pair (i.e., register B of the BC pair) first. The DAC will actually appear as a two-byte "stack" in memory to the CPU. The auto-decrementing of the stack pointer during a PUSH allows using address bit 0 of the stack pointer as the Byte1/$\overline{\text{Byte2}}$ and $\overline{\text{XFER}}$ strobes if bit 0 of the stack pointer address −1, (SP−1), is a "1" as presented to the DAC. Additional address decoding by the DM8131 will generate a unique DAC chip select (CS) and synchronize this CS to the two memory write strobes of the PUSH instruction.

To reset the stack pointer so new data may be output to the same DAC, a POP instruction followed by instructions to insure that proper data is in the DAC data register pair before it is "PUSHED" to the DAC should be executed, as the POP instruction will arbitrarily alter the contents of a register pair.

Another double byte write instruction is Store H and L Direct (SHLD), where the HL register pair would temporarily contain the DAC data and the two sequential addresses for the DAC are specified by the instruction op code. The auto incrementing of the DAC address by the SHLD instruction permits the same simple scheme of using address bit 0 to generate the byte number and transfer strobes.

7.2 DAC1000 to MC6820/1 PIA Interface

In *Figure 22* the DAC1000 is interfaced to an M6800 system through an MC6820/1 Peripheral Interface Adapter (PIA). In this case the CS pin of the DAC is grounded since the PIA is already mapped in the 6800 system memory space and no decoding is necessary. Furthermore, by using both Ports A and B of the PIA the 10-bit data transfer, assumed right justified again in two 8-bit bytes, is greatly simplified. The HIGH byte is loaded into Output Register A (ORA) of the PIA, and the LOW byte is loaded into ORB. The 10-bit data transfer to the DAC and the corresponding analog output change occur simultaneously upon CB2 going LOW under program control. The 10-bit data word in the DAC register will be latched (and hence V_{OUT} will be fixed) when CB2 is brought back HIGH.

If both output ports of the PIA are not available, it is possible to interface the DAC1000 through a single port without much effort. However, additional logic at the CB2(or CA2) lines or access to some of the 6800 system control lines will be required.

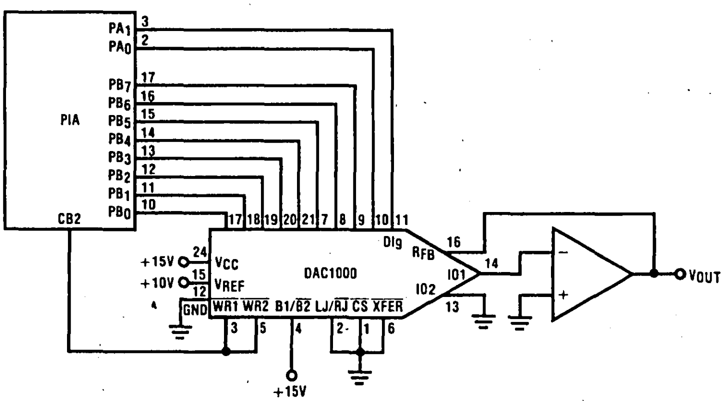
7.3 Noise Considerations

A typical digital/microprocessor bus environment is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and can cause noise spikes to appear at the DAC output. These noise spikes occur when the data bus changes state or when data is transferred between the latches of the device.

In low frequency or DC applications, low pass filtering can reduce these noise spikes. This is accomplished by overcompensating the DAC output amplifier by increasing the value of the feedback capacitor (C_C in *Figure 3*).

In applications requiring a fast transient response from the DAC and op amp, filtering may not be feasible. Adding a latch, DM74LS374, as shown in *Figure 23* isolates the device from the data bus, thus eliminating noise spikes that occur every time the data bus changes state. Another method for eliminating noise spikes is to add a sample and hold after the DAC op amp. This also has the advantage of eliminating noise spikes when changing digital codes.

6



TL/H/5688-25

FIGURE 22. DAC1000 to MC6820/1 PIA Interface

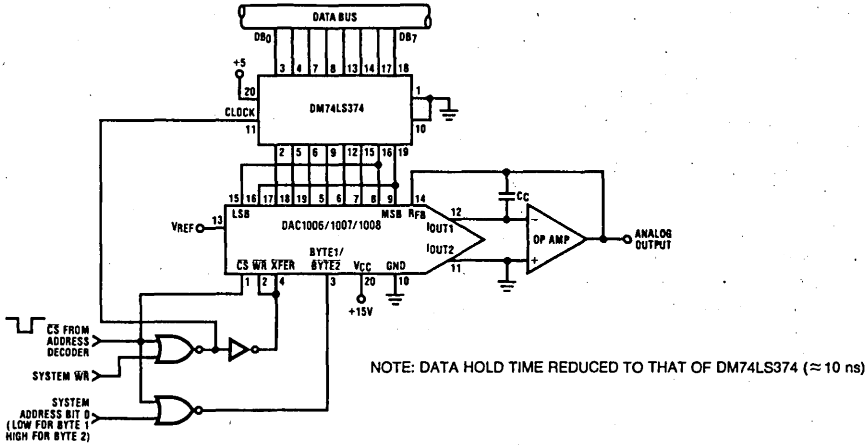
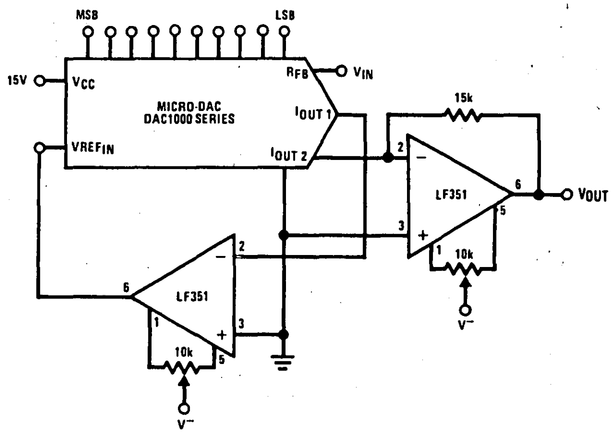


FIGURE 23. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling



TL/H/5688-26

FIGURE 24. Digitally Controlled Amplifier/Attenuator

7.4 Digitally Controlled Amplifier/Attenuator

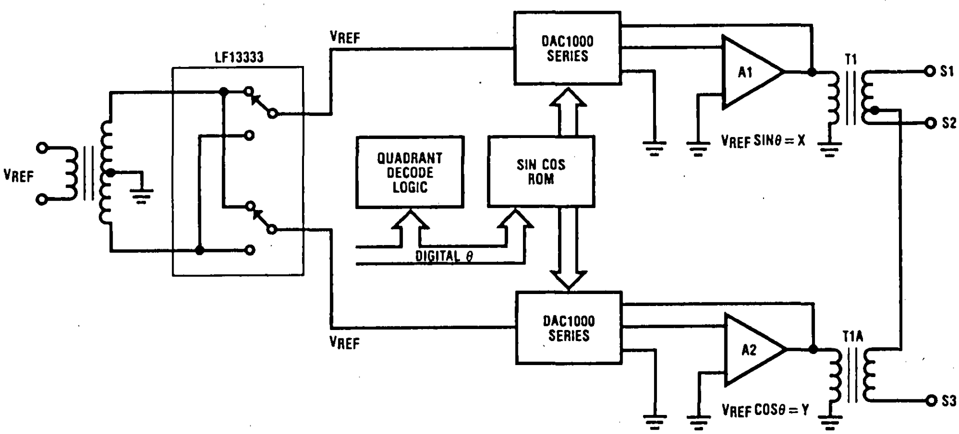
An unusual application of the DAC, *Figure 24*, applies the input voltage via the on-chip feedback resistor. The lower op amp automatically adjusts the $V_{REF\ IN}$ voltage such that I_{OUT1} is equal to the input current (V_{IN}/Rf_B). The magnitude of this $V_{REF\ IN}$ voltage depends on the digital word which is in the DAC register. I_{OUT2} then depends upon both the magnitude of V_{IN} and the digital word. The second op amp converts I_{OUT2} to a voltage, V_{OUT}, which is given by:

$$V_{OUT}=V_{IN}\left(\frac{1023-N}{N}\right), \text{ where } 0<N\leq 1023.$$

Note that $N=0$ (or a digital code of all zeros) is not allowed or this will cause the output amplifier to saturate at either $\pm V_{MAX}$, depending on the sign of V_{IN}.

To provide a digitally controlled divider, the output op amp can be eliminated. Ground the I_{OUT2} pin of the DAC and V_{OUT} is now taken from the lower op amp (which also drives the V_{REF} input of the DAC). The expression for V_{OUT} is now given by

$$V_{OUT}=-\frac{V_{IN}}{M}$$ where $M=$ Digital input (expressed as a fractional binary number). $0<M<1$.



TL/H/5688-27

FIGURE 25. Digital to Synchro Converter

Ordering Information

1. All Logic Features — 24-pin package.

Accuracy	Temperature Range −40°C to +85°C	−55°C to +125°C	0° to +70°C
0.05% (10-bit)	DAC1000LCD	DAC1000LD	DAC 1000LCN
0.10% (9-bit)	DAC1001LCD	DAC1001LD	DAC1001LCN
0.20% (8-bit)	DAC1002LCD	DAC1002LD	DAC1002LCN
Package Outline	D24C	D24C	N24A

2. For Left Justified Data — 20-pin package.(See package outline D20C).

Accuracy	Temperature Range −40°C to +85°C	−55°C to +125°C	0° to +70°C
0.05% (10-bit)	DAC1006LCD	DAC1006LD	DAC1006LCN
0.10% (9-bit)	DAC1007LCD	DAC1007LD	DAC1007LCN
0.20% (8-bit)	DAC1008LCD	DAC1008LD	DAC1008LCN
Package Outline	D20A	D20A	N20A

National Semiconductor

DAC1020, DAC1021, DAC1022 10-Bit Binary Multiplying D/A converter DAC1220, DAC1221, DAC1222 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

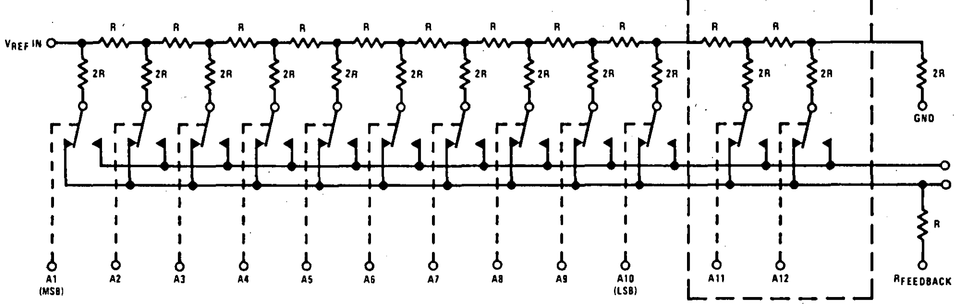
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guaranteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220, DAC1221 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq 25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—½ LSB @100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



TL/H/5689-1

Ordering Information

10-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C		−40°C to +85°C		−55°C to +125°C	
ACCURACY	0.05%	DAC1020LCN	AD7520LN,AD7530LN	DAC1020LCD	AD7520LD,AD7530LD	DAC1020LD	AD7520UD
	0.10%	DAC1021LCN	AD7520KN,AD7530KN	DAC1021LCD	AD7520KD,AD7530KD	DAC1021LD	AD7520TD
	0.20%	DAC1022LCN	AD7520JN,AD7530JN	DAC1022LCD	AD7520JD,AD7530JD	DAC1022LD	AD7520SD
PACKAGE OUTLINE		N16A		D16C		D16C	

12-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C		−40°C to +85°C		−55°C to +125°C	
ACCURACY	0.05%	DAC1220LCN	AD7521LN,AD7531LN	DAC1220LCD	AD7521LD,AD7531LD	DAC1220LD	AD7521UD
	0.10%	DAC1221LCN	AD7521KN,AD7531KN	DAC1221LCD	AD7521KD,AD7531KD	DAC1221LD	AD7521TD
	0.20%	DAC1222LCN	AD7521JN,AD7531JN	DAC1222LCD	AD7521JD,AD7531JD	DAC1222LD	AD7521SD
PACKAGE OUTLINE		N18A		D18A		D18A	

Note. Devices may be ordered by either part number.

Absolute Maximum Ratings

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Temperature (T_A)			
DAC1020LD, DAC1021LD,	−55	+125	°C
DAC1022LD, DAC1220LD,	−55	+125	°C
DAC1221LD, DAC1222LD,	−55	+125	°C
DAC1020LCD, DAC1021LCD,	−40	+85	°C
DAC1022LCD, DAC1220LCD,	−40	+85	°C
DAC1221LCD, DAC1222LCD	−40	+85	°C
DAC1020LCN, DAC1021LCN	0	+70	°C
DAC1022LCN, DAC1220LCN	0	+70	°C
DAC1221LCN, DAC1222LCN	0	+70	°C

Electrical Characteristics (V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1221, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		10			12			Bits
Linearity Error	$T_{MIN}<T_A<T_{MAX}$, $-10V<V_{REF}<+10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FSR
9-Bit Parts	DAC1021, DAC1221			0.10			0.10	% FSR
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3	1.0		0.3	1.0	% FS
Full-Scale Error Tempco	$T_{MIN}<T_A<T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$							
$I_{OUT\,1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\,2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$, (Note 2), *(Figure 2)*		0.005	0.005		0.005	0.005	% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99. 95% FS All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, V_{REF} = 20 Vp-p @ 100 kHz			10			10	mVp-p
	D Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
$I_{OUT\,1}$	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
$I_{OUT\,2}$	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN}<T_A<T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN}<T_A<T_{MAX}$	2.4			2.4			V

Electrical Characteristics (Continued)

(V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1221, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Digital Input Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: V_{REF} = ±10V and V_{REF} = ±1V. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3*.

Note 3: Both $I_{OUT\,1}$ and $I_{OUT\,2}$ must go to ground or the virtual ground of an operational amplifier. If V_{REF} = 10V, every millivolt offset between $I_{OUT\,1}$ or $I_{OUT\,2}$, 0.005% linearity error will be introduced.

Note 4: To achieve this low feedthrough in the D package, the user must ground the metal lid.

Typical Performance Characteristics

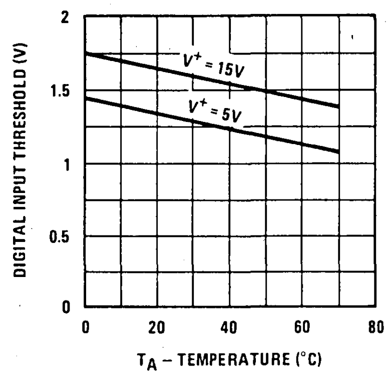
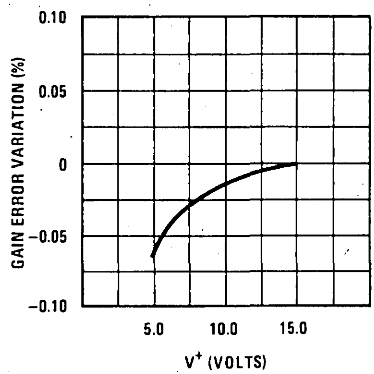


FIGURE 1. Digital Input Threshold vs Ambient Temperature



TL/H/5689-2

FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current (*Figure 3*)

The op amp bias current, I_b, flows through the 15k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 15k × I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It is therefore recommended to adjust the op amp V_{OS}. R_{OUT} is ~15k if more than 4 digital inputs are high; R_{OUT} is ~45k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust (*Figure 3*)

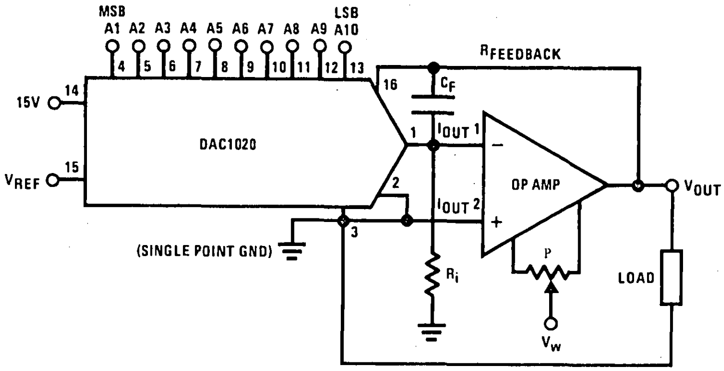
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within ±1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust (*Figure 4*)

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $\|V_{OUT}\|$ to a voltage equal to V_{REF} × 1023/1024.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

Op Amp Family	C_F	R_i	P	V_W	Circuit Settling Time, t_s	Circuit Small Signal BW
LM357	10 pF	2.4k	25k	V+	1.5 μs	1M
LM356	22 pF	∞	25k	V+	3 μs	0.5M
LF351	24 pF	∞	10k	V−	4 μs	0.5M
LM741	0	∞	10k	−	40 μs	200 kHz



TL/H/5689-3

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \bullet\bullet\bullet \frac{A10}{1024}\right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

where A_N = 1 if the A_N digital input is high

A_N = 0 if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

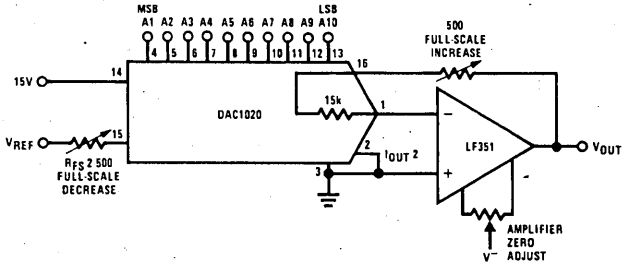


FIGURE 4: Full-Scale Adjust

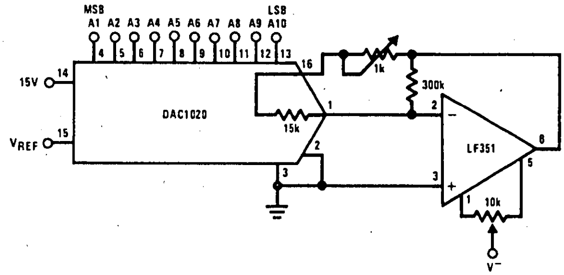
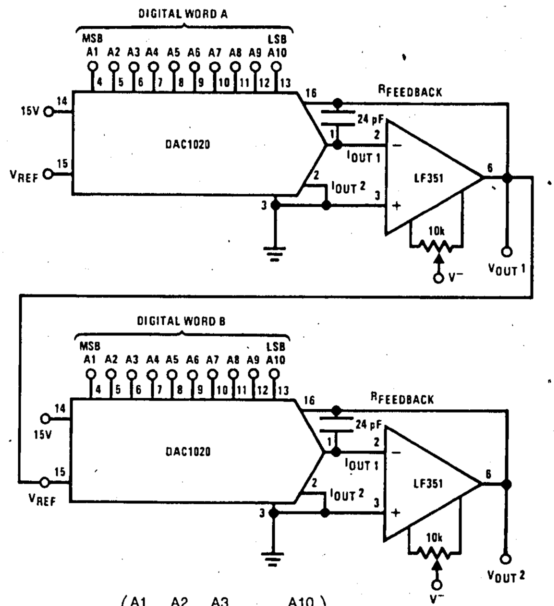


FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)



TL/H/5689–4

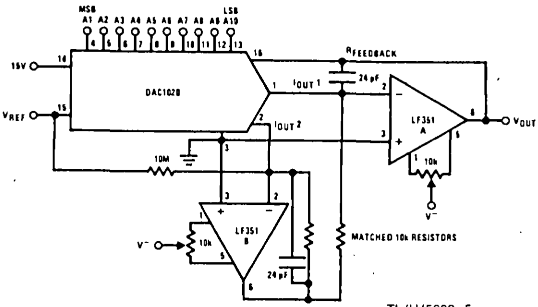
$$V_{OUT\,1} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$V_{OUT2} = V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right) \times \left(\frac{B1}{2} + \frac{B2}{4} + \frac{B3}{8} + \cdots \frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

Typical Applications (Continued)



TL/H/5689-5

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \cdots + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: AN = +1 if A_N input is high

AN = −1 if A_N input is low

COMPLEMENTARY OFFSET BINARY (BIPOLAR) OPERATION

DIGITAL INPUT										V_{OUT}
0	0	0	0	0	0	0	0	0	0	$+V_{REF}$
0	0	0	0	0	0	0	0	0	1	$V_{REF} \times 1022/1024$
0	1	1	1	1	1	1	1	1	1	$V_{REF} \times 2/1024$
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	$-V_{REF} \times 2/1024$
1	1	1	1	1	1	1	1	1	1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \frac{V_{REF}}{R_{LADDER}} \times \left(\frac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

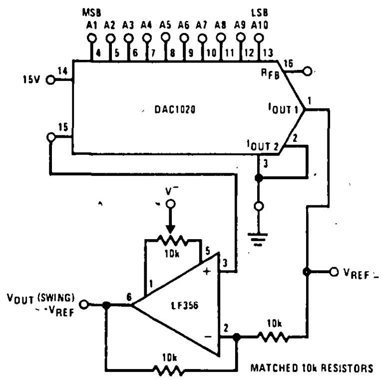
Operational Amplifiers V_{OS} Adjust (*Figure 7*)

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.



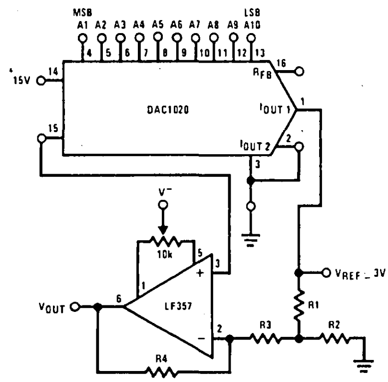
TRUE OFFSET BINARY OPERATION

DIGITAL INPUT										V_{OUT}
1	1	1	1	1	1	1	1	1	1	$V_{REF} \times 1022/1024$
1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	$-V_{REF}$

$t_s = 1.8\ \mu s$

use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp



TL/H/5689-6

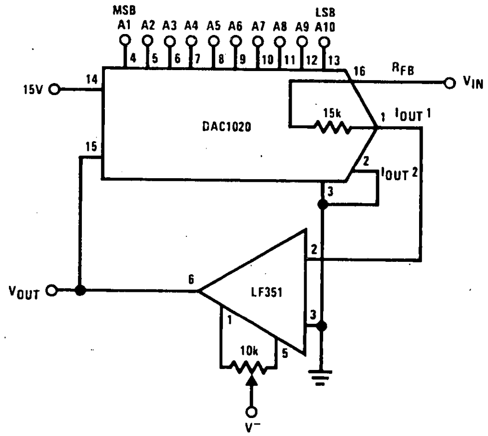
- $R4 = (2A_V^- - 1)\,R, \frac{R2}{R1} = \frac{A_V^-}{A_V^- - 1},$

  $R3 + R1 \| R2 = R;\ A_V^- = \frac{V_{OUT(PEAK)}}{V_{REF}},\ R = 20k$
- Example: $V_{REF} = 2V$, V_{OUT} (swing) ≅ ±10V; $A_V^- = 5V$

  Then R4 = 9R, R1 = 0.8 R2. If R1 = 0.2R then R2 = 0.25R, R3 = 0.64R

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

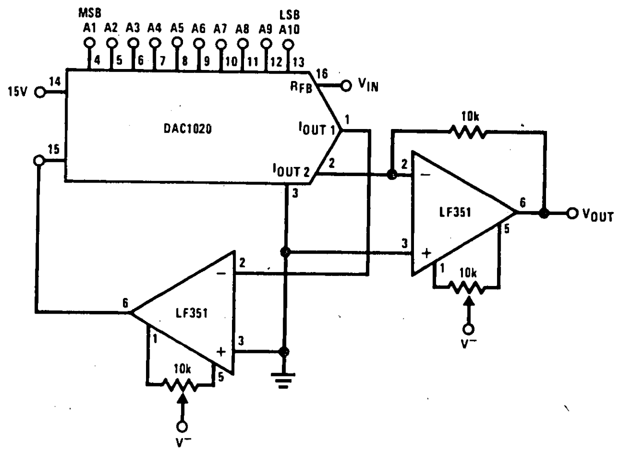


$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)



TL/H/5689-7

$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \ldots + \frac{A10}{1024}}{\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024}}\right] \text{ or } V_{OUT} = V_{REF}\left(\frac{1023 - N}{N}\right)$$

where: $0 \leq N \leq 1023$

$N = 0$ for A_N = all zeros

$N = 1$ for $A10 = 1$, $A1–A9 = 0$

.

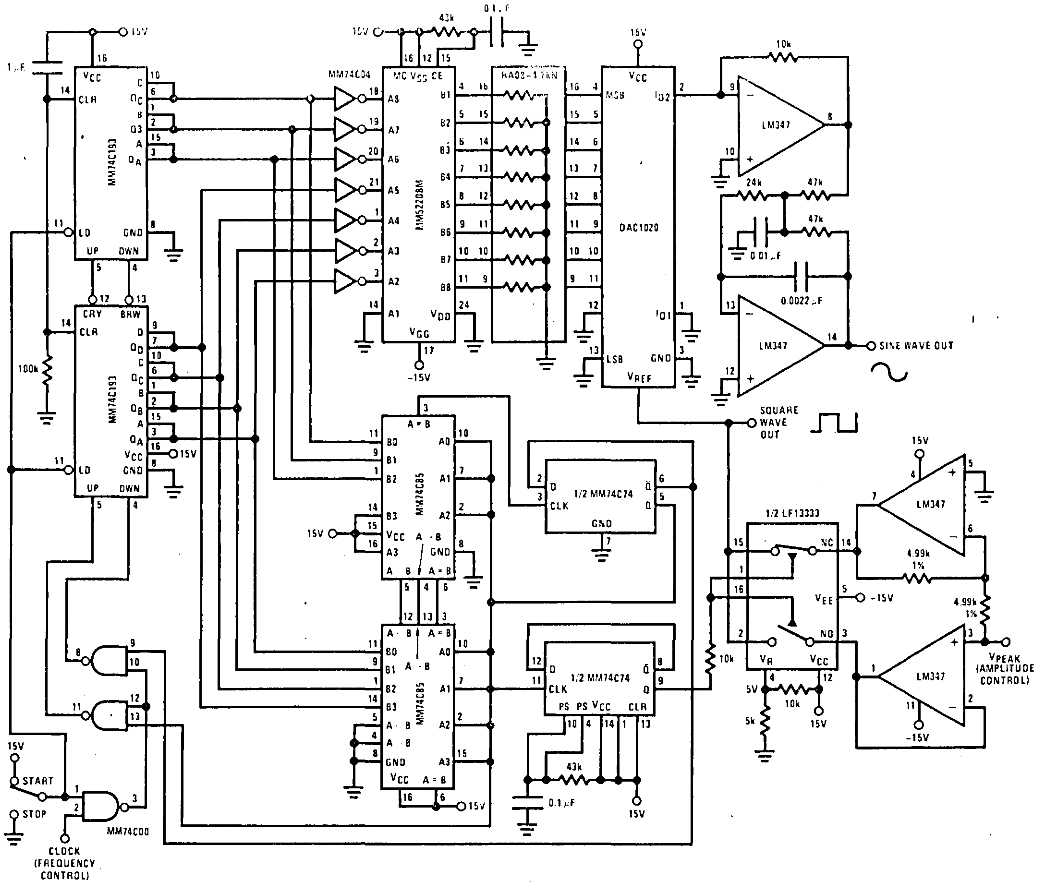
.

.

$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally controlled Amplifier-Attenuator

Typical Applications (Continued)

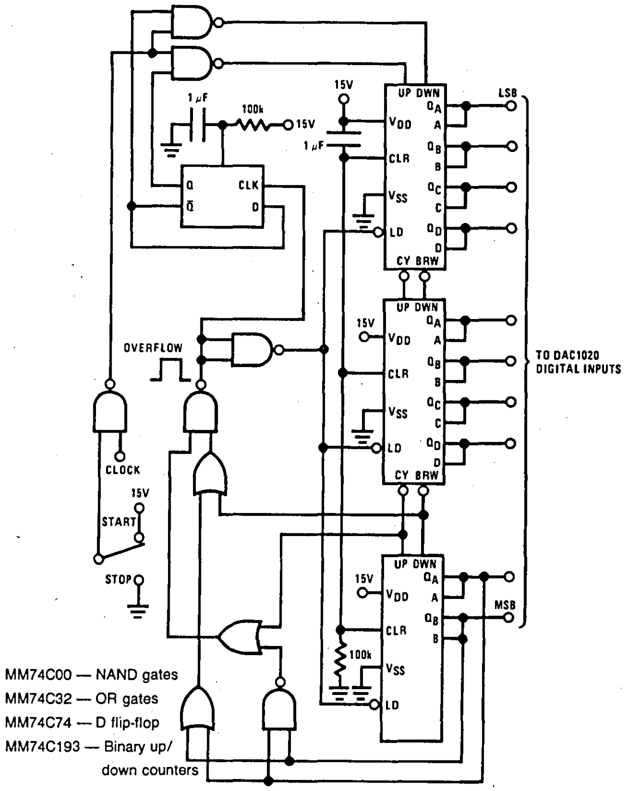


TL/H/5689-8

- Output frequency $= \frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V − 10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)



TL/H/5689-9

- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

Definition of Terms

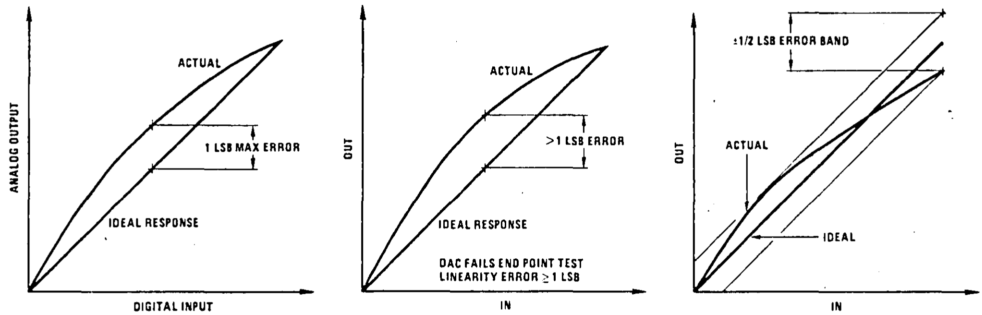
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within $\pm 1/2$ LSB of final output value.

Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V—9.8\ mV = 9.9902V$. Full-scale error is adjustable to zero as shown in *Figure 5*.



TL/H/5689-10

a | b1 | b2

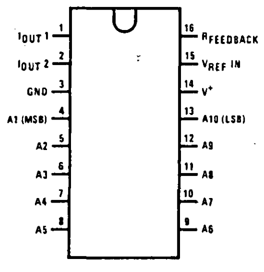
(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the $\pm 1/2$ linearity error specification

Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the $\pm 1/2$ LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

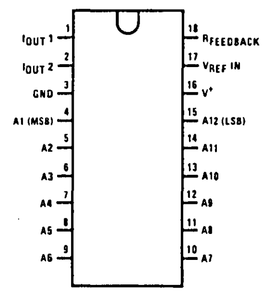
Connection Diagrams

DAC102X
Dual-In-Line Package



TOP VIEW

DAC122X
Dual-In-Line Package



TOP VIEW

TL/H/5689-11

Order Numbers DAC1020, DAC1021, DAC1022, DAC1220, DAC1221, DAC1222
See NS Packages N16A, D16C, N18A, D18A

National Semiconductor

MICRO-DAC™ DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232 12-Bit, µP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

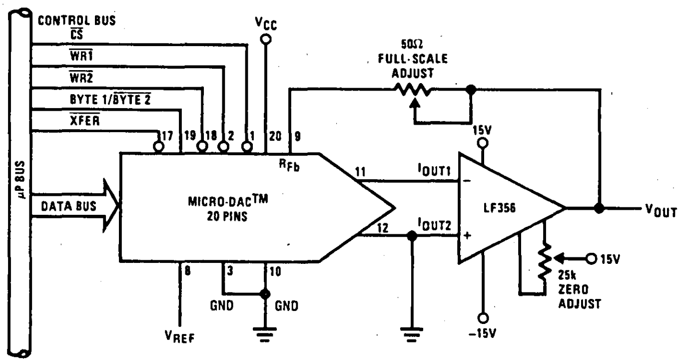
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without µP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

■ Current Settling Time	1 µS
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
■ Gain Tempco	1.5 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



TL/H/5690-1

Ordering Information

Accuracy	Package	
	20-Pin D20A	24-Pin D24C
0.012%	DAC1230LCD	DAC1208LCD
0.024%	DAC1231LCD	DAC1209LCD
0.05%	DAC1232LCD	DAC1210LCD

Absolute Maximum Ratings

(Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}

Operating Ratings

Lead Temperature (Soldering, 10 seconds)	300°C
Temperature Range	−40°C to +85°C*
Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

* Military temperature range device will be available in future.

Electrical Characteristics

T_A = 25°C, V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units	Notes
Resolution		12	12	12	Bits	
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted $T_{MIN} < T_A < T_{MAX}$ $-10V \leq V_{REF} \leq 10V$ DAC1208, DAC1230 DAC1209, DAC1231 DAC1210, DAC1232			 0.012 0.024 0.05	 % of FSR % of FSR % of FSR	4, 7 6 5
Differential Non-Linearity	Zero and Full-Scale Adjusted $T_{MIN} < T_A < T_{MAX}$ $-10V \leq V_{REF} \leq 10V$ DAC1208, DAC1230 DAC1209, DAC1231 DAC1210, DAC1232			 0.012 0.024 0.05	 % of FSR % of FSR % of FSR	4, 7 6 5
Monotonicity	$T_{MIN} < T_A < T_{MAX}$ $-10V \leq V_{REF} \leq 10V$	12	12	12	Bits	4, 6 5
Gain Error	Using Internal R_{Fb} $-10V \leq V_{REF} \leq 10V$	−0.2	−0.01	0.0	% of FS	5
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$ Using Internal R_{Fb}		±1.3	±6.0	ppm of FS/°C	6, 7 10
Power Supply Rejection	All Digital Inputs Latched High		±3.0		ppm of FSR/V	7
Reference Input Resistance		10	15	20	kΩ	
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All Data Inputs Latched Low		3		mVp-p	9
Output Capacitance	All Data Inputs Latched High I_{OUT1} All Data Inputs Latched High I_{OUT2} All Data Inputs Latched Low I_{OUT1} All Data Inputs Latched Low I_{OUT2}		200 70 70 200		pF pF pF pF	
Supply Current Drain	$T_{MIN} \leq T_A \leq T_{MAX}$		1.2	2.0	mA	6
Output Leakage Current I_{OUT1} I_{OUT2}	$T_{MIN} \leq T_A \leq T_{MAX}$ All Data Inputs Latched Low All Data Inputs Latched High			 15 15	 nA nA	6, 11 6, 11
Digital Input Threshold	$T_{MIN} \leq T_A \leq T_{MAX}$ Low Threshold High Threshold	 2.0		 0.8	 V_{DC} V_{DC}	6
Digital Input Currents	$T_{MIN} \leq T_A \leq T_{MAX}$ Digital Inputs <0.8V Digital Inputs >2.0V		 −50 0.1	 −200 10	 μA_{DC} μA_{DC}	6

Electrical Characteristics (Continued)

T_A = 25°C, V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted.

	Parameter	Conditions	Min	Typ	Max	Units	Notes
t_S	Full-Scale Current Settling Time	R_L = 100Ω, Output Settled to 0.01% $\overline{CS}$ = $\overline{WR1}$ = $\overline{WR2}$ = $\overline{XFER}$ = 0V, Byte 1/Byte 2 = 5V, DI_0 through DI_{11} Switched Simultaneously		1		μS	
t_W	Write and $\overline{XFER}$ Pulse Width	V_{IL} = 0V, V_{IH} = 5V	320	50		ns	8, 10
		$T_{MIN} \le T_A \le T_{MAX}$	320	80	—	ns	6, 8, 10
t_{DS}	Data Set-Up Time	V_{IL} = 0V, V_{IH} = 5V	320	70		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	320	80	—	ns	6, 10
t_{DH}	Data Hold Time	V_{IL} = 0V, V_{IH} = 5V	90	50		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	90	60		ns	6, 10
t_{CS}	Control Set-Up Time	V_{IL} = 0V, V_{IH} = 5V	320	60	—	ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	320	100	—	ns	6, 10
t_{CH}	Control Hold Time	V_{IL} = 0V, V_{IH} = 5V	10	0		ns	10
		$T_{MIN} \le T_A \le T_{MAX}$	10	0	—	ns	6, 10

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "Absolute Maximum" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at V_{REF} = ±10 V_{DC} and V_{REF} = ±1 V_{DC}.

Note 6: T_{MIN} = −40°C and T_{MAX} = 85°C.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR(parts per million of full-scale range) and ppm of FS(parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of ±(6)($V_{REF}/10^6$)(125°C) or ±0.75 (10^{-3}) V_{REF} which is ±0.075% of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

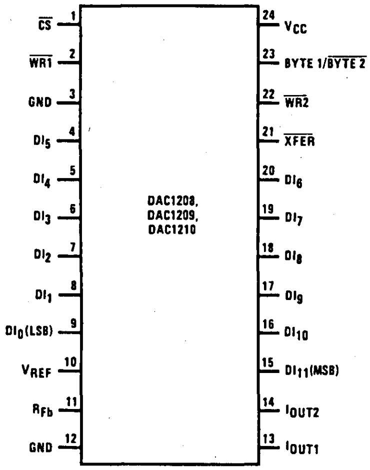
Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

Note 11: An 10 nA leakage current with R_{Fb} = 20k and V_{REF} = 10V corresponds to a zero error of $(10\times10^{-9}\times20\times10^3)\times100\%$ 10V or 0.002% of FS.

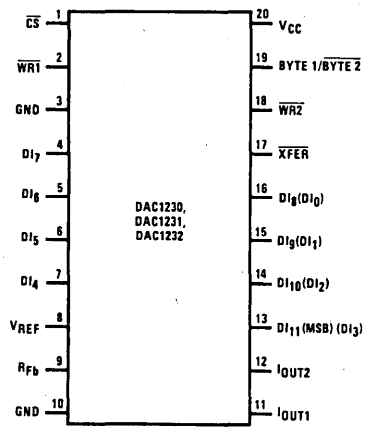
Connection Diagrams

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package

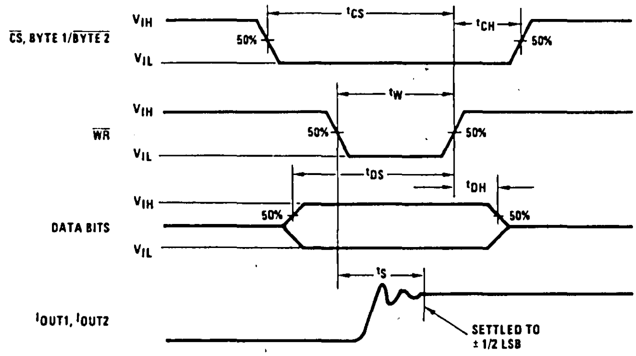


TOP VIEW

See Ordering Information

TL/H/5690-2

Switching Waveforms



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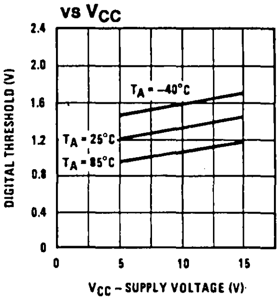
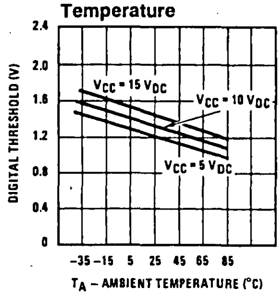
Typical Performance Characteristics

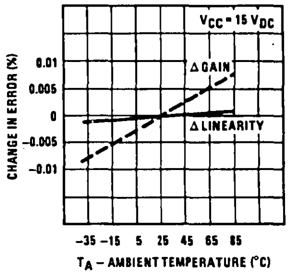
Digital Input Threshold vs V_{CC}



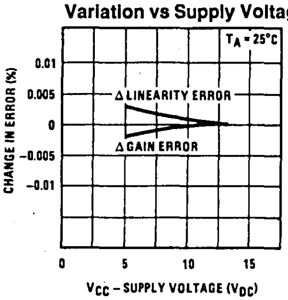
Digital Input Threshold vs Temperature



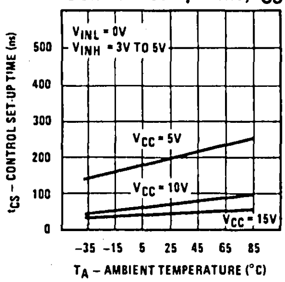
Gain and Linearity Error Variation vs Temperature



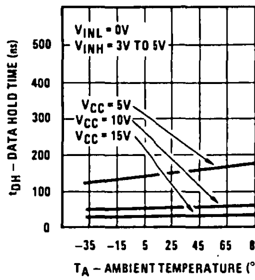
Gain and Linearity Error Variation vs Supply Voltage



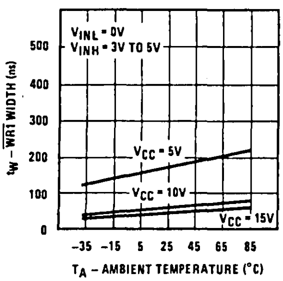
Control Set-Up Time, t_{CS}



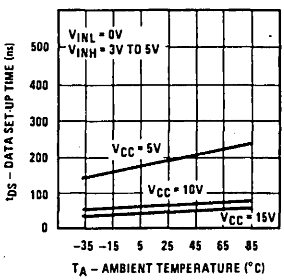
Data Hold Time, t_{DH}



Write Pulse Width, t_W



Data Set-Up Time, t_{DS}



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Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated)

$\overline{\text{CS}}$: Chip Select (active low). The $\overline{\text{CS}}$ will enable $\overline{\text{WR1}}$.

$\overline{\text{WR1}}$: Write 1. The active low $\overline{\text{WR1}}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{\text{WR1}}$ is high. The 12-bit input latch is split into two latches, one holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{\text{Byte 2}}$ control pin is used to select both latches when Byte 1/$\overline{\text{Byte 2}}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{\text{Byte 2}}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{\text{WR2}}$: Write 2 (active low). The $\overline{\text{WR2}}$ will enable $\overline{\text{XFER}}$.

$\overline{\text{XFER}}$: Transfer Control Signal (active low). This signal, in combination with $\overline{\text{WR2}}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Pin 12 voltage of the DAC1208, DAC1209, DAC1210 and Pin 10 voltage of the DAC1230, DAC1231, DAC1232 must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications. Any difference of potential (V_{OS} on these pins) will result in a linearity change of

$$\frac{V_{OS}}{3\ V_{REF}}$$

For example, if $V_{REF} = 10V$ and these ground pins are 9 mV offset from I_{OUT1} and I_{OUT2} the linearity change will be 0.03%.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

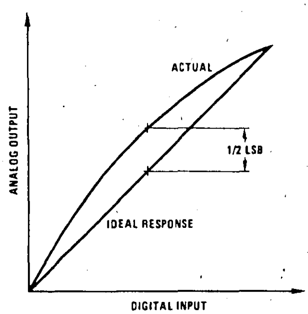
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ±½ LSB of the final output value.

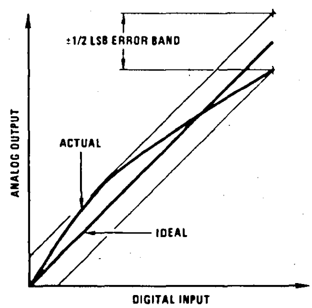
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust



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b) Shifting FS adjust to pass best straight line test

Application Hints

1.0 DIGITAL INTERFACE

These DACs are designed to provide all of the necessary digital input circuitry to permit a direct interface to a wide variety of microprocessor systems. The timing and logic level convention of the input control signals allow the DACs to be treated as a typical memory device or I/O peripheral with no external logic required in most systems. Essentially these DACs can be mapped as a two-byte stack in memory (or I/O space) to receive their 12 bits of input data in two successive 8-bit data writing sequences. The DAC1230 series is intended for use in systems with an 8-bit data bus. The DAC1208 series provides all 12 digital input lines which can be externally configured to be controlled from an 8-bit bus or can be driven directly from a 16-bit data bus.

All of the digital inputs to these DACs contain a unique threshold regulator circuit to maintain TTL voltage level compatibility independent of the applied V_{CC} to the DAC. Any input can also be driven from higher voltage CMOS logic levels in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. As a trouble-shooting aid, if any of the digital inputs are inadvertently left floating, the DAC will interpret the pin as a logic "1".

Double buffered digital inputs allow the DAC to internally format the 12-bit word used to set the current switching R-2R ladder network (see section 2.0) from two 8-bit data write cycles. *Figures 1* and *2* show the internal data registers and their controlling logic circuitry. The timing diagrams for updating the DAC output are shown in sections 1.1, 1.2 and 1.3 for three possible control modes. The method used depends strictly upon the particular application.

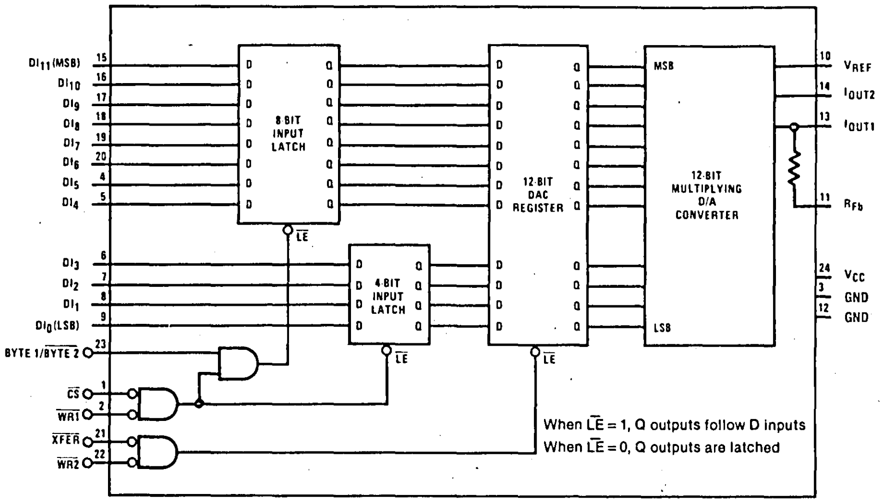

FIGURE 1. DAC1208, DAC1209, DAC1210 Functional Diagram

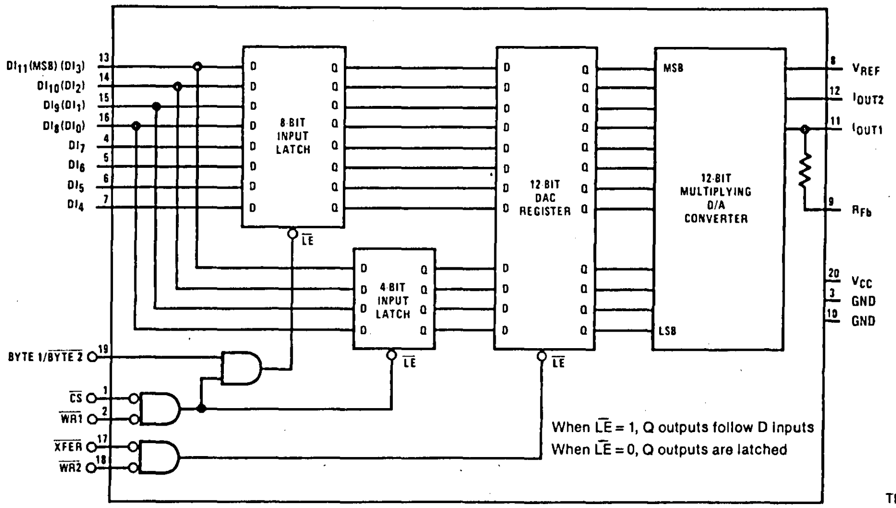

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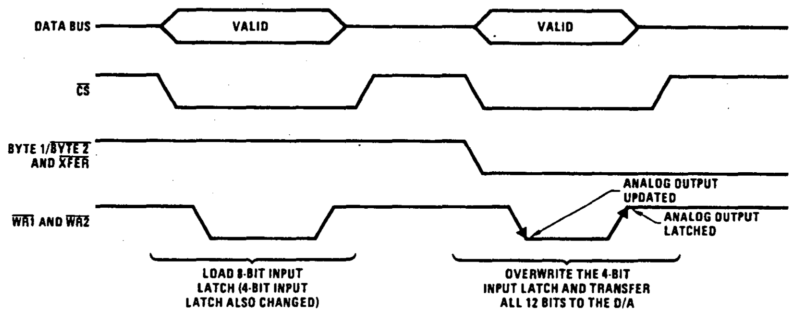
FIGURE 2. DAC1230, DAC1231, DAC1232 Functional Diagram

Application Hints (Continued)

1.1 Automatic Transfer

The 12-bit DAC word is automatically transferred to the DAC register and the R-2R ladder when the second write (the 4 LSBs of the data) occurs.



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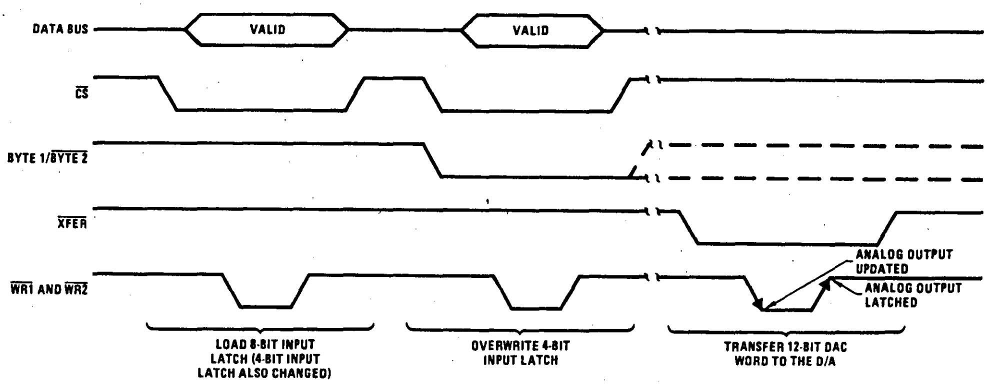
1.2 Independent Processor Transfer Control

In this case a separate address is decoded to provide the $\overline{\text{XFER}}$ signal. This allows the processor to load the next required DAC word but not change the analog output until some time later, most useful for the simultaneous updating of several DACs in a system where their $\overline{\text{XFER}}$ lines would be tied together.



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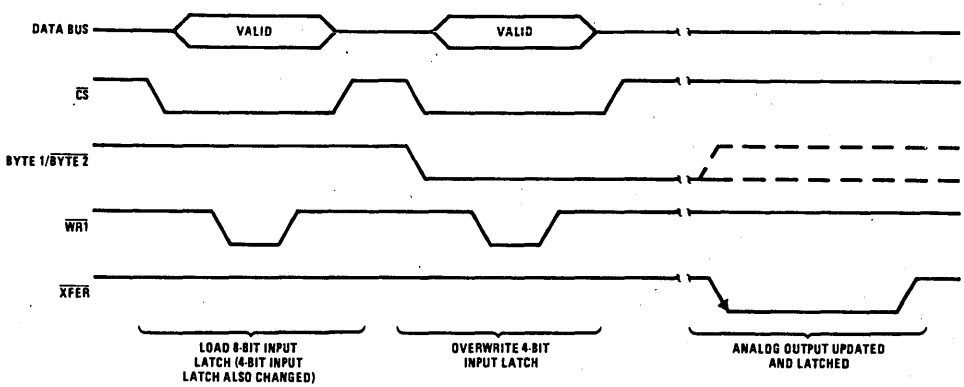
1.3 Transfer via an External Strobe

This method is basically the same as the previous operation except the $\overline{\text{XFER}}$ signal is provided by a device other than the processor. This allows the DAC to hold the code for a conditional analog output signal which will be required on demand from an external monitoring device (an analog voltage comparator for instance).



$\overline{\text{WR2}}$ tied to a logic low (0V)

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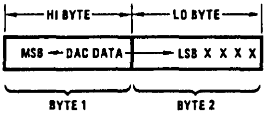
Application Hints (Continued)

1.4 Left-Justified Data Format

It is important to realize that the input registers of these DACs are arranged to accept a left-justified data word from the microprocessor with the most significant 8 bits coming first (Byte 1) and the lower 4 bits second. Left justification simply means that the binary point is assumed to be located to the left of the most significant bit. *Figure 3* shows how the 12 bits of DAC data should be arranged in 2 8-bit registers of an 8-bit processor before being written to the DAC.



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X = don't care

FIGURE 3. Left-Justified Data Format

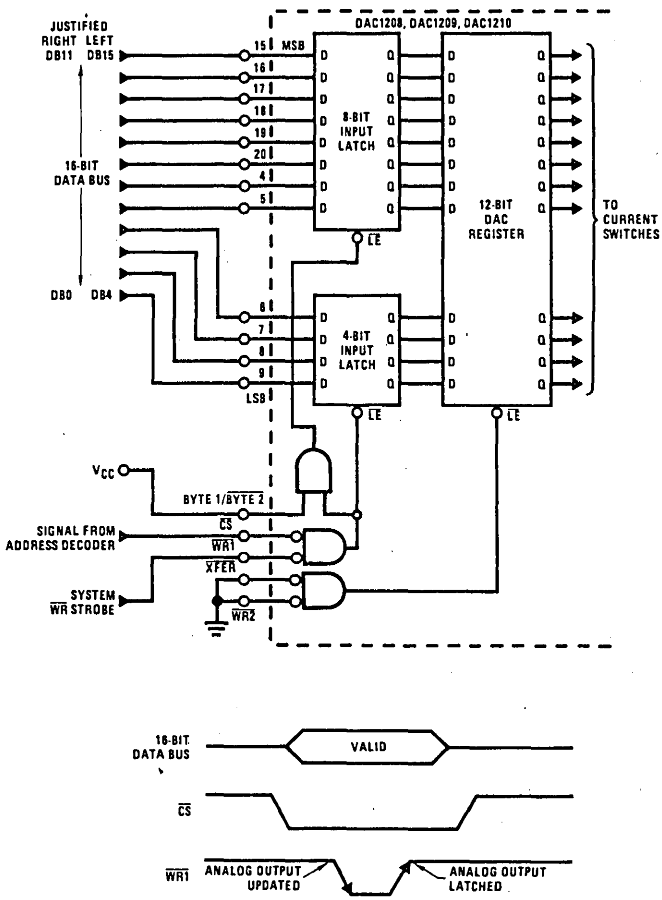
1.5 16-Bit Data Bus Interface

The DAC1208 series provides all 12 digital input lines to permit a direct parallel interface to a 16-bit data bus. In this instance, double buffering is not always necessary (unless a simultaneous updating of several DACs or a data transfer via an external strobe is desired) so the 12-bit DAC register can be wired to flow-through whereby its Q outputs always reflect the state of its D inputs. The external connections required and the timing diagram for this single buffered application are shown in *Figure 4*. Note that either left or right-justified data from the processor can be accommodated with a 16-bit data bus.

1.6 Flow-Through Operation

Through primarily designed to provide microprocessor interface compatibility, the MICRO-DACs can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary updown counter, or in function generation circuits where a ROM is continuously providing DAC data.

Interface Timing



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$\overline{XFER}$ and $\overline{WR2}$ grounded; Byte 1/$\overline{Byte 2}$ tied to V_{CC}.

FIGURE 4. 16-Bit Data Bus Interface for the DAC1208 Series

Application Hints (Continued)

Only the DAC1208, DAC1209, DAC1210 devices can have all 12 inputs flow-through. Simply grounding $\overline{CS}$, $\overline{WR1}$, $\overline{WR2}$ and $\overline{XFER}$ and tying Byte 1/$\overline{\text{Byte 2}}$ high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.7 Address Decoding Tips

It is possible to map the MICRO-DACs into system ROM space to allow more efficient use of existing address decoding hardware. The DAC in effect could share the same addresses of any number of ROM locations. The ROM outputs will only be enabled by a READ of its address (gated by the system READ strobe) and the DAC will only accept data that is written to the same address (gated by the system WRITE strobe).

The Byte 1/$\overline{\text{Byte 2}}$ control function can easily be generated by the processor's least significant address bit (A0) by placing the DAC at two consecutive address locations and utilizing double-byte WRITE instructions which automatically increment or decrement the address. The $\overline{CS}$ and $\overline{XFER}$ signals would then be decoded from the remaining address bits. Care must be taken in selecting the actual address used for Byte 1 of the DAC to prevent a carry (as a result of incrementing the address for Byte 2) from propagating through the address word and changing any of the bits decoded for $\overline{CS}$ or $\overline{XFER}$. *Figure 5* shows how to prevent this effect.

The same problem can occur from a borrow when an auto-decremented address is used; but only if the processor's address outputs are inverted before being decoded.

1.8 Control Signal Timing

When interfacing these MICRO-DACs to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 320 ns for V_{CC} = 11.4V to 15.75V and operation over temperature, but typically a pulse width of only 250 ns is adequate. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulse width. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 6* for an exemplary system which provides a 250 ns $\overline{WR}$ strobe time with a data hold time of only 10 ns.

Write Cycle	Address Bits		
	15 — 2	1*	0**
First (Byte 1)	$\underbrace{\qquad\qquad}$ Decoded to Address DAC	0	1
Second (Byte 2)		1	0

*Starting with a 0 prevents a carry on address incrementing.

**Used as Byte 1/$\overline{\text{Byte2}}$ Control

FIGURE 5

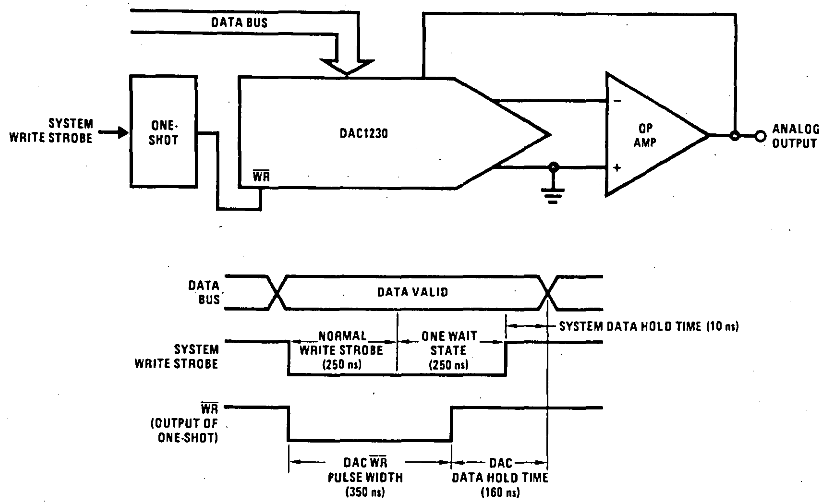

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FIGURE 6. Accommodating a High Speed System

Application Hints (Continued)

The proper data set-up time prior to the latching edge (low to high transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulse width is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.9 Digital Signal Feedthrough

A typical digital/microprocessor is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and may cause fast transients to appear at the DAC output, even when data is latched internally.

In low frequency or DC applications, low pass filtering can reduce the magnitude of any fast transients. This is most easily accomplished by over-compensating the DAC output amplifier by increasing the value of its feedback capacitor.

In applications requiring a fast output response from the DAC and op amp, filtering may not be feasible. In this event, digital signals can be completely isolated from the DAC circuitry, by the use of a DM74LS374 latch, until a valid $\overline{CS}$ signal is applied to update the DAC. This is shown in *Figure 7*.

A single TRI-STATE® data buffer such as the DM81LS95 can be used to isolate any number of DACs in a system. *Figure 8* shows this isolating circuitry and decoding hardware for a multiple DAC analog output card. Pull-up resistors are used on the buffer outputs to limit the impedance at the DAC digital inputs when the card is not selected. A unique feature of this card is that the DAC $\overline{XFER}$ strobes are controlled by the data bus. This allows a very flexible update of any combination of analog outputs via a transfer word which would contain a zero in the bit position assigned to any of the DACs required to change to a new output value.

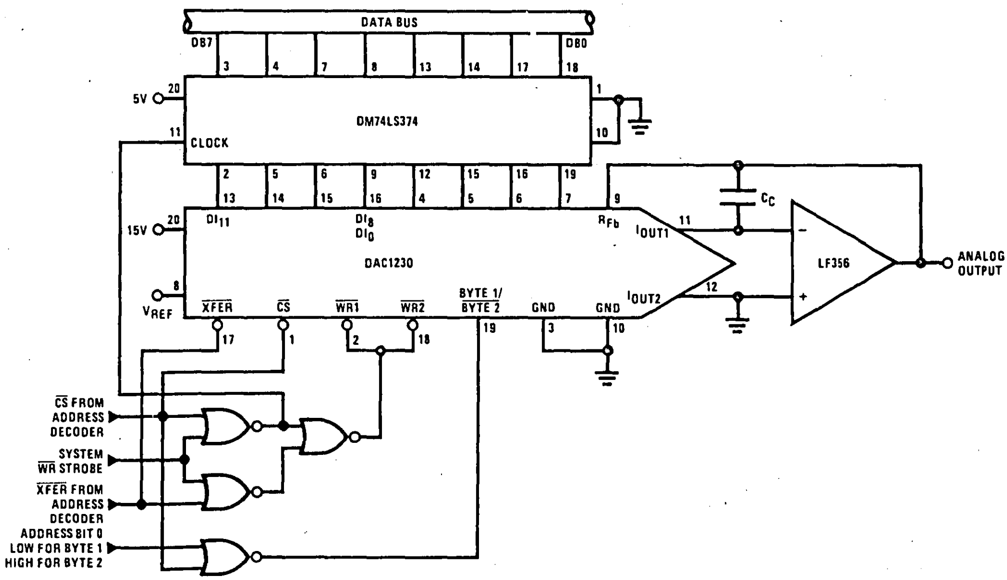

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FIGURE 7. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

Application Hints (Continued)

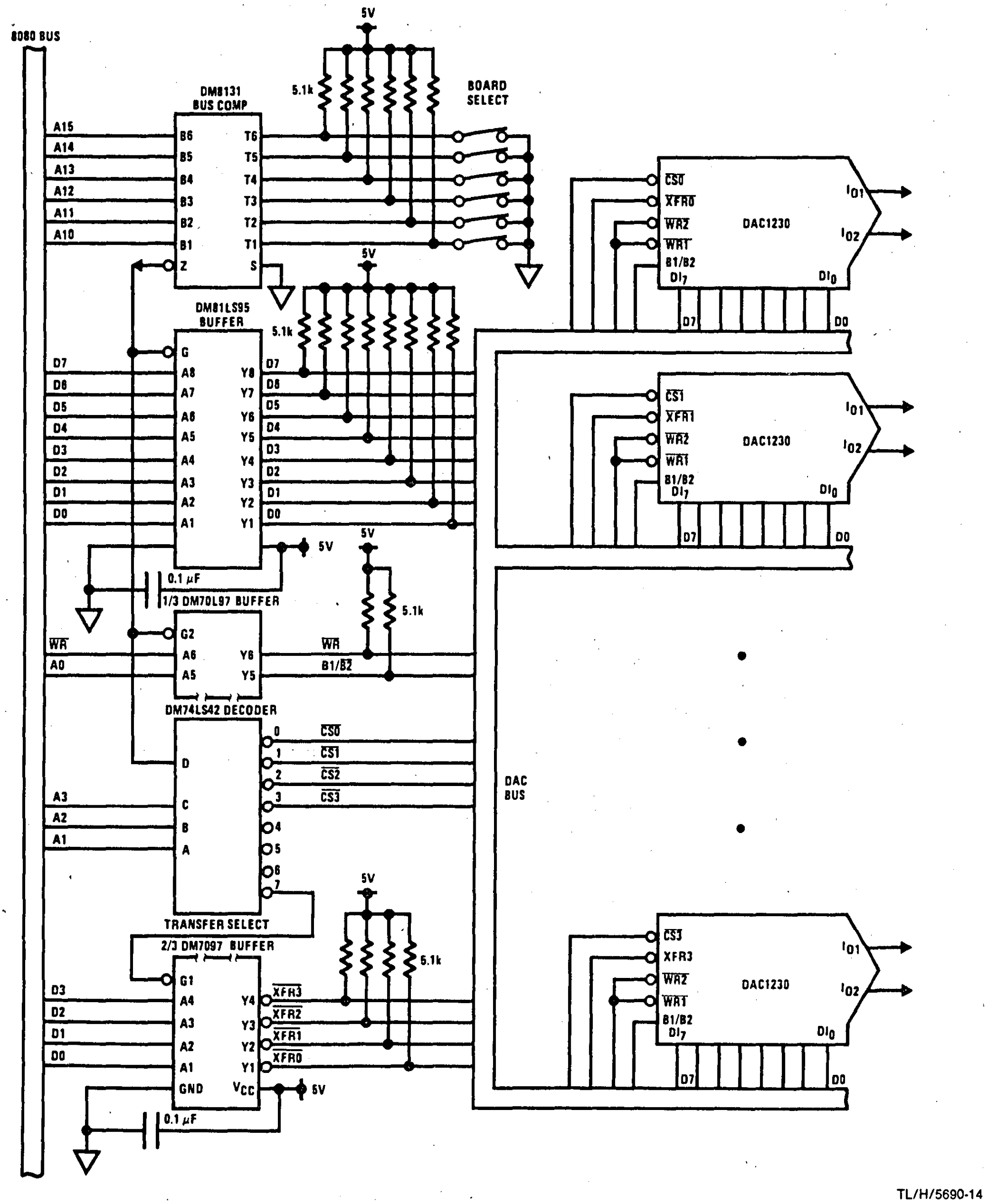


FIGURE 8. TRI-STATE® Buffers Isolate the Data and Control Lines from the DACs. A Transfer Word Provides a Flexible Update.

Application Hints (Continued)

2.0 ANALOG APPLICATIONS

The analog output signal for these DACs is derived from a conventional R-2R current switching ladder network. A detailed description of this network can be found on the DAC1000 series data sheet. Basically, output I_{OUT1} provides a current directly proportional to the product of the applied reference voltage and the digital input word. A second output, I_{OUT2} will be a current proportional to the complement of the digital input. Specifically:

$$I_{OUT1} = \frac{V_{REF}}{15k} \times \frac{D}{4096};$$

$$I_{OUT2} = \frac{V_{REF}}{15k} \times \frac{4095 - D}{4096}$$

where D is the decimal equivalent of the applied 12-bit binary word (ranging from 0 to 4095), V_{REF} is the voltage applied to the V_{REF} terminal and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder.

2.1 Obtaining a Unipolar Output Voltage

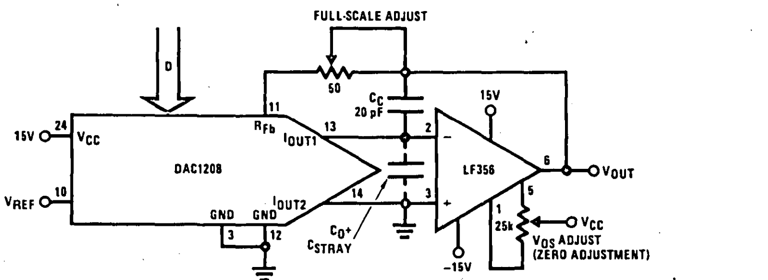
To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential (0 V_{DC}) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 9*.

The inverting input of the op amp is a virtual ground created by the feedback from its output through the internal 15 kΩ resistor, R_{Fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{Fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{Fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{Fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™ op amps are highly recommended for use with these DACs because of their very low input current.



$$V_{OUT} = -(I_{OUT1} \times R_{Fb}) = \frac{-V_{REF}(D)}{4096}$$

for $0 \le D \le 4095$

FIGURE 9. Unipolar Output Configuration

Application Hints (Continued)

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{Fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 9*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

2.1.1 Zero and Full-Scale Adjustments

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

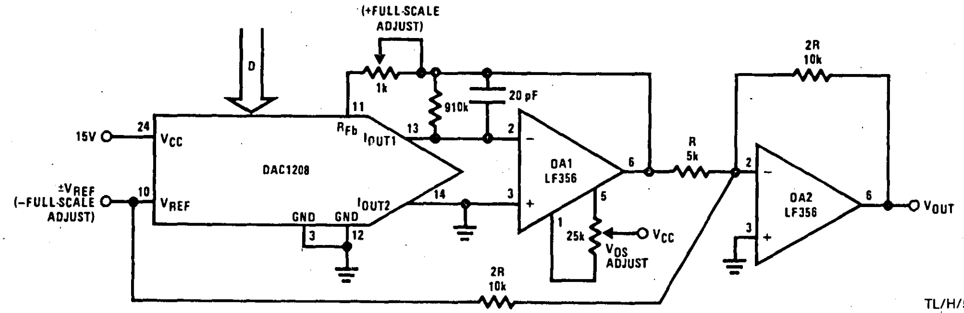
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near 0 V_{DC} as possible. This is accomplished by shorting out R_{Fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The short around R_{Fb} is then removed and the converter is zero adjusted.

A unique feature of this series of DACs is that the full-scale or gain error is guaranteed to be negative. The gain error specification is a measure of how close the value of the internal feedback resistor, R_{Fb}, matches the R-2R ladder resistors. A negative gain error indicates that R_{Fb} is a smaller resistance value than it should be. To adjust this gain error, some resistance must always be added in series with R_{Fb}. The 50Ω potentiometer shown is sufficient to adjust the worst-case gain error for these devices.

2.2 Bipolar Output Voltage from a Fixed Reference

The addition of a second op amp to the unipolar circuit can generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication. This circuit is shown in *Figure 10*.

This configuration features several improvements over existing circuits for a bipolar output shown with other multiplying DACs. Only the offset voltage of amplifier 1 affects the linearity of the DAC. The offset voltage error of the second op amp (although a constant output error) has no effect on linearity. In addition, this configuration offers a non-interactive positive and negative full-scale calibration procedure.



TL/H/5690-16

$$V_{OUT} = V_{REF}\left(\frac{D - 2048}{2048}\right)$$

for $0 \le D \le 4095$

$$1\ LSB = \frac{|V_{REF}|}{2048}$$

Input Code MSB......LSB	Ideal V_{OUT}	
	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1 1 1 1 1	V_{REF} −1 LSB	$-\lvert V_{REF}\rvert$ +1 LSB
1 1 0 0 0 0 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1 1 1 1 1	−1 LSB	+1 LSB
0 0 1 1 1 1 1 1 1 1 1 1	$-\frac{V_{REF}}{2}$ − 1 LSB	$\frac{\lvert V_{REF}\rvert}{2}$ + 1 LSB
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

FIGURE 10. Bipolar Output Voltage Configuration

Application Hints (Continued)

2.2.1 Zero and Full-Scale Adjustments

To calibrate the bipolar output circuit, three adjustments are required. The first step is to set all of the digital input LOW (to force I_{OUT1} to 0) then null the V_{OS} of amplifier 1 by setting the voltage at its inverting input (pin 2) to zero volts. Next, with a code of all zeros still applied, adjust "−full-scale adjust", the reference voltage, for $V_{OUT} = \pm|V_{REF}$ ideal$|$. The polarity of the output voltage at this time will be opposite that of the applied reference. Finally, set all of the digital inputs HIGH and adjust "+full-scale adjust" for

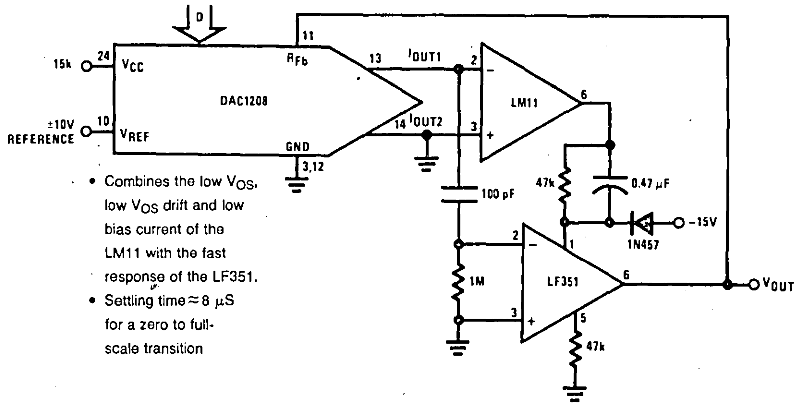
$$V_{OUT} = V_{REF} \frac{2047}{2048}.$$

The polarity of the output will be the same as that of the reference voltage.

3.0 APPLICATION IDEAS

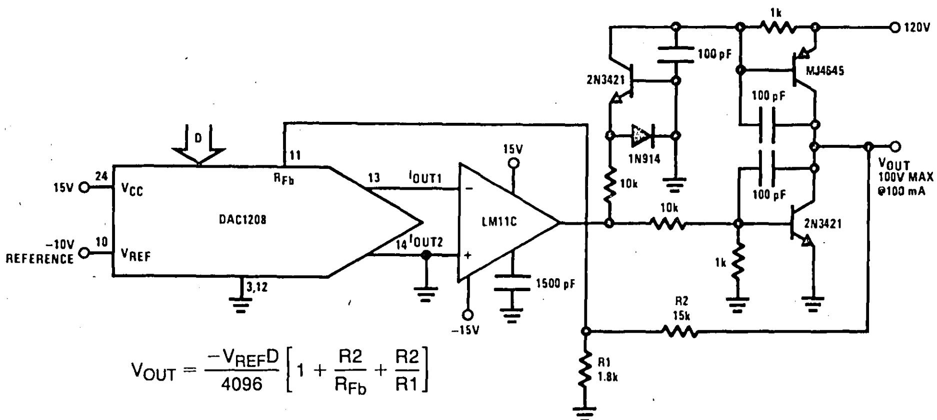
In this section the digital input word is represented by the letter D and is equal to the decimal equivalent of the 12-bit binary input. Hence D can be any integer value between 0 and 4095.

Composite Amplifier for Good DC Characteristics and Fast Output Response



- Combines the low V_{OS}, low V_{OS} drift and low bias current of the LM11 with the fast response of the LF351.
- Settling time ≈ 8 μS for a zero to full-scale transition

High Voltage, Power DAC



$$V_{OUT} = \frac{-V_{REF}D}{4096}\left[1 + \frac{R2}{R_{Fb}} + \frac{R2}{R1}\right]$$

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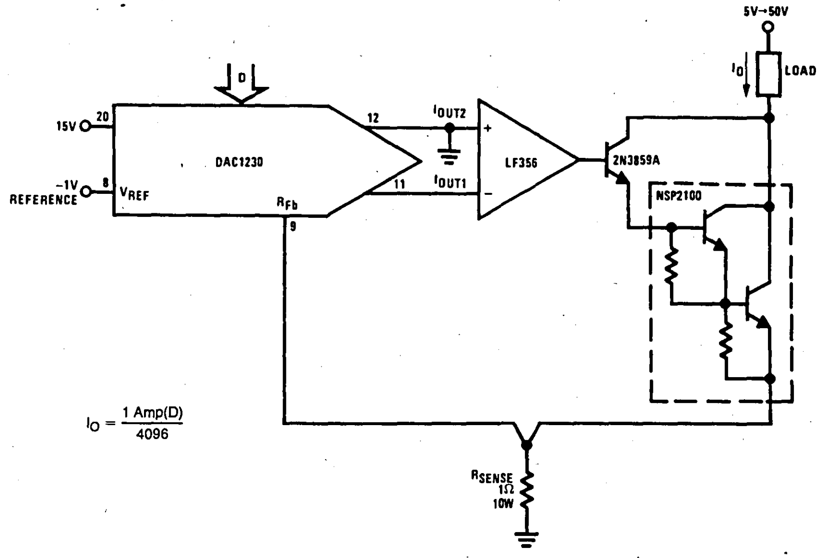
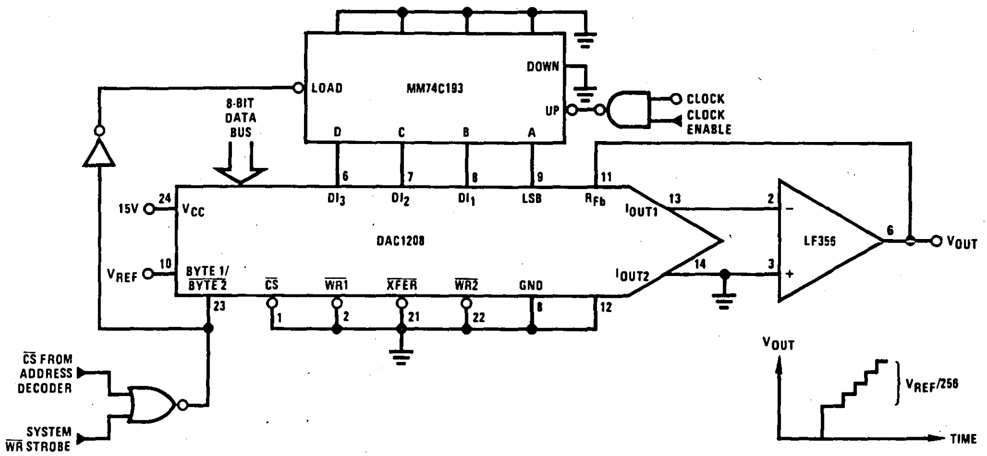
Application Hints (Continued)

High Current Controller



8-Bit Course, 4-Bit Vernier DAC



TL/H/5690-18

National Semiconductor

PRELIMINARY

DAC1218, DAC1219 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved though the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors to allow the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

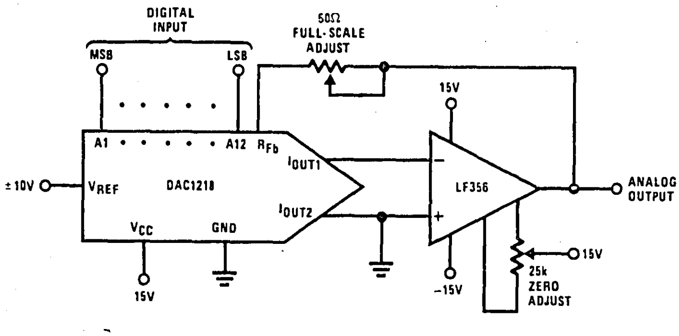
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

Current Settling Time	1 μS
Resolution	12 Bits
Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
Gain Tempco	1.5 ppm/°C
Low Power Dissipation	20 mW
Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



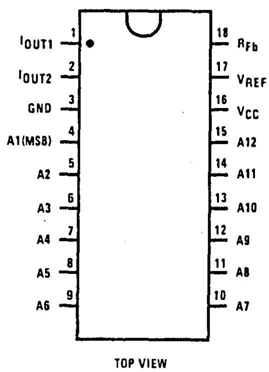
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high

AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



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Order Number DAC1218LD, DAC1218LCD, DAC1219LD or DAC1219LCD
See NS Package D18A

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
DAC1218LD, DAC1219LD	−55°C to +125°C
DAC1218LCD, DAC1219LCD	−40°C to +85°C
Range of V_{CC}	5 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

T_A = 25°C, V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units	Notes
Resolution		12	12	12	Bits	
Linearity Error	Zero and Full-Scale					4, 7
(End Point Linearity)	Adjusted $T_{MIN} < T_A < T_{MAX}$ $-10V \le V_{REF} \le 10V$ DAC1218 DAC1219			 0.012 0.024	 % of FSR % of FSR	 6 5
Differential Non-Linearity	Zero and Full-Scale Adjusted $T_{MIN} < T_A < T_{MAX}$ $-10V \le V_{REF} \le 10V$ DAC1218 DAC1219			 0.012 0.024	 % of FSR % of FSR	4, 7 6 5
Monotonicity	$T_{MIN} < T_A < T_{MAX}$ $-10V \le V_{REF} \le 10V$	 12	 12	 12	 Bits	4, 6 5
Gain Error	Using Internal R_{Fb} $-10V \le V_{REF} \le 10V$	 −0.2	 −0.01	 0.0	 % of FSR	 5, 7
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$ Using Internal R_{Fb}		 ±1.3	 ±6.0	 ppm of FS/°C	6, 7 9
Power Supply Rejection	All Digital Inputs High		±3.0		ppm of FSR/V	7
Reference Input Resistance		10	15	20	kΩ	
Output Feedthrough Error	V_{REF} = 120 Vp-p, f = 100 kHz All Data Inputs Low D Package		3 3		mVp-p mVp-p	 8
Output Capacitance	All Data Inputs High I_{OUT1} All Data Inputs High I_{OUT2} All Data Inputs Low I_{OUT1} All Data Inputs Low I_{OUT2}		200 70 70 200		pF pF pF pF	
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$		1.2	2.0	mA	6
Output Leakage Current I_{OUT1} I_{OUT2}	−40°C to +85°C All Data Inputs Low All Data Inputs High			 10 10	 nA nA	6, 10
Output Leakage Current I_{OUT1} I_{OUT2}	−55°C to +125°C All Data Inputs Low All Data Inputs High			 100 100	 nA nA	
Digital Input Threshold	$T_{MIN} \le T_A \le T_{MAX}$ Low Threshold High Threshold	 2.0		 0.8	 V_{DC} V_{DC}	6
Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$ Digital Inputs <0.8V Digital Inputs >2.0V		 −50 0.1	 −200 10	 μA_{DC} μA_{DC}	6
t_S Current Settling Time	R_L = 100Ω, Output Settled to 0.01%, All Digital Inputs Switched Simultaneously					

Electrical Characteristics Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "Absolute Maximum" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm\ 1\ V_{DC}$.

Note 6: $T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1218 is 0.012% of FSR. This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% $\times$ V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. 1 ppm of $FSR = V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ± 6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from $-40°C$ to $+85°C$ of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is $\pm 0.075\%$ of V_{REF}.

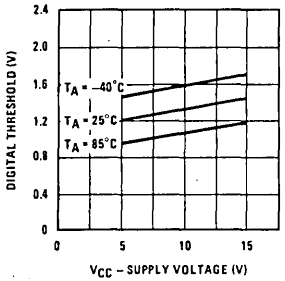
Note 8: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 9: Guaranteed by design but not tested.

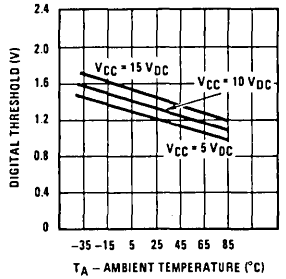
Note 10: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Typical Performance Characteristics

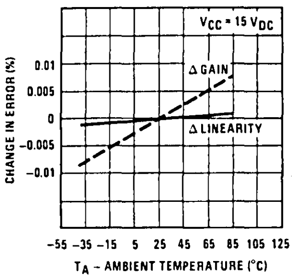
Digital Input Threshold vs V_{CC}



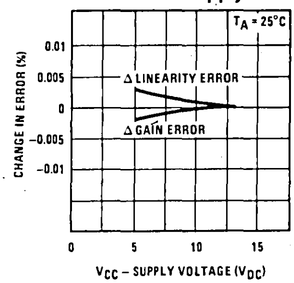
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature



Gain and Linearity Error Variation vs Supply Voltage



TL/H/5691–2

Definition of Package Pinouts

A1 and A12: Digital Inputs. A12 is the least significant digital input (LSB) and A1 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital input of all 1s, and is zero for a digital input of all 0s.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage).

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects to an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to $-10V$. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Ground. This is the ground for the circuit.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1218 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error in the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

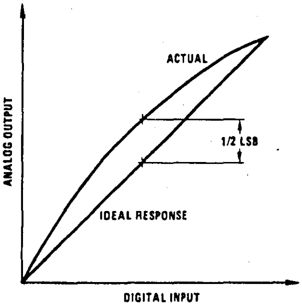
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

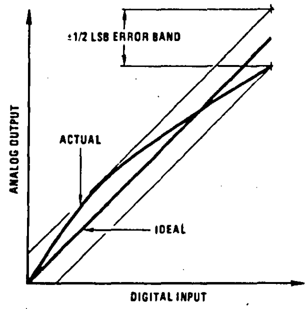
Full-scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1218 full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test

TL/H/5691-3

Application Hints

The DAC1218 and DAC1219 are pin-for-pin compatible with the DAC1220 series but feature 12 and 11-bit linearity specifications. To preserve this degree of accuracy, care must be taken in the selection and adjustments of the output amplifier and reference voltage. Careful PC board layout is important, with emphasis made on compactness of components to prevent inadvertent noise pickup and utilization of single point grounding and supply distribution.

1.0 BASIC CIRCUIT DESCRIPTION

Figure 1 illustrates the R-2R current switching ladder network used in the DAC1218 and DAC1219. As a function of the logic state of each digital input, the binarily weighted current in each leg of the ladder is switched to either I_{OUT1} or I_{OUT2}. The voltage potential at I_{OUT1} and I_{OUT2} must be at zero volts to keep the current in each leg the same, independent of the switch state.

The switches operate with a small voltage drop across them and can therefore conduct currents of either polarity. This permits the reference to be positive or negative, thereby allowing 4-quadrant multiplication by the digital input word. The reference can be a stable DC source or a bipolar AC signal within the range of ± 10V, for specified accuracy, with an absolute maximum range of ± 25V. The reference can also exceed the applied V_{CC} of the DAC.

The maximum output current from either I_{OUT1} or I_{OUT2} is equal to

$$\frac{V_{REF(max)}}{R}\left(\frac{4095}{4096}\right),$$

where R is the specified reference input resistance (typically 15 kΩ). A high level on any digital input steers current to I_{OUT1} and a low level steers current to I_{OUT2}.

2.0 CREATING A UNIPOLAR OUTPUT VOLTAGE (A DIGITAL ATTENUATOR)

To generate an output voltage quantity and keep the potential at the current output terminals at 0V, an op amp current to voltage converter is used. As shown in *Figure 2*, the current from I_{OUT1} flows through the feedback resistor forcing a proportional voltage at the amplifier output. The voltage at I_{OUT1} is held at a virtual ground potential. The feedback resistor is provided on the chip in conjunction with I_{OUT1} and should always be used as it matches and tracks the R value of the R-2R ladder. The output voltage is the opposite polarity of the applied reference voltage.

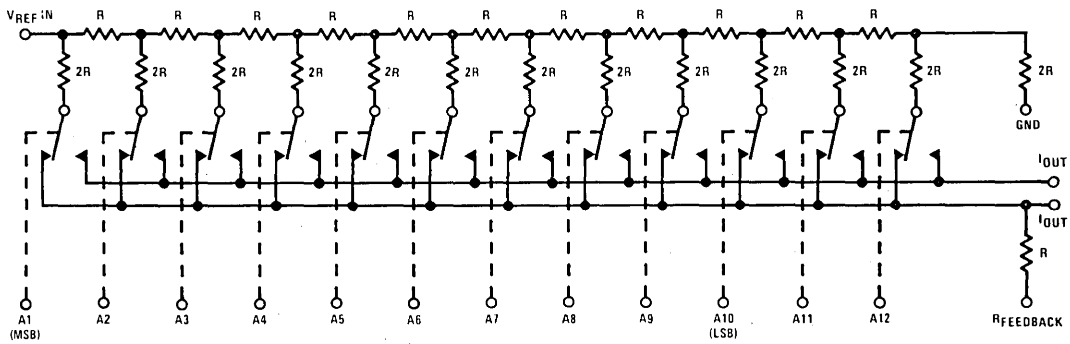
2.1 Amplifier Considerations

To maintain linearity of the output voltage with changing digital input codes the input offset voltage of the amplifier must be nulled. The resistance from I_{OUT1} to ground ($R_{I_{OUT1}}$) varies non-linearity with the applied digital code from the min of R with an all ones input to near ∞ with an all zeros code. Any offset voltage between the amplifier inputs appears at the output with a gain of

$$1+\frac{R_F}{R_{I_{OUT1}}}$$

Since $R_{I_{OUT1}}$ varies with the input code, any offset will degrade output linearity. (See Note 4 of Electrical Characteristics.)

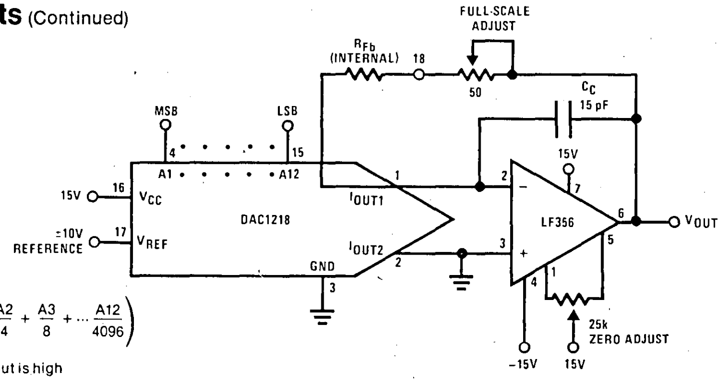
If the desired amplifier does not have offset balancing pins available (it could be part of a dual or quad package) the nulling circuit of *Figure 3* can be used. The voltage at the non-inverting input will be set to $-V_{OS}$ initially to force the inverting input to 0V. The common technique of summing current into the amplifier summing junction cannot be used as it directly introduces a zero code output current error.



Note: Switches shown in digital high state.

FIGURE 1. The R-2R Current Switching Ladder Network

Application Hints (Continued)



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

FIGURE 2. Unipolar Output Voltage

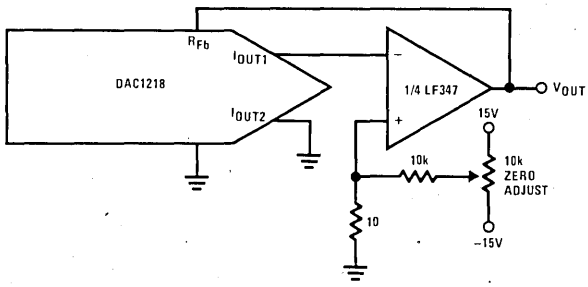


FIGURE 3. Zeroing an Amplifier Which Does Not Have Balancing Provisions

The selected amplifier should have as low an input bias current as possible since it too contributes to the current flowing through the feedback resistor. BI-FET™ op amps such as the LF356 or LF351 or bipolar op amps with super β input transistors like the LM11 or LM308A produce negligible errors.

2.2 Zero and Full-Scale Adjustments

The fundamental purpose is to make the output voltage as near 0 V_{DC} as possible. This is accomplished in the circuit of *Figure 2* by shorting out the amplifier feedback resistance, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital input of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The feedback short is then removed and the converter is zero adjusted.

A unique characteristic of these DACs is that any full-scale or gain error is always negative. This means that for a full-scale input code the output voltage, if not inherently correct, will always be less than what it should be. This insures that adding resistance in series with the internal feedback resistor, R_{Fb}, will always correct for any gain error. The 50Ω potentiometer in *Figure 2* is all that is needed to adjust the worst case DAC gain error.

Conversion accuracy is only as good as the applied reference voltage, so providing a stable source over time and temperature is an important factor to consider.

2.3 Output Settling Time

The output voltage settling time for this circuit in response to a change of the digital input code (a full-scale change is the worst case) is a combination of the DAC output current settling and the settling characterstics of the output amplifier. The amplifier settling is further degraded by a feedback pole formed by the feedback resistance and the DAC output capacitance (which varies with the digital code). First order compensation for this pole is achieved by adding a feedback zero with capacitor C_C shown in *Figure 2*.

In many applications output response time and settling is just as important as accuracy. It can be difficult to find a single op amp which combines excellent DC characteristics (low V_{OS}, V_{OS} drift and bias current) with fast response and settling time. BI-FET™ op amps offer a reasonable compromise of high speed and good DC characteristics. The circuit of *Figure 4* illustrates a composite amplifier connection which combines the speed of a BI-FET™ LF351 with the excellent DC input characteristics of the LM11. If output settling time is not so critical, the LM11 can be used alone.

Figure 5 is a settling time test circuit for the complete voltage output DAC circuit. The circuit allows the settling time of the DAC amplifier to be measured to a resolution of 1 mV out of a zero to ± 10V full-scale output change on an oscilloscope. *Figure 6* summarizes the measured settling times for several output amplifiers and feedback compensation capacitors.

Application Hints (Continued)

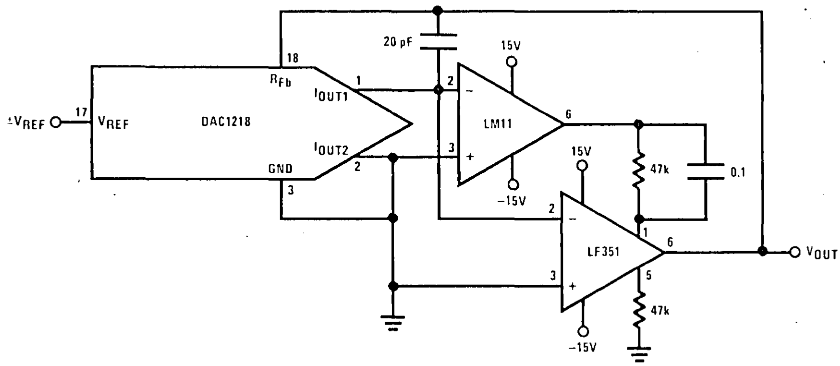
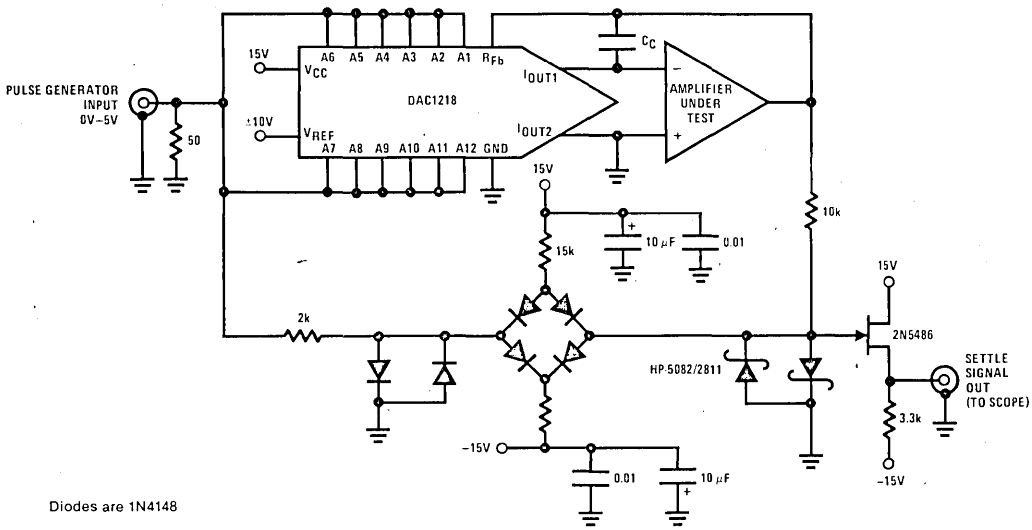


FIGURE 4. Composite Output Amplifier Connection



Diodes are 1N4148

FIGURE 5. DAC Settling Time Test Circuit

Amplifier	C_C	Settling Time to 0.01%
LM11	20 pF	30 µs
LF351	15 pF	8 µs
LF351	30 pF	5 µs
Composite LM11-LF351	20 pF	8 µs
LF356	15 pF	6 µs

FIGURE 6. Some Measured Settling Times

Application Hints (Continued)

3.0 OBTAINING A BIPOLAR OUTPUT VOLTAGE FROM A FIXED REFERENCE

The addition of a second op amp to the circuit of *Figure 2* can generate a bipolar output voltage from a fixed reference voltage *(Figure 7)*. This, in effect gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference voltage can also be reversed to realize full 4-quadrant multiplication.

The output responds in accordance to the following expression:

$$V_O = V_{REF}\left(\frac{D-2048}{2048}\right) \quad 0 \le D \le 4095$$

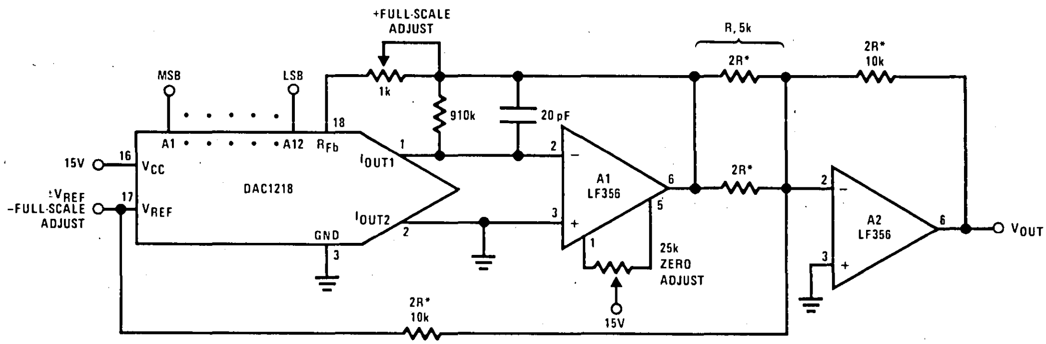
where D is the decimal equivalent of the true binary input word. This configuration inherently accepts a code (half-scale or D = 2048) to provide 0V out without requiring an external 1/2 LSB offset as needed by other bipolar multiplying DAC circuits.

Only the offset voltage of amplifier A1 need be nulled to preserve linearity. The gain setting resistors around A2 must match and track each other. A thin film, 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four resistors can be paralleled to form R and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

Applied Digital Input MSB . . . . LSB	Decimal Equivalent	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
1 1 1 1 1 1 1 1 1 1 1 1	4095	$V_{REF}-1$ LSB	$-\lvert V_{REF}\rvert+1$ LSB
1 1 0 0 0 0 0 0 0 0 0 0	3072	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0 0 0 0 0	2048	0	0
0 1 1 1 1 1 1 1 1 1 1 1	2047	-1 LSB	$+1$ LSB
0 1 0 0 0 0 0 0 0 0 0 0	1024	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
0 0 0 0 0 0 0 0 0 0 0 0	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

Where $1\ \text{LSB} = \dfrac{\lvert V_{REF}\rvert}{2048}$



*0.1% matching

FIGURE 7. Obtaining a Bipolar Output from a Fixed Reference

Application Hints (Continued)

3.1 Zero and Full-Scale Adjustments

The three adjustments needed for this circuit are shown in *Figure 7*. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adjust" for zero volts at the inverting input (pin 2) of OA1. Next, with a code of all zeros still applied, adjust "− full-scale adjust", the reference voltage, for $V_{OUT} = \pm |(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+ full-scale adjust" for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. This + full-scale adjustment scheme takes into account the effects of the V_{OS} of amplifier A2 (as long as this offset is less than 0.1% of V_{REF}) and any gain errors due to external resistor mismatch.

4.0 MISCELLANEOUS APPLICATION HINTS

The devices are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to electrostatic discharge.

During power-up supply voltage sequencing, the negative supply of the output amplifier may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is clamped to one diode drop below ground.

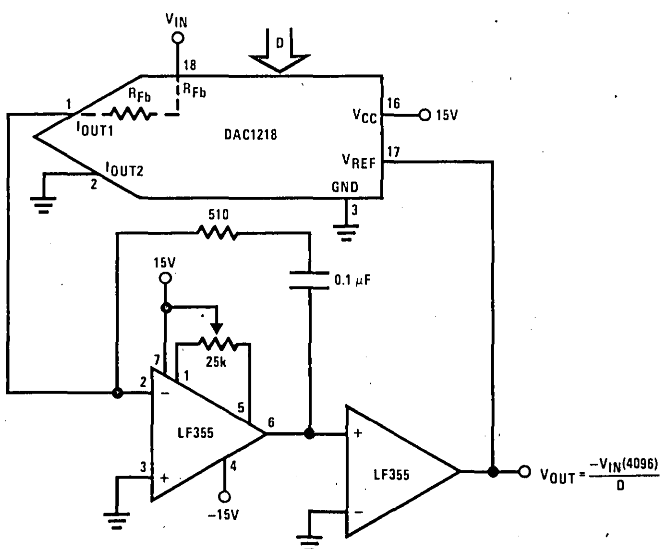
As a general rule, any unused digital inputs should be tied high or low as required by the application. As a troubleshooting aid, if any of the digital inputs are left floating, the DAC will interpret that input as a logical 1 level.

Additional Application Ideas

For the circuits shown, D represents the decimal equivalent of the binary digital input code. D ranges from 0 (for an all zeros input code) to 4095 (for an all ones input code) and for any code can be determined from:

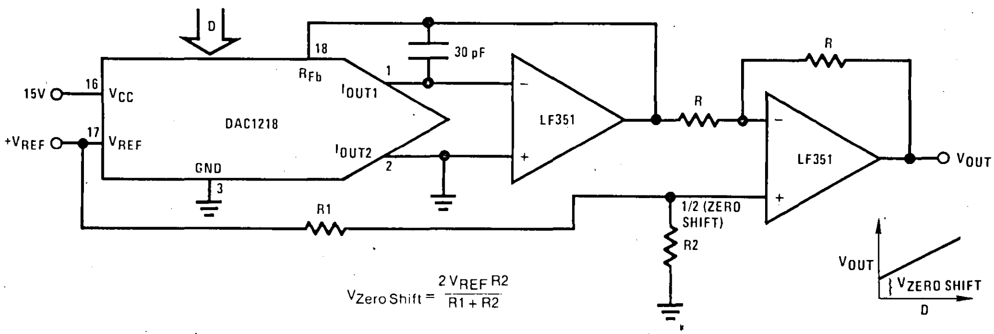
D = 2048(A1) + 1024(A2) + 512(A2) + ... 2(A11) + 1(A12)
where AN = 1 if that input is high
AN = 0 if that input is low

DAC Controlled Amplifier



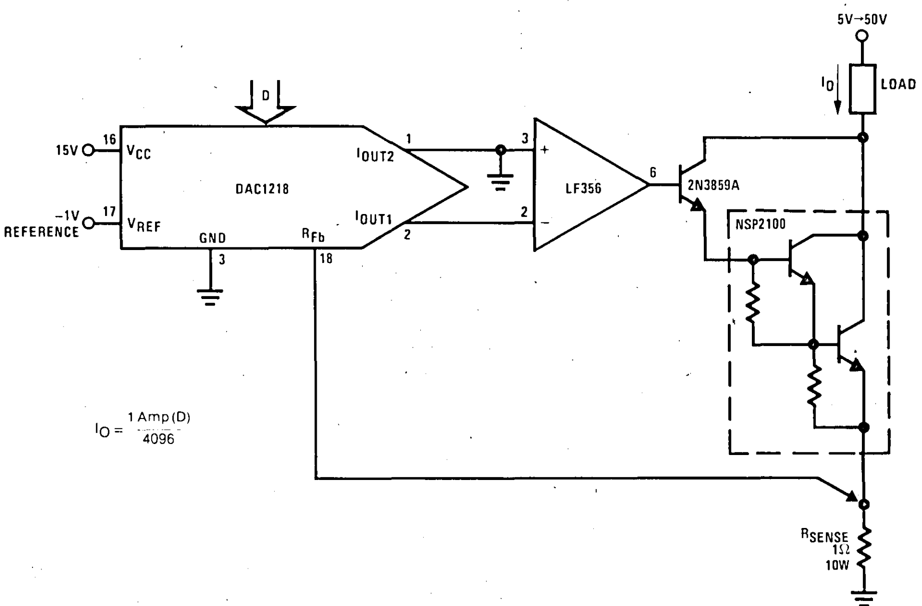
Additional Application Ideas (Continued)

Offsetting the Zero Code Output Voltage



$$V_{Zero\,Shift} = \frac{2\,V_{REF}\,R2}{R1 + R2}$$

High Current Controller

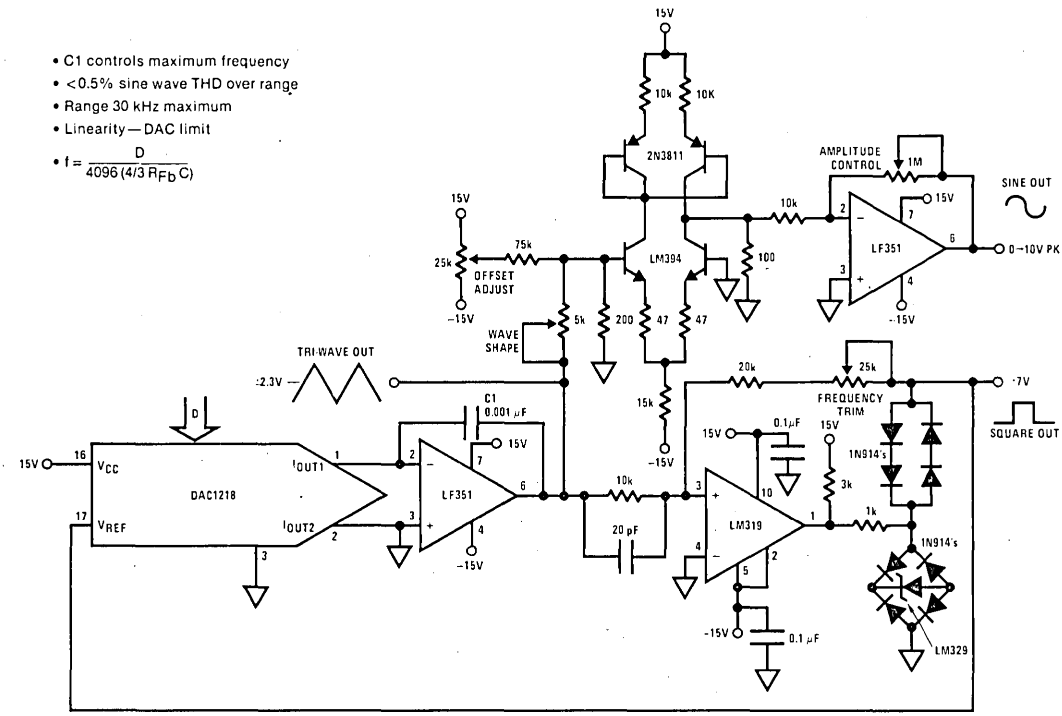


$$I_O = \frac{1\,\text{Amp}\,(D)}{4096}$$

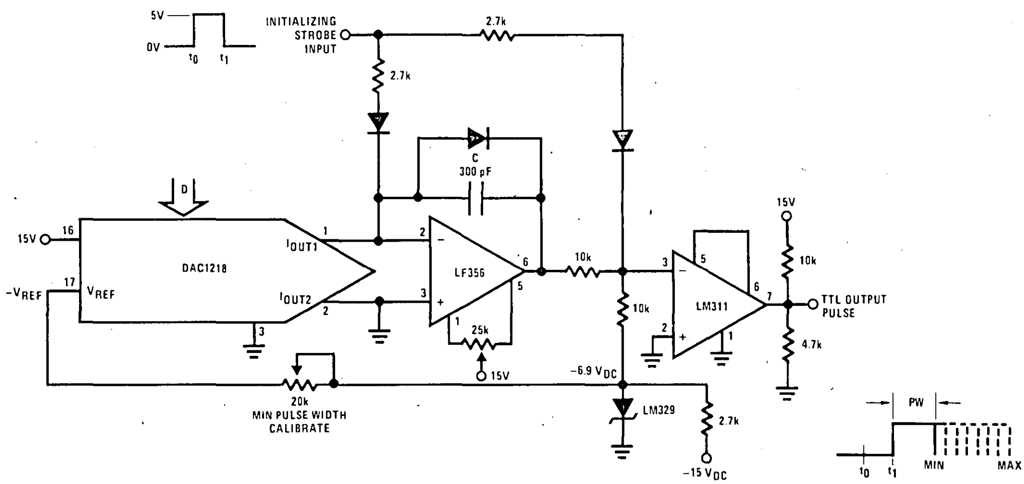
Additional Application Ideas (Continued)

DAC Controlled Function Generator

- C1 controls maximum frequency
- <0.5% sine wave THD over range
- Range 30 kHz maximum
- Linearity—DAC limit
- $f = \dfrac{D}{4096\,(4/3\,R_{Fb}\,C)}$



Digitally Programmable Pulse-Width Generator



$$PW \cong \frac{C\,(7.5V)\,(4096)\,(R_{Fb})}{D\,|V_{REF}|}$$

Section 7

Data Communications Support

7

Introduction

This section contains products that are designed to transmit digital data in a serial format from remote sources. These products can be used for TV remote control, security monitoring, process monitoring, or transmitting data that is obtained from a remote digital transducer.

The use of CMOS processes for these products ensures low active power; in addition, a power saving standby mode is available.

National Semiconductor

PRELIMINARY

MM58220 Asynchronous Low Power Transmitter Remote Controller

General Description

The MM58220 is a metal gate CMOS integrated circuit. This circuit is designed to transmit a pulse width modulated serial data stream of 18 bits. This stream consists of 7 address bits, 1 write bit, 8 data bits, 1 parity bit, and 1 dummy bit, in that order. The format of the data word is such that it is directly compatible with the MM54240 asynchronous receiver/transmitter. The serial transmission is initiated by a logic signal. This circuit is designed for low power usage. It draws less than 10 μA in its standby mode.

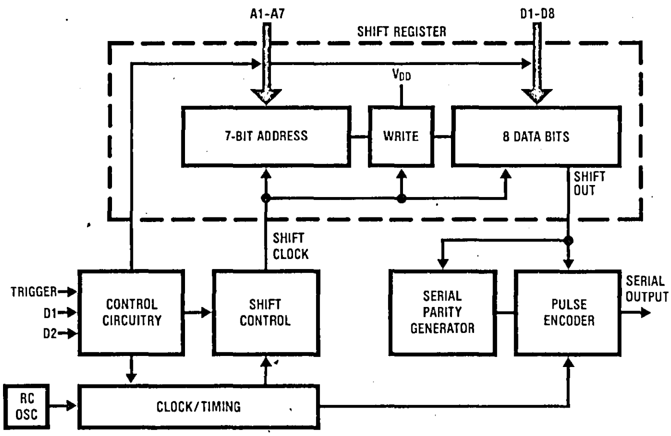
Applications

The MM58220 finds applications in transmitting data from remote sources that have limited power supply capabilities. Typical applications include security monitoring, process monitoring, and transmitting data from a remote digital transducer.

Features

- Compatible with the MM58240 receiver/transmitter
- Low power drain (less than 10 μA in standby mode)
- Wide supply voltage range (4.0V to 15.0V)
- On-chip oscillator based on inexpensive RC components
- Single or repetitive data word transmissions
- Repetitive transmissions conform to FCC standards

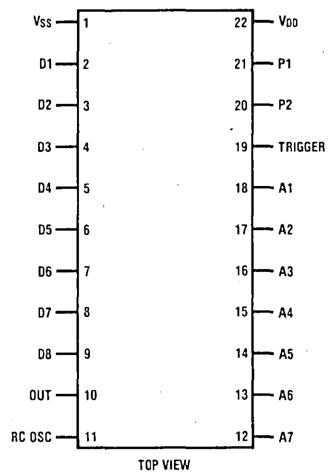
Functional Block Diagram



TL/F/6147-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6147-2

Order Number MM58220J or MM58220N
See NS Package J22A or N22A

National Semiconductor

PRELIMINARY

MM58250 Infrared Transmitter

General Description

The infrared transmitter is designed to drive an infrared LED (only one external npn transistor is required) with data encoded in a pulse-width-modulated (pwm) format. To get a better signal-to-noise-ratio the pwm scheme amplitude modulates a 38kHz carrier. The data to be transmitted is input in two ways. The primary data input mode (MS = 1) is through a 4-by-8 single-contact keyboard which is interpreted by on-chip logic. The second input mode (MS = 0) is the direct input mode. In this mode a five-bit parallel word and a load pulse are applied to the inputs. The five-bit word is then converted to the pwm format and transmitted.

The chip is designed for battery operation, so it employs a number of power-saving techniques. The chip is implemented in CMOS, so the supply current required by the logic is low. The oscillator can be disabled, allowing the stand-by current to be less than 1μA. Although the continuous transmission of the data stream is possible, the repetition rate of the continuous transmission is restricted, and the majority of the codes transmittable are repeated only three times. (Twelve outputs can be repeated continuously for analog functions such as volume and channel scanning).

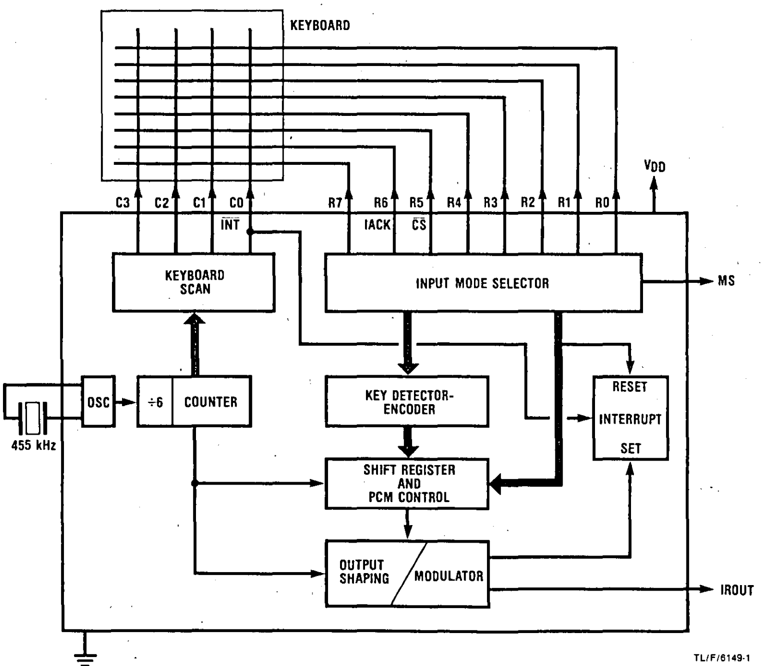
Features

- Up to 32 functions decoded and transmitted
- Single-contact scanned keyboard
- Low standby current (CMOS)
- 455kHz on-chip oscillator
- Wide power supply range (3V-10V)
- Keyboard or direct load modes
- Direct load mode TTL compatible
- 38kHz carrier for improved signal-to-noise-ratio
- High current output stage
- Compatible with MM54251 infrared receiver

Applications

- TV remote control transmitter
- 5-bit wireless asynchronous transmitter
- Intended for use with MM54251

Block Diagram



TL/F/6149-1

Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{DD} +0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500mW
V_{DD}-V_{SS}	12V
Lead Temperature (Soldering, 10 seconds)	300°C
DC Current at IR Output	−20mA

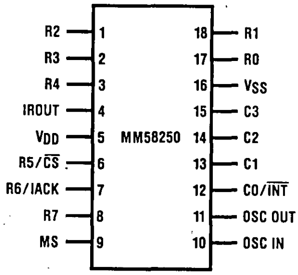
Electrical Characteristics

V_{DD} = 3.0V to 10V, T_A = ±0°C to 70°C unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply					
V_{DD} Supply Voltage		3.0		10	V
V_{DD} Supply Current (Active)				5	mA
V_{DD} Supply Current (Standby)				1	μA
Oscillator Frequency*			455		kHz
IR Output Voltage					
Logic "0"	150μA Sink			0.6	V
Logic "1"	10mA Source	V_{DD}−1.4			V
IR Output Current (Note: no short-circuit protection)	V_{DD}−1.4V	−10		−20	mA
Input Levels	MS = 0, 4.5 ≤ V_{DD} ≤ 5.5 Direct Mode				
Logic "0"				0.5	V
Logic "1"		2.4			V
Input Current	MS = 0, 4.5V ≤ V_{DD} ≤ 5.5V Direct Mode				
R_0-R_6, MS	0V ≤ V_{IN} ≤ V_{DD}	−1		1.0	μA
R_7	V_{IN} = 0.4V	0.06		0.6	mA
Input Current	MS = 1, 3.0V ≤ V_{DD} ≤ 10V Keyboard Mode				
R_0-R_7	V_{IN} = 0.4V	0.024		1.6	mA
MS	0V ≤ V_{IN} ≤ V_{DD}	−1		1	μA
Output Current C_0-C_1	MS = 1				
Logic "1" Source	V_{DD} = 3V, V_{OUT} = V_{DD}−1V	−40			μA
"1" Source	V_{DD} = 10V, V_{OUT} = V_{DD}−1V	−150			μA
Logic "0" Sink	V_{DD} = 3V, V_{OUT} = 0.4V	260			μA
"0" Sink	V_{DD} = 10V, V_{OUT} = 0.5V	1.6			mA
Output Current $C_0/\overline{Int}$ (Open Drain)	MS = 0, 4.5V ≤ V_{DD} ≤ 5.5V				
Logic "1"	0 ≤ V_{OUT} ≤ V_{DD}			1	μA
Logic "0"	V_{OUT} = 0.4V	2.5			mA

*Determined by external components.

Connection Diagram



TL/F/6149-2

Order Number MM58250N
See NS Package N18A

Pin Definitions

Mode Select (MS): This pin selects between the two modes of the MM58250's operation.

MS = "0": Parallel input mode. This mode is designed to allow five bits of data to be written to the MM58250 in a parallel fashion with all the appropriate handshaking signals required to facilitate interfacing a microprocessor.

MS = "1": Keyboard input mode. Data is input from a keyboard configured as a matrix of four column conductors and eight row conductors separated at each point of the matrix by a single contact.

R_0/-R_7/:

Keyboard Mode (MS = 1):

R_0/-R_7/: Act as row inputs for a scanned column keyboard. Internal to the MM58250, these are encoded such that if just one input is low during a scan of the column outputs, (see the discussion of pins C_0/-C_3/) a parallel-in-serial-out transmit buffer is loaded with the binary representation of the low row input and the scanning column. (The binary number loaded is equal to the decimal number in the pin name, i.e. binary 5 is stored for the R_5 input.) In addition R_3/-R_5/ cause the MM58250 to continuously transmit the data stored in its transmit buffer (see Figure 6) as long as a switch closure exists.

Parallel Mode (MS = 0):

R_0/-R_4/: These five inputs act as a parallel, non-inverting, 5-bit data entry path.

R_5/-CS/: This active low input is used to latch in the data at the R_0/-R_4/ inputs, as well as beginning the transmit cycle. The part will continue to transmit as long as this input is low and continue to transmit two to three transmit cycles after the input switches to logic "1", depending on where (see Figures 7 and 8) in the transmit cycle the logic change occured. (Note: the data on R_0/-R_4/ should be held stable a minimum of 60ms.)

R_6/-IACK: This input is used to reset the INT/ signal. It is active high. (See Figure 7)

R_7/: R_7/ enables two functions that were designed to facilitate the testing of the MM58250 quickly that might prove useful to some users.

The divide-by-six prescaler can be by-passed by applying a logic "0" to R_7/ when R_6/ = "1" and MS = "0". The by-pass is implemented by setting an RS-flip-flop that controls the multiplexing of the main clock line from the output of the divide-by-six prescaler to the output of the oscillator, by-passing the divide-by-six prescaler. The RS-flip-flop is reset by the main internal reset which is made active at the end of the transmit cycle, *begun before* the by-pass was activated. If the MM58250 is waiting for a new input, switching R_7/ low will have no effect.

The second special mode forces the main internal reset active. This causes the chip to load in new data to be transmitted and initializes the chip to the beginning of the word cycle it was currently in or in the word cycle folowing it, depending on where in the word cycle the reset occurred. If a transmit cycle has been completed this mode has no effect. A transmit cycle consists of three word cycles. If no new data is loaded, the MM58250 will go into its idle state within 45ms. See Figures 9-11 for examples of how to use these features.

C_0/-C_3/:

Keyboard Mode (MS = 1):

C_0/-C_3/: These outputs are normally low when MM58250 is waiting for a new input contact closure to occur. A contact closure causes the low signal on the column inputs to be passed to the appropriate row input. This input going low initiates the transmit cycle. As the transmit cycle begins, the oscillator is enabled and begins to oscillate within 6ms. As soon as the oscillator is enabled all the column outputs are switched to the logic "1" state. 40.9ms later, as clocked by the on-chip oscillator, these outputs are individually switched to the logic "0" state (see Figure 5) and the row inputs are sampled. If the sampling of the row inputs does not show any of these inputs low (see Figure 6b), the transmit cycle is aborted. If any of the row inputs is low, the binary representation of the low row input and the binary representation of the low column output are stored in the transmit buffer. If the low row input was R_0/, R_1/, R_2/, R_6/, or R_7/ the outputs C_0/-C_3/ all switch low, so internal logic can detect when all keyboard switches have been opened. This feature allows the MM58250 to terminate transmission after three iterations (see Figure 6a) of the output data, even when a contact closure exists longer than the time required to transmit the data three times.

Parallel Mode (MS = 0):

C_0/-C_3/: In the parallel mode only one of the column outputs is still used. This output is used as the C_0/ strobe in the keyboard mode. It is used in this mode as an active low processor interrupt (INT/). This output is designed to drive one TTL input with a 10k pullup resistor. It is reset by the IACK pin. When $R_5/\overline{CS}$ is a logic 1, this signal goes low after the last transmission is complete.

IROUT: This is the output that provides the drive signal for the transmission (see Figures 3 and 4). IROUT provides at least 10mA of current, sufficient to drive a single npn transistor hard enough to provide the 200mA of drive current for the infra-red diodes. The data is output in a serial mode with a start bit and a stop bit bracketing the five data bits. The pwm format used has a 1.6ms bit time with a 75% duty cycle for a '1' and a 25% duty cycle for a '0'. The start and stop bits are zeros.

Timing Specification

Input Timing	Min.	Max.	Units
Microprocessor Mode			
Data Set-up Time	0		s
Data Hold Time	50		ms
$\overline{CS}$ (minimum pulse width)	250		ns
IACK (minimum pulse width)	250		ns
Keyboard Mode			
Switch Bounce		40	ms
Output Timing			
Oscillator Start up (Subject to external components)		9	ms

All of the following data is based on an oscillator frequency = 455 kHz and will vary as the oscillator frequency varies.

Timing Diagrams

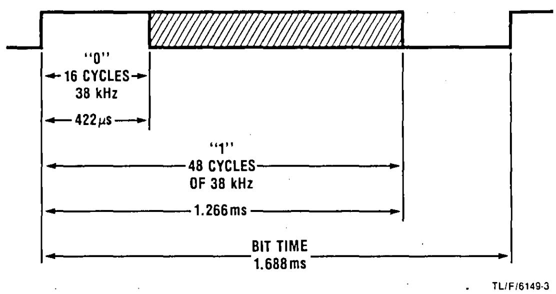


Figure 2. Bit Timing

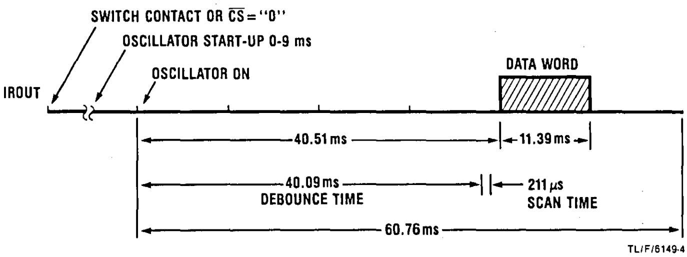


Figure 3. 1/3 Transmit Cycle

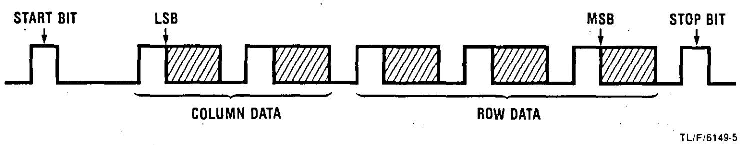


Figure 4. Data Word

Timing Diagrams (Continued)

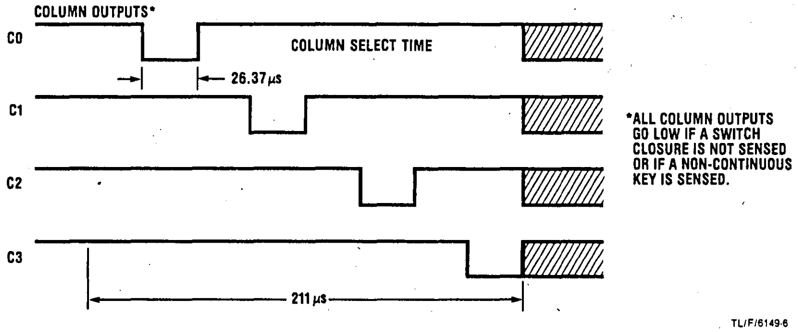


Figure 5. Column Scan Timing

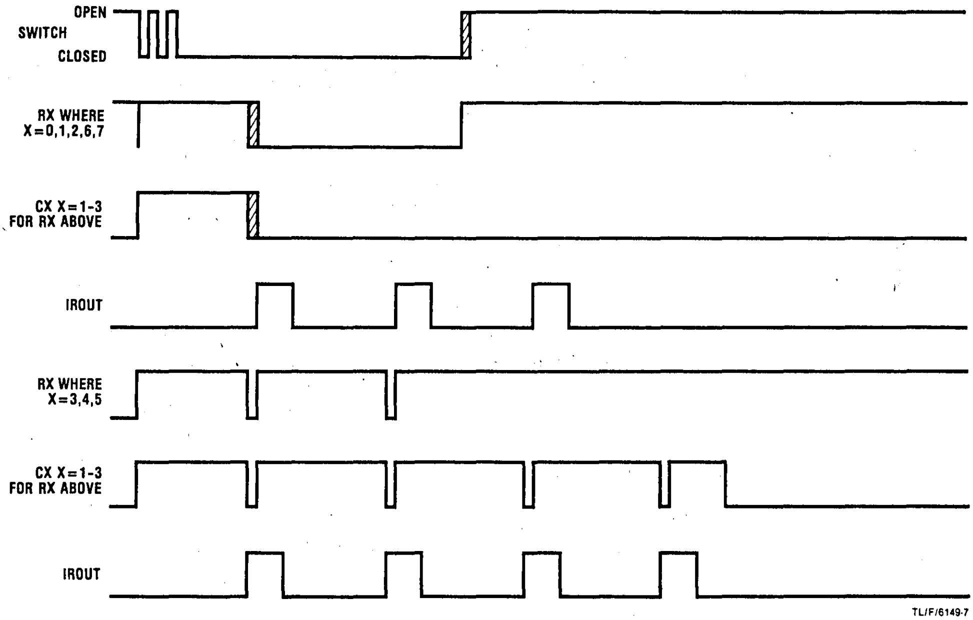


Figure 6a. Typical Transmit Cycles

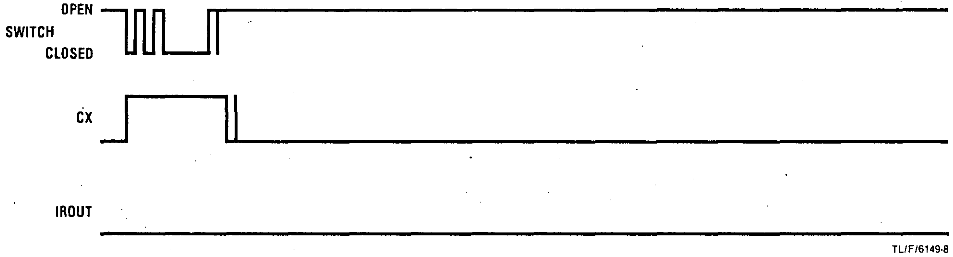


Figure 6b. Aborted Transmit Cycle

Timing Diagrams (Continued)

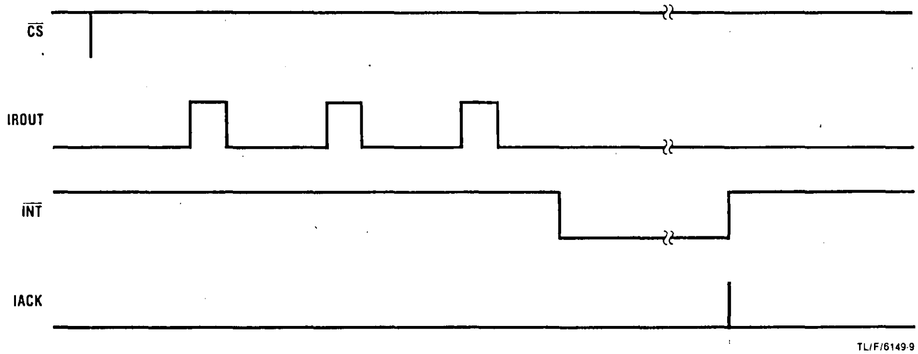


Figure 7. Interrupt Timing

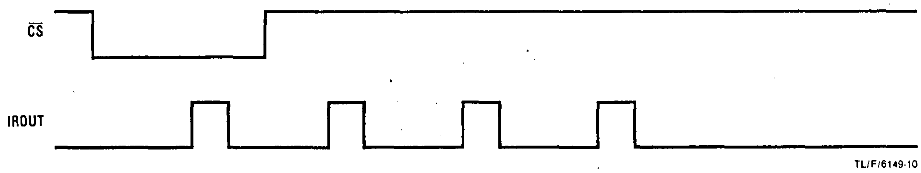


Figure 8. Typical Microprocessor Transmit Cycle

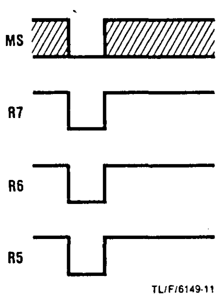


Figure 9. Reset Chip to Beginning of Transmit Cycle

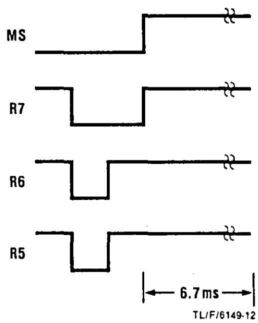


Figure 10. Complete Reset

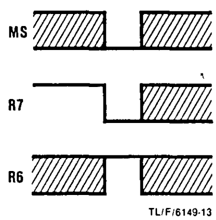


Figure 11. 6X Speed up of Transmit Cycle

Transmitter Functions

#	Code					Row								Column				Function	Notes
	16	8	4	2	1	0	1	2	3	4	5	6	7	0	1	2	3		
0	0	0	0	0	0	x								x				0 Direct Entry	1
1	0	0	0	0	1	x									x			1 Direct Entry	1
2	0	0	0	1	0	x										x		2 Direct Entry	1
3	0	0	0	1	1	x											x	3 Direct Entry	1
4	0	0	1	0	0		x							x				4 Direct Entry	1
5	0	0	1	0	1		x								x			5 Direct Entry	1
6	0	0	1	1	0		x									x		6 Direct Entry	1
7	0	0	1	1	1		x										x	7 Direct Entry	1
8	0	1	0	0	0			x						x				8 Direct Entry	1
9	0	1	0	0	1			x							x			9 Direct Entry	1
10	0	1	0	1	0			x								x		Memory Up	1
11	0	1	0	1	1			x									x	On/Off	1
12	0	1	1	0	0				x					x				Slow Up	2
13	0	1	1	0	1				x						x			Slow Down	2
14	0	1	1	1	0				x							x		Search Up	2
15	0	1	1	1	1				x								x	Mute	2
16	1	0	0	0	0					x				x				Analog I Down	2
17	1	0	0	0	1					x					x			Analog I Up	2
18	1	0	0	1	0					x						x		Analog II Down	2
19	1	0	0	1	1					x							x	Analog II Up	2
20	1	0	1	0	0						x			x				Analog III Down	2
21	1	0	1	0	1						x				x			Analog III Up	2
22	1	0	1	1	0						x					x		Analog IV Down	2
23	1	0	1	1	1						x						x	Analog IV Up	2
24	1	1	0	0	0							x		x				Not Defined	1
25	1	1	0	0	1							x			x				
26	1	1	0	1	0							x				x			
27	1	1	0	1	1							x					x		
28	1	1	1	0	0								x	x					
29	1	1	1	0	1								x		x				
30	1	1	1	1	0								x			x			
31	1	1	1	1	1								x				x		

Note 1: Three transmissions.

Note 2: Continuous transmission.

Typical Applications

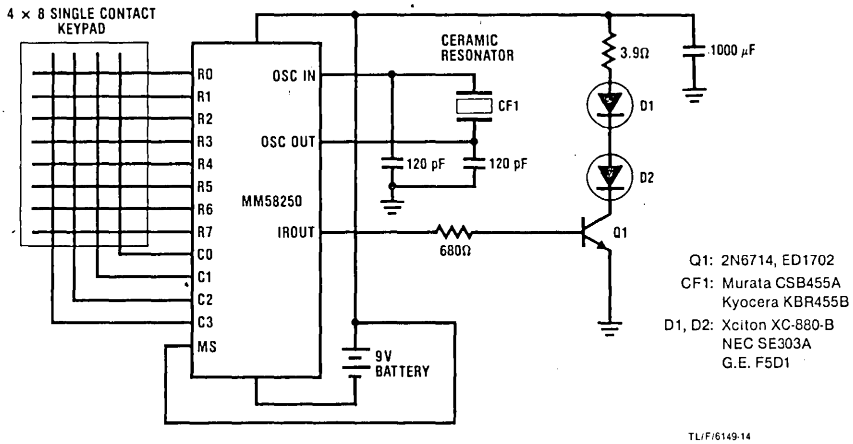


Figure 12.

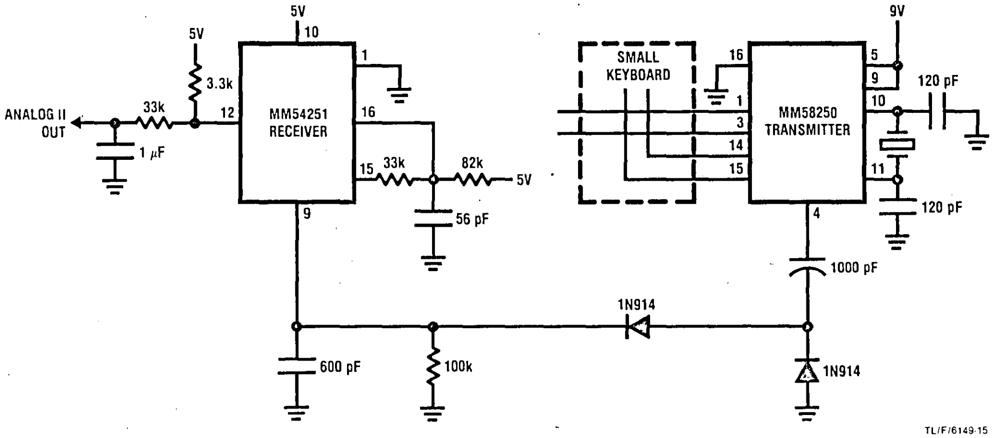


Figure 13. Quick Checkout Circuit

Section 8
Display Controllers/Drivers

8

Introduction

Incorporating efficient, imaginative displays has become a real challenge. National Semiconductor is helping you stay ahead of your competitors with the widest choice of display drivers of any electronics manufacturer. From our software-compatible standard MOS/LSI family to our cascadable dot/bar drivers to decoders and counters, there is a National driver to meet your application.

Selecting a high-quality, reliable display driver can have a long-term impact on any electronic system. As with all of our other circuits, National's display drivers incorporate strict design rules, careful materials selection and processing expertise. In addition, a rigid quality control program assures you of receiving drivers that prove themselves out in the field.

Another major consideration in choosing a circuit is the ability of the supplier to come through with timely deliveries. As one of the world's largest suppliers of semiconductor products, National has the manufacturing capabilities to consistently meet high-volume requirements with fast response times and competitive prices. That enables your company to plan production schedules with confidence.

National's complete selection of display drivers offers you many options for augmenting your overall design while keeping costs in line. For example, we supply the industry's only drivers with software compatibility.

National Semiconductor

MM5452, MM5453 Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4 1/2-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores the display data in latches after it is clocked in, and holds the data until new display data is received.

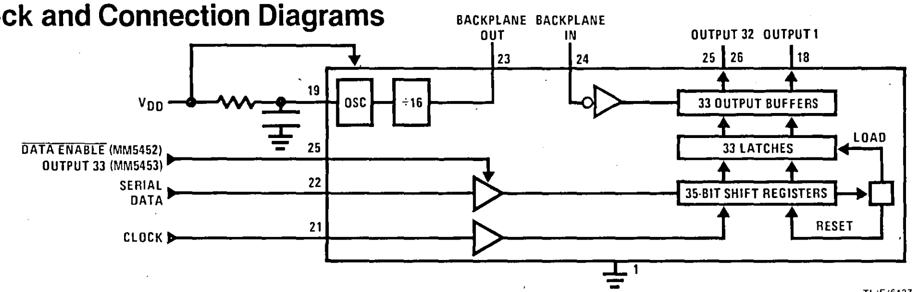
Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

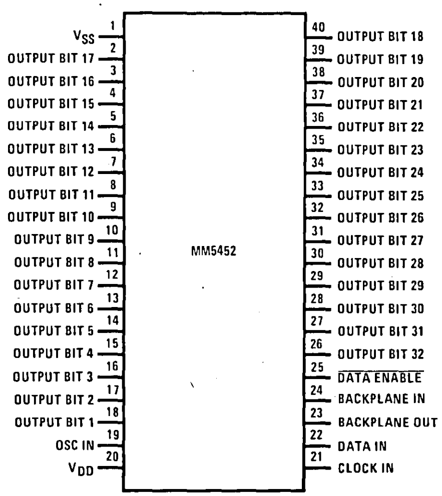
Block and Connection Diagrams



TL/F/6137-1

FIGURE 1

Dual-In-Line Package

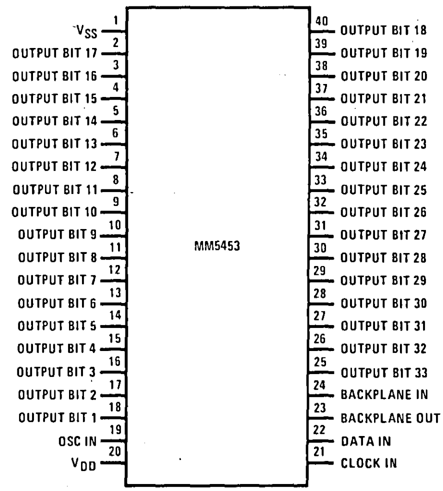


TOP VIEW

TL/F/6137-2

FIGURE 2a

Dual-In-Line Package



TOP VIEW

TL/F/6137-3

FIGURE 2b

Order Number MM5452D, MM5453D, MM5452N or MM5453N
See NS Package D40C or N40A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}+10V$	Power Dissipation	300 mW at +70°C
Operating Temperature	0°C to +70°C		350 mW at +25°C
Storage Temperature	−65° to +150°C	Junction Temperature	+150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating range, $V_{DD}=3.0V$ to 10V, $V_{SS}=0V$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3		10	V
Power Supply Current	Excluding Outputs OSC = V_{SS}, BP IN @ 32 Hz $V_{DD}=5V$, Open Outputs, No Clock			40 10	μA μA
Clock Frequency				500	kHz
Input Voltages					
Logical '0' Level	$V_{DD}<4.75$ $V_{DD}\geq4.75$	−0.3 −0.3		0.1 V_{DD} 0.8	V V
Logical '1' Level	$V_{DD}>5.25$ $V_{DD}\leq5.25$	0.8 V_{DD} 2.0		V_{DD} V_{DD}	V V
Output Current Levels					
Segments					
Sink	$V_{DD}=3V$, $V_{OUT}=0.3V$			−20	μA
Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-0.3V$	20			μA
Backplane					
Sink	$V_{DD}=3V$, $V_{OUT}=0.3V$			−320	μA
Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-0.3V$	320			μA
Output Offset Voltage	Segment Load 250 pF Backplane Load 8750 pF			±50	mV
Clock Input Frequency, f_C				500	kHz
Rise Time, t_r				300	ns
Fall Time, t_f				300	ns
High Time, t_h	$t_r=t_f=50$ ns	950			ns
Low Time, t_l		950			ns
Data Input Set-Up Time, t_{DS} Hold Time, t_{DH}		 300 300			 ns ns
Data Enable Input Set-Up Time, t_{DES}		 100			 ns

Functional Description

The MM5452 is specifically designed to operate 4 1/2-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading "1" followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in *Figure 1*. For the MM5452 a $\overline{\text{DATA ENABLE}}$ is used instead of the 33rd output. If the $\overline{\text{DATA ENABLE}}$ signal is not required, the 33rd output can be brought out. This is the MM5453 device.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be a complete set of 36 clocks otherwise the shift registers will not clear.

Figure 2a shows the pin-out of the MM5452. Bit 1 is the first bit following the start bit and it will appear on pin 18.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$.

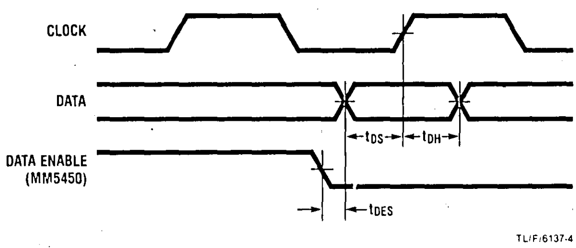


FIGURE 3

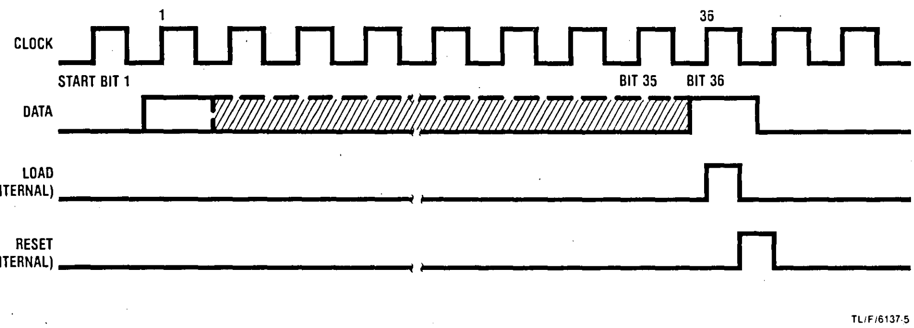
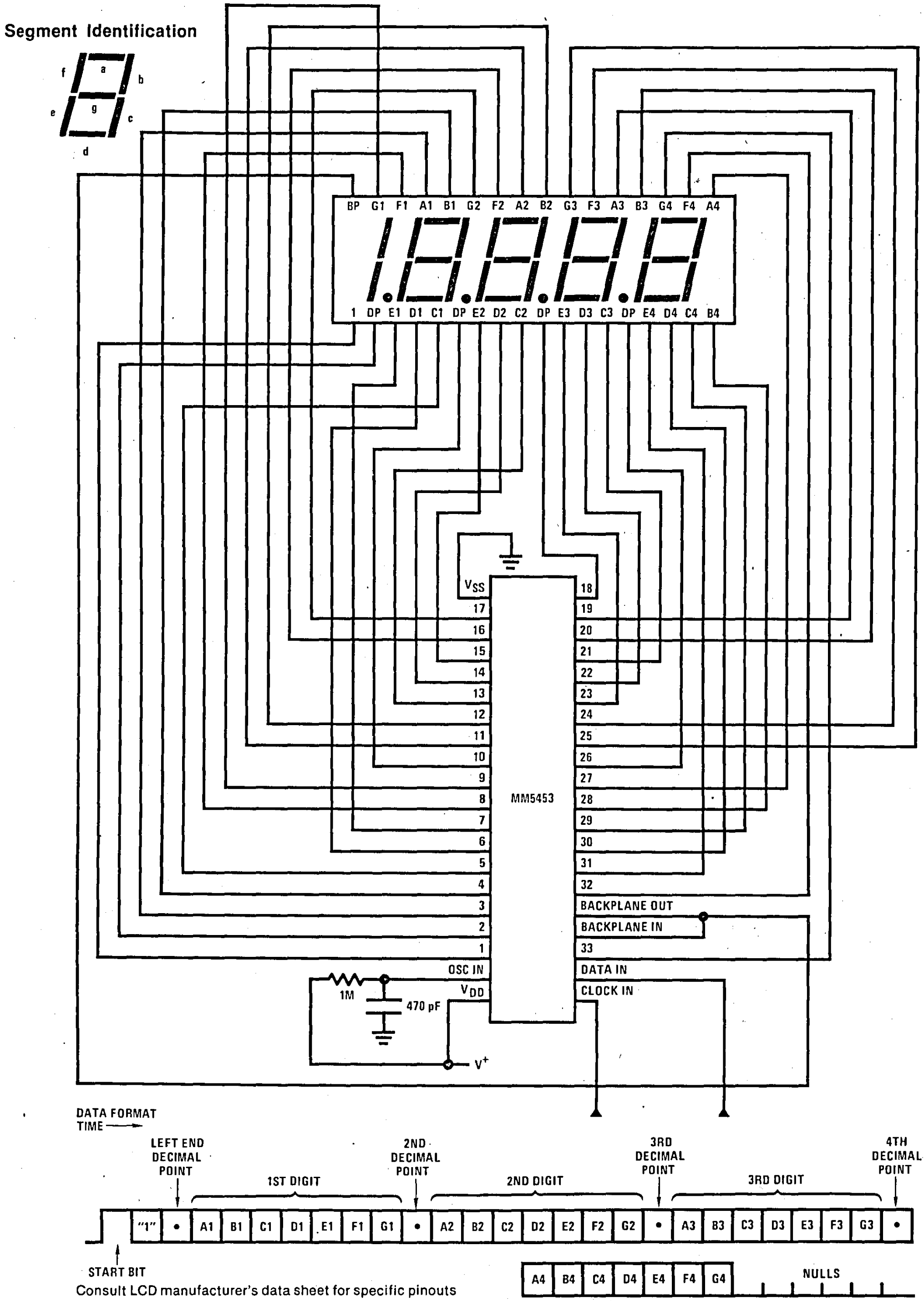


FIGURE 4. Input Data Format

Functional Description (Continued)

Figure 5 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. This application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.



Consult LCD manufacturer's data sheet for specific pinouts

FIGURE 5. Typical 4½-Digit Display Application

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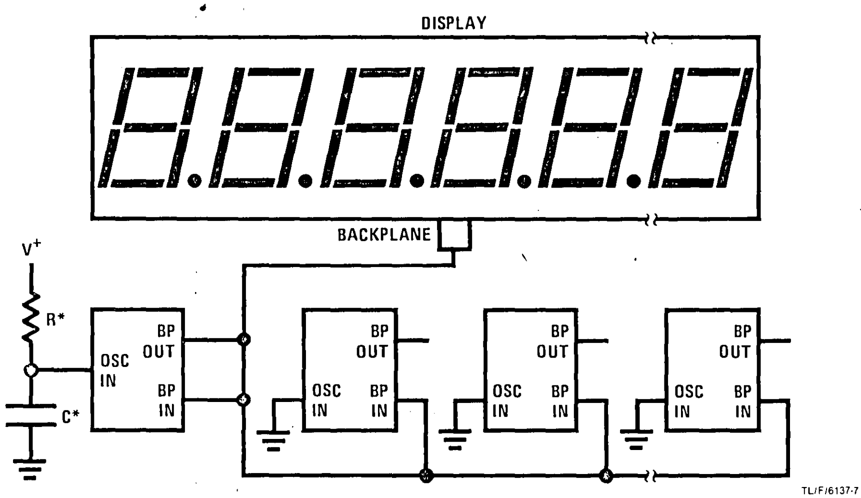
Functional Description (Continued)

Figure 8 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

Using an External Clock

The MM5452, MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%.

Deviations from a 50% duty cycle result in an offset voltage on the LCD. In *Figure 7*, a flip flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumption in the chips. The oscillator is not used.



* The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately 4.91×10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 6. Parallel Backplane Outputs

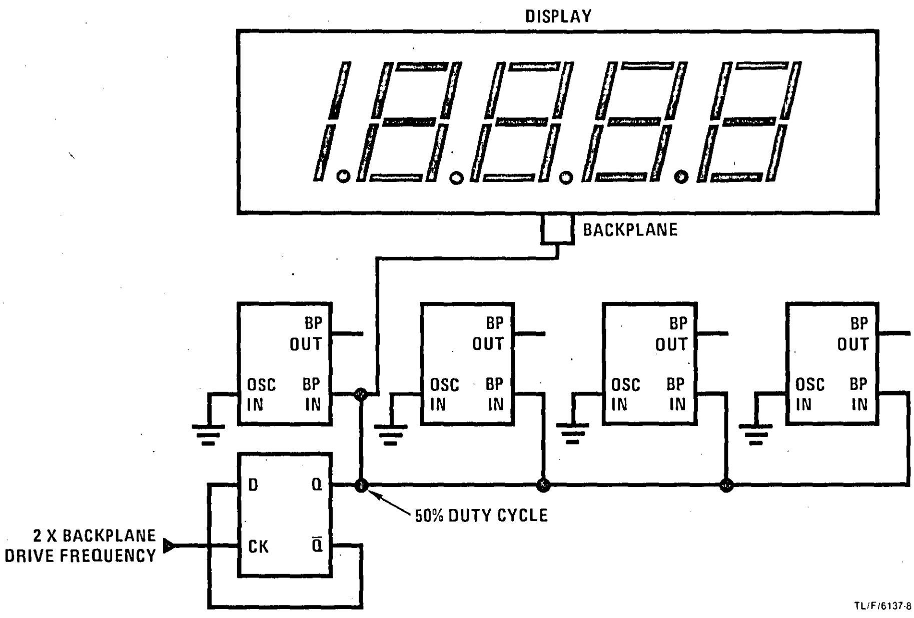


FIGURE 7. External Backplane Clock

Functional Description (Continued)

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 9 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.

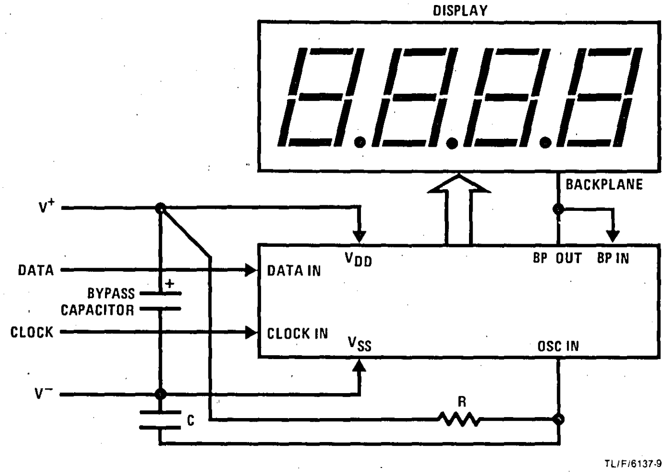
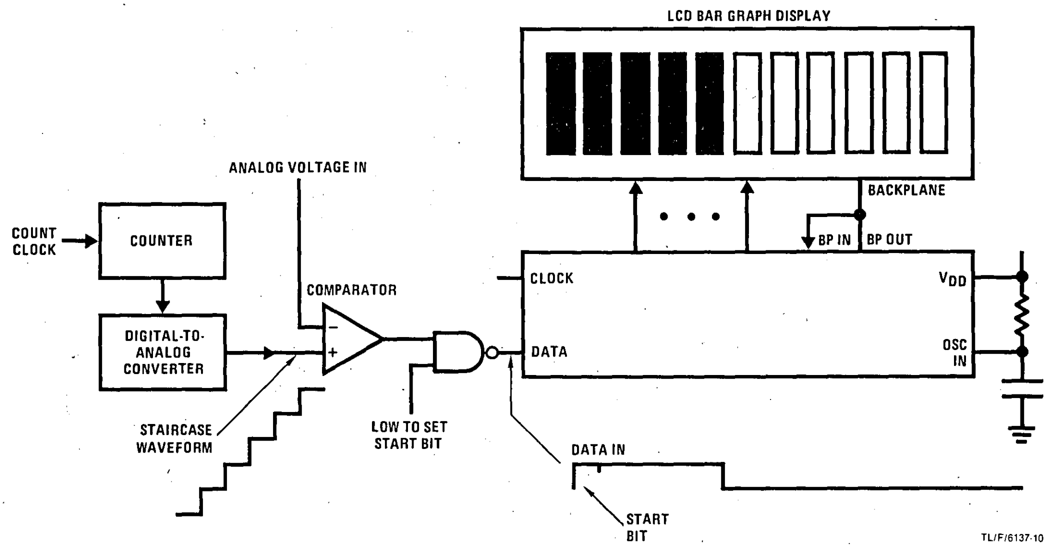


FIGURE 8. Four Wire Remote Display



Data is high until staircase>input

FIGURE 9. Analog Display

National Semiconductor

MM5483 Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received.

Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block and Connection Diagrams

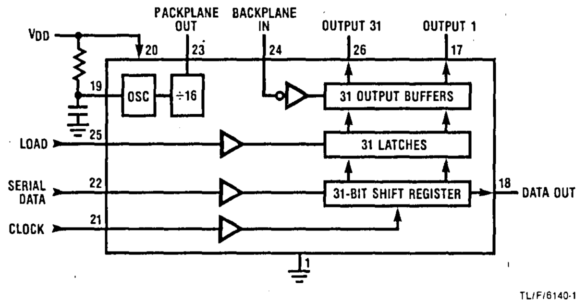
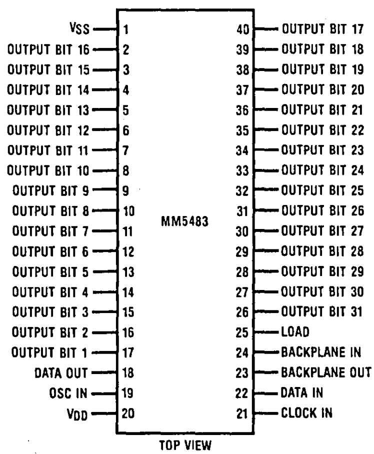


Figure 1.

Dual-in-Line Package



Order Number MM5483N
See NS Package N40A

Figure 2.

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}+10V$	Power Dissipation	300 mW at +85°C 350mW at +25°C
Operating Temperature	−40°C to +85°C	Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating range, $V_{DD}=3.0V$ to 10V, $V_{SS}=0V$, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply		3.0		10	V
Power Supply Current	R = 1M, C = 470pF, Outputs Open				
	$V_{DD}=3.0V$		9	15	μA
	$V_{DD}=5.0V$		17	25	μA
	$V_{DD}=10.0V$		35	45	μA
	OSC = 0V, Outputs Open, BPIN = 32Hz, $V_{DD}=3.0V$		1.5	2.5	μA
Clock Frequency	$V_{DD}=3.0V$			500	kHz
Input Voltage Levels	Load, Clock, Data				
Logic "0"	$V_{DD}=5.0V$			0.9	V
Logic "1"	$V_{DD}=5.0V$	2.4			V
Logic "0"	$V_{DD}=3.0V$			0.4	V
Logic "1"	$V_{DD}=3.0V$	2.0			V
Output Current Levels					
Segments and Data Out					
Sink	$V_{DD}=3.0V$, $V_{OUT}=0.3V$	20			μA
Source	$V_{DD}=3.0V$, $V_{OUT}=2.7V$	20			μA
BPOUT					
Sink	$V_{DD}=3.0V$, $V_{OUT}=0.3V$	320			μA
Source	$V_{DD}=3.0V$, $V_{OUT}=2.7V$	320			μA
Output Offset Voltage	Segment Load = 250pF BP Load = 8,750pF			±50	mV

AC Electrical Characteristics

$V_{DD} \geq 4.7V$, $V_{SS}=0$.

Symbol	Parameter	Min	Typ	Max	Units
t_{CH}	Clock Period High	500			ns
t_{CL}	Clock Period Low	500			ns
t_r	Clock Rise Time			300	ns
t_f	Clock Fall Time			300	ns
t_{DS}	Data Set-Up Before Clock	300			ns
t_{DH}	Data Hold Time After Clock	100			ns
t_{LW}	Minimum Load Pulse Width	500			ns
t_{LTC}	Load to Clock	400			ns
t_{CDO}	Clock to Data Valid		400	750	ns

Functional Description

A block diagram for the MM5483 is shown in *Figure 1* and a package pinout is shown in *Figure 2. Figure 3* shows a possible 3-wire connection system with a typical signal format for *Figure 3.* Shown in *Figure 4*, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in *Figure 5.* In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to "walk" across the display in the 2-wire mode. An AC timing diagram can be seen in *Figure 6.* It should be noted that data out is not a TTL-compatible output.

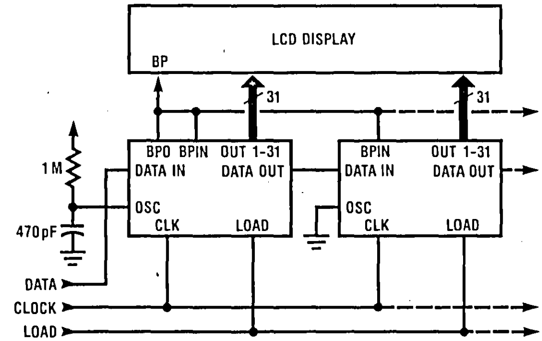


Figure 3. Three-Wire Control Mode

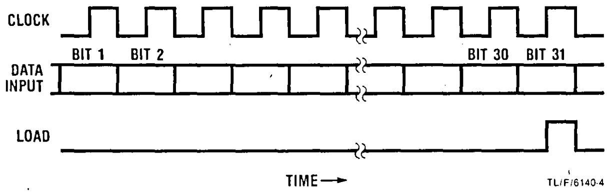


Figure 4. Data Format Diagram

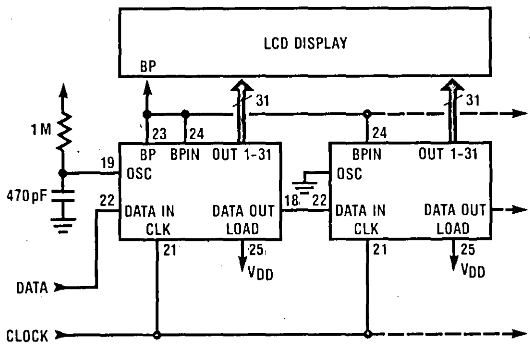


Figure 5. Two-Wire Control Mode

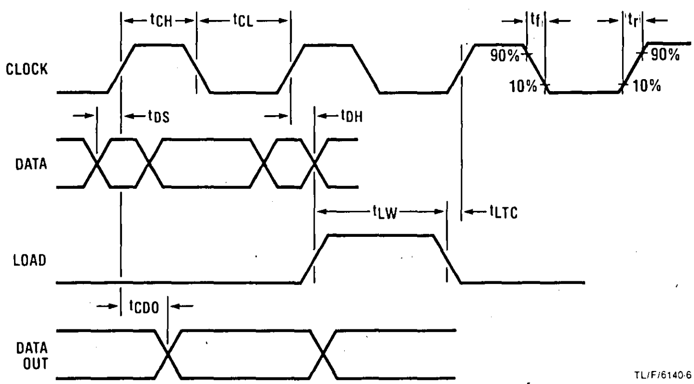


Figure 6. Timing Diagram

National Semiconductor

MM58201 Multiplexed LCD Driver

General Description

The MM58201 is a monolithic CMOS LCD driver capable of driving up to 8 backplanes and 24 segments. A 192-bit RAM stores the data for the display. Serial input and output pins are provided to interface with a controller. An RC oscillator generates the timing necessary to refresh the display. The magnitude of the driving waveforms can be adjusted with the V_{TC} input to optimize display contrast. Four additional bits of RAM allow the user to program the number of backplanes being driven, and to designate the driver as either a master or slave for cascading purposes. When two or more drivers are cascaded, the master chip drives the backplane lines, and the master and each slave chip drive 24 segment lines. Synchronizing the cascaded drivers is accomplished by tying the RC OSC pins together and the BP1 pins together.

The MM58201 is packaged in a 40-lead dual-in-line package.

Features

- Drives up to 8 backplanes and 24 segment lines
- Stores data for display
- Cascadable
- Low power
- Fully static operation

Applications

- Dot matrix LCD driver
- Multiplexed 7-segment LCD driver
- Serial in/serial out memory

Block Diagram

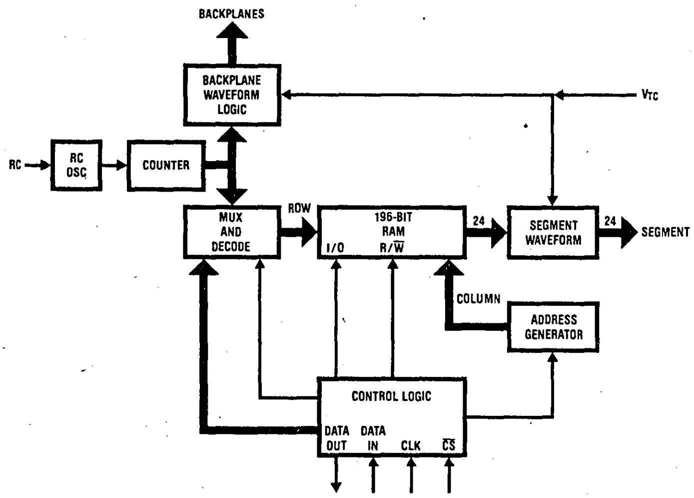


FIGURE 1. MM58201 Functional Diagram

Connection Diagram

Dual-In-Line Package

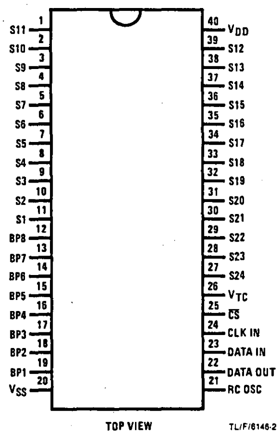


FIGURE 2

Order Number MM58201D or MM58201N
See NS Package D40C or N40A

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{SS} + 18V$
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 7.0V$ to $V_{SS} + 18.0V$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

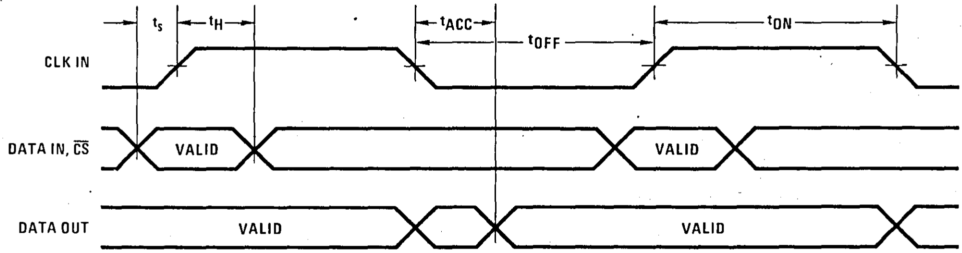
Parameter		Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Supply Current				0.3	mA
$V_{IN(1)}$	Logical "1" Input Voltage		$0.45\ V_{DD}$		$V_{DD} + 0.3$	V
$V_{IN(0)}$	Logical "0" Input Voltage		$V_{SS} - 0.3$		1.0	V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{SINK} = 0.6$ mA			0.4	V
$I_{OUT(1)}$	Logical "1" Output Leakage Current	$V_{OUT} = V_{DD}$	0		±10	μA
$I_{IN(1)}$	Logical "1" Input Leakage Current	$V_{IN} = V_{DD}$	0		1.0	μA
$I_{IN(0)}$	Logical "0" Input Leakage Current	$V_{IN} = V_{SS}$	−1.0		0	μA
V_{TC}	Input Voltage		4.5		$V_{DD} + 0.3$	V
V_{TC}	Input Impedance		10		30	kΩ
Z_{OUT}	Output Impedance	Backplane and Segment Outputs			10	kΩ
	DC Offset Voltage	Between Any Backplane and Segment Output	0		±10	mV

AC Electrical Characteristics T_A and V_{DD} within operating range unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator Frequency*		128η		400η	Hz
$f_{CLK\ IN}$	Clock Frequency		DC		100	kHz
t_{ON}	Clock Pulse Width		5.0			μs
t_{OFF}	Clock OFF Time		5.0			μs
t_s	Input Data Set-Up Time		2.0			μs
t_H	Input Data Hold Time		1.0			μs
t_{ACC}	Access Time		5.0			μs
t_r	Rise Time	Backplane, Segment Outputs $C_L = 2000$ pF			60	μs
t_f	Fall Time	Backplane, Segment Outputs $C_L = 2000$ pF			60	μs

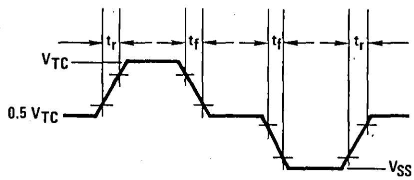
* η is the number of backplanes programmed.

Switching Time Waveforms



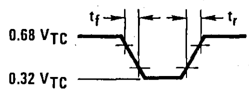
TL/F/6146-3

Backplane Output



TL/F/6146-4

Segment Output



TL/F/6146-5

Functional Description

A functional diagram of the MM58201 LCD driver is shown in *Figure 1*. A connection diagram is shown in *Figure 2*.

Serial Inputs and Output

A negative-going edge on the $\overline{CS}$ input initiates a frame. The $\overline{CS}$ input must then stay low for at least one rising edge of CLK IN, and may not be pulsed low again for the next 31 clocks. At least one clock must occur while $\overline{CS}$ is high. If CLK IN is held at a logic "1", $\overline{CS}$ is disabled. This allows the signal that drives $\overline{CS}$ to be used for other purposes when the MM58201 is not being addressed.

CLK IN latches data from the DATA IN input on its rising edge. Data from the DATA OUT pin changes on the falling edge of CLK IN and is valid before the next rising edge.

The first five bits of data following $\overline{CS}$ are the address bits *(Figure 3)*. The address selects the column where the operation is to start. Bit 1 is the MSB and bit 5 is the LSB. The sixth bit is the read/write bit. A logic "1" specifies a read operation and a logic "0" specifies a write operation. Tne next 24 bits are the data bits. The first data bit corresponds to the BP1 row of the display, the second data bit to the BP2 row, and so on. After the eighth and sixteenth data bits, the column pointer is incremented. When starting address 10110 or 10111 is specified, the column pointer increments from 10111 to 00000.

During a read or write cycle, the LCD segment outputs do not reflect the data in the RAM. To avoid disrupting the pattern viewed on the display, the read or write cycle time should be kept short. Since the LCD turn-on time can be as little as 30 ms, a clock rate of at least 10 kHz would be required in order to address the entire contents of the RAM within that time interval. The formula below can be used to estimate the minimum clock rate:

$$f_{CLK\ IN} = \frac{30}{(t_{LCD} - 7t_S)}$$

where t_s is the processor's set-up time between each read or write cycle, and t_{LCD} is the minimum turn-on or turn-off time of the LCD as specified by the LCD manufacturer.

The DATA OUT output is an open drain N-channel device to V_{SS} *(Figure 4)*. With an external pull-up this configuration allows the controller to operate at a lower supply voltage, and also permits the DATA OUT output to be wired in parallel with the DATA OUT outputs from any other drivers in the system.

To program the number of backplanes being driven and the M/$\overline{S}$ bit, load address 11000, a write bit, three bits for the number of backplanes (Table I), and the M/$\overline{S}$ bit. The remaining 20 data bits will be ignored but it is necessary to provide 21 more clocks before initiating another frame.

TABLE I. BACKPLANE SELECT

Number of Backplanes	B2	B1	B0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

Functional Description (Continued)

RC OSC Pin

This oscillator generates the timing required for multiplexing the liquid crystal display. The oscillator operates at a frequency that is 4η times the refresh rate of the display, where η is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency must be:

$$128\eta \leq f_{OSC} \leq 400\eta$$

The frequency of oscillation is related to the external R and C components in the following way:

$$f_{OSC} = \frac{1}{1.25\ RC} \pm 30\%$$

The value used for the external resistor should be in the range from 10 kΩ to 1 MΩ.

The value used for the external capacitor should be less than 0.005 μF.

V_{TC} Pin

The V_{TC} pin is an analog input that controls the contrast of the segments on the LCD. If eight backplanes are being driven ($\eta = 8$), a voltage of typically 8V is required at 25°C. The voltage for optimum contrast will vary from display to display. It also has a significant negative temperature coefficient.

The voltage source on the V_{TC} input must be of relatively low impedance since the input impedance of V_{TC} ranges from 10 kΩ to 30 kΩ. A suitable circuit is shown in *Figure 5.*

In a standby mode, the V_{TC} input can be set to V_{SS}. This reduces the supply current to less than 300 μA per driver.

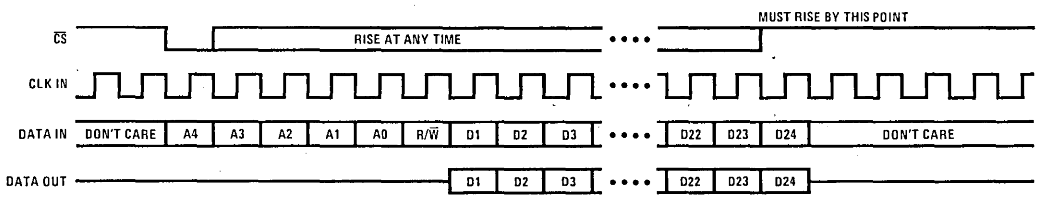
Backplane and Segment Outputs

Connect the backplane and segment outputs directly to the LCD row and column lines. The outputs are designed to drive a display with a total ON capacitance of up to 2000 pF.

The output structure consists of transmission gates tapped off of a resistor string driven by V_{TC} *(Figure 6).*

A critical factor in the lifetime of an LCD is the amount of DC offset between a backplane and segment signal. Typically, 50 mV of offset is acceptable. The MM58201 guarantees an offset of less than 10 mV.

The BP1 output is disabled when the M/$\overline{S}$ bit is set to zero. This allows the BP1 output from the master chip to be connected directly to it so that synchronizing signals can be generated. Synchronization occurs once each refresh cycle, so the cascaded chips are assured of remaining synchronized.



	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	
BP1													D1	D9	D17										B2
BP2													D2	D10	D18										B1
BP3													D3	D11	D19										B0
BP4													D4	D12	D20										M/$\overline{S}$
BP5													D5	D13	D21										
BP6													D6	D14	D22										
BP7													D7	D15	D23										
BP8													D8	D16	D24										
A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Diagram above shows where data will appear on display if starting address 01100 is specified in data format. TL/F/6146-6

FIGURE 3. Data Format

Functional Description (Continued)

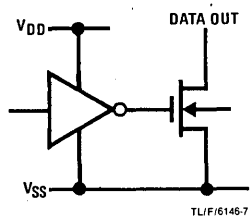


FIGURE 4. DATA OUT Structure

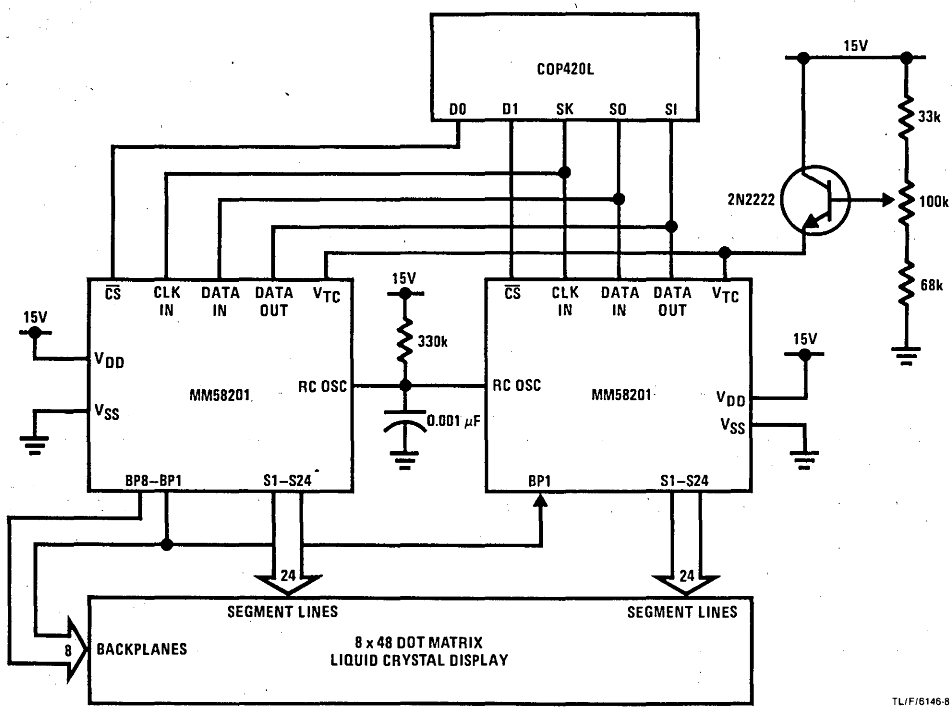


FIGURE 5. Typical Application

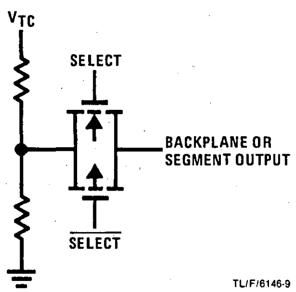


FIGURE 6. Structure of LCD Outputs

National Semiconductor

PRELIMINARY

MM58241 High Voltage Display Driver

General Description

The MM58241 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58241 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 32-digit alphanumeric or dot matrix display).

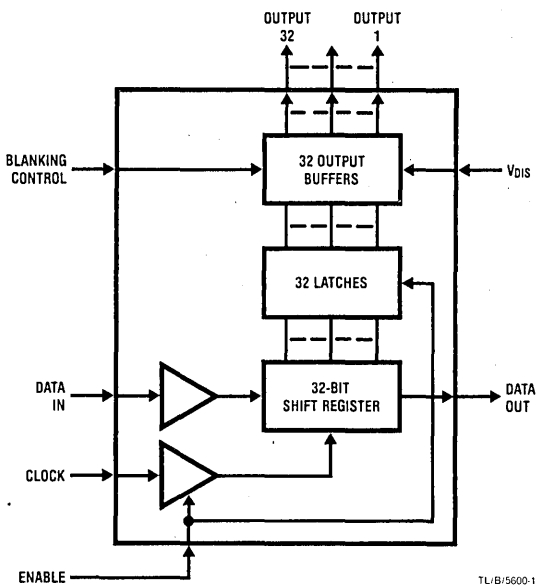
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- TTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

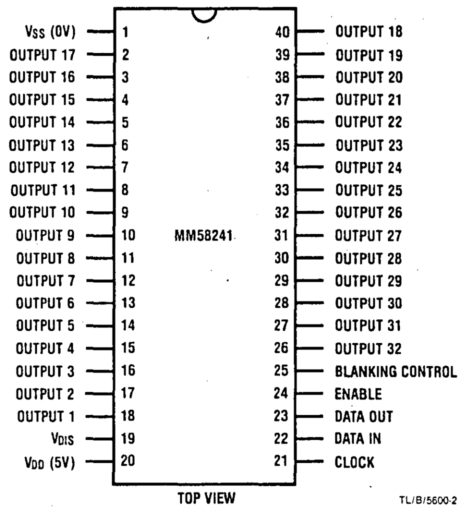
Block and Connection Diagrams



TL/B/5600-1

FIGURE 1

Dual-In-Line Package



TL/B/5600-2

FIGURE 2

Order Number MM58241N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-60V$
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	+130°C
Lead Temperature (Soldering, 10 seconds)	+300°C

DC Electrical Characteristics $T_A = -40°C$ to $+85°C$

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltages					
V_{DD}	$V_{SS}=0V$	4.5		5.5	V
V_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$	−55		−25	V
Power Supply Currents					
I_{DD}	$V_{DD}=5V$, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$, $V_{DIS}=-55V$, All Outputs Off			10	mA
Input Logic Levels DATA IN, CLOCK, ENABLE, BLANK	$V_{SS}=0V$				
Logic '0'	$V_{DD}=5V\pm0.5V$	V_{SS}		0.8	V
Logic '1'	$V_{DD}=4.5V$	2.0		V_{DD}	V
Logic '1'	$V_{DD}=5.5V$	2.4		V_{DD}	V
Input Currents DATA IN, CLOCK, ENABLE, BLANK	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$			10	μA
Input Capacitance DATA IN, CLOCK, ENABLE, BLANK	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$			15	pF
Data Output Impedance	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$				
Output High	Resistance to V_{DD}			2.0	kΩ
Output Low	Resistance to V_{SS}			700	Ω
Display Output Impedances	$V_{DD}=5V$, $V_{SS}=0V$				
Output Off (*Figure 3a*)	$V_{DIS}=-25V$	80		400	kΩ
	$V_{DIS}=-40V$	100		550	kΩ
	$V_{DIS}=-55V$	110		650	kΩ
Output On (*Figure 3b*)	$V_{DIS}=-25V$		2.5	3.0	kΩ
	$V_{DIS}=-40V$		2.2	2.7	kΩ
	$V_{DIS}=-55V$		2.0	2.5	kΩ
Display Output Leakage	$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-55V$		10	20	μA

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input					
Frequency, f_C				800	kHz
Rise Time, t_r				200	ns
Fall Time, t_f				200	ns
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input					
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output					
CLOCK Low to Data Out Time, t_{CDO}				500	ns

Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58241 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58241 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58241 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following ENABLE high. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58241, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58241.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'-'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58241, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58241 is used to provide the grid drive for a 32-digit 5 × 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.

Functional Description (Continued)

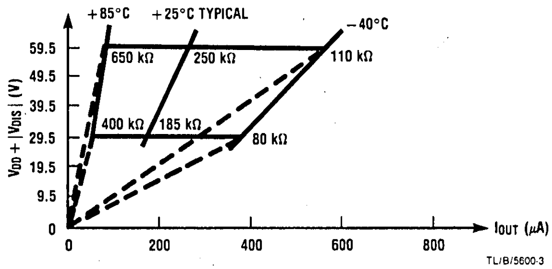


FIGURE 3a. Output Impedance Off

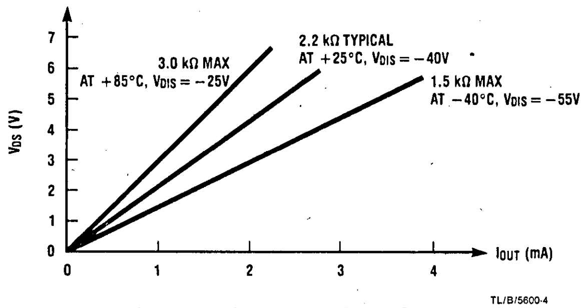
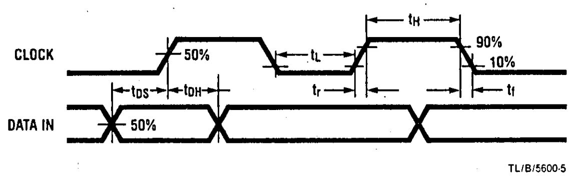


FIGURE 3b. Output Impedance On

Timing Diagrams



For the purposes of AC measurements, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings

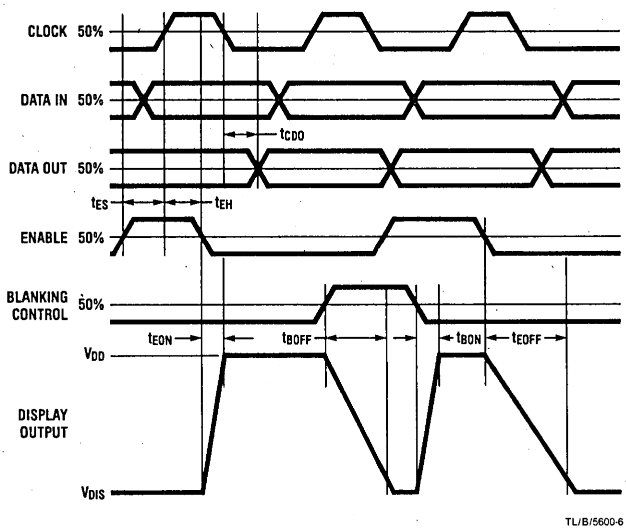


FIGURE 5. MM58241 Timings (Data Format)

Typical Application

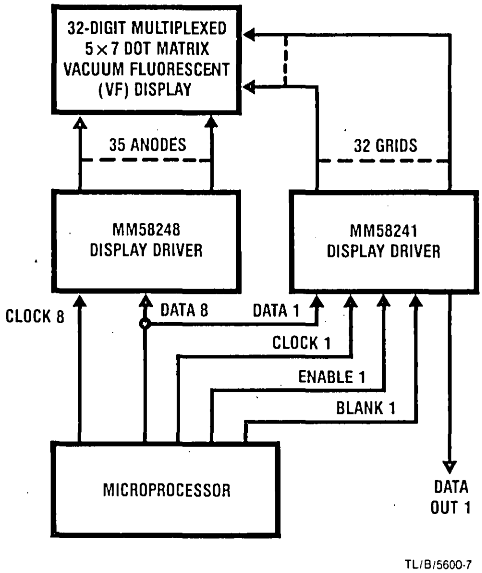


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58248 High Voltage Display Driver

General Description

The MM58248 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58248 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 5 × 7 dot matrix display).

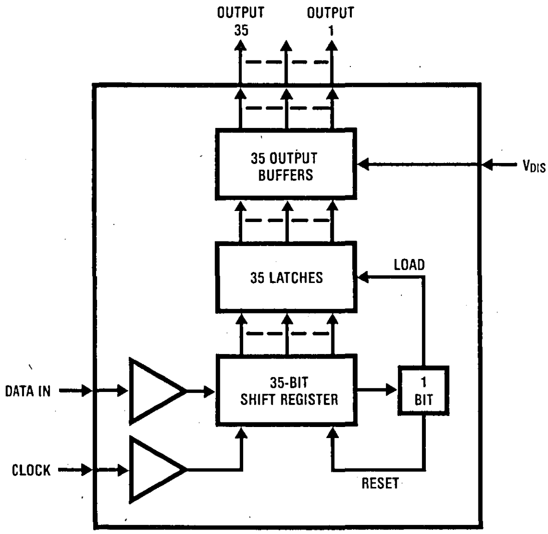
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- TTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

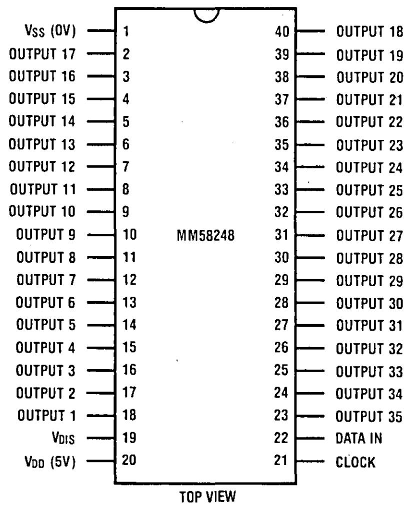
Block and Connection Diagrams



TL/B/5599-1

FIGURE 1

Dual-In-Line Package



TL/B/5599-2

FIGURE 2

Order Number MM58248N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-60V$
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	+130°C
Lead Temperature (Soldering, 10 seconds)	+300°C

DC Electrical Characteristics $T_A = -40°C$ to $+85°C$

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltages					
V_{DD}	$V_{SS}=0V$	4.5		5.5	V
V_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$	−55		−25	V
Power Supply Currents					
I_{DD}	$V_{DD}=5V$, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$, $V_{DIS}=-55V$, All Outputs Off			10	mA
Input Logic Levels	$V_{SS}=0V$				
DATA IN, CLOCK					
Logic '0'	$V_{DD}=5V\pm0.5V$	V_{SS}		0.8	V
Logic '1'	$V_{DD}=4.5V$	2.0		V_{DD}	V
Logic '1'	$V_{DD}=5.5V$	2.4		V_{DD}	V
Input Currents DATA IN, CLOCK	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$			10	μA
Input Capacitance DATA IN, CLOCK	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$			15	pF
Display Output Impedances	$V_{DD}=5V$, $V_{SS}=0V$				
Output Off (*Figure 3a*)	$V_{DIS}=-25V$	80		400	kΩ
	$V_{DIS}=-40V$	100		550	kΩ
	$V_{DIS}=-55V$	110		650	kΩ
Output On (*Figure 3b*)	$V_{DIS}=-25V$		2.5	3.0	kΩ
	$V_{DIS}=-40V$		2.2	2.7	kΩ
	$V_{DIS}=-55V$		2.0	2.5	kΩ
Display Output Leakage	$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-55V$		10	20	μA

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

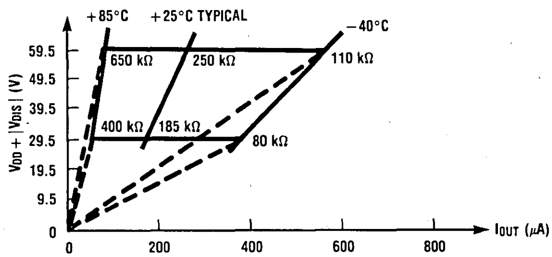
Parameter	Conditions	Min	Typ	Max	Units
Clock Input					
Frequency, f_C				1.0	MHz
Rise Time, t_r				200	ns
Fall Time, t_f				200	ns
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58248 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58248 is shown in *Figure 1.*

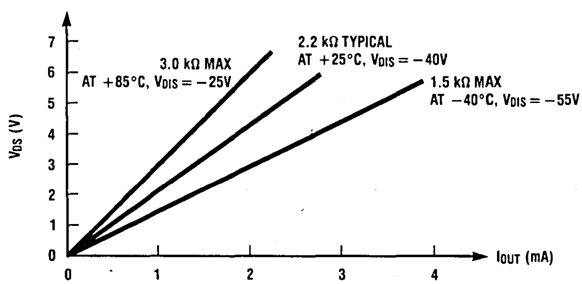
Figure 2 shows the pinout of the MM58248 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following the start bit. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by the use of the MM58248, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.



TL/B/5599-3

FIGURE 3a. Output Impedance Off



TL/B/5599-4

FIGURE 3b. Output Impedance On

Functional Description (Continued)

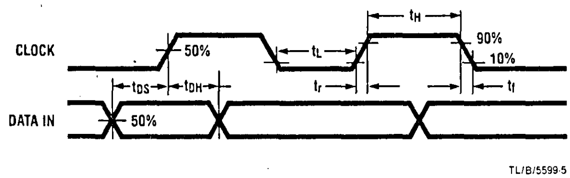
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58248.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of the start bit and the first clock pulse, and so all interface signals should be inactive at power on.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'-'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58248, or the shift register will not clear. If, at any given time, it is required that the display be cleared under microprocessor control, i.e., without power on reset, then the following flushing routine may be used. Clock in 36 'zeroes', followed by a 'one' (start bit), followed by 35 'zeroes'. This procedure will completely blank the display.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58248 is used to provide the anode drive for a 32-digit 5 × 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58241, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

Timing Diagrams



For the purposes of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$

FIGURE 4. Clock and Data Timings

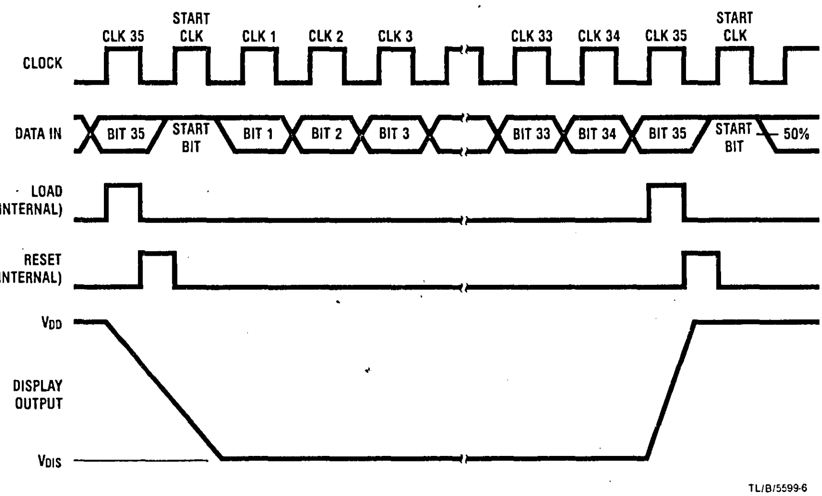


FIGURE 5. MM58248 Timings (Data Format)

Typical Application

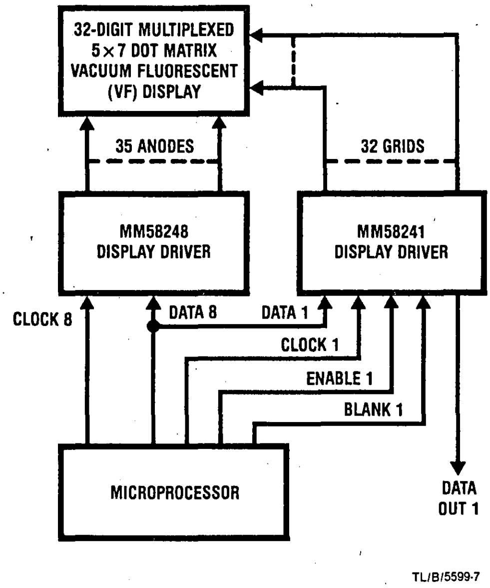


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58270 Display Driver

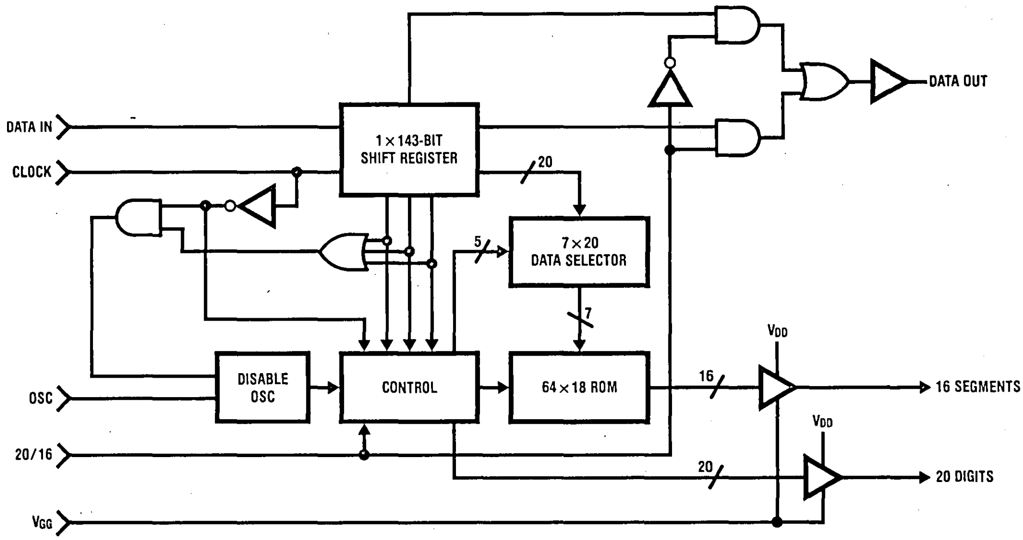
General Description

The MM58270 multiplex vacuum fluorescent display driver is a monolithic metal gate CMOS circuit with bipolar output transistors to achieve high source current drive at high voltage. On-chip pull-down resistors minimize external components. This circuit is capable of driving a 16 or 20-digit display (40 or 44-pin package). The display font is 14-segment (British Flag) plus comma and decimal point.

Features

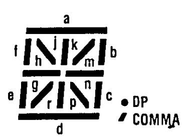
- Up to 20-digit display
- 10 mA source current
- Interdigit blanking
- Digital brightness control
- 16-segment font
- Serial input

Block Diagram



TL/F/6150-2

Font Structure

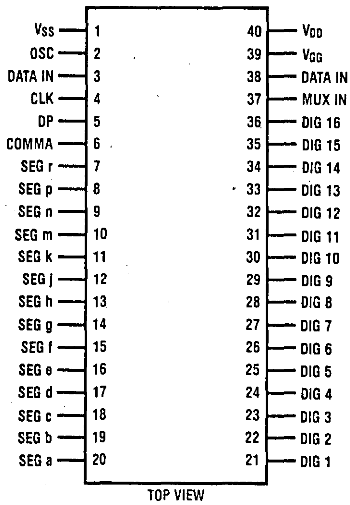


TL/F/6150-1

8

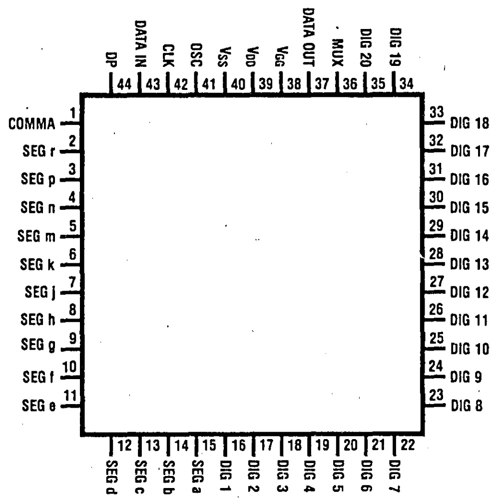
Connection Diagrams

Dual-In-Line Package



Order Number MM58270N
See NS Package N40A

Quad Package



Package Information Not
Available at This Time

National Semiconductor

PRELIMINARY

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display)

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- TTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams

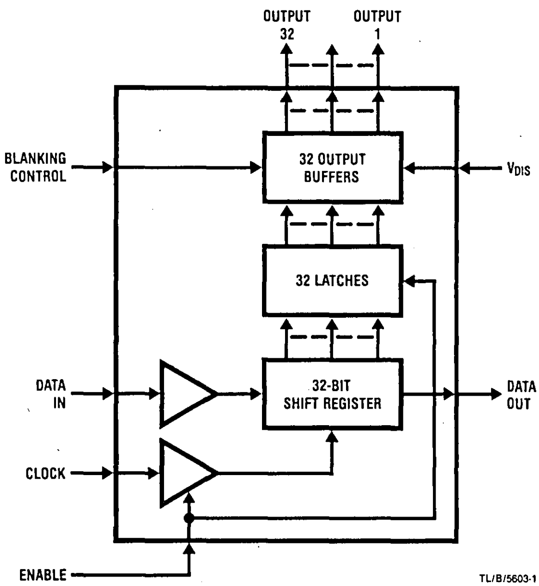


FIGURE 1

Dual-In-Line Package

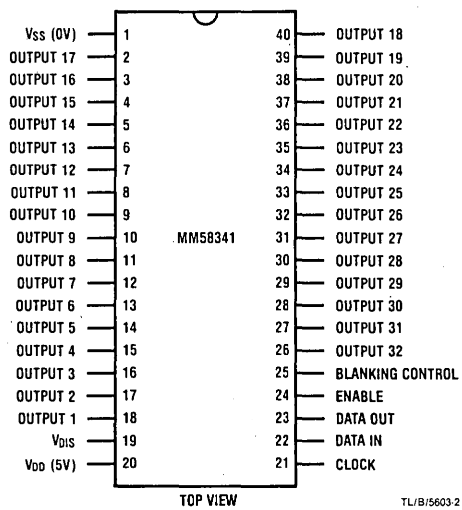


FIGURE 2

Order Number MM58341N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-35V$
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = -40°C$ to $+85°C$

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltages					
V_{DD}	$V_{SS}=0V$	4.5		5.5	V
V_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$	−30		−10	V
Power Supply Currents					
I_{DD}	$V_{DD}=5V$, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$, $V_{DIS}=-30V$, All Outputs Off			10	mA
Input Logic Levels DATA IN, CLOCK, ENABLE, BLANK	$V_{SS}=0V$				
Logic '0'	$V_{DD}=5V\pm0.5V$	V_{SS}		0.8	V
Logic '1'	$V_{DD}=4.5V$	2.0		V_{DD}	V
Logic '1'	$V_{DD}=5.5V$	2.4		V_{DD}	V
Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$			10	μA
Input Capacitance DATA IN, CLOCK ENABLE, BLANK	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$			15	pF
Data Output Impedance	$V_{DD}=5V\pm0.5V$, $V_{SS}=0V$				
Output High	Resistance to V_{DD}			2.0	kΩ
Output Low	Resistance to V_{SS}			700	Ω
Display Output Impedances	$V_{DD}=5V$, $V_{SS}=0V$				
Output Off (*Figure 3a*)	$V_{DIS}=-10V$	55		250	kΩ
	$V_{DIS}=-20V$	60		300	kΩ
	$V_{DIS}=-30V$	65		400	kΩ
Output On (*Figure 3b*)	$V_{DIS}=-10V$		550	650	Ω
	$V_{DIS}=-20V$		500	600	Ω
	$V_{DIS}=-30V$		400	500	Ω
Display Output Leakage	$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-30V$		5	2.0	μA

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input					
Frequency, f_C				800	kHz
Rise Time, t_r				200	ns
Fall Time, t_f				200	ns
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input					
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output					
Clock Low to Data Out Time, t_{CDO}				500	ns

Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58341 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58341 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58341 device, where output 1 (pin 18) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58341, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58341.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'-'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58341, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58341 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

Functional Description (Continued)

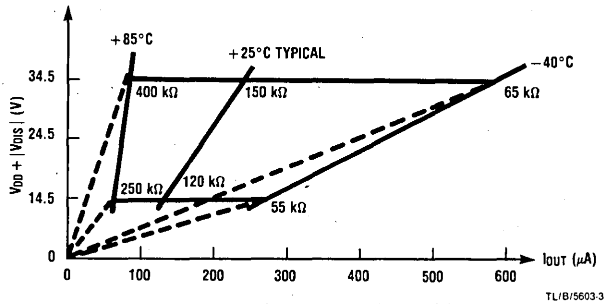


FIGURE 3a. Output Impedance Off

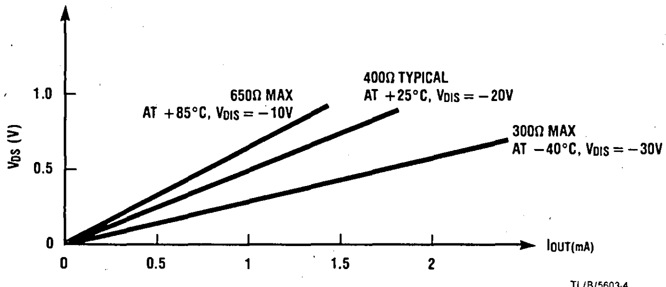
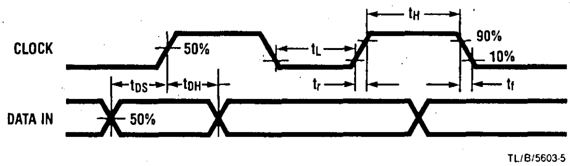


FIGURE 3b. Output Impedance On

Timing Diagrams



For the purposes of AC measurements, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings

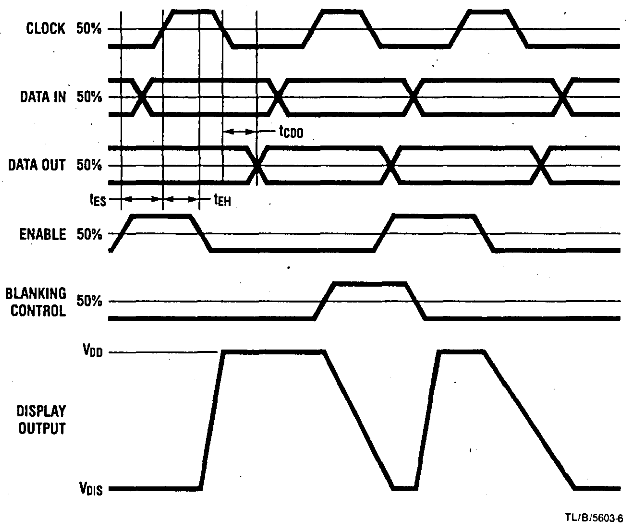


FIGURE 5. MM58341 Timings (Data Format)

Typical Application

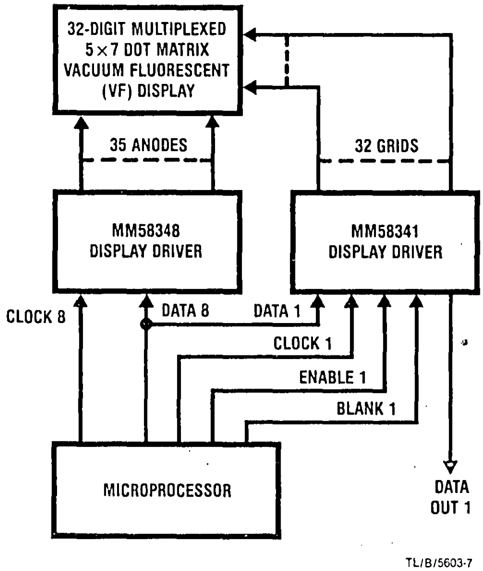


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58348 High Voltage Display Driver

General Description

The MM58348 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58348 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 5×7 dot matrix display).

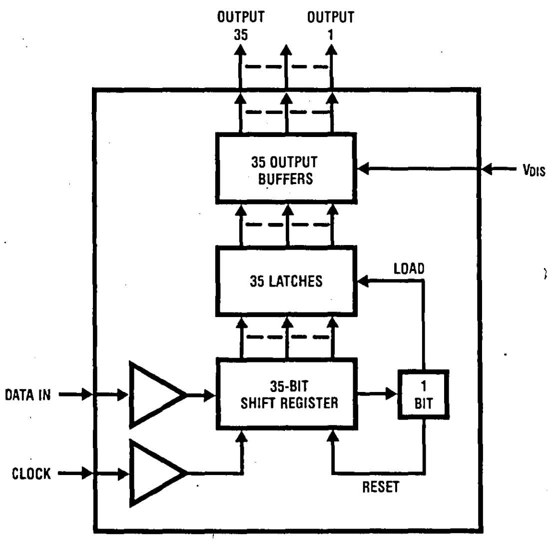
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- TTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

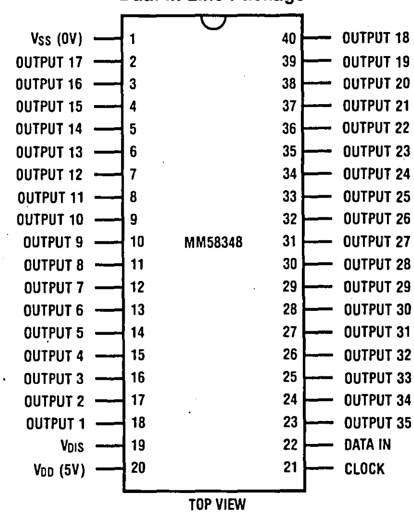
Block and Connection Diagrams



TL/B/5601-1

FIGURE 1

Dual-In-Line Package



TL/B/5601-2

FIGURE 2

Order Number MM58348N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-35V$
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = -40°C$ to $+85°C$

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltages					
V_{DD}	$V_{SS}=0V$	4.5		5.5	V
V_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$	−30		−10	V
Power Supply Currents					
I_{DD}	$V_{DD}=5V$, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}	$V_{DD}=5V$, $V_{SS}=0V$, $V_{DIS}=-30V$, All Outputs Off			10	mA
Input Logic Levels DATA IN, CLOCK	$V_{SS}=0V$				
Logic '0'	$V_{DD}=5V \pm 0.5V$	V_{SS}		0.8	V
Logic '1'	$V_{DD}=4.5V$	2.0		V_{DD}	V
Logic '1'	$V_{DD}=5.5V$	2.4		V_{DD}	V
Input Currents DATA IN, CLOCK	$V_{DD}=5V \pm 0.5V$, $V_{SS}=0V$			10	μA
Input Capacitance DATA IN, CLOCK	$V_{DD}=5V \pm 0.5V$, $V_{SS}=0V$			15	pF
Display Output Impedances	$V_{DD}=5V$, $V_{SS}=0V$				
Output Off (*Figure 3a*)	$V_{DIS}=-10V$	55		250	kΩ
	$V_{DIS}=-20V$	60		300	kΩ
	$V_{DIS}=-30V$	65		400	kΩ
Output On (*Figure 3b*)	$V_{DIS}=-10V$		550	650	Ω
	$V_{DIS}=-20V$		500	600	Ω
	$V_{DIS}=-30V$		400	500	Ω
Display Output Leakage	$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-30V$	5		20	μA

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

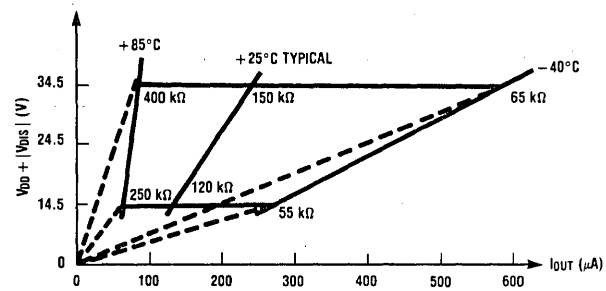
Parameter	Conditions	Min	Typ	Max	Units
Clock Input					
Frequency, f_C				1.0	MHz
Rise Time, t_r				200	ns
Fall Time, t_f				200	ns
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58348 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58348 is shown in *Figure 1.*

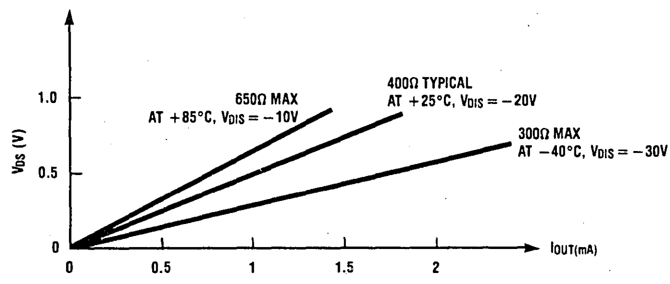
Figure 2 shows the pinout of the MM58348 device, where output 1 (pin 18) is equivalent to bit 1, (i.e., the first bit of data to be loaded into the shift register following the start bit). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58348, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.



TL/B/5601-3

FIGURE 3a. Output Impedance Off



TL/B/5601-4

FIGURE 3b. Output Impedance On

Functional Description (Continued)

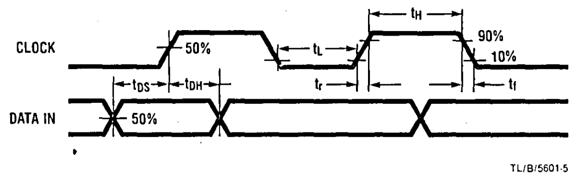
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58348.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of the start bit and the first clock pulse, and so all interface signals should be inactive at power on.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'-'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58348, or the shift register will not clear. If, at any given time, it is required that the display be cleared under microprocessor control, i.e., without power on reset, then the following flushing routine may be used. Clock in 36 'zeroes', followed by a 'one' (start bit), followed by 35 'zeroes'. This procedure will completely blank the display.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58348 is used to provide the anode drive for a 32-digit 5 × 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58341, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

Timing Diagrams



For the purpose of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$

FIGURE 4. Clock and Data Timings

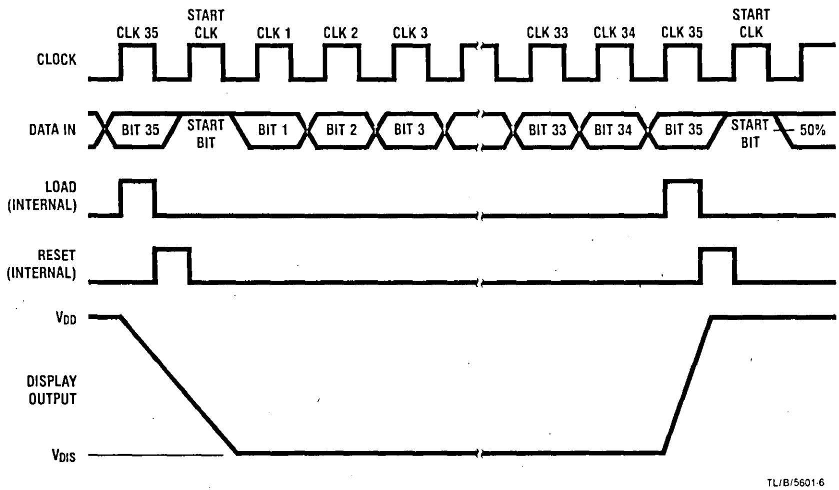


FIGURE 5. MM58348 Timings (Data Format)

Typical Application

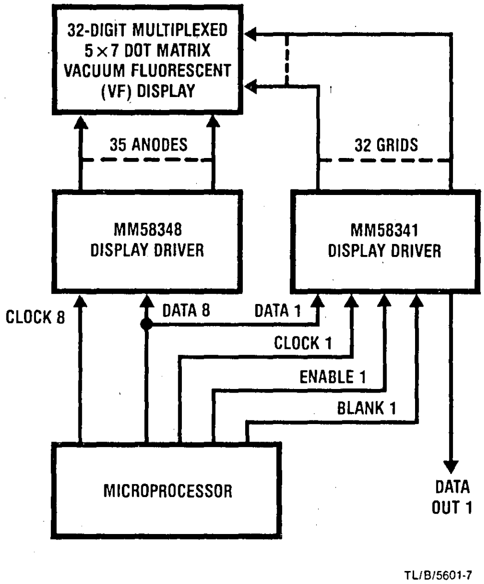


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58438 32-Bit LCD Display Driver

General Description

The MM58438 is a CMOS metal gate circuit which is capable of driving up to 32 LCD segments and is available in a 40-pin molded package. In addition, MM58438 dice is available for PCB module assembly systems. The circuit requires a minimum of interface between data source and display and can be cascaded where larger displays are required.

Features

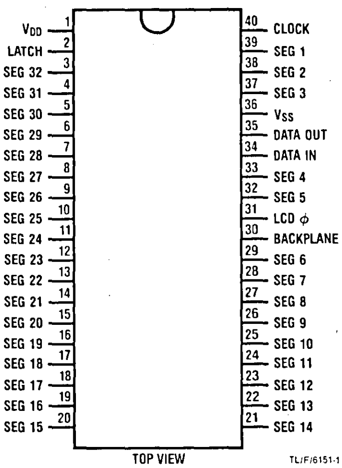
- Serial data input
- 32 segment outputs
- Cascaded operation capability
- Alphanumeric and bar graph capability
- TTL compatibility
- Non-multiplex display
- Compatible with HLCD 0438, HLCD 0438A
- Stable oscillator only requires one external component

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Digital clock, thermometer, counter, voltmeter displays
- Industrial control indicator
- Serial to parallel converter

Connection Diagram

Dual-In-Line Package



Order Number MM58438N
See NS Package N40A

Block Diagram

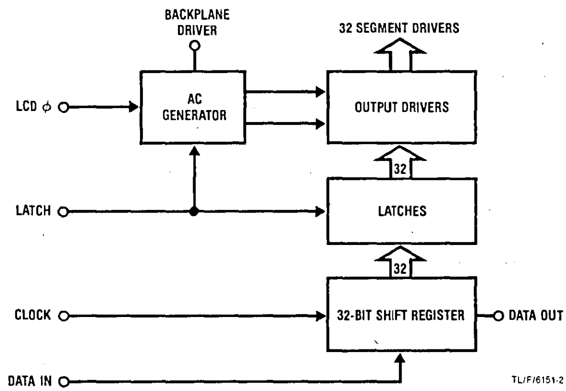


FIGURE 1

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
V_{DD} Supply Voltage	18V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_{DD}=3.0V$ to 15V, $T_A=-40°C$ to $+85°C$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{DD}		3.0		15	V
Supply Current I_{DD}	Oscillating or Driven Mode, $V_{DD}=5V$			60	μA
Input High Level V_{IH}	$V_{DD}=4.5V$ to 5.5V	2.4		V_{DD}	V
	$V_{DD}=5.5V$ to 15V	0.5 V_{DD}		V_{DD}	V
Input Low Level V_{IL}	$V_{DD}=4.5V$ to 5.5V	0		0.8	V
	$V_{DD}=5.5V$ to 15V	0		0.1 V_{DD}	V
Input Current (Any Input)				±10	μA
Input Capacitance				10	pF
Output Current Levels					
Segments					
Sink I_{OL}	$V_{DD}=4.5V$, $V_{OUT}=0.2V$	20			μA
Source I_{OH}	$V_{DD}=4.5V$, $V_{OUT}=V_{DD}-0.2V$	20			μA
Backplane					
Sink I_{OL}	$V_{DD}=4.5V$, $V_{OUT}=0.2V$	320			μA
Source I_{OH}	$V_{DD}=4.5V$, $V_{OUT}=V_{DD}-0.2V$	320			μA
Output Offset Voltage	Segment Capacitance = 250 pF				
	Backplane Capacitance = 8750 pF			±50	mV
Data Output					
Sink	$V_{DD}=4.5V$, $V_{OUT}=0.5V$			−100	μA
Source	$V_{DD}=4.5V$, $V_{OUT}=V_{DD}-0.5V$	100			μA

AC Electrical Characteristics $V_{DD}=3.0V$ to 15V, $T_A=-40°C$ to $+85°C$ unless otherwise specified *(Figure 2)*

Parameter	Conditions	Min	Typ	Max	Units
t1 Data Hold Time		0.1			μs
t2 Data Set-Up Time		0.1			μs
t3 Latch Pulse Width		1			μs
t4 Clock to Latch Time		0.1			μs
t_{pd} Data Out Delay				500	ns
Clock Frequency f		DC		500	kHz
Clock Period t(=1/f)		2			μs
Backplane Frequency	$C_{EXT}=47$ pF		100		Hz
Oscillator Stability	$V_{DD}=5V$			±50	%
V_{DD} Rise Time	0V to 5V	5			ms

Functional Description

The connection diagram for the MM58438 is shown on the first page. The circuit is designed to drive LCD displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, SERIAL DATA, CLOCK and LATCH.

The MM58438 uses a latch mode of microprocessor data transfer whereby the signal LATCH acts as a latch to the input data *(Figure 2)*. Data is input to and output from the internal shift register on the negative clock edge (i.e., a logic '1' to logic '0' transition) while the LATCH pin is held low. The contents of the shift register are latched to the output latches and display drivers on the logic '0' to logic '1' transition of the LATCH pin when it is pulsed high.

The MM58438 can be cascaded when a larger display is required where it can be considered to be driven or oscillating.

In the oscillating mode, the BACKPLANE frequency is determined by the capacitor connected to the LCD ϕ pin. When two circuits are cascaded the second LCD ϕ input is driven by the first backplane output.

When the circuit is first powered on, an internal power on reset signal is generated which primes the mode detect logic and sets the BACKPLANE to a logical high level. If the circuit is in the oscillating mode the LCD ϕ pin is connected to a capacitor which is held low by a high impedance internal pull down transistor. If the circuit is in the driven mode the LCD ϕ pin is connected to the previous BACKPLANE output and is forced high by this low impedance output. When the first LATCH pulse goes to a logic '1', the level on the LCD ϕ pin is internally latched which indicates to the rest of the logic whether the circuit is driven or oscillating.

The oscillator on the oscillating device starts as soon as the LATCH pin goes to a logic '1'.

In the driven mode, the BACKPLANE frequency is in phase with the input frequency on the LCD ϕ.

To ensure the correct latching of this function, the LATCH input must be held at a logic '0' level for a minimum of 10 μs at power on.

Once the initial conditions on power up have been obeyed, the circuit can be used as serial to parallel converters with the polarity of the output data determined by the logic level on the LCD ϕ input. A logic '1' on the LCD ϕ input produces inverted data.

Timing Diagram

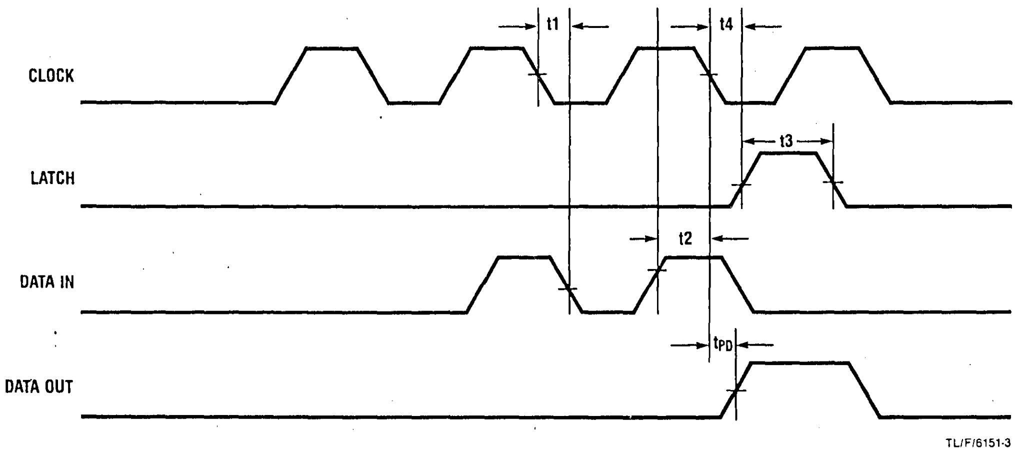


FIGURE 2

Typical Application

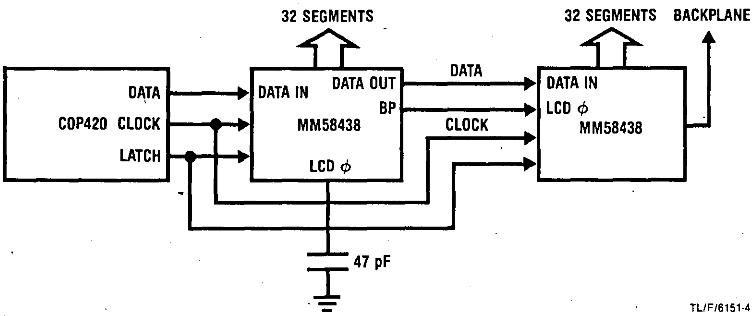


FIGURE 3. 64-Segment Display Cascading Two MM58438s

National Semiconductor

PRELIMINARY

MM58538 Multiplexed LCD Driver

General Description

The MM58538 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P- and N-channel devices, which drives an 8 row by 26 column dot matrix LCD array directly under the control of an external microprocessor. The MM58538 can be used with an MM58539 to drive a display that has up to 8 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in a 40-pin molded dual-in-line package or dice.

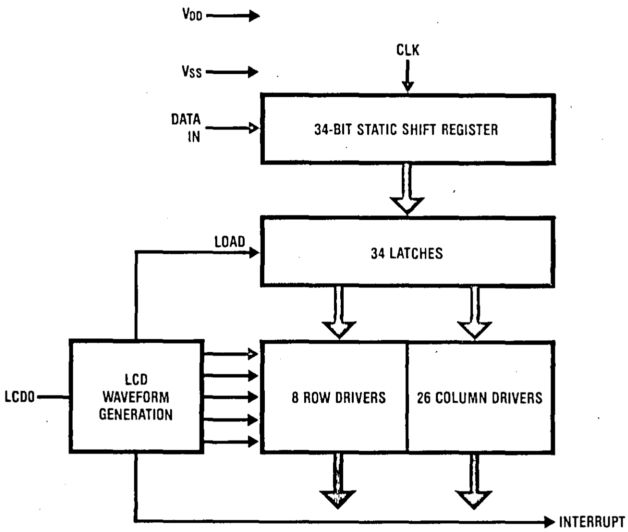
Features

- Drives up to 8 rows and 26 columns
- Expandable to larger displays with MM58539
- Flexible organization allows any display pattern
- Simple 3 line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On chip oscillator
- Compatible with HLCD 0538

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block Diagram

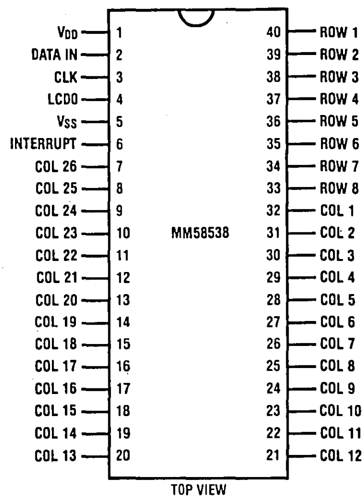


TL/B/5728-1

FIGURE 1

Connection Diagram

Dual-In-Line Package



TL/B/5728-2

FIGURE 2

Order Number MM58538N
See NS Package N40A

Absolute Maximum Ratings

Voltage at any input pin	$V_{DD} - 20V$ to $V_{DD} + 0.3V$
Voltage at any display pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Storage Temperature	$-65°C$ to $150°C$
Power Dissipation	250 mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	$-40°C$ to $70°C$

Electrical Characteristics $T = 25°C$ and $V_{DD} = 5V$ unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3		15	V
I_{DD}	Supply Current				400	μA
V_{ih}	Input High Level	All V_{DD}	.75 V_{DD}		V_{DD}	V
V_{il}	Input Low Level	All V_{DD}	$V_{DD} - 15$		.25 V_{DD}	V
I_1	Input Leakage				5	μA
C_i	Input Cap.				5	pF
V_{OH}	Row Output High	All V_{DD}			V_{DD}	V
V_{ol}	Row Output Low	All V_{DD}	V_{SS}			V
V_{om}	Row Unselected	All V_{DD}		.5V_{DD}		V
V_{oh}	Column O/P High	All V_{DD}		.68V_{DD}		V
V_{ol}	Column O/P Low	All V_{DD}		.32V_{DD}		V
V_{off}	Average DC Offset, any display element				100	mV
R_{on}	Row & Column Output Impedance	$I_1 = 10\mu A$			40	Kohm
R_{ON}	Interrupt Output Impedance	$I_1 = 100\mu A$			1	Kohm
f	Clock Frequency		DC		1.5	MHz
t_{ds}	Data-in Setup Time	Data change to clock fall	300			ns
t_{dh}	Data-in Hold Time	Clock fall to data change	100			ns
t_d	LCD0 to Int. Out Delay		300			ns
$t_{r/f}$	Clock rise/fall time				200	ns
V_{ih}	LCD0 High Level	All V_{DD}	9V_{DD}		V_{DD}	V
V_{il}	LCD0 Low Level	All V_{DD}	0		.1V_{DD}	V
R_{in}	LCD0 Input Impedance		1		3	Mohm

Functional Description

A block diagram of the MM58538 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This Interrupt signal also acts as a refresh request and new data must be loaded before the next Interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 7 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for an MM58538 together with an MM58539 in *Figure 3*. Rows generated from the MM58538 are out of phase with Interrupt if selected and at mid point voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns generated from both the MM58538 and the MM58539 are in phase with Interrupt if selected and out of phase if not selected; levels are $0.32V_{DD}$ and $0.68V_{DD}$. Backplanes, i.e., rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimise LCD contrast or for temperature compensation it is recommended that all positive supply terminals be connected together and the negative supply varied.

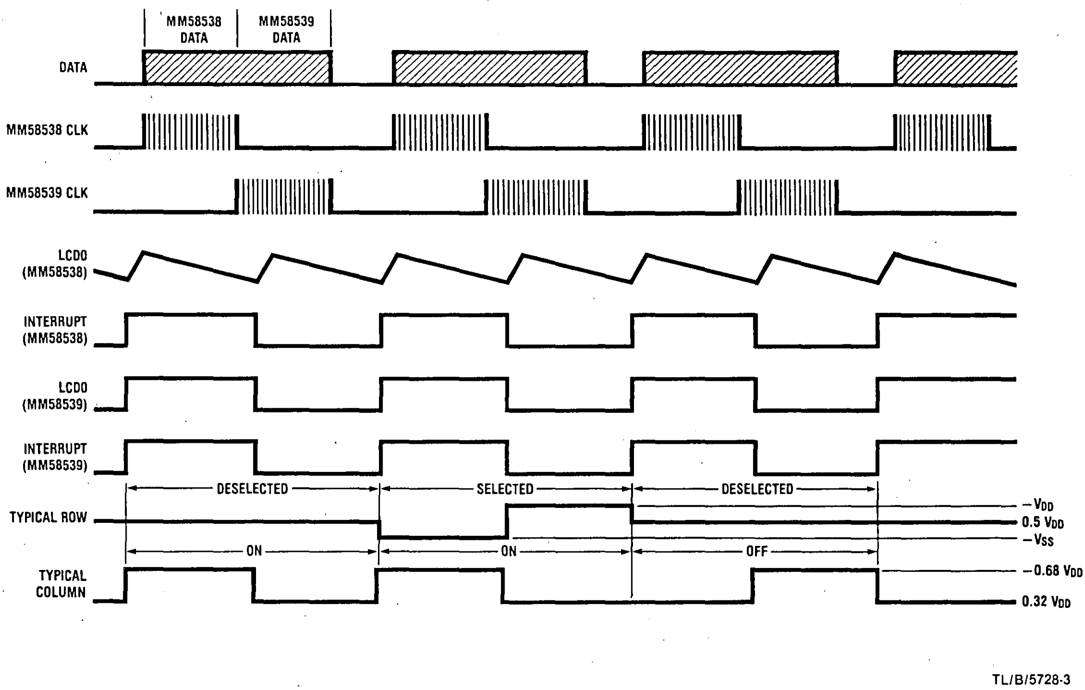


FIGURE 3

LCDO INPUT

This input can be used in two modes:

1 Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the Interrupt output as a frequency of approximately 1/RC, where R should exceed 1 Mohm.

The Interrupt output frequency should be the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2 Driven Mode

In this mode, the Interrupt output will follow the waveform input on the LCDO pin.

LCDO of a driven mode device should preferably be connected to the Interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% +/−1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the R_{OW} outputs to the Deselected state, all the Column outputs to the Off state and the Interrupt output high. If the circuit is in the Oscillating mode, the LCDO pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCDO pin is held high by the low impedence Interrupt output of the previous device. When the first clock pulse goes to a logic '1', the level on the LCDO pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating.

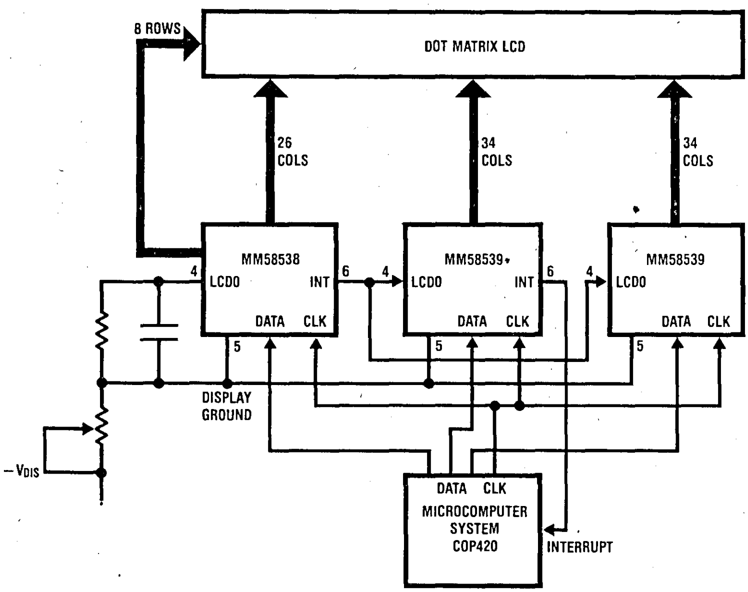
The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the Driven mode, the Interrupt frequency is in phase with the input frequency on LCDO.

CASCADING

Figure 4 shows an application where two or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The Interrupt output from the 'master' oscillating circuit is connected to the LCDO input of the other 'slave' circuits, with the 'slave' Interrupt going to the microprocessor. It would also be possible to connect all LCDO inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and separate data bus lines or vice versa.



TL/B/5728-4

FIGURE 4. Typical Application Diagram

National Semiconductor

PRELIMINARY

MM58539 Multiplexed LCD Driver

General Description

The MM58539 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P- and N-channel devices, which can drive up to 34 columns of a dot matrix LCD array directly under the control of an external processor. The MM58539 should be used with an MM58538 or MM58548 to drive a display that has up to 8 or 16 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in a 40-pin molded dual-in-line package or dice.

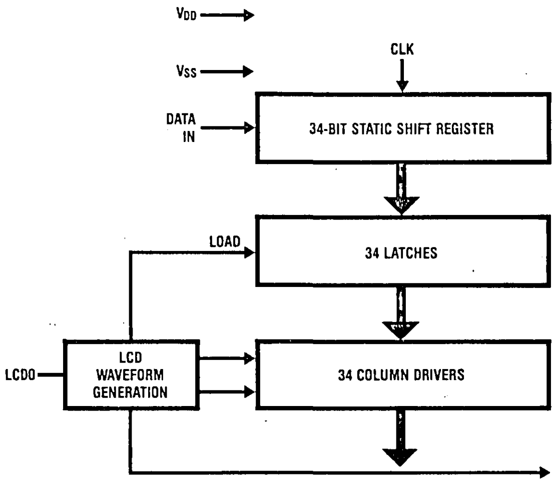
Features

- Drives up to 34 columns
- Used with the MM58538 or MM58548 for expanding to larger displays
- Flexible organization allows any display pattern
- Simple 3 line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On chip oscillator
- Compatible with HLCD 0539

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block Diagram

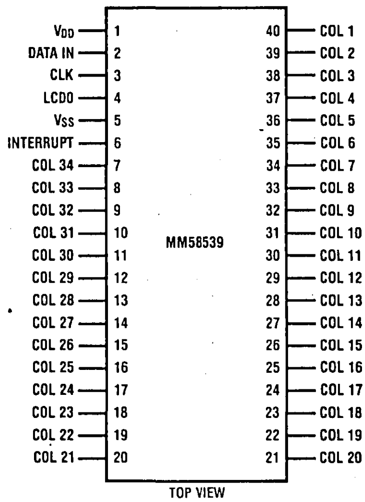


TL/B/6167-1

FIGURE 1

Connection Diagrams

Dual-In-Line Package



TL/B/6167-2

FIGURE 2

Order Number MM58539N
See NS Package N40A

Absolute Maximum Ratings

Voltage at any input pin	$V_{DD}-20V$ to $V_{DD}+0.3V$
Voltage at any display pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature	−65°C to 150°C
Power Dissipation	250 mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	−40°C to 70°C

Electrical Characteristics $T=25°C$ and $V_{DD}=5V$ unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3		15	V
I_{DD}	Supply Current				400	μA
V_{IH}	Input High Level	All V_{DD}	$.75V_{DD}$		V_{DD}	V
V_{IL}	Input Low Level	All V_{DD}	$V_{DD}-15$		$.25V_{DD}$	V
I_L	Input Leakage				5	μA
C_I	Input Cap.				5	pF
V_{OH}	Column O/P High	All V_{DD}		$.68V_{DD}$		V
V_{OL}	Column O/P Low	All V_{DD}		$.32V_{DD}$		V
V_{OFF}	Average DC Offset, any display element				100	mV
R_{ON}	Interrupt Output Impedance	$I_L=100$ μA			1	kΩ
f	Clock Frequency		DC		1.5	MHz
t_{ds}	Data-in Setup Time	Data change to clock fall	300			ns
T_{DH}	Data in Hold Time	Clock fall to data change	100			ns
t_d	LCD0 to Int. Out Delay		300			ns
$t_{r/f}$	Clock Rise/Fall Time				200	ns
V_{IH}	LCD0 High Level	All V_{DD}	$.9V_{DD}$		V_{DD}	V
V_{IL}	LCD0 Low Level	All V_{DD}	0		$.1V_{DD}$	V
R_{IN}	LCD0 Input Impedance		1		3	MΩ

Functional Description

A block diagram of the MM58539 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

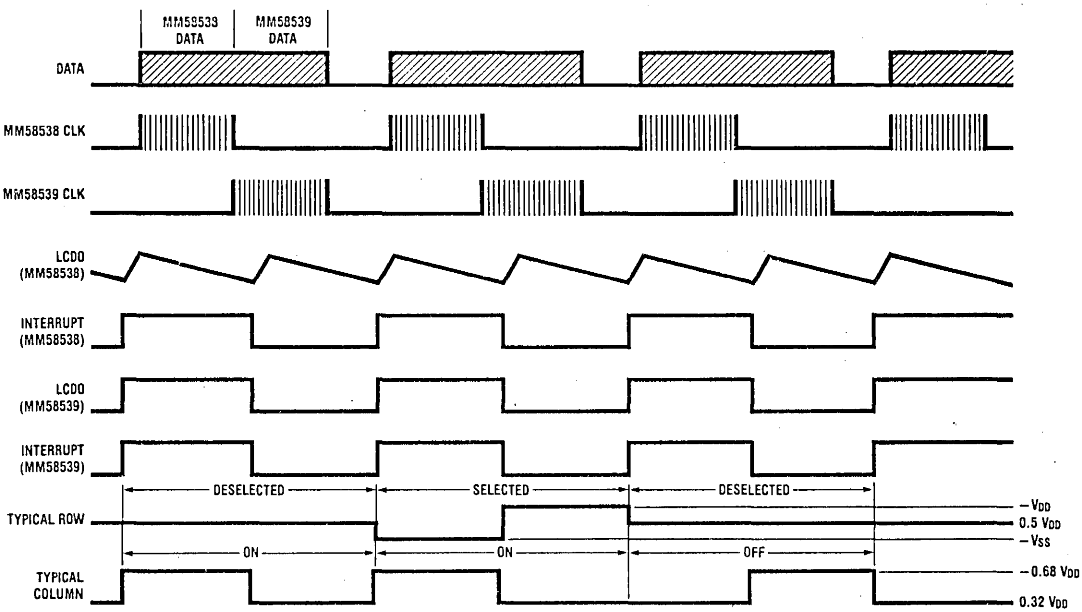
MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface when the MM58539 is used with the MM58538 to provide row and column information. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic "1" on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This Interrupt signal also acts as a refresh request and new data must be loaded before the next Interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 7 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for an MM58539 together with an MM58538 in *Figure 3*.

Rows generated from the MM58538 are out of phase with Interrupt if selected and at midpoint voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns generated from both the MM58538 and the MM58539 are in phase with Interrupt if selected and out of phase if not selected; levels are $0.32V_{DD}$ and $0.68V_{DD}$. Backplanes, ie rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimise LCD contrast or for temperature compensation it is recommended that all positive supply terminals be connected together and the negative supply varied.



TL/B/6167-3

FIGURE 3

LCD0 INPUT

This input can be used in two modes:

1. Oscillating Mode

   When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the Interrupt output as a frequency of approximately 1/RC, where R should exceed 1 MΩ.

   The Interrupt output frequency should be the minimum no-flicker frequency (approximately 30Hz) multiplied by the number of backplanes used.

2. Driven Mode

   In this mode, the Interrupt output will follow the waveform input on the LCD0 pin.

   LCD0 of a driven mode device should preferably be connected to the Interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% +/−1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the Row outputs to the Deselected state, all the Column outputs to the Off state and the Interrupt output high. If the circuit is in the Oscillating mode, the LCD0 pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCD0 pin is held high by the low impedance Interrupt output of the previous device. When the first clock pulse goes to a logic "1", the level on the LCD0 pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating.

The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the Driven mode, the Interrupt frequency is in phase with the input frequency on LCD0.

CASCADING

Figure 4 shows an application where two or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The Interrupt output from the "master" oscillating circuit is connected to the LCD0 input of the other "slave" circuits, with the "slave" Interrupt going to the microprocessor. It would also be possible to connect all LCD0 inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and separate data bus lines or vice versa.

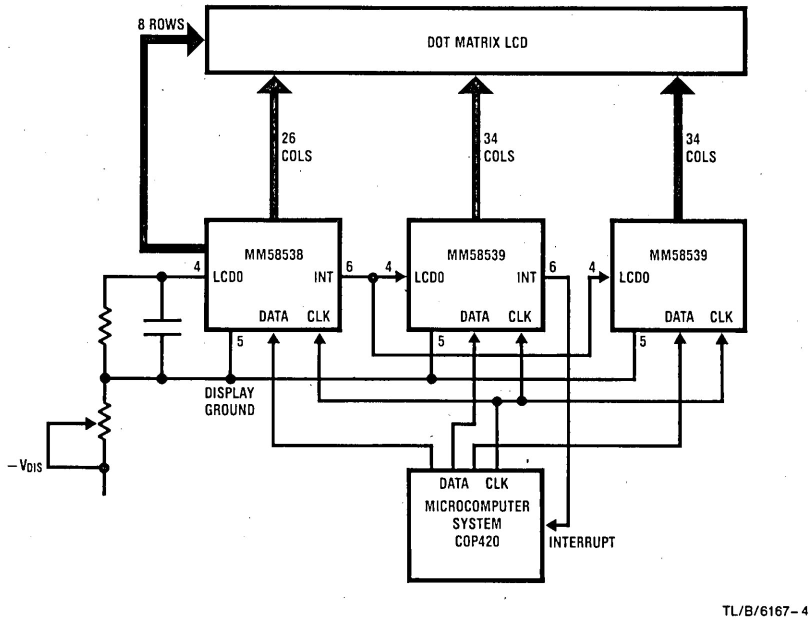


FIGURE 4. Typical Application Diagram

MM58540 Multiplexed LCD Driver

General Description

The MM58540 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P and N-channel devices. It can be externally programmed to drive either 32 rows or 32 columns under control of the ROW/COL pin. A high level selects all rows and a low level all columns. Two MM58540s with opposite selections can therefore be used to drive a 32 × 32 display. Data can be input serially from the microprocessor provided that CLKEN is high. This is done in response to an interrupt signal.

The circuit is available in either 40-pin molded dual-in-line packages or dice.

Features

- Drives either 32 rows or 32 columns
- Cascadable for larger displays
- Flexible organization allows any display pattern
- Simple 4-line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On-chip oscillator
- Compatible with HLCD 0540

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block Diagram

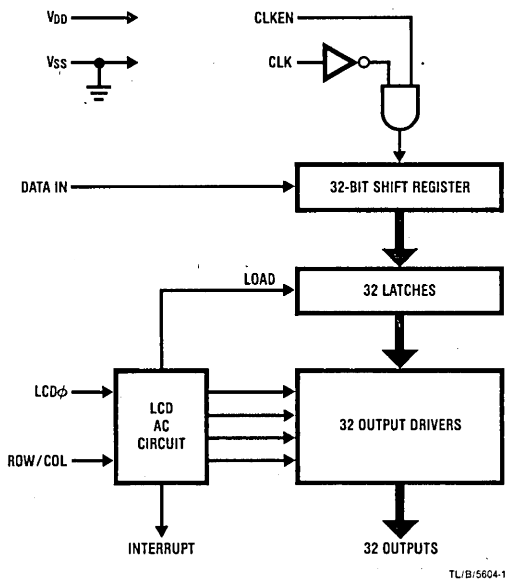


FIGURE 1

Connection Diagram

Dual-In-Line Package

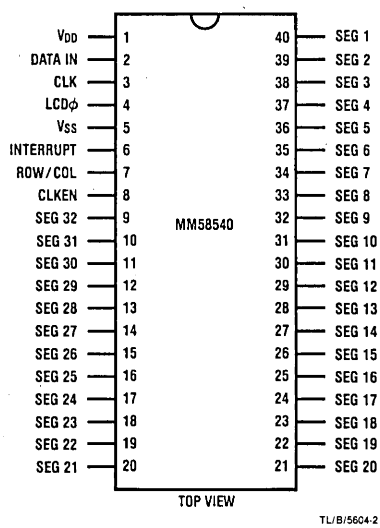


FIGURE 2

Order Number MM58540N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	V_{DD} – 20V to V_{DD} + 0.3V
Voltage at Any Display Pin	V_{SS} – 0.3V to V_{DD} + 0.3V
Storage Temperature	– 65°C to 150°C
Power Dissipation	250 mW
Operating Temperature	– 40°C to 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A = 25°C and V_{DD} = 5V unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage, V_{DD}		3		15	V
Supply Current, I_{DD}				400	μA
Input High Level, V_{IH}	All V_{DD}	0.75 V_{DD}		V_{DD}	V
Input Low Level, V_{IL}	All V_{DD}	V_{DD} – 15		0.25 V_{DD}	V
Input Leakage, I_L				5	μA
Input Capacitance, C_I				5	pF
Row Output High	All V_{DD}			V_{DD}	V
Row Output Low	All V_{DD}	V_{SS}			V
Row Unselected	All V_{DD}		0.5 V_{DD}		V
Column O/P High	All V_{DD}		0.68 V_{DD}		V
Column O/P Low	All V_{DD}		0.32 V_{DD}		V
Average DC Offset, Any Display Element				100	mV
Row and Column Output Impedance	I_L = 10 μA			40	kΩ
Interrupt Output Impedance	I_L = 100 μA			1	kΩ
Clock Frequency, f		DC		1.5	MHz
Data-In Set-Up Time, t_{DS}	Data Change to Clock Fall	300			ns
Data-In Hold Time, t_{DH}	Clock Fall to Data Change	100			ns
LCDϕ to Interrupt Out Delay, t_D		300			ns
Clock Rise/Fall Time, t_r, t_f				200	ns
LCDϕ High Level	All V_{DD}	0.9 V_{DD}		V_{DD}	V
LCDϕ Low Level	All V_{DD}	0		0.1 V_{DD}	V
LCDϕ Input Impedance		1		3	MΩ

Functional Description

A block diagram of the MM58540 LCD driver is shown in *Figure 1*. A connection diagram is shown in *Figure 2*.

MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock provided that CLKEN is high. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This interrupt signal also acts as a refresh request and new data must be loaded before the next interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 9 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for two separate devices in *Figure 3*. Rows are out of phase with interrupt if selected and at midpoint voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns are in phase with interrupt if selected and out of phase if not selected; levels are 0.32 V_{DD} and 0.68 V_{DD}. Backplanes, i.e., rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimize LCD contrast or for temperature compensation, it is recommended that all positive supply terminals be connected together and the negative supply varied.

Functional Description (Continued)

LCDϕ INPUT

This input can be used in two modes:

1) Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by 2 to provide a 50% duty cycle and will then appear at the interrupt output as a frequency of approximately 1/RC, where R should exceed 1 MΩ.

The interrupt output frequency should be the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2) Driven Mode

In this mode, the interrupt output will follow the waveform input on the LCDϕ pin.

LCDϕ of a driven mode device should preferably be connected to the interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% ±1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the row outputs to the deselected state, all the column outputs to the off state and the interrupt output high. If the circuit is in the oscillating mode, the LCDϕ pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCDϕ pin is held high by the low impedance interrupt output of the previous devices. When the first clock pulse goes to a logic '1', the level on the LCDϕ pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating. The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the driven mode, the interrupt frequency is in phase with the input frequency on LCDϕ.

CASCADING

Figure 4 shows an application where 2 or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The interrupt output from the 'master' oscillating circuit is connected to the LCDϕ input of the other 'slave' circuits, with the 'slave' interrupt going to the microprocessor. It would also be possible to connect all LCDϕ inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and data with separate clock-enable lines or by holding CLKEN high and having a common clock and separate data bus lines or vice-versa.

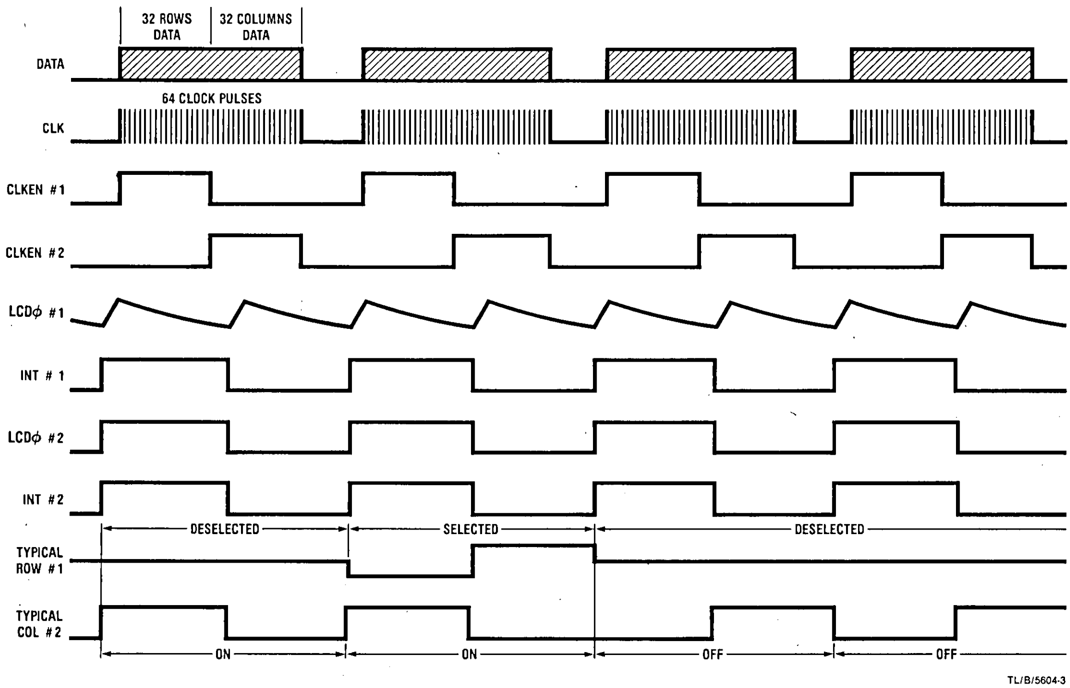


FIGURE 3

Functional Description (Continued)

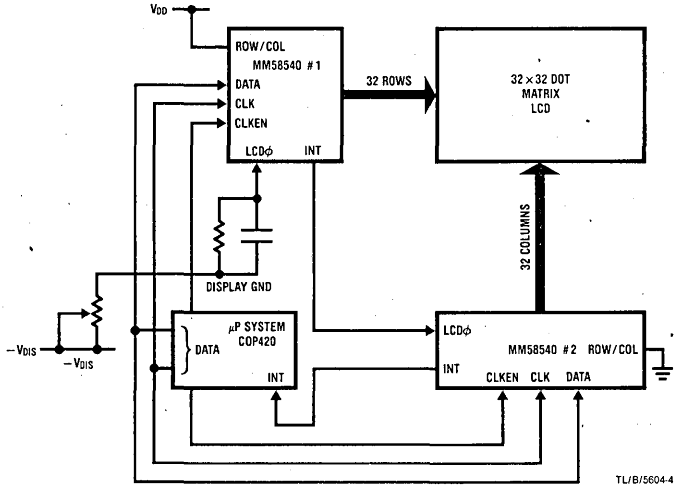


FIGURE 4

National Semiconductor

PRELIMINARY

MM58548 Multiplexed LCD Driver

General Description

The MM58548 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P and N-channel devices. It drives a 16-row by 16-column dot matrix LCD array directly under control of an external microprocessor. The MM58548 can be used with an MM58539 to drive a display that has up to 16 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in either 40-pin molded dual-in-line packages or dice.

Features

- Drives up to 16 rows and 16 columns
- Expandable to larger displays with MM58539
- Flexible organization allows any display pattern
- Simple 3-line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On-chip oscillator
- Compatible with HLCD 0548

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block Diagram

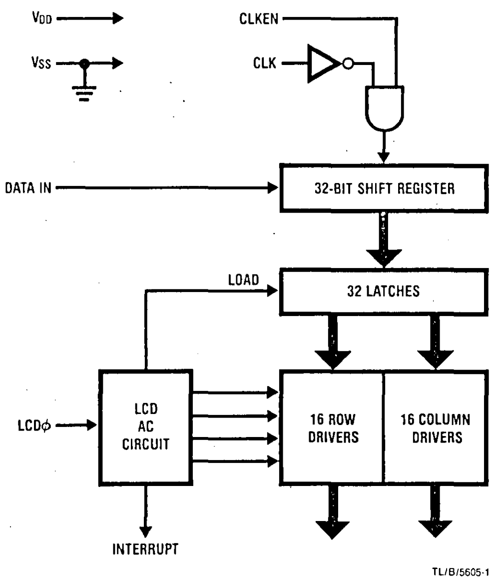


FIGURE 1

Connection Diagram

Dual-In-Line Package

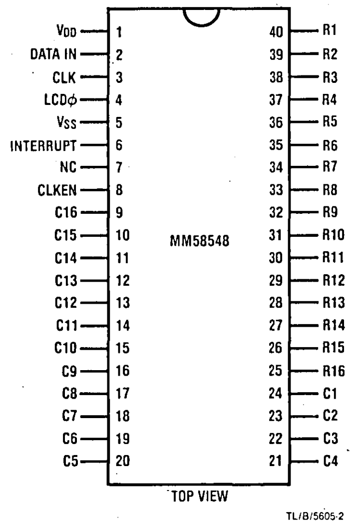


FIGURE 2

Order Number MM58548N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}-20V$ to $V_{DD}+0.3V$	Power Dissipation	250 mW
Voltage at Any Display Pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	Operating Temperature	−40°C to 70°C
Storage Temperature	−65°C to 150°C	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A=25°C$ and $V_{DD}=5V$ unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage, V_{DD}		3		15	V
Supply Current, I_{DD}				400	μA
Input High Level, V_{IH}	All V_{DD}	0.75 V_{DD}		V_{DD}	V
Input Low Level, V_{IL}	All V_{DD}	$V_{DD}-15$		0.25 V_{DD}	V
Input Leakage, I_L				5	μA
Input Capacitance, C_I				5	pF
Row Output High	All V_{DD}			V_{DD}	V
Row Output Low	All V_{DD}	V_{SS}			V
Row Unselected	All V_{DD}		0.5 V_{DD}		V
Column O/P High	All V_{DD}		0.68 V_{DD}		V
Column O/P Low	All V_{DD}		0.32 V_{DD}		V
Average DC Offset, Any Display Element				100	mV
Row and Column Output Impedance	$I_L=10\ \mu A$			40	kΩ
Interrupt Output Impedance	$I_L=100\ \mu A$			1	kΩ
Clock Frequency, f		DC		1.5	MHz
Data-In Set-Up Time, t_{DS}	Data Change to Clock Fall	300			ns
Data-In Hold Time, t_{DH}	Clock Fall to Data Change	100			ns
LCDϕ to Interrupt Out Delay, t_D		300			ns
Clock Rise/Fall Time, t_r, t_f				200	ns
LCDϕ High Level	All V_{DD}	0.9 V_{DD}		V_{DD}	V
LCDϕ Low Level	All V_{DD}	0		0.1 V_{DD}	V
LCDϕ Input Impedance		1		3	MΩ

Functional Description

A block diagram of the MM58548 LCD driver is shown in *Figure 1.* A connection diagram is shown in *Figure 2.*

MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer of data from the shift register to the latches occurs and the row and column outputs change accordingly. This interrupt signal also acts as a refresh request and new data must be loaded before the next interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 9 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown in *Figure 3.* Rows are out of phase with interrupt if selected and at midpoint voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns are in phase with interrupt if selected and out of phase if not selected; levels are 0.32 V_{DD} and 0.68 V_{DD}. Backplanes; i.e., rows, should be addressd sequentially and individually. If the supply voltage has to be altered to optimize LCD contrast or for temperature compensation, it is recommended that all positive supply terminals be connected together and the negative supply varied.

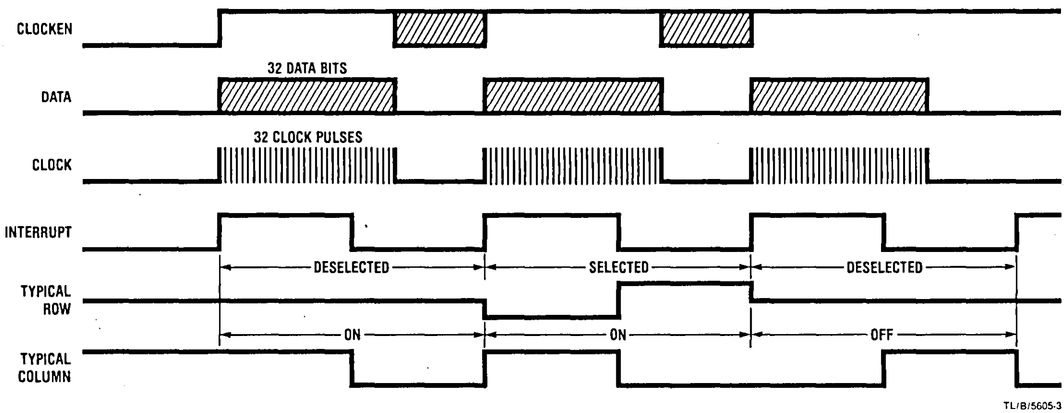


FIGURE 3

LCDϕ INPUT

This input can be used in two modes:

1) Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the interrupt output as a frequency of approximately 1/RC, where R should exceed 1MΩ.

The interrupt output frequency should be the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2) Driven Mode

In this mode, the interrupt output will follow the waveform input on the LCDϕ pin.

LCDϕ of a driven mode device should preferably be connected to the interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% ± 1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the row outputs to the deselected state, all the column outputs to the off state and the interrupt output high. If the circuit is in the oscillating mode, the LCDϕ pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCDϕ pin is held high by the low impedance interrupt output of the previous device. When the first clock pulse goes to a logic '1', the level on the LCDϕ pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating. The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the driven mode, the interrupt frequency is in phase with the input frequency on LCDϕ.

CASCADING

Figure 4 shows an application where 2 or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The interrupt output from the 'master' oscillating circuit is connected to the LCDϕ input of the other 'slave' circuits, with the 'slave' interrupt going to the microprocessor. It would also be possible to connect all LCDϕ inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and data with separate clock-enable lines or by holding CLKEN high and having a common clock and separate data bus lines or vice-versa.

Functional Description (Continued)

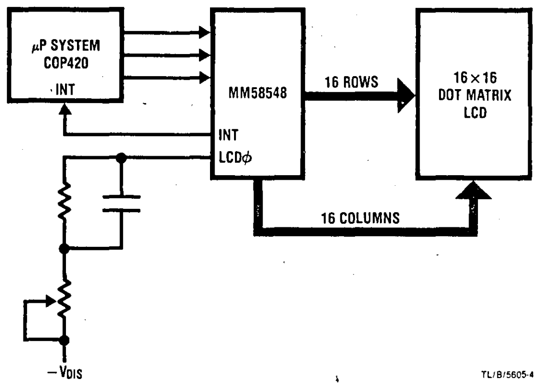


FIGURE 4

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4511/MM74HC4511
BCD-to-7 Segment Latch/Decoder/Driver

General Description

This high speed latch/decoder/driver utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

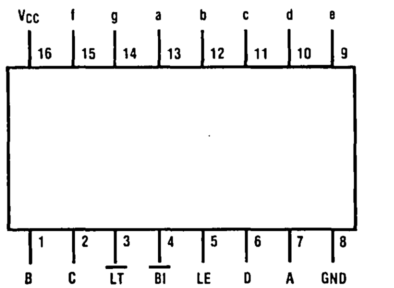
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Latch storage of input data
- Blanking input
- Lamp test input
- Low power consumption characteristics of CMOS devices
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum over full temperature range (74 Series)

Connection Diagram

Dual-In-Line Package



TL/F/5373-1

TOP VIEW

MM54HC4511/MM74HC4511

54HC4511 (J) 74HC4511 (J,N)

Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
x	x	0	x	x	x	x	1	1	1	1	1	1	1	8
x	0	1	x	x	x	x	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	x	x	x	x				*				*

x = Don't care

* = Depends upon the BCD code applied during the 0 to 1 transition of LE.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$7.5 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$9.75 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output		60	120	ns
t_S	Minimum Setup Time Inputs A thru D to LE		10	20	ns
t_H	Minimum Hold Time Inputs A thru D to LE		−3	0	ns
t_W	Minimum Pulse Width for LE			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output	LE=0V $\overline{LT}=V_{CC}$ $\overline{BI}=V_{CC}$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output	$\overline{LT}=V_{CC}$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output	$\overline{BI}=0V$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_S	Minimum Setup Time Inputs A thru D to LE		2.0V 4.5V 6.0V		100 20 17	126 25 21	149 30 25	ns ns ns
t_H	Minimum Hold Time Inputs A thru D to LE		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width for LE		2.0V 4.5V 6.0V		80 16 14	100 20 17	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

INPUTS

A, B, C, D (Pins 7, 1, 2, 6)—BCD data inputs. A (pin 7) is the least-significant data bit and D (pin 6) is the most significant bit. Hexadecimal data A–F at these inputs will cause the outputs to assume a logic low, offering an alternate method of blanking the display.

OUTPUTS

a–g—Decoded, buffered outputs. These outputs, unlike the 4511, have CMOS drivers, which will produce typical CMOS output voltage levels.

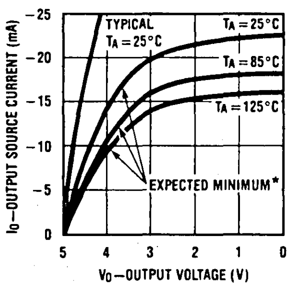
CONTROLS

$\overline{\text{BI}}$ (Pin 4)—Active-low display blanking input. A logic low on this input will cause all outputs to be held at a logic low, thereby blanking the display. LT is the only input that will override the BI input.

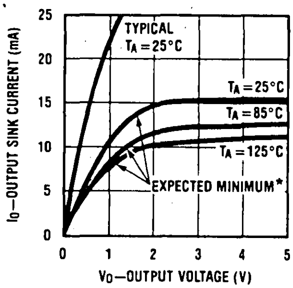
$\overline{\text{LT}}$ (Pin 3)—Active-low lamp test. A low logic level on this input causes all outputs to assume a logic high. This input allows the user to test all segments of a display, with a single control input. This input is independent of all other inputs.

LE (Pin 5)—Latch enable input. This input controls the 4-bit transparent latch. A logic high on this input latches the data present at the A, B, C and D inputs; a logic low allows the data to be transmitted through the latch to the decoder.

Output Characteristics (V_{CC} = 5V)



TL/F/5373-2



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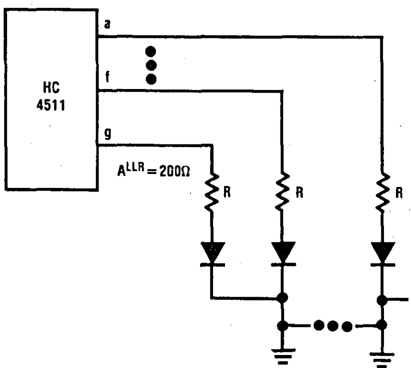
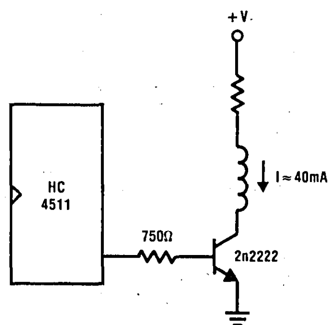
*The expected minimum curves are not guarantees, but are design aids.

Typical Applications



TL/F/5373-4

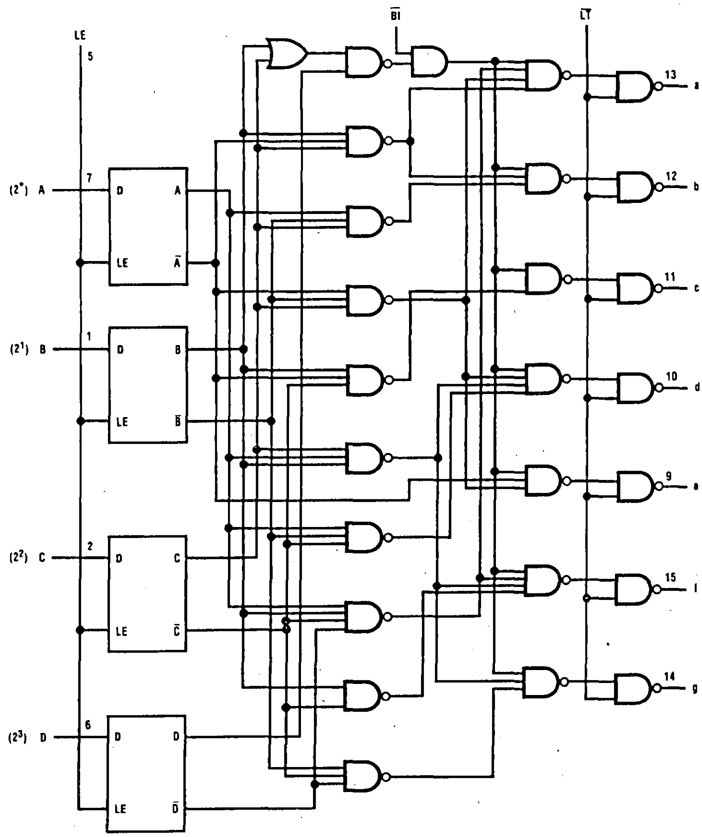
Typical Common Cathode LED Connection



TL/F/5373-5

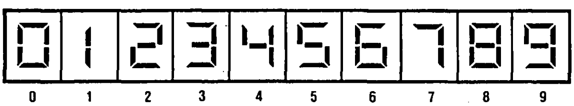
Incandescent Bulb Driving Circuit

Logic Diagram



TL/F/5373-6

Display



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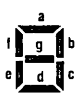
Segment Identification



TL/F/5373-8

National Semiconductor

microCMOS

MM54HC4543/MM74HC4543 BCD-to-7 Segment Latch/ Decoder/Driver for Liquid Crystal Displays

General Description

The MM54HC4543/MM74HC4543 BCD-to-7 segment latch/decoder/driver utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and can be used either as a high speed decoder or as a display driver. This circuit contains a 4-bit latch, BCD-to-7 segment decoder, and 7 output drivers. Data on the input pins flow through to the output when the LATCH ENABLE (LE) is high and is latched on the high to low transition of the LE input. The PHASE input (PH) controls the polarity of the 7 segment outputs. When PH is low the outputs are true 7 segment, and when PH is high the outputs are inverted 7 segment. When the PHASE input is driven by a liquid crystal display (LCD) backplane waveform the segment pins output the correct segment waveform for proper LCD AC drive voltages.

In addition a BLANKING INPUT (BI) is provided, which will blank the display.

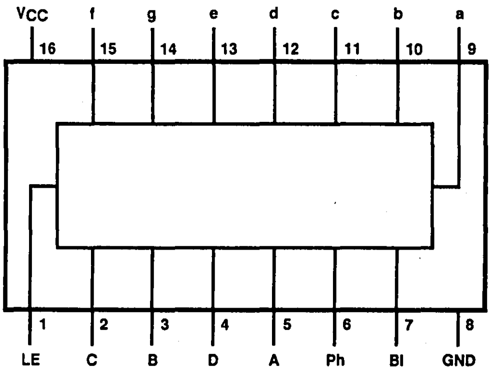
The MM54HC4543/MM74HC4543 are functionally and pinout equivalent to the CD4543BC/CD4543BM and the MC14543BA/MC14543BC. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 60 ns
- Supply voltage range: 2–6V
- Maximum input current: 1 μA
- Maximum quiescent supply current: 80 μA (74HC)
- Display blanking
- Low dynamic power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5128-1

TOP VIEW

MM54HC4543/MM74HC4543

54HC4543 (J) 74HC4543 (J,N)

Truth Table

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

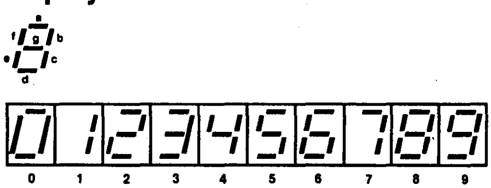
X—don't care

† = same as above combinations

* = for liquid crystal readouts, apply a square wave to Ph.

** = depends upon the BCD code previously applied when LE—H

Display Format



TL/F/5128-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	74HC T_A=−40 to 85°C Guaranteed Limits	54HC T_A=−55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 0.4$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 0.52$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 0.4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 0.52$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, BI, PH to Output		60	100	ns
t_S	Minimum Setup Time LE to Data			20	ns
t_H	Minimum Hold Time Data to LE			10	ns
t_W	Minimum LE Pulse Width			16	ns

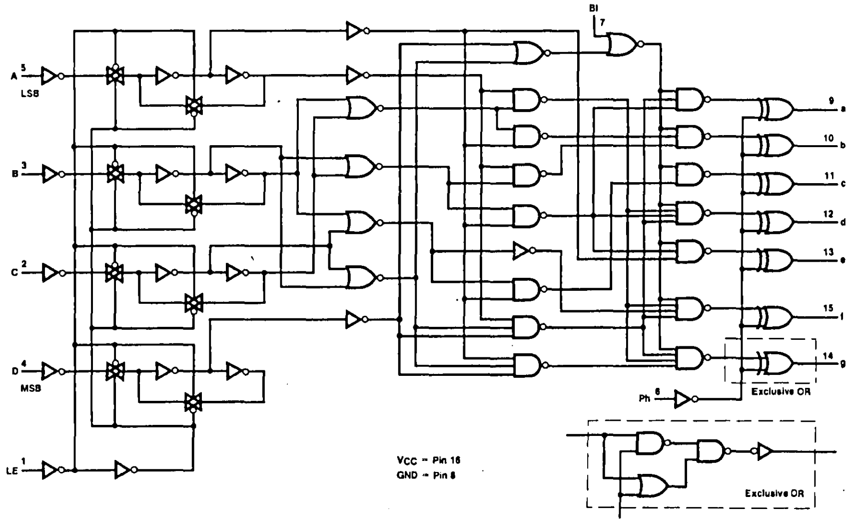
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, PH, BI to Output		2.0V	300	600	760	895	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_S	Minimum Setup Time LE to Data		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data to LE		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_W	Minimum LE Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

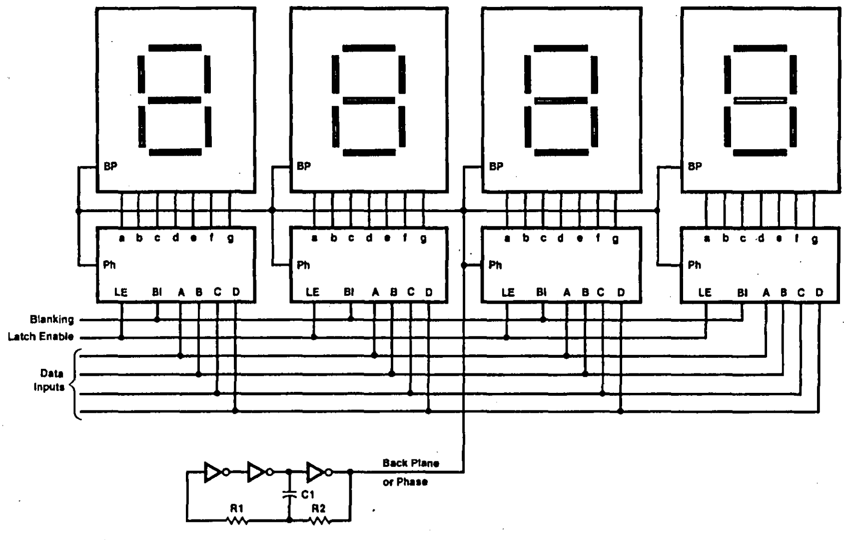
Logic Diagram



TL/F/5128-3

Typical Applications

4 Digit LCD Display



CI = 0.047 μF
R1 = R2 = 100kΩ

TL/F/5128-4

Section 9

RAMs

9

Introduction

National's CMOS static RAMs utilize microCMOS technology and may be used with CMOS logic, microprocessors, custom LSI and other semiconductor products to optimize system speed/power trade-offs. Synchronous operation is provided by on-chip address latches. Static RAM products also provide data retention at 2V.

National Semiconductor

PRELIMINARY

microCMOS

NMC6164 8192 × 8-Bit Static RAM

General Description

The NMC6164 is a 8192-word by 8-bit new generation static RAM. It is fabricated with National's proprietary microCMOS double-polysilicon technology which combines high performance and high density with low power consumption and excellent reliability.

The NMC6164 is designed to operate with a single 5V power supply with ±10% tolerance. Additional battery back-up operation is available (LP version).

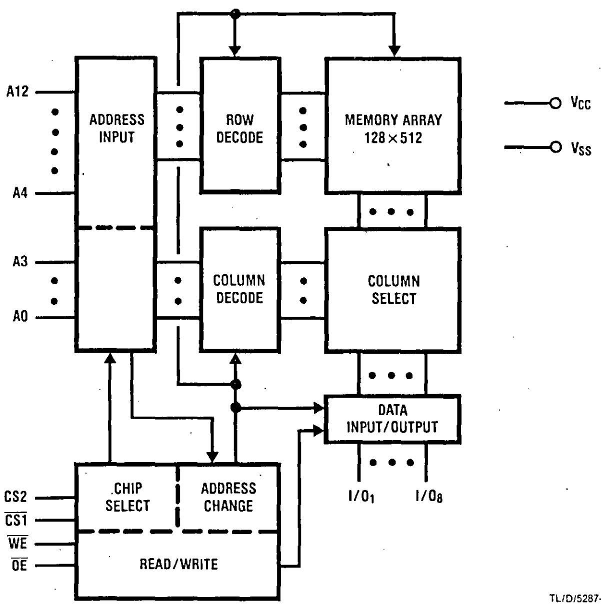
Packaging is in a standard 28-pin DIP and is available in both plastic and CERDIP. It is pin compatible with the 64k EPROM.

In addition to the inputs and outputs being TTL compatible, the outputs are also CMOS compatible in that capacitive loads are driven to V_{CC} or V_{SS}.

Features

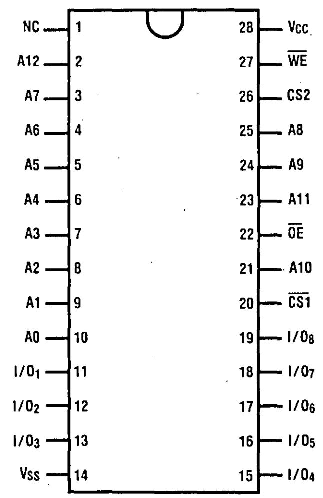
- Single power supply: 5V ± 10%
- High speed: fast access time 100 ns/120 ns/150 ns max
- Equal access and cycle time
- Completely static RAM: No clock or timing strobe required
- Low standby power and low power operation
  Standby: 10 μW typ
  Operation: 15 mW/MHz
- Battery back-up operation available (LP)
- Common data input and output, TRI-STATE® output
- TTL compatible: all inputs and outputs
- CMOS compatible: outputs drive capacitive loads to V_{CC} or V_{SS}
- Standard 28-pin package configuration
- Pin compatible with 64k EPROM
- Data retention supply voltage: 2V-5.5V

Block and Connection Diagrams



TL/D/5287-1

Dual-In-Line Package



TOP VIEW

TL/D/5287-2

Order Number NMC6164J or NMC6164N
See NS Package J28A or N28B

Absolute Maximum Ratings

Voltage on Any Pin Relative to GND, V_{SS}	−0.5V–7V
Operating Temperature, T_{OPR}	0°C–70°C
Storage Temperature, T_{STG}	−55°C–125°C
Temperature under Bias, T_{BIAS}	−10°C–85°C
Power Dissipation, P_D	1.0W
Current Through Any Pin	100 mA max

Recommended DC Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
V_{SS} Supply Voltage	0	0	V
V_{IH}, Input High Voltage (Logic 1)			
TTL	2.2	6.0	V
CMOS	$V_{CC}-0.2$	$V_{CC}+0.2$	V
V_{IL}, Input Low Voltage (Logic 0)			
TTL	−0.3	0.8	V
CMOS	−0.2	0.2	V

DC Electrical Characteristics at recommended operating conditions

Symbol		Parameter	Conditions	Min	Max	Units
I_{LI}		Input Leakage Current	$V_{IN}=V_{SS}$ to V_{CC}	−2	2	μA
I_{LO}		Output Leakage Current	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $OE=V_{IH}$ $V_{I/O}=V_{SS}$ to V_{CC}	−2	2	μA
I_{CC}		Active Quiescent Current	All Inputs at TTL Levels $\overline{CS1}=V_{IL}$, TTL or $CS2=V_{IH}$, TTL $I_{I/O}=0$ mA		25	mA
I_{CC}	P	Active Quiescent Current	All Inputs at CMOS Levels $\overline{CS1}=V_{IL}$, CMOS or $CS2=V_{IH}$, CMOS $I_{I/O}=0$ mA		2	mA
	LP				100	μA
I_{CC1}		Average Operating Current	Duty Cycle = 100%, All Inputs at TTL Levels, $\overline{CS1}=V_{IL}$, $CS2=V_{IH}$			
			TTL		60	mA
			CMOS		40	mA
I_{SB}	P	Standby Power Supply Current	$\overline{CS1}=V_{IH}$, TTL or $CS2=V_{IL}$, TTL		4	mA
	LP		$I_{I/O}=0$ mA		2	mA
I_{SB1}	P	Standby Power Supply Current	$\overline{CS1}=V_{IH}$, CMOS $CS2=V_{IH}$, CMOS or V_{IL}, CMOS		2	mA
	LP				100	μA
I_{SB2}	P	Standby Power Supply Current	$CS2=V_{IL}$, CMOS		2	mA
	LP				100	μA
V_{OL}		Output Low Voltage, TTL	$I_{OL}=2.1$ mA		0.4	V
		Output Low Voltage, CMOS	$I_{OL}=\pm 10\ \mu A$	−0.2	0.2	V
V_{OH}		Output High Voltage, TTL	$I_{OH}=-1.0$ mA	2.4		V
		Output High Voltage, CMOS	$I_{OH}=\pm 10\ \mu A$	$V_{CC}-0.2$	$V_{CC}+0.2$	V

Capacitance

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	$V_{IN}=0V$ (Note 5)	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}=0V$ (Note 5)	8	pF

AC Electrical Characteristics (Note 1)

Symbol	Parameter	NMC6164 P(LP) – 10		NMC6164 P(LP) – 12		NMC6164 P(LP) – 15		Units
		Min	Max	Min	Max	Min	Max	
READ CYCLE (Note 4)								
t_{RC}	Read Cycle Time	100		120		150		ns
t_{AA}	Address Access Time		100		120		150	ns
t_{CO1}	Chip Selection ($\overline{CS1}$) to Output		100		120		150	ns
t_{CO2}	Chip Selection (CS2) to Output		100		120		150	ns
t_{OE}	Output Enable ($\overline{OE}$) to Output Valid		50		60		70	ns
t_{LZ1}	Chip Selection ($\overline{CS1}$) to Output in Low Z	10		10		15		ns
t_{LZ2}	Chip Selection (CS2) to Output in Low Z	10		10		15		ns
t_{OLZ}	Output Enable ($\overline{OE}$) to Output in Low Z	5		5		5		ns
t_{HZ1}	Chip Deselection ($\overline{CS1}$) to Output in Hi-Z (Notes 2 and 3)	0	35	0	40	0	50	ns
t_{HZ2}	Chip Deselection (CS2) to Output in Hi-Z (Notes 2 and 3)	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z (Notes 2 and 3)	0	35	0	40	0	50	ns
t_{OHA}	Output Hold from Address Change	10		10		15		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	100		120		150		ns
t_{CW}	Chip Selection to End of Write (Note 10)	80		85		100		ns
t_{AS}	Address Set-Up Time (Note 7)	0		0		0		ns
t_{AW}	Address Valid to End of Write	80		85		100		ns
t_{WP}	Write Pulse Width	60		70		90		ns
t_{WR1}	Write Recovery Time (Note 8)	0		5		10		ns
t_{WR2}	Write Recovery Time from CS2 (Note 8)	0		5		10		ns
t_{WHZ}	Beginning of Write to Output in Hi-Z (Notes 9 and 13)	0	35	0	40	0	50	ns
t_{DW}	Data Valid to Write Time Overlap	35		40		50		ns
t_{DH}	Data Hold from End of Write	0		0		0		ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write (Notes 11 and 12)	5		5		10		ns

Note 1: AC test conditions $T_A = 0°C$ to $+70°C$. $V_{CC} = 5V \pm 10\%$.

Note 2: t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

Note 3: At any given temperature and voltage condition, t_{HZMAX} is less than t_{LZMIN}, both for a given device and from device to device.

Note 4: $\overline{WE}$ is high for read cycle.

Note 5: $T_A = 25°C$, f = 1.0 MHz. This parameter is sampled and not 100% tested.

Note 6: A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$ and a high CS2 and a low $\overline{WE}$.

Note 7: t_{AS} is measured from the address changes to the beginning of the write.

Note 8: t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

Note 9: During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

Note 10: If the $\overline{CS1}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the outputs will remain in a Hi-Z state.

Note 11: D_{OUT} is the same phase of write data of this write cycle.

Note 12: D_{OUT} is the read data of next address.

Note 13: If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. At this time, the data input signals of opposite phase to the outputs must not be applied.

Note 14: CS2 controls the address buffers, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, D_{IN} buffer and $\overline{OE}$ buffer. When CS2 controls the data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$) can be in the high impedance state. When $\overline{CS1}$ controls the data retention mode, CS2 must be at V_{IH}, CMOS. All other input levels (address, $\overline{WE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention

Symbol	Parameter	Conditions	Min	Max	Units
V_{DR1}	V_{CC} for Data Retention	$\overline{CS1} > V_{IH}$, CMOS $CS2 > V_{IH}$, CMOS	2.0		V
V_{DR2}	V_{CC} for Data Retention	$CS2 < V_{IL}$, CMOS	2.0		V
I_{CCDR1}	Data Retention Current (Note 14)	$V_{CC} = 3.0V$, $\overline{CS1} > V_{IH}$, CMOS $CS2 > V_{IH}$, CMOS		60	μA
I_{CCDR2}	Data Retention Current (Note 14)	$V_{CC} = 3.0V$, $CS2 < V_{IL}$, CMOS		60	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}		ns

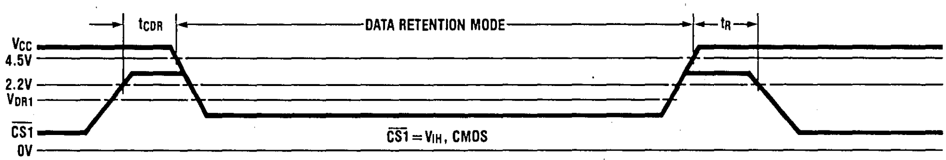
Truth Table

Mode	WE	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	Current	
Not Selected (Power Down)	*	H	*	*	Hi-Z	I_{SB}, I_{SB1}	
	*	*	L	*	Hi-Z	I_{SB}, I_{SB2}	
Output Disabled	H	L	H	H	Hi-Z	I_{CC}, I_{CC1}	
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}	
Write	L	L	H	H	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 1
	L	L	H	L	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 2

* Don't care (H or L)

Low V_{CC} Data Retention Waveforms

No. 1 (CS1 Controlled)



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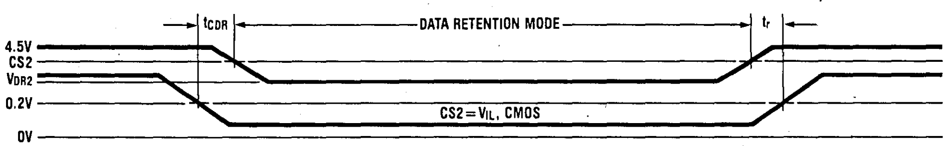
No. 2 (CS2 Controlled)



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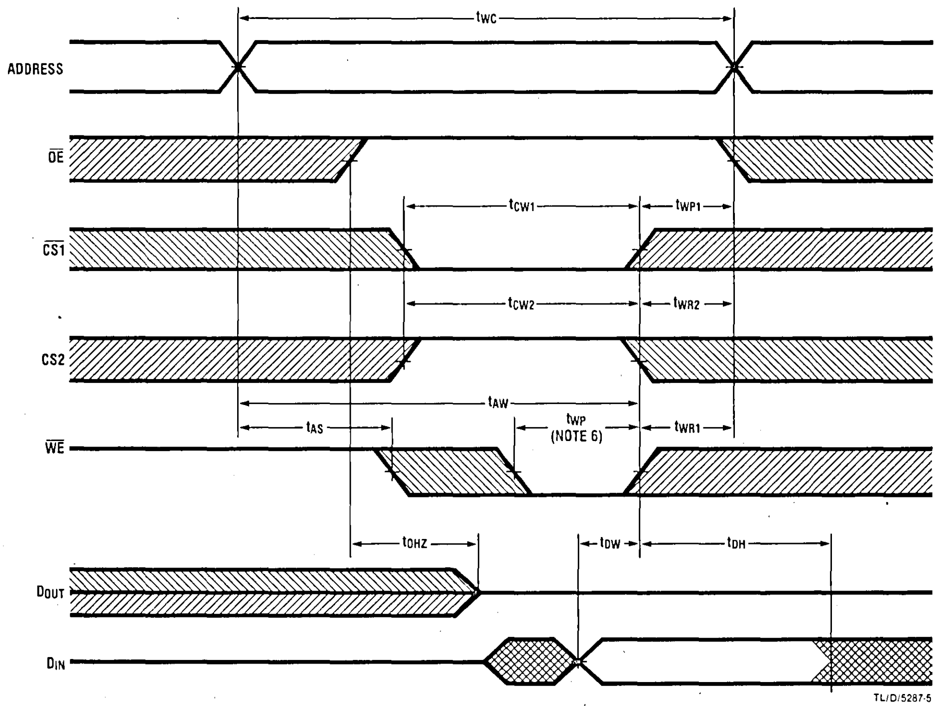
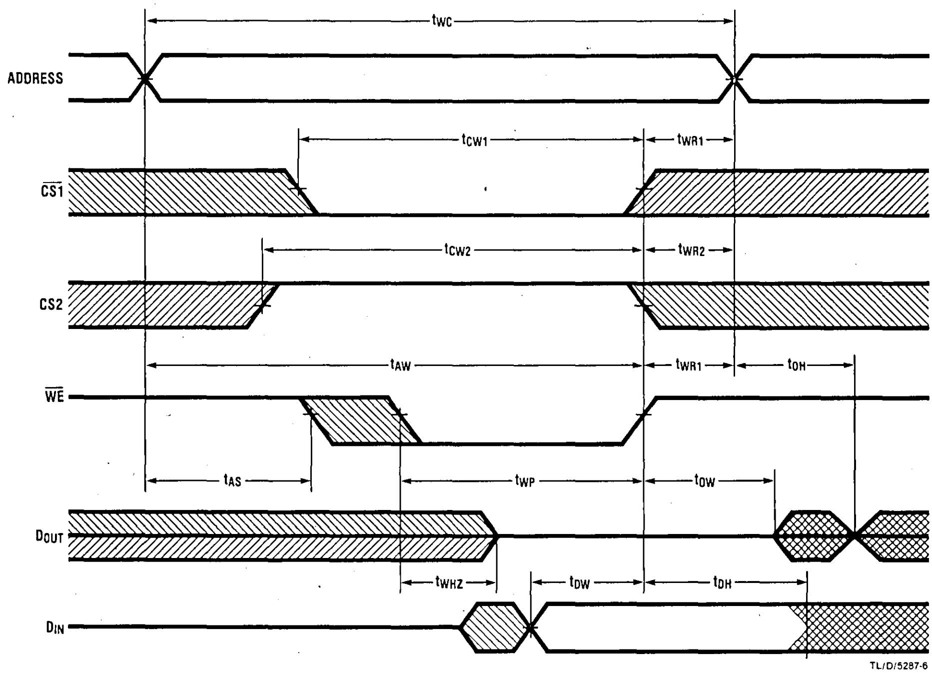
Timing Waveforms

Write Cycle 1 ($\overline{OE}$ Clocked)

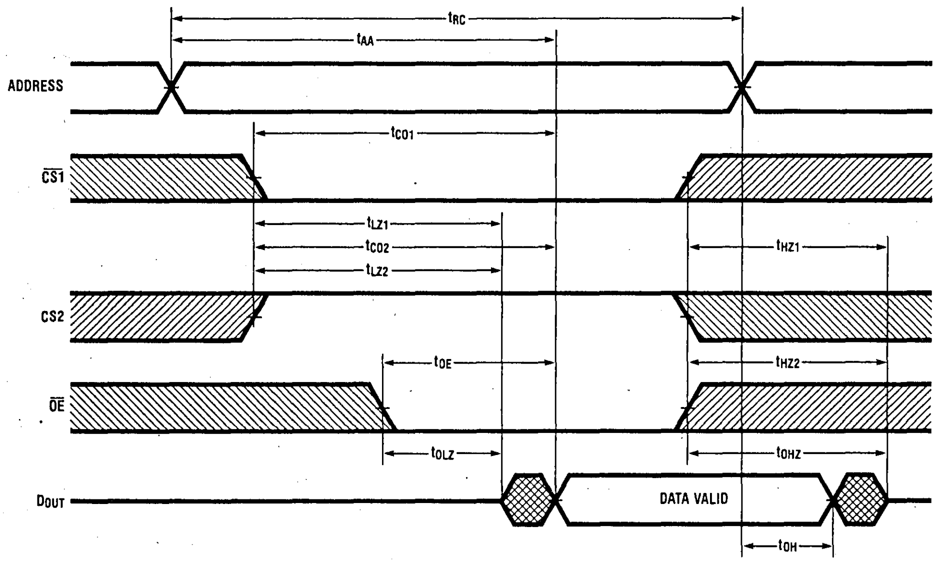


Write Cycle 2 ($\overline{OE}$ Low Fixed)



Timing Waveforms (Continued)

Read Cycle



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Section 10

PROMs

10

Introduction

When considering replacing existing NMOS EPROMs with the new CMOS memories in any system, one advantage overshadows all others: significantly reduced power consumption. For example, the maximum active current rating for a 16k NMOS EPROM is 100 mA. The equivalent CMOS EPROM of equal size and speed has a maximum rating of one tenth of this. The surprising aspect is that this smaller power drain does not increase with increases in memory density.

When the density of the memory is increased, the NMOS EPROMs draw more power, but CMOS EPROMs do not, as shown in *Figure 10-1.* This is achieved because the CMOS EPROMs only draw current when their inputs or outputs switch, so 16k CMOS EPROMs can be replaced with 32k or even 64k EPROMs with no detectable increase in power consumption.

National's CMOS EPROMs use less dynamic standby power and also less read/write power. This results from the connection of chip enable ($\overline{CE}$) to extra transistors in the address and control inputs. If $\overline{CE}$ is not active, these transistors are OFF and no current flows—regardless of changing states on the inputs.

The difference in typical ratings is even more dramatic. When the memory is not selected, it is in the standby mode and draws minimum current. The maximum standby current for a typical 16k NMOS EPROM is 10 mA. The equivalent CMOS device has a maximum standby current rating of 1 μA: 1/1000th of the NMOS rating.

CMOS-NMOS INTERFACE COMPATIBILITY

National's CMOS EPROMs are designed to be compatible with NMOS EPROMs in pinout, drive capability and access speed. This allows direct replacement in systems where power consumption has grown to excessive levels with no penalty at all in performance.

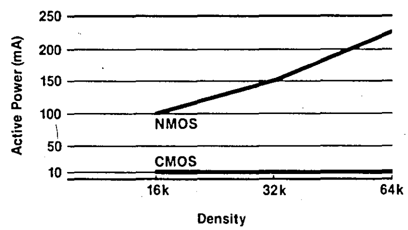


FIGURE 10-1. Power-Drain Dependence on Memory Density

National Semiconductor

PRELIMINARY

microCMOS

NMC27C16 16,384-Bit (2048 × 8) UV Erasable CMOS PROM

Parameter/Order Number	NMC27C16-35	NMC27C16-45 NMC27C16H-45
Access Time (ns)	350	450
V_{CC} Power Supply	5V ± 5%	5V ± 5%

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

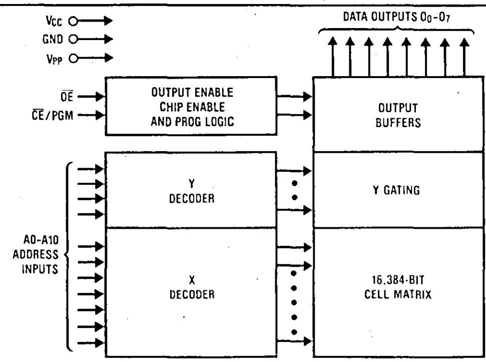
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, microCMOS silicon gate technology.

Features

- Access time down to 350 ns
- Low CMOS power consumption
  - Active power: 26.25 mW max
  - Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C16E-45), −40°C to +85°C, 450 ns ± 5% power supply
- 10 ms programming available (NMC27C16H-45), an 80% time savings
- Pin compatible to MM2716 and National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block and Connection Diagrams



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Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Dual-In-Line Package

NMC27C16 TOP VIEW

27C256 27256	27C128 27128	27C64 2764	27C32 2732	NMC27C16	Pin	Pin	NMC27C16	27C32 2732	27C64 2764	27C128 27128	27C256 27256
V_{PP}	V_{PP}	V_{PP}							V_{CC}	V_{CC}	V_{CC}
A12	A12	A12							$\overline{PGM}$	$\overline{PGM}$	A14
A7	A7	A7	A7	A7	1	24	V_{CC}	V_{CC}	NC	A13	A13
A6	A6	A6	A6	A6	2	23	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	3	22	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	4	21	V_{PP}	A11	A11	A11	A11
A3	A3	A3	A3	A3	5	20	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2	6	19	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	7	18	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0	8	17	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	9	16	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	10	15	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	11	14	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	12	13	O_3	O_3	O_3	O_3	O_3

TL/D/5275-2

NS Package Number J24A-Q

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16 pins.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND − 0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 9)

Temperature Range	
NMC27C16-35, NMC27C16-45, NMC27C16H-45	0°C to +70°C
NMC27C16E-45	−40°C to +85°C
V_{CC} Power Supply (Notes 2 and 3)	5V ± 5%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz, I/O = 0 mA		2	10	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE}$ = VIL, Inputs = V_{CC} or GND f = 1 MHz, I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Characteristics

Symbol	Parameter	Conditions	NMC27C16-35		NMC27C16E-45 NMC27C16-45 NMC27C16H-45		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		350		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		350		450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		120		120	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

NMC27C16

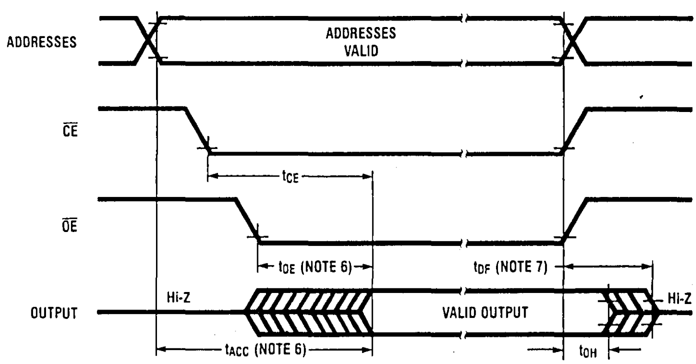
Capacitance (Note 5) ($T_A = +25°C$, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2)



TL/D/5275-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. $I_{CC1} \leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Note 11: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

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PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	μA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V

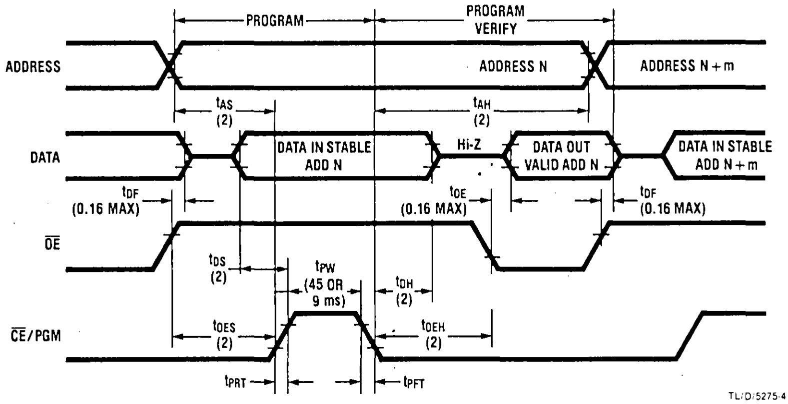
AC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	NMC27C16 Devices			NMC27C16H-45			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2			2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			2			μs
t_{DS}	Data Set-Up Time		2			2			μs
t_{AH}	Address Hold Time		2			2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			2			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		160	0		160	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			160			160	ns
t_{PW}	Program Pulse Width		45	50	55	9	10	11	ms
t_{PRT}	Program Pulse Rise Time		5			5			ns
t_{PFT}	Program Pulse Fall Time		5			5			ns

AC Test Conditions

V_{CC}	$5V \pm 5\%$
V_{PP}	$25V \pm 1V$
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3) ($V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$)



Note: All times shown in parentheses are minimum and in µs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C16 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C16 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

Read Mode

The NMC27C16 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Standby Mode

The NMC27C16 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C16 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the NMC27C16.

Initially, and after each erasure, all bits of the NMC27C16 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C16H-45), active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C16H-45). The NMC27C16 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming multiple NMC27C16s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled NMC27C16s.

TABLE I. MODE SELECTION

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C16s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel NMC27C16s may be common. A TTL level program pulse applied to an NMC27C16's $\overline{CE}$/PGM input with V_{PP} at 25V will program that NMC27C16. A low level $\overline{CE}$/PGM input inhibits the other NMC27C16 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å -4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C16 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C16 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27C16 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C16 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

NMC27C32

National Semiconductor

PRELIMINARY

microCMOS

NMC27C32 32,768-Bit (4096 × 8) UV Erasable CMOS PROM

Parameter/Order Number	NMC27C32-35	NMC27C32-45 NMC27C32H-45
Access Time (ns)	350	450
V_{CC} Power Supply	5V ± 5%	5V ± 5%

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

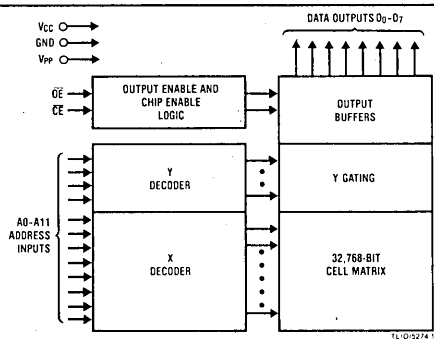
The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, microCMOS silicon gate technology.

Features

- Access time down to 350 ns
- Low CMOS power consumption
  Active power: 26.25 mW max
  Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C32E-45), −40°C to +85°C, 450 ns ± 5% power supply
- 10 ms programming available (NMC27C32H-45), an 80% time savings
- Pin compatible to NMC2732 and National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- Two-line control
- TRI-STATE® output

Block and Connection Diagrams



Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Dual-In-Line Package

27C256 27256	27C128 27128	27C64 2764	27C16 2716	NMC27C32 TOP VIEW	Pin	Pin	NMC27C32 TOP VIEW	27C16 2716	27C64 2764	27C128 27128	27C256 27256
V_{PP}	V_{PP}	V_{PP}							V_{CC}	V_{CC}	V_{CC}
A12	A12	A12							$\overline{PGM}$	$\overline{PGM}$	A14
A7	A7	A7	A7	A7	1	24	V_{CC}	V_{CC}	NC	A13	A13
A6	A6	A6	A6	A6	2	23	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	3	22	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	4	21	A11	VPP	A11	A11	A11
A3	A3	A3	A3	A3	5	20	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2	6	19	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	7	18	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0	8	17	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	9	16	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	10	15	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	11	14	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	12	13	O_3	O_3	O_3	O_3	O_3

NS Package Number J24A-Q

TL/D/5274-2

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32 pins.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND − 0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C32-35, NMC27C32-45, NMC27C32H-45	0°C to +70°C
NMC27C32E-45	−40°C to +85°C
V_{CC} Power Supply	5V ± 5%

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IH} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{CC} or GND, f = 1 MHz I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Characteristics

Symbol	Parameter	Conditions	NMC27C32-35		NMC27C32E-45 NMC27C32-45 NMC27C32H-45		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		350		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		350		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		150		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	130	0	130	ns
t_{OH} (Note 3)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

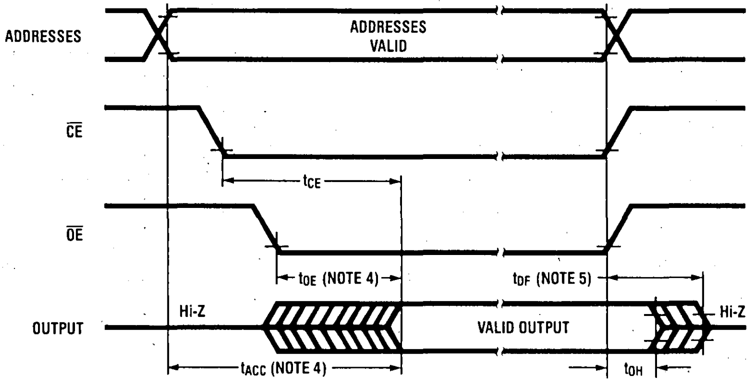
Capacitance (Note 3) ($T_A = +25°C$, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$		20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms



TL/D/5274-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to $V_{CC} + 0.3V$ to avoid latch-up and device damage.

PROGRAMMING (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{CC}$ or GND			10	μA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ μA	2.4			V
I_{CC}	V_{CC} Supply Current			2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0		$V_{CC} + 1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA

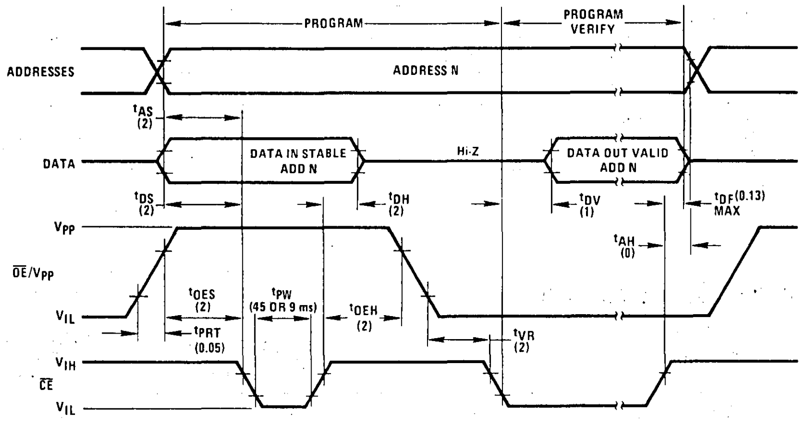
AC Programming Characteristics ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	NMC27C32 Devices			NMC27C32H-45			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2			2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			2			μs
t_{DS}	Data Set-Up Time		2			2			μs
t_{AH}	Address Hold Time		0			0			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			2			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Chip Enable to Output Float Delay		0		130	0		130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$			1			1	μs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	9	10	11	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			50			ns
t_{VR}	V_{PP} Recovery Time		2			2			μs

AC Test Conditions

V_{CC}	$5V \pm 5\%$
V_{PP}	$25V \pm 1V$
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)



TL/D/5274-4

Note: All times shown in parentheses are minimum and in μs unless otherwise specified. The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C32 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C32 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The NMC27C32 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The NMC27C32 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C32 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the NMC27C32.

Initially, and after each erasure, all bits of the NMC27C32 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC}, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C32H-45), active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C32H-45). The NMC27C32 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple NMC27C32s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32s.

Program Inhibit

Programming multiple NMC27C32s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C32s may be common. A TTL level program pulse applied to an NMC27C32's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that NMC27C32. A high level $\overline{CE}$ input inhibits the other NMC27C32s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

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Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C32 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C32 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27C32 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

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Section 11

COPS Microcontrollers

11

Introduction

National's family of COPS microcontrollers provides a flexible, cost-effective solution for all types of applications that require timing, counting, and other control functions. These microcontrollers can replace discrete logic, miniaturize, reduce component count, and/or add features in a wide variety of applications ranging from industrial systems to consumer products.

The COPS family was designed with the industry's most ROM-efficient instruction set. The result is that this controller often requires significantly less ROM to carry out a set of tasks than other 4-bit or 8-bit devices. The family incorporates:

- a common instruction set,
- a common architecture,
- a common pinout.

As your program progresses, COPS enables you to select the optimum device for the application. It is easy for a designer to vary the amount of 0.5k to 2k × 8 ROM and 32k to 128k × 4 RAM by simply specifying a different part number—the pinouts stay common. These package options, together with National's MICROWIRE serial communications protocol (which saves I/O lines and allows smaller packages), allow COPS to provide more features and more capabilities in your final product—and at the lowest possible cost.

USER SELECTABLE POWER CONSUMPTION

The device power consumption is truly selectable by the choice of power supply voltage and operating clock frequency. The devices operate over a wide range of power supply voltages, 2.4V to 5.5V, and operate over a wide range of clock frequency, DC to 4 MHz (this is as fast as NMOS COPS). The minimum power dissipation of 15 μW max occurs when the device is put into the halt mode (oscillator stopped). The device can easily be put into the halt mode by either a halt instruction or by forcing CKO high.

A unique feature of the COP424C and COP444C family of devices is the dual oscillator option. Under software control a D0 oscillator can be selected or a CKI oscillator. For example, a 1 MHz RC oscillator circuit could be selected as the D0 oscillator and a much lower frequency (i.e., 32 kHz) oscillator to CKI. The D0 oscillator would be selected where high speed processing is needed and the much lower frequency oscillator when minimum current drain and possibly only timekeeping is needed.

microCMOS COPS FOR EXTENDED TEMPERATURE RANGES

The microCMOS process allows extending the operating temperature range of the new COPS products from −55°C to +125°C. Now COPS address the harsh environment presented by both military and automotive applications. Special COPS devices will also be available that are processed to MIL-STD-883B.

TOTAL CMOS COPS DEVELOPMENT SUPPORT

The MOLE (Microcontroller On Line Emulator)* development system brings dedicated support to the COPS CMOS family of microcontrollers. Comprised of a brain board, personality board, software, and a choice of host computers, the new system lets you cross-assemble and download your program to the MOLE boards and perform real-time in-circuit emulation.

The MOLE system offers a low entrance cost by working with the host computer to reduce hardware and software duplication. By using the familiar host computer to do program editing and disk loading, the need to learn a new computer system is eliminated; code development is completed more rapidly.

MOLE software runs with a variety of host computers including National's STARPLEX I, STARPLEX II and COP400-PDS I/II, the popular Intellec Series II and MDS800 and other CP/M-80® systems, and even some popular personal computers.

Once the program is assembled, the code is downloaded over an RS-232 link to the MOLE brain and COPS CMOS personality board. The resident firmware then allows the MOLE to operate in a free-standing workstation mode by connecting a CRT (and printer, if hard copy is desired).

The MOLE has powerful debugging tools in the workstation mode including trace memory, multiple breakpoints, and single-step diagnostics, in addition to internal register and shared memory modifications.

The MOLE CMOS COPS system emulates the halt and idle on timer instructions important to power-down modes, as well as allowing V_{CC} operating voltages down to 2.7V. Additionally, the MOLE emulates the option configuration commands for dual clock, internal/external events, Microbus and frequency divide-by. These features ensure that the CMOS chip selected will be properly emulated in the circuit. The MOLE development system is ready to meet the needs of the CMOS design engineer, and remember, the MOLE also supports NMOS COPS and TMP.

*See data sheet, pg. 13-11, in Section 13 of this databook.

National Semiconductor

PRELIMINARY

microCMOS

COP404C ROMless CMOS Microcontrollers

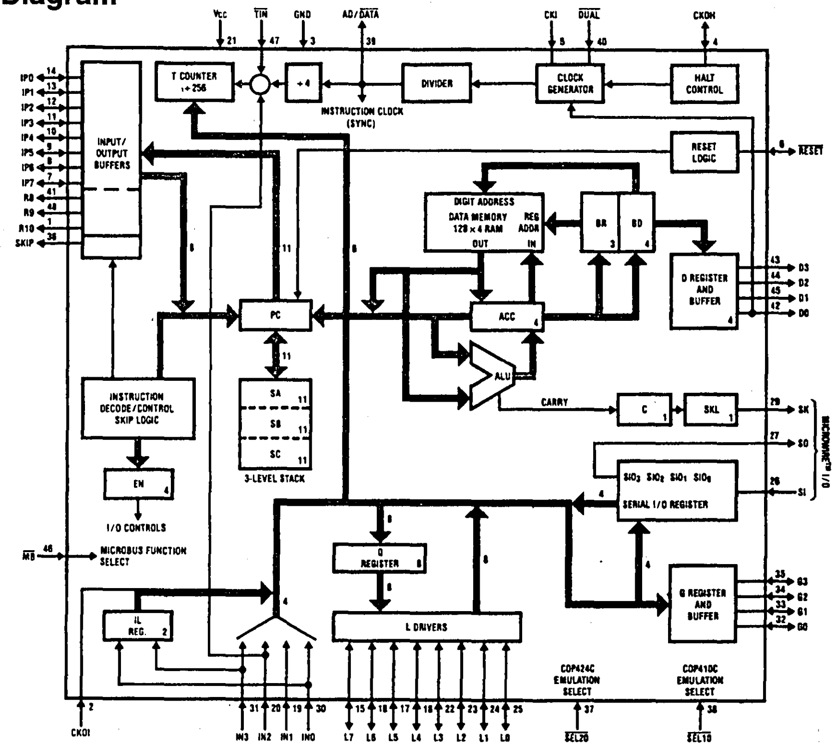
General Description

The COP404C ROMless Microcontroller is a member of the COPS™ family, fabricated using double-poly, silicon gate CMOS (microCMOS) technology. The COP404C contains CPU, RAM, I/O and is identical to a COP444C device except the ROM has been removed and pins have been added to output the ROM address and to input the ROM data. The COP404C can be configured, by means of external pins, to function as a COP444C, a COP424C, or a COP410C. Pins have been added to allow the user to select the various functional options that are available on the family of mask-programmed CMOS parts. The COP404C is primarily intended for use in the development and debug of a COP program for the COP444C/445C, COP424C/425C, and COP410C/411C devices prior to masking the final part. The COP404C is also appropriate in low volume applications or when the program might be changing.

Features

- Accurate emulation of the COP444C, COP424C and COP410C
- Lowest Power Dissipation (50 μW typical)
- Fully static (can turn off the clock)
- Power saving IDLE state and HALT mode
- 4 μs instruction time, plus software selectable clocks
- 128 $\times$ 4 RAM, addresses 2k $\times$ 8 ROM
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Single supply operation (2.4V to 5.5V)
- Programmable read/write 8-bit timer/event counter
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible
- MICROBUS™ compatible
- Software/hardware compatible with other members of the COP400 family

Block Diagram



TL/B/5530-1

FIGURE 1. Block Diagram

Absolute Maximum Ratings

Supply Voltage	6V
Voltage at any pin	$-0.3V$ to $V_{CC} + 0.3V$
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating temperature range	0° to +70°C
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 10 sec.)	300°C

DC Electrical Characteristics $0°C \leq T_a \leq 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Note 5)	peak to peak		$0.1\ V_{CC}$	V
Supply Current (Note 1)	$V_{CC}=2.4V$, $t_c=64\ \mu s$		120	μA
	$V_{CC}=5.0V$, $t_c=16\ \mu s$		700	μA
	$V_{CC}=5.0V$, $t_c=4\ \mu s$ (T_c is instruction cycle time)		3000	μA
HALT Mode Current (Note 2)	$V_{CC}=5.0V$, $F_{IN}=0$ kHz		40	μA
	$V_{CC}=2.4V$, $F_{IN}=0$ kHz		12	μA
Input Voltage Levels				
$\overline{RESET}$, D0 (clock input)				
CKI				
Logic High		$0.9\ V_{CC}$		V
Logic Low			$0.1\ V_{CC}$	V
All other inputs (Note 7)				
Logic High		$0.7\ V_{CC}$		V
Logic Low			$0.2\ V_{CC}$	V
Input Pull-up current	$V_{CC}=4.5V$, $V_{IN}=0$	30	330	μA
Hi-Z input leakage		−1	+1	μA
Input capacitance (Note 4)			7	pF
Output Voltage Levels	Standard outputs			
LSTTL Operation	$V_{CC}=5.0V \pm 5\%$			
Logic High	$I_{OH}=-100\ \mu A$	2.7		V
Logic Low	$I_{OL}=400\ \mu A$		0.4	V
CMOS Operation				
Logic High	$I_{OH}=-10\ \mu A$	$V_{CC}-0.2$		V
Logic Low	$I_{OL}=10\ \mu A$		0.2	V
Output current levels				
Sink (Note 6)	$V_{CC}=4.5V$, $V_{OUT}=V_{CC}$	1.2		mA
	$V_{CC}=2.4V$, $V_{OUT}=V_{CC}$	0.2		mA
Source (Standard option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	0.5		mA
	$V_{CC}=2.4V$, $V_{OUT}=0V$	0.1		mA
Source (Low current option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	30	330	μA
	$V_{CC}=2.4V$, $V_{OUT}=0V$	6	80	μA
Allowable Sink/Source current per pin (Note 6)			5	mA
Allowable Loading on CKOH			100	pF
Current needed to over-ride HALT (Note 3)				
To continue	$V_{CC}=4.5V$, $V_{IN}=2V_{CC}$		.7	mA
To halt	$V_{CC}=4.5V$, $V_{IN}=7V_{CC}$		1.6	mA
TRI-STATE leakage current		−2.5	+2.5	μA

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

COP404C

AC Electrical Characteristics $0°C \le T_A \le 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Instruction Cycle	$V_{CC} \ge 4.5V$	4	DC	µs
Time (t_c)	$4.5V > V_{CC} \ge 2.4V$	16	DC	µs
Operating CKI	$V_{CC} \ge 4.5V$	DC	1.0	MHz
Frequency	$4.5V > V_{CC} \ge 2.4V$	DC	250	kHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz external clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz external clock		40	ns
Instruction Cycle	$R = 30k$, $V_{CC} = 5V$			
Time using D0 as a	$C = 82$ pF	8	16	µs
RC Oscillator Dual-				
Clock Input (Note 4)				
INPUTS: (See *Fig. 3*)				
t_{SETUP}	G Inputs, $V_{CC} \ge 4.5V$	$T_c/4+.7$		µs
	SI Input, $V_{CC} \ge 4.5V$	0.3		µs
	IP Input, $V_{CC} \ge 4.5V$	1.0		µs
	All Others, $V_{CC} \ge 4.5V$	1.7		µs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		µs
	$4.5V > V_{CC} \ge 2.4V$	1.0		µs
OUTPUT PROPAGATION DELAY	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5K$			
IP7–IP0, A10–A8, SKIP				
t_{PD1}, t_{PD0}	$V_{CC} \ge 4.5V$		1.94	µs
	$4.5V > V_{CC} \ge 2.4V$		7.75	µs
AD/$\overline{DATA}$				
t_{PD1}, t_{PD0}	$V_{CC} \ge 4.5V$		375	ns
	$4.5V > V_{CC} \ge 2.4V$		1.5	µs
ALL OTHER OUTPUTS				
t_{PD1}, t_{PD0}	$V_{CC} > 4.5V$		1.0	µs
	$4.5V > V_{CC} \ge 2.4V$		4.0	µs
MICROBUS TIMING Read Operation (*Fig. 4*)	$C_L = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Chip select stable before $\overline{RD}$ $-t_{CSR}$		65		ns
Chip select hold time for $\overline{RD}$ $-t_{RCS}$		20		ns
$\overline{RD}$ pulse width $-t_{RR}$		400		ns
Data delay from $\overline{RD}$ $-t_{RD}$			375	ns
$\overline{RD}$ to data floating $-t_{DF}$ (Note 4)			250	ns
Write Operation (*Fig. 5*)				
Chip select stable before $\overline{WR}$ $-t_{CSW}$		65		ns
Chip select hold time for $\overline{WR}$ $-t_{WCS}$		20		ns
$\overline{WR}$ pulse width $-t_{WW}$		400		ns
Data set-up time for $\overline{WR}$ $-t_{DW}$		320		ns
Data hold time for $\overline{WR}$ $-t_{WD}$		100		ns
INTR transition time from $\overline{WR}$ $-t_{WI}$			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 16.

Note 2: Test conditions: All inputs tied to V_{CC}; L lines in TRI-STATE mode and tied to Ground; all outputs tied to Ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4: This parameter is only sampled and not 100% tested.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than 0.2 V_{CC} to prevent entering test mode.

Note 7: $\overline{MB}$, $\overline{TIN}$, $\overline{DUAL}$, $\overline{SEL10}$, $\overline{SEL20}$, Input levels at V_{CC} or V_{SS}.

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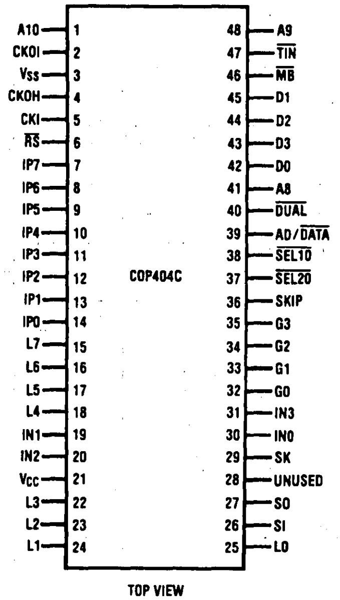
Connection Diagram



TL/B/5530-2

Order Number COP404CD or COP404CN
See NS Package D48A or N48A

Pin	Description
V_{CC}	Most positive voltage
V_{SS}	Ground
CKI	Clock input
$\overline{RS}$	Reset input
CKOI	General purpose input
L0–L7	8 TRI-STATE I/O
G0–G3	4 general purpose I/O
D1–D3	3 general purpose outputs
D0	Either general purpose output or Dual-Clock RC input
IN0–IN3	4 general purpose inputs
SO	Serial data output
SI	Serial data input
SK	Serial data clock output
IP0–IP7	I/O for ROM address and data
A8, A9, A10	3 address outputs
SKIP	Skip status output
AD/$\overline{DATA}$	Clock output
$\overline{MB}$	MICROBUS select input
CKOH	Halt I/O pin
$\overline{DUAL}$	Dual-Clock select input
$\overline{TIN}$	Timer input select pin
$\overline{SEL10}$	COP410C emulation select input
$\overline{SEL20}$	COP424C emulation select input
UNUSED	Ground

FIGURE 2

The internal architecture is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1", when a bit is reset, it is a logic "0".

PROGRAM MEMORY

Program Memory consists of a 2048-byte external memory (typically PROM). Words of this memory may be program instructions, constants or ROM addressing data.

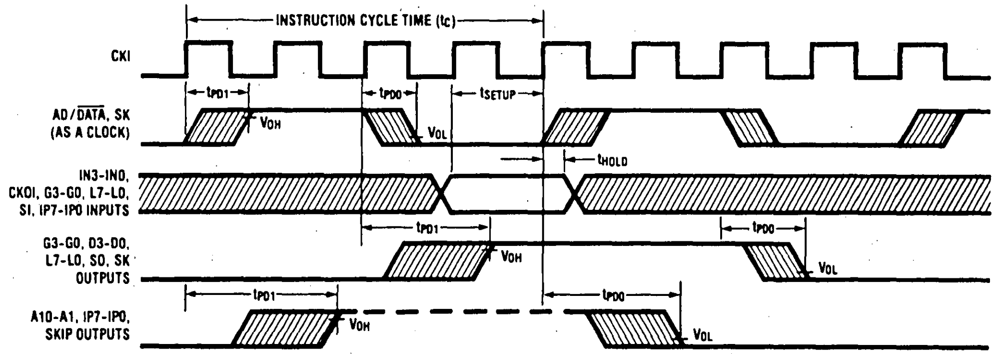
ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

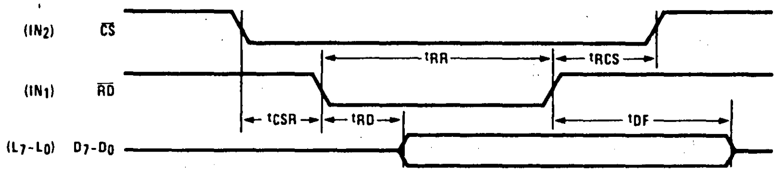
Data memory consists of a 512-bit RAM, organized as 8 data registers of 16 × 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (B_r) select 1 of 8 data registers and lower 4 bits (B_d) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or T counter or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions. The B_d register also serves as a source register for 4-bit data sent directly to the D outputs.

Timing Diagrams



TL/B/5530-3

FIGURE 3. Input/Output Timing



TL/B/5530-4

FIGURE 4. MICROBUS Read Operation Timing

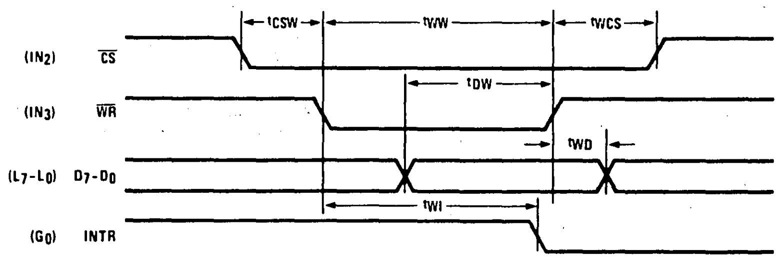


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FIGURE 5. MICROBUS Write Operation Timing

INTERNAL LOGIC

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the B_r and B_d portions of the B register, to load and input 4 bits of the 8-bit Q latch or T counter, L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be operated in two modes: as a timer if $\overline{\text{TIN}}$ pin is tied to Ground or as an external event counter if $\overline{\text{TIN}}$ pin is tied to V_{CC}. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in *Figure 10a*.

Four general-purpose inputs, IN3–IN0, are provided. IN1, IN2 and IN3 may be selected (by pulling $\overline{\text{MB}}$ pin low) as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of B_d. In the dual clock mode, D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be selected as an output for MICROBUS applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. With the MICROBUS option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O port. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS option allows L I/O port data to be latched into the Q register.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE™ I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

EN is an internal 4-bit register loaded by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register:

0. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output equals the value of EN3. With EN0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK outputs SKL ANDed with the instruction cycle clock.
1. With EN1 set, interrupt is enabled. Immediately following an interrupt, EN1 is reset to disable further interrupts.
2. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting EN2 disables the L drivers, placing the L I/O port in a high-impedance input state.
3. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected) SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to "0".

INTERRUPT

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once recognized as explained below, pushes the next sequential program counter address (PC+1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN1 is reset.

b. An interrupt will be recognized only on the following conditions:
   1. EN1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide has occurred on the IN1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g. if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

TABLE I. ENABLE REGISTER MODES — BITS EN0 AND EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL=1, SK=clock If SKL=0, SK=0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL=1, SK=clock If SKL=0, SK=0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of an ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to pop the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt service routine, since their popping of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

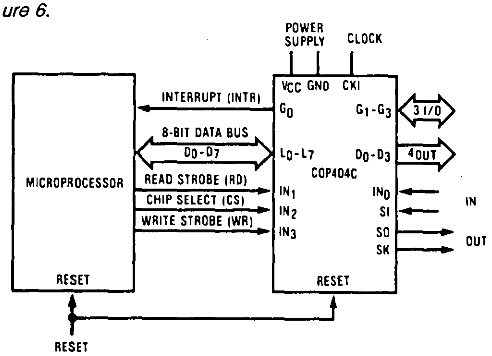
d. The instruction at hex address 0FF must be a NOP.

e. An LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

MICROBUS INTERFACE

With $\overline{MB}$ pin tied to Ground, the COP404C can be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (μP). IN1, IN2 and IN3 general purpose inputs become MICROBUS compatible read-strobe, chip-select, and write-strobe lines, respectively. IN1 becomes $\overline{RD}$ — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the μP. IN2 becomes $\overline{CS}$ — a logic "0" on this line selects the COP404C and the μP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the COP404C. G0 becomes INTR a "ready" output, reset by a write pulse from the μP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the COP404C.

This option has been designed for compatibility with National's MICROBUS - a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication). The functioning and timing relationships between the signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams (*Figures 4* and *5*). Connection of the COP404C to the MICROBUS is shown in *Figure 6*.



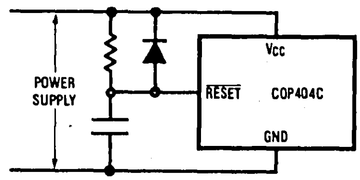
TL/B/5530-7

FIGURE 6. MICROBUS Option Interconnect

INITIALIZATION

The external RC network shown in *Figure 7* must be connected to the $\overline{RESET}$ pin for the internal reset logic to initialize the device upon power-up. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, providing it stays low for at least three instruction cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL latch is set, thus enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).



RC ≥ 5X POWER SUPPLY RISE TIME AND RC ≥ 100X CKI PERIOD.

TL/B/5530-8

FIGURE 7. Power-Up Circuit

TIMER

There are two modes selected by $\overline{TIN}$ pin:

a) Time-base counter ($\overline{TIN}$ pin low). In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The prescaler is cleared during execution of a CAMT instruction and on reset. For example, using a 1MHz crystal, the instruction cycle frequency of 250 kHz (divide by 4) increments the 10-bit timer every 4 μS. By presetting the counter and detecting overflow, accurate timeouts between 16 μS (4 counts) and 4.096 mS (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

b) External event counter ($\overline{TIN}$ pin high). In this mode, a low-going pulse ("1" to "0") at least 2 instruction cycles wide on the IN2 input will increment the 8-bit T counter.

Note: the IT instruction is not allowed in this mode.

HALT MODE

The COP404C is a FULLY STATIC circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may also be halted by two other ways (see *Figure 8*):

— Software HALT: by using the HALT instruction.

— Hardware HALT: by using the HALT I/O port CKOH. It is an I/O flip-flop which is an indicator of the HALT status. An external signal can over-ride this pin to start and stop the chip. By forcing CKOH high the chip will stop as soon as CKI is high and CKOH output will stay high to keep the chip stopped if the external driver returns to high impedance state.

Once in the HALT mode, the internal circuitry does not receive any clock signal and is therefore frozen in the exact state it was in when halted. All information is retained until continuing.

The chip may be awakened by one of two different methods:

- Continue function: by forcing CKOH low, the system clock will be re-enabled and the circuit will continue to operate from the point where it was stopped. CKOH will stay low.
- Restart: by forcing the $\overline{\text{RESET}}$ pin low (see Initialization)

The HALT mode is the minimum power dissipation state.

Note: if the user has selected dual-clock ($\overline{\text{DUAL}}$ pin tied to Ground) AND is forcing an external clock on D0 pin AND the COP404C is running from the D0 clock, the HALT mode - either hardware or software - will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the D0 clock to minimize power.

Oscillator Options

There are two basic clock oscillator configurations available as shown by *Figure 9.*

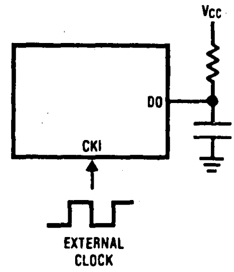
- CKI oscillator: CKI is configured as a LSTTL compatible input external clock signal. The external frequency is divided by 4 to give the instruction cycle time.
- Dual oscillator. By tying $\overline{\text{DUAL}}$ pin to Ground, pin D0 is now a single pin RC controlled Schmitt trigger oscillator input. The user may software select between the D0 oscillator (the instruction cycle time equals the D0 oscillation frequency divided by 4) by setting the D0 latch high or the CKI oscillator by resetting D0 latch low.

  Note that even in dual clock mode, the counter, if used as a time-base counter, is always connected to the CKI oscillator.

  For example, the user may connect up to a 1 MHz RC circuit to D0 for faster processing and a 32 kHz external clock to CKI for minimum current drain and time keeping.

Note: CTMA instruction is not allowed when the chip is running from D0 clock.

Figures 10a and *10b* show the timer and clock diagrams with and without Dual-Clock.



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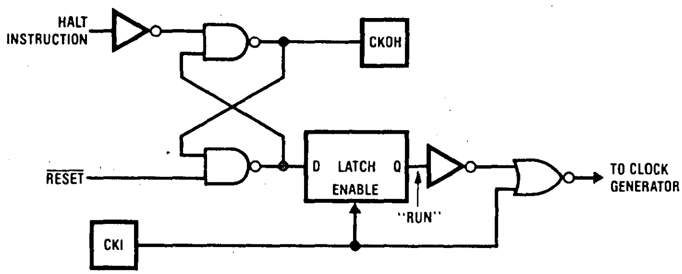
R	C	Cycle Time	V_{CC}
15k	82 pF	4–9 μs	≥4.5V
30k	82 pF	8–16 μs	≥4.5V
60k	100 pF	16–32 μs	2.4–4.5V

Note: $15k \leq R \leq 150k$

$50\ pF \leq C \leq 150\ pF$

FIGURE 9. Dual-Oscillator Component Values



TL/B/5530-10

FIGURE 8. HALT Mode

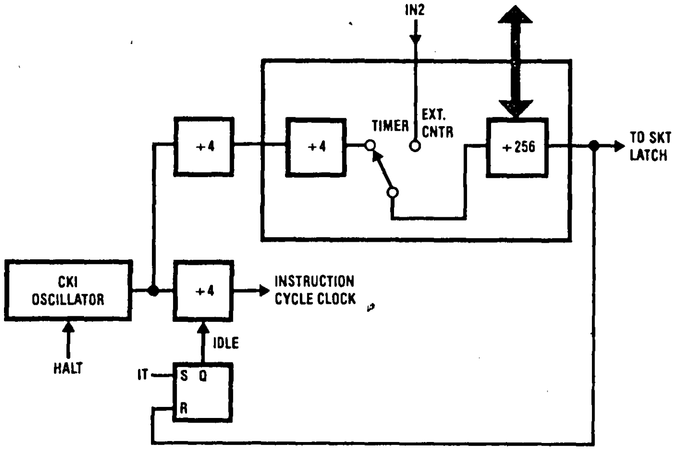


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FIGURE 10a. Clock and Timer Block Diagram without Dual-Clock

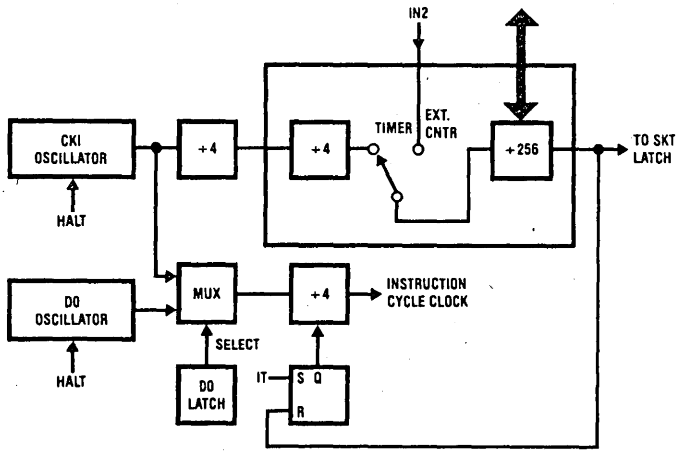

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Figure 10b. Clock and Timer Block Diagram with Dual-Clock

External Memory Interface

The COP404C is designed for use with an external Program Memory.

This memory may be implemented using any devices having the following characteristics:

1. random addressing
2. LSTTL or CMOS-compatible TRI-STATE outputs
3. LSTTL or CMOS-compatible inputs
4. access time = 1. 0 μs max.

Typically, these requirements are met using bipolar PROMs or MOS/CMOS PROMs, EPROMs or E²PROMs.

During operation, the address of the next instruction is sent out on A10, A9, A8 and IP7 through IP0 during the time that AD/$\overline{\text{DATA}}$ is high (logic "1" = address mode). Address data on the IP lines is stored into an external latch on the high-to-low transition of the AD/DATA line; A10, A9 and A8 are dedicated address outputs, and do not need to be latched. When AD/$\overline{\text{DATA}}$ is low (logic "0" = data mode), the output of the memory is gated onto IP7 through IP0, forming the input bus. Note that AD/$\overline{\text{DATA}}$ output has a period of one instruction time, a duty cycle of approximately 50%, and specifies whether the IP lines are used for address output or data input. A simplified block diagram of the external memory interface is shown in *Figure 11.*

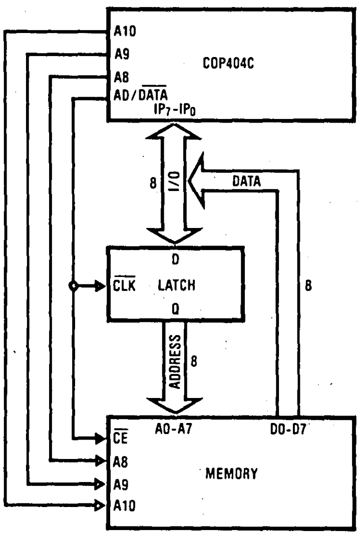

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FIGURE 11. External Memory Interface to COP404C

COP404C Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table III provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

Table II. Instruction Set Table Symbols

Symbol	Definition
Internal Architecture Symbols	
A	4-bit Accumulator
B	7-bit RAM address register
Br	Upper 3 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry register
D	4-bit Data output port
EN	4-bit Enable register
G	4-bit General purpose I/O port
IL	two 1-bit (IN0 and IN3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/O port
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA	11-bit Subroutine Save Register A
SB	11-bit Subroutine Save Register B
SC	11-bit Subroutine Save Register C
SIO	4-bit Shift register and counter
SK	Logic-controlled clock output
SKL	1-bit latch for SK output
T	8-bit timer
Instruction operand symbols	
d	4-bit operand field, 0–15 binary (RAM digit select)
r	3-bit operand field, 0–7 binary (RAM register select)
a	11-bit operand field, 0–2047
y	4-bit operand field, 0–15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x
Operational Symbols	
+	Plus
–	Minus
–>	Replaces
<–>	is exchanged with
=	Is equal to
$\overline{A}$	one's complement of A
⊕	exclusive-or
:	range of values

Instruction Set TABLE III (Continued)

TABLE: III. COP404C INSTRUCTION SET

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 0000	A+C+RAM(B) $\rightarrow$ A Carry $\rightarrow$ C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 0001	A+RAM(B) $\rightarrow$ A	None	Add RAM to A
ADT		4A	0011 0001	A+10_{10} $\rightarrow$ A	None	Add Ten to A
AISC	y	5–	0101 y	A+y $\rightarrow$ A	Carry	Add Immediate. Skip on Carry (y$\neq$ 0)
CASC		10	0001 0000	$\overline{A}$+RAM(B)+C $\rightarrow$ A Carry $\rightarrow$ C	Carry	Compliment and Add with Carry, Skip on Carry
CLRA		00	0000 0000	0 $\rightarrow$ A	None	Clear A
COMP		40	0100 0000	$\overline{A}$ $\rightarrow$ A	None	Ones complement of A to A
NOP		44	0100 0100	None	None	No Operation
RC		32	0011 0010	"0" $\rightarrow$ C	None	Reset C
SC		22	0010 0010	"1" $\rightarrow$ C	None	Set C
XOR		02	0000 0010	A $\oplus$ RAM(B) $\rightarrow$ A	None	Exclusive-OR RAM with A
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111 1111	ROM ($PC_{10:8}$ A,M) $\rightarrow$ $PC_{7:0}$	None	Jump Indirect (note 2)
JMP	a	6– —	0110 0 $a_{10:8}$ $a_{7:0}$	a $\rightarrow$ PC	None	Jump
JP	a	— —	1 $a_{6:0}$ (pages 2,3 only) or 11 $a_{5:0}$ (all other pages)	a $\rightarrow$ $PC_{6:0}$ a $\rightarrow$ $PC_{5:0}$	None	Jump within Page (Note 3)
JSRP	a	—	10 $a_{5:0}$	PC+1 $\rightarrow$ SA $\rightarrow$ SB $\rightarrow$ SC 00010 $\rightarrow$ $PC_{10:6}$ a $\rightarrow$ $PC_{5:0}$	None	Jump to Subroutine Page (Note 4)
JSR	a	6– —	0110 1 $a_{10:8}$ $a_{7:0}$	PC+1 $\rightarrow$ SA $\rightarrow$ SB $\rightarrow$ SC a $\rightarrow$ PC	None	Jump to Subroutine
RET		48	0100 1000	SC $\rightarrow$ SB $\rightarrow$ SA $\rightarrow$ PC	None	Return from Subroutine
RETSK		49	0100 1001	SC $\rightarrow$ SB $\rightarrow$ SA $\rightarrow$ PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33 38	0011 0011 0011 1000		None	HALT processor
IT		33 39	0011 0011 0011 1001		None	IDLE till timer overflows then continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33 3F	0011 0011 0011 1111	A $\rightarrow$ $T_{7:4}$ RAM(B) $\rightarrow$ $T_{3:0}$	None	Copy A, RAM to T
CTMA		33 2F	0011 0011 0010 1111	$T_{7:44}$ $\rightarrow$ RAM(B) $T_{3:0}$ $\rightarrow$ A	None	Copy T to RAM, A
CAMQ		33 3C	0011 0011 0011 1100	A $\rightarrow$ $Q_{7:4}$ RAM(B) $\rightarrow$ $Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	0011 0011 0010 1100	$Q_{7:4}$ $\rightarrow$ RAM(B) $Q_{3:0}$ $\rightarrow$ A	None	Copy Q to RAM, A
LD	r	–5	00 r 0101 (r=0:3)	RAM(B) $\rightarrow$ A Br$\oplus$ r $\rightarrow$ Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 —	0010 0011 0 r d	RAM(r,d) $\rightarrow$ A	None	Load A with RAM pointed to direct by r,d
LQID		BF	1011 1111	ROM($PC_{10:8,A,M}$) $\rightarrow$ Q SB $\rightarrow$ SC	None	Load Q Indirect (Note 2)
RMB	0	4C	0100 1100	0 $\rightarrow$ $RAM(B)_0$	None	Reset RAM Bit
	1	45	0100 0101	0 $\rightarrow$ $RAM(B)_1$		
	2	42	0100 0010	0 $\rightarrow$ $RAM(B)_2$		
	3	43	0100 0011	0 $\rightarrow$ $RAM(B)_3$		

Instruction Set TABLE III (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SMB	0	4D	|0100|1101|	1 → RAM(B)$_0$	None	Set RAM Bit
	1	47	|0100|0111|	1 → RAM(B)$_1$		
	2	46	|0100|0110|	1 → RAM(B)$_2$		
	3	4B	|0100|1011|	1 → RAM(B)$_3$		
STII	y	7–	|0111| y |	y → RAM(B) Bd ⊕ 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	–6	|00| r |0110| (r=0:3)	RAM(B) → A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 —	|0010|0011| |1| r | d |	RAM(r,d) → A	None	Exchange A with RAM pointed to directly by r,d
XDS	r	–7	|00| r |0111| (r=0:3)	RAM(B) → A Bd–1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd. Exclusive-OR Br with r
XIS	r	–4	|00| r |0100| (r=0:3)	RAM(B) → A Bd+1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTIONS

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
CAB		50	|0101|0000|	A → Bd	None	Copy A to Bd
CBA		4E	|0100|1110|	Bd → A	None	Copy Bd to A
LBI	r,d	—	|00| r |(d-1)| (r=0:3: d=0,9:15) or	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 5)
		33 —	|0011|0011| |1| r | d | (any r, any d)			
LEI	y	33 6–	|0011|0011| |0110| y |	y → EN	None	Load EN Immediate (Note 6)
XABR		12	|0001|0010|	A ←→ Br	None	Exchange A with Br (Note 7)

TEST INSTRUCTIONS

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SKC		20	|0010|0000|		C="1"	Skip if C is True
SKE		21	|0010|0001|		A=RAM(B)	Skip if A Equals RAM
SKGZ		33 21	|0011|0011| |0010|0001|		$G_{3:0}$=0	Skip if G is Zero (all 4 bits)
SKGBZ		33	|0011|0011|	1st byte		Skip if G Bit is Zero
	0	01	|0000|0001|	2nd byte	G_0=0	
	1	11	|0001|0001|		G_1=0	
	2	03	|0000|0011|		G_2=0	
	3	13	|0001|0011|		G_3=0	
SKMBZ	0	01	|0000|0001|		RAM(B)$_0$=0	Skip if RAM Bit is Zero
	1	11	|0001|0001|		RAM(B)$_1$=0	
	2	03	|0000|0011|		RAM(B)$_2$=0	
	3	13	|0001|0011|		RAM(B)$_3$=0	
SKT		41	|0100|0001|		A time-base counter carry has occured since last test	Skip on Timer (Note 2)

Instruction Set TABLE III (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
INPUT/OUTPUT INSTRUCTIONS						
ING		33	|0011|0011|	G → A	None	Input G Ports to A
		2A	|0010|1010|			
ININ		33	|0011|0011|	IN → A	None	Input IN Inputs to A
		28	|0010|1000|			
INIL		33	|0011|0011|	IL_3, CKO, "0", IL_0 → A	None	Input IL Latches to A (Note 2)
		29	|0010|1001|			
INL		33	|0011|0011|	$L_{7:4}$ → RAM(B)	None	Input L Ports to RAM,A
		2E	|0010|1110|	$L_{3:0}$ → A		
OBD		33	|0011|0011|	Bd → D	None	Output Bd to D Outputs
		3E	|0011|1110|			
OGI	y	33	|0011|0011|	y → G	None	Output to G Ports Immediate
		5–	|0101| y |			
OMG		33	|0011|0011|	RAM(B) → G	None	Output RAM to G Ports
		3A	|0011|1010|			
XAS		4F	|0100|1111|	A ←→ SIO, C → SKL	None	Exchange A with SIO (Note 2)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 3: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 4: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 5: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B(Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 6: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Note 7: If $\overline{SEL20}$ = 1, A ←→ Br (0 → A3)
If $\overline{SEL20}$ = 0, A ←→ Br (0,0 → A3, A2).

XAS INSTRUCTION

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10: PC8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows: A → PC (7:4), RAM(B) → PC(3:0), leaving PC(10), PC(9) and PC(8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost.

Note: LQID uses 2 instruction cycles if executed, one if skipped.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10: 8, A, M. PC10, PC9 and PC8 are not affected by JID.

Note: JID uses 2 instruction cycles if executed, one if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal

Note: If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter:

```
CAMT    ; load T counter
SKT     ; skip if overflow flag is set and reset it
NOP
```

IT INSTRUCTION

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped. IT instruction is not allowed if the T counter is used as an external event counter ($\overline{TIN}$ pin tied to V_{CC}).

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKOI and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. The state of CKOI is input into A2. A 0 is input into A1. IL latches are cleared on reset.

Instruction Set Notes

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Power Dissipation

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, for minimum power dissipation, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. For example, an RC oscillator on D0 will draw more current than a square wave clock input since it is a slow rising signal.

If using an external square wave oscillator, the following equation can be used to calculate the COP404C operating current drain:

$$I_{co} = I_q + V \times 40 \times F_i + V \times 1400 \times F_i / 4$$

where:

I_{co} = chip operating current drain in microamps

I_q = quiescent leakage current (from curve)

F_i = CKI frequency in MegaHertz

V = chip V_{CC} in volts

For example at 5 volts V_{CC} and 400 kHz:

$$I_{co} = 20 + 5 \times 40 \times .4 + 5 \times 1400 \times .4 / 4$$

$$I_{co} = 20 + 80 + 700 = 800\ \mu A$$

at 2.4 volts V_{CC} and 30 kHz:

$$I_{co} = 6 + 2.4 \times 40 \times .03 + 2.4 \times 1400 \times .03/4$$

$$I_{co} = 6 + 2.88 + 25.2 = 34.08\ \mu A$$

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation:

$$I_{ci} = I_q + V \times 40 \times F_i$$

For example, at 5 volts V_{CC} and 400 kHz

$$I_{ci} = 20 + 5 \times 40 \times .4 = 100\ \mu A$$

The total average current will then be the weighted average of the operating current and the idle current:

$$Ita = Ico \times \frac{To}{To + Ti} + Ici \times \frac{Ti}{To + Ti}$$

where:

I_{ta} = total average current

I_{co} = operating current

I_{ci} = idle current

T_o = operating time

T_i = idle time

I/O OPTIONS

COP404C outputs have the following configurations, illustrated in *Figure 12*.

a. Standard — A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL. (Used on SO, SK, AD/$\overline{DATA}$, SKIP, A10:8 and D outputs.)

b. Low Current — This is the same configuration as a. above except that the sourcing current is much less. (Used on G outputs.)

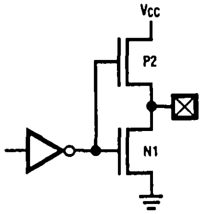
c. Standard TRI-STATE L Output — A CMOS output buffer similar to a. which may be disabled by program control. (Used on L outputs.)

All inputs have the following configuration:

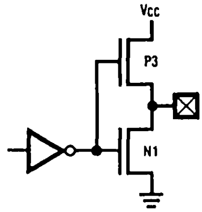
d. Input with on chip load device to V_{CC}. (Used on CKOI.)

e. HI-Z input which must be driven by the users logic. (Used on CKI, $\overline{RESET}$, IN, SI, $\overline{DUAL}$, $\overline{TIN}$, $\overline{MB}$, $\overline{SEL10}$ and $\overline{SEL20}$ inputs.)

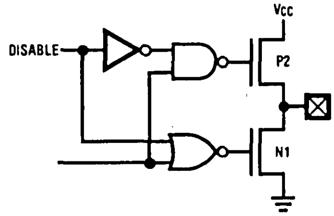
All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 13* for each of these devices to allow the designer to effectively use these I/O configurations.



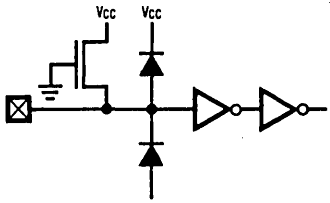
a. Standard Push-Pull Output



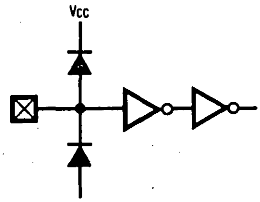
b. Low Current Push-Pull Output



Standard TRI-STATE "L" Output



d. Input with Load



e. Hi-Z Input

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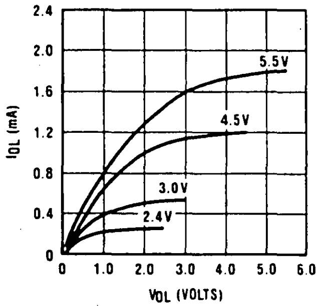
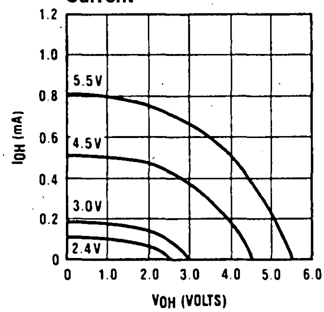
FIGURE 12. Input/Output Configurations

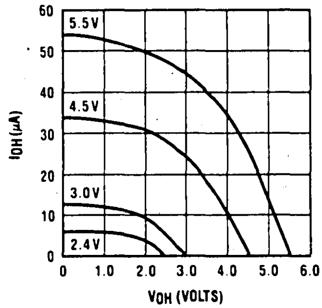
Minimum Sink Current



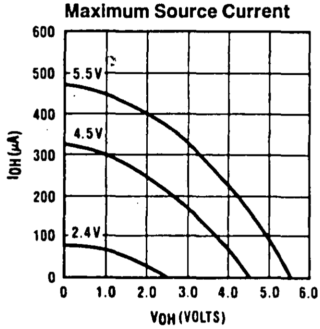
Standard Minimum Source Current



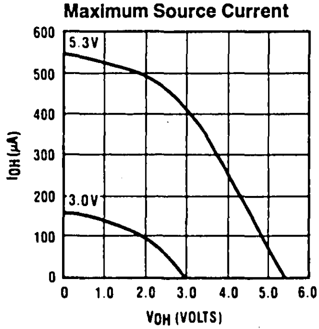
Low Current Option Minimum Source Current



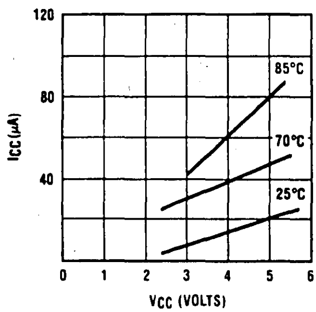
Low Current Option Maximum Source Current



Low Current Option Maximum Source Current



Maximum Quiescent Current



TL/B/5530–16

FIGURE 13. Input/Output Characteristics

Emulation

The COP404C may be used to exactly emulate the COP444C/445C, COP424C/425C, and COP410C/411C. However, the Program Counter always addresses 2k of external ROM whatever chip is being emulated. *Figure 14* shows the interconnect to implement a hardware emulation. This connection uses a NMC27C16 EPROM as external memory. Other memory can be used such as bipolar PROM or RAM.

Pins IP7–IP0 are bidirectional inputs and outputs. When the AD/$\overline{\text{DATA}}$ clocking output turns on, the EPROM drivers are disabled and IP7–IP0 output addresses. The 8-bit latch (MM74C373) latches the addresses to drive the memory.

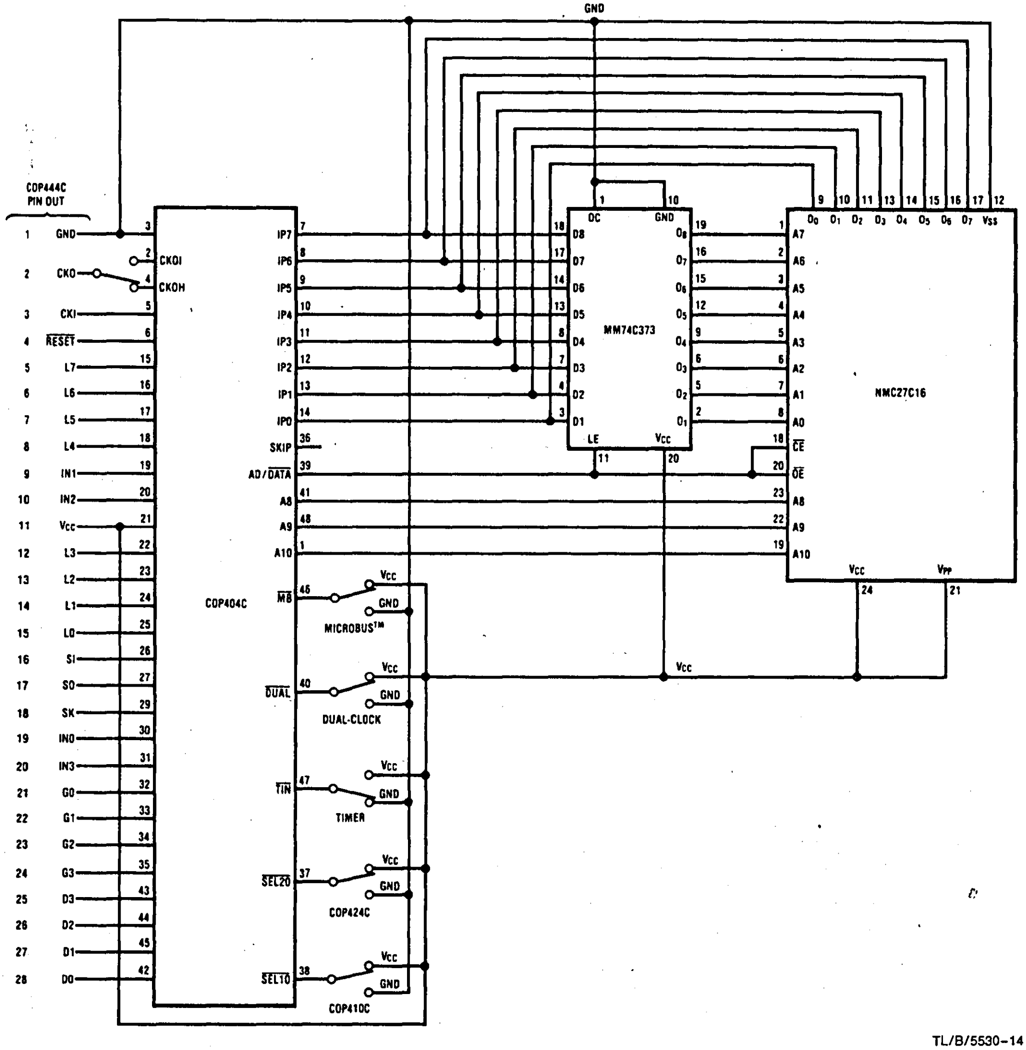


FIGURE 14. COP404C Used To Emulate A COP444C

When AD/$\overline{\text{DATA}}$ turns off, the EPROM is enabled and the IP7–IP0 pins will input the memory data. A10, A9 and A8 output the most significant address bits to the memory. (SKIP output may be used for program debug if needed.)

— CKI is divided by 4. Other divide-by are emulated by external divider.

— CKO can be emulated as a general purpose input by using CKOI or as a Halt I/O port by using CKOH.

— $\overline{\text{MB}}$ pin can be pulled low if the MICROBUS feature of the COP444C and COP424C is needed. Othewise it should be high.

— $\overline{\text{DUAL}}$ pin can be pulled low if the Dual-Clock feature of the COP444C and COP424C is needed. Otherwise it should be high.

— $\overline{\text{TIN}}$ pin controls the input of the 8-bit timer of the COP444C and COP424C (internal timer if $\overline{\text{TIN}}$ is low, external event counter if $\overline{\text{TIN}}$ is high).

— The $\overline{\text{SEL10}}$ and $\overline{\text{SEL20}}$ inputs are used to emulate the COP444C/445C, COP424C/425C, or COP410C/411C.

- When emulating the COP444C/445C, the user must configure $\overline{\text{SEL20}}$ = 1 and $\overline{\text{SEL10}}$ = 1.
- When emulating the COP424C/425C, the user must configure $\overline{\text{SEL20}}$ = 0 and $\overline{\text{SEL10}}$ = 1. In this mode, the user RAM is physically halved. As in the COP424C/425C, the user has 64 digits (256 bits) of RAM available. Pin A10 should not be connected to the program memory (most significant address bit of the program memory should be grounded if using a 2k×8 memory).
- When emulating the COP410C/411C, the user must configure $\overline{\text{SEL20}}$ = 0 and $\overline{\text{SEL10}}$ = 0. In this mode, the user has 32 digits (128 bits) of RAM available organized in the same way as the COP410C/411C - 4 registers of 8 digits each. Pins A10 and A9 should not be connected to the program memory (the 2 most significant address bits of the program memory should be grounded).

Furthermore, the subroutine stack is decreased from 3 levels to 2 levels.

The pins $\overline{\text{SEL10}}$ and $\overline{\text{SEL20}}$ change the internal logic of the device to accurately emulate the devices as indicated above. However, the user must remember that the COP424C/425C is a subset of the COP444C/COP445C with respect to memory size. The COP410C/411C is a subset both in memory size and in function. The user must take care not to use features and instructions which are not available on the COP410C/411C (see table IV. below) when using the COP404C to emulate the COP410C/411C.

TABLE IV. FEATURES AND INSTRUCTIONS NOT AVAILABLE ON COP410C/411C.

Timer	ADT		
Dual-clock	CASC		
Interrupt	CAMT		
Microbus	CTMA		
	IT		
	LDD	r, d	
	XAD	r, d	(except 3, 15)
	XABR		
	SKT		
	ININ		
	INIL		
	OGI	y	

COP404C MAS OPTIONS

The following COP444C options have been implemented in the COP404C:

Option value	Comment
Option 1 = 0	Ground Pin -- no option available
Option 2 = 1, 2	CKO is replaced by CKOI and CKOH
Option 3 = 5	CKI is external clock input divided by 4
Option 4 = 1	$\overline{\text{RESET}}$ is Hi-Z input
Option 5-8 = 0	L outputs are standard TRI-STATE
Option 9 = 1	IN1 is a Hi-Z input
Option 10 = 1	IN2 is a Hi-Z input
Option 11 = 0	V_{CC} pin -- no option available
Option 12-15 = 0	L outputs are standard TRI-STATE
Option 16 = 0	SI is a Hi-Z input
Option 17 = 0	SO is a standard output
Option 18 = 0	SK is a standard output
Option 19 = 1	IN0 is a Hi-Z input
Option 20 = 1	IN3 is a Hi-Z input
Option 21-24 = 1	G outputs are low-current
Option 25-28 = 0	D outputs are standard
Option 29 = 1	No internal initialization logic
Option 30 = 0, 1	DUAL-CLOCK is pin selectable
Option 31 = 0, 1	TIMER is pin selectable
Option 32 = 0, 1	MICROBUS is pin selectable
Option 33 = N/A	48-pin package

National Semiconductor

microCMOS

COP410C/COP411C, COP310C/COP311C and COP210C/COP211C Single-Chip CMOS Microcontrollers

General Description

The COP410C, COP411C, COP310C, COP311C, COP210C, and COP211C fully static, single-chip CMOS microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon-gate CMOS technology. These controller-oriented processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and BCD data manipulation. The COP411C is identical to the COP410C but with 16 I/O lines instead of 20. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller-oriented processor at a low end-product cost.

The COP310C/COP311C is the extended temperature range version of the COP410C/COP411C, and the COP210C/COP211C is the military temperature range version of the COP410C/COP411C.

Features

- Lowest power dissipation (40μW typical)
- Low cost
- Power-saving HALT mode with Continue function
- Powerful instruction set
- 512 × 8 ROM, 32 × 4 RAM
- 20 I/O lines (COP410C)
- Two-level subroutine stack
- DC to 4μs instruction time
- Single supply operation (2.4V to 5.5V)
- General purpose and TRI-STATE® outputs
- Internal binary counter register with MICROWIRE™ compatible serial I/O
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with other members of the COP400 family
- Extended temperature (−40°C to +85°C) devices available
- Military temperature (−55°C to +125°C) devices to be available. **Note:** At time of printing electrical specifications were not available.

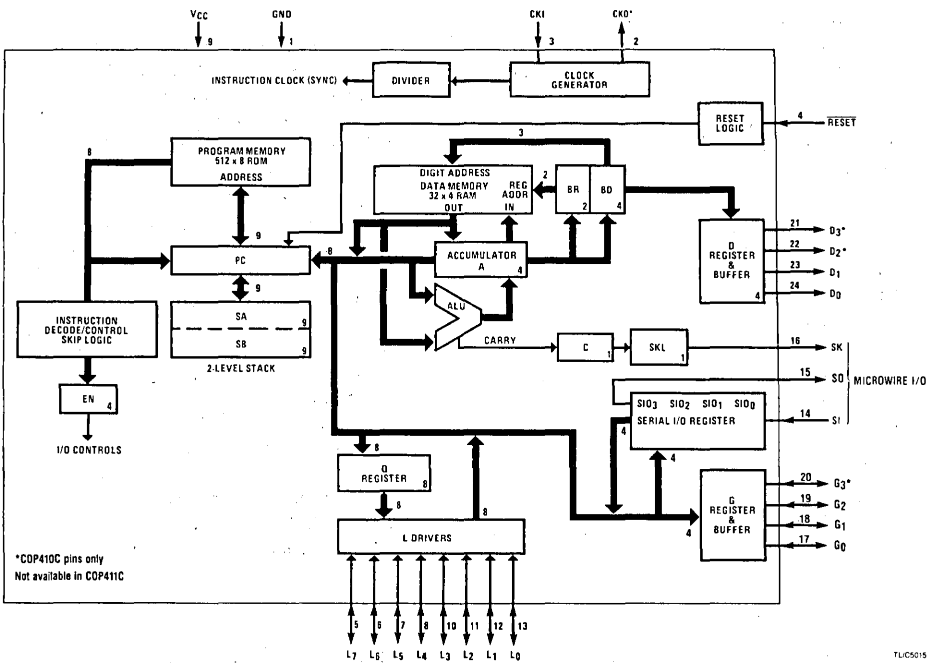


FIGURE 1. COP410C/411C Block Diagram

COP410C/COP411C

Absolute Maximum Ratings

Voltage at any pin	−0.3V to V_{CC}+0.3V
Total allowable source current	25mA
Total allowable sink current	25mA
Operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 10 sec.)	300°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics 0°C ≤ T_A ≤ 70°C unless otherwise specified

Parameter	Conditions	Min.	Max.	Units
Operating Voltage		2.4	5.5	V
Supply Current[1]	V_{CC} = 2.4V, t_c = 125μs V_{CC} = 5.0V, t_c = 16μs V_{CC} = 5.0V, t_c = 4μs (t_c is instruction cycle time)		80 500 2000	μA μA μA
HALT Mode Current[2]	V_{CC} = 5.0V, F_{IN} = 0kHz V_{CC} = 2.4V, F_{IN} = 0kHz		30 10	μA μA
Input Voltage Levels				
RESET, CKI				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Hi-Z Input Leakage		−1	+1	μA
Input Capacitance			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	V_{CC} = 5.0V ± 5%			
Logic High	I_{OH} = 25μA	2.7		V
Logic Low	I_{OL} = 400μA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10μA	V_{CC} − 0.2		V
Logic Low	I_{OL} = 10μA		0.2	V
Output Current Levels				
Sink	V_{CC} = 4.5V, V_{OUT} = V_{CC} V_{CC} = 2.4V, V_{OUT} = V_{CC}	1.2 0.2		mA mA
Source (Standard Option)	V_{CC} = 4.5V, V_{OUT} = 0V V_{CC} = 2.4V, V_{OUT} = 0V	0.5 0.1		mA mA
Source (Low Current Option)	V_{CC} = 4.5V, V_{OUT} = 0V V_{CC} = 2.4V, V_{OUT} = 0V	30 6	330 80	μA μA

COP410C/COP411C

DC Electrical Characteristics (continued)

Parameter	Conditions	Min.	Max.	Units
CKO Current Levels (As Clock Out)				
Sink ÷4	$V_{CC}=4.5V$, $CKI=V_{CC}$, $V_{OUT}=V_{CC}$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	$V_{CC}=4.5V$, $CKI=0V$, $V_{OUT}=0V$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Allowable Loading on CKO (as HALT I/O pin)			100	pF
Current Needed to Override HALT[3]				
To Continue	$V_{CC}=4.5V$, $V_{IN}=0.2\ V_{CC}$		0.6	mA
To Halt	$V_{CC}=4.5V$, $V_{IN}=0.7\ V_{CC}$		1.6	mA
TRI-STATE or Open Drain Leakage Current		−2	+2	μA

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 13.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations.

Note 3: When forcing HALT, current is only needed for a short time (approximately 200ns) to flip the HALT flip-flop.

COP410C/COP411C

AC Electrical Characteristics $0°C \leq T_A \leq 70°C$ unless otherwise specified

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time (t_c)	$V_{CC} \geq 4.5V$	4	DC	μs
	$4.5V > V_{CC} \geq 2.4V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \geq 4.5V$	DC	1.0	MHz
÷8 mode		DC	2.0	MHz
÷16 mode		DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \geq 2.4V$	DC	250	kHz
÷8 mode		DC	500	kHz
÷16 mode		DC	1.0	MHz
Instruction Cycle Time RC Oscillator	$R=30k \pm 5\%$, $V_{CC}=5V$, $C=82pF \pm 5\%$ (÷4 Mode)	8	16	μs
Inputs (See Figure 3)				
t_{SETUP}	G Inputs, $V_{CC} \geq 4.5V$	tc/4+0.7		μs
	SI Input, $V_{CC} \geq 4.5V$	0.3		μs
	All Others, $V_{CC} \geq 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		μs
	$V_{CC} \geq 2.4V$	1.0		μs
Output Propagation Delay	$V_{OUT}=1.5V$, $C_L=100pF$, $R_L=5k$			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$V_{CC} \geq 2.4V$		4.0	μs

COP310C/COP311C

Absolute Maximum Ratings

Voltage at any pin	−0.3V to V_{CC}+0.3V
Total allowable source current	25mA
Total allowable sink current	25mA
Operating temperature range	−40°C to +85°C
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 10 sec.)	300°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics $-40°C \leq T_A \leq +85°C$ unless otherwise specified

Parameter	Conditions	Min.	Max.	Units
Operating Voltage		3.0	5.3	V
Supply Current[1]	$V_{CC}=3.0V$, $t_c=125\mu s$		100	μA
	$V_{CC}=5.0V$, $t_c=16\mu s$		600	μA
	$V_{CC}=5.0V$, $t_c=4\mu s$		2500	μA
	(t_c is instruction cycle time)			
HALT Mode Current[2]	$V_{CC}=5.0V$, $F_{IN}=0kHz$		50	μA
	$V_{CC}=3.0V$, $F_{IN}=0kHz$		20	μA
Input Voltage Levels				
RESET, CKI				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All Other Inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Hi-Z Input Leakage		−2	+2	μA
Input Capacitance			7	pF
Output Voltage Levels	Standard Outputs			
LSTTL Operation	$V_{CC}=5.0V \pm 5\%$			
Logic High	$I_{OH}=25\mu A$	2.7		V
Logic Low	$I_{OL}=400\mu A$		0.4	V
CMOS Operation				
Logic High	$I_{OH}=-10\mu A$	$V_{CC}-0.2$		V
Logic Low	$I_{OL}=10\mu A$		0.2	V
Output Current Levels				
Sink	$V_{CC}=4.5V$, $V_{OUT}=V_{CC}$	1.2		mA
	$V_{CC}=3.0V$, $V_{OUT}=V_{CC}$	0.2		mA
Source (Standard Option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	0.5		mA
	$V_{CC}=3.0V$, $V_{OUT}=0V$	0.1		mA
Source (Low Current Option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	30	440	μA
	$V_{CC}=3.0V$, $V_{OUT}=0V$	8	200	μA

COP310C/COP311C

DC Electrical Characteristics (continued)

Parameter	Conditions	Min.	Max.	Units
CKO Current Levels (As Clock Out)				
Sink ÷4	$V_{CC} = 4.5V$, $CKI = V_{CC}$, $V_{OUT} = V_{CC}$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	$V_{CC} = 4.5V$, $CKI = 0V$, $V_{OUT} = 0V$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Allowable Loading on CKO (as HALT I/O pin)			100	pF
Current Needed to Override HALT[3]				
To Continue	$V_{CC} = 4.5V$, $V_{IN} = 0.2\ V_{CC}$		0.8	mA
To Halt	$V_{CC} = 4.5V$, $V_{IN} = 0.7\ V_{CC}$		2.0	mA
TRI-STATE or Open Drain Leakage Current		−4	+4	μA

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 13.

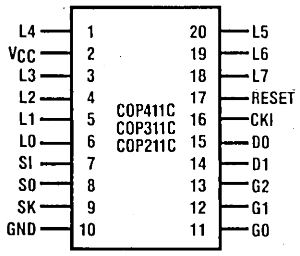
Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations.

Note 3: When forcing HALT, current is only needed for a short time (approximately 200ns) to flip the HALT flip-flop.

COP310C/COP311C

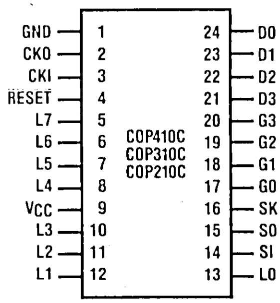
AC Electrical Characteristics $-40°C \leq T_A \leq +85°C$ unless otherwise specified

Parameter	Conditions	Min.	Max.	Units
Instruction Cycle Time (t_c)	$V_{CC} \geq 4.5V$	4	DC	μs
	$4.5V > V_{CC} \geq 3.0V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \geq 4.5V$	DC	1.0	MHz
÷8 mode		DC	2.0	MHz
÷16 mode		DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \geq 3.0V$	DC	250	kHz
÷8 mode		DC	500	kHz
÷16 mode		DC	1.0	MHz
Instruction Cycle Time RC Oscillator	$R = 30k \pm 5\%$, $V_{CC} = 5V$, $C = 82pF \pm 5\%$ (÷4 Mode)	8	16	μs
Inputs (See Figure 3)				
t_{SETUP}	G Inputs, $V_{CC} \geq 4.5V$	tc/4+0.7		μs
	SI Input, $V_{CC} \geq 4.5V$	0.3		μs
	All Others, $V_{CC} \geq 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		μs
	$V_{CC} \geq 3.0V$	1.0		μs
Output Propagation Delay	$V_{OUT} = 1.5V$, $C_L = 100pF$, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$V_{CC} \geq 3.0V$		4.0	μs



Order Number COP311C-XXX/D,
COP411C-XXX/D
NS Package D20A

Order Number COP311C-XXX/N,
COP411C-XXX/N
See NS Package N20A



Order Number COP310C-XXX/D,
COP410C-XXX/D
See NS Package D24C

Order Number COP310C-XXX/N,
COP410C-XXX/N
NS Package Number N24A

Pin	Description	Pin	Description
L_7–L_0	8-bit bidirectional I/O port with TRI-STATE	SK	Logic-controlled clock (or general purpose output)
G_3–G_0	4-bit bidirectional I/O port (G_2–G_0 for 20-pin package)	CKI	System oscillator input
D_3–D_0	4-bit general purpose output port (D_1–D_0 for 20-pin package)	CKO	Crystal oscillator output, or HALT mode I/O port (24-pin package only)
SI	Serial input (or counter input)	$\overline{\text{RESET}}$	System reset input
SO	Serial output (or general purpose output)	V_{CC}	System power supply
		GND	System Ground

FIGURE 2. Connection Diagrams

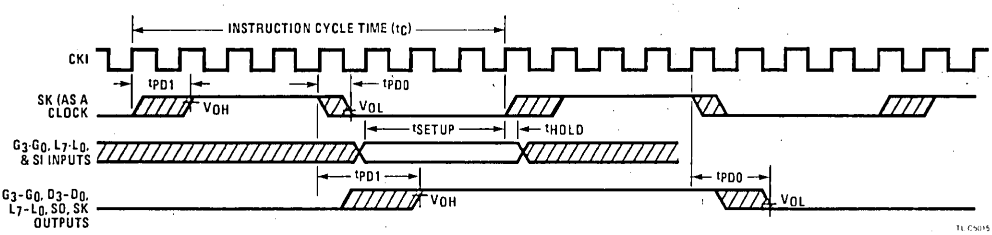


FIGURE 3. Input/Output Timing Diagrams (Divide-by-8 Mode)

Functional Description

To ease reading of this description, only COP410C and/or COP411C are referenced; however, all such references apply equally to COP310C and/or COP311C, and COP210C and/or COP211C, respectively.

A block diagram of the COP410C is given in Figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1"; when a bit is reset, it is a logic "0".

Program Memory

Program memory consists of a 512-byte ROM. As can be seen by an examination of the COP410C/411C instruction set, these words may be program instructions, program data, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, and LQID instructions, ROM must often be thought of as being organized into 8 pages of 64 words (bytes) each.

ROM Addressing

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by two 9-bit subroutine save registers, SA and SB.

ROM instruction words are fetched, decoded, and executed by the instruction decode, control and skip logic circuitry.

Data Memory

Data Memory consists of a 128-bit RAM, organized as four data registers of 8 × 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper two bits (Br) selects one of four data registers and lower three bits of the 4-bit Bd select one of eight 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), they may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3,15 instruction. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

The most significant bit of Bd is not used to select a RAM digit. Hence, each physical digit of RAM may be selected by two different values of Bd as shown in Figure 4. The skip condition for XIS and XDS instructions will be true if Bd changes between 0 and 15, but *not* between 7 and 8 (see Table 3).

Internal Logic

The internal logic of the COP410C/411C is designed to ensure fully static operation of the device.

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load four bits of the 8-bit Q latch data and to perform data exchanges with the SIO register.

The 4-bit adder performs the arithmetic and logic functions of the COP410C/411C, storing its results in A. It also outputs the carry information to a 1-bit carry register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description below.)

The G register contents are outputs to four general purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from RAM and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The eight L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and RAM.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter, depending upon the

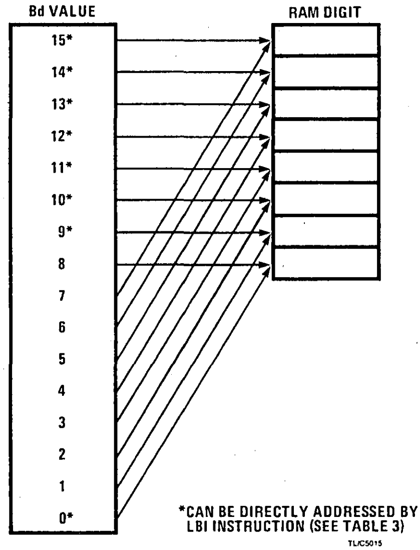


FIGURE 4. RAM Digit Address to Physical RAM Digit Mapping

contents of the EN register. (See EN register description below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. With SIO functioning as a serial-in/serial-out shift register and SK as a sync clock, the COP410C/411C is MICROWIRE™ compatible.

The D register provides four general purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK is a sync clock, inhibited when SKL is a logic "0".

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN3-EN0).

1. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or as a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN3. With EN0 reset, SIO is a serial shift register, shifting left each instruction cycle time. The data present at SI is shifted into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each instruction cycle time. (See 4. below.) The SK output becomes a logic-controlled clock.
2. EN1 is not used, it has *no* effect on the COP410C/411C.
3. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN2 disables the L drivers, placing the L I/O ports in a high impedance input state.
4. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected), SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected, disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0".

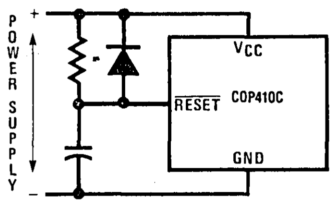
Initialization

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32kHz, otherwise the external RC network shown in Figure 5 must be connected to the $\overline{RESET}$ pin. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, providing it stays low for at least three instruction cycle times.

When V_{CC} power is applied, the internal reset logic will keep the chip in initialization mode for up to 2500 instruction cycles. If the CKI clock is running at a low frequency, this could take a long time, therefore, the internal logic should be disabled by a mask option with initialization controlled solely by $\overline{RESET}$ pin.

Note: If CKI clock is less than 32kHz, the internal reset logic (Option 25 = 1) *must* be disabled and the external RC network *must* be present.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. Data memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).



RC > 5 × POWER SUPPLY RISE TIME
AND RC > 100 × CKI PERIOD

TL/C5015

FIGURE 5. Power-Up Clear Circuit

COP411C

If the COP410C is bonded as a 20-pin package, it becomes the COP411C, illustrated in Figure 2, COP410C/COP411C Connection Diagrams. Note that the COP411C does not contain D2, D3, G3, or CKO. Use of this option, of course, precludes use of D2, D3, G3, and CKO options. All other options are available for the COP411C.

Table 1. Enable Register Modes — Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

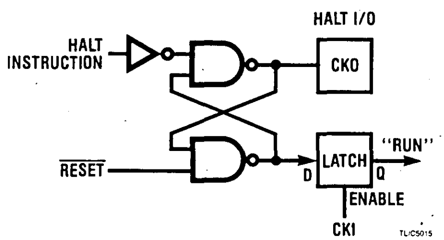
HALT Mode

The COP410C/411C is a *fully static* circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip also may be halted by the HALT instruction or by forcing CKO high when it is used as a HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal, and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The HALT mode is the minimum power dissipation state.

The HALT mode has slight differences depending upon the type of oscillator used.

a. 1-pin oscillator—RC or external
   The HALT mode may be entered into by either program control (HALT instruction) or by forcing CKO to a logic "1" state.
   The circuit may be awakened by one of two different methods:
   1) Continue function. By forcing CKO to a logic "0", the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
   2) Restart. Forcing the $\overline{\text{RESET}}$ pin to a logic "0" will restart the chip regardless of HALT or CKO (see Initialization).

b. 2-pin oscillator—crystal
   The HALT mode may be entered into by program control (HALT instruction) which forces CKO to a logic "1" state. The circuit can be awakened only by the $\overline{\text{RESET}}$ function.



Halt I/O Port

CKO Pin Options

In a crystal-controlled oscillator system, CKO is used as an output to the crystal network. CKO will be forced high during the execution of a HALT instruction, thus inhibiting the crystal network. If a 1-pin oscillator system is chosen (RC or external), CKO will be selected as HALT and is an I/O flip-flop which is an indicator of the HALT status. An external signal can override this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and the CKO output will go high to keep the chip stopped. By forcing a low level to CKO, the chip will continue and CKO output will go low.

All features associated with the CKO I/O pin are available with the 24-pin package only.

Oscillator Options

There are three options available that define the use of CKI and CKO.

a. Crystal-Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optionally by 8 or 4).

b. External Oscillator. CKI is configured as LSTTL-compatible input accepting an external clock signal. The external frequency is divided by 16 (optionally by 8 or 4) to give the instruction cycle time. CKO is the HALT I/O port.

c. RC-Controlled Oscillator. CKI is configured as a single pin RC-controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port.

The RC oscillator is not recommended in systems that require accurate timing or low current. The RC oscillator draws more current than an external oscillator (typically an additional 100μA at 5V). However, when the part halts, it stops with CKI high and the halt current is at the minimum.

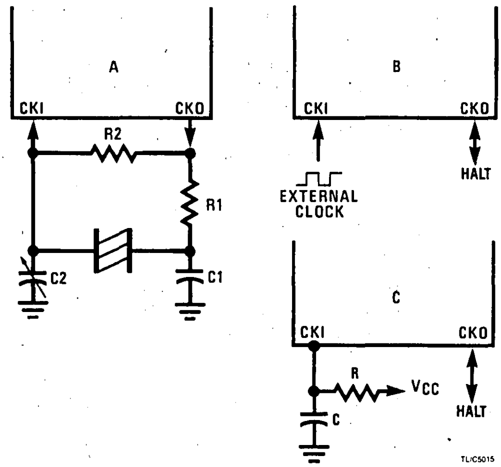


FIGURE 6. COP410C Oscillator

Crystal or Resonator					RC-Controlled Oscillator			
Crystal Value	R1	R2	C1pF	C2pF	R	C	Cycle Time	V_{CC}
32kHz	220k	20M	30	5–36	15k	82pF	4–9μs	≥4.5V
455kHz	5k	10M	80	40	30k	82pF	8–16μs	≥4.5V
2.096MHz	2k	1M	30	6–36	47k	100pF	16–32μs	2.4to4.5
4.0MHz	1k	1M	30	6–36	Note: 15k≤R≤150k, 50pF≤C≤150pF			

COP410C/COP411C Instruction Set

Table 2 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP410C/COP411C instruction set.

Table 2. COP410C/411C Instruction Set Table Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
L	8-bit TRI-STATE® I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0-15 binary (RAM Digit Select)
r	2-bit Operand Field, 0-3 binary (RAM Register Select)
a	9-bit Operand Field, 0-511 binary (ROM Address)
y	4-bit Operand Field, 0-15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
→	Replaces
←→	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

Table 3. COP410C/411C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	0011 | 0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 | 0001	A + RAM(B) → A	None	Add RAM to A
AISC	y	5-	0101 | y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CLRA		00	0000 | 0000	0 → A	None	Clear A
COMP		40	0100 | 0000	$\overline{A}$ → A	None	One's complement of A to A
NOP		44	0100 | 0100	None	None	No Operation
RC		32	0011 | 0010	"0" → C	None	Reset C
SC		22	0010 | 0010	"1" → C	None	Set C
XOR		02	0000 | 0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

Table 3. COP410C/411C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	|1 1 1 1|1 1 1 1|	ROM (PC_8,A,M) → $PC_{7:0}$	None	Jump Indirect (Note 2)
JMP	a	6-	|0 1 1 0|0 0 0|a_8|	a → PC	None	Jump
		--	| $a_{7:0}$ |			
JP	a	--	|1| $a_{6:0}$ | (pages 2,3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 1)
			or			
		--	|1 1| $a_{5:0}$ | (all other pages)	a → $PC_{5:0}$		
JSRP	a	--	|1 0| $a_{5:0}$ |	PC + 1 → SA → SB 010 → $PC_{8:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 2)
JSR	a	6-	|0 1 1 0|1 0 0|a_8|	PC + 1 → SA → SB a → PC	None	Jump to Subroutine
		--	| $a_{7:0}$ |			
RET		48	|0 1 0 0|1 0 0 0|	SB → SA → PC	None	Return from Subroutine
RETSK		49	|0 1 0 0|1 0 0 1|	SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33	|0 0 1 1|0 0 1 1|		None	Halt processor
		38	|0 0 1 1|1 0 0 0|			
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33	|0 0 1 1|0 0 1 1|	A → $Q_{7:4}$	None	Copy A, RAM to Q
		3C	|0 0 1 1|1 1 0 0|	RAM(B) → $Q_{3:0}$		
LD	r	-5	|0 0|r|0 1 0 1|	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LQID		BF	|1 0 1 1|1 1 1 1|	ROM(PC_8,A,M) → Q SA → SB	None	Load Q Indirect
RMB	0	4C	|0 1 0 0|1 1 0 0|	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	|0 1 0 0|0 1 0 1|	0 → $RAM(B)_1$		
	2	42	|0 1 0 0|0 0 1 0|	0 → $RAM(B)_2$		
	3	43	|0 1 0 0|0 0 1 1|	0 → $RAM(B)_3$		
SMB	0	4D	|0 1 0 0|1 1 0 1|	1 → $RAM(B)_0$	None	Set RAM Bit
	1	47	|0 1 0 0|0 1 1 1|	1 → $RAM(B)_1$		
	2	46	|0 1 0 0|0 1 1 0|	1 → $RAM(B)_2$		
	3	4B	|0 1 0 0|1 0 1 1|	1 → $RAM(B)_3$		
STII	y	7-	|0 1 1 1| y |	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	-6	|0 0|r|0 1 1 0|	RAM(B) ←→ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23	|0 0 1 0|0 0 1 1|	RAM(3,15) ←→ A	None	Exchange A with RAM (3,15)
		BF	|1 0 1 1|1 1 1 1|			
XDS	r	-7	|0 0|r|0 1 1 1|	RAM(B) ←→ A Bd − 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	-4	|0 0|r|0 1 0 0|	RAM(B) ←→ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

Table 3. COP410C/411C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 1110	Bd → A	None	Copy Bd to A
LBI	r,d	--	00 r (d − 1) (d = 0, 9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d
LEI	y	33	0011 0011	y → EN	None	Load EN Immediate
		6-	0110 y			
TEST INSTRUCTIONS						
SKC		20	0010 0000		C = "1"	Skip if C is True
SKE		21	0010 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33	0011 0011		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
		21	0010 0001			
SKGBZ		33	0011 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 0001	2nd byte	G_0 = 0	
	1	11	0001 0001		G_1 = 0	
	2	03	0000 0011		G_2 = 0	
	3	13	0001 0011		G_3 = 0	
SKMBZ	0	01	0000 0001		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0001 0001		$RAM(B)_1$ = 0	
	2	03	0000 0011		$RAM(B)_2$ = 0	
	3	13	0001 0011		$RAM(B)_3$ = 0	
INPUT/OUTPUT INSTRUCTIONS						
ING		33	0011 0011	G → A	None	Input G Ports to A
		2A	0010 1010			
INL		33	0011 0011	$L_{7:4}$ → RAM(B)	None	Input L Ports to RAM,A
		2E	0010 1110	$L_{3:0}$ → A		
OBD		33	0011 0011	Bd → D	None	Output Bd to D Outputs
		3E	0011 1110			
OMG		33	0011 0011	RAM(B) → G	None	Output RAM to G Ports
		3A	0011 1010			
XAS		4F	0100 1111	A ←→ SIO, C → SKL	None	Exchange A with SIO

Note 1: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 2: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP410C/COP411C programs.

XAS Instruction

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register. If SIO is selected as a shift register, an XAS instruction must be performed once every four instruction cycle times to effect a continuous data stream.

JID Instruction

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower eight bits of the ROM address register PC with the contents of ROM addressed by the 9-bit word, PC_8, A, M. PC_8 is not affected by this instruction.

Note: JID uses two instruction cycles if executed, one if skipped.

LQID Instruction

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table look-up or code conversion such as BCD to 7-segment. The LQID instruction "pushes" the stack ($PC+1 \rightarrow SA \rightarrow SB$) and replaces the least significant eight bits of the PC as follows: $A \rightarrow PC_{7:4}$, $RAM(B) \rightarrow PC_{3:0}$, leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" ($SB \rightarrow SA \rightarrow PC$), restoring the saved value of the PC to continue sequential program execution. Since LQID pushes $SA \rightarrow SB$, the previous contents of SB are lost.

Note: LQID uses two instruction cycles if executed, one if skipped.

Instruction Set Notes

a. The first word of a COP410C/COP411C program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed (except JID and LQID).

c. The ROM is organized into eight pages of 64 words each. The program counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: A JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word in page 3 or 7 will access data in the next group of four pages.

Power Dissipation

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, to minimize power consumption, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to ensure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal- or resonator-generated clock will typically draw 100µA more than a squarewave input. An RC oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the COP410C current drain.

$$Ic = Iq + (V \times 20 \times Fi) + (V \times 1280 \times Fi/Dv)$$

where Ic = chip current drain in microamps
Iq = quiescent leakage current (from curve)
Fi = CKI frequency in megahertz
V = chip V_{CC} in volts
Dv = divide by option selected

For example, at 5V V_{CC} and 400kHz (divide by 4),

$$Ic = 10 + (5 \times 20 \times 0.4) + (5 \times 1280 \times 0.4/4)$$
$$Ic = 10 + 40 + 640 = 690\mu A$$

I/O Options

COP410C/COP411C outputs have the following optional configurations, illustrated in Figure 7:

a. Standard. A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current. This is the same configuration as (a) above except that the sourcing current is much less.

c. Open Drain. An N-channel device to ground only, allowing external pull-up as required by the user's application.

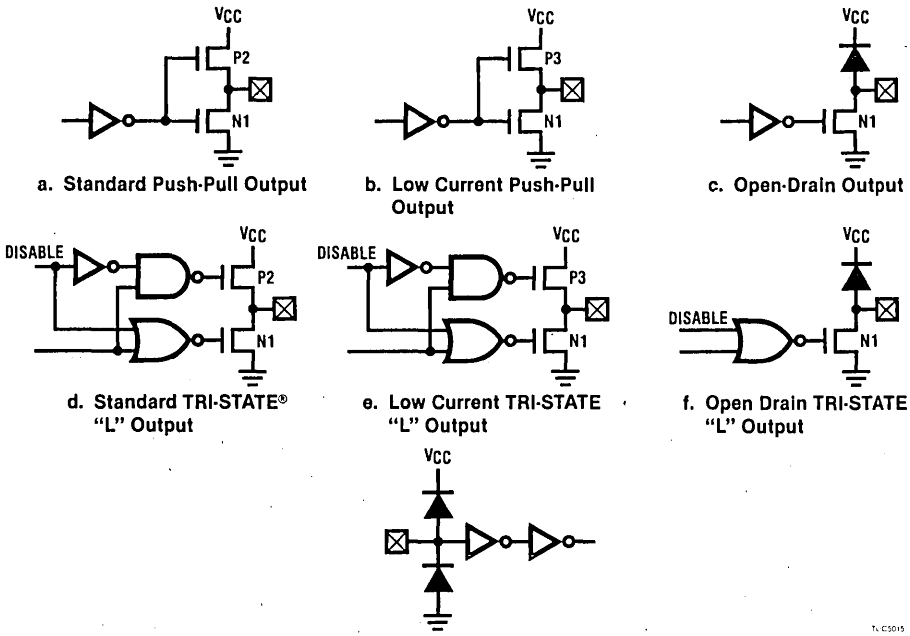
d. Standard TRI-STATE L Output. A CMOS output buffer similar to (a) which may be disabled by program control.

e. Low-Current TRI-STATE L Output. This is the same as (d) above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output. This has the N-channel device to ground only.

The SI and $\overline{RESET}$ inputs are Hi-Z inputs (*Figure 7g*).

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available: Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion, the Q registers must be set to a logic "1" level and the L drivers *must be enabled* by an LEI instruction.



a. Standard Push-Pull Output
b. Low Current Push-Pull Output
c. Open-Drain Output
d. Standard TRI-STATE® "L" Output
e. Low Current TRI-STATE "L" Output
f. Open Drain TRI-STATE "L" Output
g. Hi-Z Input

FIGURE 7. I/O Configurations

All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in Figure 8 for each of these devices to allow the desiger to effectively use these I/O configurations.

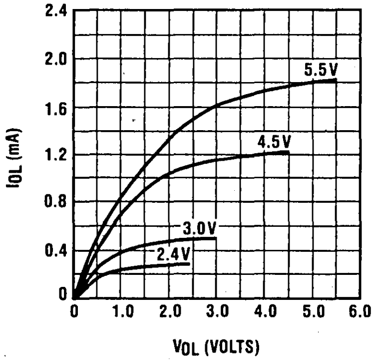
Option List

The COP410C/COP411C mask-programmable options are assigned numbers which correspond with the COP410C pins.

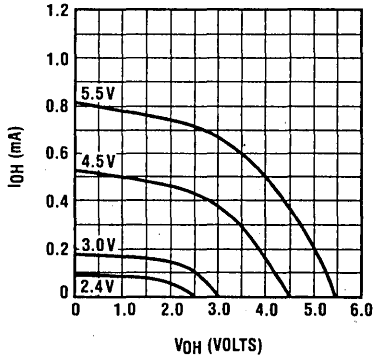
The following is a list of COP410C options. When specifying a COP411 chip, options 20, 21, and 22 must be set to 0. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1: 0 = Ground Pin. No options available.
Option 2: CKO I/O Port. Determined by Option 3.
Option 3: CKI Input.
= 0: Crystal-controlled oscillator input (÷4).
= 1: Single-pin RC-controlled oscillator (÷4).
= 2: External oscillator input (÷4).
= 3: Crystal oscillator input (÷8).
= 4: External oscillator input (÷8).
= 5: Crystal oscillator input (÷16).
= 6: External oscillator input (÷16).
Option 4: $\overline{\text{RESET}}$ Input = 1: Hi-Z input. No option available.
Option 5: L_7 Driver
= 0: Standard TRI-STATE push-pull output.
= 1: Low-current TRI-STATE push-pull output.
= 2: Open-drain TRI-STATE output.
Option 6: L_6 Driver. (Same as Option 5.)
Option 7: L_5 Driver. (Same as Option 5.)
Option 8: L_4 Driver. (Same as Option 5.)
Option 9: V_{CC} Pin.
Option 10: L_3 Driver. (Same as Option 5.)
Option 11: L_2 Driver. (Same as Option 5.)
Option 12: L_1 Driver. (Same as Option 5.)
Option 13: L_0 Driver. (Same as Option 5.)
Option 14: SI Input.
No option available.
= 1: Hi-Z input.
Option 15: SO Output.
= 0: Standard push-pull output.
= 1: Low-current push-pull output.
= 2: Open-drain output.
Option 16: SK Driver. (Same as Option 15.)
Option 17: G_0 I/O Port. (Same as Option 15.)
Option 18: G_1 I/O Port. (Same as Option 15.)
Option 19: G_2 I/O Port. (Same as Option 15.)
Option 20: G_3 I/O Port. (Same as Option 15.)
Option 21: D_3 Output. (Same as Option 15.)
Option 22: D_2 Output. (Same as Option 15.)
Option 23: D_1 Output. (Same as Option 15.)
Option 24: D_0 Output. (Same as Option 15.)
Option 25: Internal Initialization Logic.
= 0: Normal operation.
= 1: No internal initialization logic.
Option 26: No option available.
Option 27: COP Bonding.
= 0: COP410C (24-pin device).
= 1: COP411C (20-pin device).
= 2: COP410C and COP411C.

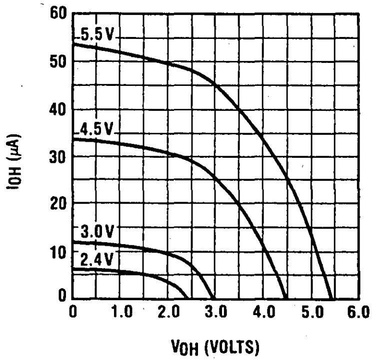
Minimum Sink Current



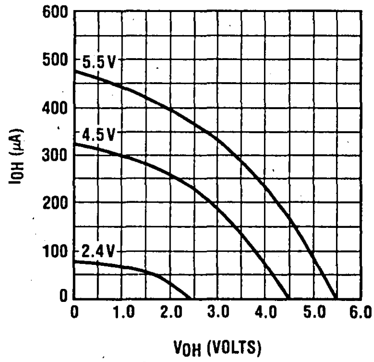
Standard
Minimum Source Current



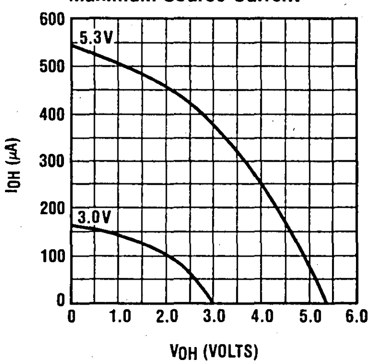
Low Current Option
Minimum Source Current



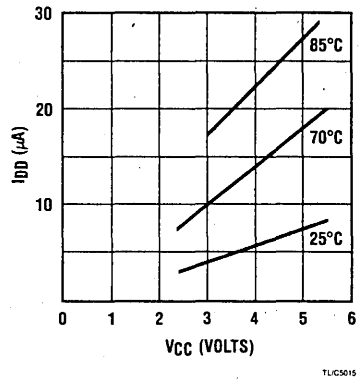
COP410C/COP411C
Low Current Option
Maximum Source Current



COP310C/COP311C
Low Current Option
Maximum Source Current



Maximum Quiescent Current



National Semiconductor

PRELIMINARY

microCMOS

COP424C, COP425C, COP426C, COP324C, COP325C, COP326C and COP444C, COP445C, COP344C, COP345C Single Chip 1k and 2k CMOS Microcontrollers

General Description

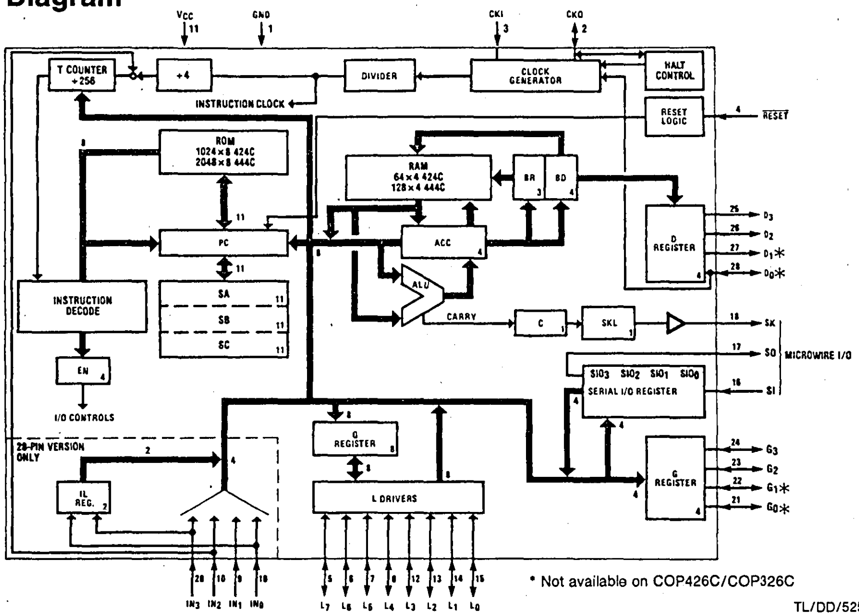
The COP424C, COP425C, COP426C, COP444C and COP445C fully static, Single-Chip CMOS Microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon gate CMOS (microCMOS) technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP424C and COP444C are 28 pin chips. The COP425C and COP445C are 24-pin versions (4 inputs removed) and COP426C is 20-pin version with 15 I/O lines. Standard test procedures and reliable high-density techniques provide the medium to large volume customers with a customized microcontroller at a low end-product cost. These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

The COP424C is an improved product which replaces the COP420C.

Features

- Lowest Power Dissipation (50 μW typical)
- Fully static (can turn off the clock)
- Power saving IDLE state and HALT mode
- 4 μs instruction time, plus software selectable clocks
- 2k × 8 ROM, 128 × 4 RAM (COP444C/COP445C)
- 1k × 8 ROM, 64 × 4 RAM (COP424C/COP425C/COP426C)
- 23 I/O lines (COP444C and COP424C)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Single supply operation (2.4V to 5.5V)
- Programmable read/write 8-bit timer/event counter
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible
- MICROBUS™ compatible
- Software/hardware compatible with COP400 family
- Extended temperature range devices COP324C/COP325C/COP326C and COP344C/COP345C (−40°C to +85°C)
- Military devices (−55°C to +125°C) to be available

Block Diagram



* Not available on COP426C/COP326C

TL/DD/5259-1

FIGURE 1.

COP424C/COP425C/COP426C and COP444C/COP445C

Absolute Maximum Ratings

Supply Voltage (V_{CC})	6V
Voltage at any pin	$-0.3V$ to $V_{CC} + 0.3V$
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics $0°C \leq T_A \leq 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		2.4	5.5	V
Power Supply Ripple (Note 5)	Peak to Peak		$0.1\ V_{CC}$	V
Supply Current (Note 1)	$V_{CC}=2.4V$, $tc=64\ \mu s$		120	μA
	$V_{CC}=5.0V$, $tc=16\ \mu s$		700	μA
	$V_{CC}=5.0V$, $tc=4\ \mu s$ (tc is instruction cycle time)		3000	μA
HALT Mode Current (Note 2)	$V_{CC}=5.0V$, $F_{IN}=0$ kHz		40	μA
	$V_{CC}=2.4V$, $F_{IN}=0$ kHz		12	μA
Input Voltage Levels				
$\overline{RESET}$, CKI, Do (clock input)				
Logic High		$0.9\ V_{CC}$		V
Logic Low			$0.1\ V_{CC}$	V
All other inputs				
Logic High		$0.7\ V_{CC}$		V
Logic Low			$0.2\ V_{CC}$	V
Input Pull-up current	$V_{CC}=4.5V$, $V_{IN}=0$	30	330	μA
Hi-Z input leakage		−1	+1	μA
Input capacitance (Note 4)			7	pF
Output Voltage Levels	Standard outputs			
LSTTL Operation	$V_{CC}=5.0V \pm 5\%$			
Logic High	$I_{OH}=-100\ \mu A$	2.7		V
Logic Low	$I_{OL}=400\ \mu A$		0.4	V
CMOS Operation				
Logic High	$I_{OH}=-10\ \mu A$	$V_{CC}-0.2$		V
Logic Low	$I_{OL}=10\ \mu A$		0.2	V
Output current levels (except CKO)				
Sink (Note 6)	$V_{CC}=4.5V$, $V_{OUT}=V_{CC}$	1.2		mA
	$V_{CC}=2.4V$, $V_{OUT}=V_{CC}$	0.2		mA
Source (Standard Option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	0.5		mA
	$V_{CC}=2.4V$, $V_{OUT}=0V$	0.1		mA
Source (Low Current Option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	30	330	μA
	$V_{CC}=2.4V$, $V_{OUT}=0V$	6	80	μA
CKO Current Levels (As Clock Out)				
Sink ÷4	$V_{CC}=4.5V$, $CKI=V_{CC}$, $V_{OUT}=V_{CC}$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	$V_{CC}=4.5V$, $CKI=0V$, $V_{OUT}=0V$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Allowable Sink/Source current per pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current needed to over-ride HALT (Note 3)				
To continue	$V_{CC}=4.5V$, $V_{IN}=.2V_{CC}$		.7	mA
To halt	$V_{CC}=4.5V$, $V_{IN}=.7V_{CC}$		1.6	mA
TRI-STATE or open drain leakage current		−2.5	+2.5	μA

COP424C/COP425C/COP426C and COP444C/COP445C

AC Electrical Characteristics $0°C \leq T_A \leq 70°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (tc)	$V_{CC} \geq 4.5V$	4	DC	μs
	$4.5V > V_{CC} \geq 2.4V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \geq 4.5V$	DC	1.0	MHz
÷8 mode		DC	2.0	MHz
÷16 mode		DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \geq 2.4V$	DC	250	kHz
÷8 mode		DC	500	kHz
÷16 mode		DC	1.0	MHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz external clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz external clock		40	ns
Instruction Cycle Time. RC Oscillator (Note 4)	$R = 30k$, $V_{CC} = 5V$, $C = 82$ pF (÷4 Mode)	8	16	μs
Inputs: (See *Figure 3*)				
t_{SETUP}	G Inputs, $V_{CC} \geq 4.5V$	tc/4+.7		μs
	SI Input, $V_{CC} \geq 4.5V$	0.3		μs
	All Others, $V_{CC} \geq 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \geq 4.5V$	0.25		μs
	$4.5V > V_{CC} \geq 2.4V$	1.0		μs
Output propagation delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \geq 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \geq 2.4V$		4.0	μs
MICROBUS™ timing	$CL = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Read Operation (*Figure 4*)				
Chip select stable before $\overline{RD}$ $-t_{CSR}$		65		ns
Chip select hold time for $\overline{RD}$ $-t_{RCS}$		20		ns
$\overline{RD}$ pulse width $-t_{RR}$		400		ns
Data delay from $\overline{RD}$ $-t_{RD}$			375	ns
$\overline{RD}$ to data floating $-t_{DF}$ (Note 4)			250	ns
Write Operation (*Figure 5*)				
Chip select stable before $\overline{WR}$ $-t_{CSW}$		65		ns
Chip select hold time for $\overline{WR}$ $-t_{WCS}$		20		ns
$\overline{WR}$ pulse width $-t_{WW}$		400		ns
Data set-up time for $\overline{WR}$ $-t_{DW}$		320		ns
Data hold time for $\overline{WR}$ $-t_{WD}$		100		ns
INTR transition time from $\overline{WR}$ $-t_{WI}$			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 17.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4: This parameter is only sampled and not 100% tested.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than $0.2V_{CC}$ when part is running in order to prevent entering test mode.

COP324C/COP325C/COP326C and COP344C/COP345C

Absolute Maximum Ratings

Supply Voltage	6V
Voltage at any pin	$-0.3V$ to V_{CC} + 0.3V
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Operating temperature range	−40°C to +85°C
Storage temperature range	−65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		3.0	5.3	V
Power Supply Ripple (Note 5)	Peak to Peak		$0.1V_{CC}$	V
Supply Current (Note 1)	$V_{CC}=3.0V$, tc=64 μs		180	μA
	$V_{CC}=5.0V$, tc=16 μs		800	μA
	$V_{CC}=5.0V$, tc=4 μs		3600	μA
	(tc is instruction cycle time)			
HALT Mode Current (Note 2)	$V_{CC}=5.0V$, $F_{IN}=0$ kHz		60	μA
	$V_{CC}=3.0V$, $F_{IN}=0$ kHz		30	μA
Input Voltage Levels				
RESET, CKI, D_O (clock input)				
Logic High		0.9 V_{CC}		V
Logic Low			0.1 V_{CC}	V
All other inputs				
Logic High		0.7 V_{CC}		V
Logic Low			0.2 V_{CC}	V
Input Pull-up current	$V_{CC}=4.5V$, $V_{IN}=0$	30	440	μA
Hi-Z input leakage		−2	+2	μA
Input capacitance (Note 4)			7	pF
Output Voltage Levels	Standard outputs			
LSTTL Operation	$V_{CC}=5.0V \pm 5\%$			
Logic High	$I_{OH}=-100$ μA	2.7		V
Logic Low	$I_{OL}=400$ μA		0.4	V
CMOS Operation				
Logic High	$I_{OH}=-10$ μA	$V_{CC}-0.2$		V
Logic Low	$I_{OL}=10$ μA		0.2	V
Output current levels (except CKO)				
Sink (Note 6)	$V_{CC}=4.5V$, $V_{OUT}=V_{CC}$	1.2		mA
	$V_{CC}=3.0V$, $V_{OUT}=V_{CC}$	0.2		mA
Source (Standard Option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	0.5		mA
	$V_{CC}=3.0V$, $V_{OUT}=0V$	0.1		mA
Source (Low Current Option)	$V_{CC}=4.5V$, $V_{OUT}=0V$	30	440	μA
	$V_{CC}=3.0V$, $V_{OUT}=0V$	8	200	μA
CKO Current Levels (As Clock Out)				
Sink ÷4	$V_{CC}=4.5V$, $CKI=V_{CC}$, $V_{OUT}=V_{CC}$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Source ÷4	$V_{CC}=4.5V$, CKI=0V, $V_{OUT}=0V$	0.3		mA
÷8		0.6		mA
÷16		1.2		mA
Allowable Sink/Source current per pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			100	pF
Current needed to over-ride HALT (Note 3)				
To continue	$V_{CC}=4.5V$, $V_{IN}=0.2V_{CC}$		0.9	mA
To halt	$V_{CC}=4.5V$, $V_{IN}=0.7V_{CC}$		2.1	mA
TRI-STATE or open drain leakage current		−5	+5	μA

COP324C/COP325C/COP326C and COP344C/COP345C

AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless other specified

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (tc)	$V_{CC} \ge 4.5V$	4	DC	μs
	$4.5V > V_{CC} \ge 3.0V$	16	DC	μs
Operating CKI Frequency ÷4 mode	$V_{CC} \ge 4.5V$	DC	1.0	MHz
÷8 mode		DC	2.0	MHz
÷16 mode		DC	4.0	MHz
÷4 mode	$4.5V > V_{CC} \ge 3.0V$	DC	250	kHz
÷8 mode		DC	500	kHz
÷16 mode		DC	1.0	MHz
Duty Cycle (Note 4)	$f_1 = 4$ MHz	40	60	%
Rise Time (Note 4)	$f_1 = 4$ MHz external clock		60	ns
Fall Time (Note 4)	$f_1 = 4$ MHz external clock		40	ns
Instruction Cycle Time. RC Oscillator (Note 4)	R = 30k, V_{CC} = 5V C = 82 pF (÷4 Mode)	8	16	μs
Inputs: (See *Figure 3*)				
t_{SETUP}	G Inputs, $V_{CC} \ge 4.5V$	tc/4+.7		μs
	SI Inputs, $V_{CC} \ge 4.5V$	0.3		μs
	All Others, $V_{CC} \ge 4.5V$	1.7		μs
t_{HOLD}	$V_{CC} \ge 4.5V$	0.25		μs
	$4.5V > V_{CC} \ge 3.0V$	1.0		μs
Output propagation delay	$V_{OUT} = 1.5V$, $C_L = 100$ pF, $R_L = 5k$			
t_{PD1}, t_{PD0}	$V_{CC} \ge 4.5V$		1.0	μs
t_{PD1}, t_{PD0}	$4.5V > V_{CC} \ge 3.0V$		4.0	μs
MICROBUS™ timing	$C_L = 50$ pF, $V_{CC} = 5V \pm 5\%$			
Read Operation (*Figure 4*)				
Chip select stable before $\overline{RD}$ $-t_{CSR}$		65		ns
Chip select hold time for $\overline{RD}$ $-t_{RCS}$		20		ns
$\overline{RD}$ pulse width $-t_{RR}$		400		ns
Data delay from $\overline{RD}$ $-t_{RD}$			375	ns
$\overline{RD}$ to data floating $-t_{DF}$ (Note 4)			250	ns
Write Operation (*Figure 5*)				
Chip select stable before $\overline{WR}$ $-t_{CSW}$		65		ns
Chip select hold time for $\overline{WR}$ $-t_{WCS}$		20		ns
$\overline{WR}$ pulse width $-t_{WW}$		400		ns
Data set-up time for $\overline{WR}$ $-t_{DW}$		320		ns
Data hold time for $\overline{WR}$ $-t_{WD}$		100		ns
INTR transition time from $\overline{WR}$ $-t_{WI}$			700	ns

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 20k resistors. See current drain equation on page 17.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC}, L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

Note 4: This parameter is only sampled and not 100% tested.

Note 5: Voltage change must be less than 0.5 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than $0.2V_{CC}$ when part is running in order to prevent entering test mode.

Functional Description

The internal architecture is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1", when a bit is reset, it is a logic "0".

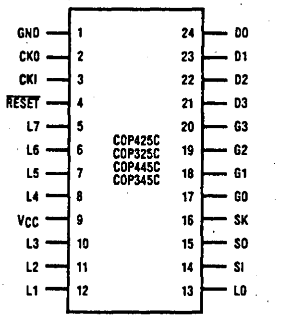
For ease of reading only the COP424C/425C/COP426C/444C/445C are referenced; however, all such references apply equally to COP324C/325C/COP326C/344C/345C.

PROGRAM MEMORY

Program Memory consists of ROM, 1024 bytes for the COP424C/425C/COP426C and 2048 bytes for the COP444C/445C. These bytes of ROM may be program instructions, constants or ROM addressing data.

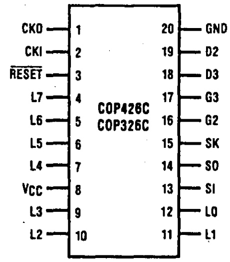
ROM addressing is accomplished by a 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Connection Diagrams



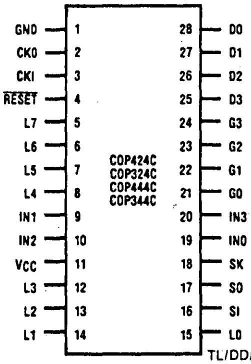
TL/DD/5259-2

Order Number COP425C-XXX/D, COP325C-XXX/D, COP445C-XXX/D, COP345C-XXX/D
See NS Package D24C
Order Number COP425C-XXX/N, COP325C-XXX/N, COP445C-XXX/N, COP345C-XXX/N
See NS Package N24A



TL/DD/5259-3

Order Number COP326C-XXX/D, COP426C-XXX/D
See NS Package D20A
Order Number COP426C-XXX/N, COP326C-XXX/N
See NS Package N20A



TL/DD/5259-16

Order Number COP424C-XXX/D, COP324C-XXX/D, COP444C-XXX/D, COP344C-XXX/D
See NS Package D28C
Order Number COP424C-XXX/N, COP324C-XXX/N, COP444C-XXX/N, COP344C-XXX/N
See NS Package N28B

FIGURE 2.

Pin	Description	Pin	Description
L7-L0	8-bit bidirectional port with TRI-STATE	CKI	Chip oscillator input
G3-G0	4-bit bidirectional I/O port	CKO	Oscillator output, HALT I/O port or general purpose input
D3-D0	4-bit output port	RESET	Reset input
IN3-IN0	4-bit input port (28 pin package only)	V_{CC}	Most positive power supply
SI	Serial input or counter input	GND	Ground
SO	Serial or general purpose output		
SK	Logic controlled clock output		

Functional Description (Continued)

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM for the COP444C/445C, organized as 8 data registers of 16 × 4-bit digits. RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register.

Data memory consists of a 256-bit RAM for the COP424C/425C/426C, organized as 4 data registers of 16 × 4-bits digits. The B register is 6 bits long. Upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or T counter or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch or T counter, to input 4 bits of L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be operated in two modes depending on a mask-programmable option: as a timer or as an external event counter. When the T counter overflows, an overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in *Figure 10a*.

Four general-purpose inputs, IN3-IN0, are provided. IN1, IN2 and IN3 may be selected, by a mask-programmable option as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS application.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. In the dual clock mode, D0 latch controls the clock selection (see dual oscillator below).

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G0 may be mask-programmed as an output for MICROBUS applications.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports

Functional Description (Continued)

when the L drivers are enabled under program control. With the MICROBUS option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurence of a write strobe from the host CPU.

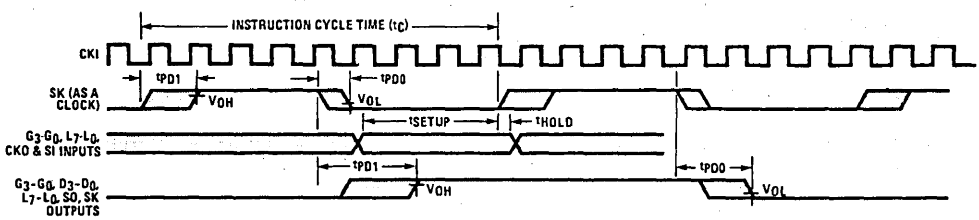
The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O port. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS option allows L I/O port data to be latched into the Q register.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the ouput of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

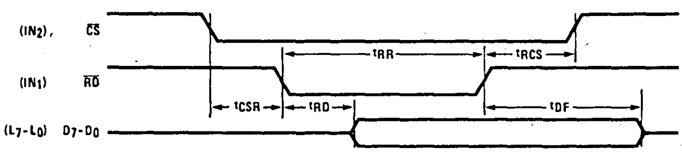
EN is an internal 4-bit register loaded by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register:

0. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output equals the value of EN3. With EN0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK outputs SKL ANDed with the instruction cycle clock.
1. With EN1 set, interrupt is enabled. Immediately following an interrupt, EN1 is reset to disable further interrupts.
2. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting EN2 disables the L drivers, placing the L I/O port in a high-impedance input state.
3. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected) SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected disables SO as the output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to "0".



TL/DD/5259-4

FIGURE 3. Input/Output Timing Diagrams (divide by 8 mode)



TL/DD/5259-5

FIGURE 4. MICROBUS Read Operation Timing

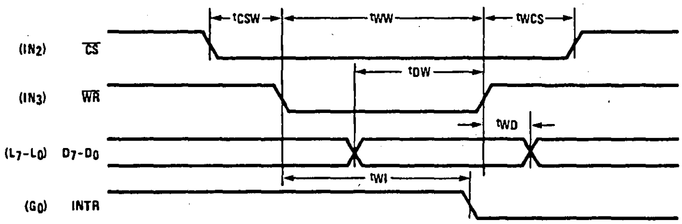


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FIGURE 5. MICROBUS Write Operation Timing

Functional Description (Continued)

TABLE 1. Enable Register Modes — Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL=1,SK=clock If SKL=0,SK=0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL=1,SK=clock If SKL=0,SK=0
1	0	Binary Counter	Input to Counter	0	SK=SKL
1	1	Binary Counter	Input to Counter	1	SK=SKL

INTERRUPT

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

a. The interrupt, once recognized as explained below, pushes the next sequential program counter address (PC+1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN1 is reset.

b. An interrupt will be recognized only on the following conditions:
   1. EN1 has been set.
   2. A low-going pulse ("1" to "0") at least two instruction cycles wide has occurred on the IN_1 input.
   3. A currently executing instruction has been completed.
   4. All successive transfer of control instructions and successive LBIs have been completed (e.g. if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to pop the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt service routine, since their popping of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

d. The instruction at hex address 0FF must be a NOP.

e. An LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

MICROBUS INTERFACE

The COP444C/424C has an option which allows it to be used as a peripheral microprocessor device, inputting and outputting data from and to a host microprocessor (uP). IN1, IN2 and IN3 general purpose inputs become MICROBUS compatible read-strobe, chip-select, and write-strobe lines, respectively. IN1 becomes $\overline{RD}$ — a logic "0" on this input will cause Q latch data to be enabled to the L ports for input to the uP. IN2 becomes $\overline{CS}$ — a logic "0" on this line selects the COP444C/424C as the uP peripheral device by enabling the operation of the $\overline{RD}$ and $\overline{WR}$ lines and allows for the selection of one of several peripheral components. IN3 becomes $\overline{WR}$ — a logic "0" on this line will write bus data from the L ports to the Q latches for input to the COP444C/424C. G0 becomes INTR a "ready" output, reset by a write pulse from the uP on the $\overline{WR}$ line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the COP444C/424C.

This option has been designed for compatibility with National's MICROBUS — a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication). The functioning and timing relationships between the signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams (*Figures 4* and *5*). Connection of the COP444C/424C to the MICROBUS is shown in *Figure 6*.

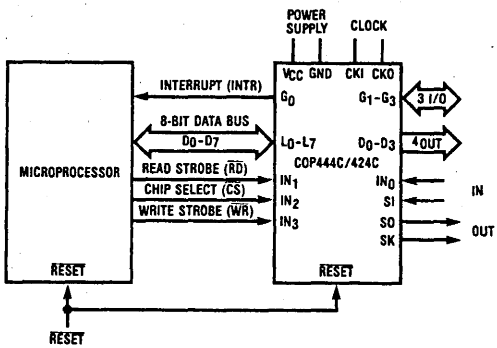

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FIGURE 6. MICROBUS Option Interconnect

INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in *Figure 7* must be connected to the $\overline{RESET}$ pin (the conditions in *Figure 7* must be met). The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used, it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, providing it stays low for at least three instruction cycle times.

NOTE: If CKI clock is less than 32 kHz, the internal reset logic (option #29=1) MUST be disabled and the external RC circuit must be used.

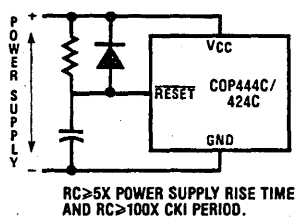

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FIGURE 7. Power-Up Circuit

Functional Description (Continued)

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL latch is set, thus enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

TIMER

There are two modes selected by mask option:

a. Time-base counter. In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The prescaler is cleared during execution of a CAMT instruction and on reset.

   For example, using a 4 MHz crystal with a divide-by-16 option, the instruction cycle frequency of 250 kHz increments the 10-bit timer every 4 μs. By presetting the counter and detecting overflow, accurate timeouts between 16 μs (4 counts) and 4.096 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

b. External event counter. In this mode, a low-going pulse ("1" to "0") at least 2 instruction cycles wide on the IN2 input will increment the 8-bit T counter.

   NOTE: The IT instruction is not allowed in this mode.

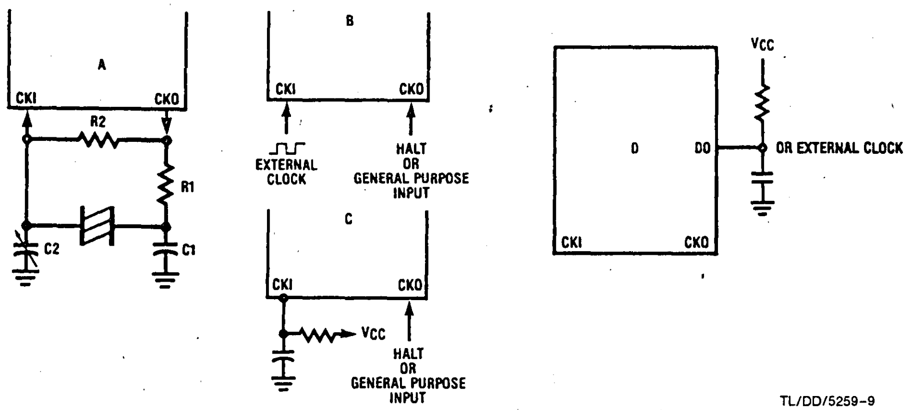
HALT MODE

The COP444C/445C/424C/425C/426C is a FULLY STATIC circuit; therefore, the user may stop the system oscillator at any time to halt the chip. The chip may also be halted by the HALT instruction or by forcing CKO high when it is mask-programmed as an HALT I/O port. Once in the HALT mode, the internal circuitry does not receive any clock signal and is therefore frozen in the exact state it was in when halted. All information is retained until continuing. The chip may be awakened by one of two different methods:

- Continue function: by forcing CKO low, if it mask-programmed as an HALT I/O port, the system clock is re-enabled and the circuit continues to operate from the point where it was stopped.
- Restart: by forcing the $\overline{\text{RESET}}$ pin low (see Initialization).

The HALT mode is the minimum power dissipation state.

NOTE: If the user has selected dual-clock with D0 as external oscillator (option 30=2) AND the COP444C/424C is running with the D0 clock, the HALT mode — either hardware or software — will NOT be entered. Thus, the user should switch to the CKI clock to HALT. Alternatively, the user may stop the D0 clock to minimize power.



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Crystal or resonator

Crystal value	R1	R2	C1 (pF)	C2 (pF)
32 kHz	220k	20M	30	6–36
455 kHz	5k	10M	80	40
2.096 MHz	2k	1M	30	6–36
4.0 MHz	1k	1M	30	6–36

(Component Values: R1, R2, C1, C2)

RC controlled Oscillator

R	C	Cycle time	V_{CC}
15k	82 pF	4–9 μs	≥4.5V
30k	82 pF	8–16 μs	≥4.5V
60k	100 pF	16–32 μs	2.4–4.5V

Note: 15k≤R≤150k
50 pF≤C≤150 pF

FIGURE 8. Oscillator Component values

Functional Description (Continued)

CKO Pin Options

a. Two-pin oscillator — (Crystal). See *Figure 9A*.

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. The HALT mode may be entered by program control (HALT instruction) which forces CKO high, thus inhibiting the crystal network. The circuit can be awakened only by forcing the $\overline{\text{RESET}}$ pin to a logic "0" (restart).

b. One-pin oscillator — (RC or external). See *Figure 9B*.

If a one-pin oscillator system is chosen, two options are available for CKO:

- CKO can be selected as the HALT I/O port. In that case, it is an I/O flip-flop which is an indicator of the HALT status. An external signal can over-ride this pin to start and stop the chip. By forcing a high level to CKO, the chip will stop as soon as CKI is high and CKO output will stay high to keep the chip stopped if the external driver returns to high impedance state.

  By forcing a low level to CKO, the chip will continue and CKO will stay low.
- As another option, CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

OSCILLATOR OPTIONS

There are four basic clock oscillator configurations available as shown by *Figure 8*.

a. Crystal Controlled Oscillator. CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency optionally divided by 4, 8 or 16.

b. External Oscillator. The external frequency is optionally divided by 4, 8 or 16 to give the instruction cycle time. CKO is the HALT I/O port or a general purpose input.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is the HALT I/O port or a general purpose input.

d. Dual oscillator. By selecting the dual clock option, pin D0 is now a single pin oscillator input. Two configurations are available: RC controlled Schmitt trigger oscillator or external oscillator.

The user may software select between the D0 oscillator (in that case, the instruction cycle time equals the D0 oscillation frequency divided by 4) by setting the D0 latch high or the CKI (CKO) oscillator by resetting D0 latch low. Note that even in dual clock mode, the counter, if mask-programmed as a time-base counter, is always connected to the CKI oscillator.

For example, the user may connect up to a 1 MHz RC circuit to D0 for faster processing and a 32 kHz watch crystal to CKI and CKO for minimum current drain and time keeping.

NOTE: CTMA instruction is not allowed when chip is running from D0 clock.

Figures 10A and *10B* show the clock and timer diagrams with and without Dual clock.

COP445C AND COP425C 24-PIN PACKAGE OPTION

If the COP444C/424C is bonded in a 24-pin package, it becomes the COP445C/425C, illustrated in *Figure 2*, Connection diagrams. Note that the COP445C/425C does not contain the four general purpose IN inputs (IN3–IN0). Use of this option precludes, of course, use of the IN options, interrupt feature, external event counter feature, and the MICROBUS option which uses IN1–IN3. All other options are available for the COP445C/425C.

NOTE: If user selects the 24-pin package, options 9, 10, 19 and 20 must be selected as a "0" (load to V_{CC} on the IN inputs). See option list.

COP426C 20-PIN PACKAGE OPTION

If the COP425C is bonded as 20-pin device it becomes the COP426C. Note that the COP426C contains all the COP425C pins except D_0, D_1, G_0, and G_1.

Block Diagrams

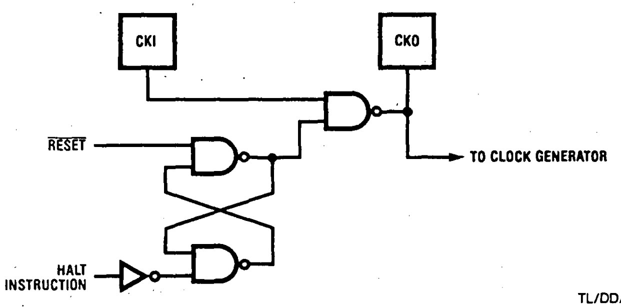

FIGURE 9A: Halt Mode — Two-Pin Oscillator

Block Diagrams (Continued)

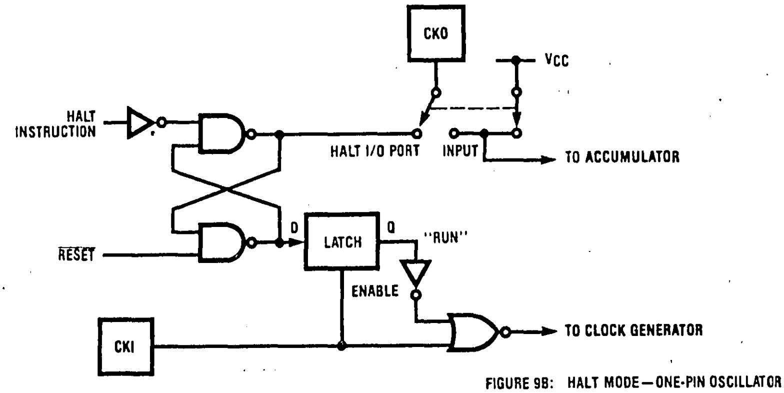

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FIGURE 9B: Halt Mode — One-Pin Oscillator

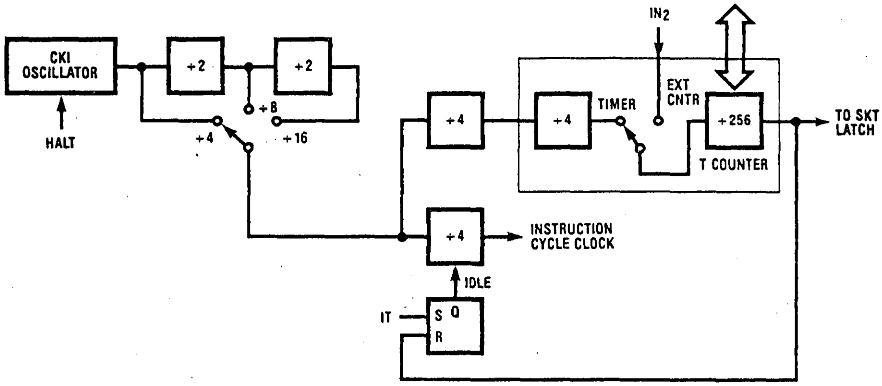

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FIGURE 10A: Clock and Timer without Dual-Clock

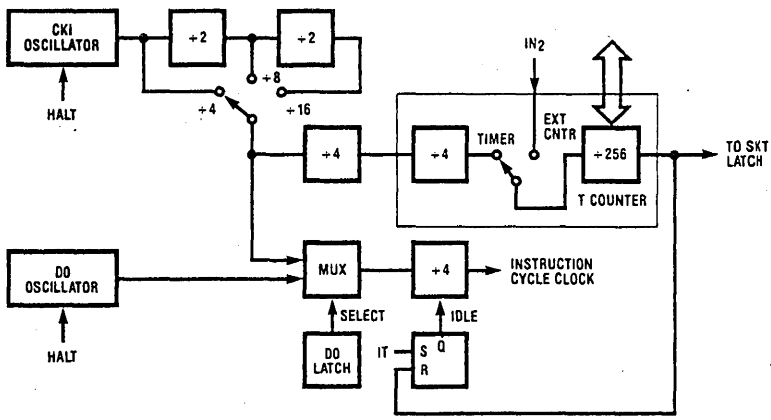

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FIGURE 10B: Clock and Timer with Dual-Clock

Instruction Set

Table 2 is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

TABLE 2. Instruction Set Table Symbols

Symbol	Definition
Internal Architecture Symbols	
A	4-bit Accumulator
B	7-bit RAM address register (6-bit for COP424C)
Br	Upper 3 bits of B (register address) (2-bit for COP424C)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry register
D	4-bit Data output port
EN	4-bit Enable register
G	4-bit General purpose I/O port
IL	two 1-bit (IN0 and IN3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/O port
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA,SB,SC	11-bit 3-level subroutine stack
SIO	4-bit Shift register and counter
SK	Logic-controlled clock output
SKL	1-bit latch for SK output
T	8-bit timer
Instruction operand symbols	
d	4-bit operand field, 0–15 binary (RAM digit select)
r	3(2)-bit operand field, 0–7(3) binary (RAM register select)
a	11-bit operand field, 0–2047 (1023)
y	4-bit operand field, 0–15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x
Operational Symbols	
+	Plus
–	Minus
→	Replaces
↔	is exchanged with
=	Is equal to
$\overline{A}$	one's complement of A
⊕	exclusive-or
:	range of values

TABLE 3. COP444C/445C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	|0011|0000|	A+C+RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	|0011|0001|	A+RAM(B) → A	None	Add RAM to A
ADT		4A	|0100|1010|	A+10_{10} → A	None	Add Ten to A
AISC	y	5–	|0101| y |	A+y → A	Carry	Add Immediate. Skip on Carry (y ≠ 0)
CASC		10	|0001|0000|	$\overline{A}$+RAM(B)+C → A Carry → C	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	|0000|0000|	0 → A	None	Clear A
COMP		40	|0100|0000|	$\overline{A}$ → A	None	Ones complement of A to A
NOP		44	|0100|0100|	None	None	No Operation
RC		32	|0011|0010|	"0" → C	None	Reset C
SC		22	|0010|0010|	"1" → C	None	Set C
XOR		02	|0000|0010|	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	|1111|1111|	ROM ($PC_{10:8}$ A,M) → $PC_{7:0}$	None	Jump Indirect (Notes 1, 3)
JMP	a	6– – –	|0110|0|$a_{10:8}$| |$a_{7:0}$|	a → PC	None	Jump
JP	a	– –	|1| $a_{6:0}$| (pages 2,3 only)	a → $PC_{6:0}$	None	Jump within Page (Note 4)
			or			
		– –	|11|$a_{5:0}$| (all other pages)	a → $PC_{5:0}$		
JSRP	a	– –	|10|$a_{5:0}$|	PC+1 → SA → SB → SC 00010 → $PC_{10:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6– – –	|0110|1|$a_{10:8}$| |$a_{7:0}$|	PC+1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	|0100|1000|	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	|0100|1001|	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33 38	|0011|0011| |0011|1000|		None	HALT processor
IT		33 39	|0011|0011| |0011|1001|		None	IDLE till timer overflows then continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33 3F	|0011|0011| |0011|1111|	A → $T_{7:4}$ RAM(B) → $T_{3:0}$	None	Copy A, RAM to T
CTMA		33 2F	|0011|0011| |0010|1111|	$T_{7:4}$ → RAM(B) $T_{3:0}$ → A	None	Copy T to RAM, A (Note 9)
CAMQ		33 3C	|0011|0011| |0011|1100|	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
CQMA		33 2C	|0011|0011| |0010|1100|	$Q_{7:4}$ → RAM(B) $Q_{3:0}$ → A	None	Copy Q to RAM, A
LD	r	–5	|00|r|0101| (r=0:3)	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 – –	|0010|0011| |0|r|d|	RAM(r,d) → A	None	Load A with RAM pointed to directly by r,d
LQID		BF	|1011|1111|	ROM($PC_{10:8}$,A,M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0	4C	|0100|1100|	0 → $RAM(B)_0$	None	Reset RAM Bit
	1	45	|0100|0101|	0 → $RAM(B)_1$		
	2	42	|0100|0010|	0 → $RAM(B)_2$		
	3	43	|0100|0011|	0 → $RAM(B)_3$		

Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SMB	0	4D	|0100|1101|	1 → RAM(B)$_0$	None	Set RAM Bit
	1	47	|0100|0111|	1 → RAM(B)$_1$		
	2	46	|0100|0110|	1 → RAM(B)$_2$		
	3	4B	|0100|1011|	1 → RAM(B)$_3$		
STII	y	7–	|0111| y |	y → RAM(B) Bd ⊕ 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	–6	|00|r|0110| (r=0:3)	RAM(B) → A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 – –	|0010|0011| |1| r | d |	RAM(r,d) → A	None	Exchange A with RAM pointed to directly by r,d
XDS	r	–7	|00|r|0111| (r=0:3)	RAM(B) → A Bd–1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd. Exclusive-OR Br with r
XIS	r	–4	|00|r|0100| (r=0:3)	RAM(B) → A Bd+1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	|0101|0000|	A → Bd	None	Copy A to Bd
CBA		4E	|0100|1110|	Bd → A	None	Copy Bd to A
LBI	r,d	– –	|00|r|(d–1)| (r=0:3: d=0,9:15) or	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
		33 – –	|0011|0011| |1| r | d | (any r, any d)			
LEI	y	33 6–	|0011|0011| |0110| y |	y → EN	None	Load EN Immediate (Note 7)
XABR		12	|0001|0010|	A ←→ Br	None	Exchange A with Br (Note 8)
TEST INSTRUCTIONS						
SKC		20	|0010|0000|		C="1"	Skip if C is True
SKE		21	|0010|0001|		A=RAM(B)	Skip if A Equals RAM
SKGZ		33 21	|0011|0011| |0010|0001|		$G_{3:0}=0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	|0011|0011|	1st byte		Skip if G Bit is Zero
	0	01	|0000|0001|	2nd byte	$G_0=0$	
	1	11	|0001|0001|		$G_1=0$	
	2	03	|0000|0011|		$G_2=0$	
	3	13	|0001|0011|		$G_3=0$	

Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
SKMBZ	0	01	0000 0001		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0001 0001		$RAM(B)_1 = 0$	
	2	03	0000 0011		$RAM(B)_2 = 0$	
	3	13	0001 0011		$RAM(B)_3 = 0$	
SKT		41	0100 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 0011 0010 1010	$G \rightarrow A$	None	Input G Ports to A
ININ		33 28	0011 0011 0010 1000	$IN \rightarrow A$	None	Input IN Inputs to A (Note 2)
INIL		33 29	0011 0011 0010 1001	IL_3, CKO, "0", $IL_0 \rightarrow A$	None	Input IL Latches to A (Note 3)
INL		33 2E	0011 0011 0010 1110	$L_{7:4} \rightarrow RAM(B)$ $L_{3:0} \rightarrow A$	None	Input L Ports to RAM,A
OBD		33 3E	0011 0011 0011 1110	$Bd \rightarrow D$	None	Output Bd to D Outputs
OGI	y	33 5–	0011 0011 0101 y	$y \rightarrow G$	None	Output to G Ports Immediate
OMG		33 3A	0011 0011 0011 1010	$RAM(B) \rightarrow G$	None	Output RAM to G Ports
XAS		4F	0100 1111	$A \leftrightarrow SIO$, $C \rightarrow SKL$	None	Exchange A with SIO (Note 3)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B(Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Note 8: For 2K ROM devices, $A \leftrightarrow Br$ ($0 \rightarrow A3$). For 1K ROM devices, $A \leftrightarrow Br$ ($0,0 \rightarrow A3, A2$).

Note 9: Do not use CTMA instruction when dual-clock option is selected and part is running from D0 clocks.

Description of Selected Instructions

XAS INSTRUCTION

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC+1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows: A → PC(7:4), RAM(B) → PC(3:0), leaving PC(10), PC(9) and PC(8) unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost.

NOTE: LQID uses 2 instruction cycles if executed, one if skipped.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10,PC9 and PC8 are not affected by JID.

NOTE: JID uses 2 instruction cycles if executed, one if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

NOTE: If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter:

```
CAMT  ; load T counter
SKT   ; skip if overflow flag is set and reset it
NOP
```

IT INSTRUCTION

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped. IT instruction is not allowed if the T counter is mask-programmed as an external event counter (option #31=1).

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN3 and IN0 inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A 0 is input into A1. IL latches are cleared on reset. IL latches are not available on the COP445C/425C, and COP426C.

INSTRUCTION SET NOTES

a. The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.

c. The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

NOTE: The COP424C/425C/426C needs only 10 bits to address its ROM. Therefore, the eleventh bit (P10) is ignored.

Power Dissipation

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. For example, a 500 kHz crystal input will typically draw 100 μA more than a squarewave input. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate the COP444C/424C/426C operating current drain.

$$I_{CO} = I_Q + V \times 40 \times Fi + V \times 1400 \times Fi/Dv$$

where I_{CO} = chip operating current drain in microamps
I_Q = quiescent leakage current (from curve)
Fi = CKI frequency in MegaHertz
V = chip V_{CC} in volts
Dv = divide by option selected

For example at 5 volts V_{CC} and 400 kHz (divide by 4)

$$I_{CO} = 20 + 5 \times 40 \times 0.4 + 5 \times 1400 \times 0.4/4$$
$$I_{CO} = 20 + 80 + 700 = 800\ \mu A$$

At 2.4 volts V_{CC} and 30 kHz (divide by 4)

$$I_{CO} = 6 + 2.4 \times 40 \times 0.03 + 2.4 \times 1400 \times 0.03/4$$
$$I_{CO} = 6 + 2.88 + 25.2 = 34.08\ \mu A$$

Power Dissipation (Continued)

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation:

$Ici = I_Q + V \times 40 \times Fi$

For example, at 5 volts V_{CC} and 400 kHz

$Ici = 20 + 5 \times 40 \times 0.4 = 100\ \mu A$

The total average current will then be the weighted average of the operating current and the idle current:

$$Ita = I_{CO} \times \frac{To}{To+Ti} + Ici \times \frac{Ti}{To+Ti}$$

where: Ita = total average current
I_{CO} = operating current
Ici = idle current
To = operating time
Ti = idle time

I/O OPTIONS

Outputs have the following optional configurations, illustrated in *Figure 11*:

a. Standard — A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC}, compatible with CMOS and LSTTL.

b. Low Current — This is the same configuration as a. above except that the sourcing current is much less.

c. Open Drain — An N-channel device to ground only, allowing external pull-up as required by the user's application.

d. Standard TRI-STATE L Output — A CMOS output buffer similar to a. which may be disabled by program control.

e. Low-Current TRI-STATE L Output — This is the same as d. above except that the sourcing current is much less.

f. Open-Drain TRI-STATE L Output — This has the N-channel device to ground only.

All inputs have the following options:

g. Input with on chip load device to V_{CC}

h. Hi-Z input which must be driven by the users logic.

When using either the G or L I/O ports as inputs, a pull-up device is necessary. This can be an external device or the following alternative is available: Select the low-current output option. Now, by setting the output registers to a logic "1" level, the P-channel devices will act as the pull-up load. Note that when using the L ports in this fashion the Q registers must be set to a logic "1" level and the L drivers MUST BE ENABLED by an LEI instruction (see description above).

All output drivers use one or more of three common devices numbered 1 to 3. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 12* for each of these devices to allow the designer to effectively use these I/O configurations.

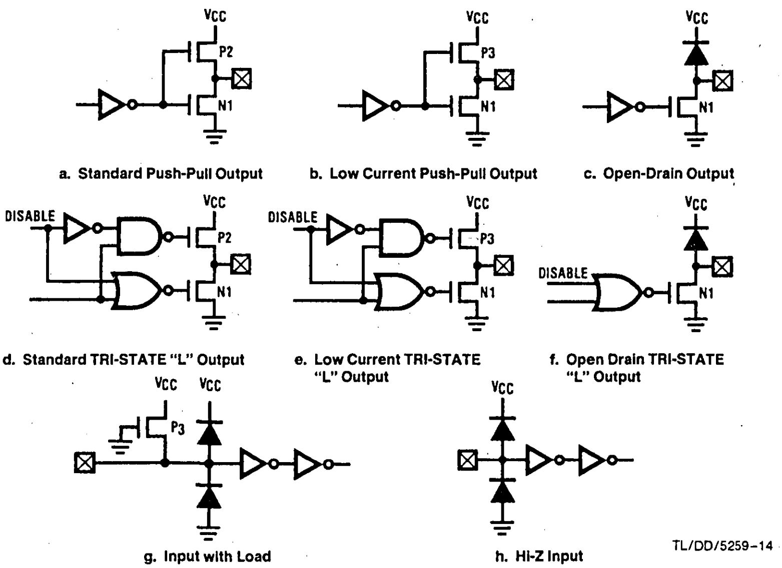
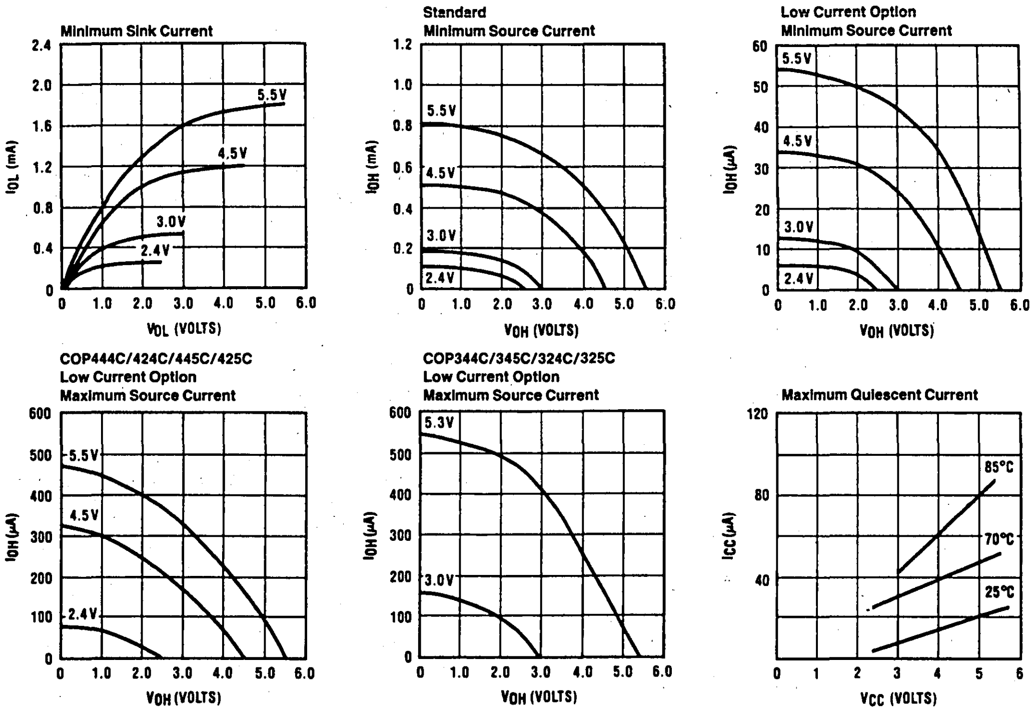


FIGURE 11. Input/Output Configurations



TL/DD/5259-15

FIGURE 12. Input/Output Characteristics

Option List

The COP444C/445C/424C/425C/COP426C mask-programmable options are assigned numbers which correspond with the COP444C/424C pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin
- = 0: clock generator output to crystal/resonator
- = 1: HALT I/O port
- = 2: general purpose input with load device to V_{CC}
- = 3: general purpose input, high-Z

Option 3: CKI input
- = 0: Crystal controlled oscillator input divide by 4
- = 1: Crystal controlled oscillator input divide by 8
- = 2: Crystal controlled oscillator input divide by 16
- = 4: Single-pin RC controlled oscillator (divide by 4)
- = 5: External oscillator input divide by 4
- = 6: External oscillator input divide by 8
- = 7: External oscillator input divide by 16

Option 4: $\overline{\text{RESET}}$ input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 5: L7 Driver
- = 0: Standard TRI-STATE push-pull output
- = 1: Low-current TRI-STATE push-pull output
- = 2: Open-drain TRI-STATE output

Option 6: L6 Driver — (same as option 5)

Option 7: L5 Driver — (same as option 5)

Option 8: L4 Driver — (same as option 5)

Option 9: IN1 input
- = 0: load device to V_{CC}
- = 1: Hi-Z input

Option 10: IN2 input — (same as option 9)

Option 11 = 0: V_{CC} Pin — no option available

Option 12: L3 Driver — (same as option 5)

Option 13: L2 Driver — (same as option 5)

Option 14: L1 Driver — (same as option 5)

Option 15: L0 Driver — (same as option 5)

Option List (Continued)

Option 16: SI input — (same as option 9)
Option 17: SO Driver
 = 0: Standard push-pull output
 = 1: Low-current push-pull output
 = 2: Open-drain output
Option 18: SK Driver — (same as option 17)
Option 19: IN0 Input — (same as option 9)
Option 20: IN3 Input — (same as option 9)
Option 21: G0 I/O Port — (same as option 17)
Option 22: G1 I/O Port — (same as option 17)
Option 23: G2 I/O Port — (same as option 17)
Option 24: G3 I/O Port — (same as option 17)
Option 25: D3 Output — (same as option 17)
Option 26: D2 Output — (same as option 17)
Option 27: D1 Output — (same as option 17)
Option 28: D0 Output — (same as option 17)
Option 29: Internal Initialization Logic
 = 0: Normal operation
 = 1: No internal initialization logic
Option 30: Dual Clock
 = 0: Normal operation
 = 1: Dual Clock. D0 RC oscillator (opt. #28 must = 2)
 = 2: Dual Clock. D0 ext. clock input (opt. #28 must = 2)

Option 31: Timer
 = 0: Time-base counter
 = 1: External event counter
Option 32: MICROBUS
 = 0: Normal
 = 1: MICROBUS (opt. #31 must = 0)
Option 33: COP bonding
(1k and 2K Microcontroller)
 = 0: 28-pin package
 = 1: 24-pin package
 = 2: Same die purchased in both 24 and 28 pin version.
(1K Microcontroller only)
 = 3: 20-pin package
 = 4: 28- and 20-pin package
 = 5: 24- and 20-pin package
 = 6: 28-, 24- and 20-pin package

Note:—if opt. #33 = 2 then opt. #9, 10, 19, 20 and 32 must = 0—if opt. #33 = 3, 4, 5 or 6 then opt. #9, 10, 19, 20, 21, 22, 30 and 32 must = 0

National Semiconductor

microCMOS

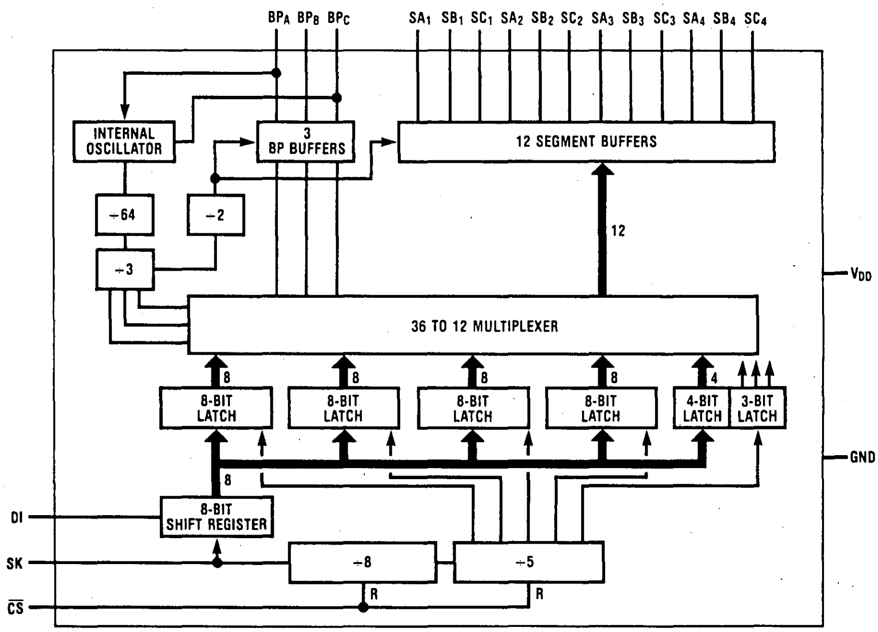
COP472-3 Liquid Crystal Display Controller

General Description

The COP472-3 Liquid Crystal Display (LCD) Controller is a peripheral member of the COPS™ family, fabricated using CMOS technology. The COP472 drives a multiplexed liquid crystal display directly. Data is loaded serially and is held in internal latches. The COP472 contains an on-chip oscillator and generates all the multi-level waveforms for backplanes and segment outputs on a triplex display. One COP472 can drive 36 segments multiplexed as 3 x 12 (4½ digit display). Two COP472 devices can be used together to drive 72 segments (3 x 24) which could be an 8½ digit display.

Features

- Direct interface to TRIPLEX LCD
- Low power dissipation (100 μW typ.)
- Low cost
- Compatible with all COP400 processors
- Needs no refresh from processor
- On-chip oscillator and latches
- Expandable to longer displays
- Software compatible with COP470 V.F. Display Driver chip
- Operates from display voltage
- MICROWIRE™ compatible serial I/O
- 20-pin dual-in-line package



COP472 Block Diagram

Absolute Maximum Ratings

Voltage at CS, DI, SK pins	−0.3V to +9.5V
Voltage at all other Pins	−0.3V to V_{DD} + 0.3V
Operating Temperature Range	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

DC Electrical Characteristics

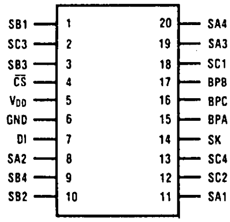
GND = 0V, V_{DD} = 2.4V to 5.5V, T_A = 0°C to 70°C (depends on display characteristics)

Parameter	Conditions	Min.	Max.	Units
Power Supply Voltage, V_{DD}		3.0	5.5	Volts
Power Supply Current, I_{DD} (Note 1)	V_{DD} = 5.5V		250	μA
	V_{DD} = 3V		100	μA
Input Levels DI, SK, CS V_{IL} V_{IH}		 0.7 V_{DD}	 0.8 9.5	 Volts Volts
BPA (as Osc. In) V_{IL} V_{IH}		 V_{DD} − 0.6	 0.6 V_{DD}	 Volts Volts
Output Levels, BPC (as Osc. Out) V_{OL} V_{OH}		 V_{DD} − 0.4	 0.4 V_{DD}	 Volts Volts
Backplane Outputs (BPA, BPB, BPC) $V_{BPA, BPB, BPC}$ ON $V_{BPA, BPB, BPC}$ OFF	 During BP^+ Time	 $V_{DD} - \Delta V$ $\frac{1}{3}V_{DD} - \Delta V$	 V_{DD} $\frac{1}{3}V_{DD} + \Delta V$	 Volts Volts
$V_{BPA, BPB, BPC}$ ON $V_{BPA, BPB, BPC}$ OFF	During BP^- Time	0 $\frac{2}{3}V_{DD} - \Delta V$	ΔV $\frac{2}{3}V_{DD} + \Delta V$	Volts Volts
Segment Outputs ($SA_1 \sim SA_4$) V_{SEG} ON V_{SEG} OFF	 During BP^+ Time	 0 $\frac{2}{3}V_{DD} - \Delta V$	 ΔV $\frac{2}{3}V_{DD} + \Delta V$	 Volts Volts
V_{SEG} ON V_{SEG} OFF	During BP^- Time	$V_{DD} - \Delta V$ $\frac{1}{3}V_{DD} - \Delta V$	V_{DD} $\frac{1}{3}V_{DD} + \Delta V$	Volts Volts
Internal Oscillator Frequency		15	80	kHz
Frame Time (Int. Osc. ÷ 192)		2.4	12.8	ms
Scan Frequency ($1/T_{SCAN}$)		39	208	Hz
SK Clock Frequency		4	250	kHz
SK Width		1.7		μs
DI Data Setup, t_{SETUP} Data Hold, t_{HOLD}		 1.0 100		 μs ns
$\overline{CS}$ t_{SETUP} t_{HOLD}		 1.0 1.0		 μs μs
Output Loading Capacitance			100	pF

Note 1: Power supply current is measured in stand-alone mode with all outputs open and all inputs at V_{DD}.

Note 2: $\Delta V = 0.05 V_{DD}$ for $V_{DD} \geq 3V$. $\Delta V = 0.15V$ for $V_{DD} < 3V$.

COP472
Connection Diagram



Order Number COP472N-3
NS Package N20A

Figure 2. Connection Diagram

Pin	Description
$\overline{CS}$	Chip select
V_{DD}	Power supply (display voltage)
GND	Ground
DI	Serial data input
SK	Serial clock input
BP_A	Display backplane A(or oscillator in)
BP_B	Display backplane B
BP_C	Display backplane C (or oscillator out)
SA1~SC4	12 multiplexed outputs

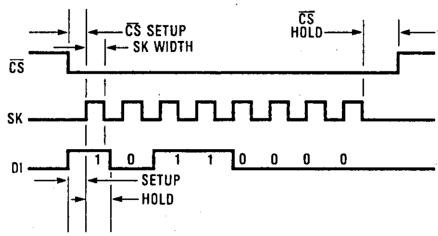


Figure 3. Serial Load Timing Diagram

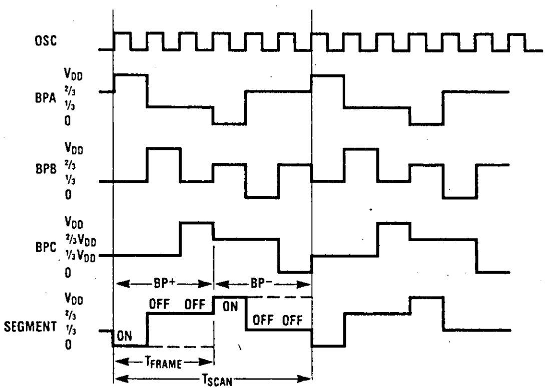


Figure 4. Backplane and Segment Waveforms

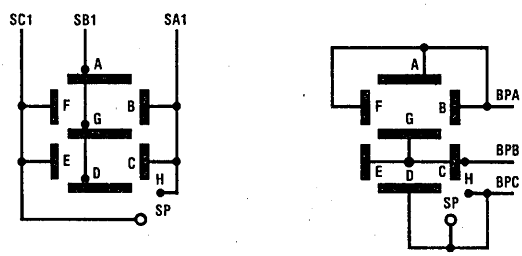


Figure 5. Typical Display Internal Connections Epson LD-370

Functional Description

The COP472 drives 36 bits of display information organized as twelve segments and three backplanes. The COP472 requires 40 information bits: 36 data and 4 control. The function of each control bit is described below. Display information format is a function of the LCD interconnections. A typical segment/backplane configuration is illustrated in Figure 5, with this configuration the COP472 will drive 4 digits of 9 segments.

To adapt the COP472 to any LCD display configuration, the segment/backplane multiplex scheme is illustated in Table 1.

Two or more COP472 chips can be cascaded to drive additional segments. There is no limit to the number of COP472's that can be used as long as the output loading capacitance does not exceed specification.

Table 1. COP472 Segment/Backplane Multiplex Scheme

Bit Number	Segment, Backplane	Data to Numeric Display	
1	SA1, BPC	SH	Digit 1
2	SB1, BPB	SG	
3	SC1, BPA	SF	
4	SC1, BPB	SE	
5	SB1, BPC	SD	
6	SA1, BPB	SC	
7	SA1, BPA	SB	
8	SB1, BPA	SA	
9	SA2, BPC	SH	Digit 2
10	SB2, BPB	SG	
11	SC2, BPA	SF	
12	SC2, BPB	SE	
13	SB2, BPC	SD	
14	SA2, BPB	SC	
15	SA2, BPA	SB	
16	SB2, BPA	SA	
17	SA3, BPC	SH	Digit 3
18	SB3, BPB	SG	
19	SC3, BPA	SF	
20	SC3, BPB	SE	
21	SB3, BPC	SD	
22	SA3, BPB	SC	
23	SA3, BPA	SB	
24	SB3, BPA	SA	
25	SA4, BPC	SH	Digit 4
26	SB4, BPB	SG	
27	SC4, BPA	SF	
28	SC4, BPB	SE	
29	SB4, BPC	SD	
30	SA4, BPB	SC	
31	SA4, BPA	SB	
32	SB4, BPA	SA	
33	SC1, BPC	SP1	Digit 1
34	SC2, BPC	SP2	Digit 2
35	SC3, BPC	SP3	Digit 3
36	SC4, BPC	SP4	Digit 4
37	not used		
38	Q6		
39	Q7		
40	SYNC		

Segment Data bits

Data is loaded in serially, in sets of eight bits. Each set of segment data is in the following format:

SA	SB	SC	SD	SE	SF	SG	SH

Data is shifted into an eight bit shift register. The first bit of the data is for segment H, digit 1. The eighth bit is segment A, digit 1. A set of eight bits is shifted in and then loaded into the digit one latches. The second set of 8 bits is loaded into digit two latches. The third set into digit three latches, and the fourth set is loaded into digit four latches.

Control Bits

The fifth set of 8 data bits contains special segment data and control data in the following format:

SYNC	Q7	Q6	X	SP4	SP3	SP2	SP1

The first four bits shifted in contain the special character segment data. The fifth bit is not used. The sixth and seventh bits program the COP472 as a stand alone LCD driver or as a master or slave for cascading COP472's. BPC of the master is conected to BPA of each slave. The following table summarizes the function of bits six and seven:

Q7	Q6	Function	BPC Output	BPA Output
1	1	Slave	Backplane Output	Oscillator Input
0	1	Stand Alone	Backplane Output	Backplane Output
1	0	Not Used	Internal Osc. Output	Oscillator Input
0	0	Master	Internal Osc. Output	Backplane Output

The eighth bit is used to synchronize two COP472's to drive an 8½-digit display.

Loading Sequence to Drive a 4½-Digit Diaplay

Steps:

1. Turn $\overline{CE}$ low.
2. Clock in 8 bits of data for digit 1.
3. Clock in 8 bits of data for digit 2.
4. Clock in 8 bits of data for digit 3.
5. Clock in 8 bits of data for digit 4.
6. Clock in 8 bits of data for special segment and control function of BPC and BPA.

   0 0 1 1 SP4 SP3 SP2 SP1

7. Turn $\overline{CS}$ high.

Note: $\overline{CS}$ may be turned high after any step. For example to load only 2 digits of data, do steps 1, 2, 3, and 7.

$\overline{CS}$ must make a high to low transition before loading data in order to reset internal counters.

Loading Sequence to Drive an 8½-Digit Display

Two or more COP472's may be connected together to drive additional segments. An eight digit multiplexed display is shown in Figure 7. The following is the loading sequence to drive an eight digit display using two COP472's. The right chip is the master and the left the slave.

Steps:

1. Turn $\overline{CS}$ low on both COP472's.
2. Shift in 32 bits of data for for the slave's four digits.
3. Shift in 4 bits of special segment data: a zero and three ones.

1	1	1	0	SP4	SP3	SP2	SP1

   This synchronizes both the chips and BPA is oscillator input. Both chips are now stopped.
4. Turn CS high to both chips.
5. Turn CS low to master COP472.
6. Shift in 32 bits of data for the master's 4 digits.
7. Shift in four bits of special segment data, a one and three zeros.

0	0	0	1	SP4	SP3	SP2	SP1

   This sets the master COP472 to BPA as a normal backplane output and BPC as oscillator output. Now both the chips start and run off the same oscillator.
8. Turn $\overline{CS}$ high.

The chips are now synchronized and driving 8 digits of display. To load new data simply load each chip separately in the normal manner, keeping the correct status bits to each COP472 (0110 or 0001).

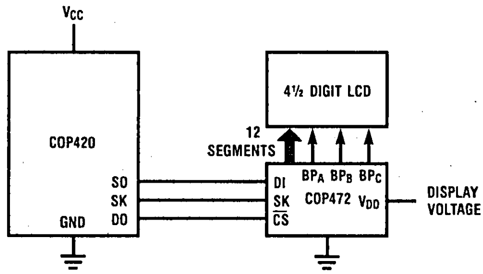


Figure 6. System Diagram — 4½ Digit Display

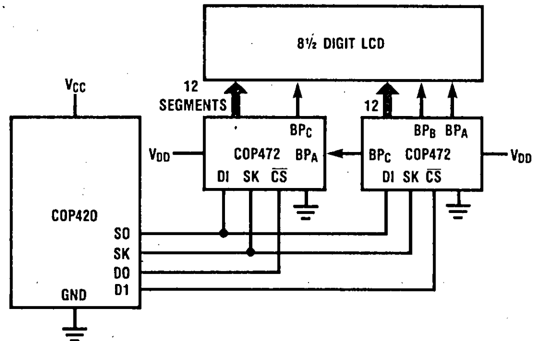


Figure 7. System Diagram — 8½ Digit Display

Example Software

Example 1

COP420 Code to load a COP472 [Display data is in M(0, 12)-M(0, 15), special segment data is in M(0, 0)]

```
              LBI 0, 12           ; POINT TO FIRST DISPLAY DATA
              OBD                 ; TURN CS LOW (DO)
LOOP:         CLRA
              LQID                ; LOOK UP SEGMENT DATA
              CQMA                ; COPY DATA FROM Q TO M & A
              SC                  ; SET C TO TURN ON SK
              XAS                 ; OUTPUT LOWER 4 BITS OF DATA
              NOP                 ; DELAY
              NOP                 ; DELAY
              LD                  ; LOAD A WITH UPPER 4 BITS
              XAS                 ; OUTPUT 4 BITS OF DATA
              NOP                 ; DELAY
              NOP                 ; DELAY
              RC                  ; RESET C
              XAS                 ; TURN OFF SK CLOCK
              XIS                 ; INCREMENT B FOR NEXT DATA
              JP LOOP             ; SKIP THIS JUMP AFTER LAST DIGIT
              SC                  ; SET C
              LBI 0, 0            ; ADDRESS SPECIAL SEGMENTS
              LD                  ; LOAD INTO A
              XAS                 ; OUTPUT SPECIAL SEGMENTS
              NOP                 ;
              CLRA                ;
              AISC 12             ; 12 to A
              XAS                 ; OUTPUT CONTROL BITS
              NOP                 ;
              LBI 0, 15           ; 15 to B
              RC                  ; RESET C
              XAS                 ; TURN OFF SK
              OBD                 ; TURN CS HIGH (DO)
```

Example 2

COP420 Code to load two COP472 parts [display data is in M(0, 12)-M(0,15) and M(1, 12)-M(1, 15), special segment data is in M(0, 0) and M(1, 0)]

```
INIT:     LBI    0, 15
          OBD           ; TURN BOTH CS'S HIGH
          LEI    8      ; ENABLE SO OUT OF S. R.
          RC
          XAS           ; TURN OFF SK CLOCK
          LBI    3, 15  ; USE M(3, 15) FOR CONTROL BITS
          STII   7      ; STORE 7 TO SYNC BOTH CHIPS
          LBI    0, 12  ; SET B TO TURN BOTH CS'S LOW
          JSR    OUT    ; CALL OUTPUT SUBROUTINE
```

MAIN DISPLAY SEQUENCE

```
DISPLAY:  LBI    3, 15
          STII   8      ; SET CONTROL BITS FOR SLAVE
          LBI    0, 13  ; SET B TO TURN SLAVE CS LOW
          JSR    OUT    ; OUTPUT DATA FROM REG. 0
          LBI    3, 15
          STII   6      ; SET CONTROL BITS FOR MASTER
          LBI    1, 14  ; SET B TO TURN MASTER CS LOW
          JSR    OUT    ; OUTPUT DATA FROM REG. 1
```

OUTPUT SUBROUTINE

```
OUT:      OBD           ; OUTPUT B TO CS'S
          CLRA
          AISC   12     ; 12 TO A
          CAB           ; POINT TO DISPLAY DIGIT (BD=12)
LOOP:     CLRA
          LQID          ; LOOK UP SEGMENT DATA
          CQMA          ; COPY DATA FROM Q TO M & A
          SC
          XAS           ; OUTPUT LOWER 4 BITS OF DATA
          NOP           ; DELAY
          NOP           ; DELAY
          LD            ; LOAD A WITH UPPER 4 BITS
          XAS           ; OUTPUT 4 BITS OF DATA
          NOP           ; DELAY
          NOP           ; DELAY
          RC            ; RESET C
          XAS           ; TURN OFF SK
          XIS           ; INCREMENT B FOR NEXT DISPLAY DIGIT
          JP     LOOP   ; SKIP THIS JUMP AFTER LAST DIGIT
          SC            ; SET C
          NOP
          LD            ; LOAD SPECIAL SEGS. TO A (BD=0)
          XAS           ; OUTPUT SPECIAL SEGMENTS
          NOP
          LBI    3, 15
          LD            ; LOAD A
          XAS           ; OUTPUT CONTROL BITS
          NOP
          NOP
          RC
          XAS           ; TURN OFF SK
          OBD           ; TURN CS'S HIGH (BD=15)
          RET
```

National Semiconductor

COP498/COP398 Low Power CMOS RAM and Timer (RAT™) COP499/COP399 Low Power CMOS Memory

General Description

The COP498/398 Low Power CMOS RAM and Timer (RAT) and the COP499/399 Memory are peripheral members of the COPS™ family, fabricated using low power CMOS technology. These devices provide external data storage and/or timing, and are accessed via the simple MICROWIRE™ serial interface. Each device contains 256 bits of read/write memory organized into 4 registers of 64 bits each; each register can be serially loaded or read by a COPS controller.

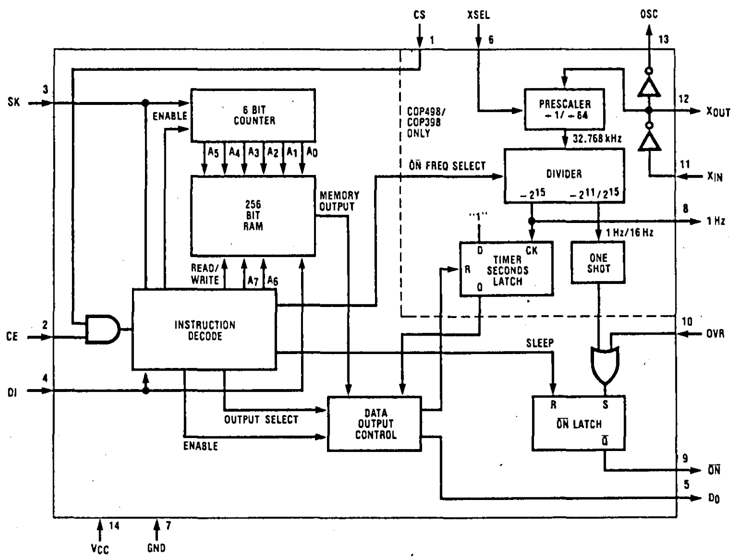
The COP498/398 also contain a crystal-based timer for timekeeping purposes, and can provide a "wake-up" signal to turn on a COPS controller. Hence, these devices are ideal for applications requiring very low power drain in a standby mode, while maintaining a real-time clock (e.g., electronically-tuned automobile radio). Power is minimized by cycling controller power off for periods of time when no processing is required.

The COP499/399 contain circuitry that enables the user to turn a controller on and off while maintaining the integrity of the memory.

A COP400 series N-channel microcontroller coupled with a COP498 (or 499) RAM/Timer offers a user the low-power advantages of an all CMOS system and the low-cost advantage of an NMOS system. This type of system is ideally suited to a wide variety of automotive and instrumentation applications.

Features

- Low power dissipation
- Quiescent current = 40 nA typical (25°C, V_{CC} = 3.0 V)
- Low cost
- Single supply operation (2.4V–5.5V)
- CMOS-compatible I/O
- 4 × 64 serial read/write memory
- Crystal-based selectable timer — 2.097152 MHz or 32.768 kHz (COP498/398)
- Software selectable 1 Hz or 16 Hz "wake-up" signal for COPS controller (COP498/398)
- External override to "wake-up" controller
- Compatible with all COP400 processors (processor $V_{CC} \leq 9.5V$)
- MICROWIRE-compatible serial I/O
- Memory protection with write enable and write disable instructions
- 14-pin dual-in-line package (COP498/398) or 8-pin dual-in-line package (COP499/399)



Absolute Maximum Ratings

Voltage relative to GND	
At XSEL, 1 Hz, X_{IN}, X_{OUT}, DO	−0.3V to V_{CC} + 0.3V
At all other pins	−0.3V to 10V
Maximum V_{CC} Voltage	6.5V
Total Sink Current Allowed	15 mA
Total Source Current Allowed	10 mA
Ambient Operating Temperature	
COP398/COP399	−40°C to +85°C
COP498/COP499	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	50 mW

"Absolute maximum ratings" indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not insured when operating the device at absolute maximum ratings.

DC Electrical Characteristics

COP398/COP399: −40°C ≤ T_A ≤ +85°C unless otherwise specified.
COP498/COP499: 0°C ≤ T_A ≤ +70°C unless otherwise specified.

Parameter	Conditions	Min.	Max.	Units
Operating Voltage	COP498/COP499	2.4	5.5	V
	COP398/COP399	3.0	5.5	V
Quiescent Current	All inputs at GND			
	T_A = 70°C, V_{CC} = 3.0V		4.0	μA
	T_A = 70°C, V_{CC} = 5.0V		10	μA
	T_A = 70°C, V_{CC} = 5.5V		20	μA
(COP398/COP399 only)	T_A = 85°C, V_{CC} = 3.0V		8.0	μA
	T_A = 85°C, V_{CC} = 5.0V		16	μA
	T_A = 85°C, V_{CC} = 5.5V		30	μA
COP498/COP398				
Standby Current (sleep mode)	V_{CC} = Min., Osc. = 2.097 MHz		200	μA
(running with crystal)	V_{CC} = Max., Osc. = 2.097 MHz		700	μA
	V_{CC} = Min., Osc. = 32.768 kHz		20	μA
	V_{CC} = Max., Osc. = 32.768 kHz		100	μA
Operating Current	SK = 250 kHz square wave			
	V_{CC} = Min., Osc. = 2.097 MHz		300	μA
	V_{CC} = Max., Osc. = 2.097 MHz		920	μA
	V_{CC} = Min., Osc. = 32.768 kHz		120	μA
	V_{CC} = Max., Osc. = 32.768 kHz		320	μA
COP499/COP399 Operating Current	SK = 250 kHz square wave			
	V_{CC} = Min.		100	μA
	V_{CC} = Max.		250	μA
Input Voltage Levels				
CE Input	(Schmitt Trigger Input)			
Logic High (V_{IH})		0.8 V_{CC}		V
Logic Low (V_{IL})			0.4 V_{CC}	V
OVR Input	(Schmitt Trigger Input)			
Logic High (V_{IH})		0.8 V_{CC}		V
Logic Low (V_{IL})			0.2 V_{CC}	V
All Other Inputs				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})			0.3 V_{CC}	V

DC Electrical Characteristics (cont'd)

Parameter	Conditions	Min.	Max.	Units
Output Voltage Levels — DO, 1 Hz				
CMOS Operation				
Logic High (V_{OH})	$I_{OH} = -10\mu A$	$V_{CC} - 0.1$		V
Logic Low (V_{OL})	$I_{OL} = 10\mu A$		0.1	V
Input Leakage Current	COP498/COP499, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	−1.0	+1.0	μA
	COP398/COP399, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	−2.0	+2.0	μA
TRI-STATE®, Open Drain Leakage Current	COP498/COP499, $V_H = V_{CC}$, $V_L = 0V$	−2.5	+2.5	μA
	COP398/COP399, $V_H = V_{CC}$, $V_L = 0V$	−5.0	+5.0	μA
Output Current Levels	$V_{CC} = 4.5V$			
Sink Current				
$\overline{OSC}$	$V_{OL} = 0.4V$	0.5		mA
$\overline{ON}$	$V_{OL} = 1.5V$	1.5	7.5	mA
X_{OUT}	XSEL = 1, $X_{IN} = 4.5V$, $V_{OL} = 1.0V$	0.25		mA
X_{OUT}	XSEL = 0, $X_{IN} = 4.5V$, $V_{OL} = 2.0V$	8.0		μA
1 Hz, DO	$V_{OL} = 0.8V$	0.8		mA
Source Current				
$\overline{ON}$	$V_{OH} = 1.0V$	60		μA
X_{OUT}	XSEL = 1, $X_{IN} = 0V$, $V_{OH} = 3.0V$	0.27		mA
X_{OUT}	XSEL = 0, $X_{IN} = 0V$, $V_{OH} = 3.0V$	10		μA
1 Hz, DO	$V_{OH} = 2.0V$	0.4		mA

AC Electrical Characteristics

COP398/COP399: $-40°C \leq T_A \leq +85°C$ unless otherwise specified.
COP498/COP499: $0°C \leq T_A \leq +70°C$ unless otherwise specified.

Parameter	Conditions	Min.	Max.	Units
COP Interface				
SK Frequency	CS = 1, CE = 1, COP498/COP499	4.096	250	kHz
	CS = 1, CE = 1, COP398/COP399	8.192	250	kHz
SK Duty Cycle	SK frequency ≥ 25 kHz	25	75	%
	SK frequency = Min.	48	52	%
Inputs				
CS				
t_{CSS}		0.2		μs
t_{CSH}		0		μs
DI				
t_{SETUP}		0.4		μs
t_{HOLD}		0.4		μs
Output				
DO	$C_L = 100pF$, $4.5V \leq V_{CC} \leq 5.5V$,			
t_{pd1}, t_{pd0}	$V_{OH} = 0.7V_{CC}$, $V_{OL} = 0.4V$		2.0	μs
t_{pd1}, t_{pd0}	$C_L = 50pF$, V_{CC} = Min., $V_{OH} = 2V$, $V_{OL} = 0.7V$		2.4	μs
Crystal Osc. Frequency	XSEL = 1		2.1	MHz
	XSEL = 0		65	kHz

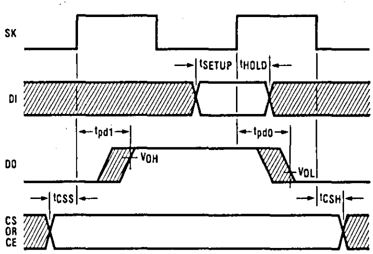
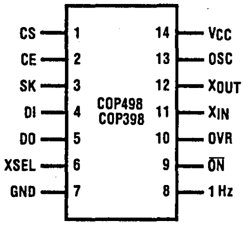
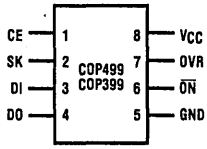


Figure 2. Synchronous Data Timing



Order Number COP498N, COP398N
NS Package N14A



Order Number COP499N, COP399N
NS Package N08E

Figure 3. Pin Connection Diagrams

Pin	Description	Pin	Description
CS	Chip Select	1 Hz	1 Hz Square Wave Output
CE	Chip Enable	$\overline{ON}$	Active Low Wake-Up Signal to COPS™ Controller
SK	Serial Data Clock	OVR	External Override Wake-Up for COPS Controller
DI	Serial Data Input	OSC	Open Drain Oscillator Output
DO	Serial Data Output	V_{CC}	Power Supply
XSEL	Crystal Option Select	GND	Ground
X_{IN}	Crystal Oscillator Input		
X_{OUT}	Crystal Oscillator Output		

COP398 and COP399 are extended temperature devices (−40 °C to +85 °C) of COP498 and COP499 (0 °C to 70 °C) respectively, with all other functional and electrical characteristics being the same. Therefore, no further attempt will be made to distinguish between COP498 and COP398 or between COP499 and COP399. Unless otherwise specified, the following descriptions will apply to both COP498 and COP499, and they will be known as the device.

Instruction Set

COP498 has six instructions as indicated in Figure 4. Note that the MSB of any given instruction is a "1". This bit is properly viewed as a start bit in the interface sequence. The lower 4 bits of the instruction contain the command for the device. One of the instructions (TSEC) should not be used in COP499 as it serves no purpose.

Instruction	Opcode (MSB)	Comments
WRITE	1 s 1 r_1 r_0	s=$\overline{ON}$ (wake up signal) frequency select 1=16 Hz, 0=1 Hz (s selection for COP498 only) (s=0 for COP499)
READ	1 1 0 r_1 r_0	r_1, r_0 = register number (00, 01, 10, 11)
WREN	1 0 0 1 1	Write enable
WRDS	1 0 0 0 0	Write disable
TSEC	1 0 0 1 0	Test timer seconds latch (COP498 only)
SLEEP	1 0 0 0 1	Put COPS™ controller to sleep ($\overline{ON}$ high)

Figure 4. Instruction Set

Functional Description

A block diagram of COP498 and COP499 is given in Figure 1. Positive logic is used. When a bit is set to the higher voltage it is a logic "1"; when a bit is reset to the lower voltage it is a logic "0". The COP498 can execute six instructions: READ (from any one of 4 registers in memory); WRITE (to any one of 4 registers in memory); WREN (write enable); WRDS (write disable); TSEC (test and reset timer seconds latch); and SLEEP (drive $\overline{ON}$ signal high to turn off COPS™ controller). The COP499 can execute all the above instructions except TSEC. All communications with the device are via the serial MICROWIRE™ interface. Both CS and CE (CE only in COP499) must be high to enable the device. The device must be deselected between instructions — either CS and/or CE must go low to insure proper operation. The deselecting of the device resets the counters and serial input register.

Read/Write Memory

The device has 256 bits of read/write memory. The memory is organized as 4 registers of 64 bits each. The data is accessed serially through the Data Input (DI) and Data Output (DO) pins. SK is the clock signal for data and instructions.

The memory address register can be conceived of as two registers: one two bits long and loaded directly from the instruction; the other six bits long and incremented by 1 with each SK pulse as long as the chip is selected. The two bit register does not change during the execution of a given instruction. The six bit register is reset to zero while the device is deselected. When counting, the six bit register wraps around from its maximum value back to zero. Thus memory locations are addressed relative to the number of SK pulses after the chip is selected.

The READ instruction will select one of the 4 registers (the register being identified in the instruction opcode as indicated in Figure 4) and output the contents of that register to the DO pin until the device is deselected. Note that data output from the device, as a result of a READ instruction, continues as long as the device is selected and clocks are provided. Reading more than 64 bits will cause rereading of some bits as the memory address register wraps around from the maximum value back to zero.

The WRITE instruction selects one of the 4 registers (the register being identified in the instruction opcode as indicated in Figure 4) and takes the data from the DI pin and stores that data into the memory register until the device is deselected. The write operation continues as long as the device is selected and clocks are provided. Thus writing more than 64 bits will cause a portion of the data to be overwritten.

Timer (COP498 only)

With the XSEL pin tied high (V_{CC}), the timer is a 21 stage counter which can divide a 2.097152 MHz signal down to 1 Hz. This creates the 1 Hz signal output. With XSEL tied low (ground), the timer is a 15 stage counter which divides a 32.768 kHz signal down to create the 1 Hz signal output. The rising edge of the 1 Hz signal is used internally to set the timer seconds latch. A wake-up signal is generated at the $\overline{ON}$ output. This signal can be used to turn a COPS controller on. The wake-up rate is software selectable and may be either 1 Hz or 16 Hz. A bit in the WRITE instruction controls this wake-up rate (see Figure 4). By means of the SLEEP instruction a COPS controller may cause the $\overline{ON}$ signal to go high thereby providing a means for the controller to safely turn itself off.

An override capability is present whereby the $\overline{ON}$ pin may be prevented from going high. A "1" level at the OVR pin will force $\overline{ON}$ to go low (or stay low) thereby causing the controller to turn on or remain on. $\overline{ON}$ will remain low, and the controller on, as long as the OVR pin is high. To preserve timekeeping when using the override feature, a timer seconds latch is provided. This latch is set by the rising edge of the 1 Hz signal and is read and reset by the TSEC instruction. The timer seconds latch is primarily intended for use when the override feature is implemented. However, it does provide a convenient one second timer which is software testable over a common serial port.

System Considerations

When the COPS processor is being turned on and off, during the power supply transition between ground and operating voltage, some pulses may occur at the output pins of the processor. By using the WRDS and WREN instructions, together with the higher "1" level of the CE pin, accidental writing into the memory may be prevented. This is done by disabling the write operation before going to sleep and enabling the write operation when the COPS processor starts execution. A WRDS instruction is automatically executed if the SLEEP instruction causes $\overline{ON}$ to go high turning off the COPS processor. Furthermore, WREN instruction is disabled as long as $\overline{ON}$ remains high.

The XSEL pin, which identifies the timer counter length, should be tied to either V_{CC} or ground depending on the crystal input. For proper operation, the state of XSEL should not be changed while the device is in operation. If the oscillator and timer features are not used, the X_{IN} pin should be connected to the GND pin and XSEL tied to V_{CC}. If the override feature is not used the OVR pin should be connected to the GND pin.

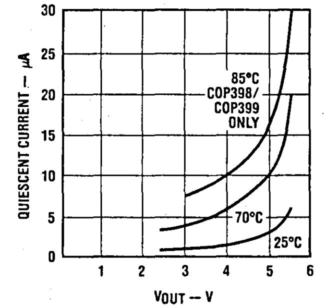
The device is in a static mode when either the CS or CE pin is low. However, the device is in a dynamic mode when both CS and CE are high and at least one high level has been detected at SK while both pins are high. Because of this, a minimum frequency is specified for the SK clock. This minimum frequency really translates to maximum on and off times for the SK clock. As the SK clock slows down, the duty cycle must get closer to 50%. For best operation, the user should regard the maximum on and off times for the SK clock as about 122 µs (61 µs for COP398/COP399).

COPS™ Controller to COP498/COP499 Hardware Interface

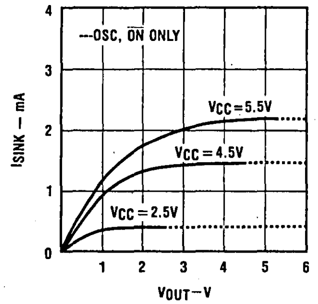
If the COPS controller is operating with a 4 µs instruction cycle time, a 47k resistor should be connected between SK and V_{CC} to speed up the rise time of the SK clock. If the override feature is used in COP498, the override signal should be connected to the OVR pin of the COP498 and an input of the COPS controller. This is simply to provide a means for the controller to know if it was turned on by override or normal timeout. The override signal should be free of noise. In systems where the COPS controller is operating with V_{CC} greater than 6 volts, SI and the override input on the controller should have high impedance, standard TTL level input options selected. To minimize current drain in the controller, the override input to the controller should always use the high impedance option.

Figure 6a illustrates the COP498 interface in a system with supply voltage less than 6 volts. The COPS controller can either be turned on by the timer or an external signal. A PNP transistor, controlled by the $\overline{ON}$ signal of the COP498, is used to gate the power to the COPS controller. A 0.05 µF capacitor is connected across the supply pins of the controller to reduce voltage variations due to current spikes. It is not recommended to use large capacitance values here as problems can be introduced if the power supply fall time is too long. The switched supply fall time should be kept to about ten instruction cycles of the COPS processor. Resistor R2, between the $\overline{ON}$ pin of the COP498 and the base of the transistor, is used to limit current. Resistor R1, between the base and emitter of the transistor, is used to turn the transistor off when $\overline{ON}$ is high. The CE pin of the COP498 is tied to the V_{CC} pin of the controller. This guarantees that the controller is at its full operating voltage before the COP498 can be accessed. When turned on, the PNP transistor should be saturated in order to minimize the voltage drop across it. The system power supply, which here is V_{CC} to the COP498, must be high enough to insure that the controller V_{CC} — which is the system supply less the voltage drop across the PNP transistor — is high enough to be recognized as a logic "1" at the CE input of the COP498. It is also desirable to have all input signals to the COP498 as close as possible to the COP498 supply levels to eliminate any static power drain which could significantly increase standby and operating current.

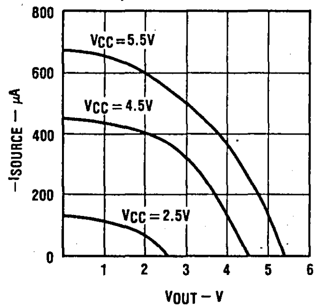
Maximum Quiescent Current COP498/499/398/399



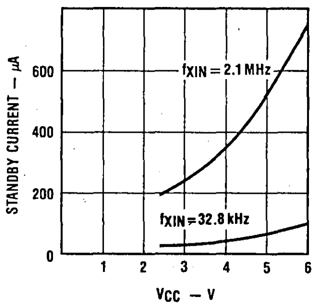
Minimum Sink Current for DO, 1 Hz, OSC, $\overline{ON}$



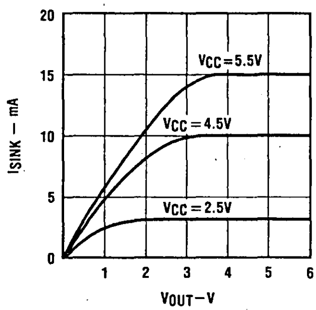
Minimum Source Current for DO, 1 Hz



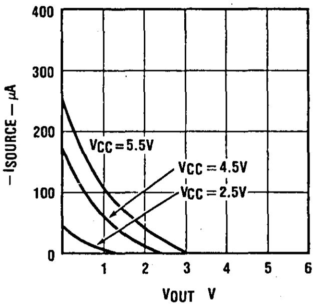
Maximum Standby Current for COP498/398



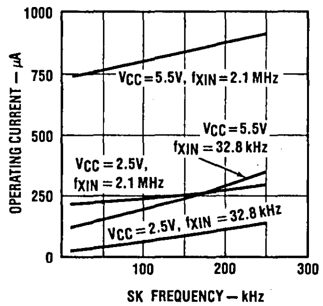
Maximum Sink Current for $\overline{ON}$



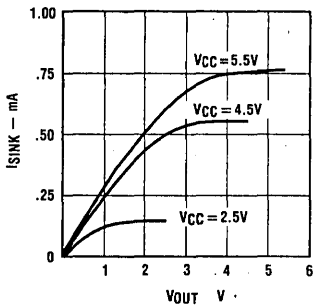
Minimum Source Current for $\overline{ON}$



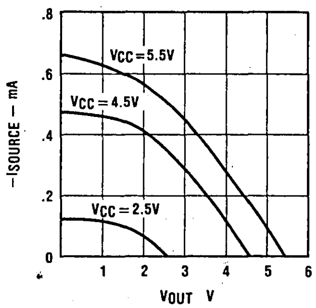
Maximum COP498/398 Operating Current



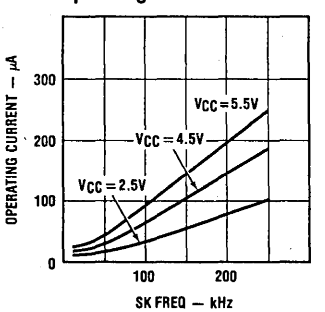
X_{OUT} Minimum Sink Current with XSEL = 1



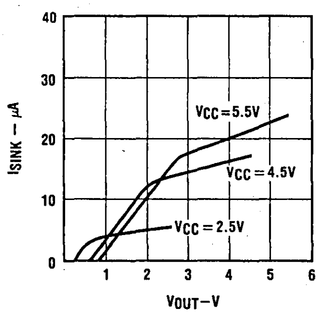
X_{OUT} Minimum Source Current with XSEL = 1



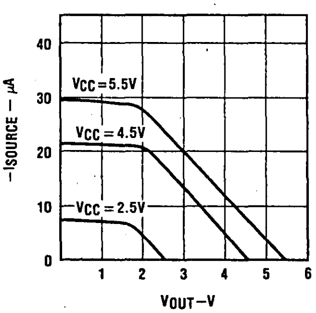
Maximum COP499/399 Operating Current



X_{OUT} Minimum Sink Current with XSEL = 0



X_{OUT} Minimum Source Current with XSEL = 0



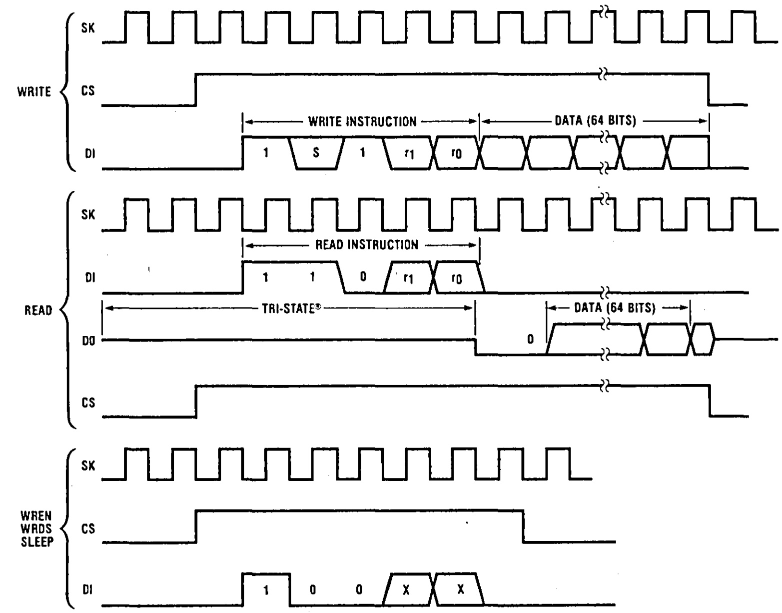


Figure 5a. Instruction Timing

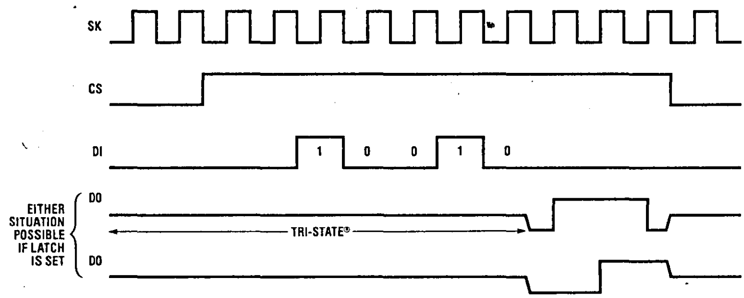


Figure 5b. TSEC Instruction Timing

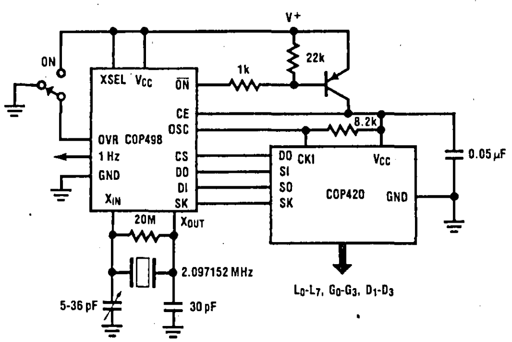


Figure 6a. COP498-COP420 Interface

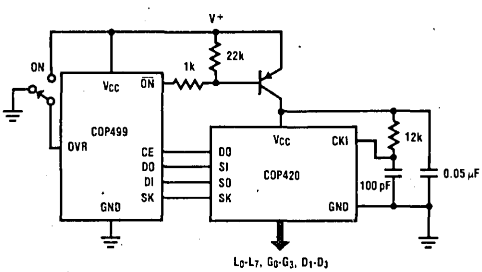


Figure 6b. COP499-COP420 Interface

Figure 6b illustrates the COP499 interface in a system with a supply voltage less than 6 volts. The COPS processor is being turned on by a switch (or an external signal) connected to the OVR pin.

Figure 7 illustrates a COP498 interface in a system with a supply voltage greater than 6 volts. In such a system, the COP498 cannot be connected directly across the system supply. The power to the COP498 is derived from the system supply by means of a standard zener diode arrangement. A zener diode with a breakdown of about 5 volts is recommended. A capacitor is connected across the COP498 supply pins to reduce voltage variations due to current spikes and to supply extra current when the COP498 is in active operation. Here it is assumed that the COP498 is in standby mode, i.e., deselected, most of the time and is active, selected, for a short period (less than 100 SK periods).

The zener diode series resistor R3 should be selected to meet the current requirements of the zener diode and the standby current of the device. The primary purpose of the zener diode is to place an upper limit on the value of V_{CC} to the device. This insures that V_{CC} to the device will not exceed the specified maximum value. Since the device will operate from 2.5V to 6.0V, the choice of zener diode and series resistor is not critical.

Note that the user may generate the two supply voltages in any manner compatible with system requirements.

Because the COPS™ controller and the device have different operating voltages, the high impedance standard TTL level input should be selected on the COPS controller for SI and any other input to the controller from the device.

Sample System Current Drain Calculation

Suppose a 5V system consists of a COP420 and a COP498 with a 32.768 kHz crystal. The COP420 is being turned on once a second. Assume that the COP420 needs 10 ms for internal reset and 10 ms to update all the necessary information, then the COP420 will be turned on for 20 ms every second, i.e., a duty cycle of 2%; and the COP498 will be in operating mode for at most 10 ms, i.e., a duty cycle of less than 1%. Because of the short duty cycle, it is further assumed that the COP498 current drain will be that of standby current, about 75 μA at 5V. The current drain through the base of the switching transistor that turns on the COP420 can be estimated by the voltage drop across the current limiting resistor and in this case is assumed to be 3.5 mA.

COP498 current drain = 75 μA
COP420 current drain = 0.02 × 25 mA = 500 μA
Switching transistor base current = 0.02 × 3.5 mA = 70 μA
Total system current drain = 500 + 70 + 75 μA = 645 μA

The result shows that it is possible to achieve the low cost of NMOS and low power dissipation of CMOS simultaneously with a system consisting of a COP498 and a COPS processor.

COPS™ Controller — COP498/398 Software Interface

Figure 8 shows a typical flow chart for a COP498 or COP499 interface to a COPS microcontroller system. This flow chart also illustrates the override feature. Since the override feature is being used, the first step is to inquire the device if it is necessary to increment the time. It is assumed that timekeeping is a necessary part of the application. This interrogation of the device is

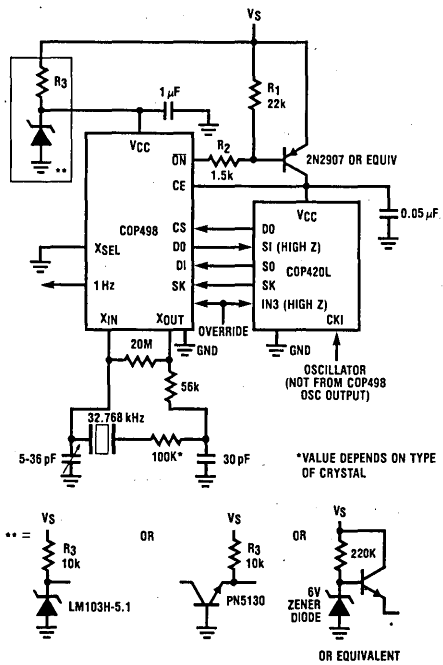


Figure 7. COP498-COP420L Interface with $V_S = 9V$ and 32.768 kHz Crystal

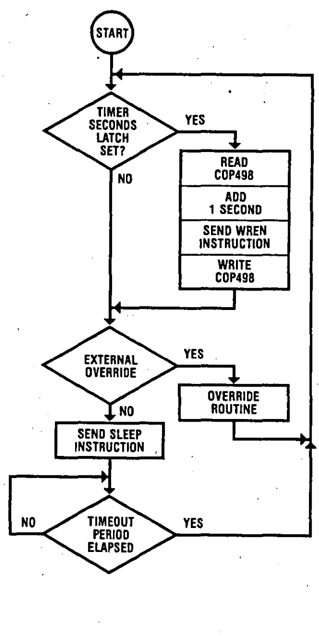


Figure 8. Typical COP498 Interface Flowchart

accomplished by means of the TSEC instruction which dumps the contents of the timer seconds latch to the serial output port and resets the latch. If the latch was set, the time must be incremented. This is accomplished by reading the appropriate memory register into the controller, incrementing the time and writing the register back out to the device. The next step is to check for the override signal. If it is present a special override routine may be performed. If no override is present, the controller turns itself off by sending a SLEEP command to the device. After sending the SLEEP command, the controller goes into a loop to wait for power to go off. In the event the controller is turned back on by the override signal before the voltage has dropped, the loop has a time limit which, when exceeded, causes the controller to jump to the beginning of the program and start again. If the override feature is not used there is no need to test the timer seconds latch nor to test for the override signal. Without the override, the controller can only be turned on by the COP498 if the time out period has elapsed. Note also that the timer features continue to operate regardless of the state of the override signal. The override signal, when high, merely forces the $\overline{ON}$ pin to go low. The operation of the rest of the chip is in no way affected by the override signal.

General Code for Software Interface

The code in Figure 9a is recommended for interfacing the device to any COPS controller other than COP410L/COP411L. The code in Figure 9b is the recommended interface code for COP410L/COP411L. The code is written as subroutines and the code uses one level of subroutine internally. It is apparent from the code that the software interface is somewhat different for the READ and WRITE instructions than for the rest of the instructions. The routine labelled SETUP is assumed to be in page 2 of the ROM. The rest of the code may be located anywhere in program memory subject to the usual programming rules of COPS microcontrollers. The lower four bits of the instruction opcode are assumed to be located in RAM location COMAND, which is chosen as location 3,15. Data I/O uses register 2. The controller-COP498/499 interface is assumed to be as in Figure 6 or Figure 7. It is assumed that the SIO register in the COPS controller is enabled as serial I/O prior to entry to these routines.

```
WRITE:   JSRP   SETUP
RW:      LD
         XAS             ; READ/WRITE DATA
         XIS
         JP     RW
         OBD             ; DISABLE THE COP498/499 (B = 0)
         JP     FINISH
READ:    JSRP   SETUP
         NOP             ; NEED A TOTAL OF 5 SK CLOCK DELAYS (5 NOP'S)
         NOP             ; UNTIL DATA OUT IS VALID AT SIO REGISTER
         NOP
         NOP
         NOP
         JP     RW
INSTRT:  JSRP   SETUP    ; ROUTINE FOR THE REST OF THE INSTRUCTIONS
         NOP
         NOP             ; DELAYS TO INSURE PROPER TIMING
FINISH:  CLRA
         RC
         OBD             ; DESELECT THE COP498/499 (B = 0)
         XAS             ; TURN OFF THE CLOCK
         RET
         . PAGE 2
SETUP:   LBI    COMAND   ; POINT TO LOCATION WHERE COMMAND STORED
         CLRA
         SC
         XAS             ; TURN ON SK CLOCK
         OBD             ; ENABLE THE COP498/499 (B = 15)
         CLRA
         XAS             ; MAKE SURE NO INVALID DATA SENT
         CLRA
         AISC   1        ; SET UP START BIT
         SC
         XAS             ; SEND START BIT MSD OF INSTRUCTION
         LD              ; FETCH COMMAND TO A
         NOP
         NOP             ; MAINTAIN PROPER TIMING
         XAS             ; SEND COMMAND
         LBI    2,0      ; POINT TO READ/WRITE REGISTER
         RET             ; RETURN TO MAIN ROUTINE
```

Figure 9a. Software Interface to COP498/COP499 for COPS™ Controllers Other Than COP410L/COP411L

```
WRITE:  JSRP   SETUP
RW1:    XAS                  ; SEND COMMAND
RW2:    LD
        XDS                  ; POSITION Bd PROPERLY
RW:     LD
        XAS
        XIS
        JP     RW
        OBD                  ; DISABLE THE COP498/499 (B = 0)
        JP     FINISH
READ:   JSRP   SETUP
        XAS                  ; SEND READ COMMAND
        NOP                  ; DELAY FOR DATA VALID
        NOP
        NOP
        NOP
        NOP
        JP     RW2
INSTRT: JSRP   SETUP         ; ROUTINE FOR REST OF INSTRUCTIONS
        XAS                  ; SEND INSTRUCTION
        NOP
        NOP
        NOP                  ; DELAY FOR INSTRUCTION ACCEPT
        NOP
FINISH: CLRA
        RC
        OBD                  ; DESELECT THE COP498/499
        XAS                  ; TURN OFF THE CLOCK
        RET
        . PAGE 2
SETUP:  LBI    COMAND
        CLRA
        SC
        XAS                  ; TURN ON SK CLOCK
        OBD                  ENABLE THE COP498/COP499 (B = 15)
        CLRA
        XAS                  ; MAKE SURE NO INVALID DATA SENT
        CLRA
        AISC   1
        SC
        XAS                  ; SEND START BIT-MSD OF INSTRUCTION
        LD                   ; FETCH INSTRUCTION
        LBI    2,9
        RET
```

Figure 9b. COP410L/COP411L Software Interface to COP498/COP499

The code in Figure 9a will read or write 64 bits at a time. Note that in the COP410L/411L the code in Figure 9b will read or write 32 bits at a time. The code of Figure 10 is recommended if the user wishes to work in blocks of 64 bits with the COP410L/411L. Only the code which is different from that shown in Figure 9b is shown in Figure 10.

The routine in Figure 10 will read/write into registers 2 and 1 in the COP410L/411L. Figure 10 illustrates the preferred method of achieving full utilization of the device memory when the COP410L/411L is the controller. Remember that all the other routines are as shown in Figure 9B. Figure 10 illustrates only that code that must be changed to achieve full usage of the device memory when using the COP410L/411L.

General Notes

1. For complete safety in all cases it is recommended that the SK clock be turned off after the device has been deselected since the device is dynamic when it is enabled. If the clock is turned off while the device is selected, special care must be given to the SK timing characteristics. In no case should the clock be turned off while the device is selected if the SK period is greater than about 50μs.
2. The device does not become dynamic until both CS and CE are high and at least one high level is seen at the SK input. Thus the device may be safely enabled prior to turning on the clock as long as SK is low when the device is enabled.

```
WRITE: JSRP   SETUP     ; INITIALIZE, SEE FIGURE 9B
RW1:   XAS              ; SEND COMMAND
RW2:   LD               ; POSITION Bd
       XDS
RW:    LD
       XAS
       X      3         ; USE REGISTERS 2 AND 1
       LD
       NOP
       XAS
       XIS    3
       JP     RW
       OBD              ; DESELECT THE COP498/499
       JP     FINISH
```

Figure 10. COP410L/411L-COP498/499 Special Routine

3. The device must be deselected between instructions. Failure to do so will yield improper operation. The device relies on the select lines changing state in order to clear internal registers. Only one of the select lines on the COP498 needs to go low between instructions.
4. The user must insure that a WREN (write enable) instruction has been performed in order to write to the device memory. The WREN command need be given only once unless the SLEEP feature is used. If $\overline{ON}$ goes high as a result of a SLEEP command, a write disable is automatically performed in order to provide maximum protection to the device memory while the COPS™ controller is powering up and powering down. As long as $\overline{ON}$ remains high, WRITE and WREN instructions are disabled. Thus when the COPS controller wakes up after previously issuing a SLEEP command, a WREN instruction is required before data can be written to the device.
5. The six bit section of the RAM address register will increment whenever there are clock pulses present when the CS and CE pins are high. Thus the user can position the RAM address register if he wishes by selecting the device, holding the DI pin low and supplying the appropriate number of clocks. Then, without deselecting the device, the user would send the instruction and read or write data. Although possible, this technique is not recommended as it is fairly involved.
6. When using the TSEC command in COP498 with the code as given in Figure 9, the master program should test for the accumulator greater than 1 to determine if the timer seconds latch was set. Note again, test for greater than 1; do not test for greater than zero.

Note on MICROWIRE™ Interface

If the device is connected to a MICROWIRE interface containing other circuits whose DO (data output) pins may produce a signal swing higher than V_{CC} of the device, some protection is needed on the DO pin of the device. This happens when the DO pins of several peripherals powered by different voltages are connected together; e.g. a COP453 at 9.5V with a COP498 at 5.5V, or a COP452 at 4.5V with a COP499 at 2.4V. When the DO pin of COP498/499 is externally driven above its power supply voltage, a current will flow into it and this current must be limited to 1 mA. As an example, we have two COP453's with a COP420L operating at 9.5V and a COP498 operating at 4.5V. When enabled, the DO pin of a COP453 may swing higher than 4.5V, the power supply voltage of the COP498. One way to limit the current is to use a current limiting resistor of 5.6 kΩ between the DO pins of the COP453 and the COP498. NOTE: the SI pin of the COPS processor MUST BE A Hi-Z INPUT. Two configurations are possible as shown in Figure 11. Note that the resistor between DO and SI will give extra RC delay to the signal going from the DO pin to the SI pin of the COPS processor. Connection B is preferred because the DO signal from COP498 has nearly a whole SK cycle to become valid at SI input before the signal is read by the processor. When a ROMless COPS processor (COP401L/-COP402/COP404L) is used for emulation, the circuit shown in Figure 12 may be used to simulate a Hi-Z input for the SI pin.

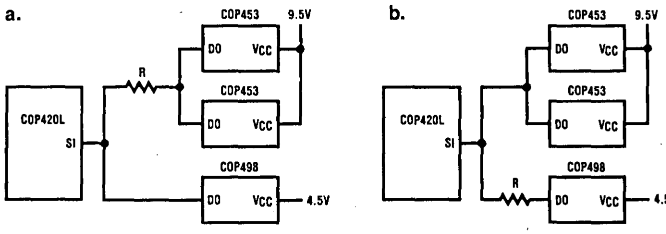


Figure 11. High Voltage Protection on DO Pin

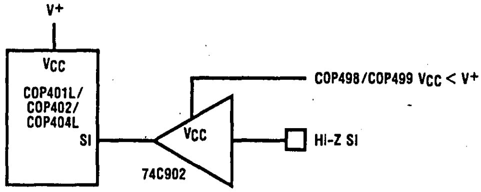


Figure 12. Simulating HI-Z SI Input on ROMless Processors

Section 12

8-Bit Microprocessors

12

Introduction

Combining CMOS processes with microprocessors provides today's systems designers with a number of important benefits. The most significant of these is the low power consumption inherent in microCMOS technology.

National has designed a CMOS microprocessor, the NSC800™, a product family that combines the Z80® instruction set with the 8085 multiplexed bus.

THE NSC800: A COMPUTER SYSTEM FOR LESS THAN 5W

The internal architecture of the NSC800 is similar to that of the Z80, including the alternate register set, making it 100% code compatible with the Z80. The NSC800 is also CP/M® compatible. In addition, the use of a multiplexed bus allows the NSC800 to implement extra functions that are not found on the Z80, including:

- five interrupts (for faster response),
- two special status lines (to ease decoding),
- an on-board clock generator,
- a power-save feature,
- and a single-step pin.

Program compatibility exists because the NSC800 executes the 158 instructions of the Z80. In addition, with the many programs that are now commercially available, you can be up and running in the minimum amount of time with some of the most powerful and comprehensive software on the market.

With the Z80 architecture implemented in the NSC800, there are 10 addressing modes and 22 programmable registers available. You can directly address 64k bytes of memory and 256 I/O locations. In addition, the efficient multiplexed bus structure of the NSC800 allows many extra functions to be provided by the CPU.

A minimum system can be assembled from three chips: the NSC800 CPU, the NSC810 RAM-I/O Timer, and the NSC830 ROM-I/O. This provides 2,048 bytes of mask-programmable ROM, 128 bytes of static RAM, 42 I/O lines, two 16-bit timers, and five levels of interrupts. All of these products, and even a special NSC831 I/O chip, are offered in three clock speeds: 1 MHz, 2.5 MHz, and 4 MHz. A CMOS real-time clock chip (the MM58167A) is also available that uses an on-board 32.768 kHz crystal-controlled oscillator circuit and can be operated in a low power drain battery-backup application where only 4 μA are taken from a 2.5V power supply.

In addition to the peripherals shown in *Figure 12-1*, more peripherals are being designed for the NSC800, such as the NSC858 (a CMOS UART).

All the devices needed for an NSC800-based system are available from National Semiconductor. A wide variety of A/D and D/A converters, peripheral controllers and memory components (including RAMs and EPROMs) are offered. For example, the ADC0801 A/D converter features accuracy as good as ± 1/4 LSB, eliminates the need for external zero and full-scale adjustments and is designed to provide a direct interface to the NSC800. CMOS μP-compatible D/A converters are also available in 8-bit, 10-bit and 12-bit resolutions to fit a wide variety of applications.

To make it easier to "check out" the NSC800, an evaluation PC board is also available. This NSC888 Evaluation Board is a complete single-board computer system that includes the NSC800 CPU, the NSC810 RAM-I/O timers, a monitor in an EPROM, additional RAM and interface circuitry and software for terminal communications (via RS232).

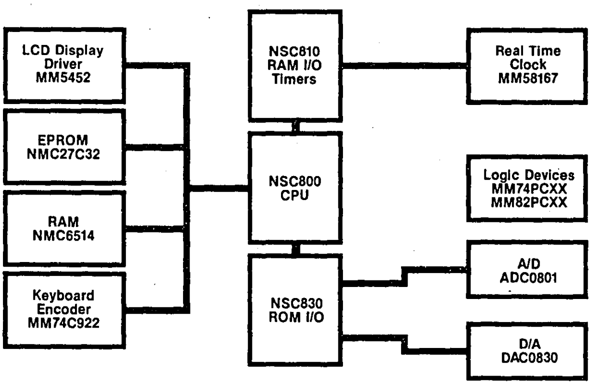


FIGURE 12-1. The NSC800 Family with a Broad Line of Low Power Peripheral Components

National Semiconductor

PRELIMINARY

microCMOS

MA2000 Base Plane and Power Supply Module

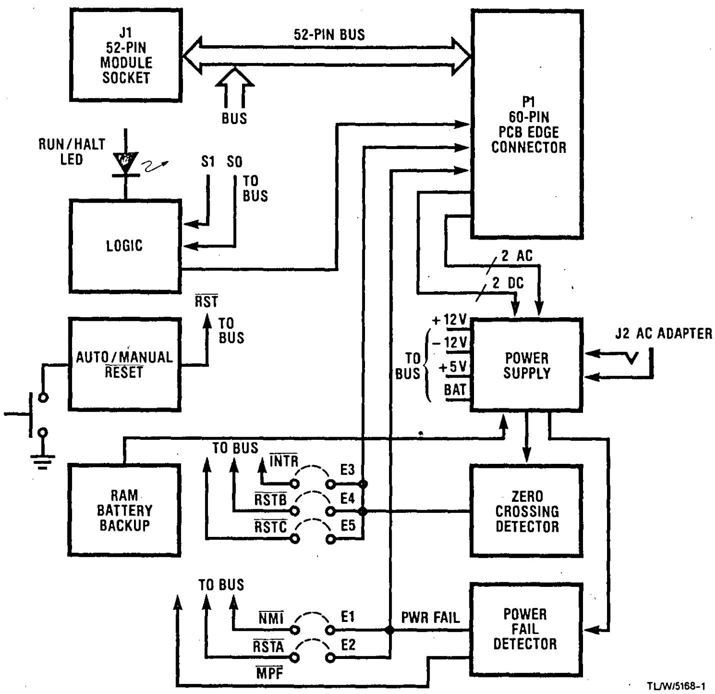
General Description

The MA2000 module provides a base and power supply subsystem for National Semiconductor's Modular Macrocomponent™ family. The base plane provides power conversion from a low voltage AC or DC input to the regulated +5V, +12V and −12V supplies used by the MA2000 series modules. A reset pushbutton is provided along with a MA2800 LED status indicator. The base plane provides for a battery back-up system as well as power-fail output logic. Zero crossing output logic is also included. The base plane includes a 52-pin socket for the MA2000 series modules and a 60-pin edge connector for user access to the bus and other functions.

Features

- Operates off wide range of AC or DC input power
- Internal or external RAM battery backup system
- Power-fail output logic
- Zero crossing output logic (AC input only)
- System operating status LED indicator
- Manual reset switch
- 60-pin I/O connector for user access to bus and other functions
- 52-pin socket for MA2000 series macrocomponents

Block Diagram



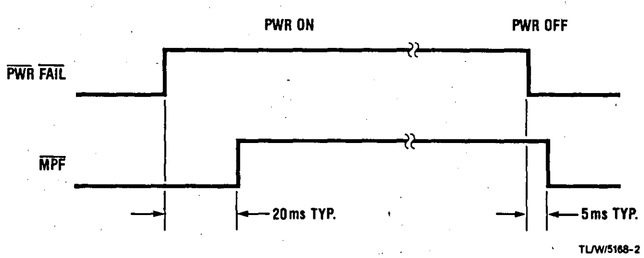
TL/W/5168-1

Absolute Maximum Ratings

Ambient Operating Temperature	−40° to +85°C
Storage Temperature	−55°C to +100°C

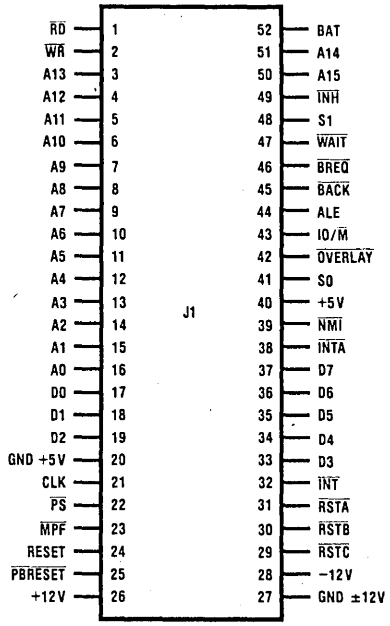
Electrical Characteristics
Unless otherwise stated, T_A+25°C, V_{IN} = +9.0V to +18.0V_{DC}

Parameter		Conditions	Min	Typ	Max	Units
Power Supply Section		DC Load				
	AC Inputs	+5V, = 250mA +12V, = 40mA +12V, = 40mA	8.0 47		14.0 440	V_{RMS} Hz
	DC Input		9.0		18.0	V
	V_{OUT}+12V	I_O = 0 to 80 mA	11.4		12.6	V
	V_{OUT}−12V	−I_O = 0 to 80 mA	−11.4		−12.6	V
	V_{OUT}+5V	I_O = 0 to 500 mA	4.75		5.25	V
	$V_{RIPPLE\ RMS}$ + and −12V	I_O = ±80mA		50		mV_{RMS}
	$V_{RIPPLE\ RMS}$ +5V	I_O = 500 mA		25		mV_{RMS}
	+5V Overhead After Power Fail Flag	+5V, I_O = 250mA +12V, I_O = 40mA −12V, I_O = 40mA		10		ms
Zero Crossing Detector		AC Input, f_{IN} = 50 or 60 Hz, phase referenced to actual AC input zero crossing (i.e., transformer secondary). AC input = 8.0 to 14.0 V_{RMS}.				
	θ Angle			±3		Degree
	V_{OL} CMOS to CMOS	V_{CC} = 5v, I_O = 10μa			0.5	V
	V_{OH} CMOS to CMOS	V_{CC} = 5v, I_Oμa	4.5			V
	P_W			40		μs
Power Failure Detector						
	V_{TH}	Threshold Voltage of V_{IN}		8.5		V
	V_{OL}	I_{SINK} ≤ 2mA, V_{IN} ≤ V_{TH}			0.4	V
	V_{OH}	I_{SOURCE} ≤ 5μA, V_{IN} ≥ T_{TH}	4.0			V
System Status Output/Indicator		LED Off = Off Flashing = Running Continuous = Halt		10		Hz
	Output V_{OL}	I_{SINK} ≤ 50mA			0.4	V
	V_{OH}	I_{SOURCE} ≤ 10μA	3.5			V



Power On/Off Timing

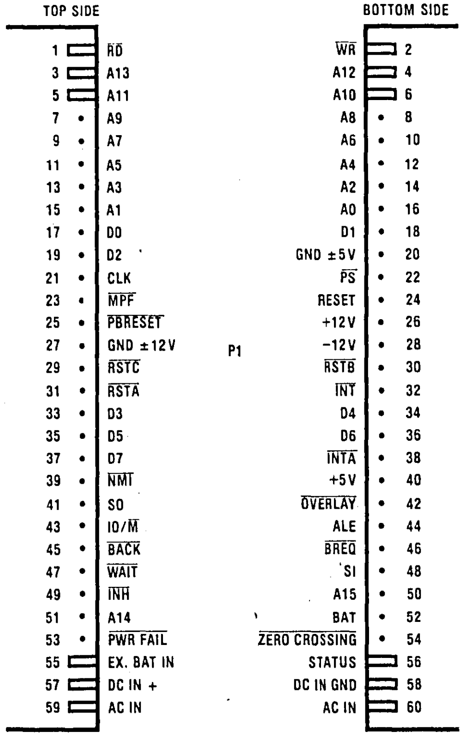
System Socket Pin Identification



TL/W/5168-3

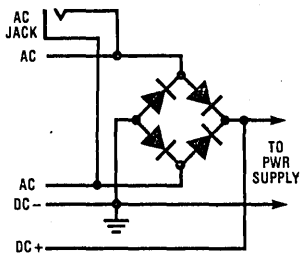
See the MA2800 data sheet for a functional description of the pins.

Edge Connector Identification



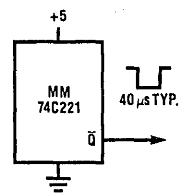
TL/W/5168-4

Input/Output Configurations



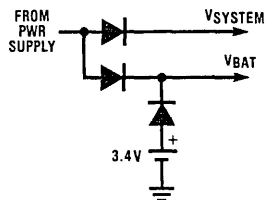
TL/W/5168-5

PWR Input



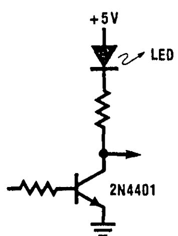
TL/W/5168-6

Zero Crossing Output



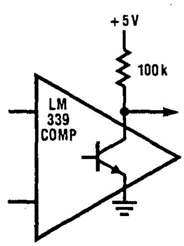
TL/W/5168-7

RAM Backup



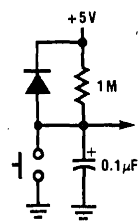
TL/W/5168-8

System Status Indicator



TL/W/5168-9

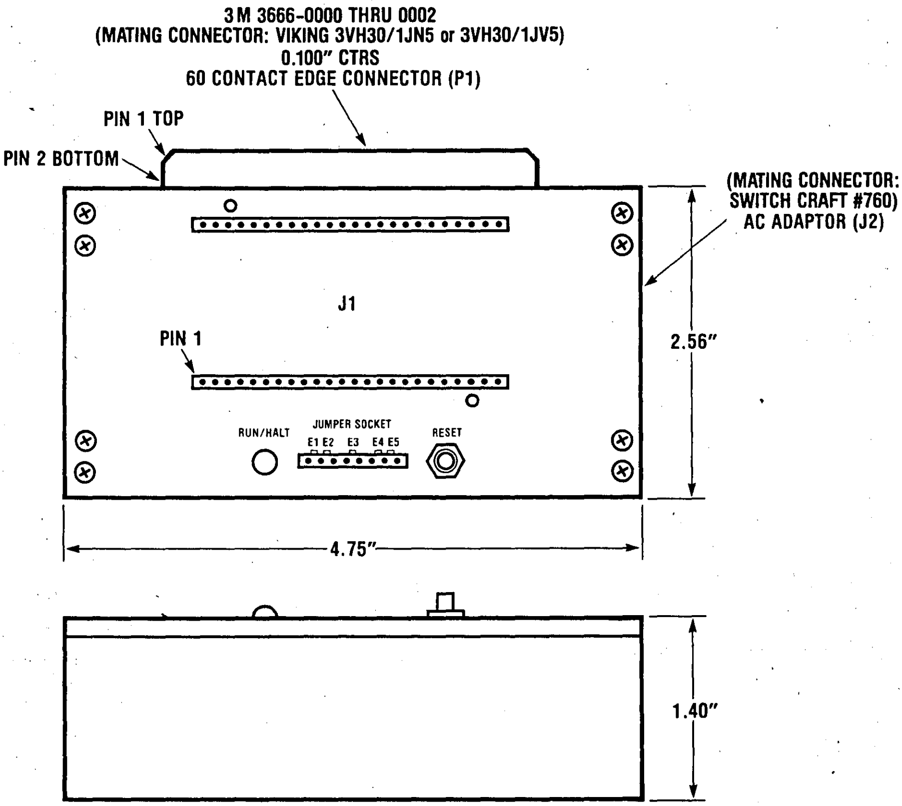
Power Fail and $\overline{MPF}$



TL/W/5168-10

Reset System

Mechanical



NS Package MA2000

National Semiconductor

PRELIMINARY

microCMOS

MA2016 16,384 × 8-Bit CMOS Static RAM Module

General Description

The MA2016 consists of eight 2k × 8-bit CMOS RAMs along with an address decoder capable of decoding up to a 128k × 8-bit low power CMOS RAM. It operates on a single 5V power supply and is able to retain data down to 2V. The MA2016 does not require a refresh and all inputs and outputs are TTL compatible. Multiple MA2016 modules may be stacked in a piggyback fashion or laid out in any manner desired. The low power requirements and versatile layout make the MA2016 very useful for low power hand-held battery powered applications.

Applications

- Portable terminals
- Hand-held devices
- Pos terminals
- Remote instrumentation
- Process controllers
- Microcomputer memory

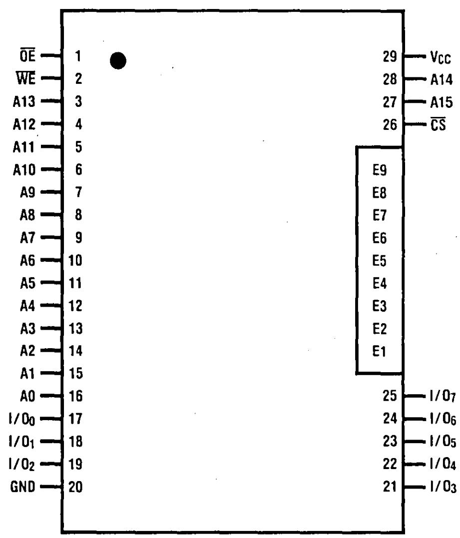
Features

- 16k × 8-bits fully decoded
- Outputs directly TTL compatible
- Low power—typical 400 mW
- 250 ns access time
- Static operation—no clocks or refreshing required
- Single 5V supply ± 10%
- 2V minimum for data retention
- TRI-STATE® outputs for bus operation
- Common data I/O pins
- Separate OE pin
- Internal power supply decoupling

Ordering Information

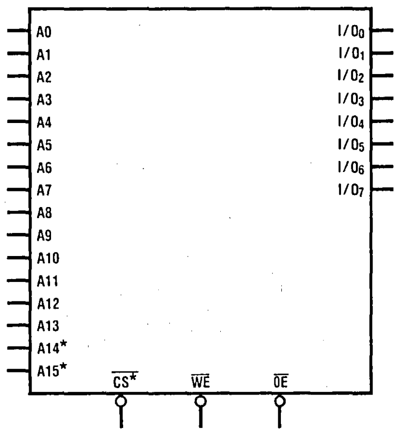
MA2016

Connection Diagram



TOP VIEW

Logic Symbol



* active state user selectable

Pin Names

$\overline{CS}$	Chip Select Input (user programmable)
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_0–I/O_7	Data Inputs/Outputs
A0–A15	Address Inputs (A14, A15 Block Select, user programmable)
V_{CC}	Power (typical 5V)
GND	Ground

Truth Table

$\overline{CS}$*	$\overline{WE}$	$\overline{OE}$	I/O	Mode
H	X	X	Hi-Z	Standby
L	H	L	D_{OUT}	Read
L	H	H	Hi-Z	Read
L	L	X	D_{IN}	Write

* $\overline{CS}$ state is user selectable. Table shown with jumper E7 to E8 and E4 to E5 installed.

Absolute Maximum Ratings

Voltage at Any Pin with Respect to GND	−0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

AC Test Conditions

Input Pulse Levels:	0.8V to 2.4V
Input Rise and Fall Times:	10 ns
Input and Output Timing Reference Levels:	1.5V
Output Load:	1 TTL gate and $C_L = 100$ pF (including scope and fixturing)

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V, $T_A = 0°C$ to 70°C unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\lvert I_{LI} \rvert$	Input Leakage Current A0–A10, $\overline{OE}$, $\overline{WE}$	$V_{IN} = 0V$ to V_{CC}			20	μA
$\lvert I_{LI} \rvert$	Input Leakage Current A11–A15, $\overline{CS}$	$V_{IN} = 0V$ to V_{CC}			5	μA
$\lvert I_{LO} \rvert$	Output Leakage Current	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = 0V$ to V_{CC}			20	μA
I_{CCOP}	Operating Power Supply Current	$\overline{CS} = V_{IL}$, $I_{I/O} = 0$ mA		55 (Note 1)		mA
I_{CCSB}	Standby Power Supply Current	$\overline{CS} = V_{IH}$		32 (Note 1)		mA
I_{CCDR}	Standby Power Supply Current Data Retention	$V_{CC} = 2.0V$, $\overline{CS} = V_{CC}$ $V_{IN} = 0V$ or V_{CC}		35 (Note 1)		μA
V_{DR}	Data Retention Voltage	$\overline{CS} = V_{CC}$, $V_{IN} = 0V$ or V_{CC}	2			V
V_{OL}	Output Voltage Low	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output Voltage High	$I_{OH} = -1.0$ mA	2.4			V
V_{IL}	Input Voltage Low		−0.3		0.8	V
V_{IH}	Input Voltage High		$V_{CC} - 2.0$		$V_{CC} + 0.3$	V

Capacitance (Note 2) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance I/O_0–I/O_7	$V_{I/O} = 0V$		70		pF
C_{IN}	Input Capacitance A0–A10, $\overline{WE}$, $\overline{OE}$	$V_{IN} = 0V$		55		pF
C_{IN}	Input Capacitance A11–A15, $\overline{CS}$			20		pF

Note 1: $V_{CC} = 5V$, $T_A = 25°C$

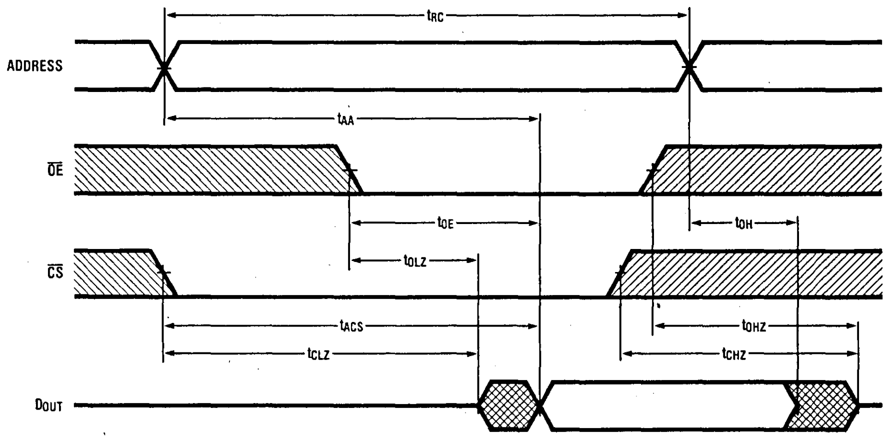
Note 2: This parameter is sampled and not 100% tested.

AC Characteristics-Read Cycle ($V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$)

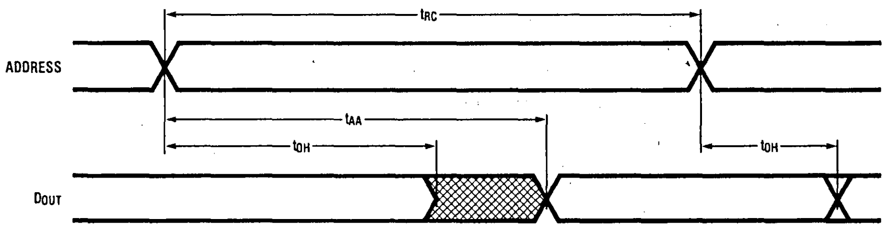
Symbol	Parameter	Min	Typ	Max	Units
t_{RC}	Read Cycle Time	200			ns
t_{AA}	Address Access Time			200	ns
t_{ACS}	Chip Select Access Time			200	ns
t_{CLZ}	Chip Selection to Output in Low Z	65			ns
t_{OE}	Output Enable to Output Valid			150	ns
t_{OLZ}	Output Enable to Output in Low Z	65			ns
t_{CHZ}	Chip Selection to Output in Hi-Z			100	ns
t_{OHZ}	Output Disable to Output in Hi-Z			100	ns
t_{OH}	Output Hold from Address Change	65			ns

Timing Waveforms

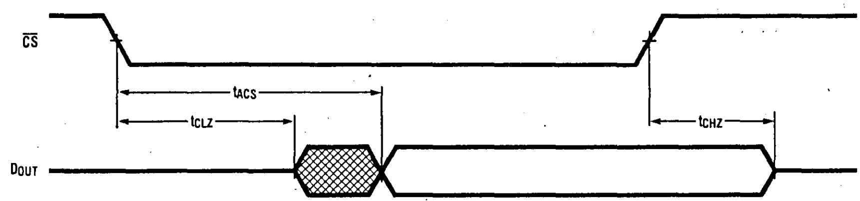
Read Cycle [1] (Notes 1 and 5)



Read Cycle [2] (Notes 1, 2, 4 and 5)



Read Cycle [3] (Notes 1, 3, 4 and 5)



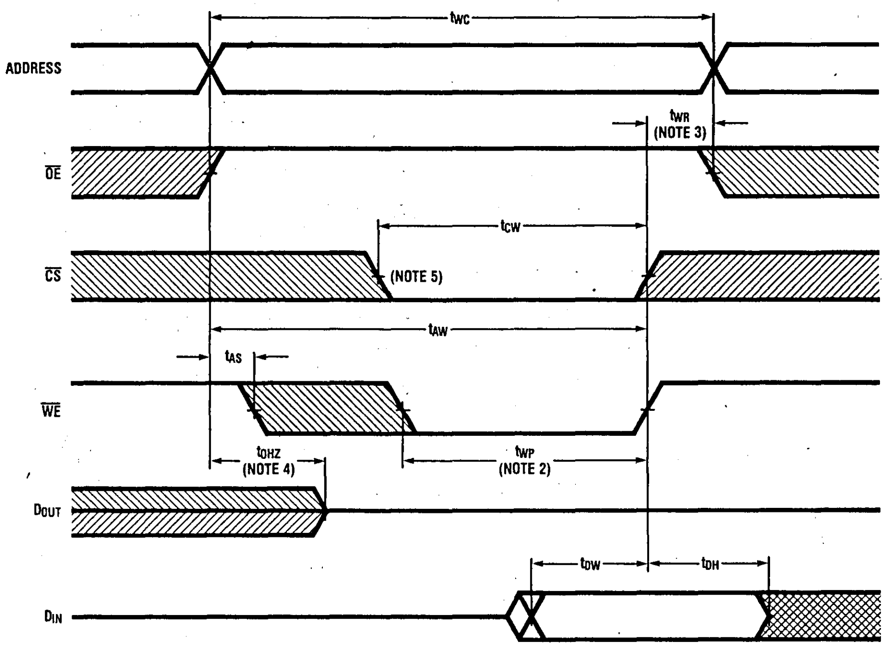
Note 1: $\overline{WE}$ is high for read cycle.
Note 2: Device is continuously selected, $\overline{CS} = V_{IL}$.
Note 3: Address valid prior to or coincident with $\overline{CS}$ transition low.
Note 4: $\overline{OE} = V_{IL}$.
Note 5: When $\overline{CS}$ is low, the address input must not be in the high impedance state.

AC Characteristics-Write Cycle ($V_{CC}=5V \pm 10\%$, $T_A=0°C$ to $70°C$)

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time	200			ns
t_{CW}	Chip Selection to End of Write	140			ns
t_{AW}	Address Valid to End of Write	160			ns
t_{AS}	Address Set-Up Time	70			ns
t_{WP}	Write Pulse Width	140			ns
t_{WR}	Write Recovery Time	60			ns
t_{OHZ}	Output Disable to Output in Hi-Z			100	ns
t_{WHZ}	Write to Output in Hi-Z			110	ns
t_{DW}	Data to Write Time Overlap	100			ns
t_{DH}	Data Hold from Write Time	60			ns
t_{OW}	Output Active from End of Write	60			ns

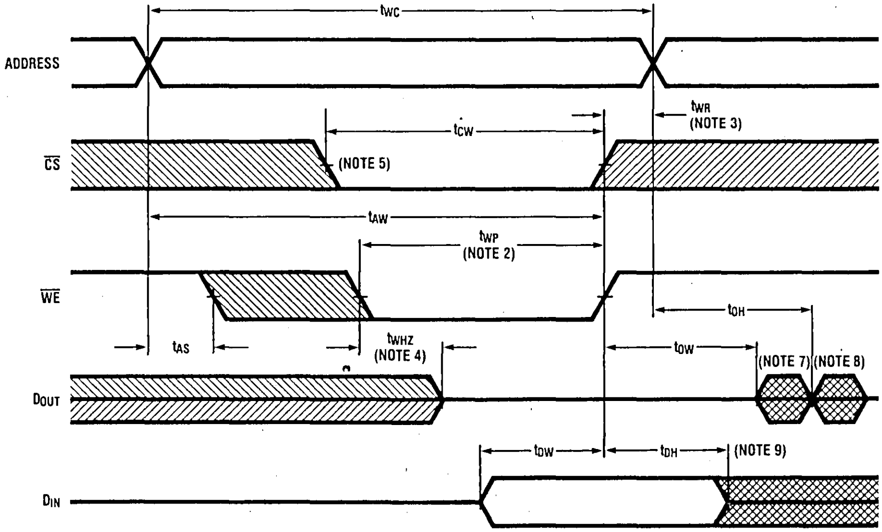
Timing Waveforms (Continued)

Write Cycle [1] (Note 1)



Timing Waveforms (Continued)

Write Cycle [2] (Notes 1 and 6)

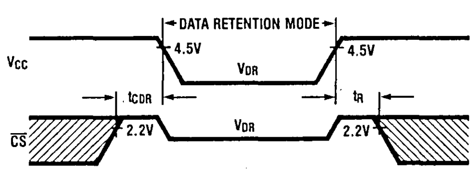


Note 1: $\overline{WE}$ must be high during all address transitions.
Note 2: A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
Note 3: t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
Note 4: During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
Note 5: If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
Note 6: $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$.)
Note 7: D_{OUT} is the the same phase of write data of this write cycle.
Note 8: D_{OUT} is the read data of next address.
Note 9: If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

Low V_{CC} Data Retention Characteristics ($T_A = 0°C$ to $70°C$)

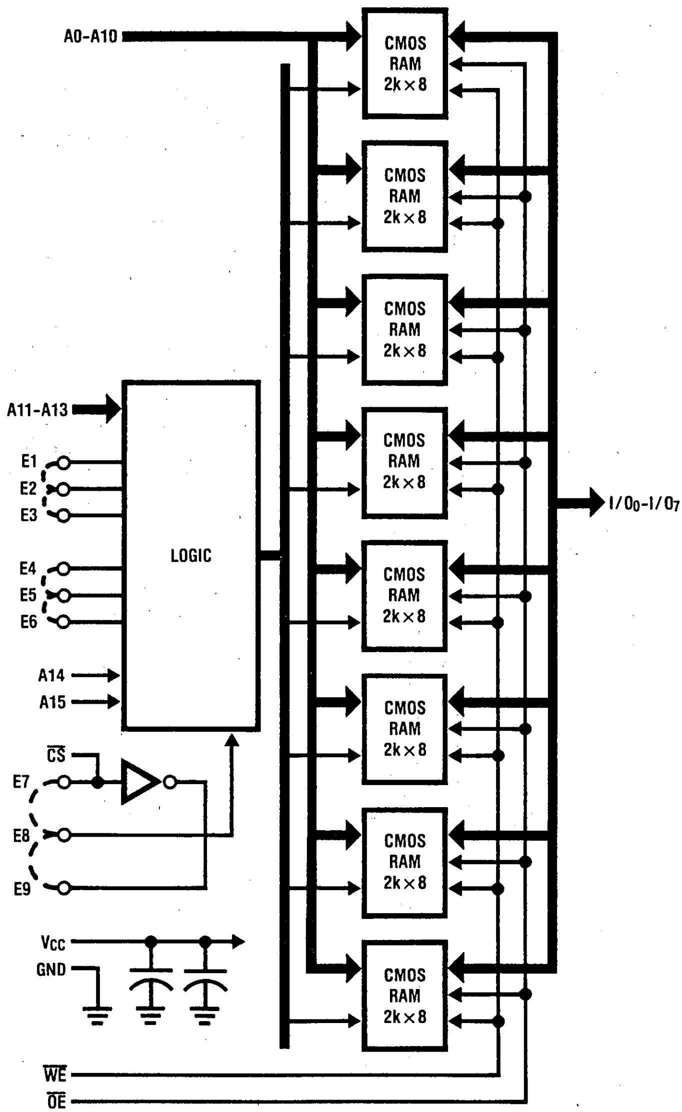
Symbol	Parameter	Min	Typ	Max	Units
t_{CDR}	Chip Deselect to Data Retention Time	0			ns
t_R	Operation Recovery Time	200			ns

Low V_{CC} Data Retention Waveform



12

Block Diagram



Memory Expansion

BLOCK ADDRESS DEDICATION

The user must assign 16k block address boundaries by installing provided jumpers for each module. A summary of jumper connections for contiguous address boundaries from 0k–128k are shown in Table I.

The modules may be stacked up (8 max) or layed out horizontally in any order or combination to fit system profile constraints *(Figure 1)*.

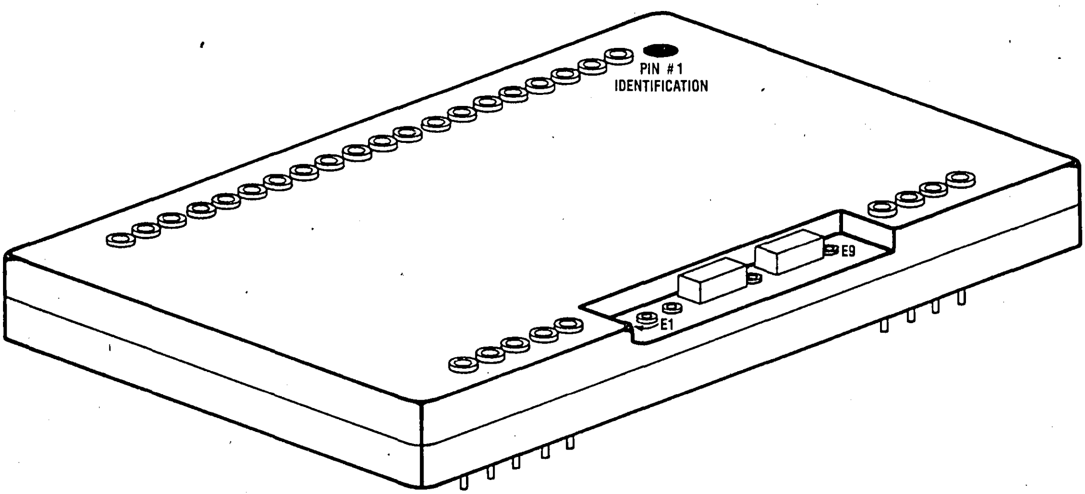
The low voltage data retention feature is usable to a max of four modules when stacked vertically.

Memory Expansion (Continued)

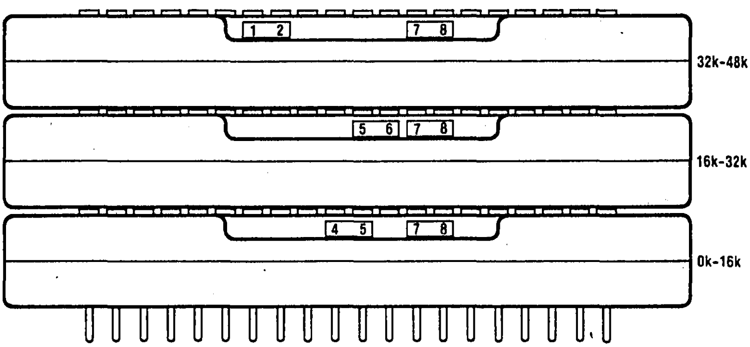
TABLE I

MA2016 #	$\overline{OE}$	$\overline{CS}$	Jumpers* E9	E8	E7	E6	E5	E4	E3	E2	E1	I/O	Address Boundary (Hex)	
1	L	L		●	●		●	●				0k–16k	0000_{16}	$3FFF_{16}$
2	L	L		●	●	●	●					16k–32k	4000_{16}	$7FFF_{16}$
3	L	L		●	●					●	●	32k–48k	8000_{16}	$BFFF_{16}$
4	L	L		●	●				●	●		48k–64k	$C000_{16}$	$FFFF_{16}$
5	L	H	●	●			●	●				64k–80k	10000_{16}	$13FFF_{16}$
6	L	H	●	●		●	●					80k–96k	14000_{16}	$17FFF_{16}$
7	L	H	●	●						●	●	96k–112k	18000_{16}	$1BFFF_{16}$
8	L	H	●	●					●	●		112k–128k	$1C000_{16}$	$1FFFF_{16}$
	H	X	X									TRI-STATE		

H = high = logic "1"
L = low = logic "0"
X = don't care
TRI-STATE = HI-Z
* Any configuration must have 2 jumpers per module.



a. 16k Configuration



b. 48k Configuration

FIGURE 1

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MA2732 8k-Byte CMOS UVPROM/RAM Module

General Description

The MA2732 8k-byte CMOS UVPROM module is a member of the MA2000 series family. It provides a standard modular macrocomponent package and bus interconnect facility for industry-standard 27C16 or 27C32 UVPROMs. The module provides two standard sockets for the packaged parts. The UVPROMs are selected and programmed by the user and then simply inserted into the sockets provided in the MA2732 module. The MA2732 can be configured by the user in PROM capacities of 2k-bytes, 4k-bytes or 8k-bytes at the user's option. The MA2732 is designed such that if the user needs only one of the two sockets for program memory the remaining socket can be populated with a 2k × 8 CMOS RAM to obtain additional data memory. The internal macrobus provides for simple integration of the MA2732 with other members of the MA2000 family. Key features of this module include a complete UVPROM subsystem, self-contained memory map selection logic, opcode, decode and wait-state generator, and output buffered single 5V operation.

Features

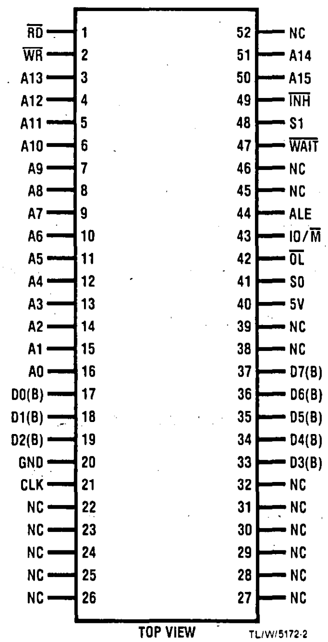
- Complete UVPROM subsystem
- Configurable as either 2k, 4k or 8k-bytes of ROM or 2/4k ROM and 2k RAM
- User selectable jumpers for memory mapping
- Internal user selectable wait-state generator
- Buffered data outputs
- Low power—when using two NMC27C32 EPROMs for a full 8k-bytes
- Sockets will accept any of the popular 24-pin ROMs/RAMs
- When the module is not selected it is automatically placed in standby mode (10 mW max using two NMC27C32s)
- Single 5V operation
- Unique stackable module

Applications

- Portable terminals
- Hand-held devices
- Pos terminals
- Remote instrumentation
- Process controllers
- Microcomputer memory

Connection Diagram

Dual-In-Line Package



NC = no connection

TOP VIEW

TL/W/5172-2

Pin Names

$\overline{RD}$	Read strobe input
A0–A15	Address inputs
D0–D7	Data outputs (buffered)
CLK	Clock input
S0–S1	Status inputs
$\overline{OL}$	Overlay input
IO/$\overline{M}$	Input/output memory input
ALE	Address latch enable input
$\overline{INH}$	Inhibit input
5V	Power supply input
GND	Digital GND
$\overline{WR}$	Write strobe input

Absolute Maximum Ratings

V_{CC} Supply Voltage	6.0V
Voltage at Any Pin Relative to GND	GND − 0.3V to V_{CC} + 0.3V
Ambient Operating Temperature	−40°C to +85°C
Storage Temperature	−55°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics T_A = +25°C, V_{CC} = 5V ± 10%, GND = 0 unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		3.5			V
I_{IN}	Input Leakage A11-A15, $\overline{INH}$, CLK, $\overline{RD}$, $\overline{WR}$	V_{IN} = 0 to V_{CC} (Note 1)	−100	1	100	μA
I_{IN}	Input Current (Internal Pull-Up Resistors) $\overline{OL}$, E1-E6, IO/$\overline{M}$	V_{IN} = 0.4V	100		25	μA
I_{IN}	Input Current (Internal Pull-Down Resistors) ALE, S1, S0	V_{IN} = 2.4V	25		100	μA
V_{OL}	Output Low Voltage D0-D7	I_O = 2.0 mA			0.4	V
V_{OH}	Output High Voltage D0-D7	I_O = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage $\overline{WAIT}$	I_O = 3.0 mA			0.4	V
V_{OH}	Output High Voltage $\overline{WAIT}$	I_O = −1.0 mA	2.4			V
I_{CC}	Supply Current	V_{IN} = V_{CC} Outputs Open			600 (Note 2)	μA

Control Timing Diagram

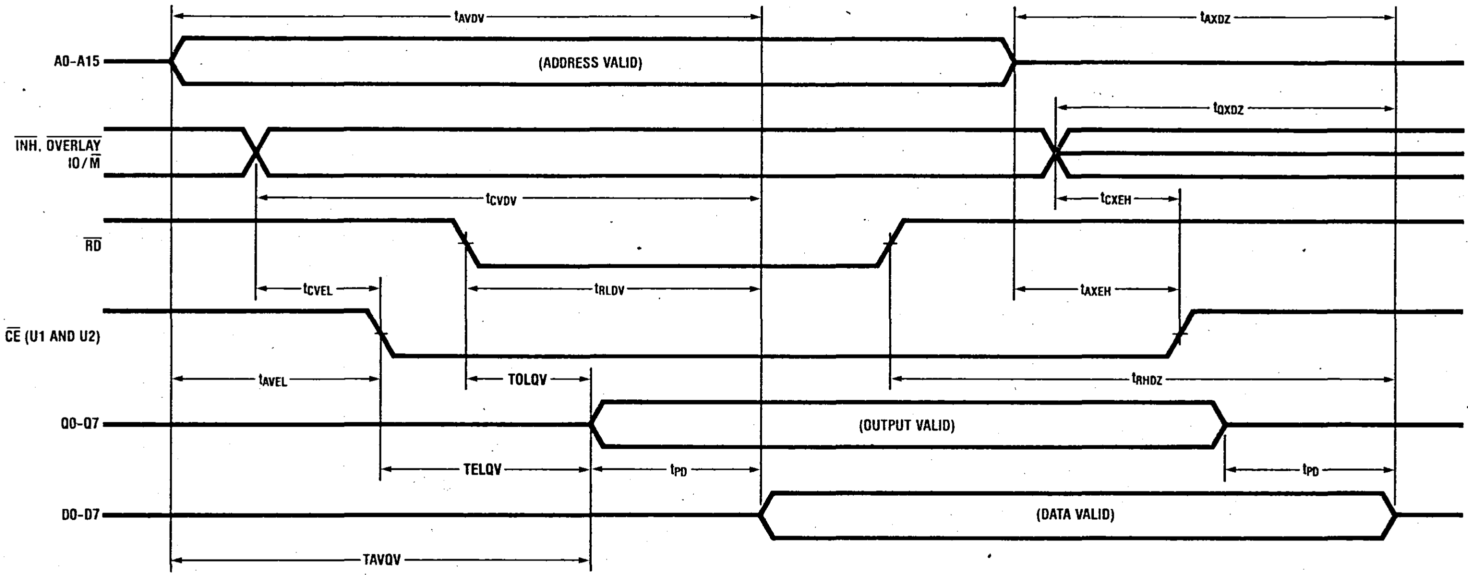
Symbol	Parameter	Conditions	Typ	Units
t_{AVDV}	Valid Address to Valid Data		105	ns
t_{AXDZ}	Address to Data Hi-Z		120	ns
t_{AVEL}	Valid Address to Chip Enable		25	ns
t_{AXEH}	Address to Chip Disable		35	ns
t_{CVDV}	Valid Control Lines to Valid Data	$\overline{INH}$ = E5; IO/$\overline{M}$ = V_{IL}; $\overline{OL}$ = V_{IH}	100	ns
t_{CXDZ}	Control Line to Data Hi-Z	$\overline{INH}$ = E5; IO/$\overline{M}$ = V_{IH}; $\overline{OL}$ = V_{IL}	115	ns
t_{CVEL}	Valid Control Lines to Chip Enable	Same as for t_{CVDV}	25	ns
t_{CXEH}	Control Line to Chip Disable	Same as for t_{CXDZ}	35	ns
t_{WLDV}	$\overline{WR}$ Low to Data Valid Data		125	ns
t_{WHDZ}	$\overline{WR}$ High to Data Hi-Z		75	ns
t_{RLDV}	$\overline{RD}$ Low to Data Valid		125	ns
t_{RHDZ}	$\overline{RD}$ High to Data Hi-Z		75	ns
t_{PD}	Propagation Delay		50	ns
FOR MA2800 INTERFACE ONLY				
TAVQV	Valid Address to Valid Output (Note 3)		≤450	ns
TELQV	Chip Enable to Valid Output (Note 3)		≤450	ns
TOLQV	Output Enable ($\overline{RD}$) to Valid Output (Note 3)		≤120	ns
TQVWH	Output Valid to $\overline{WR}$ High		≤400	ns
TQVEH	Output Valid to $\overline{CE}$ High		≤500	ns
TELEH	Enable Strobe Width		≤1	μs

Note 1: I_{IN} on A0-A10 depends on user selected ROM or RAM.

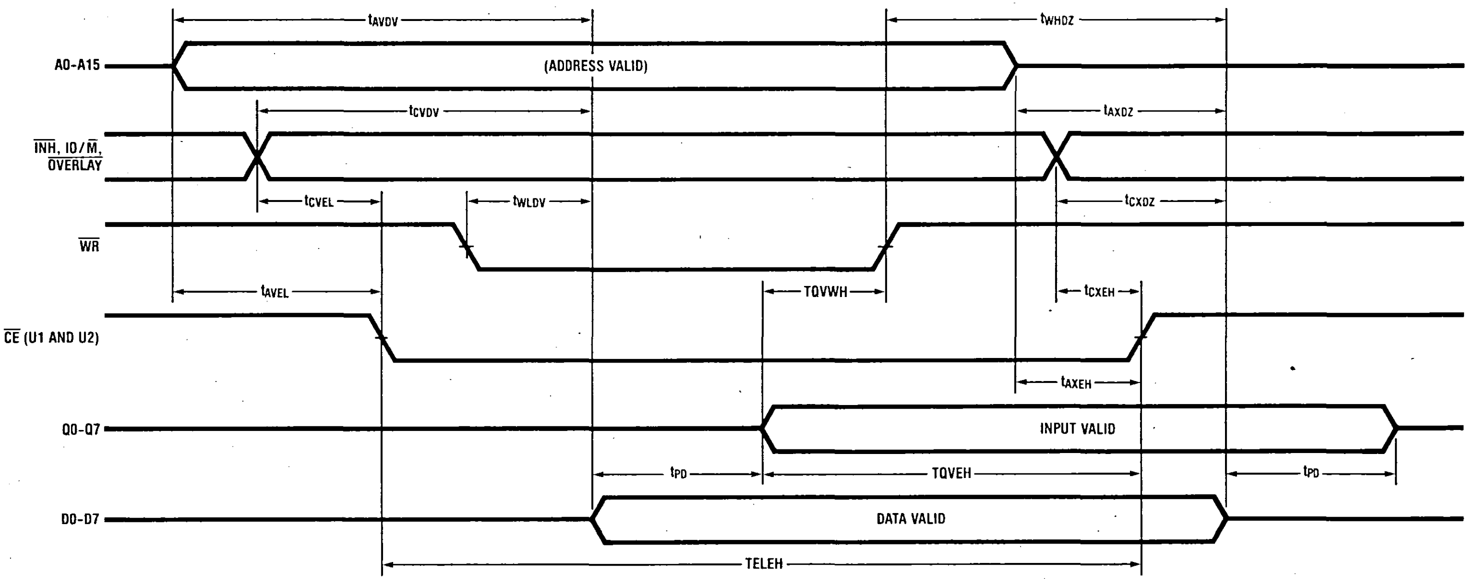
Note 2: This does not include user supplied ROM or RAM.

Note 3: During an opcode fetch these timing values can be increased by 400 ns through jumpering E7.

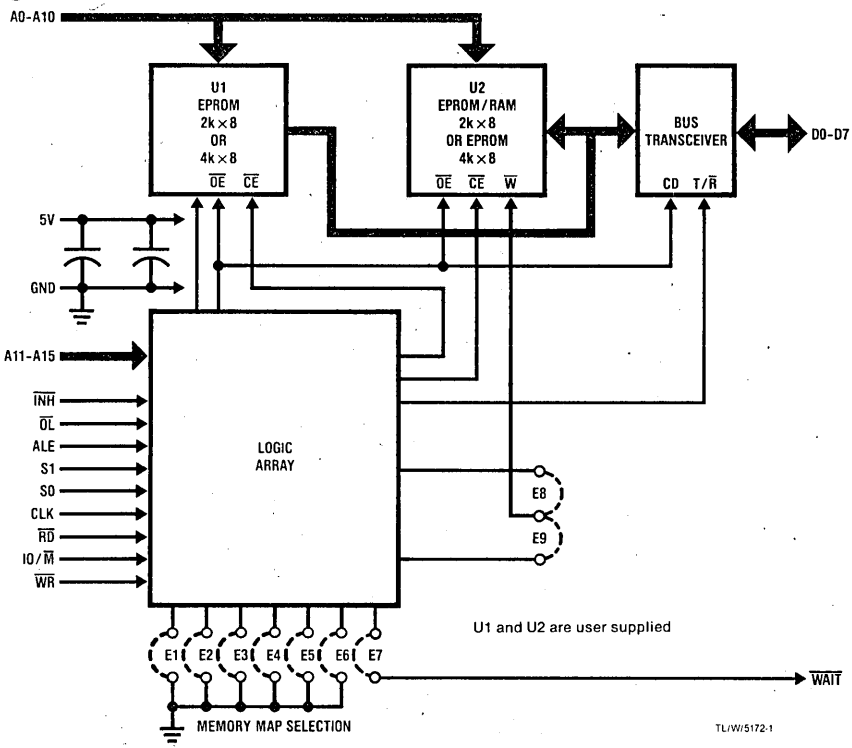
Typical Read Cycle



Typical Write Cycle



Block Diagram



MEMORY MAPPING

E1	E2	E3	E4	E6	Address	Boundary (HEX)	
•	•	•	•	•	0000	FFF	4k Blocks U1 = Lower 2k U2 = Higher 2k
•	•	•		•	1000	1FFF	
•	•		•	•	2000	2FFF	
•	•			•	3000	3FFF	
•		•	•	•	4000	4FFF	
•		•		•	5000	5FFF	
•			•	•	6000	6FFF	
•				•	7000	7FFF	
	•	•	•	•	8000	8FFF	
	•	•		•	9000	9FFF	
	•		•	•	A000	AFFF	
	•			•	B000	BFFF	
		•	•	•	C000	CFFF	
		•		•	D000	DFFF	
			•	•	E000	EFFF	
				•	F000	FFFF	
•	•	•	X		0000	1FFF	8k Blocks U1 = Lower 4k U2 = Higher 4k or 2k RAM
•	•		X		2000	3FFF	
•		•	X		4000	5FFF	
•			X		6000	7FFF	
	•	•	X		8000	9FFF	
	•		X		A000	BFFF	
		•	X		C000	DFFF	
			X		E000	FFFF	

X = don't care

E1 = A15 = logic "0" when jumper is installed (•)

E2 = A14 = logic "0" when jumper is installed (•)

E3 = A13 = logic "0" when jumper is installed (•)

E4 = A12 = logic "0" when jumper is installed (•)

E5 = $\overline{INH}$ = logic "0" when jumper is installed (•)

E6 = 4k block select = logic "0" when jumper is installed (•) otherwise 8k block

E7 = $\overline{WAIT}$ when jumper is installed (•) adds one wait state during opcode fetch only.

E8 = U2 is ROM when jumper is installed.

E9 = U2 is RAM when jumper is installed.

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PRELIMINARY

microCMOS

MA2800 8-Bit CMOS Microcomputer Module

General Description

The MA2800 is a low power, 8-bit CMOS microcomputer system. It provides a CPU, ROM, RAM, parallel and serial I/O ports, a system clock, programmable timers, priority interrupt logic, a software monitor program and 5 MHz operation—in a single 1.6 by 3.3 by 0.45 inch, 52-pin module.

The CPU module utilizes an NSC800™, which provides basic CPU functions, vectored priority interrupt, power-save feature, interrupt acknowledge and Z80 software compatibility.

The 4k ROM in the CPU module contains the resident monitor program which aids in developing software and manipulating I/O devices and memory bytes.

The CPU module also contains 2k of RAM. The resident monitor program uses the top 256 bytes for a scratchpad; the remaining space is user available.

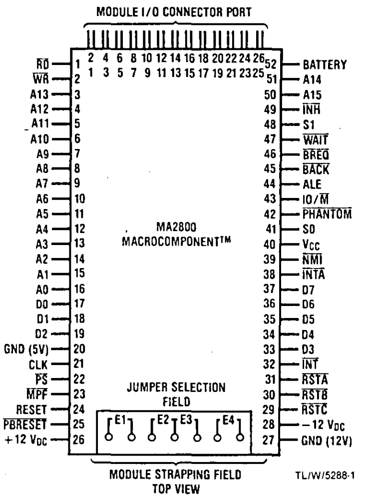
An NSC810 in the CPU module provides the I/O ports and timer. The CPU module utilizes its three ports for basic I/O operation: 8 bits of port A; 6 bits of port B; and 6 bits of port C. Port A can operate in a strobed mode by using 3 bits of port C for handshaking. Two bits of port B can be controlled by the monitor program for serial interfacing. The CPU module also utilizes its two programmable 16-bit timers, capable of DC to 4 MHz operation.

The CPU module controls two memory maps, internal—16k, and external—64k. The internal memory maps consist of the 4k monitor program in ROM, the 2k scratchpad RAM and a user supplied 8k block for programs. The external memory map is user supplied. When selected, the external memory map shadows the internal memory map. The internal memory map defaults to the external memory map at addresses above the 16k block; thus, the top 48k of memory space can be considered common memory.

Features

- General
  - Single 5V power supply
  - On-board monitor program
  - Addresses 64k bytes of memory
  - Addresses 256 I/O spaces
  - Unique save-power feature
  - Standard MA2XXX bus structure
  - Multiplexed and non-multiplexed bus interface capability
  - On-board controller and 2.5 MHz clock generator
  - Speed: 1.6 μs instruction cycle
  - Small size: 1.6 by 3.3 by 0.45 inches
- CPU
  - Fully compatible with Z80 instruction set
  - Powerful set of 158 instructions
  - 10 addressing modes
  - 22 internal registers
  - Five prioritized interrupt request lines
- I/O Ports
  - 3 programmable I/O ports
  - Strobed mode operation
  - Serial interface capability
  - Single instruction I/O bit operation
- Timer
  - Two 16-bit programmable counter/timers
  - Timer operation: DC to 4 MHz

Connection Diagram



TL/W/5288-1

I/O Pin Descriptions

1. RFSH	10. PC1	19. PA7
2. CLK	11. OSC IN	20. PA4
3. T0 OUT	12. PB4	21. PA5
4. T0 IN	13. PB5	22. PA2
5. PC4	14. PB2	23. PA3
6. PC5	15. PB3	24. PA0
7. PC2	16. PB0	25. PA1
8. PC3	17. PB1	26. GND
9. PC0	18. PA6	

Functional Pin Description

SYSTEM BUS INPUT SIGNALS

Power-Save ($\overline{\text{PS}}$): Active low. Places the CPU in a reduced power consumption mode.* $\overline{\text{PS}}$ is sampled at the end of each instruction cycle. If $\overline{\text{PS}}$ is low, the CPU stops executing at the end of the current instruction and puts itself in the low power mode. In this mode, the internal CPU clock is suspended, halting CPU operation (but the oscillator still operates and the CLK signal will still output). Normal operation resumes when $\overline{\text{PS}}$ is returned high.

Reset In ($\overline{\text{PBRESET}}$): Active low. Resets the CPU module. When active, the CPU resets itself by clearing the contents of the PC, I and R registers, disabling the interrupts and setting RESET high.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. Allows a peripheral to interrupt the CPU's normal operation. An active $\overline{\text{NMI}}$ sends the CPU to a dedicated address within the memory map (Table I). An active $\overline{\text{NMI}}$ request is recognized at the end of the current instruction. $\overline{\text{NMI}}$ has the highest priority. $\overline{\text{NMI}}$ execution saves the PC register on the stack.

Restart Interrupts A, B and C ($\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, $\overline{\text{RSTC}}$): Active low. Allows peripherals to interrupt the CPU's normal operations. When enabled (Table II), an active restart interrupt sends the CPU to a dedicated address within the memory map (Table I). Restarts are recognized at the end of the current instruction cycle, when the respective interrupt enable and master interrupt enable bits are set. The order in which the CPU recognizes the interrupt is fixed (highest first) as follows: $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$ and $\overline{\text{RSTC}}$. If not enabled, these lines do not affect the system.

Interrupt Request ($\overline{\text{INT}}$): Active low. Allows a peripheral to interrupt the CPU's normal operation. When enabled (Table II), an active $\overline{\text{INT}}$ sends the CPU to a dedicated address within the memory map (Table I). Active interrupt requests are recognized at the end of the current instruction, provided the interrupt enable and master interrupt enable bits are set. $\overline{\text{INT}}$ has the lowest priority. In conjunction with the $\overline{\text{INTA}}$ output, $\overline{\text{INT}}$ can execute in three distinct modes via software control. If not enabled, this line cannot affect the system.

Bus Request ($\overline{\text{BREQ}}$): Active low. Allows another device control of the system bus. $\overline{\text{BREQ}}$ is recognized at the end of the current machine cycle. If active, the data bus, the address bus and the control signals ($\overline{\text{RD}}$, $\overline{\text{WR}}$, CLK and IO/$\overline{\text{M}}$) are TRI-STATE®. $\overline{\text{BREQ}}$ is acknowledged via setting $\overline{\text{BACK}}$ active.

Wait ($\overline{\text{WAIT}}$): Active low. Extends the machine cycle in order to accommodate slow peripherals communicating with the CPU module. When set low during RD or WR, the CPU extends its machine cycles (in increments of T) until $\overline{\text{WAIT}}$ returns high.

Phantom ($\overline{\text{PHANTOM}}$): Active low. Control line generated by future external modules for disabling external memory. Not used by the CPU module.

Inhibit External Memory ($\overline{\text{INH}}$): Active low. Selects between internal and external memory maps. A low signal activates the internal memory map (disables external memory) and a high signal activates the external memory map (disables internal memory). Note that when using MA2016 external memory modules with the MA2800, jumper E8-E9 must be installed.

SYSTEM BUS OUTPUT SIGNALS

Read Strobe ($\overline{\text{RD}}$): Active low. On the trailing edge of the $\overline{\text{RD}}$ strobe the data lines are input to the CPU. This line is TRI-STATE during reset and bus request cycles.

Write Strobe ($\overline{\text{WR}}$): Active low. When active, the CPU outputs valid data on the data lines. This signal is TRI-STATE during reset and bus request cycles.

Address Bits (A0–A15): Active high. These are the address lines for memory and I/O space. The address bus is TRI-STATE during reset and bus request cycles.

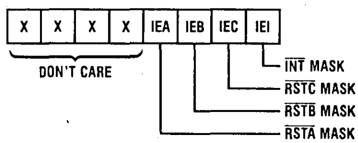
Data Bits (D0–D7): Active high. Typically these lines form the data bus. They input data to the CPU when $\overline{\text{RD}}$ or $\overline{\text{INTA}}$ are active and they output data from the CPU when $\overline{\text{WR}}$ is active. The data bus also contains the addresses (A0–A7) while ALE is high, enabling the CPU module to interface with multiplexed systems (thus, often referred to as DA0–DA7). The data bus is TRI-STATE during reset and bus request cycles.

* Actual power saved is minimal in the module because of ROM and RAM supply currents. I_{CC} drops from approx. 30 mA to 27 mA.

TABLE I

Interrupt Name	Opcode/Instruction (Mode 0 $\overline{\text{INTA}}$ Responses)	Restart Address ROM	Restart Address RAM
$\overline{\text{RST0}}$	C7H	000H	17D0H
$\overline{\text{RST1}}$	CFH	0008H	17D3H
$\overline{\text{RST2}}$	D7H	0010H	17D6H
$\overline{\text{RST3}}$	DFH	0018H	17D9H
$\overline{\text{RST4}}$	E7H	0020H	17DCH
$\overline{\text{RST5}}$	EFH	0028H	17DFH
$\overline{\text{RST6}}$	F7H	0030H	17E2H
$\overline{\text{RST7}}$	FFH	0038H	17E5H
$\overline{\text{INT}}$	N/A	0038H	17E5H
$\overline{\text{RSTA}}$	N/A	003CH	17E8H
$\overline{\text{RSTB}}$	N/A	0034H	17EBH
$\overline{\text{RSTC}}$	N/A	002CH	17EEH
$\overline{\text{NMI}}$	N/A	0066H	17F4H

TABLE II. INTERRUPT CONTROL REGISTER (WRITE TO I/O PORT 0BBH)



0 = disable
1 = enable

Note: When an interrupt occurs, the interrupt control register is cleared to 00. The register can be reset to the previous condition either by re-writing the data to I/O port 0BBH or by executing a Reset to Interrupt Mask Set (RETH) instruction.

Functional Pin Description (Continued)

Clock (CLK): This output provides the system clock. Its frequency is one-half the oscillator's frequency. The CLK is TRI-STATE during bus request cycles.

Reset Out (RESET): Active high. Provides system reset for devices interfacing with the CPU module. When active, it indicates the CPU is being reset, as well as the on-board I/O ports.

Interrupt Acknowledge ($\overline{\text{INTA}}$): Active low. CPU's handshaking response to acknowledge an interrupt that occurred on the $\overline{\text{INT}}$ input. The $\overline{\text{INTA}}$ output activates during the M cycle following the last instruction M cycle. Typically, $\overline{\text{INT}}$ gates the interrupt response vector from the peripheral controller onto the data/address lines.

Status (S0, S1): These outputs indicate the current CPU status.

Input-Output/Memory (IO/$\overline{\text{M}}$): Shows whether the current M cycle is performing an I/O or memory operation. An active high indicates the CPU is interfacing with an input-output device. An active low signifies the CPU is interfacing with memory. This line is TRI-STATE during reset and bus request cycles.

Address Latch Enable (ALE): Active high. ALE is active only during the T1 state of M cycles and T3 state of M1 cycles. The high to low transition of ALE indicates that a valid memory/I-O/refresh address is available on the AD(0-7) lines.

Bus Acknowledge ($\overline{\text{BACK}}$): Active low. A CPU handshake response to acknowledge that a $\overline{\text{BREQ}}$ has occurred. When active, the address, data bus and other control signals have been TRI-STATE, thus relinquishing control of the system bus to the requesting device.

POWER/MISCELLANEOUS SIGNALS

5 Volts (V_{CC}): This input supplies the power (5V) for the entire MA2XXX family.

Ground (5V) [GND (5V)]: Ground return for the 5V power supply.

12 Volts (12V): This input supplies 12V for the MA2XXX family. Not required by the MA2800 CPU module.

−12 Volts (−12V): This input supplies −12V for the MA2XXX family. Not required by the MA2800 CPU module.

Ground (12V) [GND (12V)]: Ground return for the 12V and −12V power supplies. This ground is isolated from GND (5V). Not required by the MA2800 CPU module.

Battery (BATT): Battery source for external memory modules. Not required by the MA2800 CPU module.

Memory Power Fail ($\overline{\text{MPF}}$): Active low. Deselects external devices upon power fail. Not used in MA2800 CPU module.

I/O BUS

Refresh ($\overline{\text{RFSH}}$): Active low. Indicates the CPU is performing a dynamic RAM refresh cycle. $\overline{\text{RFSH}}$ is active only during an opcode fetch cycle. The refresh cycle is transparent to the user.

Port A (PA0-PA7): Parallel I/O port. Port A provides both basic (non-strobed) and strobed (handshake) modes of operation. In the strobed modes of operation, 3 bits of port C provide the handshaking signals.

Port B (PB0-PB5): Parallel I/O port, with serial capability via the monitor program. Port B provides 6 bits (maximum) of basic I/O operation. The monitor program uses bits 4 (out) and 5 (in) of port B for serial interfacing.

Oscillator Input (OSC IN): Oscillator input for the MA2800 system clock. On special request, the internal 5 MHz oscillator is omitted, allowing a user to run at other frequencies via OSC IN (not ordinarily connected within the MA2800 CPU module).

Port C (PC0-PC5): Port C not only provides 6 bits of basic I/O operation; but, each pin performs a second function as follows:

PC0/$\overline{\text{INTR}}$: $\overline{\text{INTR}}$ is an active low strobed mode interrupt to the CPU.

PC1/BF: BF is an active high output to peripheral devices indicating buffer full.

PC2/$\overline{\text{STB}}$: $\overline{\text{STB}}$ is an active low strobe input from peripheral devices.

PC3/TG: TG is the timer gating signal.

PC4/T1 IN: T1 IN is the clock input for timer 1.

PC5/T1 OUT: T1 OUT is the programmable output of timer 1.

PC6/T0 OUT: T0 OUT is the programmable output of timer 0.

PC7/T0 IN: T0 IN is the clock input for timer 0.

Clock (CLK): CLK is the clock output of the NSC800. It is an unbuffered clock signal. This signal runs at one-half the frequency of the on-board oscillator (2.5 MHz output).

Ground (GND): Signal ground for the I/O signals.

JUMPERS

E1: Hardware option of jumpering SQ WAVE to $\overline{\text{RSTC}}$. Internally, the MA2800 creates SQ WAVE by routing the oscillator's output through 20 cascaded, serial flip-flops. Thus, a 5.0 MHz input creates a 2 Hz SQ WAVE signal. When E1 is shorted, SQ WAVE is wired to the $\overline{\text{RSTC}}$ interrupt line. When open, SQ WAVE is not connected to the $\overline{\text{RSTC}}$ interrupt line and is therefore inaccessible to the user.

E2: Hardware option of jumpering port C, bit 0 to $\overline{\text{RSTA}}$. When shorted, PC0 is wired to $\overline{\text{RSTA}}$. When open, PC0 is disconnected from $\overline{\text{RSTA}}$.

E3: Hardware option of jumpering port C, bit 0 to $\overline{\text{RSTB}}$. When shorted, PC0 is wired to $\overline{\text{RSTB}}$. When open, PC0 is disconnected from $\overline{\text{RSTB}}$.

E4: Hardware option of selecting between internal and external memory maps. When open, the MA2800 CPU module will power-up and remain in the external memory map. Software manipulation cannot cause the system to access the internal memory map. When shorted, the CPU module accesses the internal memory map during power-up. User may now switch between the internal and external memory map by programming bit 7 of port B to zero or one, respectively. Note that PB7 is not an output on the I/O connector and is only accessible via software.

System Description

GENERAL

This data sheet is intended to be used in conjunction with the National Semiconductor NSC800 Microprocessor Family Handbook. Further information on how to use the on-board NSC800 and NSC810 and how to program the NSC800 can be found in this handbook. *Figure 1* provides a block diagram illustrating the internal circuitry of the MA2800. Subsequent descriptions detail information unique to the MA2800.

INITIALIZATION

To ensure proper power-up conditions, the following power-up and initialization procedure is recommended. See *Figure 2* for recommended power-on reset circuitry.

1. Apply power (V_{CC} and GND) and set $\overline{\text{PBRESET}}$ active (low). Allow sufficient time (approximately 100 ms if crystal is used) for the oscillator and internal clocks to stabilize. $\overline{\text{PBRESET}}$ must remain low for at least 3 T-states (CLK). Following the clock stabilization period, RESET OUT responds by going high, indicating that the MA2800 has been reset. RESET OUT becomes available to reset the peripherals.

2. Set and maintain $\overline{\text{PBRESET}}$ high. ($\overline{\text{PBRESET}}$ does not have an internal pull-up resistor.) RESET OUT will go low and the CPU will initiate the first opcode fetch cycle.

I/O SPACE

The CPU module can address up to 256 I/O devices. Addresses 00H through 1FH are reserved for the on-board NSC810. Addresses 20H through 27H are reserved for a serial interface module (e.g., MA2232). Location BBH is reserved by the CPU for the interrupt control register, so, special precautions should be taken using this location. All other locations are uncommitted and available for the user's I/O devices.

INTERNAL MEMORY MAP

The internal memory map is 16k bytes (i.e., from 0000H to 3FFFH). The first 4k (0000H to 0FFFH) of internal memory space contains the monitor program. The next 2k (1000H to 17FFH) contains RAM. The monitor program uses this RAM (from 1700H to 17FFH) as a scratchpad. Most of the space in this RAM is user available (i.e., from 1000H to 16FFH). The next 2k (1800H to 1FFFH) is not accessible to the user or system, it is a 2k hole. The last 8k (2000H to 3FFFH) is available for the user to plug 8k of his memory into the system. This allows the user to run an 8k program in a minimum system configuration.

When in the internal memory map and an address at 4000H or above occurs, the CPU automatically addresses external memory space. The CPU automatically returns to the internal memory map when the address is less than 4000H. The internal memory map automatically defaults to the external memory map whenever the address is above 4000H; thus, the user can add another 48k of memory. Therefore, the user can actually have 56k of

Block Diagram

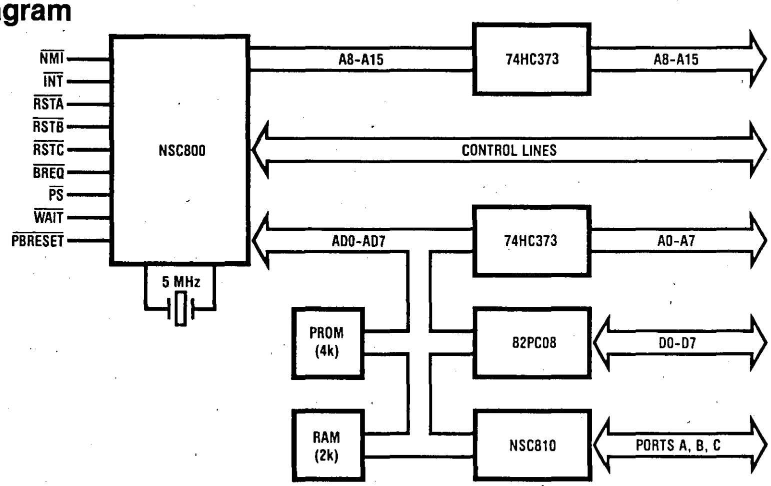
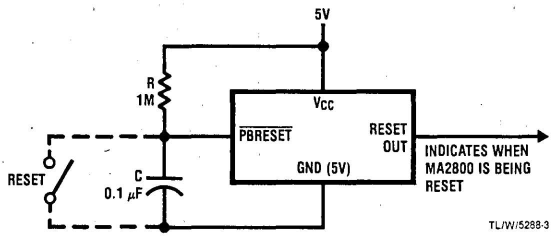


FIGURE 1

TL/W/5288-2



TL/W/5288-3

FIGURE 2. Power-On, Reset Circuitry

System Description (Continued)

memory space available. For applicable control signals, see Table III.

TABLE III

Memory Map	Control Signals			Address Space
	E4	PB7	$\overline{INH}$	
Internal	Shorted	Zero	Low	0000H-3FFFH
External	Shorted	One	High	0000H-FFFFH
	Open	Don't Care		

EXTERNAL MEMORY MAP

The external memory map is a full 64k bytes (i.e., from 0000H to FFFFH). When in the external memory map, the resident monitor program and 2k scratchpad RAM cannot be accessed because the external memory map shadows the internal memory map. The external memory map is accessed through software or hardware. Software selection of the external memory map requires shorting jumper E4 and outputting a one on bit 7 of port B. Hardware selection of the external memory map requires jumper E4 to be left open. Note how the external memory map is accessed by the internal memory map, since the top 48k of memory space is common to the internal and external memory maps. For applicable control signals, see Table III.

MONITOR PROGRAM

The MA2800 contains a software monitor program; its commands ease control of ports, memory and peripherals. Upon power-up, the monitor program checks if a MA2232 Serial Interface Macrocomponent is at I/O address 20H through 27H. If present, the MA2800 prefers it for serial interfacing. If not present or chosen, the monitor program utilizes port B, bits 4 and 5, for serial interfacing. The monitor program automatically adjusts to the baud rate of the serial interface, if less than or equal to a 9600 baud rate.

When not using a MA2232 or equivalent, interfacing the MA2800 to a RS232 port requires connecting I/O connector pins 12, 13 and 26 (PB4, PB5 and GND) to RS232 port pins 2, 3 and 7, (transmitted data, received data and signal ground), respectively. Also, connect a 5V zener diode between RS232 port pins 2 and 7, cathode on pin 2.

The monitor program is brought on-line by hitting the period (.) key until the following message displays: "MA2800 Monitor Rev. (date)". (Be sure E4 is shorted.) After this message and prompt appear, the monitor program is accessible. After a reset, bring the monitor program back on-line by the above procedure.

All commands in the MA2800 monitor consist of a single character followed by possibly optional arguments separated by either commas or spaces. In all cases, the value used is the last two hex digits typed for 1 byte arguments and the last 4 characters typed for 2 byte parameters. All commands terminate with a carriage return except as noted. All commands and data can be typed in either upper or lower case, but will be echoed in upper case.

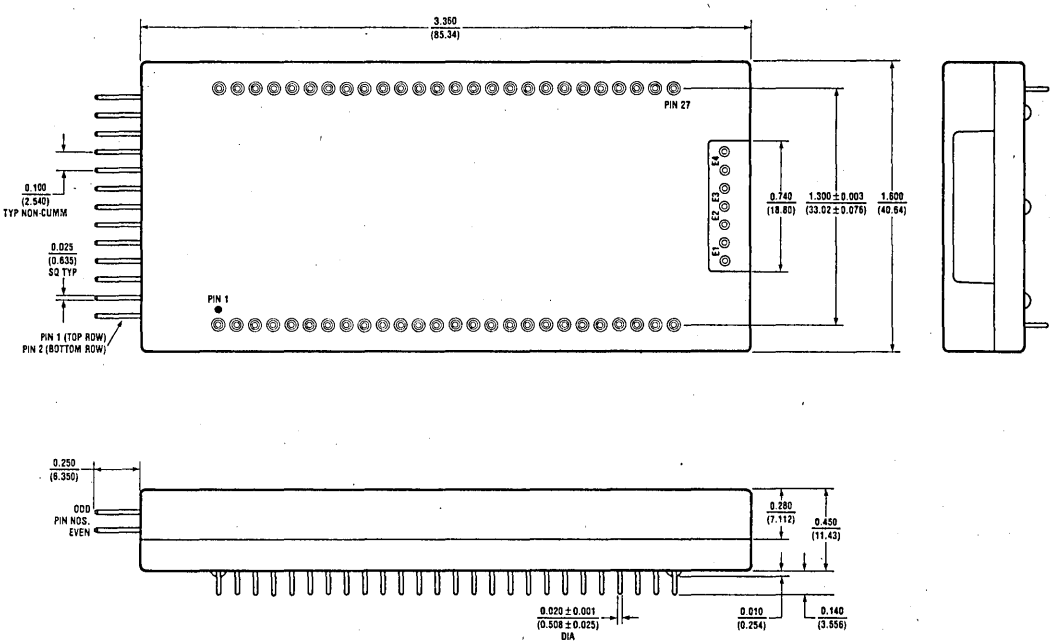
Command		Example
A:	Disable Interrupts	A
B:	Enable Interrupts	B
C:	Change 16 bit immediate	Cssss,wwww
D:	Display Memory	Dssss,ffff
E:	Display Registers	E OR Err retn
F:	Find word in memory	Fwwww,ssss,ffff
G:	Go <with breakpoints>	Gssss<,bbbb<,cccc>>
H:	Add and subtract Hex	Haa,bb
I:	Input from port	Ipp,qq
L:	Output data to serial	Lpp,ssss,ffff
M:	Move memory	Mssss,ffff,dddd
N:	Single Step	N
O:	Output to port	Opp,dd
P:	Put ASCII to memory	Pssss retn (ascii text) D to terminate
R:	Read hex format data	R OR Rssss
S:	Substitute memory	S OR Sssss SPACE. Terminate with illegal character
T:	Memory Test	Tssss,ffff
U:	User define function	U must set up loc 17F2 with address before using
V:	Verify memory	Vssss,ffff,dddd No message means successful verify
W:	Write hex format data	Wssss,ffff
X:	Display Registers	X OR Xrr retn
Y:	32 byte memory Search	Yaa,bb,cc,...search all 65k of memory and display starting addr of any occurrences of the byte sequence
Z:	Set MA2232 Baud rate	Zpp,rrrr
?:	List commands	?
^F:	Fill memory	^Fbb,ssss,ffff
^J or CR:	Display last loc.	This is the default memory location used by the Substitute command
^R:	Transfer to RAM	displays the message 'RUNNING IN RAM' on terminal, then branches to loc 0 and waits for auto baud character
^p:	Printer toggle	ON/OFF control of serial printer using MA2232 at port 28h defaults to 9600 baud.

System Description (Continued)

In the previous table examples, the upper case letter represents the command character and the lower case designators are as follows:

aa	two hex digits
bb	two hex digits
bbbb	breakpoint 1 address
cc	two hex digits
cccc	breakpoint 2 address
dd	two hex digits
dddd	destination address
ffff	end of memory range
pp	port number (start)
qq	ending port number
rr	register name
rrrr	baud rate
ssss	start of memory range
wwww	two byte word (hi byte first)

Physical Dimensions inches (millimeters)



Order Number MA2800

National Semiconductor

microCMOS

MM82PC08
8-Bit Bidirectional Transceiver

General Description

The MM82PC08 is an 8-bit TRI-STATE® high-performance, low-power microCMOS transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured.

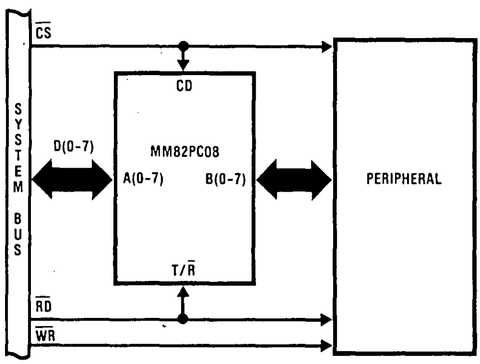
One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver; Transmit specifies data flow from Port A to Port B; Receive specifies data flow from Port B to Port A. The Chip Disable input disables both ports by placing them in the high impedance state.

The MM82PC08 may be utilized in completing NSC800 high-performance, low-power designs. For military applications, the MM82PC08 is available with class B screening in accordance with Method 5004 of MIL-STD-883.

Features

- microCMOS technology
- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus-oriented systems
- Full interface to CMOS logic levels
- Pinouts simplify system interconnections
- Transmit/receive and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Compact 28-pin leaded chip carrier
- Low power
- Both ports have 150 pF load drive capability
- TTL drive capability When $V_{CC} = 5V$

System Configuration



TL/C/5595-1

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to 150°C
Voltage at Any Pin with Respect to Ground	−0.3V to $V_{CC}+0.3V$
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	500mW
Maximum V_{CC}	7V

Note: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Operating Range $V_{CC}=5V\pm10\%$

Ambient Temperature	
Military	−55°C to 125°C
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

DC Electrical Characteristics $T_A=-55°C$ to $+125°C$, $V_{CC}+5V\pm10\%$, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Input Low Voltage		0		0.2 V_{CC}	V
V_{OH}	Output High Voltage	$V_{CC}=4.5V$, $V_{IH}=4.5V$, $I_{OH}=-2$ mA	2.4			V
V_{OL}	Output Low Voltage	$V_{CC}=5.5V$, $V_{IL}=0V$ $V_{IH}=5.5V$, $I_{OL}=2$ mA			0.4	V
I_{IH}	Input High Current	$V_{CC}=5.5V$, $V_{IN}=5.5V$			10	μA
I_{IL}	Input Low current	$V_{CC}=5.5V$, $V_{IN}=0V$			−10	μA
I_{OH}	Output High Current	$V_{CC}=4.5V$, $V_{OUT}=2.4V$, $V_{IH}=4.5V$	−2.0			mA
I_{OL}	Output Low Current	$V_{CC}=5.5V$, $V_{OUT}=0.4V$, $V_{IL}=0V$	2.0			mA
I_{CC}	Power Supply Current	$V_{CC}=5.5V$, $V_{IH}=5.5V$, $V_{IL}=0V$			400	μA
I_{OZL}	TRI-STATE Low Leakage Current	$V_{CC}=5.5V$, $V_{OUT}=0V$			−10	μA
I_{OZH}	TRI-STATE High Leakage Current	$V_{CC}=4.5V$, $V_{OUT}=4.5V$			+10	μA

AC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $C_L = 150\ pF$

Symbol	Parameter	Test Conditions	Min	Typ 100 pF	Max 100 pF	Units
t_{DLH}	Propagation Delay to Logical "1" from Port A, B to Port B, A	See *Figure 1*		50	70	ns
t_{DHL}	Propagation Delay to Logical "0" from Port A, B to Port B, A	See *Figure 1*		50	70	ns
t_{ZHTR}	Propagation Delay from High Impedance to Logical "1" from T/R to Port	See *Figure 2*		55	100	ns
t_{ZLTR}	Propagation Delay from High Impedance to Logical "0" from T/R to Port	See *Figure 2*		65	100	ns
t_{HZTR}	Propagation Delay from Logical "1" to High Impedance from T/R to Port	See *Figure 2*		50	100	ns
t_{LZTR}	Propagation Delay from Logical "0" to High Impedance from T/R to Port	See *Figure 2*		55	100	ns
t_{ZH}	Propagation Delay from High Impedance to Logical "1" from CD to Port	See *Figure 3*		50	100	ns
t_{ZL}	Propagation Delay from High Impedance to Logical "0" from CD to Port	See *Figure 3*		65	100	ns
t_{HZ}	Propagation Delay from Logical "1" to High Impedance from CD to Port	See *Figure 3*		50	100	ns
t_{LZ}	Propagation Delay from Logical "0" to High Impedance from CD to Port	See *Figure 3*		55	100	ns

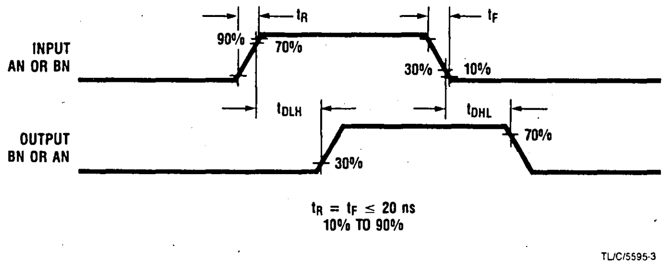


FIGURE 1. Propagation Delay from Input Port to Output Port

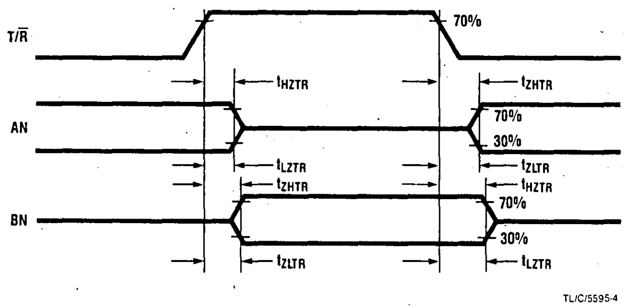


FIGURE 2. Propagation Delay from T/R to Ports

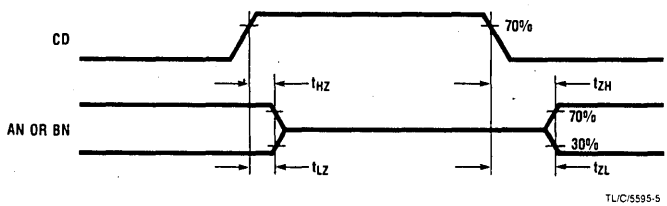


FIGURE 3. Propagation Delay from CD to Ports

Functional Pin Descriptions

INPUT SIGNALS

Chip Disable (CD): When CD is high, Port A and Port B are disabled. A low on CD allows data to be transmitted in the direction specified by T/$\overline{R}$.

Transmit/Receive (T/$\overline{R}$): When T/$\overline{R}$ is high, Port A is designated as "IN" and Port B is designated as "OUT." When T/$\overline{R}$ is low, the flow is reversed so that the Port B is "IN" and Port A is "OUT."

INPUT/OUTPUT SIGNALS

Port A (A0–A7): Port A is an 8-bit bidirectional port with TRI-STATE outputs for bus-oriented microprocessor and digital communications systems.

Port B (B0–B7): Port B is identical to Port A including drive capability.

Logic Diagram

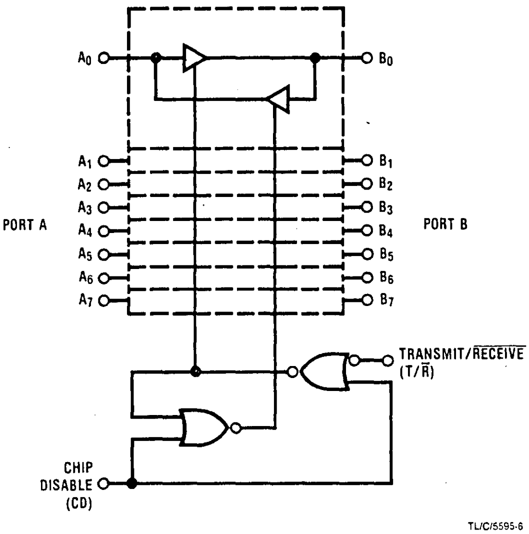


FIGURE 4

Truth Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	Port A	Port B
0	0	OUT	IN
0	1	IN	OUT
1	X	High Z	High Z

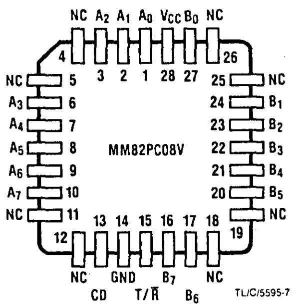
X = don't care

Reliability Information

Gate Count 70
Transistor Count 174

Connection Diagrams

V Package



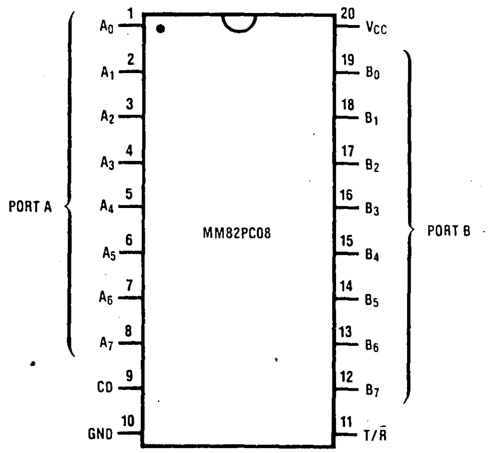
NC = No Connect

Plastic Dual In-Line Package (N)
NS Package Number N20A

28-Lead Plastic Chip Carrier (V)
NS Package Number V28

Ceramic Dual In-Line Package (J)
NS Package Number J20A

Dual In-Line Package



Top View

Ordering Information

MM82PC08XXX

- /A+ = A+ Reliability Screening
- /883 = MIL-STD-883B Screening (Note 1)

- I = Industrial Temperature (−40°C to +85°C)
- M = Military Temperature (−55°C to +125°C)
- No Designation = Commercial Temperature (0°C to +70°C)

- N = Plastic Package
- J = Cerdip Package
- V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)

Note 1: Do not specify a temperature option; all parts are screened to military temperature.

National Semiconductor

microCMOS

MM82PC12

MM82PC12 8-Bit Input/Output Port

General Description

The MM82PC12 is a microCMOS™ 8-bit input/output port contained in a standard 24-pin dual-in-line package. The MM82PC12 can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The MM82PC12 includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

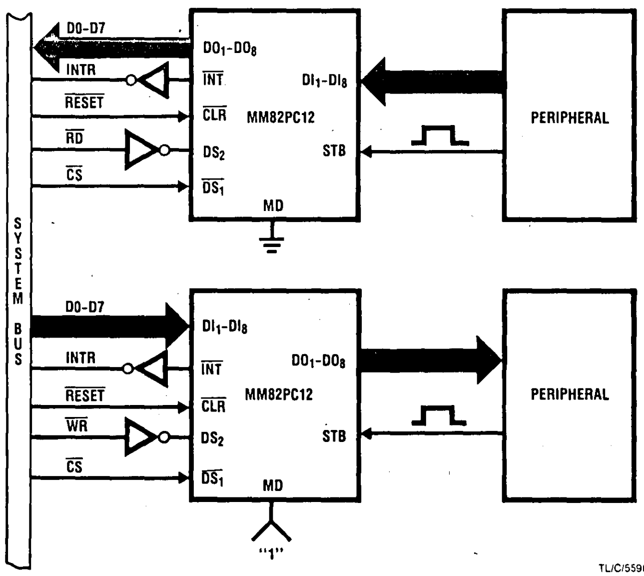
The MM82PC12 is pinout and function compatible with standard INS8212 and DP8212 devices.

For military applications, the MM82PC12 is available with class B screening in accordance with method 5004 of MIL-STD-883.

Features

- Drive capability — 150 pF load
- High noise immunity
- Low power dissipation
- Full interface to CMOS logic levels
- microCMOS technology
- TTL drive capability when V_{CC} = 5V
- 8-bit data latch and buffer
- Service request flip-flop for generation and control of interrupts
- 1 μA input load current
- Reduces system package count by replacing buffers, latches, and multiplexers in microcomputer systems

System Configuration



TL/C/5596-1

12

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin With Respect to Ground	−0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	500 mW
Maximum V_{CC}	7V

Note: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Operating Range V_{CC} = 5V ± 10%

Ambient Temperature	
Military	−55°C to +125°C
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

DC Electrical Characteristics T_A = −55°C to +125°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise specified

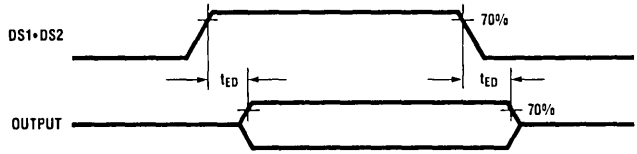
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Input Low Voltage		0		0.2 V_{CC}	V
V_{OH}	Output High Voltage	V_{CC} = 4.5V, V_{IH} = 4.5V, I_{OH} = −2 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = 5.5V, V_{IL} = 0V, V_{IH} = 5.5V, I_{OL} = 2 mA			0.4	V
I_{IH}	Input High Current	V_{CC} = 5.5V, V_{IN} = 5.5V			10	μA
I_{IL}	Input Low Current	V_{CC} = 5.5V, V_{IN} = 0V			−10	μA
I_{OH}	Output High Current	V_{CC} = 4.5V, V_{OUT} = 2.4V, V_{IH} = 4.5V	−2.0			mA
I_{OL}	Output Low Current	V_{CC} = 5.5V, V_{OUT} = 0.4V, V_{IL} = 0V	2.0			mA
I_{CC}	Power Supply Current	V_{CC} = 5.5V, V_{IH} = 5.5V, V_{IL} = 0V			400	μA
I_{OZL}	TRI-STATE Low Leakage Current	V_{CC} = 5.5V, V_{OUT} = 0V			−10	μA
I_{OZH}	TRI-STATE High Leakage Current	V_{CC} = 4.5V, V_{OUT} = 4.5V			10	μA

AC Electrical Characteristics T_A = −55°C to +125°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PW}	Pulse Width(STB, DS1•DS2, CLR)			25	40	ns
t_{PD}	Data In to Data Out			45	60	ns
t_{WE}	Write Enable to Data Out			55	75	ns
t_{SET}	Data Setup Time		15			ns
t_H	Data Hold Time		20			ns
t_R	Reset to Data Out			50	65	ns
t_S	Select to Interrupt			50	65	ns
t_C	Clear to Data Out			45	60	ns
t_{ED}	Output Enable/Disable Time			50	65	ns

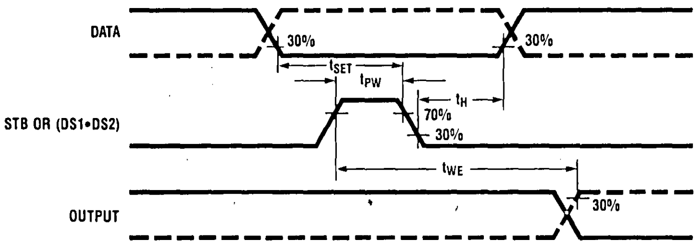
Timing Waveforms

Read Timing



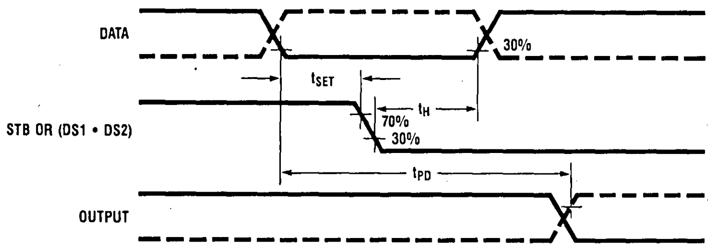
TL/C/5596-2

Write Timing



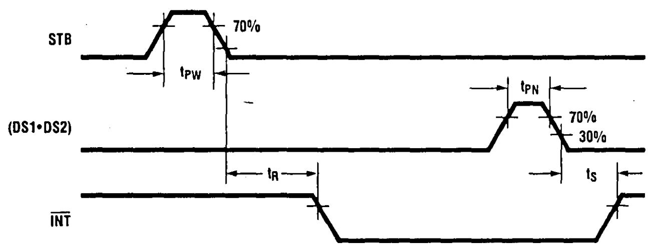
TL/C/5596-3

Data Setup, Hold Delay Timing



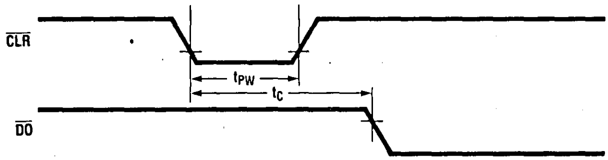
TL/C/5596-4

Interrupt Timing



TL/C/5596-5

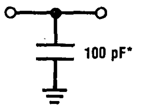
Clear Timing



TL/C/5596-6

Propagation Delays

Figure 1 illustrates the calculations of a more useful propagation delay. The figure uses a 5-volt supply with a tolerance of ±10%, ambient temperature of +25°C, and a load capacitance of 100 pF. The AC Characteristics table depicts t_{PD}, at 5 volts, 25°C, equalling 25 ns. Use the graph in *Figure 1* to get the degradation multiple for 150 pF. The number shown is 1.09. The adjusted propagation delay is, therefore 25 × 1.09 or 27 ns.



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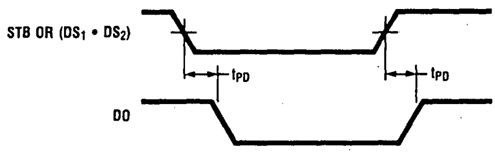
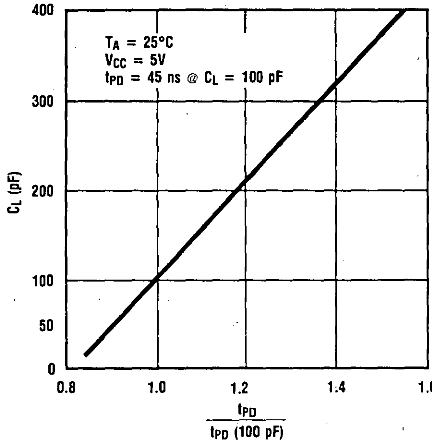
*Including jig and probe capacitance.

Output Test Circuit for Propagation Delays



TL/C/5596-8



TL/C/5596-9

FIGURE 1. Normalized Typical Propagation Delay vs. Load Capacitance

Functional Pin Descriptions

The following describes the function of all the MM82PC12 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS_1}$, DS_2): When $\overline{DS_1}$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When MD is high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic (DS_1 • DS_2). When MD is low (input mode), the state of the output buffers is determined by the device selection logic (DS_1 • DS_2) and the source of the data latch clock input is the strobe (STB) input.

Strobe (STB): STB is used as the data latch clock input when the mode (MD) input is low (input mode). STB is also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1–DI_8): Data In is the 8-bit data input to the data latch, which consists of eight D-type flip-flops incorporating a level sensitive clock. While the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. Clear ($\overline{CLR}$) is only effective when the clock is low (latch in the latched state).

Clear ($\overline{CLR}$): When $\overline{CLR}$ is low, the data latch is reset (cleared) if the clock is also low. The clock input high overrides the clear ($\overline{CLR}$) input data latch reset. $\overline{CLR}$ being low also resets the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

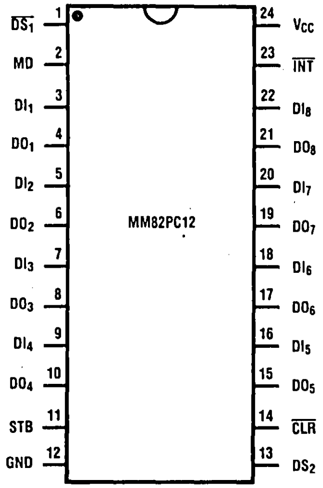
Interrupt ($\overline{INT}$): The interrupt pin goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO_1–DO_8): Data Out is the 8-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

Reliability Information

Gate Count 108
Transistor Count 248

Connection Diagrams

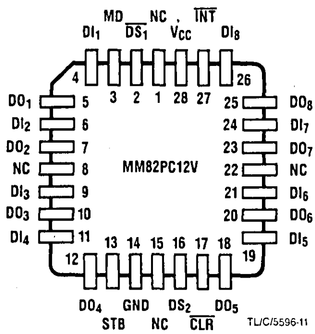


TL/C/5596-10

Plastic Dual In-Line Package (N)
NS Package Number N24A

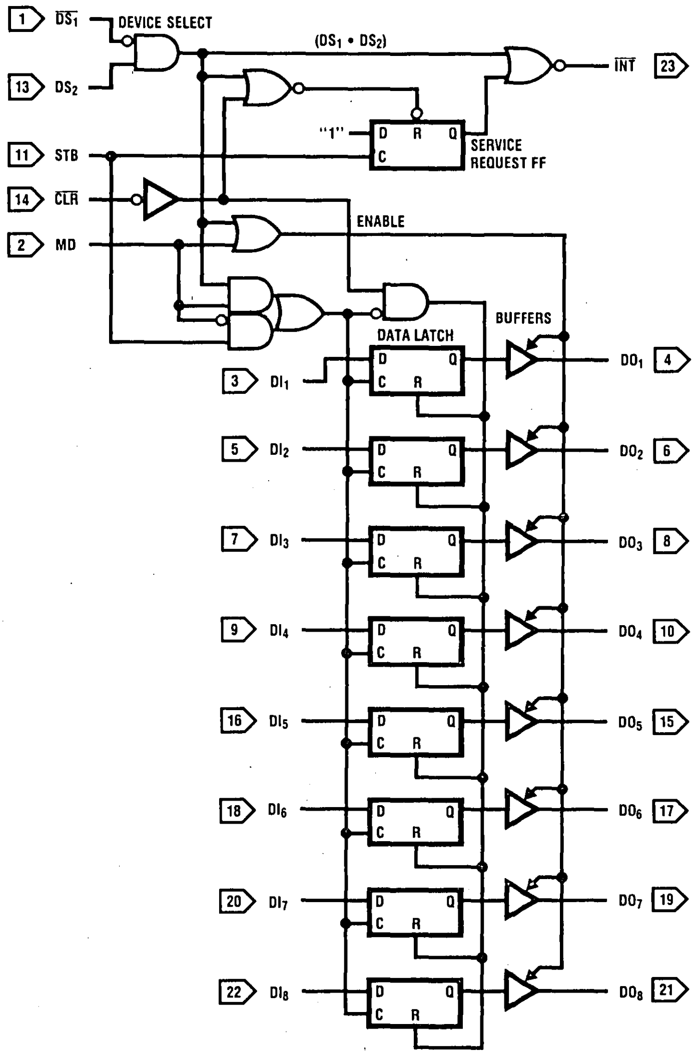
28-Lead Plastic Chip Carrier (V)
NS Package Number V28

Ceramic Dual In-Line Package (J)
NS Package Number J24A



TL/C/5596-11

Logic Diagram



TL/C/5596-12

Logic Table A

STB	MD	$DS_1 \bullet DS_2$	Data Out Equals
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

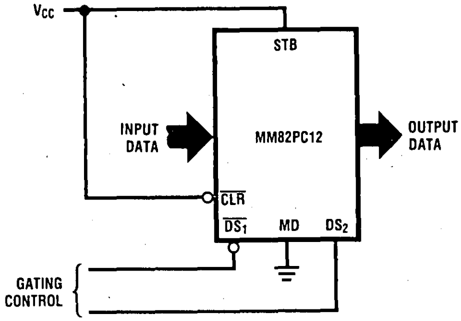
Note: $\overline{CLR}$ ‾|_ resets data latch to the output low state. The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

$\overline{CLR}$	$DS_1 \bullet DS_2$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	‾|_	1	0
1	1 RESET	0	0	0
1	0	0	0	1

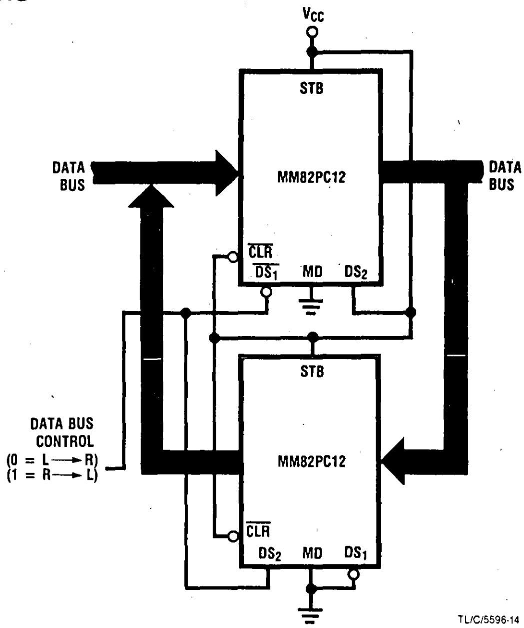
*Internal Service Request flip-flop.

Applications in Microcomputer Systems



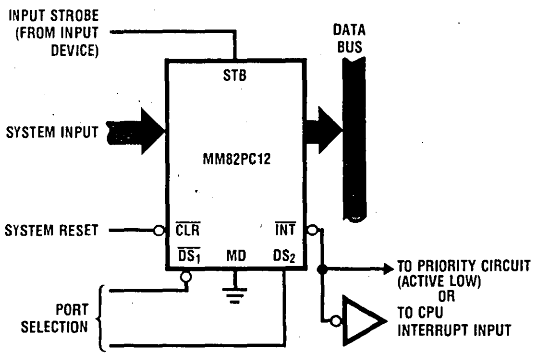
TL/C/5596-13

Gated Buffer (TRI-STATE)



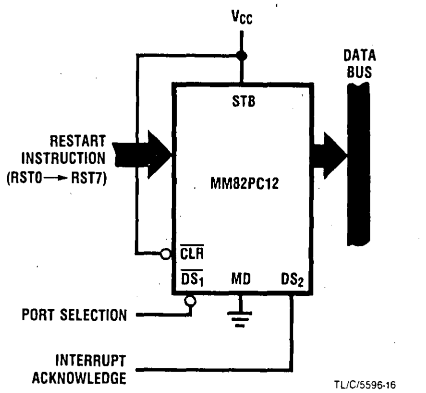
TL/C/5596-14

Bidirectional Bus Driver



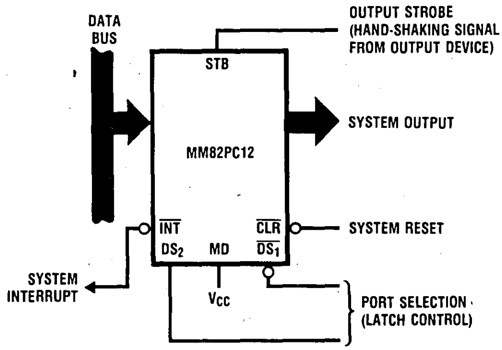
TL/C/5596-15

Interrupting Input Port



TL/C/5596-16

Interrupt Instruction Port



TL/C/5596-17

Output Port (with Handshaking)

Ordering Information

MM82PC12XXX

- /A+ = A+ Reliability Screening
- /883 = MIL-STD-883B Screening (Note 1)

- I = Industrial Temperature (−40°C to +85°C)
- M = Military Temperature (−55°C to +125°C)
- No Designation = Commercial Temperature (0°C to +70°C)

- N = Plastic Package
- J = Cerdip Package
- V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)

Note 1: Do not specify a temperature option; all parts are screened to military temperature.

National Semiconductor

microCMOS

NSC800™ High-Performance Low-Power Microprocessor

General Description

The NSC800 is an 8-bit microprocessor that functions as the central processing unit (CPU) in National Semiconductor's NSC800 microcomputer family. The device is fabricated using National's microCMOS technology. This technology provides the system designer with devices equaling the performance levels of comparable NMOS products, combined with the low-power advantages of CMOS. Many system functions are incorporated on the device, such as: vectored priority interrupts, refresh control, power-save feature and interrupt acknowledge. The NSC800 is housed in dual-in-line and chip carrier packages.

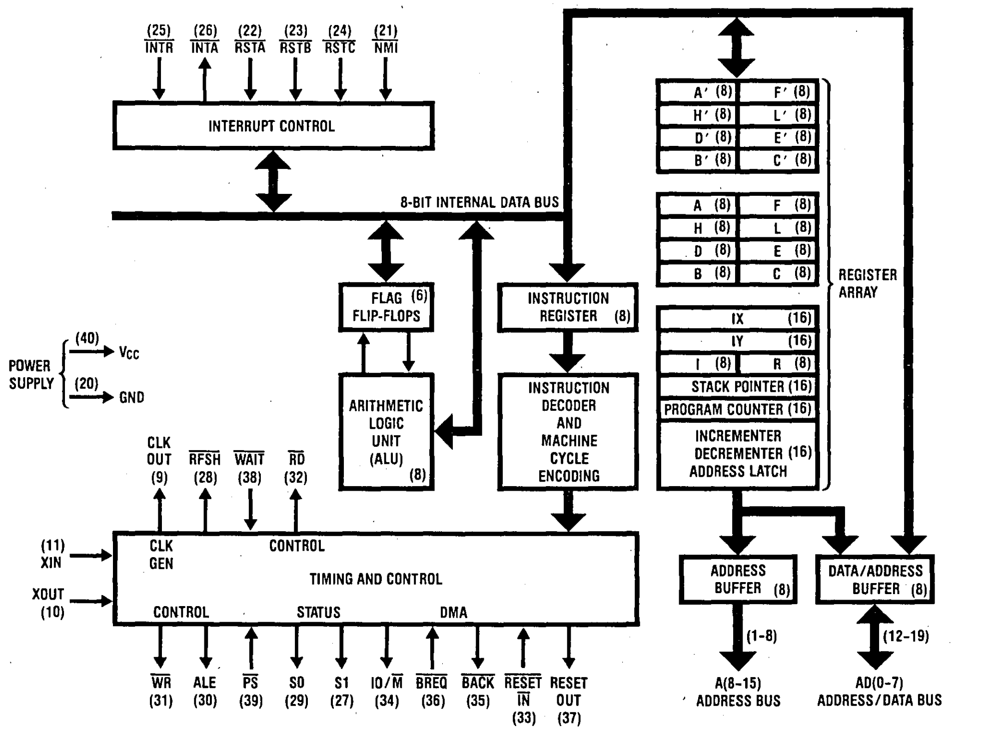
Dedicated peripherals (NSC810A RAM I/O Timer, NSC831 I/O and NSC858 UART) have on-chip logic for direct interface to the NSC800. In addition, National also offers a full line of CMOS components to allow a full low-power solution to system designs.

For military applications, the NSC800 is available with class B screening in accordance with Method 5004 of MIL-STD-883.

Features

- Variable power supply 2.4V – 6.0V
- Fully compatible with Z80 instruction set
- Powerful set of 158 instructions
- 10 addressing modes
- 22 internal registers
- Low power: 50 mW at 5V V_{CC}
- Multiplexed bus structure
- On-chip bus controller and clock generator
- On-chip 8-bit dynamic RAM refresh circuitry
- Speed: 1.0 µs instruction cycle at 4.0 MHz
  - NSC800-4 4.0 MHz
  - NSC800 2.5 MHz
  - NSC800-1 1.0 MHz
- Capable of addressing 64k bytes of memory and 256 I/O devices
- Five interrupt request lines on-chip
- Schmitt trigger input on reset
- Unique standby-current (power-save) feature

CPU Functional Block Diagram



TL/C/5171-1

Absolute Maximum Ratings (Note 1)

Storage Temperature	$-65°C$ to $+150°C$
Voltage on Any Pin with Respect to Ground	$-0.3V$ to $V_{CC}+0.3V$
Maximum V_{CC}	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions $V_{CC}=5V \pm 10\%$

Ambient Temperature	
Military	$-55°C$ to $+125°C$
Industrial	$-40°C$ to $+85°C$
Commercial	$0°C$ to $+70°C$

DC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC}=5V \pm 10\%$, GND = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{HY}	Hysteresis at RESET IN input	$V_{CC}=5V$	0.25	0.5		V
V_{OH1}	Logical 1 Output Voltage	$I_{OUT}=-1.0$ mA	2.4			V
V_{OH2}	Logical 1 Output Voltage	$I_{OUT}=-10\ \mu A$	$V_{CC}-0.5$			V
V_{OL1}	Logical 0 Output Voltage	$I_{OL}=2$ mA	0		0.4	V
V_{OL2}	Logical 0 Output Voltage	$I_{OUT}=10\ \mu A$	0		0.1	V
I_{IL}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$	-10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \leq V_{IN} \leq V_{CC}$	-10.0		10.0	μA
I_{CCA}	Active Supply Current	$I_{OUT}=0$, $f_{(XIN)}=5$ MHz		10	15	mA
I_{CCA}	Active Supply Current	$I_{OUT}=0$, $f_{(XIN)}=8$ MHz		15	21	mA
I_{CCQ}	Quiescent Current	$f_{(XIN)}=0$ MHz		2	4	mA
I_{CPS}	Power-Save Current	$f_{(XIN)}=5.0$ MHz		5		mA
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			8	12	pF
V_{CC}	Power Supply Voltage	Note 2	2.4	5	6	V

Note 1: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

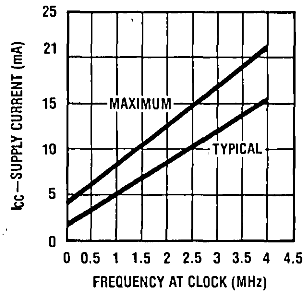
Note 2: CPU operation at lower voltages will reduce the maximum operating speed. DC and AC electrical characteristics at voltages other than 5V ± 10% are forthcoming.

Preliminary (not tested)

Max CPU Speed*	NSC800-1	NSC800	NSC800-4	Units
@2.4V	—	500	500	kHz
@3.0V	—	1	1	MHz

*Speed of CPU is expressed in clock speed, not crystal speed.

I_{CC} vs System Speed



TL/C/5171-2

12

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V

(Valid for the following temperature & speed)

NSC800-1 → $T_A = 0°C$ to 70°C
$T_A = -40°C$ to +85°C
NSC800 → $T_A = 0°C$ to 70°C
$T_A = -40°C$ to +85°C
$T_A = -55°C$ to +125°C

NSC800-4 → $T_A = 0°C$ to 70°C
$T_A = -40°C$ to +85°C
$T_A = -55°C$ to +125°C

Symbol	Parameter	NSC800-1		NSC800		NSC800-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_X	Period at XIN and XOUT Pins	500	31250	200	31250	125	31250	ns	
T	Period at Clock Output (= 2 t_X)	1000	62500	400	62500	250	62500	ns	
t_R	Clock Rise Time		110		110		75	ns	Measured from 10%–90% of signal
t_F	Clock Fall Time		60		60		40	ns	Measured from 10%–90% of signal
t_L	Clock Low Time	490		190		95		ns	50% duty cycle, square wave input on XIN
t_H	Clock High Time	450		150		80		ns	50% duty cycle, square wave input on XIN
$t_{ACC(RD)}$	ALE to Valid Data		1375		500		300	ns	Add t for each $\overline{WAIT}$ STATE Add t/2 for memory read cycles
t_{AFR}	AD(0–7) Float after $\overline{RD}$ Falling		0		0		0	ns	
t_{BABE}	$\overline{BACK}$ Rising to Bus Enable		1000		400		250	ns	
t_{BABF}	$\overline{BACK}$ Falling to Bus Float		50		50		50	ns	
t_{BACL}	$\overline{BACK}$ Falling to CLK Falling	425		125		55		ns	
t_{BRH}	$\overline{BREQ}$ Hold Time	0		0		0		ns	
t_{BRS}	$\overline{BREQ}$ Set-Up Time	100		50		35		ns	
t_{CAF}	Clock Falling to ALE Falling	0	30	0	30	0	35	ns	
t_{CAR}	Clock Rising to ALE Rising	0	100	0	100	0	75	ns	
t_{DAI}	ALE Falling to $\overline{INTA}$ Falling	530		230		100		ns	
t_{DAR}	ALE Falling to $\overline{RD}$ Falling	525	575	225	250	125	160	ns	
t_{DAW}	ALE Falling to $\overline{WR}$ Falling	990	1010	390	410	220	250	ns	
$t_{D(BACK)1}$	ALE Falling to $\overline{BACK}$ Falling	2500		1000		600		ns	Add t for each $\overline{WAIT}$ state Add t for opcode fetch cycles
$t_{D(BACK)2}$	$\overline{BREQ}$ Rising to $\overline{BACK}$ Rising	500	1600	200	700	125	475	ns	
$t_{D(I)}$	ALE Falling to $\overline{INTR}$, $\overline{NMI}$, $\overline{RSTA\text{-}C}$, $\overline{PS}$, $\overline{BREQ}$, Inputs Valid		1375		475		250	ns	Add t for each $\overline{WAIT}$ state Add t for opcode fetch cycles
t_{DPA}	Rising $\overline{PS}$ to Falling ALE	500	1550	200	650	125	475	ns	See *Figure 12* also
$t_{D(RFSH)}$	Falling ALE to Falling $\overline{RFSH}$	1500		600		325		ns	Add t for each $\overline{WAIT}$ state
$t_{D(WAIT)}$	ALE Falling to $\overline{WAIT}$ Input Valid		550		250		125	ns	

AC Electrical Characteristics (Continued) $V_{CC} = 5V \pm 10\%$, GND = 0V

(Valid for the following temperature & speed)

NSC800-1 — $T_A = 0°C$ to $70°C$
$T_A = -40°C$ to $+85°C$
NSC800 — $T_A = 0°C$ to $70°C$
$T_A = -40°C$ to $+85°C$
$T_A = -55°C$ to $+125°C$

NSC800-4 — $T_A = 0°C$ to $70°C$
$T_A = -40°C$ to $+85°C$
$T_A = -55°C$ to $+125°C$

Symbol	Parameter	NSC800-1		NSC800		NSC800-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
$t_{H(ADH)1}$	A(8–15) Hold Time During Opcode Fetch	0		0		0		ns	
$t_{H(ADH)2}$	A(8–15) Hold Time During Memory or IO, $\overline{RD}$ and $\overline{WR}$	400		100		60		ns	
$t_{H(ADL)}$	AD(0–7) Hold Time	100		60		30		ns	
$t_{H(WD)}$	Write Data Hold Time	400		100		75		ns	
t_{INH}	Interrupt Hold Time	0		0		0		ns	
t_{INS}	Interrupt Set-Up Time	100		50		35		ns	
t_{NMI}	Width of NMI Input	50		30		20		ns	
t_{RDH}	Data Hold after Read	0		0		0		ns	
t_{RFL}	$\overline{RFSH}$ Rising to ALE Rising		−100		−100		−70	ns	Negative number means ALE occurs first
$t_{RL(MR)}$	$\overline{RD}$ Rising to ALE Rising (Memory Read)	450		150		85		ns	
$t_{RL(OP)}$	$\overline{RD}$ Rising to ALE Rising (Opcode)		−75		−65		−55	ns	Negative number means ALE occurs first
$t_{S(AD)}$	AD(0–7) Set-Up Time	300		80		40		ns	
$t_{S(ALE)}$	A(8–15), SO, SI, IO/$\overline{M}$ Set-Up Time	350		100		50		ns	
$t_{S(WD)}$	Write Data Set-Up Time	385		85		50		ns	
$t_{W(ALE)}$	ALE Width	430		130		75		ns	
t_{WH}	$\overline{WAIT}$ Hold Time	0		0		0		ns	
$t_{W(I)}$	Width of $\overline{INTR}$, $\overline{RSTA\text{-}C}$, $\overline{PS}$, $\overline{BREQ}$	500		200		125		ns	
$t_{W(INTA)}$	$\overline{INTA}$ Strobe Width	1000		400		200		ns	Add two t states for first $\overline{INTA}$ of each interrupt response string Add t for each $\overline{WAIT}$ state
t_{WL}	$\overline{WR}$ Rising to ALE Rising	450		150		90		ns	
$t_{W(RD)}$	Read Strobe Width During Opcode Fetch	1000		400		225		ns	Add t for each $\overline{WAIT}$ State Add t/2 for Memory Read Cycles
$t_{W(RFSH)}$	Refresh Strobe Width	1925		725		400		ns	
t_{WS}	$\overline{WAIT}$ Set-Up Time	100		50		35		ns	
$t_{W(WAIT)}$	$\overline{WAIT}$ Input Width	550		250		175		ns	
$t_{W(WR)}$	Write Strobe Width	1000		400		220		ns	Add t for each $\overline{WAIT}$ state
t_{XCF}	XIN to Clock Falling	25	55	25	55	25	55	ns	
t_{XCR}	XIN to Clock Rising	45	75	45	75	45	75	ns	

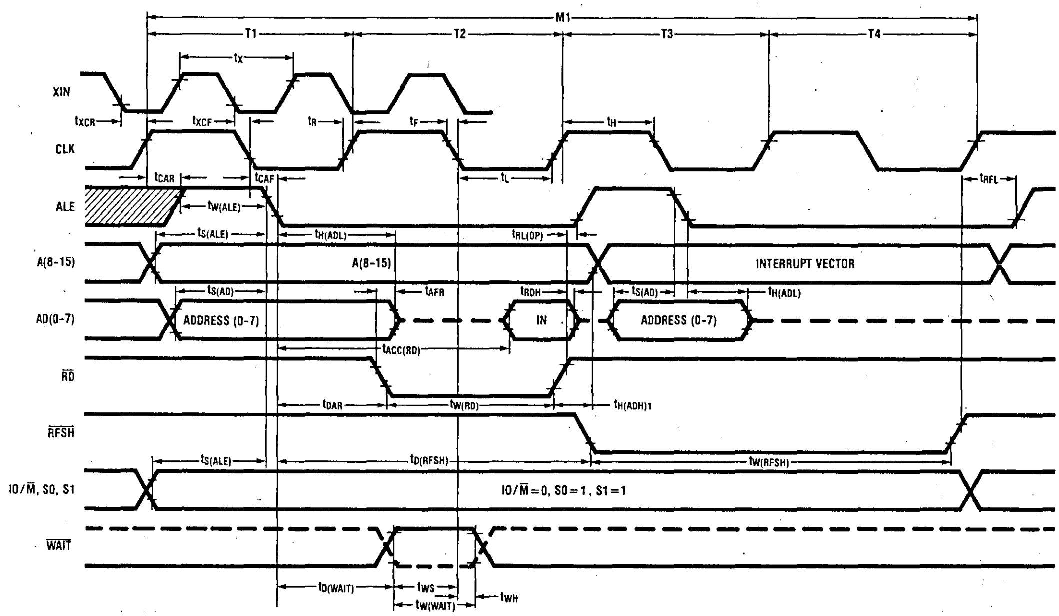
Note 1: Test conditions: t = 1000 ns for NSC800-1, 400 ns for NSC800, 250 ns for NSC800-4.

Note 2: Output timings are measured with a purely capacitive load of 150 pF. The following correction factor can be used for other loads:
$150\ pF < C_L \leq 300\ pF$: +0.25 ns/pF
$50\ pF \leq C_L < 150\ pF$: −0.15 ns/pF.

Note 3: To calculate timing specifications at other values of t use Table I.

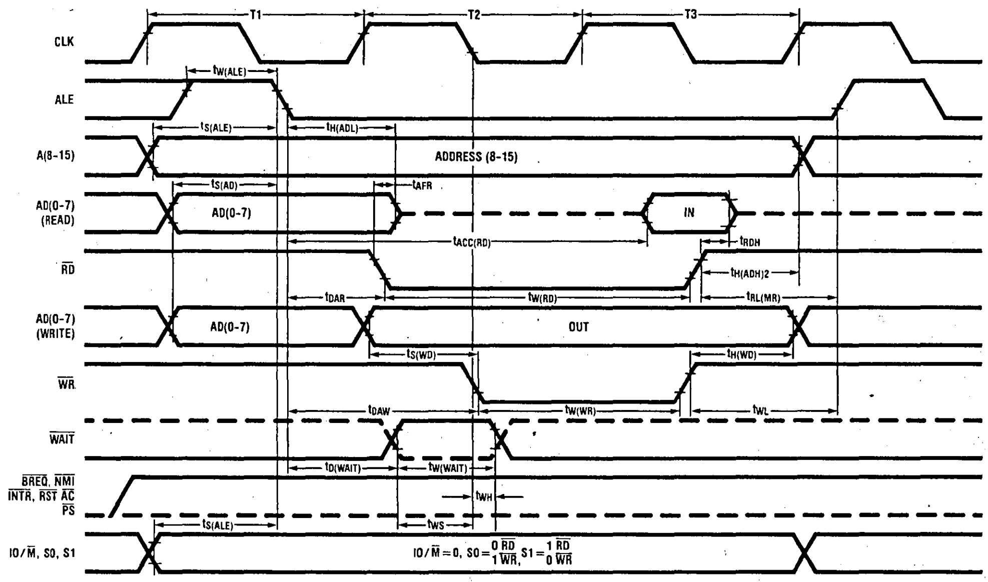
Timing Waveforms

Opcode Fetch Cycle



TL/C/5171-3

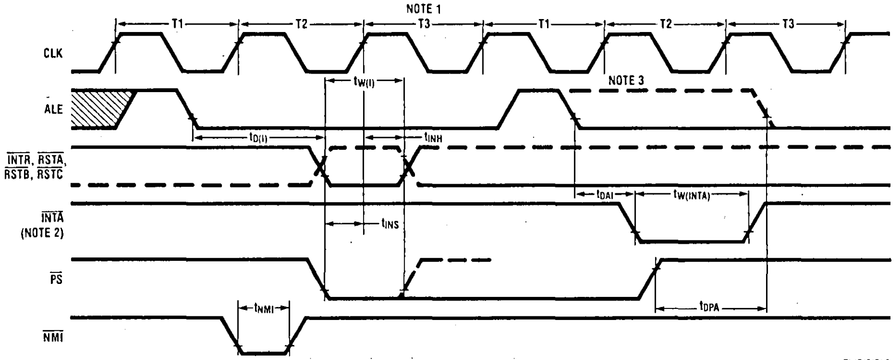
Memory Read and Write Cycle



TL/C/5171-4

Timing Reference

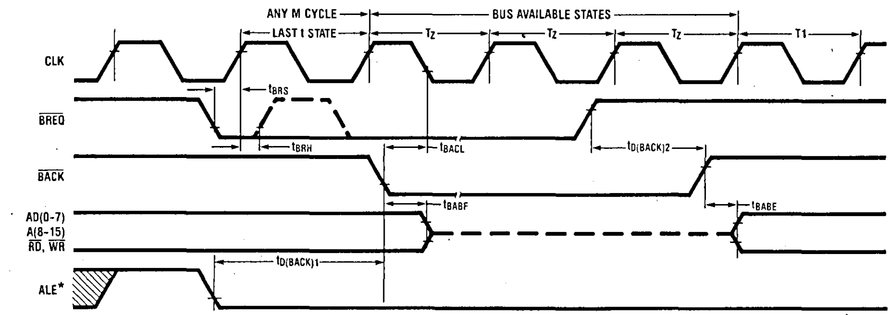
Interrupt—Power-Save Cycle



TL/C/5171-5

Note 1: This t state is the last t state of the last M cycle of any instruction.
Note 2: Response to INTR input.
Note 3: Response to PS input.

Bus Acknowledge Cycle



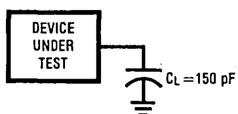
TL/C/5171-6

*Waveform not drawn to proportion. Use only for specifying test points.

AC Testing Input/Output Waveform

TL/C/5171-7

AC Testing Load Circuit



TL/C/5171-8

TABLE I. BUS TIMING AS T DEPENDENT (APPROX.)

Symbol	1/T< 2.5 MHz	2.5 MHz< 1/T< 4.0 MHz		Symbol	1/T< 2.5 MHz	2.5 MHz< 1/T< 4.0 MHz	
t_L	(1/2)T − 10	(1/2)T − 30	Min	$t_{D(RFSH)}$	(3/2 + N)T	(3/2 + N)T − 50	Min
t_H	(1/2)T − 50	(1/2)T − 45	Min	$t_{D(WAIT)}$	(1/2)T + 50	(1/2)T	Max
$t_{ACC(RD)}$	(1 + N)T + 100	(1 + N)T + 50	Max	$t_{H(ADH)2}$	(1/2)T − 100	(1/2)T − 65	Min
t_{BABE}	T	T	Max	$t_{H(ADL)}$	(1/2)T − 100	(1/2)T − 75	Min
t_{BACL}	(1/2)T − 75	(1/2)T − 70	Min	$t_{H(WD)}$	(1/2)T − 100	(1/2)T − 50	Min
t_{DAI}	(1/2)T + 30	(1/2)T − 25	Min	$t_{RL(MR)}$	(1/2)T − 50	(1/2)T − 40	Min
t_{DAR}	(1/2)T + 25	(1/2)T	Min	$t_{S(AD)}$	(1/2)T − 120	(1/2)T − 85	Min
t_{DAR}	(1/2)T + 50	(1/2)T + 35	Max	$t_{S(ALE)}$	(1/2)T − 100	(1/2)T − 75	Min
t_{DAW}	T − 10	T − 30	Min	$t_{S(WD)}$	(1/2)T − 115	(1/2)T − 75	Min
t_{DAW}	T + 10	T	Max	$t_{W(ALE)}$	(1/2)T − 70	(1/2)T − 50	Min
$t_{D(BACK)1}$	(5/2 + N)T	(5/2 + N)T − 25	Min	$t_{W(INTA)}$	(1 + N)T	(1 + N)T − 50	Min
$t_{D(BACK)2}$	(1/2)T	(1/2)T	Min	t_{WL}	(1/2)T − 50	(1/2)T − 35	Min
$t_{D(BACK)2}$	(3/2)T + 100	(3/2)T + 100	Max	$t_{W(RD)}$	(1 + N)T	(1 + N)T − 25	Min
$t_{D(I)}$	(3/2 + N)T − 125	(3/2 + N)T − 125	Max	$t_{W(RFSH)}$	2T − 75	2T − 100	Min
t_{DPA}	(1/2)T	(1/2)T	Min	$t_{W(WR)}$	(1 + N)T	(1 + N)T − 30	Min
t_{DPA}	(3/2)T + 50	(3/2)T + 100	Max				

Note: N is equal to number of WAIT states.

Functional Pin Descriptions

The following describes the function of all NSC800 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Reset Input ($\overline{\text{RESET IN}}$): Active low. Sets A (8–15) and AD (0–7) to TRI-STATE® (high impedance). Clears the contents of PC, I and R registers, disables interrupts, and causes a reset output to be activated.

Bus Request ($\overline{\text{BREQ}}$): Active low. Used when another device is requesting the system bus. $\overline{\text{BREQ}}$ is recognized at the end of the current machine cycle, then A(8–15), AD(0–7), IO/$\overline{\text{M}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ are set to the high impedance mode and the request is acknowledged via the $\overline{\text{BACK}}$ output signal.

Non-Maskable Interrupt ($\overline{\text{NMI}}$): Active low. The non-maskable interrupt, generated by the peripheral device(s), is the highest priority interrupt request line. The interrupt is edge sensitive and only a pulse is required to set an internal flip-flop which generates the internal interrupt request. Since the $\overline{\text{NMI}}$ flip-flop is monitored on the same clock edge as the other interrupts, it must also meet the minimum set-up time spec for the interrupt to be accepted in the current machine instruction. Once the interrupt is accepted the flip-flop is reset automatically. Its execution is independent of the interrupt enable flip-flop. $\overline{\text{NMI}}$ execution involves saving the PC on the stack and automatic branching to restart address X'0066 in memory.

Restart Interrupts A, B, C ($\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, $\overline{\text{RSTC}}$): Active low level sensitive. Restarts generated by the peripherals are recognized at the end of the current instruction if their respective interrupt enable bits and master enable bit are set. Execution is identical to $\overline{\text{NMI}}$ except interrupts are enabled for the following restart addresses:

Name	Restart Address (X')
$\overline{\text{NMI}}$	0066
$\overline{\text{RSTA}}$	003C
$\overline{\text{RSTB}}$	0034
$\overline{\text{RSTC}}$	002C
$\overline{\text{INTR}}$ (Mode 1)	0038

The order of priority is fixed (highest first) as follows:

1) $\overline{\text{NMI}}$ 2) $\overline{\text{RSTA}}$ 3) $\overline{\text{RSTB}}$ 4) $\overline{\text{RSTC}}$ 5) $\overline{\text{INTR}}$

Interrupt Request ($\overline{\text{INTR}}$): Active low level sensitive. An interrupt request input generated by a peripheral device is recognized at the end of the current instruction provided that the interrupt enable and master interrupt enable bits are set. $\overline{\text{INTR}}$ is the lowest priority interrupt request input. Under program control, $\overline{\text{INTR}}$ can be executed in three distinct modes in conjunction with the $\overline{\text{INTA}}$ output.

Wait ($\overline{\text{WAIT}}$): Active low. When set low during $\overline{\text{RD}}$, $\overline{\text{WR}}$ or $\overline{\text{INTA}}$ machine cycles, (during the write machine cycle, wait must be valid prior to write going active), the CPU extends its machine cycle in increments of t (wait) states. The wait machine cycle continues until the $\overline{\text{WAIT}}$ input returns high.

The wait strobe input will be accepted only during machine cycles that have $\overline{\text{RD}}$, $\overline{\text{WR}}$ or $\overline{\text{INTA}}$ strobes and during the machine cycle immediately after an interrupt has been accepted by the CPU. The later cycle has its RD strobe suppressed but it will still accept the wait.

Power-Save ($\overline{\text{PS}}$): Active low. $\overline{\text{PS}}$ is sampled at the end of the current instruction cycle. When $\overline{\text{PS}}$ is low, the CPU stops executing at the end of current instruction and keeps itself in the low-power mode. Normal operation resumes when $\overline{\text{PS}}$ is returned high.

Functional Pin Descriptions (Continued)

OUTPUT SIGNALS

Bus Acknowledge ($\overline{BACK}$): Active low. $\overline{BACK}$ indicates to the bus requesting device that the CPU bus and its control signals are in the TRI-STATE mode. The requesting device may then take control of the bus and its control signals.

Address Bits 8-15 [A(8-15)]: Active high. These are the most significant 8 bits of the memory address during a memory instruction. During an I/O instruction, the port address on the lower 8 bits of address get duplicated onto these 8 bits. During a BREQ/BACK cycle, the A (8-15) bus is in the TRI-STATE mode.

Reset Out (RESET OUT): Active high. When RESET OUT is high, it indicates the CPU is being reset. The signal is normally used to reset the peripheral devices.

Input/Output/Memory (IO/$\overline{M}$): An active high on the IO/$\overline{M}$ output signifies that the current machine cycle is relative to an input/output device. An active low on the IO/$\overline{M}$ output signifies that the current machine cycle is relative to memory. It is TRI-STATE during $\overline{BREQ}/\overline{BACK}$ cycles.

Refresh ($\overline{RFSH}$): Active low. The refresh output indicates that the dynamic RAM refresh cycle is in progress. $\overline{RFSH}$ goes low during T3 and T4 states of all M1 cycles. During the refresh cycle, AD(0-7) has the refresh address and A(8-15) indicates the interrupt vector register I.

Address Latch Enable (ALE): ALE is active only during the T1 state of any M cycle and also T3 state of M1 cycle. The high to low transition of ALE indicates that a valid memory/I-O/refresh address is available on the AD(0-7) lines.

Read Strobe ($\overline{RD}$): Active low. On the trailing edge of the $\overline{RD}$ strobe, data is input to the CPU via the AD(0-7) lines. The $\overline{RD}$ line is in the TRI-STATE mode during $\overline{BREQ}/\overline{BACK}$ cycles.

Write Strobe ($\overline{WR}$): While the $\overline{WR}$ line is low, valid data is output by the CPU on the AD(0-7) lines. The $\overline{WR}$ line is in the TRI-STATE mode during $\overline{BREQ}/\overline{BACK}$ cycles.

Clock (CLK): CLK is an output provided for use as a system clock. The CLK output is a square wave at one half the input frequency.

Interrupt Acknowledge ($\overline{INTA}$): Active low. The interrupt acknowledge output is activated in the M1 cycle (S) immediately following the t state in which the $\overline{INTR}$ input is recognized. [Output is normally used to gate the interrupt response vector from the peripheral controller onto the AD(0-7) lines.] It is used in two of the three interrupt modes. In mode 0, an instruction is gated onto the AD(0-7) line during $\overline{INTA}$. There will be from 1 to 4 $\overline{INTA}$ strobes issued for each mode 0 interrupt. The amount of $\overline{INTA}$ strobes issued is instruction dependent. In mode 2, a single interrupt response vector is gated onto the data bus. In mode 1, $\overline{INTA}$ is not used. In this mode, $\overline{INTR}$ functions like the restart interrupts.

Status (S0, S1): Bus status outputs indicate encoded information regarding the ensuing M cycle as follows:

Machine Cycle	Status			Control	
	S0	S1	IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$
Opcode Fetch	1	1	0	0	1
Memory Read	0	1	0	0	1
Memory Write	1	0	0	1	0
I/O Read	0	1	1	0	1
I/O Write	1	0	1	1	0
Halt*	0	0	0	0	1
Internal Operation*	0	1	0	1	1
Acknowledge of Int**	1	1	0	1	1

*ALE is not suppressed in this cycle.

**This is the cycle that occurs immediately after the CPU accepts an interrupt ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, $\overline{INTR}$, $\overline{NMI}$).

Note 1: During halt, CPU continues to do dummy opcode fetch from location following the halt instruction with a halt status. This is so CPU can continue to do its dynamic RAM refresh.

Note 2: No early status is provided for interrupt or hardware restarts.

INPUT/OUTPUT SIGNALS

Power (V_{CC}): +5V supply.

Ground (GND): 0V reference.

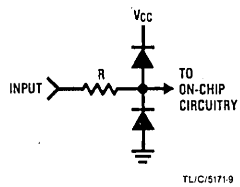
Crystal (XIN, XOUT): XIN may be used as an external clock input.

Multiplexed Address/Data [AD(0-7)]: Active high

At $\overline{RD}$ Time:	Input data to CPU.
At $\overline{WR}$ Time:	Output data from CPU.
At Falling Edge of ALE Time:	Least significant byte of address during memory reference cycle. 8-bit port address during I/O reference cycle.
During $\overline{BREQ}/\overline{BACK}$ Cycle:	High impedance.

Input Protection

All inputs are protected from static charge with diode clamps to both V_{CC} and GND. Normal precautions taken with MOS devices are recommended.



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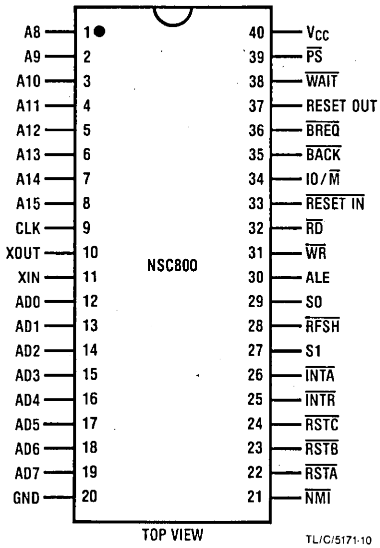
$100\Omega < R < 300\Omega$

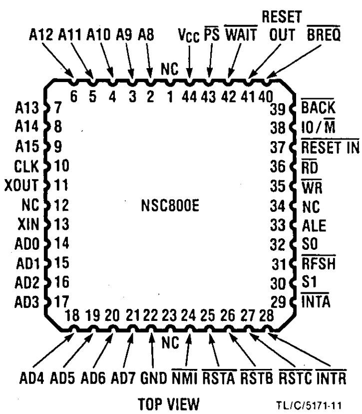
Connection Diagrams

Dual-In-Line Package



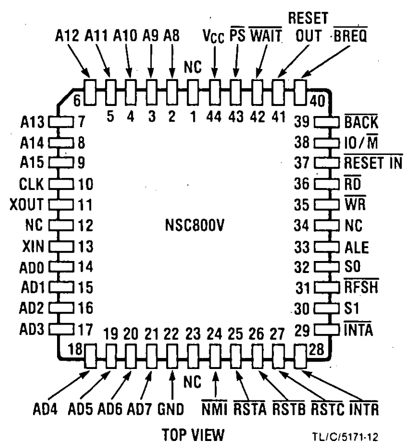
See NS Package D40C, J40A or N40A

E Package



See NS Package ED44A

V Package



See NS Package V44

Timing Control

All necessary timing signals are provided by a single state inverter oscillator contained on the NSC800 chip. The chip operation frequency is equal to one half of the frequency of this oscillator. The oscillator frequency can be controlled by one of the following methods:

1. Leaving the XOUT pin unterminated and driving the XIN pin with an externally generated clock as shown in *Figure 1a*. When driving XIN with a square wave, the minimum duty cycle is 30%–70%, either high or low.
2. Connecting a crystal with the proper biasing network between XIN and XOUT as shown in *Figure 1b*. Recommended crystal is a parallel resonance AT cut crystal.

Resistor capacitor feedback network described in earlier data sheets will not oscillate due to gain of internal inverter circuit. A modification of this circuit by adding two inverters in series between the RC network and XIN will work.

The CPU has a minimum clock frequency input (@ XIN) of 32 kHz, which results in 16 kHz system clock speed. All registers internal to the chip are static, however there is dynamic logic which limits the minimum clock speed. The input clock can be stopped without fear of losing any data or damaging the part. You stop it in the phase of the clock that has XIN low and CLK OUT high. When restarting the CPU, precautions must be taken so that the input clock meets minimum specification. Once started, the CPU will continue operation from the same location at which it was stopped. During DC operation of the CPU, typical current drain will be 2 mA. This current drain can be reduced by placing the CPU in a wait state during an opcode fetch cycle then stopping the clock.

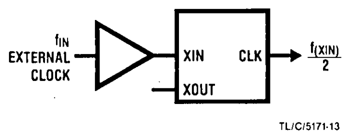
Functional Description

The NSC800 is an 8-bit general purpose microprocessor designed for stand-alone and DMA (direct memory access) applications. A minimum system can be constructed with an NSC800, an NSC810A (RAM I/O Timer) and an NMC27C16 (EPROM).

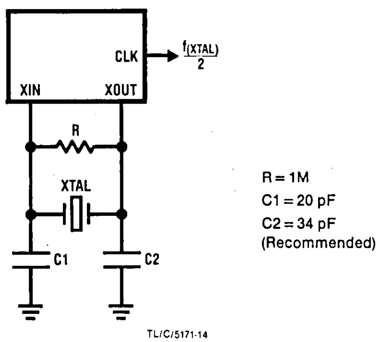
NSC800 uses a multiplexed bus for data and addresses. The 16-bit address bus is divided into a high-order 8-bit address bus that handles bits 8–15 of the address, and a low-order 8-bit multiplexed address/data bus that handles bits 0–7 of the address and bits 0–7 of the data. Strobe outputs from the NSC800 (ALE, $\overline{RD}$ and $\overline{WR}$) indicate when a valid address or data is present on the bus. IO/$\overline{M}$ indicates whether the ensuing cycle accesses memory or I/O.

During an input or output instruction, the CPU duplicates the lower half of the address [AD(0–7)] onto the upper half [A(8–15)]. The eight bits of address will stay on A(8–15) for the entire machine cycle.

Figure 2 illustrates the timing relationship for opcode fetch cycles with and without a wait state. *Figure 3* illustrates the timing relationship for memory read and write cycles with and without a wait state. Input/output cycles with and without a wait state are shown in *Figure 4*. One wait state is automatically inserted into each I/O instruction.



a.



b.

FIGURE 1. Timing Control Configurations

Functional Description (Continued)

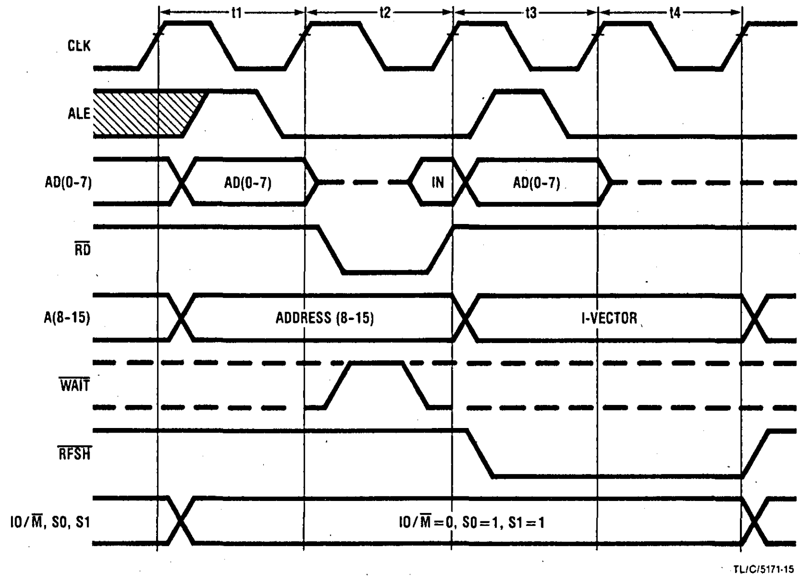


FIGURE 2a. Opcode Fetch Cycles without $\overline{\text{WAIT}}$ States

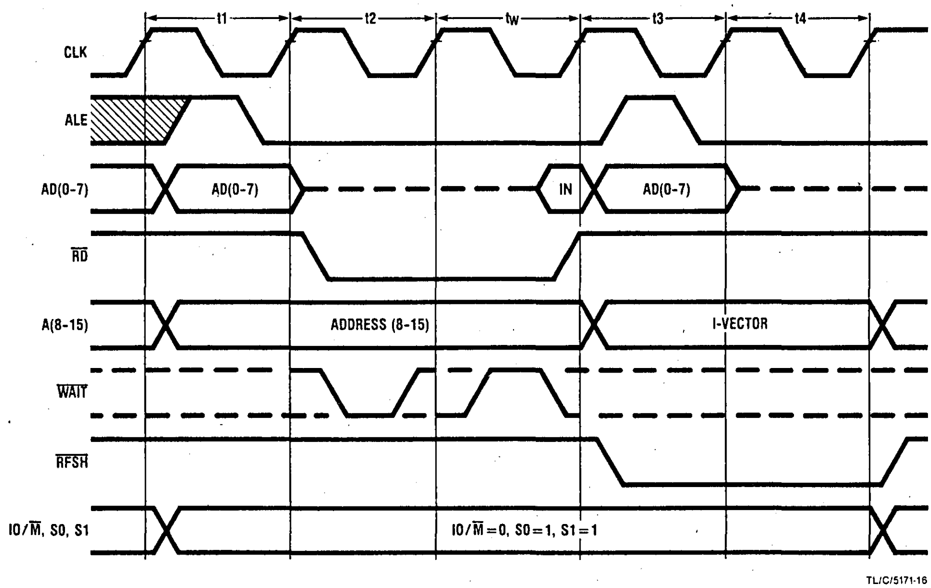


FIGURE 2b. Opcode Fetch Cycles with $\overline{\text{WAIT}}$ States

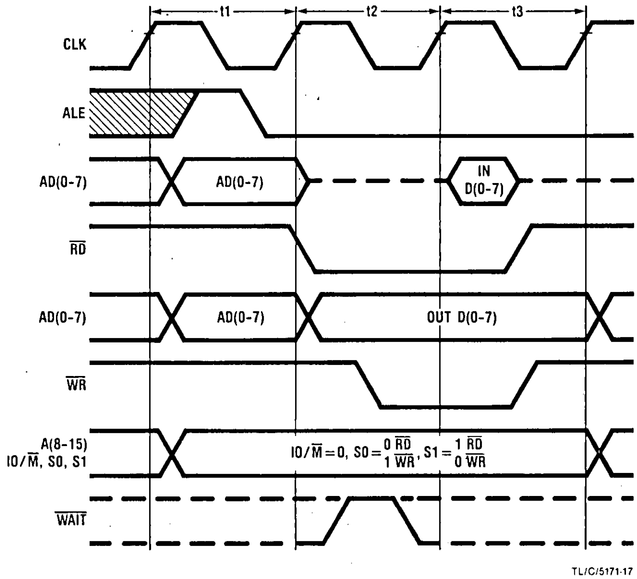


FIGURE 3a. Memory Read/Write Cycles without $\overline{WAIT}$ States

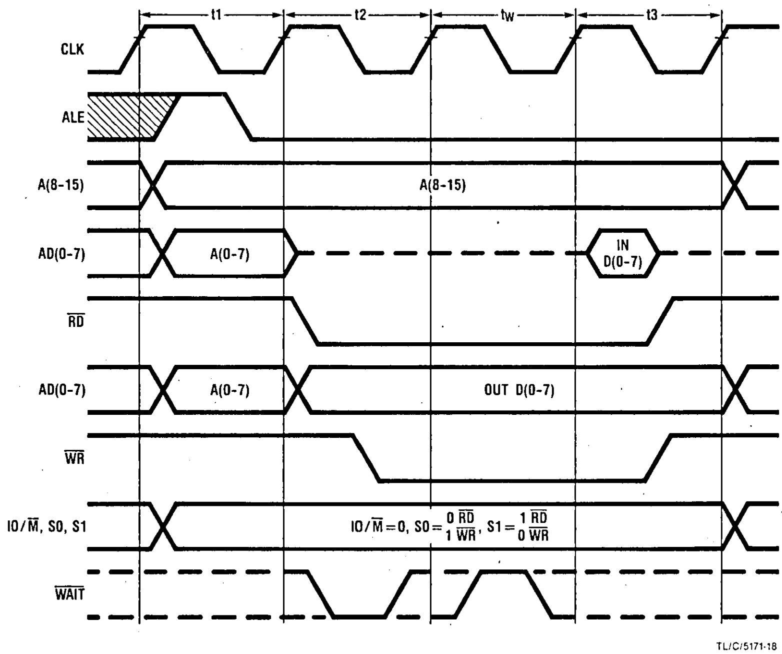


FIGURE 3b. Memory Read and Write with $\overline{WAIT}$ States

Functional Description (Continued)

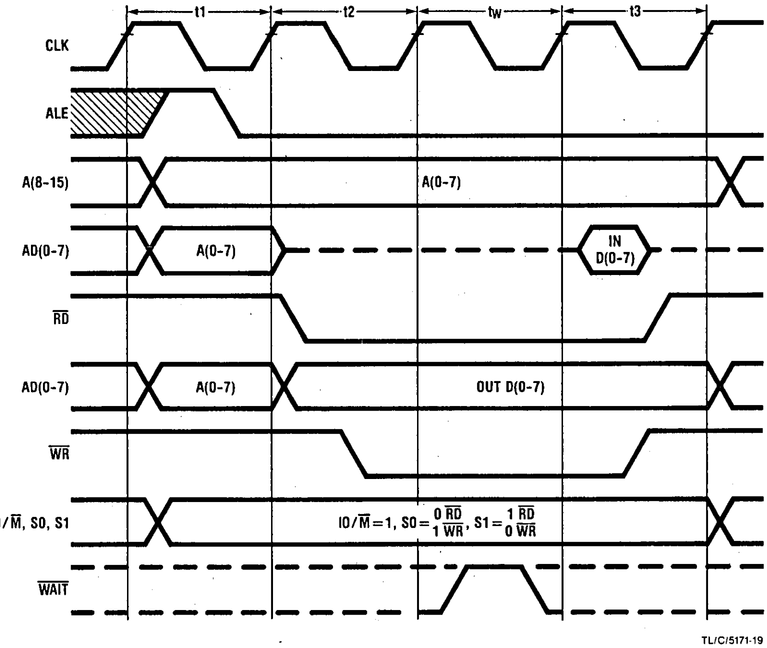
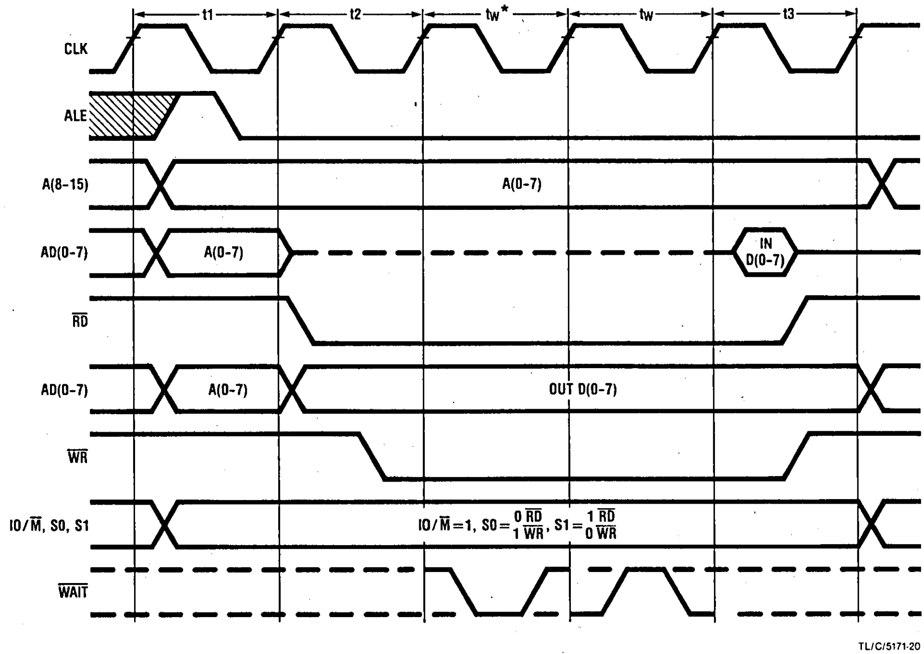


FIGURE 4a. Input and Output Cycles without WAIT States



*WAIT state automatically inserted during IO operation.

FIGURE 4b. Input and Output Cycles with WAIT States

Functional Description (Continued)

INITIALIZATION

The NSC800 and its peripheral components are initialized by $\overline{\text{RESET IN}}$ and RESET OUT. $\overline{\text{RESET IN}}$ input is associated with an on-chip Schmitt trigger that facilitates using an R-C network power-on reset scheme (*Figure 5*).

To ensure proper power-up conditions for the NSC800, the following power-up and initialization procedure is recommended:

1. Apply power (V_{CC} and GND) and set $\overline{\text{RESET IN}}$ active (low). Allow sufficient time (approximately 100 ms if crystal used) for the oscillator and internal clocks to stabilize. $\overline{\text{RESET IN}}$ must remain low for at least 3t state (CLK) times. RESET OUT, following the clock stabilization period, responds by going high, indicating to the system that the NSC800 is being reset. RESET OUT signal becomes available to reset the peripherals.
2. Set $\overline{\text{RESET IN}}$ high, following which the RESET OUT goes low and the CPU initiates the first opcode fetch cycle.

NOTE: *The NSC800 initialization includes: Clear PC to X'0000 (the first opcode fetch, therefore, is from memory location X'0000). Clear registers I (Interrupt Vector Base) and R (Refresh Counter) to X'00. Clear interrupt control register bits IEA, IEB and IEC. The interrupt control bit IEI is set to 1 to maintain INS8080A/Z80A compatibility (see INTERRUPTS for more details). Maskable interrupts are disabled and the CPU enters Interrupt Mode 0. While $\overline{\text{RESET IN}}$ is active (low), the A(8-15) and AD(0-7) lines go to high impedance (TRI-STATE) and all CPU strobes go to the inactive state.*

BUS ACCESS CONTROL

Figure 6 illustrates bus access control in the NSC800. The external device controller produces an active $\overline{\text{BREQ}}$ signal that requests the bus. When the CPU responds with $\overline{\text{BACK}}$ then the bus and related control strobes go to high impedance (TRI-STATE). It should be noted that (1) $\overline{\text{BREQ}}$ is sampled at the last t state of any M machine cycle only. (2) The NSC800 will not acknowledge any interrupt/restart requests, and will not perform any dynamic RAM refresh functions until after $\overline{\text{BREQ}}$ input signal is inactive high. (3) $\overline{\text{BREQ}}$ signal has priority over all interrupt request signals, should $\overline{\text{BREQ}}$ and interrupt request become active simultaneously.

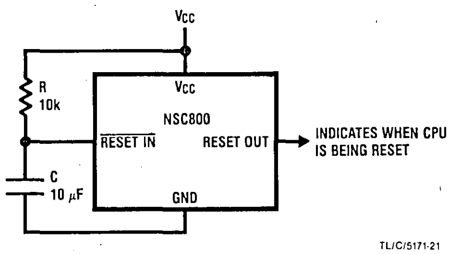
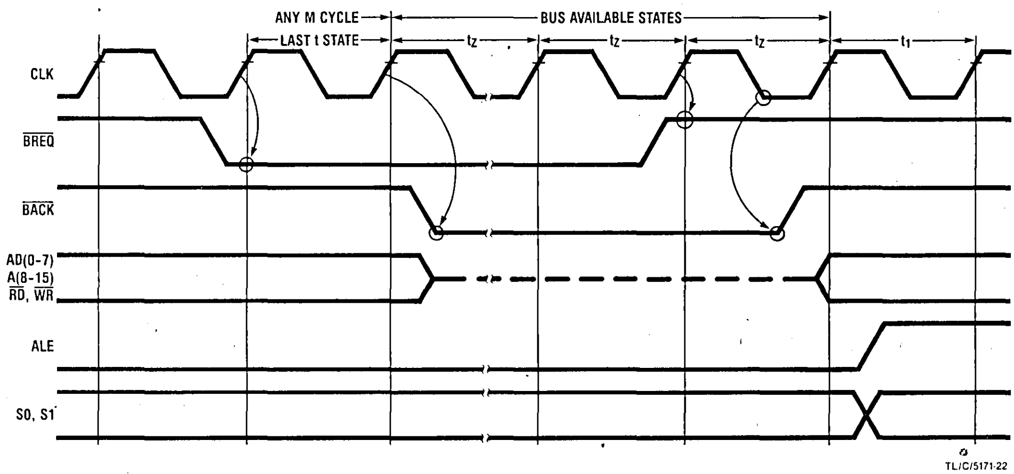


FIGURE 5. Power-On Reset



*S0, S1 during $\overline{\text{BREQ}}$ will indicate same machine cycle as during cycle when $\overline{\text{BREQ}}$ was accepted.
t_Z = time states bus and control signals are in high impedance mode.

FIGURE 6. Bus Acknowledge Cycle

Functional Description (Continued)

REGISTER CONFIGURATION

The NSC800 contains 22 programmable registers as shown in *Figure 7.* The CPU working registers are arranged in two 8-register configurations, each of which includes an 8-bit accumulator, a flag register, and six general purpose 8-bit registers. Only one 8-bit register set may be active at any given moment. However, simple instructions exist that allow the programmer to exchange the active and alternate register sets.

It should also be noted that the six 8-bit general purpose registers (B, C, D, E, H, and L) can be accessed as 16-bit registers (BC, DE, and HL). The functions of these become apparent in the instruction set description.

CPU Main Working Register Set

Accumulator	(8)	Flags F	(8)
Register B	(8)	Register C	(8)
Register D	(8)	Register E	(8)
Register H	(8)	Register L	(8)

CPU Alternate Working Register Set

Accumulator A′	(8)	Flags F′	(8)
Register B′	(8)	Register C′	(8)
Register D′	(8)	Register E′	(8)
Register H′	(8)	Register L′	(8)

CPU Dedicated Registers

Index Register IX	(16)
Index Register IY	(16)
Interrupt Vector Register I	(8)
Memory Refresh Register R	(8)
Stack Pointer SP	(16)
Program Counter PC	(16)

FIGURE 7. Register Configuration

DEDICATED REGISTERS

Program Counter (PC): The program counter contains the 16-bit address of the current instruction being fetched from memory. The PC is incremented after its contents have been transferred to the address lines. When a program jump occurs, the new address is placed in the PC, overriding the incrementer.

Stack Pointer (SP): The stack pointer contains the 16-bit address of the current top of a stack located in external system RAM memory. The external stack memory is organized as a last-in, first-out (LIFO) file. The stack allows simple implementation of multiple level interrupts, virtually unlimited subroutine nesting and simplification of many types of data manipulation.

Index Registers (IX and IY): The two 16-bit index registers hold a 16-bit base address used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer.

Interrupt Page Address Register (I): The NSC800 CPU can indirectly call any memory location in response to a mode 2 interrupt. The I register is used to store the high-order 8 bits of the address. The low-order 8 bits are supplied by the interrupting peripheral. This feature allows interrupt routines to be dynamically located anywhere in memory with minimal access time to the routine.

Memory Refresh Register (R): The NSC800 CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. This 8-bit register is automatically incremented after each instruction fetch. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer.

ACCUMULATORS AND FLAG REGISTERS

The CPU includes two 8-bit accumulators and two associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operation. The flag register indicates specific conditions for 8-bit or 16-bit operations.

FLAG REGISTERS (F,F′)

The two NSC800 flag registers each contain six status bits that are set or reset (cleared) by various CPU operations (*Figure 8*). Four of these bits (carry, zero, sign, and parity/overflow flags) can be tested by the programmer. The descriptions of the flags follow.

Carry Flag (C): This flag is set by the carry from the highest order bit of the accumulator during an add instruction or a borrow generated during a subtraction instruction. Specific shift and rotate instructions also affect this bit.

Zero Flag (Z): This flag is set when a zero is loaded into the accumulator as a result of an operation. Otherwise it remains clear.

Sign Flag (S): This flag stores the state of bit 7 (the sign bit) in the accumulator after an arithmetic operation. This flag is intended to be used with signed numbers.

Parity/Overflow Flag (P/V): During logical operations this flag is set when the parity of the result is even and reset when it is odd. It represents overflow when signed two's complement arithmetic operations are performed. An overflow occurs when the resultant of a two's complement operation (in the accumulator) is out of range.

The two non-testable flag register bits used for BCD arithmetic are:

Half Carry (H): This flag indicates a BCD carry or borrow result from the least significant four bits of an operation; when using the DAA (Decimal Adjust Accumulator Instruction), it is used to correct the result of a previously packed decimal add or subtract.

Functional Description (Continued)

Add/Subtract Flag (N): Since the algorithm for correcting BCD operations is different for addition or subtraction, this flag specifies what type of instruction was executed last in order that the DAA operation will be correct for either operation.

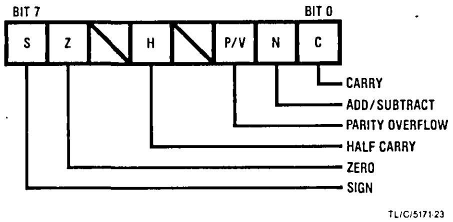


FIGURE 8. Flag Register

INTERRUPTS

The NSC800 has five interrupt/restart inputs, four are maskable ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and $\overline{INTR}$) and one is non-maskable ($\overline{NMI}$). $\overline{NMI}$, having the highest priority of all interrupts, is always serviced and cannot be disabled by the user. After recognizing an active input on $\overline{NMI}$, the CPU stops before the next instruction, pushes the PC onto the stack, and jumps to address X'0066, where the user's interrupt service routine is located (i.e., restart to memory location X'0066). $\overline{NMI}$ is intended for interrupts requiring immediate attention, such as power-down, control panel, etc.

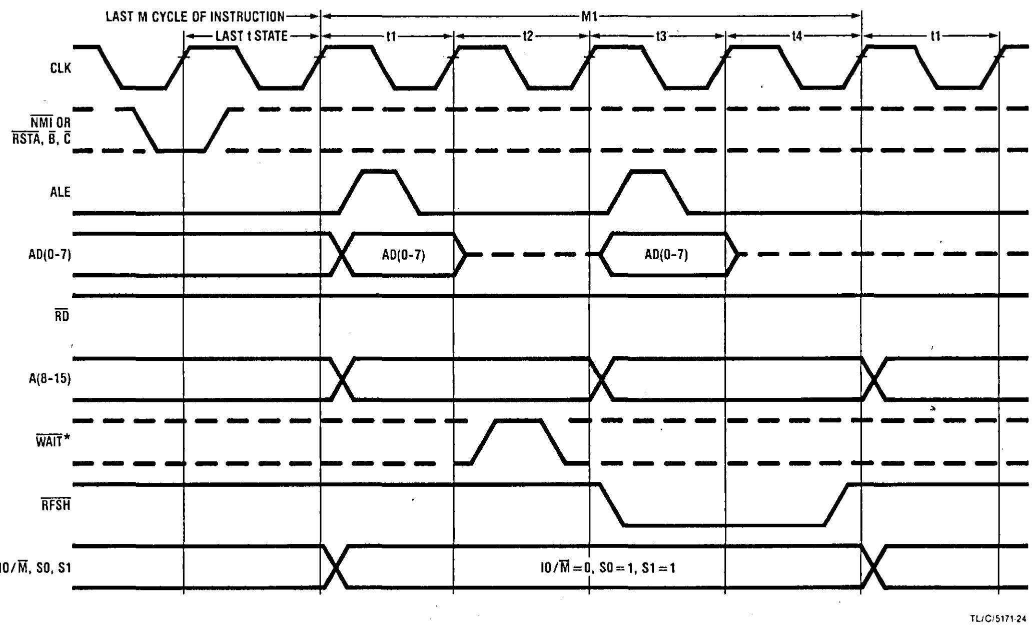
$\overline{RSTA}$, $\overline{RSTB}$ and $\overline{RSTC}$ are restart inputs, which, if enabled, execute a restart to memory location X'003C, X'0034, and X'002C, respectively. Note that the CPU response to the $\overline{NMI}$ and $\overline{RST}$ ($\overline{A}$, $\overline{B}$, $\overline{C}$) request input is basically identical. Unlike $\overline{NMI}$, however, restart request inputs must be enabled.

Figure 9 illustrates $\overline{NMI}$ and $\overline{RST}$ interrupt machine cycles. M1 cycle will be a dummy opcode fetch cycle followed by M2 and M3 which are stack push operations. The following instruction will then start from the interrupts restart location.

The NSC800 also provides one more general purpose interrupt request input, $\overline{INTR}$. When enabled, the CPU responds to $\overline{INTR}$ in one of the three modes defined by instruction IM0, IM1, and IM2 for modes 0, 1, and 2, respectively. Following reset, the CPU automatically sets itself in mode 0.

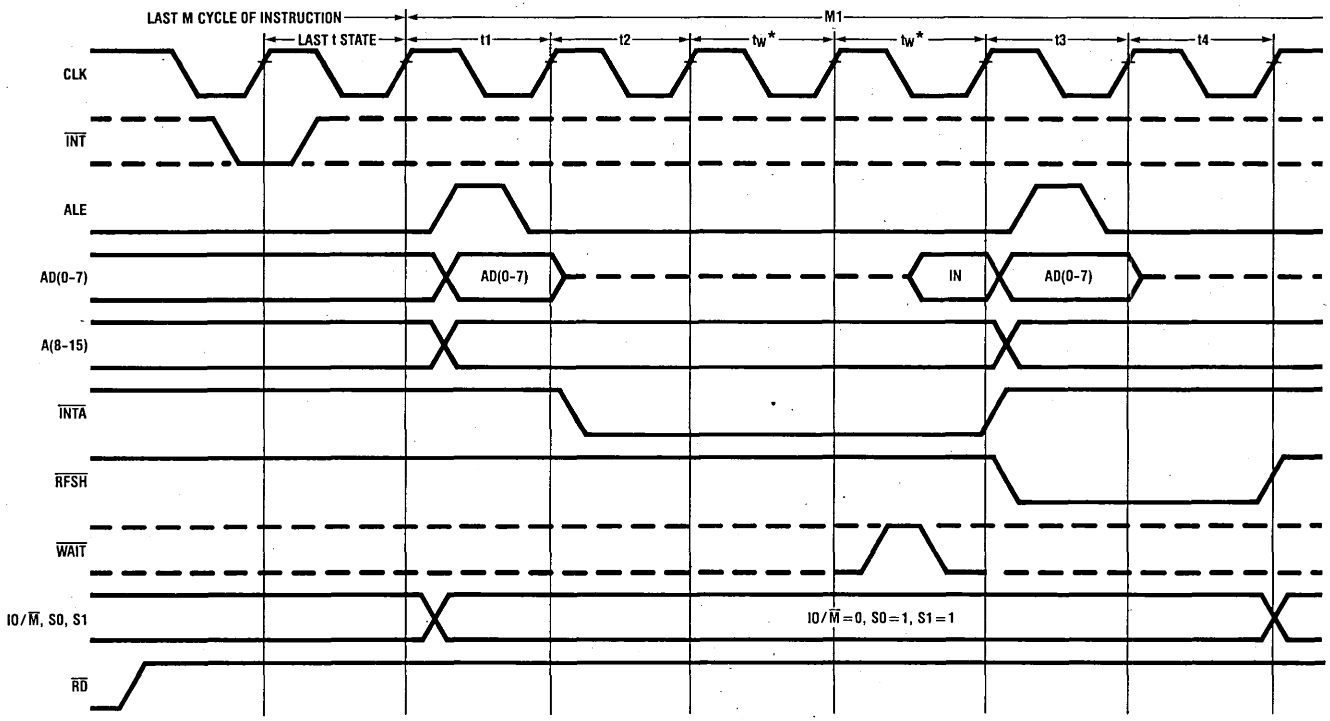
Interrupt ($\overline{INTR}$) Mode 0: Similar to INS8080A mode. The CPU responds to an interrupt request by providing an INTA (interrupt acknowledge) strobe, which can be used to gate an instruction from a peripheral onto the data bus. Two wait states are automatically inserted by the CPU during the first $\overline{INTA}$ cycle to allow the interrupting device (or its controller) ample time to gate the instruction and determine external priorities. (*Figure 10*). This can be any instruction from one to four bytes. The most popular instruction would be a one-byte call (restart instruction) or a three-byte call (CALL NN instruction). If it is a three-byte call, the CPU issues a total of three $\overline{INTA}$ strobes. The last two read NN (which do not include wait states).

Interrupt ($\overline{INTR}$) Mode 1: Similar to the restart interrupts except the restart location is X'0038 (*Figure 9*).



*This is the only machine cycle that does not have an $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$ strobe but will accept a wait strobe.

FIGURE 9. Non-Maskable and Restart Interrupt Machine Cycle



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*t_W is the CPU generated WAIT state in response to an interrupt request.

FIGURE 10. Interrupt Acknowledge Machine Cycle

Interrupt ($\overline{\text{INTR}}$) Mode 2: With this mode, the programmer maintains a table that contains the 16-bit starting address of every interrupt service routine. This table may be located anywhere in memory. When the mode 2 interrupt is accepted (*Figure 11*), a 16-bit pointer must be formed to obtain the desired interrupt service routine starting address from the table. The upper 8 bits of this pointer are from the contents of the I register, which has been previously loaded with the desired value by the programmer. The lower 8 bits of the pointer are supplied by the interrupting device with the low-order bit forced to zero. The pointer is used to get two adjacent bytes from the interrupt service routine starting address table to complete 16-bit service routine starting address. The first byte of each entry in the table is the least significant (low-order) portion of the address. The programmer must obviously fill this table with the desired addresses before any interrupts are to be accepted.

Note that this table can be changed at any time to allow peripherals to be serviced by different service routines. Once the interrupting device supplies the lower portion of the pointer, the CPU automatically pushes the program counter onto the stack, obtains the starting address from the table and does a jump to this address.

The interrupts have fixed priorities built into the NSC800 as:

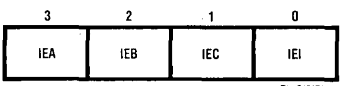
$\overline{\text{NMI}}$	(Highest Priority)
$\overline{\text{RSTA}}$	
$\overline{\text{RSTB}}$	
$\overline{\text{RSTC}}$	
$\overline{\text{INTR}}$	(Lowest Priority)

ENABLING INTERRUPTS

$\overline{\text{NMI}}$, being a non-maskable interrupt request, is executed as it occurs and can never be disabled.

The maskable interrupt inputs ($\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, $\overline{\text{RSTC}}$, and $\overline{\text{INTR}}$) are enabled under program control through the use of the interrupt control register and enable/disable interrupt instruction.

The appropriate interrupt control bits in 4-bit interrupt control register (IEA, IEB, IEC, and IEI) must be enabled in conjunction with IFF1 and IFF2, before the maskable $\overline{\text{INTR}}$ and $\overline{\text{RST}}$ $\overline{\text{A}}$, $\overline{\text{B}}$, $\overline{\text{C}}$ can be accepted by the CPU.



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The interrupt control register is an on-chip write only output port located at port address X'BB. It can only be written to by either the OUT (C), r or OUT (N), A instructions (for example OUTI instruction will not affect Interrupt Control Register). Its contents are:

Bit	Name	Function
0	IEI	Interrupt Enable for $\overline{\text{INTR}}$
1	IEC	" " " $\overline{\text{RSTC}}$
2	IEB	" " " $\overline{\text{RSTB}}$
3	IEA	" " " $\overline{\text{RSTA}}$

For example: In order to enable $\overline{\text{RSTB}}$, CPU interrupts must be enabled and IEB must be set.

At reset, IEI bit is set and other mask bits, IEA, IEB, IEC are cleared. This maintains the software compatibility between NSC800 and INS8080A (or Z80A).

Execution of an IO block move instruction will not affect the state of the interrupt control bits. The only two instructions that will modify this write only register are OUT (C), r and OUT (N), A.

POWER-SAVE FEATURE

The NSC800 provides a unique power-save mode by the means of the $\overline{\text{PS}}$ pin. $\overline{\text{PS}}$ input is sampled at the last t state of the last M cycle of an instruction. After recognizing an active (low) level on $\overline{\text{PS}}$, the NSC800 stops its internal clocks, thereby reducing its power dissipation to one half of operating power, yet maintaining all register values and internal control status. The NSC800 keeps its oscillator running, and makes the CLK signal available to the system. When in power-save the ALE strobe will be stopped high and the address lines [AD(0–7), A(8–15)] will indicate the next machine address. When $\overline{\text{PS}}$ is returned high, the opcode fetch (or M1 cycle) of the CPU begins in a normal manner. Note this M1 cycle could also be an interrupt acknowledge cycle if the NSC800 was interrupted simultaneously with $\overline{\text{PS}}$. *Figure 12* illustrates the power-save feature.

In the event $\overline{\text{BREQ}}$ is asserted (low) at the end of an instruction cycle and $\overline{\text{PS}}$ is active simultaneously, the following occurs:

1. The NSC800 will go into $\overline{\text{BACK}}$ cycle
2. Upon completion of $\overline{\text{BACK}}$ cycle if $\overline{\text{PS}}$ is still active the CPU will go into power-save mode.

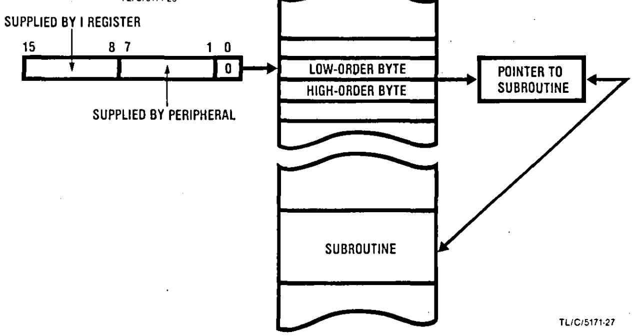

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FIGURE 11. Interrupt Mode 2

Timing Waveforms (Continued)

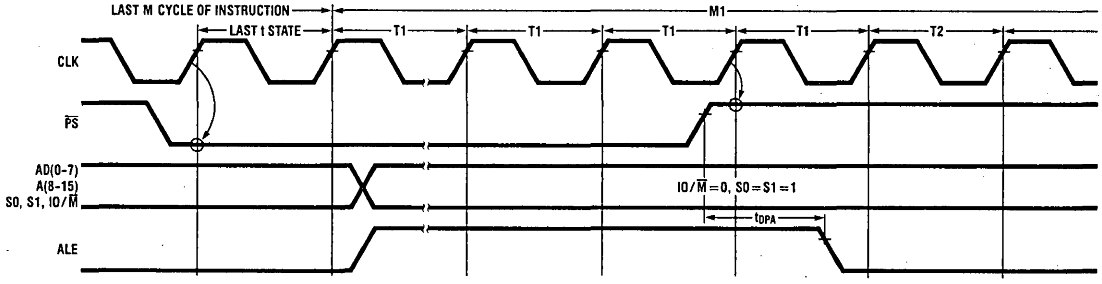


FIGURE 12. NSC800 Power-Save

Instruction Set

In the following instruction set listing, the notation used is shown below.

b: Used in instructions employing bit mode addressing to designate one bit in a register or memory location.

cc: Designates condition codes used in conditional Jumps, Calls, and Return instructions; may be

NZ = Non Zero (Z Flag = 0)
Z = Zero (Z Flag = 1)
NC = Non Carry (C Flag = 0)
C = Carry (C Flag = 1)
PO = Parity Odd or No Overflow (P/V = 0)
PE = Parity Even or Overflow (P/V = 1)
P = Positive (S = 0)
M = Negative (S = 1)

d: Used in instructions employing relative or indexed modes of addressing to designate 8-bit signed 2's complement displacement.

kk: Subset of cc condition codes used in conjunction with conditional relative jumps; may be NZ, Z, NC or C.

m1: Used in instructions employing register indirect or indexed modes of addressing; may be (HL), (IX + d), or (IY + d).

m2: Used in instructions employing register indirect or direct modes of addressing; may be (BC), (DE), or (nn).

n: Any 8-bit binary number.

nn: Any 16-bit binary number.

pp: Used in 16-bit arithmetic instructions employing register modes of addressing; may be BC, DE, SP, or register designated as destination operand.

qq: Used in instructions employing register modes of addressing; may be BC, DE, HL, AF, IX, or IY.

r: Used in instructions employing register mode of addressing; may be A, B, C, D, E, H, or L.

rr: Used in instructions employing register mode of addressing; may be BC, DE, HL, SP, IX, or IY.

ss: Used in instructions employing register mode of addressing; may be HL, IX, or IY.

T: Used in restart instructions employing modified page zero addressing mode; may take on hex values of 0, 8, 10, 18, 20, 28, 30, or 38.

X_L: Subscript L indicates the low-order byte of a 16-bit register.

X_H: Subscript H indicates the high-order byte of a 16-bit register.

( ): Parentheses indicate the contents are considered a pointer to a memory or I/O location.

8-Bit Loads

REGISTER TO REGISTER

Mnemonic	Description	Operation
LD r_d, r_s	Load register r_d with r_s	$r_d \leftarrow r_s$
LD A, I	Load ACC with register I	A←I
LD I, A	Load register I with ACC	I←A
LD A, r	Load ACC with register R	A←r
LD r, A	Load register R with ACC	r←A
LD r, n	Load register r with immediate data n	r←n

REGISTER TO MEMORY

Mnemonic	Description	Operation
LD m1, r	Load memory from register r	m1←r
LD m2, A	Load memory from ACC	m2←A
LD m1, n	Load memory with immediate data n	m1←n

MEMORY TO REGISTER

Mnemonic	Description	Operation
LD r, m1	Load register r from memory	r←m1
LD A, m2	Load ACC from memory	A←m2

16-Bit Loads

REGISTER TO REGISTER

Mnemonic	Description	Operation
LD rr, nn	Load register rr with immediate data nn	rr←nn
LD SP, ss	Load SP register with register ss	SP←ss

REGISTER TO MEMORY

Mnemonic	Description	Operation
LD (nn), rr	Load memory location nn with 16 bit register rr	(nn)←rr_L (nn + 1)←rr_H
PUSH qq	Push contents of 16-bit register qq onto memory stack	(SP − 1)←qq_H (SP − 2)←qq_L SP←SP − 2

MEMORY TO REGISTER

Mnemonic	Description	Operation
LD rr, (nn)	Load 16-bit register rr from memory location nn	rr_L←(nn) rr_H←(nn + 1)
POP qq	Pop contents of stack to register qq	qq_L←(SP) qq_H←(SP + 1) SP←SP + 2

8-Bit Arithmetic

REGISTER ADDRESSED ARITHMETIC

Mnemonic	Description	Operation
ADD A, r	Add contents of register r to ACC	A←A + r
ADC A, r	Add with carry contents of register r to ACC	A←A + r + CY
SUB r	Subtract contents of register r from ACC	A←A − r
SBC A, r	Subtract with carry contents of register r from ACC	A←A − r − CY
AND r	Logically AND contents of register r with ACC	A←A ∧ r
OR r	Logically OR contents of register r with ACC	A←A ∨ r
XOR r	Exclusive OR contents of register r with ACC	A←A ∀ r
CP r	Compare contents of register r to ACC	A:r Z flag←1 if A = r else Z Flag←0
INC r	Increment contents of register r	r←r + 1
DEC r	Decrement contents of register r	r←r − 1
DAA	Decimal adjust ACC	(ACC adjust for BCD)
CPL	Complement ACC (1's complement)	A←A
NEG	Negate ACC (2's complement)	A←0 − A
CCF	Complement carry flag	CY←CY
SCF	Set carry flag	CY←1

IMMEDIATE ADDRESSING MODE ARITHMETIC

Mnemonic	Description	Operation
ADD A, n	Add number n to ACC	A←A + n
ADC A, n	Add with carry number n to ACC	A←A + n + CY
SUB n	Subtract number n from ACC	A←A − n
SBC A, n	Subtract with carry number n from ACC	A←A − n − CY
AND n	AND number n with ACC	A←A ∧ n
OR n	OR number n with ACC	A←A ∨ n
XOR n	Exclusive OR number n with ACC	A←A ∀ n
CP n	Compare number n to ACC	A: n Z flag←1 if A = n else Z Flag←0

MEMORY ADDRESSED ARITHMETIC

Mnemonic	Description	Operation
ADD A, m1	Add memory to ACC	A←A + m1
ADC A, m1	Add with carry memory to ACC	A←A + m1 + CY
SUB m1	Subtract memory from ACC	A←A − m1
SBC A, m1	Subtract with carry memory from ACC	A←A − m1 − CY
AND m1	AND memory with ACC	A←A ∧ m1
OR m1	OR memory with ACC	A←A ∨ m1
XOR m1	Exclusive OR memory with ACC	A←A ∀ m1
CP m1	Compare memory with ACC	A: m1 Z flag←1 if A = r else Z Flag←0
INC m1	Increment memory	m1←m1 + 1
DEC m1	Decrement memory	m1←m1 − 1

16-Bit Arithmetic

REGISTER ADDRESSED ARITHMETIC

Mnemonic	Description	Operation
ADD ss, pp	Add 16-bit register pp to 16-bit register ss	ss←ss + pp
ADC HL, pp	Add with carry 16-bit register pp to HL	HL←HL + pp + CY
SBC HL, pp	Subtract with carry 16-bit register pp from HL	HL←HL − pp − CY
INC rr	Increment 16-bit register rr	rr←rr + 1
DEC rr	Decrement 16-bit register rr	rr←rr − 1

Bit Set, Reset, and Test

REGISTER

Mnemonic	Description	Operation
SET b, r	Set bit b in register r	$r_b \leftarrow 1$
RES b, r	Reset bit b in register r	$r_b \leftarrow 0$
BIT b, r	Test bit b in register r	$Z \leftarrow r_b$

MEMORY

Mnemonic	Description	Operation
Set b, m1	Set bit b in memory location m1	m1b←1
RES b, m1	Reset bit b in memory location m1	m1b←0
BIT b, m1	Test bit b in memory location m1	Z←m1b

Exchanges

REGISTER/REGISTER

Mnemonic	Description	Operation
EX DE, HL	Exchange contents of DE and HL register	DE↔HL
EX AF, AF1	Exchange contents of A and F registers with A1 and F1 registers	AF↔AF'
EXX	Exchange contents of BC, DE and HL registers with corresponding alternate registers	BC↔BC' DE↔DE' HL↔HL'

REGISTER/MEMORY

Mnemonic	Description	Operation
EX (SP), ss	Exchange top of stack with 16-bit register ss	$(SP) \leftrightarrow ss_L$ $(SP+1) \leftrightarrow ss_H$

Memory Block Moves and Searches

Block move and search instructions (such as LDIR and INIR) insert a dummy instruction fetch after each cycle to keep refresh going.

SINGLE OPERATIONS

Mnemonic	Description	Operation
LDI	Move data from memory location (HL) to memory location (DE), increment memory pointers, and decrement byte counter BC.	(DE)←(HL) DE←DE+1 HL←HL+1 BC←BC−1
LDD	Move data from memory location (HL) to memory location (DE), and decrement memory pointer and byte counter BC.	(DE)←(HL) DE←DE−1 HL←HL−1 BC←HL−1
CPI	Compare data in memory location (HL) to ACC, increment memory pointer and decrement byte counter BC.	A−(HL) HL←HL+1 BC←BC−1
CPD	Compare data in memory location (HL) to ACC and decrement memory pointer and byte counter BC.	A−(HL) HL←HL−1 BC←BC−1

REPEAT OPERATIONS

Mnemonic	Description	Operation
LDIR	Move data from memory location (HL) to memory location (DE), increment memory pointers, decrement byte counter BC, repeat until BC=0	(DE)←(HL) DE←DE+1 HL←HL+1 BC←BC−1 Repeat until BC=0
LDDR	Move data from memory location (HL) to memory location (DE), decrement memory pointers and byte counter BC, repeat until BC=0	(DE)←(HL) DE←DE−1 HL←HL−1 BC←BC−1 Repeat until BC=0
CPIR	Compare data in memory location (HL) to ACC, increment memory pointer, decrement byte counter BC, repeat until BC=0 or (HL)=A	A−(HL) HL←HL+1 BC←BC−1 Repeat until BC=0 or (HL)=A
CPDR	Compare data in memory location (HL) to ACC, decrement memory pointer and byte counter BC, repeat until BC=0 or (HL)=A	A−(HL) HL←HL−1 BC←BC−1 Repeat until BC=0 or (HL)=A

Input/Output

Due to the multiplexed bus structure, the NSC800 handles the address bus differently than the Z80 during input and output instructions. The NSC800 duplicates the port address on the upper and lower halves of the address.

Mnemonic	Description	Operation
IN A, (n)	Input from I/O device at address n to ACC	A←(n)
OUT (n), A	Output to I/O device at address n from ACC	(n)←A
IN r, (C)	Input from I/O device at address (C) to register	r←(C)
OUT (C), r	Output to I/O device at address (C) from register	(C)←r
INI	Input from I/O device at address (C) to memory location (HL), increment pointer, and decrement B counter	(HL)←(C) HL←HL+1 B←B−1

Input/Output (Continued)

Mnemonic	Description	Operation
OUTI	Output to I/O at address (C) from memory location (HL), increment pointer, and decrement B counter	(C)←(HL) HL←HL+1 B←B−1
IND	Input from I/O device at address (C) to memory location (HL) and decrement pointer, and B counter	(HL)←(C) HL←HL−1 B←B−1
OUTD	Output to I/O device at address (C) from memory location (HL) and decrement pointer and B counter	(C)←(HL) HL←HL−1 B←B−1
INIR	Input from I/O device at address (C) to memory location (HL), increment pointer, decrement B counter, and repeat until B=0	(HL)←C HL←HL+1 B←B−1 Repeat until B=0
OUTIR	Output to I/O device at address (C) from memory location (HL), increment pointer, decrement B counter, and repeat until B=0	(C)←(HL) HL←HL+1 B←B−1 Repeat until B=0
INDR	Input from I/O device at address (C) to memory location (HL), decrement pointer and B counter, and repeat until B=0	(HL)←(C) HL←HL−1 B←B−1 Repeat until B=0
OUTDR	Output to I/O device at address (C) from memory location (HL), decrement pointer and B counter, and repeat until B=0	(C)←(HL) HL←HL−1 B←B−1 Repeat until B=0

CPU Control

Mnemonic	Description	Operation
NOP	No operation	
HALT*	Halt processor	
DI	Disable Interrupts	
EI	Enable Interrupts	
IM 0	Set Interrupt Mode 0	
IM 1	Set Interrupt Mode 1	
IM 2	Set Interrupt Mode 2	

* Halt instruction locks CPU into an endless cycle of instruction fetches until CPU is reset or interrupted. Therefore dynamic memory refresh continues to run.

Program Control

JUMPS

Mnemonic	Description	Operation
JP nn	Unconditional jump direct to nn	PC←nn
JP (ss)	Unconditional jump indirect via ss register	PC←ss
JP cc, nn	Conditionally jump direct to nn if cc is true	If cc true, PC←nn, else continue
JR d	Unconditional jump to PC+d	PC←PC+d
JR kk, d	Conditionally jump PC+d if kk is true	If kk true, PC←PC+d
DJNZ, d	Decrement B register and jump to PC+d if B≠0, otherwise continue	B←B−1 if B=0 PC←PC+d

CALLS

Mnemonic	Description	Operation
CALL nn	Unconditional call to subroutine at location nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ PC←nn
CALL cc, nn	Conditional call to subroutine at location nn if cc true	If cc true, $(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ PC←nn, else continue

RETURNS

Mnemonic	Description	Operation
RET	Unconditonal return from subroutine	$PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$
RET cc	Conditional return from subroutine	If cc true: $PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$ else continue
RETI	Return from interrupt	$PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$
RETN	Return from non-maskable interrupt	$PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$ Restore interrupt enable status

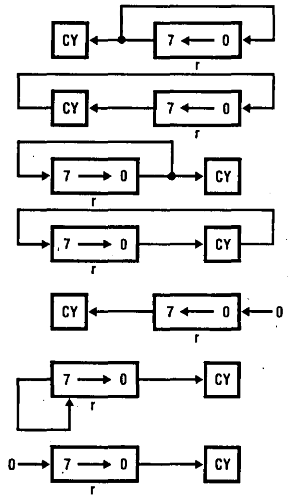
RESTARTS

Mnemonic	Description	Operation
RST T	Interrupt to location T	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ PC←T

Rotate and Shift

REGISTER MNEMONIC	DESCRIPTION
RLC r	ROTATE REGISTER r LEFT CIRCULAR
RL r	ROTATE REGISTER r LEFT THROUGH CARRY
RRC r	ROTATE REGISTER r RIGHT CIRCULAR
RR r	ROTATE REGISTER r RIGHT THROUGH CARRY
SLA r	SHIFT REGISTER r LEFT ARITHMETIC
SRA r	SHIFT REGISTER r RIGHT ARITHMETIC
SRL r	SHIFT REGISTER r RIGHT LOGICAL

OPERATION



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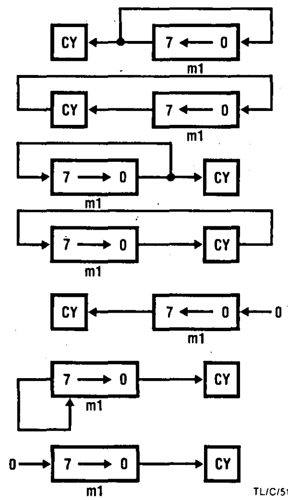
MEMORY MNEMONIC	DESCRIPTION
RLC m1	ROTATE MEMORY LEFT CIRCULAR
RL m1	ROTATE MEMORY LEFT THROUGH CARRY
RRC m1	ROTATE MEMORY RIGHT CIRCULAR
RR m1	ROTATE MEMORY RIGHT THROUGH CIRCULAR
SLA m1	SHIFT MEMORY LEFT ARITHMETIC
SRA m1	SHIFT MEMORY RIGHT ARITHMETIC
SRL m1	SHIFT MEMORY RIGHT LOGICAL

OPERATION



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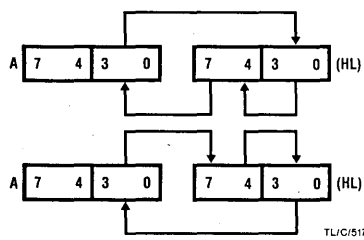
REGISTER/MEMORY MNENONIC	DESCRIPTION
RLD	ROTATE DIGIT LEFT AND RIGHT BETWEEN ACC AND MEMORY (HL)
RRD	ROTATE DIGIT RIGHT AND LEFT BETWEEN ACC AND MEMORY (HL)

OPERATION



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NSC800M/883B MIL-STD-883 Class B Screening

National Semiconductor offers the NSC800D and NSC800E with full class B screening per MIL-STD-883B for Military/Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

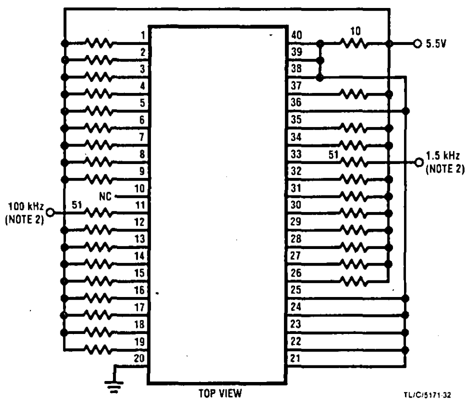
Electrical testing is performed in accordance with RETS800X, which tests or guarantees all of the electrical performance characteristics of the NSC800 data sheet. A copy of the current revision of RETS800X is available upon request.

100% SCREENING FLOW

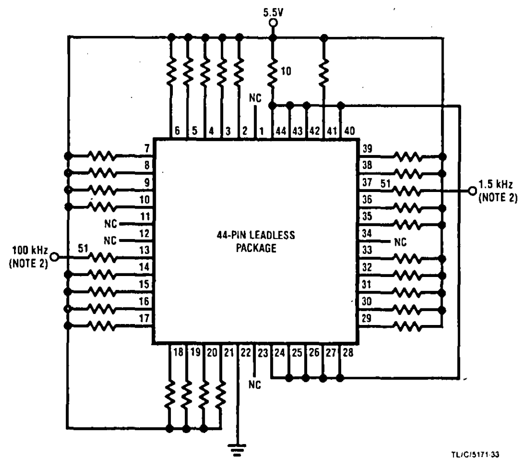
Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010B	100%
Stabilization Bake	1008 C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010 C 10 Cycles −65°C/+150°C	100%
Constant Acceleration	2001 E 30,000 G's, Y1 Axis	100%
Fine Leak	1014 B 5×10^{-8}	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS800X	100%
PDA	10% Max	
	+125°C AC and DC per RETS800X	100%
	−55°C AC and DC per RETS800X	100%
	+25°C AC per RETS800X	100%
QA Acceptance	Group A (sample, each lot)	
Quality Conformance	Group B (sample, each inspection lot)	
	Group C (sample every 90 days per microcircuit group)	
	Group D (sample every 6 months per package type)	
External Visual	2009	100%

Burn-In Circuits

5240HR
NSC800D/883B (Dual-In-Line)



5241HR
NSC800E/883B (Leadless Chip Carrier)



All resistors 2.7 kΩ unless marked otherwise.

Note 1: All resistors are 1/4W ± 5% unless otherwise specified.

Note 2: All clocks 0V to 3V, 50% duty cycle, in phase with < 1 μs rise and fall time.

Note 3: Device to be cooled down under power after burn-in.

Ordering Information

NSC800 X X X X

- **/A +** = A + Reliability Screening
- **/883** = MIL-STD-883B Screening (Note 1)

- **I** = Industrial Temperature (−40°C to +85°C)
- **M** = Military Temperature (−55°C to +125°C)
- **No Designation** = Commercial Temperature (0°C to 70°C)

- **−1** = 1 MHz Clock Output (Note 2)
- **−4** = 4 MHz Clock Output
- **No Designation** = 2.5 MHz Clock Output

- **D** = Ceramic Package
- **J** = CERDIP Package (availability to be announced)
- **N** = Plastic Package
- **E** = Ceramic Leadless Chip Carrier (LCC)
- **V** = Plastic Leaded Chip Carrier (PCC) (availability to be announced)

Note 1: Do not specify a temperature option; all parts are screened to military temperature.

Note 2: −1 part only available in D-1, N-1, D-1I, N-1I, V-1, V-1I

EXAMPLES

NSC800E-4/883
NSC800N
NSC800D-1I/A +

Reliability Information

Gate Count 2750

Transistor Count 11,000

National Semiconductor

microCMOS

NSC810A RAM-I/O-Timer

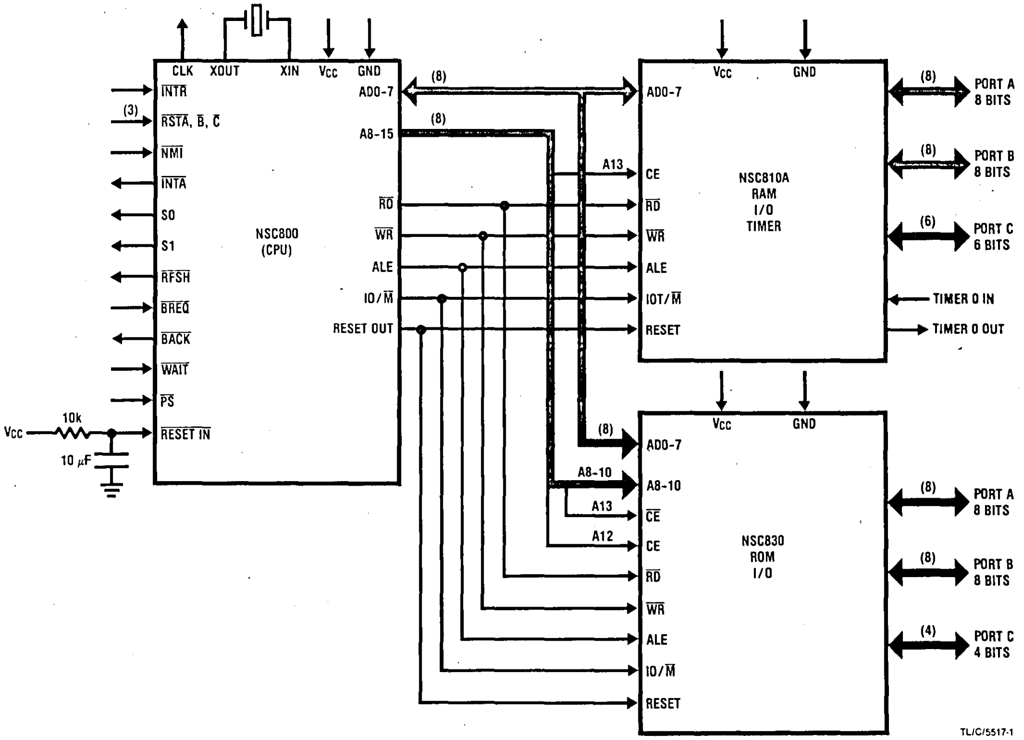
General Description

The NSC810A, which is fabricated using microCMOS silicon gate technology, functions as a memory, an input/output peripheral interface and a timing device. The memory is comprised of 1024 bits of static RAM organized as 128 × 8. The I/O portion consists of 22 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through port A. The timer portion of the device consists of two programmable 16-bit binary down-counters each capable of operation in any one of 6 modes. Timer counts are extendable by one of the available prescale values. The NSC810A comes in various speeds and package configurations, including the new high density LCC package. The NSC810A is available in full military specification 883B.

Features

- Three programmable I/O ports
- Two 16-bit programmable counter/timers
- 2.4V–6.0V power supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Timer operation—DC to 5 MHz
- Bus compatible with NSC800™ family
- Speed: compatible with NSC800
  NSC810A-4→NSC800-4 @ 4.0 MHz
  NSC810A→NSC800 @ 2.5 MHz
  NSC810A-1→NSC800-1 @ 1.0 MHz

NSC800 Microcomputer Family Block Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature Range	$-65°C$ to $+150°C$
Voltage at Any Pin with Respect to Ground	$-0.3V$ to $V_{CC}+0.3V$
V_{CC}	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions $V_{CC}=5V \pm 10\%$

T_A, Ambient Temperature

Military	$-55°C$ to $+125°C$
Industrial	$-40°C$ to $+85°C$
Commercial	$0°C$ to $+70°C$

DC Electrical Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC}=5V \pm 10\%$, GND = 0V, unless otherwise specified.

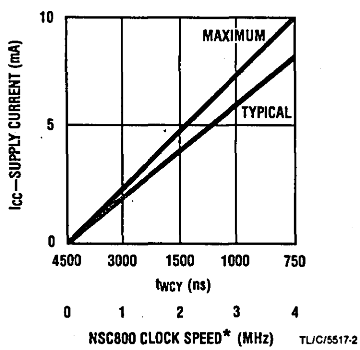
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	$I_{OH} = -1.0$ mA $I_{OUT} = -10\ \mu A$	2.4 $V_{CC}-0.5$			V V
V_{OL}	Logical 0 Output Voltage	$I_{OL}=2$ mA $I_{OUT}=10\ \mu A$	0 0		0.4 0.1	V V
I_{IL}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	-10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \le V_{IN} \le V_{CC}$	-10.0		10.0	μA
I_{CC}	Active Supply Current	$I_{OUT}=0$, Timer = Mode 1, T0IN = T1IN = 2.5 MHz, $t_{WCY}=750$ ns		8	10	mA
I_Q	Quiescent Current	No Input Switching, $T_A=25°C$		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage		2.4	5	6	V
V_{DRV}	Data Retention Voltage		1.2			V

Low Voltage Operation Preliminary

Voltage	NSC810A-1	NSC810A	NSC810A-4	Units
2.4	—	500	500	kHz
3.0	—	1	1	MHz

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

I_{CC} vs Speed



*When NSC810A is used with NSC800

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V

(Valid for the following temperature and speed)

NSC810A-1 → 0°C to 70°C
−40°C to +85°C

NSC810A → 0°C to 70°C
−40°C to +85°C
−55°C to +125°C

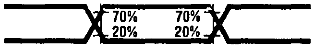
NSC810A-4 → 0°C to 70°C
−40°C to +85°C
−55°C to +125°C

Symbol	Parameter	Conditions	NSC810A-1		NSC810A		NSC810A-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	$C_L = 150$ pF		1000		400		300	ns
t_{AH}	AD0–7, CE, IOT/$\overline{M}$ Hold Time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		125		75		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		75		ns
t_{AS}	AD0–7, CE, IOT/$\overline{M}$ Set-Up Time		100		75		40		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		310		300	ns
t_{DS}	Data Set-Up Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Set-Up Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Output			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		220		ns
t_{RDD}	Data Bus Disable		0	100	0	100	0	75	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		75		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold with Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to $\overline{INTR}$ Output			300		300		300	ns
t_{SS}	Peripheral Data Set-Up with Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		340		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

Timer AC Electrical Characteristics

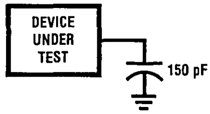
Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_C	Clock Frequency		DC		2.5	MHz
F_{CP}	Clock Frequency	Prescale Selected	DC		5.0	MHz
t_{CW}	Clock Pulse Width		150			ns
t_{CWP}	Clock Pulse Width	Prescale Selected	75			ns
t_{GS}	Gate Set-Up Time	With Respect to Negative Clock Edge	100			ns
t_{GH}	Gate Hold Time	With Respect to Negative Clock Edge	250			ns
t_{CO}	Clock to Output Delay	$C_L = 100$ pF			350	ns

AC Testing Input/Output Waveform



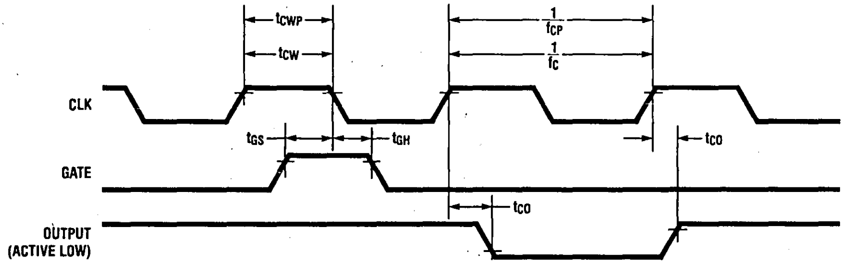
TL/C/5517-3

AC Testing Load Circuit



TL/C/5517-4

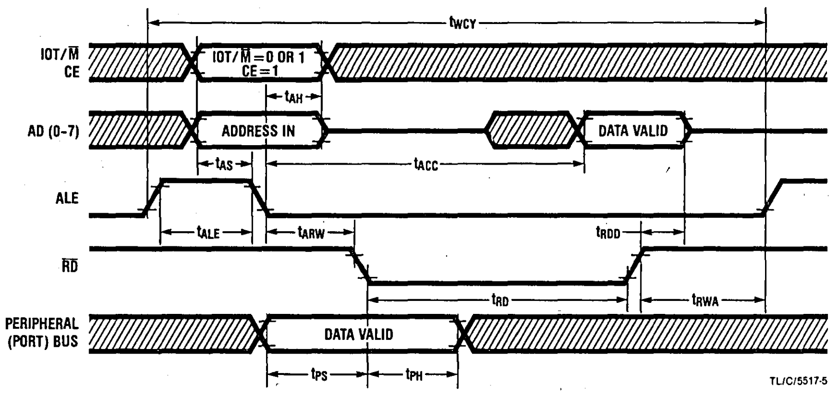
Timer Waveforms



TL/C/5517-9

General Timing Waveforms

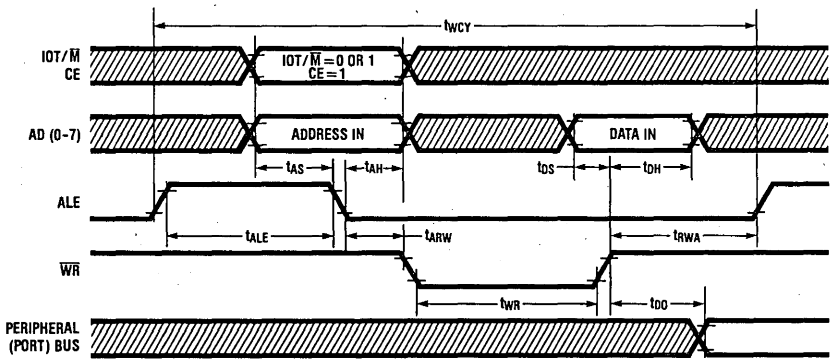
Read Cycle (Read from RAM, Port or Timer)



TL/C/5517-5

Note: Diagonal lines indicate interval of invalid data.

Write Cycle (Write to RAM, Port or Timer)

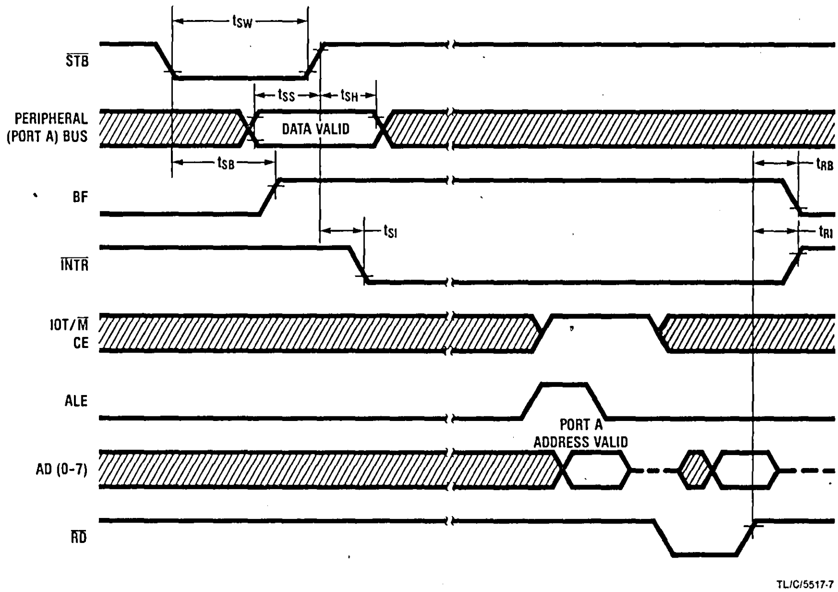


TL/C/5517-6

Note: Diagonal lines indicate interval of invalid data.

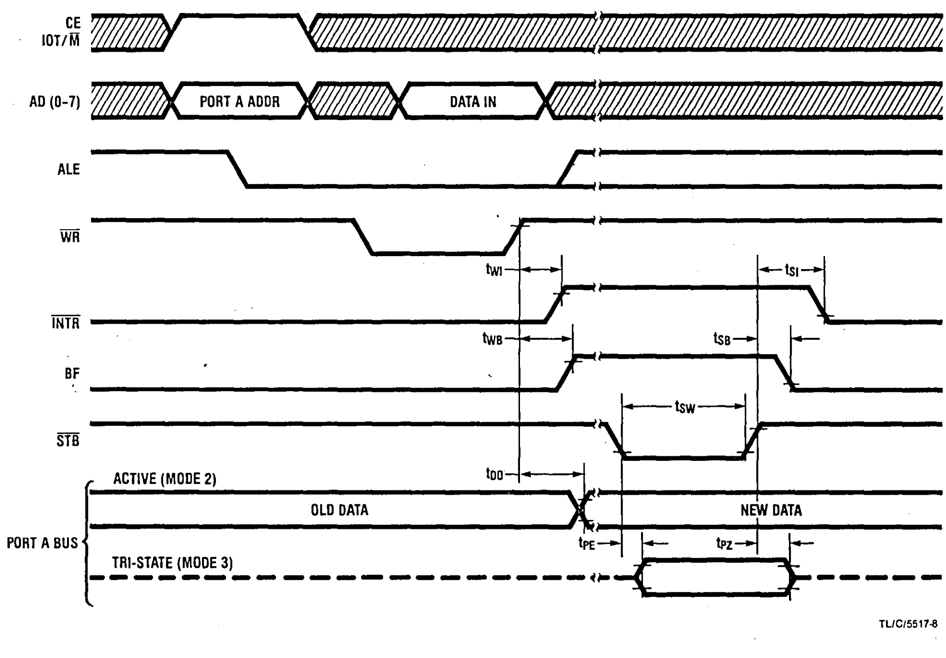
Handshake Timing

Strobed Mode Output



Note: Diagonal lines indicate interval of invalid data.

Strobed Mode Input



Note: Diagonal lines indicate interval of invalid data.

NSC810A Functional Pin Descriptions

The function and mnemonic for the NSC810A signals are described below:

INPUT SIGNALS

Reset (RESET): RESET is an active-high input that resets all registers to 0 (low). The RAM contents remain unaltered.

Input/Output Timer or RAM Select (IOT/$\overline{\text{M}}$): IOT/$\overline{\text{M}}$ is an I/O memory select input line. A logic 1 (high) input selects the I/O-timer portion of the chip; a logic 0 (low) input selects the RAM portion of the chip. IOT/$\overline{\text{M}}$ is latched at the falling edge of ALE.

Chip Enable (CE): CE is an active-high input that allows access to the NSC810A. CE is latched at the falling edge of ALE.

Read ($\overline{\text{RD}}$): The $\overline{\text{RD}}$ is an active-low input that enables a read operation of the RAM or I/O-timer location.

Write ($\overline{\text{WR}}$): The $\overline{\text{WR}}$ is an active-low input that enables a write operation to RAM or I/O-timer locations.

Address Latch Enable (ALE): The falling edge of the ALE input latches AD0–AD7, CE and IOT/$\overline{\text{M}}$ inputs to form the address for RAM, I/O or timer.

Timer 0 Input (T0IN): T0IN is the clock input for timer 0.

OUTPUT SIGNALS

Timer 0 Output (T0OUT): T0OUT is the programmable output of timer 0. After reset, T0OUT is set high.

POWER SUPPLY PINS

Positive DC Voltage (V_{CC}): V_{CC} is the 5V supply pin.

Ground (GND): Ground reference pin.

INPUT/OUTPUT SIGNALS

Address/Data Bus (AD0–AD7): The multiplexed bidirectional address/data bus, AD0–AD7 pins, are in the high impedance state when the NSC810A is not selected. AD0–AD7 will latch address inputs at the falling edge of ALE. The address will designate a location in RAM, I/O or timer. $\overline{\text{WR}}$ input enables 8-bit data to be written into the addressed location. $\overline{\text{RD}}$ input enables 8-bit data to be read from the addressed location. The $\overline{\text{RD}}$ or $\overline{\text{WR}}$ inputs occur while ALE is low.

Port A, 0–7 (PA0–PA7): Port A is an 8-bit basic mode input/output port, also capable of strobed mode I/O utilizing three control signals from port C. Strobed mode of operation on port A has three different modes: strobed input, strobed output with active bus, strobed output with TRI-STATE bus.

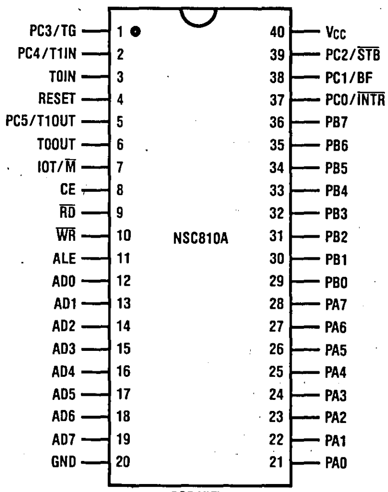
Port B, 0–7 (PB0–PB7): Port B is an 8-bit basic mode input/output port.

Port C, 0–5 (PC0–PC5): Port C is a 6-bit basic mode I/O port. Each pin has a programmable second function, as follows:

- **PC0/$\overline{\text{INTR}}$:** $\overline{\text{INTR}}$ is an active-low strobed mode interrupt request to the Central Processor Unit (CPU).
- **PC1/BF:** BF is an active-high buffer full output to peripheral devices.
- **PC2/$\overline{\text{STB}}$:** $\overline{\text{STB}}$ is an active-low strobe input from peripheral devices.
- **PC3/TG:** TG is the timer gating signal.
- **PC4/T1IN:** T1IN is the clock input for timer 1.
- **PC5/T1OUT:** T1OUT is the programmable output of timer 1.

Connection Diagrams

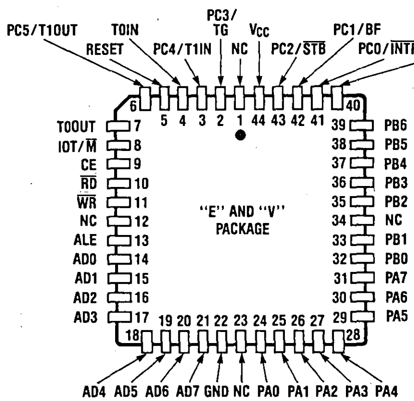
Dual-In-Line Package



TOP VIEW

TL/C/5517-10

See NS Package D40C, J40A or N40A



TOP VIEW

TL/C/5517-11

NC = no connect

See NS Package ED44A or V44

NSC810A Functional Description

Refer to *Figure 1* for a detailed block diagram of the NSC810A.

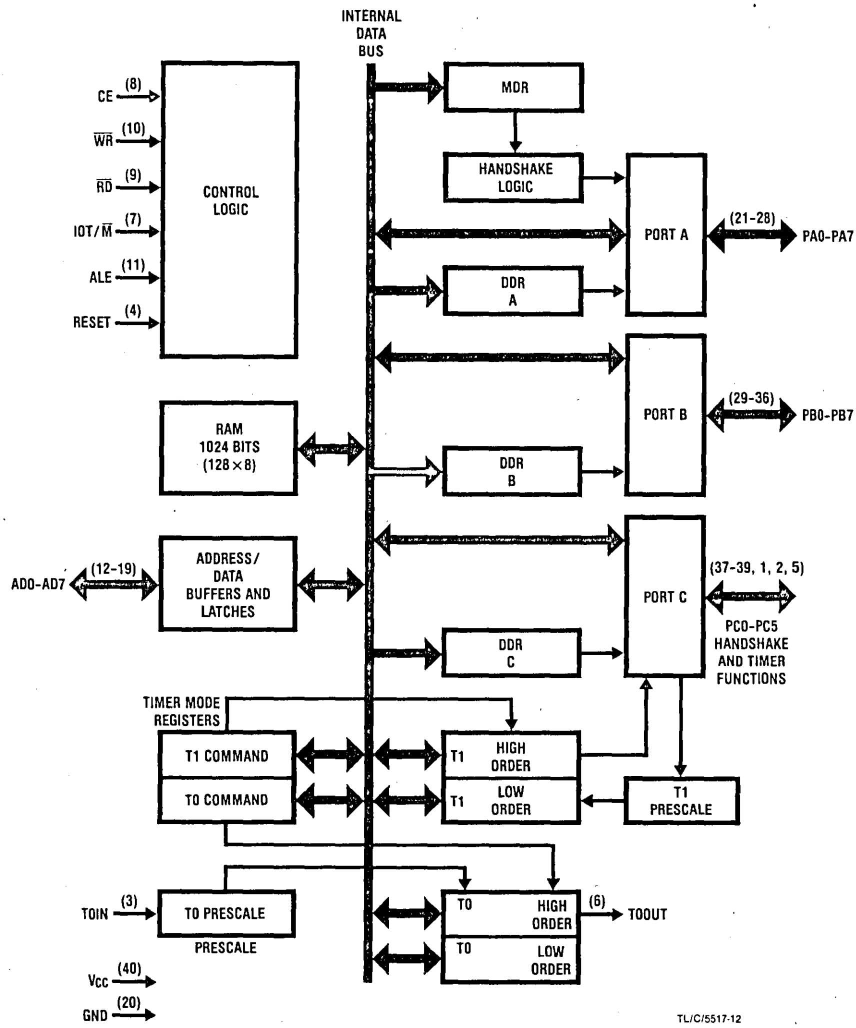
RANDOM ACCESS MEMORY (RAM)

The memory portion of the RAM-I/O-timer is accessed by a 7-bit address input to pins AD0 through AD6. The IOT/$\overline{M}$ input must be low (RAM select) and the CE input must be high at the falling edge of ALE to address the RAM. Address bit AD7 is a "don't care" for RAM addressing. Timing for RAM read and write operations is shown in the timing diagrams.

INPUT/OUTPUT (I/O)

The I/O portion of the NSC810A contains three sets of I/O called ports. There are two ports (A and B) which contain eight bits each and one port (port C) which has six bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (6 bits for port C). All ports share common function of Read, Write, Bit-Set and Bit-Clear. Additionally, port A is programmable for strobed (handshake) mode input or output. Port C has programmable second functions for each bit associated with strobed modes and timer functions. Table I defines the address location of the ports, timers and control registers.

Detailed Block Diagram



Note: Applicable pinout for 40-pin dual-in-line package within parentheses

FIGURE 1

NSC810A Functional Description (Continued)

TABLE I. I/O AND TIMER ADDRESS DESIGNATIONS

8-Bit Address Field Bits 7 6 5 4 3 2 1 0	Designation I/O Port, Timer, etc.	R (Read) W (Write)
x x x 0 0 0 0 0	Port A (byte)	R/W
x x x 0 0 0 0 1	Port B (byte)	R/W
x x x 0 0 0 1 0	Port C (byte)	R/W
x x x 0 0 0 1 1	Not Used	**
x x x 0 0 1 0 0	DDR—Port A	W
x x x 0 0 1 0 1	DDR—Port B	W
x x x 0 0 1 1 0	DDR—Port C	W
x x x 0 0 1 1 1	Mode Definition Reg.	W
x x x 0 1 0 0 0	Port A—Bit-Clear	W
x x x 0 1 0 0 1	Port B—Bit-Clear	W
x x x 0 1 0 1 0	Port C—Bit-Clear	W
x x x 0 1 0 1 1	Not Used	**
x x x 0 1 1 0 0	Port A—Bit-Set	W
x x x 0 1 1 0 1	Port B—Bit-Set	W
x x x 0 1 1 1 0	Port C—Bit-Set	W
x x x 0 1 1 1 1	Not Used	**
x x x 1 0 0 0 0	Timer 0 (LB)	*
x x x 1 0 0 0 1	Timer 0 (HB)	*
x x x 1 0 0 1 0	Timer 1 (LB)	*
x x x 1 0 0 1 1	Timer 1 (HB)	*
x x x 1 0 1 0 0	STOP Timer 0	W
x x x 1 0 1 0 1	START Timer 0	W
x x x 1 0 1 1 0	STOP Timer 1	W
x x x 1 0 1 1 1	START Timer 1	W
x x x 1 1 0 0 0	Timer 0 Mode	R/W
x x x 1 1 0 0 1	Timer 1 Mode	R/W
x x x 1 1 0 1 0	Not Used	**
x x x 1 1 0 1 1	Not Used	**
x x x 1 1 1 0 0	Not Used	**
x x x 1 1 1 0 1	Not Used	**
x x x 1 1 1 1 0	Not Used	**
x x x 1 1 1 1 1	Not Used	**

x = don't care
LB = low-order byte
HB = high-order byte
* A write accesses the modulus register, a read the read buffer.
** A read from an unused location reads invalid data, a write does not affect any operation of NSC810A.

MODE DEFINITION REGISTER (MDR)

The mode definition register (MDR) defines the operating mode for port A. While ports B and C are always in the basic I/O mode, there are four operating modes for port A:

Mode 0—Basic I/O (Input or Output)
Mode 1—Strobed Mode Input
Mode 2—Strobed Mode Output—Active Peripheral Bus
Mode 3—Strobed Mode Output—TRI-STATE Peripheral Bus

The MDR has the address assignment xxx00111 and is illustrated for the four modes in Table II.

TABLE II. MODE DEFINITION REGISTER BIT ASSIGNMENTS

Mode \ Bit	7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	0
1	x	x	x	x	x	x	0	1
2	x	x	x	x	x	0	1	1
3	x	x	x	x	x	1	1	1

x = don't care

DATA DIRECTION REGISTERS (DDR)

Each port bit has a data direction register (DDR) that defines the I/O state of the bit. The bit is configured as an input if a "0" is written into its DDR, or as an output if a "1" is written. The DDR bits cannot be individually written to; the entire DDR byte is affected by a write to the DDR address. Thus, all data must be consistent with the direction desired for each port.

Any write or read operations on a port contradicting the DDR will not affect the port output or input. However, a read of a port bit, defined as an output, will cause a read from the output latch, and a write to a port bit, defined as an input, will modify the output latch. Refer to *Figure 2*.

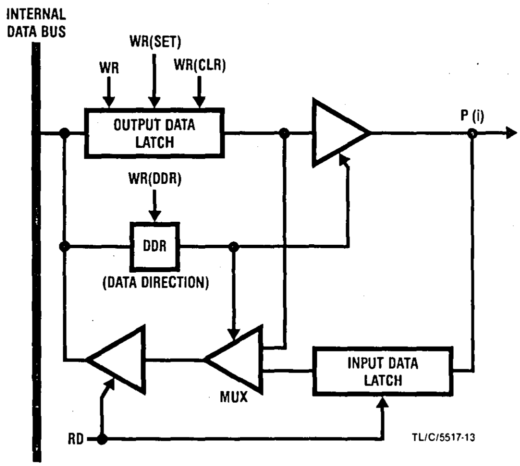


FIGURE 2. Block Diagram for Port Bit (i)

BIT OPERATIONS

The I/O features of the RAM-I/O-timer allow modification of a single bit or several bits of a port with Bit-Set and Bit-Clear command. The address is set up to indicate that a Bit-Set (or Clear) is taking place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing 1s will cause the indicated operation to be performed on the corresponding port bit. All bits of the data mask with 0s cause the corresponding port bits to remain unchanged. Three sample operations are shown in Table III using port B as an example.

NSC810A Functional Description (Continued)

TABLE III. BIT-SET AND CLEAR EXAMPLES

Operation	Set B7	Clear B2 and B0	Set B4, B3 and B1
Address	xxx01101	xxx01001	xxx01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

PORT FUNCTIONS—BASIC I/O

Basic I/O is the mode of operation of ports B and C and mode 0 of port A (defined by the MDR). Read and write byte operations, and bit operations can be executed in the basic I/O mode. The timing for basic input and basic output modes is shown in the AC Characteristics tables.

When a read occurs, the information is latched from the peripheral (port) bus during the leading (falling) edge of the $\overline{RD}$ strobe. When a write occurs, the port bus is modified after the trailing (rising) edge of the $\overline{WR}$ strobe with data from the AD bus. Port output data remains valid at the output pin from one trailing edge of $\overline{WR}$ strobe to the trailing edge of the next $\overline{WR}$ strobe which then modifies that port.

PORT A—STROBED (HANDSHAKE) MODE

Port A can be programmed (via the MDR) into one of 3 types of strobed mode for handshake communication with intelligent peripherals. When port A is in mode 1, 2, or 3 (see description of MDR), port C pins 0, 1, and 2 are used as handshake signals between the peripheral and the CPU. These handshake signals are designated $\overline{STB}$, BF, and $\overline{INTR}$. Timing parameters and timing diagrams are detailed under AC Characteristics.

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the I/O to the CPU. In strobed input mode, the CPU reads the valid data at port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing to port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving the ability to control strobed data transfer under software control. It is enabled or disabled respectively, by setting (=1) or clearing (=0) the output data latch of bit 2, port C. Port bit PC2 is used as the $\overline{STB}$ input. Since PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation. Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear instructions. The port C byte write command will not alter the output data latch of PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active-low input from the peripheral device, signaling that data-transfer is about to begin. This strobe is interpreted as an "output request" if port A is in a strobed output mode, or as a "data-valid" signal if port A is in strobed input mode.

BF (Buffer Full) is an output from the I/O to the peripheral signaling that data transfer is complete. In strobed input mode, this strobe indicates that data is received into port A and that no further data should be transmitted by the peripheral device until the port has been read (emptied). In strobed output mode, BF indicates that the request from the peripheral has been processed by the CPU and the valid data now appears in port A.

Note: In either input or output mode BF may be cleared by rewriting mode definition register.

The bits of port C that are used for handshake control of port A (bits C0, C1 and C2) must be direction-defined appropriately in the DDR. Also, the DDR of port A must be consistent with the mode specified in the MDR. Register set-up configurations for the three handshake modes are illustrated in Table IV.

TABLE IV. MODE DEFINITION REGISTER CONFIGURATIONS

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Strobed Input	xxxxxx01	00000000	xxx011	xxx1xx
Strobed Output (Active)	xxxxx011	11111111	xxx011	xxx1xx
Strobed Output (TRI-STATE)	xxxxx111	11111111	xxx011	xxx1xx

Strobed Input (Mode 1)

During strobed input operations, an external device can load data into port A with the $\overline{STB}$ signal. Data is input to the PA0–7 input latches on the leading (negative) edge of $\overline{STB}$, causing BF to go high (true). On the trailing (positive) edge of $\overline{STB}$ the data is latched and the interrupt signal, INTR, becomes valid indicating to the CPU that data is available for reading. $\overline{INTR}$ will become valid only if the interrupt is enabled, that is the output data latch for PC2 is true.

When the CPU reads port A, address X'00, the trailing edge of the $\overline{RD}$ strobe causes BF and $\overline{INTR}$ to become inactive, indicating that the strobed input cycle has been completed.

Strobed Output (Mode 2)

During strobed output operations, an external device can read data from port A with the $\overline{STB}$ signal. Data is initially loaded into port A by the CPU writing to I/O address X'00. On the trailing edge of $\overline{WR}$, $\overline{INTR}$ is set inactive and BF becomes valid indicating data is available for the external

NSC810A Functional Description (Continued)

device. When the external device is ready to accept the data in port A it pulses the $\overline{STB}$ signal. $\overline{STB}$ will reset BF with its rising edge and also activates the $\overline{INTR}$ signal.

$\overline{INTR}$ in this mode indicates a condition that requires CPU intervention, which is the output of the next byte of data.

Strobed Output—TRI-STATE Mode (Mode 3)

The strobed output TRI-STATE mode and the strobed output active (peripheral) bus mode function in a similar manner with one exception. The exception is that the data signals on PA0–7 assume the high impedance state at all times except when accessed by the $\overline{STB}$ signal. Thus, in addition to its timing function, $\overline{STB}$ activates port A outputs to active logic levels. This mode 3 operation allows other data sources, in addition to the NSC810, to feed a common external device.

TIMERS

The two timers in the RAM-I/O-timer are 16-bit binary down-counters, each timer having six modes of operation. Full count is reached at "n + 1", where "n" is the value loaded into the modulus register. Read and write commands can occur at any time, asynchronous to timer operation by addressing the timer read buffer or modulus register, respectively. Each timer has a mode register and a write-only start/stop register. Each timer also has a prescaler which divides the incoming clock signal by a programmable value, extending the effective ranges of the timers while maintaining 16-bit precision. Selected timer outputs are ÷ 1 or ÷ 2 for timer 1, and ÷ 1, ÷ 2, or ÷ 64 for timer 0. A diagram representing one timer and associated registers is shown in *Figure 3.*

TIN, TOUT, AND TG

Timer 0 has dedicated pins for its clock, T0IN, and its output, T0OUT. Timer 1 must borrow its input and output pins from port C. This is accomplished by writing to the TMR for timer 1. If mode 1, 2, 3, 4, 5, or 6 is specified in TMR 1, the pins from port C (PC3, PC4, and PC5) are automatically made available to the timer(s) for gating (TG), T1IN, and T1OUT, respectively. These pins are also taken from port C any time timer 0 is in mode 2, 3, or 4. This is also automatically accomplished by writing TMR 0. In order to reconfigure pins PC3, PC4, PC5 to their original configuration as standard I/O, the timer mode registers must be reset by selecting mode 0 or 7.

TG (PC3), the timer gate, is used to hardware control the starting/stopping (or triggering) of the timers. The timer gate may be used individually by either timer or simultaneously by both timers.

For modes 2 and 3, the timer starts on the gate-active transition assuming the start address was previously written. If the timer gate makes an active transition prior to a write to the start address, the trailing edge of the WR strobe starts the timer. However, for mode 4 the timer always waits for an active gate edge following a write to the start address.

The DDR for port C must be programmed with the correct I/O direction for TG and the input and output of timer 1. See Table V for programming examples.

TIMER MODES

The low-order three bits (bits 0, 1, 2) of the timer mode registers (TMR) define the mode of operation for the timers. Each TMR may be written to, or read from, at any time. However, to ensure accurate timing, it is important to modify the mode of the timer only when the timer is stopped. Inputs of 000 or 111 will define a NOP (no operation) mode, the timer is stopped and the output is inactive. Inputs of 001 through 110 will select one of six distinct timer functions.

In the explanations that follow, assume that the modulus for the timer is loaded with the appropriate value by writing to the low and high bytes of each timer (I/O addresses X'10 and X'11 for timer T0 and X'12 and X'13 for timer T1). Assume also that the timer is started by writing the I/O address X'15 (T0) or X'17 (T1) and the prescaler is not selected.

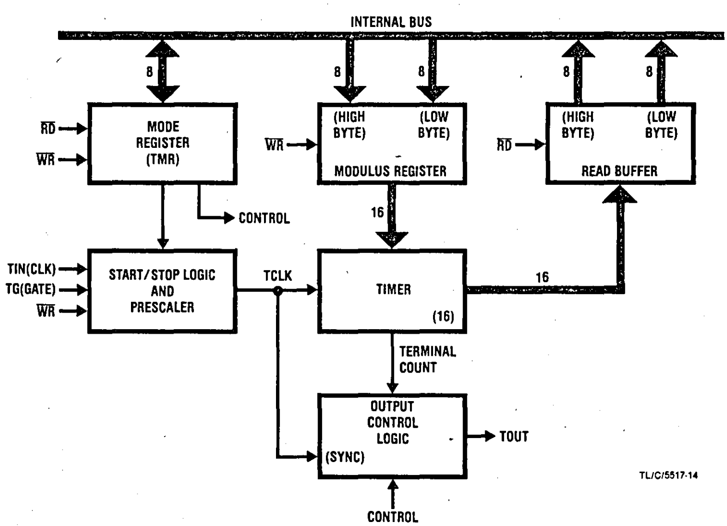


FIGURE 3. Timer Internal Block Diagram (One of Two)

NSC810A Functional Description (Continued)

TABLE V. TIMER PROGRAMMING SELECTION EXAMPLE

Mode Register Bit 7 6 5 4 3 2 1 0	Output Sense Active L/H	Timer Gate Polarity Active L/H	Mode Description Single/Double Precision S/D	Prescale Value	Timing Mode	Port C DDR 5 4 3 2 1 0
TIMER 0						
x x x x x 0 0 0	x	x	x	x	0	x x x x x x
0 x 0 0 0 0 0 1	L	x	D	÷1	1	x x x x x x
1 x 0 1 1 1 1 0	H	x	D	÷64	6	x x x x x x
1 0 0 0 1 1 0 0	H	H	D	÷2	4	1 0 0 x x x
0 1 1 0 0 0 1 0	L	L	S	÷1	2	1 0 0 x x x
TIMER 1						
x x x x x 1 1 1	x	x	x	x	7	x x x x x x
0 x 0 x 0 0 0 1	L	x	D	÷1	1	1 0 0 x x x
1 0 1 x 1 1 0 1	H	L	S	÷2	5	1 0 0 x x x
0 1 0 x 0 0 1 1	L	H	D	÷1	3	1 0 0 x x x

x = don't care

Event Counter (Mode 1, TMR Bits = 001)

In the non-gated mode, the count is decremented for each clock period at the input of the timer (see *Figure 4a*). When the count reaches zero, the output goes valid and remains valid until the timer count is read by the CPU, or the timer is halted.

The timer is reloaded at the terminal count (= 0) with the modulus and continues to decrement even when the output is valid.

Accumulative Timer (Mode 2, TMR Bits = 010)

In this gated mode, the counter will decrement only when the gate input is active (see *Figure 4b*). If the gate becomes inactive, the counter will hold at its present value and continue to decrement when the gate again becomes active. When the counter decrement is zero, the output becomes valid and remains valid until the count is read by the CPU or the timer is halted.

At the terminal count the timer is reloaded and the count continues as long as the gate is active.

Restartable Timer (Mode 3, TMR Bits = 011)

In this gated mode, the counter will decrement only when the gate input is active. If the gate becomes inactive, the counter will reload the modulus and hold this value until the gate again becomes active (see *Figure 4c*). If the timer is read when the gate is inactive, you will always read the value the timer has counted down to, not the value the timer has been reloaded with. The timer restarts at its modulus value. The prescaler is not reset at this time.

At terminal count the output becomes valid and the timer is reloaded. The timer will continue to run as normal, the only difference is the output is valid. Once the output is valid it remains valid until the count is read by the CPU or the timer is halted.

Note: The gate inactive time must be longer than the high time of the internal clock on the chip. Therefore, with ÷64 prescale selected the gate inactive time must be 33 input clocks or greater.

One Shot (Mode 4, TMR Bits = 100)

In this gated mode, the timer holds the modulus count until the active gate edge (see *Figure 4d*). The output immediately becomes valid and remains valid as the counter decrements. The gating signal may go inactive without affecting the count. If TG (the gate) becomes inactive and returns active prior to the terminal count, the modulus will be reloaded, retriggering the one shot period. When the timer reaches the terminal count, the output becomes inactive. The gate, in this mode, is edge sensitive; the active edge is defined in TMR.

Note: The one shot cannot be retriggered during its last internal count regardless of prescaler selected. Therefore, in divide by 1 prescaler, it cannot be retriggered during the last clock, in divide by 2 prescaler, during the last two clocks and divide by 64 prescaler, during the last 64 clocks.

Square Wave (Mode 5, TMR Bits = 101)

In this non-gated mode, the output will go active as soon as the timer is started. The counter decrements for each clock period and complements its output when zero is reached (see *Figure 4e*). The modulus is then reloaded and counting continues. Assuming a regular clock input, the output will then be a square wave with a period equal to twice the value loaded into the modulus. Therefore, varying the modulus will vary the duty cycle of the square wave.

Stopping then restarting the timer does not reset the timer. In order to reload the modulus and start from the beginning of the cycle, the timer mode register must be reset by selecting mode 0 and then reprogramming the timer.

Pulse Generator (Mode 6, TMR Bits = 110)

In this non-gated mode, the counter decrements for each clock period (see *Figure 4f*). When the timer decrements to zero, the output becomes valid for one clock width.

NSC810A Functional Description (Continued)

With a prescale of divide by 2 the output will be valid for one full clock and with divide by 64 prescale the output will be valid for 32 clocks. The modulus is then reloaded and the sequence is repeated. Varying the modulus value will vary the frequency of the pulse.

Stopping then restarting the timer does not reset the timer. In order to reload the modulus and start from the beginning of the cycle, the timer mode register must be reset by selecting mode 0 and then reprogramming the timer.

Timer Mode Examples (Modulus register is loaded with 0004 for these examples)

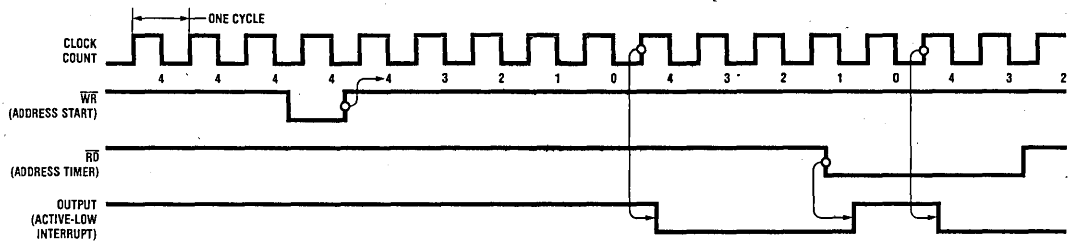


FIGURE 4a. Event Counter Mode (Mode 1)

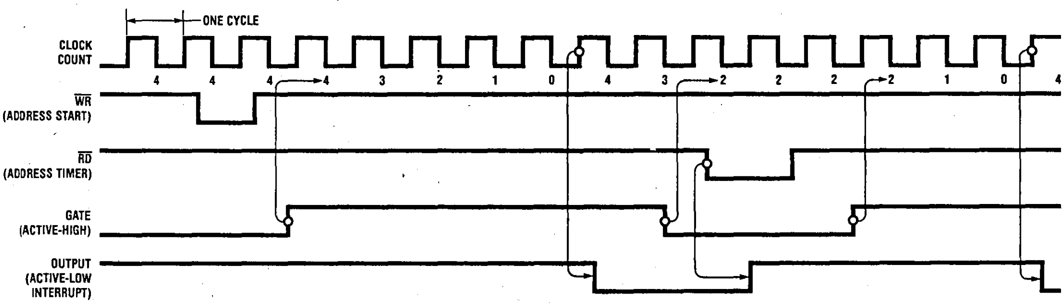


FIGURE 4b. Accumulative Timer (Mode 2)

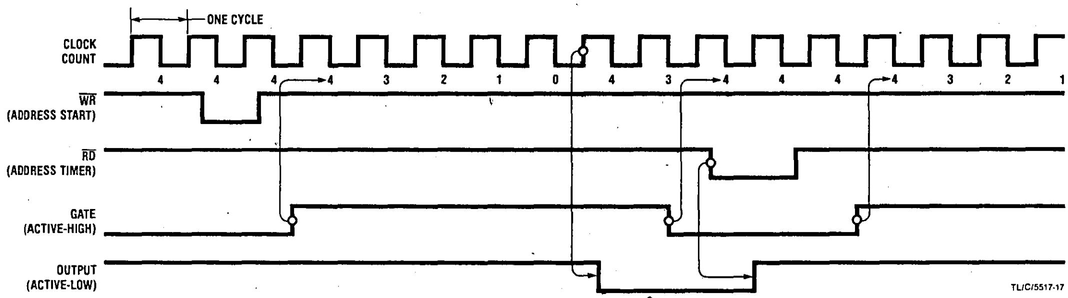


FIGURE 4c. Restartable Timer (Mode 3)

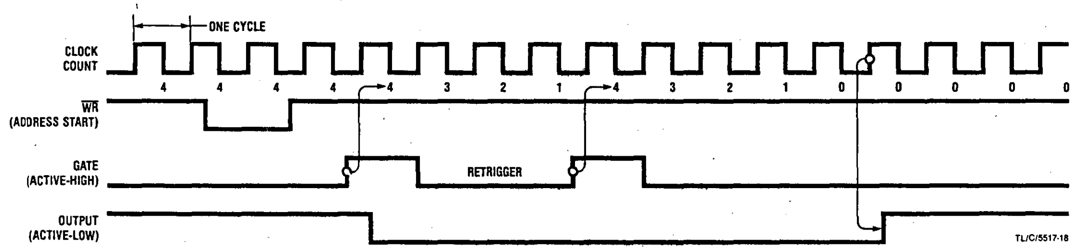


FIGURE 4d. One Shot (Mode 4)

Timer Mode Examples (Continued) (Modulus register is loaded with 0004 for these examples)

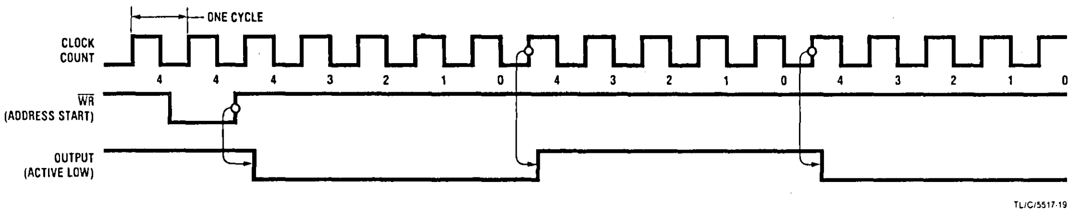


FIGURE 4e. Square Wave (Mode 5)

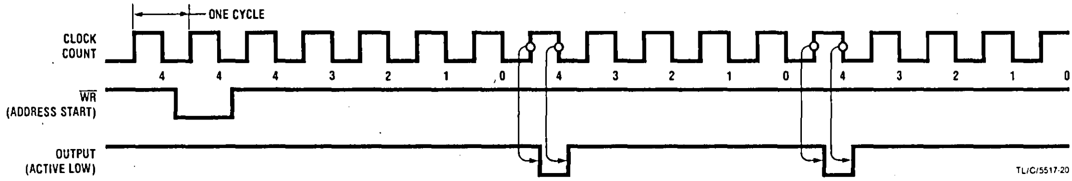
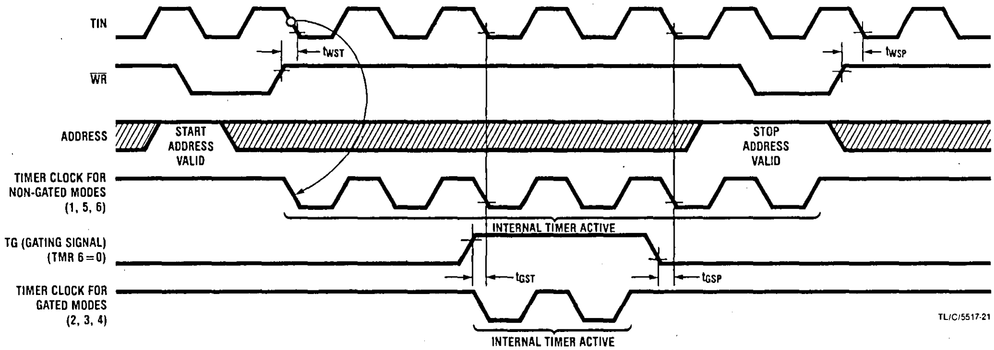


FIGURE 4f. Pulse Generator (Mode 6)



Note: Diagonal lines indicate interval of invalid data.
For mode 4 (one shot), only start-timing applies
t_{WST}—$\overline{WR}$ set-up for starting timer 150 ns
t_{WSP}—$\overline{WR}$ set-up for stopping timer 150 ns
t_{GST}—TG (gate) set-up for starting timer 100 ns
t_{GSP}—TG (gate) set-up for stopping timer 100 ns

FIGURE 5. Start/Stop Timing

TIMER MODE REGISTER

The timer mode register (TMR) may be written or read at any time; however, to assure accurate timing it is important to modify the mode when the timer is stopped. The timer mode is selected from one of six modes with TMR bits 0, 1, and 2. Bits 3 and 4 select the prescale value if the prescaler is to be used. Bits 5, 6 and 7 select the read/write mode, gate input polarity, and output sense (active-high or low). The bit functions of the TMR are further illustrated in *Figure 6*.

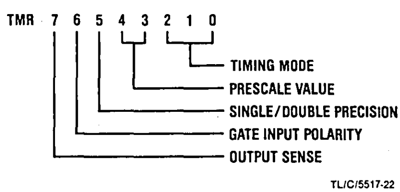


FIGURE 6. Timer Mode Register

TABLE VI. MODE SELECTION

BIT 2 1 0		Timer Function
0 0 0	—	Timer Stopped and Reset
0 0 1	—	Event Counter
0 1 0	—	Event Timer (Stopwatch)
0 1 1	—	Event Timer (Resetting)
1 0 0	—	One Shot
1 0 1	—	Square Wave
1 1 0	—	Pulse Generator
1 1 1	—	Timer Stopped and Reset

Timer Prescaler

There is a prescale function associated with each timer. It serves as an additional divisor to lengthen the counts for each timer circuit. The value of the divisor is fixed and selectable in each TMR.

The timer output is affected by the prescale selection. The output responds to the timer clock, not the incoming clock (TIN); so, TOUT will be prescaled by the same value as the timer. Although the 16-bit prescaled count of the timer may be read, the internal value of the prescaler cannot be read by the user. A "00" for either timer represents ÷1 (no prescale). Timer 0 has the two possibilities of ÷2 or ÷64:

Timer Bit	4 3	Prescale
	0 0	÷1
	0 1	÷2
	1 1	÷64

Timer 1 has only the ÷2 prescale available; TMR bit 4 is a "don't care."

Timer Bit	4 3	Prescale
	x 0	÷1
	x 1	÷2

Single/Double Precision

A two-byte word (or a single byte when one byte is a "don't care") may be read from or writen to the timers. To program the timer buffers, TMR bit 5 must be set as follows:

0—Double byte read or write low byte first, then high byte. *The order of low byte first, high byte second must be maintained for proper Read/Write communications.*

1—Single byte read or write low byte only—high byte "don't care" or high byte only with low byte "don't care."

The difference between these modes is that the double byte mode freezes the read buffer or the modulus register until you have had an opportunity to read or write both bytes. The following example clearly illustrates this point. If the timer had a value of 200 when the low byte was read and then decremented to 1FF before the high byte was read then the double byte mode would have read 00 and 02, respectively. The single precision mode would have read 00 and 01.

Note: In the double precision mode, the high byte should be read immediately after the low byte. Do not access any other registers or unused address location between the reads.

Gate Input Polarity

The TG input is the hardware control for starting and stopping the timers. For modes 2 and 3, the timer starts on the gate-active transition assuming the start address was previously written. If the timer gate makes an active transition prior to a write to the start address, the trailing edge of the WR strobe starts the timer. However, for mode 4 the timer always waits for an active gate edge following a write to the start address.

The polarity of the gate input may be selected by the contents of bit 6 of the TMR. If bit 6 equals 0, the gate signal will be active-high or positive edge for mode 4; if bit 6 equals 1, the gate polarity will be active-low or negative edge for mode 4.

Timer Output Polarity

Like the gating function, the polarity of the output signal is also programmable via bit 7 of the TMR. A zero will cause an active-low output; a one will generate an active-high output.

The output for T1 is multiplexed with port C, bit 5. (Similarly T1IN is multiplexed with port C, bit 4.) When any timer mode other than 0 or 7 is specified for T1, or when mode 2, mode 3, or mode 4 is specified for T0, the three port C pins, bit 3, bit 4, and bit 5, become TG, T1IN and T1OUT, respectively.

TIMER PROGRAMMING

The proper sequence to program the timer is as follows:

1. Write timer mode register with mode 0 or 7 selected. This stops the timer, resets the prescaler, and sets internal clock high.
2. Write timer mode register again, this time setting it up to your requirements.
3. Write the modulus values, low byte first, high byte second.
4. Start the timers.

The timer output latches are only updated when the internal timer clock gets an active transition. The internal timer clock is defined as the output of the prescaler. Therefore, it is impossible to read back the value just written to the timer unless you have an active transition on the internal clock.

To guarantee the integrity of the data during a read operation, updates to the timer output latches are blocked out. If an update is blocked out due to a read, the output latches will not be updated until the next active transition. If continuous reads were made to the timers and an update was blocked out it would appear as if a count was skipped. For example, if the output latches were FF when a block out occurred, the next update would occur at FD, thereby giving an appearance of the count FE being skipped. In actuality the correct number of clocks has occurred for the timer to read FD.

Writing the modulus value when the timer is running does not update the timer immediately. The new value written will get into the timer when the timer hits its terminal count and reloads its value. If the timer is stopped and a modulus is written the new modulus value will get into the timer only if the internal clock is high for some period before the start command. If it does not go high then the next time the timer hits its terminal count it will load the new modulus. One way to guarantee the data will get into the timer immediately is to follow steps 1-4. Although this procedure guarantees that the data will get into the timer you will not be able to read it back until you get an active transition on the internal clock.

Rewriting modulus does not reset the prescaler. The only way to reset the prescaler is to write the mode register and have internal clock signal be high for some period between the write of the mode register and the start of the timer. Once again steps 1 through 4 will reset the prescaler.

NSC810A/883B MIL-STD-883 Class B Screening

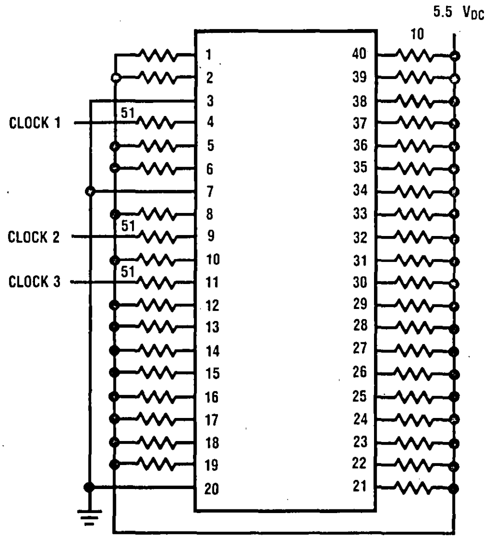
National Semiconductor offers the NSC810AD and NSC810AE with full class B screening per MIL-STD-883B for Military/Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

Electrical testing is performed in accordance with RETS810AX, which tests or guarantees all of the electrical performance characteristics of the NSC810A data sheet. A copy of the current revision of RETS810AX is available upon request. The following table is the MIL-STD-883 flow as of the date of publication.

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010 B	100%
Stabilization Bake	1008 C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010 C 10 Cycles −65°C/+150°C	100%
Constant Acceleration	2001 E 30,000 G's, Y1 Axis	100%
Fine Leak	1014 B 5×10^{-8}	100%
Gross Leak	1014 C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS810AX	100%
PDA	10% Max	
	+125°C AC and DC per RETS810AX	100%
	−55°C AC and DC per RETS810AX	100%
	+25°C AC per RETS810AX	100%
QA Acceptance	Group A (sample, each lot)	
Quality Conformance	Group B (sample, each inspection lot)	
	Group C (sample every 90 days per microcircuit group)	
	Group D (sample every 6 months per package type)	
External Visual	2009	100%

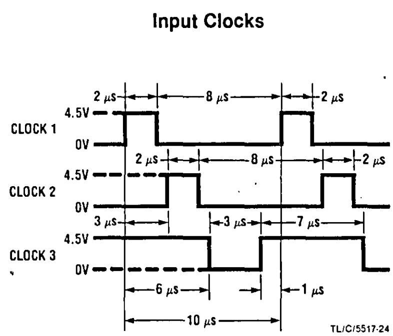
Burn-In Circuit

5242HR
NSC810AD/883B (Dual-In-Line)



TL/C/5517-23

Timing Diagram



TL/C/5517-24

Note 1: All resistors ±5%, 1/4 watt unless otherwise designated, 125°C operating life circuit.

Note 2: E package burn-in circuit 5244HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V.

Note 5: Device to be cooled down under power after burn-in.

Ordering Information

NSC810A X X X X

- X (4th): **/A+** = A+ Reliability Screening; **/883** = MIL-STD-883B Screening (Note 1)
- X (3rd): **I** = Industrial Temperature (−40°C to +85°C); **M** = Military Temperature (−55°C to +125°C); **No Designation** = Commercial Temperature (0°C to 70°C)
- X (2nd): **−1** = 1 MHz Clock Output (Note 2); **−4** = 4 MHz Clock Output; **No Designation** = 2.5 MHz Clock Output
- X (1st): **D** = Ceramic Package; **J** = CERDIP Package (availability to be announced); **N** = Plastic Package; **E** = Ceramic Leadless Chip Carrier (LCC); **V** = Plastic Leaded Chip Carrier (PCC) (availability to be announced)

Note 1: Do not specify a temperature option; all parts are screened to military temperature.

Note 2: −1 part only available in D-1, N-1, D-1I, N-1I, V-1, V-1I

EXAMPLES

NSC810AE-4/883
NSC810AN
NSC810AD-1I/A+

Reliability Information

Gate Count	4000
Transistor Count	14,000

National Semiconductor

microCMOS

NSC830 ROM-I/O; NSC831 I/O Only

General Description

The NSC830 is a ROM-I/O device contained in a standard 40-pin, dual-in-line package. The chip, which is fabricated using microCMOS silicon gate technology, functions as a memory, and an input/output peripheral interface device. The memory is comprised of 16,384 bits of ROM organized as 2048 x 8. The I/O portion consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written to or read from in bytes. Several types of strobed mode operations are available through Port A.

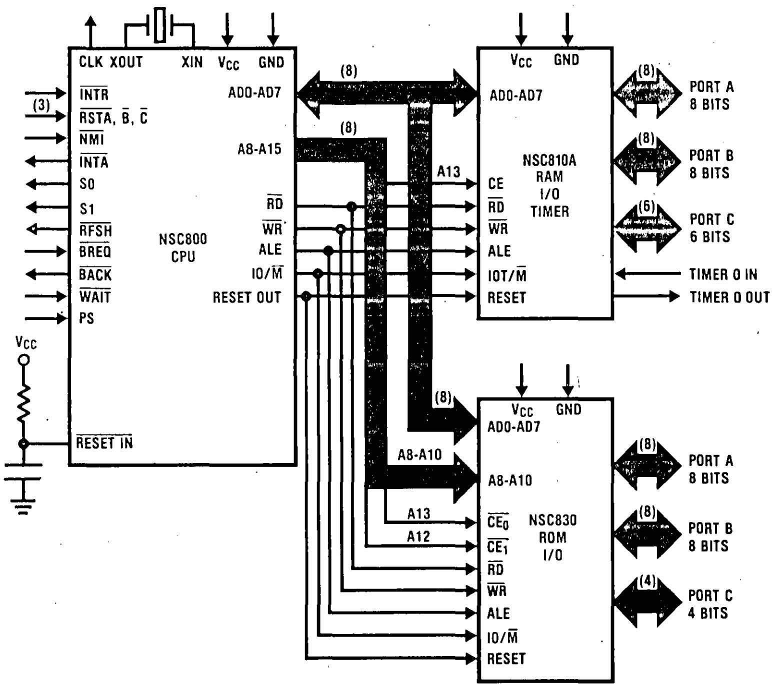
The NSC831 I/O Only is similar to the NSC830 except it has no ROM. The NSC831 is useful for prototyping work prior to ordering the NSC830, and when on-chip ROM is not required.

For military applications the NSC831 is available with class B screening in accordance with methods 5004 of MIL-STD-883.

Features

- 2K x 8 read only memory
- Three programmable I/O ports
- Single 5V Power Supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Directly compatible with NSC800 family
- Strobed modes available on Port A

Microcomputer Family Block Diagram



Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin With Respect to Ground	−0.3V to V_{CC} + 0.3V
V_{CC}	7V
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	1W

Note: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Operating Range V_{CC} = 5V ± 10%

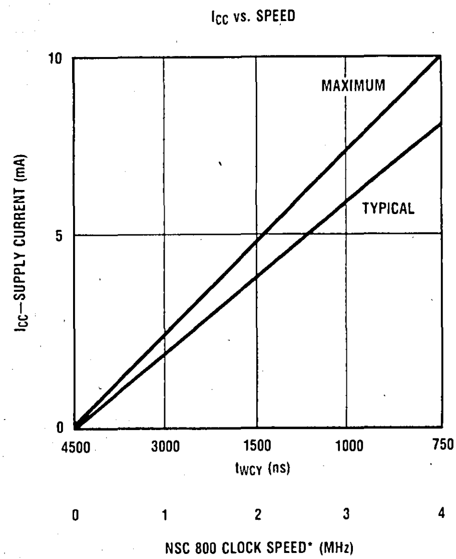
Ambient Temperature	
Military	−55°C to +125°C
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

DC Electrical Characteristics T_A = −55°C to +125°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	I_{OH} = −1.0 mA	2.4			V
		I_{OUT} = −10 μA	V_{CC} − 0.5			V
V_{OL}	Logical 0 Output Voltage	I_{OL} = 2 mA	0		0.4	V
		I_{OUT} = 10 μA	0		0.1	V
I_{IL}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, t_{WCY} = 750 ns		8	10	mA
I_Q	Quiescent Current	No Input Switching, T_A = 25°C		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage		2.4	5	6	V

Low Voltage Operation Preliminary

Voltage	NSC831-1	NSC831	NSC831-4	Units
2.4	—	500	500	kHz
3.0	—	1	1	MHz



*WHEN NSC830/NSC831 IS USED WITH NSC800 TL/C/5594-2

AC Electrical Characteristics

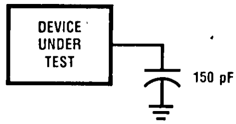
$V_{CC} = 5V \pm 10\%$, GND = 0V
Valid for the following temperature and speed:
NSC830-1, NSC831-1: 0°C to +70°C; −40°C to +85°C
NSC830, NSC831: 0°C to +70°C; −40°C to +85°C; −55°C to +125°C
NSC830-4, NSC831-4: 0°C to +70°C; −40°C to +85°C; −55°C to +125°C

Symbol	Parameter	Test Conditions	NSC830-1 NSC831-1		NSC830 NSC831		NSC830-4 NSC831-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	C_L = 150 pF		1000		400		300	ns
t_{AH}	AD0–AD7, CE, IOT/$\overline{M}$ Hold time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		125		75		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		75		ns
t_{AS}	AD0–AD7, CE, IOT/$\overline{M}$ Set-Up Time		100		75		40		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		310		300	ns
t_{DS}	Data Set-Up Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Set-Up Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Output			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		220		ns
t_{RDD}	Data Bus Disable		0	100	0	100	0	75	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		75		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold With Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to INTR Output			300		300		300	ns
t_{SS}	Peripheral Data Set-Up With Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		340		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

AC Testing Input/Output Waveform

TL/C/5517-3

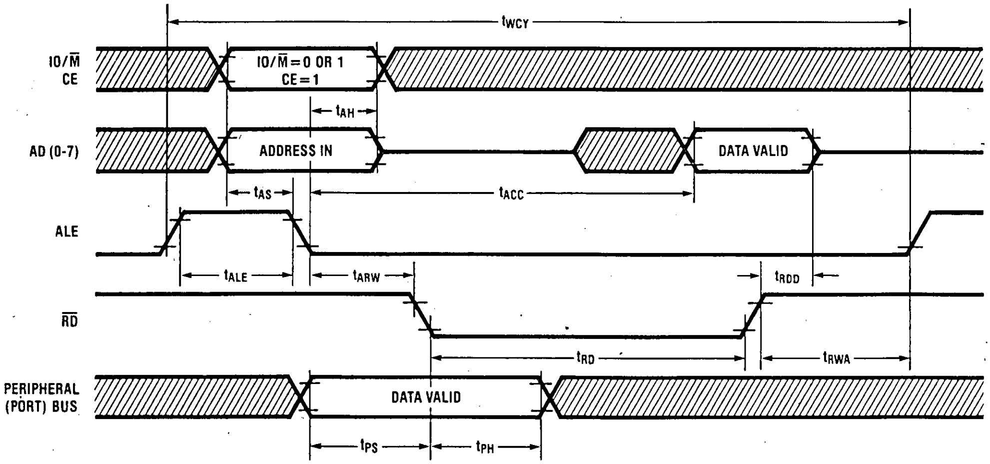
AC Testing Load Circuit



TL/C/5517-4

General Timing Waveforms

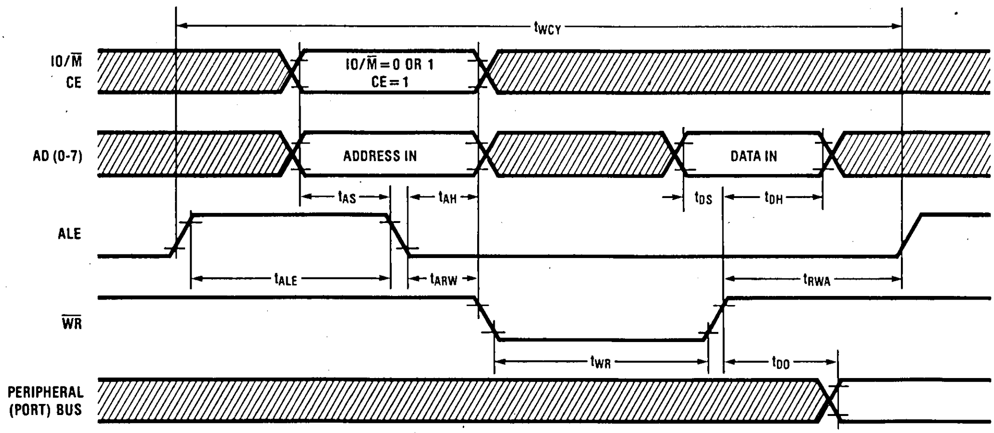
Read Cycle (Read from ROM or Port)



Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-11

Write Cycle (Write to Port)

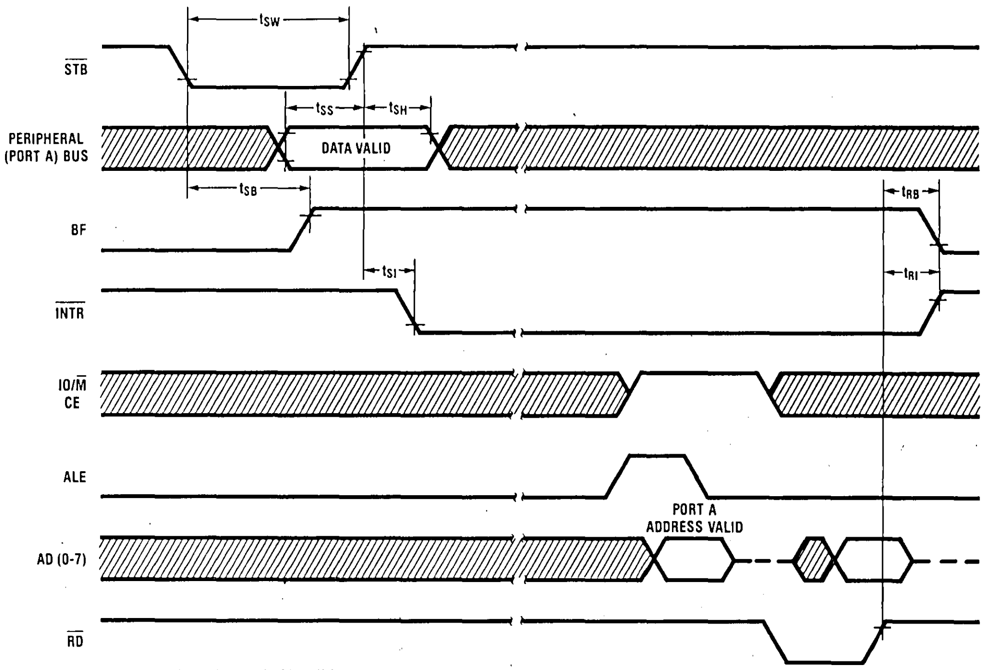


Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-12

Handshake Timing

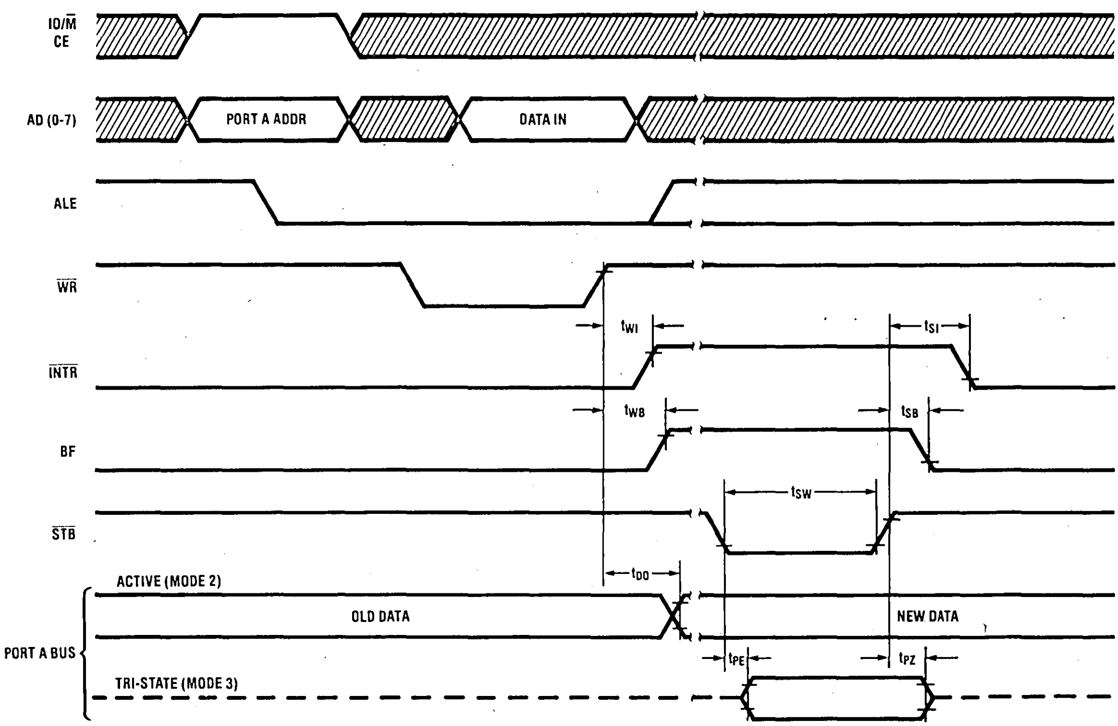
Strobed Mode Output



Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-13

Strobed Mode Input



Note: Diagonal lines indicate interval of invalid data.

TL/C/5594-14

NSC830 Functional Pin Description

The following describes the function of all NSC830 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Master Reset (RESET): An active-high input on the RESET pin initializes the chip causing the three I/O ports (A, B and C) to revert to the input mode. The three ports, the three data direction registers and the mode definition register are reset to low (0).

Input/Output/Memory Select (IO/$\overline{M}$): The IO/$\overline{M}$ pin is a latched, select input line. A high (1) input selects the I/O portion of the chip; a low (0) input selects the ROM portion of the chip. The select input is latched by the trailing edge (high to low transition) of the ALE signal.

Chip Enable ($CE_0/\overline{CE_0}$, $\overline{IOR}/CE_1/\overline{CE_1}$): The chip enable inputs are mask programmable at the factory. The CE inputs permit the use of multiple NSC830s in a system without using a chip select decoder. The CE inputs must be active at the falling edge of ALE. At ALE time, the CE inputs are latched to provide access to the NSC830. The $\overline{IOR}$ input performs the same function as the combination of IO/$\overline{M}$ input high and the $\overline{RD}$ input low.

Read ($\overline{RD}$): When the $\overline{RD}$ (or the $\overline{IOR}$, when mask programmed) input is an active low, data is read from the AD0–AD7 bus. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD0–AD7 bus is in the high impedance state.

Write ($\overline{WR}$): When the CE inputs are active, and the IO/$\overline{M}$ input is high, an active low $\overline{WR}$ input causes the selected output port to be written with the data from the AD0–AD7 bus.

Address Latch Enable (ALE): The trailing edge (high to low transition) of the ALE input signal latches the address/data present on the AD0–AD7 bus, A8–A10 bus, plus the input control signals on IO/$\overline{M}$, $CE_0/\overline{CE_0}$, and $CE_1/\overline{CE_1}$.

Address Bus A8–A10: The high-order bits of the ROM address are input on this 3-bit bus and are latched by the high-to-low transition of the ALE input. These bits do not affect the I/O operations.

Power (V_{CC}): 5V power supply.

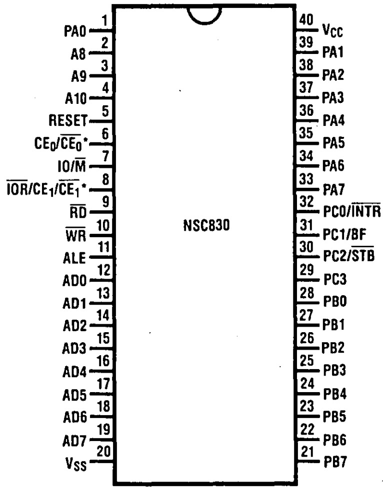
Ground (V_{SS}): Ground reference.

INPUT/OUTPUT SIGNALS

Bidirectional Address/Data Bus AD0–AD7: The lower 8 bits of the ROM or I/O address are applied to these pins, and latched by the trailing edge of ALE. During read operations, 8 bits are present on these pins, and are read when $\overline{RD}$ or $\overline{IOR}$ is low. During an I/O write cycle, Port A, B, or C is written with the data present on this bus at the trailing edge of the $\overline{WR}$ strobe.

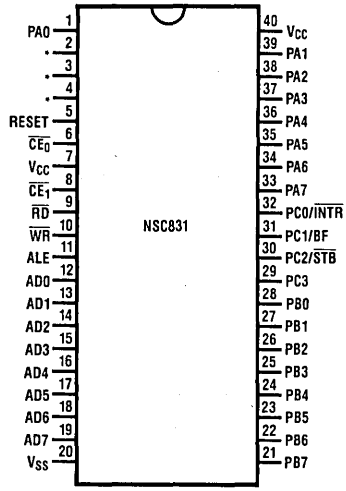
Ports A, B, C (PA0–PA7, PB0–PB7, PC0–PC3): These are general purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDRs).

Connection Diagrams



TOP VIEW TL/C/5594-3

*Pin 6 is mask programmable as CE_0 or $\overline{CE_0}$.
Pin 8 is mask programmable as $\overline{IOR}$, CE_1, or $\overline{CE_1}$.

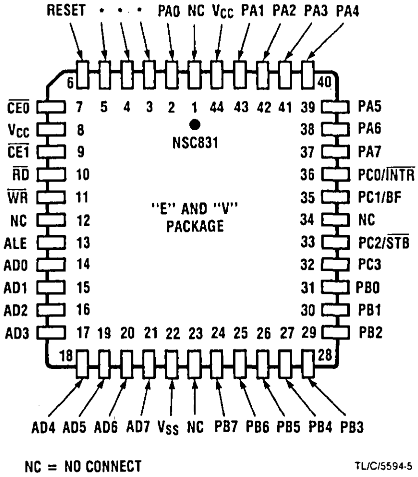


TOP VIEW TL/C/5594-4

*Tie pins 2, 3, and 4 to either V_{CC} or V_{SS}.

See NS Package D40C, J40A or N40A

Connection Diagrams (Continued)



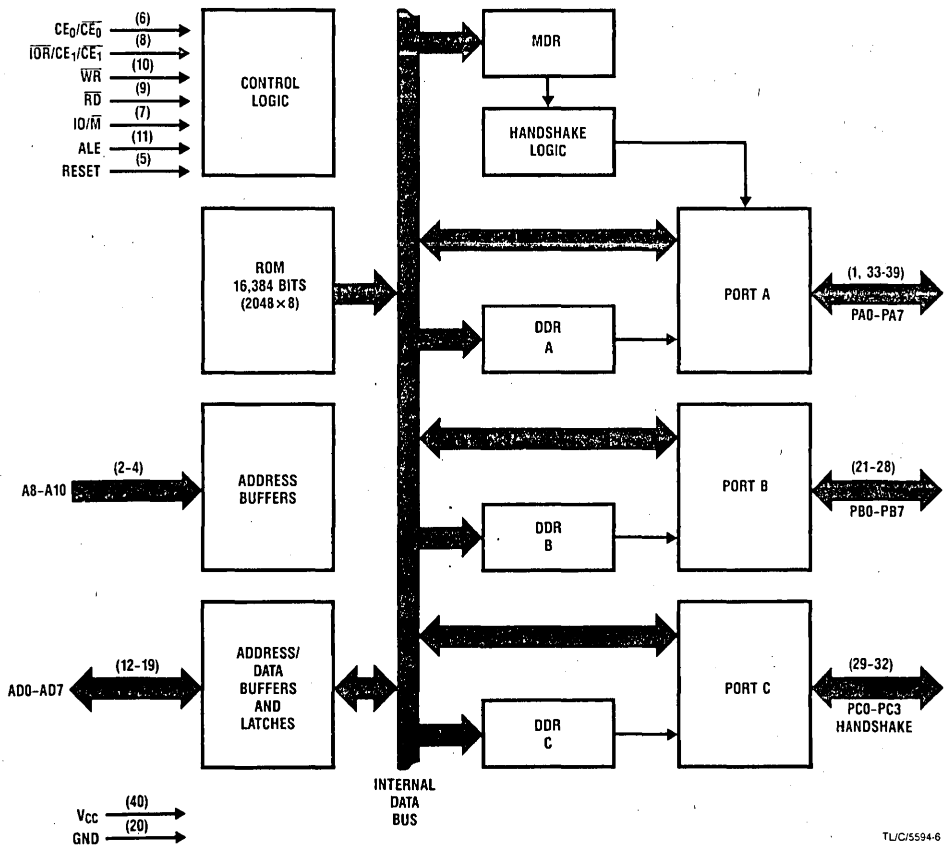
See NS Package ED44A or V44

NSC830 Functional Description

Refer to *Figure 1* for a detailed block diagram of the NSC830, while reading the following paragraphs.

Read Only Memory (ROM): The memory portion of the ROM-I/O is accessed by an 11-bit address input to pins AD0–AD7 and A8–A10. The IO/$\overline{M}$ input must be low (ROM select) and the chip enable pins in the active programmed state at the falling edge of ALE to address the ROM. Timing for ROM read and write operations is shown in the timing diagrams.

Input/Output (I/O): The I/O portion of the NSC830 contains three sets of I/O called Ports. There are two ports (A and B) which contain 8 bits each and one port (Port C) which has 4 bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (4 bits for Port C). When reading Port C, bits 4–7 will be read as ones. All ports share common functions of Read, Write, Bit-Set and Bit-Clear. Additionally, Port A is programmable for strobed (handshake) mode input or output. Port C has a programmable second function for each bit associated with strobed modes. *Table 1* defines the address location of the ports and control registers.



Note: Applicable pinout for 40-pin dual-in-line package within parentheses.

FIGURE 1. NSC830 Block Diagram

Table 1. I/O and Address Designations

8-Bit Address Field Bits 7	6	5	4	3	2	1	0	Designation I/O Port, etc.	R (Read) W (Write)
X	X	X	X	0	0	0	0	Port A (byte)	R/W
X	X	X	X	0	0	0	1	Port B (byte)	R/W
X	X	X	X	0	0	1	0	Port C (byte)	R/W
X	X	X	X	0	0	1	1	Not Used	—
X	X	X	X	0	1	0	0	DDR — Port A	W
X	X	X	X	0	1	0	1	DDR — Port B	W
X	X	X	X	0	1	1	0	DDR — Port C	W
X	X	X	X	0	1	1	1	Mode Definition Register	W
X	X	X	X	1	0	0	0	Port A — Bit Clear	W
X	X	X	X	1	0	0	1	Port B — Bit Clear	W
X	X	X	X	1	0	1	0	Port C — Bit Clear	W
X	X	X	X	1	0	1	1	Not Used	—
X	X	X	X	1	1	0	0	Port A — Bit Set	W
X	X	X	X	1	1	0	1	Port B — Bit Set	W
X	X	X	X	1	1	1	0	Port C — Bit Set	W
X	X	X	X	1	1	1	1	Not Used	—

Note: X = don't care

MODE DEFINITION REGISTER (MDR)

The Mode Definition Register (MDR) defines the operating mode for Port A. While Ports B and C are always in the basic I/O mode, there are four operating modes for Port A:

Mode 0 — Basic I/O (Input or Output)

Mode 1 — Strobed Mode Input

Mode 2 — Strobed Mode Output
- Active Peripheral Bus

Mode 3 — Strobed Mode Output
- TRI-STATE (high impedance) Peripheral Bus

The MDR has the I/O address assignment XXX00111. The bit configuration for the mode selection is illustrated below:

Mode	Bit 7	6	5	4	3	2	1	0
0	X	X	X	X	X	X	X	0
1	X	X	X	X	X	X	0	1
2	X	X	X	X	X	0	1	1
3	X	X	X	X	X	1	1	1

Note: X = don't care

DATA DIRECTION REGISTERS (DDR)

Each port bit has a data direction register (DDR) which defines the I/O state of the bit. The bit is configured as an input if a "0" is written into its DDR, or as an output if a "1" is written. The DDR bits cannot be individually written to; the entire DDR byte is affected by a write to the DDR address. Thus all data must be consistent with the direction desired for each port.

Any write or read operations on a port contradicting the DDR will not affect the port output or input. However, a read of a port bit defined as an output will cause a read from the output latch, and a write to a port bit defined as an input will modify the output latch.

PORT FUNCTIONS — BASIC I/O

Basic I/O is the mode of operation of Ports B and C and mode 0 of Port A (defined by the MDR). Read, write, and bit operations can be executed in the basic I/O mode. The timing for basic input and basic output modes is shown in the AC Characteristics tables.

When a read occurs the information is latched from the peripheral bus on the leading (falling) edge of the $\overline{RD}$ strobe. When a write occurs the port bus is modified after the trailing (rising) edge of the $\overline{WR}$ strobe with data from the AD bus. Port output data remains valid on the output pin from one trailing edge of $\overline{WR}$ strobe to the trailing edge of the next $\overline{WR}$ strobe.

BIT OPERATIONS

The I/O features of the ROM-I/O allow modification of a single bit or several bits of a port with Bit-Set and Bit-Clear (see *Figure 2*). The address is set up to indicate that a bit set (or clear) is taking place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing "1s" will cause the indicated operation to be performed on the corresponding port bit. All bits of the data mask with "0s" cause the corresponding port bits to remain unchanged. Three sample operations are given, using Port B as an example:

Operation	Set B7	Bit B2 and B0	Set B4, B3 and B1
Address	XXX01101	XXX01001	XXX01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

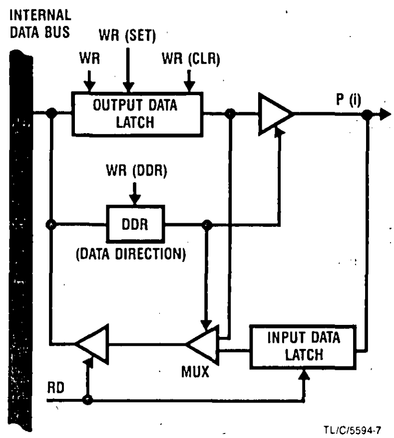


FIGURE 2. Block Diagram for Port Bit (i)

PORT A — STROBED (HANDSHAKE) MODE

Port A can be programmed (via the MDR) into one of 3 types of strobed mode for handshake communication with intelligent peripherals. When Port A is in mode 1, 2, or 3 (see description of MDR), Port C pins 0, 1, and 2 are used as signals to and from the peripheral and to the CPU, controlling handshake operations. These control signals are designated $\overline{\text{STB}}$, BF, and $\overline{\text{INTR}}$. Timing parameters and timing diagrams are detailed under AC Characteristics.

$\overline{\text{INTR}}$ (Strobe Mode Interrupt) is an active-low interrupt from the I/O to the CPU. In strobed input mode, the CPU reads the valid data at Port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writting to Port A.

The $\overline{\text{INTR}}$ output can be enabled or disabled, thus giving the ability to control strobed data transfer under software control. It is enabled or disabled respectively, by setting (= 1) or clearing (= 0) the output data latch of bit 2, port C. Port bit PC2 is used as the $\overline{\text{STB}}$ input. Since PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{\text{INTR}}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{\text{INTR}}$ pin for strobed operation. Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear instructions. The Port C byte write command will not alter the output data latch of the PC2 during the strobed mode of operation.

$\overline{\text{STB}}$ (Strobe) is an active-low input from the peripheral device, signaling that data transfer is about to begin. This strobe is interpreted as an "output request" if Port A is in a strobed output mode, or as a "data valid" signal if Port A is in strobed input mode.

BF (Buffer Full) is an output from the I/O to the peripheral signaling that data transfer is complete. In strobed input mode this strobe indicates that data is received into Port A and that no further data should be transmitted by the peripheral device until the port has been read (emptied). In strobed output mode the BF indicates that the request from the peripheral has been processed by the CPU and the valid data now appears in Port A.

The bits of Port C that are used for handshake control of Port A (bits C0, C1, and C2) must be direction-defined appropriately in the DDR. Also, the DDR of Port A must be consistent with the mode specified in the MDR. Register set-up configurations for the three handshake modes are illustrated in Table 2.

Table 2. Mode Definition Register Configurations

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Strobed Input	XXXXXX01	00000000	XXX011	XXX1XX
Strobed Output (Active)	XXXXX011	11111111	XXX011	XXX1XX
Strobed Output (TRI-STATE)	XXXXX111	11111111	XXX011	XXX1XX

NSC831/833B MIL-STD-883 Class B Screening

National Semiconductor offers the NSC831D and NSC831E with full class B screening per MIL-STD-883B for Military/Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

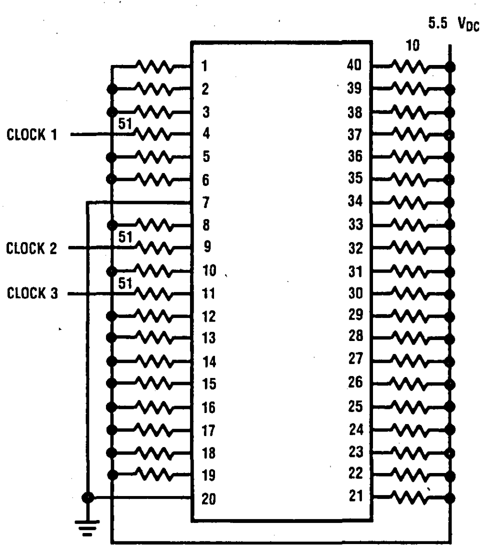
Electrical testing is performed in accordance with RET831X which tests or guarantees all of the electrical performance characteristics of the NSC831 data sheet. A copy of the current revision of RET831X is available upon request. The following table is the MIL-STD-883 flow as of the date of publication.

100% SCREENING FLOW

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010B	100%
Stabilization Bake	1008C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010C 10 Cycles −65°C/+150°C	100%
Constant Acceleration	2001E 30,000 Gs, Y1 Axis	100%
Fine Leak	1014B 5×10^{-8}	100%
Gross Leak	1014C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS831X	100%
PDA	10% Max	
	+125°C AC and DC per RETS831X	100%
	−55°C AC and DC per RETS831X	100%
	+25°C AC per RETS831X	100%
QA Acceptance	Group A (sample, each lot)	
Quality Conformance	Group B (sample, each inspection lot)	
	Group C (sample, every 90 days per microcircuit group)	
	Group D (sample every 6 months per package type)	
External Visual	2009	100%

Burn-In Circuit

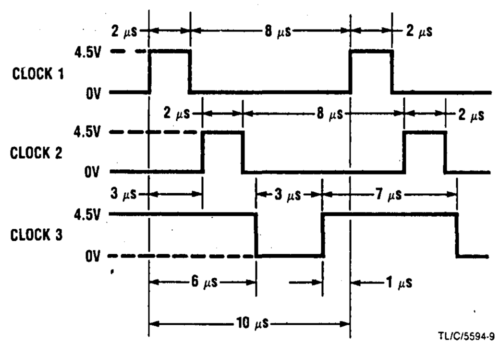
5243HR
NSC831D/883B (Dual In-Line)



TL/C/5594-8

Timing Diagram

Input Clocks



TL/C/5594-9

Note 1: All resistors ±5%, 1/4 watt unless otherwise designated, 125°C operating life circuit.

Note 2: E package burn-in circuit 5556HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V

Note 5: Device to be cooled down under power after burn-in.

APPROVED FORMATS FOR CUSTOM PROGRAMMED PARTS

Input Medium:

2716 EPROM
2708 EPROM
Paper Tape

IMPORTANT — EPROM LABELING

Only one customer program may be included in a single order. The following method must be used to identify the EPROMs comprising a program.

a. The EPROMs used for storing a custom program are designated as shown:

2716:	Block A	0–2047
2708:	Block A	0–1023
	Block B	1024–2047

b. All EPROMs must be labeled (stickers, paint, etc.) with this block designation plus a customer assigned print or identification number.

Example:

1. Customer Data
   - Custom Program Length — 2K
   - Medium — Two 2708s
   - Customer Print or I.D. No. C123-45
2. EPROM Labels

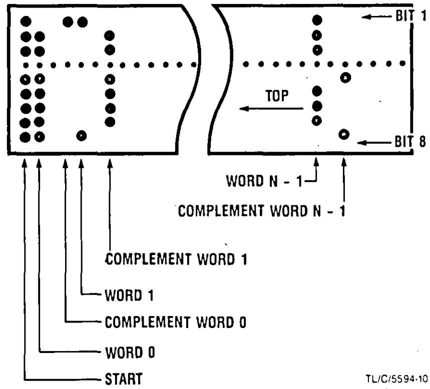
C123-45 A 0–1023	C123-45 B 1024–2047

Paper Tape

Tapes may only be submitted in binary complement format. The following information should be written on the paper tape.

Company Name
Customer Print or I.D. No.
NSC Part No.
A Punch = ("1" or "0")
This is _____ logic (POS or NEG)

BINARY COMPLEMENT FORMAT



TL/C/5594-10

Note 1: Tape must be blank except for the data words.

Note 2: Tape must start with a rubout character.

Note 3: Data is comprised of two words, the first being the actual data and the second being the complement of the data.

Verification

You will receive a listing of the options ordered and the input data. If you also wish to receive EPROMs for verification, please send additional blank EPROMs as necessary for this purpose. You can use software (the listing) or hardware (EPROMs) to verify the program.

You will be asked for a GO/NO GO response within one week after you receive the listing.

VERIFICATION LISTING

The verification listing has six sections:

1. A cover sheet with provision for "STOP, DO NOT PROCEED" or "VERIFICATION CERTIFIED" signatures.
2. Description of the options you have chosen.
3. A description of the log designations and assumptions used to process the data.
4. A listing of the data you have submitted.
5. An error summary.
6. A definition of the standard logic definitions for the ROM and the reduced form of the data. This list shows the output word corresponding to each address coded in binary.

ORDERING INFORMATION FOR CUSTOM PROGRAMMED PARTS

The following information must be submitted with each custom ROM program. An order will not be processed unless it is accompanied by this information.

Person (Customer, Sales Representative, etc.) to whom Verification Package be sent:	NATIONAL PART NUMBER AND PACKAGE
Name	ROM Letter Code (National Use Only)
Company	Customer Name and Location
Address	Customer Print or I.D. Number for this ROM Program
City, State, and Zip Code	Purchase Order Number
Person (Customer) NS Can Contact for Technical Questions	Device Marking Instruction (Unless otherwise instructed, NS will always mark devices with Date Code, National Part No., and ROM Code. Any additional marking should be shown below.)
Telephone Number	
Sales Representative	Customer Service Representative

INPUT MEDIUM

See following page for approved formats. Please check the medium you are using:

- ☐ Paper Tape
- ☐ 2716 EPROM
- ☐ 2708 EPROM

_____Total number of EPROMs

OPTIONS FOR NSC830 ROM — I/O

Option 1 = ☐

CE_0 Select, enter: 0 for CE_0
1 for $\overline{CE_0}$

Option 2 = ☐

CE_1/IOR Select, enter: 0 for IOR
1 for CE_1
2 for $\overline{CE_1}$

Ordering Information

NSC830XXX X X X X

- /A+ = A+ Reliability Screening
- I = Industrial Temperature (−40°C to +85°C)
  M = Military Temperature (−55°C to = +125°C)
  No Designation = Commercial Temperature (0°C to +70°C)
- −1 = 1 MHz Clock Output (Note 1)
  −4 = 4 MHz Clock Output
  No Designation = 2.5 MHz Clock Output
- D = Ceramic Package
  J = Cerdip Package (Availability to be announced)
  N = Plastic Package
  E = Ceramic Leadless Chip Carrier (LCC)
  V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)
- Unique ROM code (Alpha characters assigned by National)

Note 1: −1 part only available in D-1, N-1, D-1I, N-1I, V-1, V-1I

Examples

NSC830XXX/N
NSC830XXX/E-4/A+

Reliability Information (NSC830)

Gate Count* 2150 (min)
2278 (max)

Transistor Count* 8500 (min)
24,884 (max)

*Dependent on ROM program size.

Ordering Information

NSC831 X X X X

- /A+ = A+ Reliability Screening
  /883 = MIL-STD-883B Screening (Note 1)
- I = Industrial Temperature (−40°C to +85°C)
  M = Military Temperature (−55°C to = +125°C)
  No Designation = Commercial Temperature (0°C to +70°C)
- −1 = 1 MHz Clock Output (Note 2)
  −4 = 4 MHz Clock Output
  No Designation = 2.5 MHz Clock Output
- D = Ceramic Package
  J = Cerdip Package (Availability to be announced)
  N = Plastic Package
  E = Ceramic Leadless Chip Carrier (LCC)
  V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)

Note 1: Do not specify a temperature option: all parts are screened to military temperature.

Note 2: −1 part only available in D-1, N-1, D-1I, N-1I, V-1, V-1I.

Examples

NSC831E-4/883
NSC831N
NSC831D-1I/A+

Reliability Information (NSC831)

Gate Count 1900

Transistor Count 7400

National Semiconductor

PRELIMINARY

microCMOS

NSC858 Universal Asynchronous Receiver/Transmitter

General Description

The NSC858 is a CMOS programmable Universal Asynchronous Receiver/Transmitter (UART) which includes a programmable baud rate generator on chip and is packaged in various 28-pin packages. The chip, which is fabricated using microCMOS silicon gate technology, functions as a receiver, transmitter, and an input/output interface for your microcomputer system.

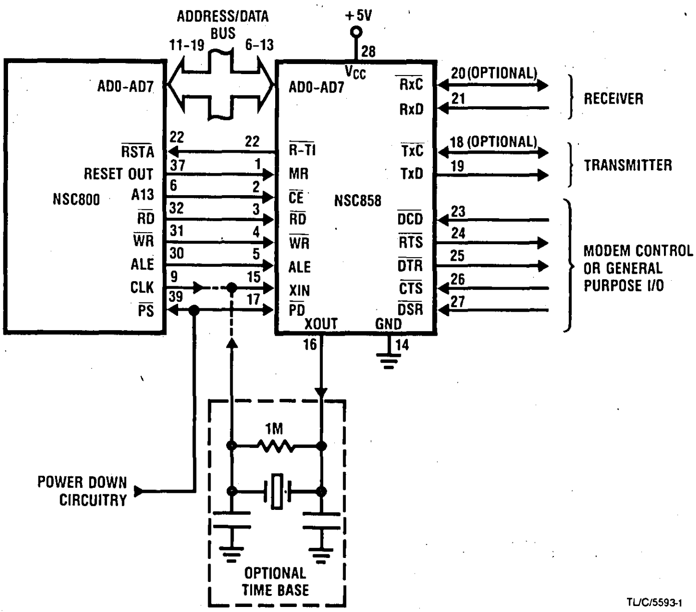
Parallel data from the CPU is converted to serial form by the transmitter, where it is shifted out in the standard asynchronous communication data format. Appropriate start, parity, and stop bits are added to the outgoing serial stream. Incoming serial data is converted to parallel form by the receiver. The incoming data is checked for errors (parity, overrun, framing or break interrupt) and then converted from serial to parallel for transfer to the CPU. Five pins on the chip are available for modem control functions or they can be used as general purpose I/O.

The NSC858 includes a programmable baud generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16} – 1), and producing a 1X, 16X, 32X, 64X clock for driving the transmitter and/or receiver logic. Both the transmitter and receiver can either be driven by an external clock or the internal baud rate generator. The NSC858 has an interrupt system that can be tailored to the user's requirements. In addition to the CMOS power consumption levels there are hardware and software power down modes which further reduce power consumption levels.

Features

- Asynchronous operation
- Maximum baud rate 256K BPS (16X), 1M BPS (1X)
- Programmable baud rate generator
- Double buffered receiver and transmitter
- Independently configured receiver and transmitter
  - 5-, 6-, 7-, 8-bit characters
  - Odd, even, force high, force low, or no parity
  - 1, 1½, 2 stop bits
- Five bits modem I/O or general purpose I/O (3 input, 2 output)
- Programmable auto enables for $\overline{CTS}$ and $\overline{DCD}$
- Local and remote loopback diagnostics
- False start bit detection
- Break condition detection and generation
- Program polled, or interrupt driven operation
  - 8 maskable status conditions for receiver and transmitter interrupt
  - 4 maskable status conditions for modem interrupt
- Variable power supply (2.4V–6.0V)
- Low power consumption with software and hardware power down modes
- 8-bit multiplexed address/data bus directly compatible with NSC800

System Configuration



TL/C/5593-1

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} + 0.3V
Maximum V_{CC}	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions V_{CC} = 5V ± 10%

Ambient Temperature	
Military	−55°C to +125°C
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V, unless otherwise specified.

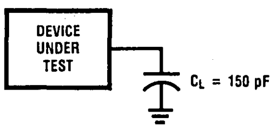
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{HY}	Hysteresis at RESET IN Input	V_{CC} = 5V	0.25	0.5		V
V_{OH1}	Logical 1 Output Voltage	I_{OUT} = −1.0 mA	2.4			V
V_{OH2}	Logical 1 Output Voltage	I_{OUT} = −10 μA	V_{CC} − 0.5			V
V_{OL1}	Logical 0 Output Voltage	I_{OL} = 2 mA	0		0.4	V
V_{OL2}	Logical 0 Output Voltage	I_{OUT} = 10 μA	0		0.1	V
I_{IL}	Input Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
I_{OL}	Output Leakage Current	0 ≤ V_{IN} ≤ V_{CC}	−10.0		10.0	μA
I_{CCA}	Active Supply Current			10		mA
I_{HPD}	Current Hardware Power Down	Pin $\overline{PD}$ = 0		100		μA
I_{SPD}	Current Software Power Down	Power Down Reg Bit 0 = 1		200		μA
I_{CQ}	Quiescent Current	T_A = 25°C		100		μA
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			8	12	pF
V_{CC}	Power Supply Voltage		2.4	5	6	V

Note 1: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

AC Testing Input/Output Waveform

TL/C/5593-3

AC Testing Load Circuit



TL/C/5593-4

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V, C_L = 150 pF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BUS						
t_{AS}	Address 0–7 Set-Up Time		40			ns
t_{AH}	Address 0–7 Hold Time		30			ns
t_{ALE}	ALE Strobe Width (High)		100			ns
t_{ARW}	ALE to Read or Write Strobe		100			ns
t_{CRW}	Chip Enable to Read or Write		100			ns
t_{RD}	Read Strobe Width		250	375		ns
t_{DDR}	Data Delay from Read	C_L = 150 pF		180	200	ns
t_{RDD}	Data Bus Disable	C_L = 150 pF		50		ns
t_{CH}	Chip Enable Hold After Read or Write		100			ns
t_{RWA}	Read or Write to Next ALE		100			ns
t_{WR}	Write Strobe Width		200	250		ns
t_{DS}	Data Set-Up Time			100		ns
t_{DH}	Data Hold Time			100		ns
MODEM						
t_{MD}	$\overline{WR}$ Command Reg. to Modem Outputs Delay	150 pF Load		180		ns
t_{SIM}	Delay to Set Interrupt from Modem Input			200		ns
t_{RIM}	Delay to Reset Modem Status Interrupt from $\overline{RD}$			240		ns
t_{SMI}	$\overline{WR}$ to Status Mask Reg., Delay to $\overline{RTI}$			220		ns
POWER DOWN						
t_{PCS}	Power Down to All Clocks Stopped			1	2	$t_{BIT} + t_{XC}$
t_{PCR}	Power Down Removed to Clocks Running			1	2	$t_{BIT} + t_{XC}$
t_{PXS}	Power Down Removed to XTAL Oscillator Stable	When Using On Chip Inverter for Oscillator Circuit		100		ms
t_{PSE}	Power Down Set-Up Before $\overline{RD}$ or $\overline{WR}$ Edge		160	260		ns
t_{EPI}	$\overline{WR}$ or $\overline{RD}$ Edge Following $\overline{PD}$ to Internal Signals	Enable or Disable		100		ns
BAUD GENERATOR						
t_{XH}	XTAL In High		100			ns
t_{XL}	XTAL In Low		100			ns
f_{BRC}	Baud Rate Clock Input Frequency				4.1	MHz
t_{BD1}	Baud Out Delay ÷1			160		ns
t_{BD2}	Baud Out Delay ÷2			200		ns
t_{BD3}	Baud Out Delay ÷3			200		ns
t_{BDN}	Baud Out Delay ÷N > 3			200		ns
t_{XC}	Baud Clock Cycle	$t_{XC} = \frac{1}{f_{BRC}}$	243			ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TRANSMITTER						
t_{TCD}	TxD Delay from $\overline{TxC}$	External Clock		220		ns
		Internal Clock		140		ns
t_{TXC}	Cycle Time $\overline{TxC}$	16X, 32X, 64X Clock Factor	243			ns
		1X Clock Factor	1000			ns
t_{TCH}	$\overline{TxC}$ High		100			ns
t_{TCL}	$\overline{TxC}$ Low		100			ns
t_{HRI}	$\overline{WR}$ TxHR to Reset TxBE $\overline{RTI}$			260		ns
t_{HTS}	$\overline{WR}$ TxHR to TxD Start		2	3	4	t_{BIT}
t_{TSI}	Skew Start Bit to $\overline{RTI}$		−100	+20	+120	ns
t_{ETS}	Enable Tx to Start Bit		3	4	5	t_{BIT}
t_{BIT}[1]	One Bit Time	1X	1000			ns
		16X	3.88			μs
		32X	7.77			μs
		64X	15.55			μs
RECEIVER						
t_{RS}	RxD Set-Up	1X Clock Factor		160		ns
t_{RH}	RxD Hold	1X Clock Factor		100		ns
t_{RXC}	Cycle Time $\overline{RxC}$	16X, 32X, 64X Clock Factor	243			ns
		1X Clock Factor	1000			ns
t_{RCH}	$\overline{RxC}$ High		100			ns
t_{RCL}	$\overline{RxC}$ Low		100			ns
t_{RRI}	$\overline{RD}$ to Reset $\overline{RTI}$	150 pF Load		300		ns
t_{BIT}[1]	One Bit Time	1X	1000			ns
		16X	3.88			μs
		32X	7.77			μs
		64X	15.55			μs
t_{ERS}	Enable Rx to Correctly Detect Start Bit	All Clock Factors	2	3	4	t_{RXC}
t_{RNO}	Read RxHR Before Next Data; No OE		240			ns
t_{BI}	$\overline{RxC}$, Break to $\overline{RTI}$			340		
t_{REI}	Receiver Error Int			½ Clock Factor		t_{RXC}
t_{RDI}	Receiver Ready Int			$t_{REI}+t_i$		t_{RXC}
t_{RSI}	$\overline{RxC}$ to $\overline{RTI}$			300		ns
RESET TIMING						
t_{MR}	MR Pulse Width			100		ns
t_{RA}	MR to ALE if Valid $\overline{WR}$ or $\overline{RD}$ Cycle			100		ns

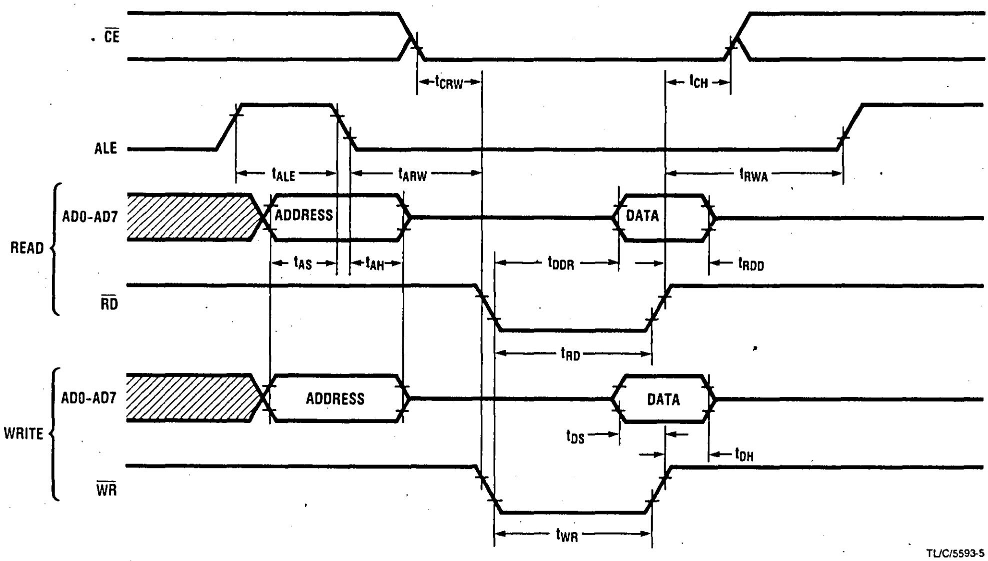
Note 1: $t_{BIT} = t_{TXC} \times$ Clock Factor (1, 16, 32, 64), transmitter

$t_{BIT} = t_{RXC} \times$ Clock Factor (1, 16, 32, 64), receiver

$$t_{BIT} = \frac{1}{\text{Baud Rate}}$$

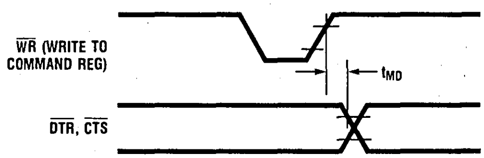
Timing Waveforms

Read and Write Cycles

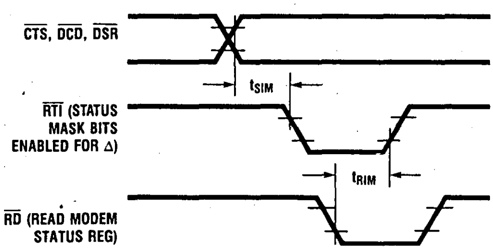


TL/C/5593-5

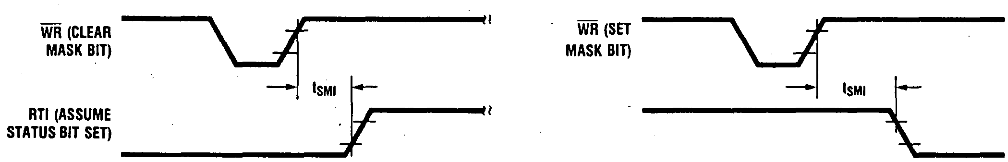
Modem Timing



TL/C/5593-19



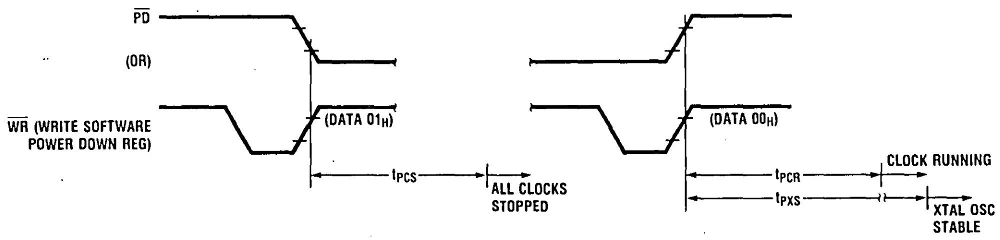
TL/C/5593-20



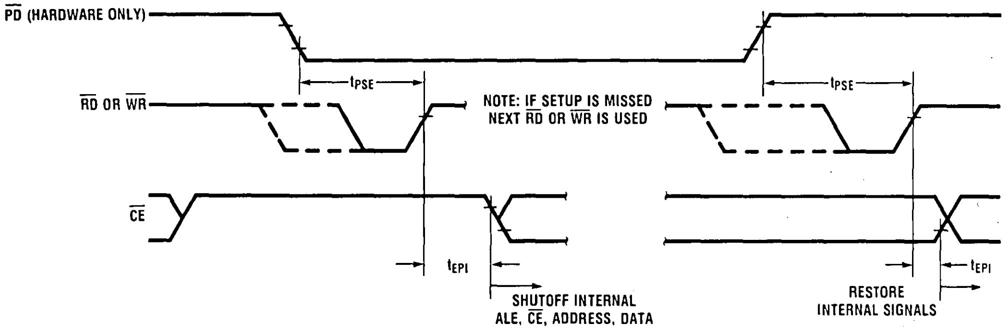
TL/C/5593-21

Timing Waveforms (Continued)

Power Down Timing

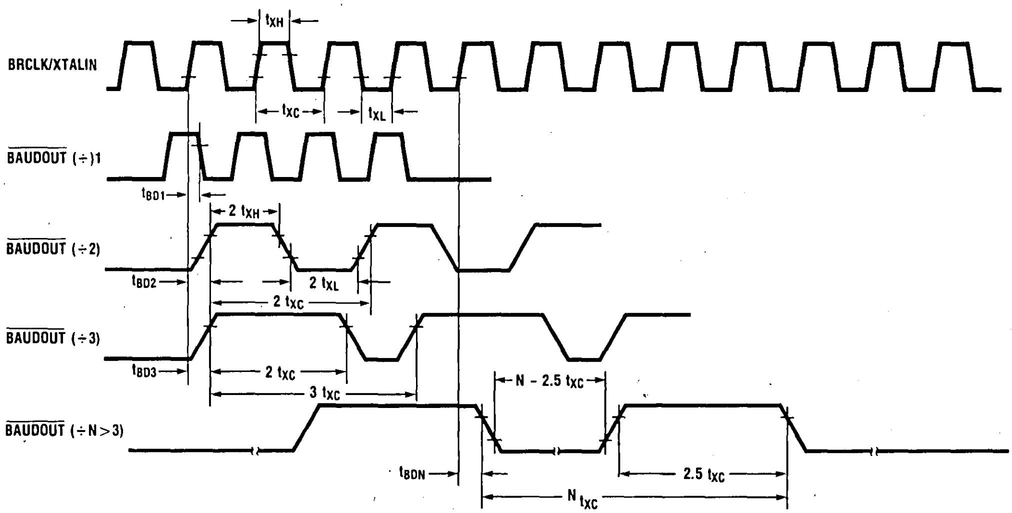


TL/C/5593-7



TL/C/5593-8

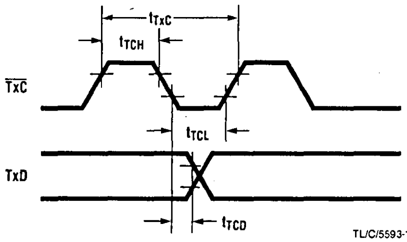
Baud Out Timing



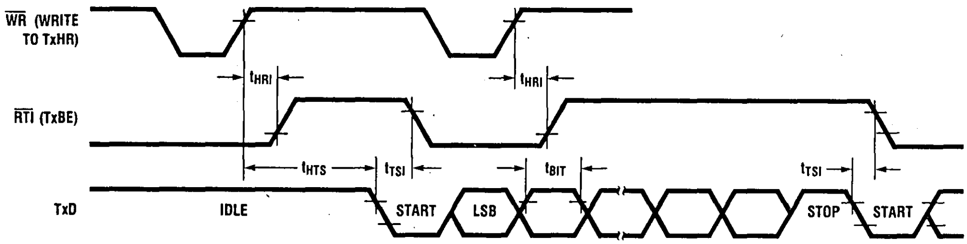
TL/C/5593-9

Timing Waveforms (Continued)

Transmitter Timing

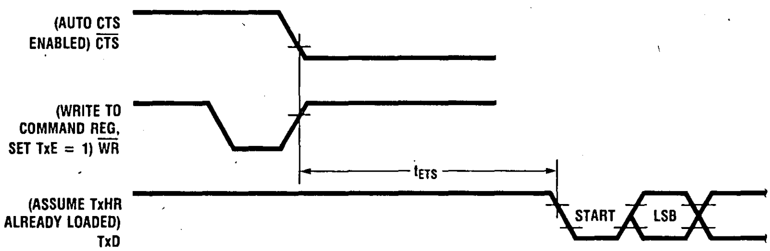


TL/C/5593-10



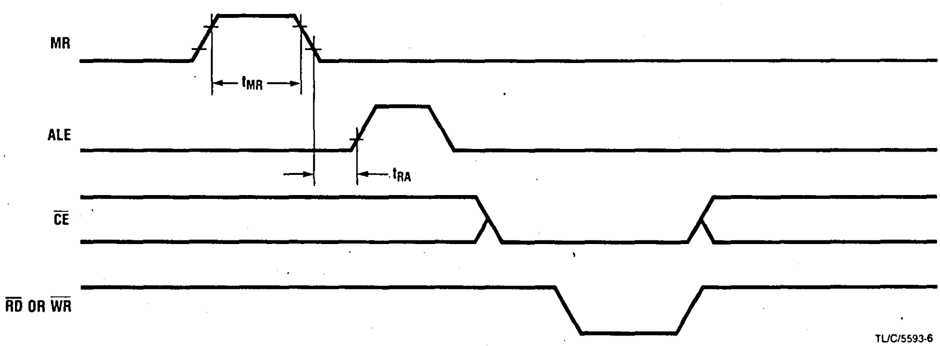
$$t_{BIT} = \frac{1}{\text{BAUD RATE}} = t_{TxC} \times \text{CLOCK FACTOR (1, 16, 32, 64)}$$

TL/C/5593-11



TL/C/5593-12

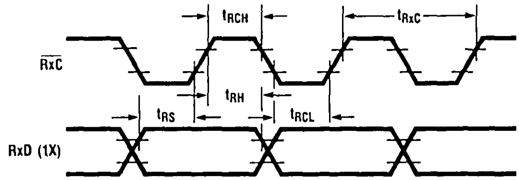
Reset Timing



TL/C/5593-6

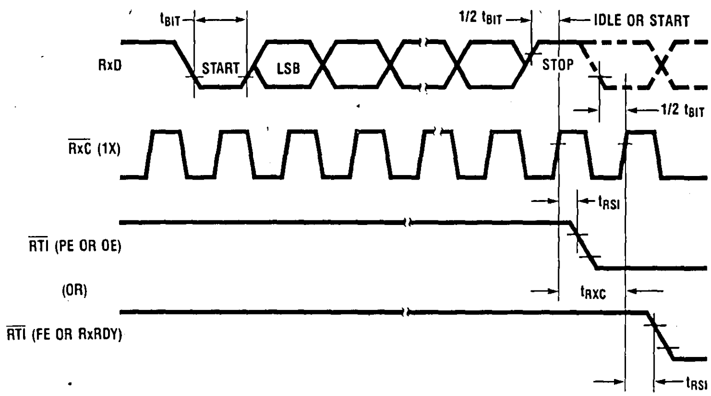
Timing Waveforms (Continued)

Receiver Timing

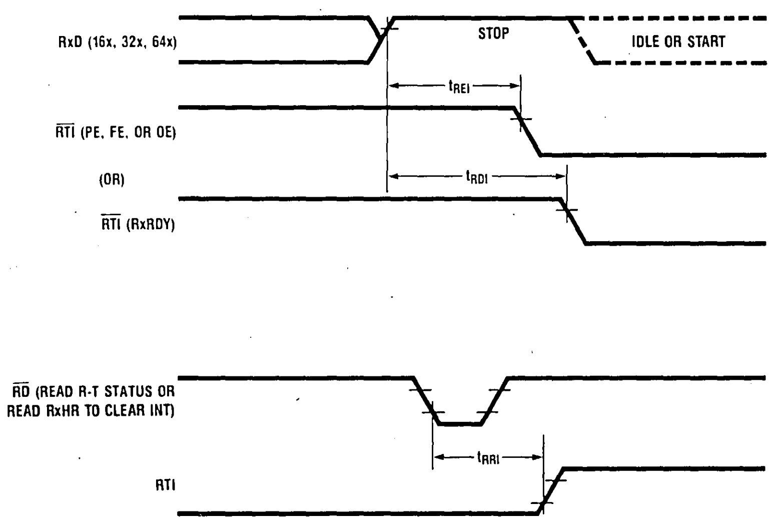


TL/C/5593-13

$$t_{BIT} = \frac{1}{\text{BAUD RATE}} = t_{RxC} \times \text{CLOCK FACTOR (1, 16, 32, 64)}$$



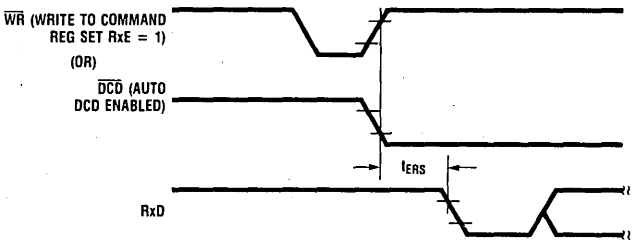
TL/C/5593-14



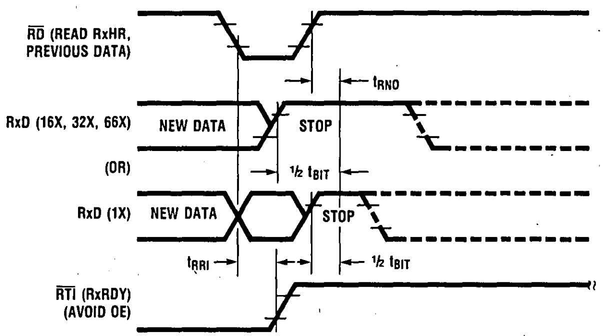
TL/C/5593-15

Timing Waveforms (Continued)

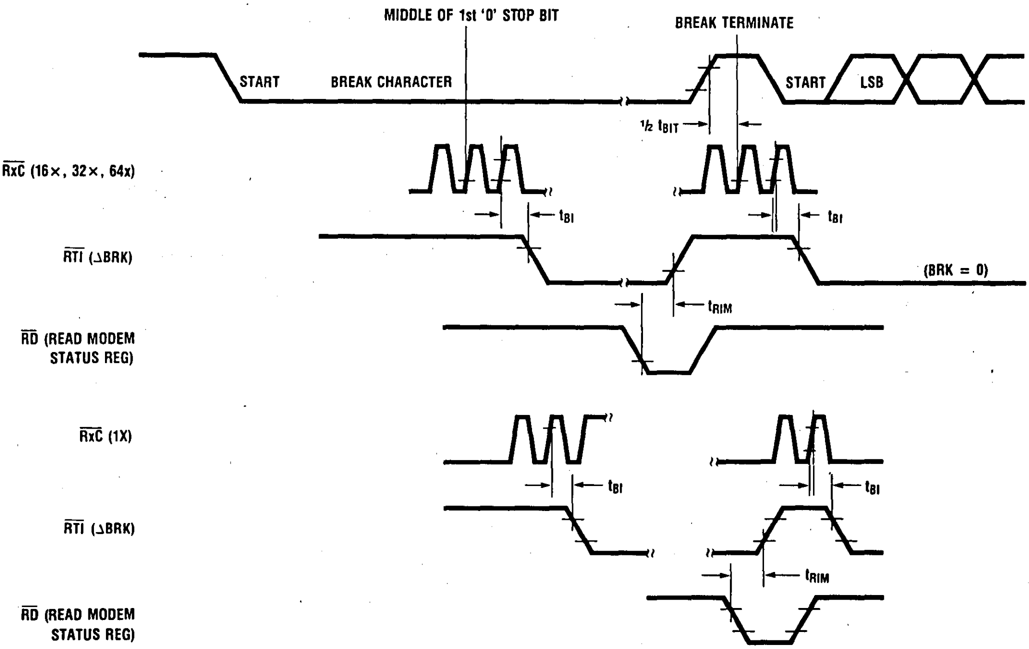
Receiver Timing (Continued)



TL/C/5593-16



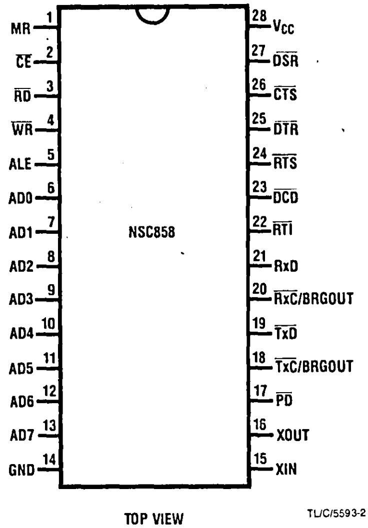
TL/C/5593-17



TL/C/5593-18

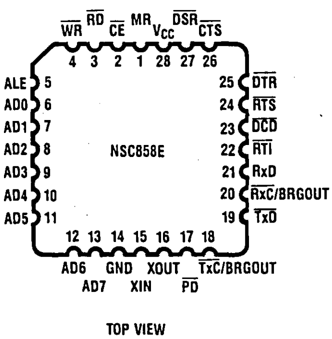
Connection Diagrams

Dual In-Line Package



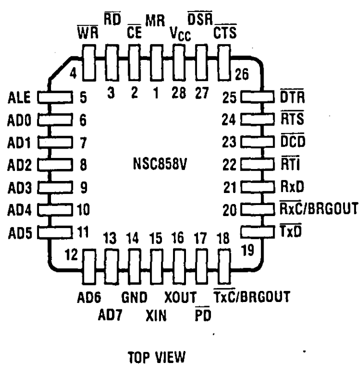
See NS Package D28C, J28B or N28B

E Package



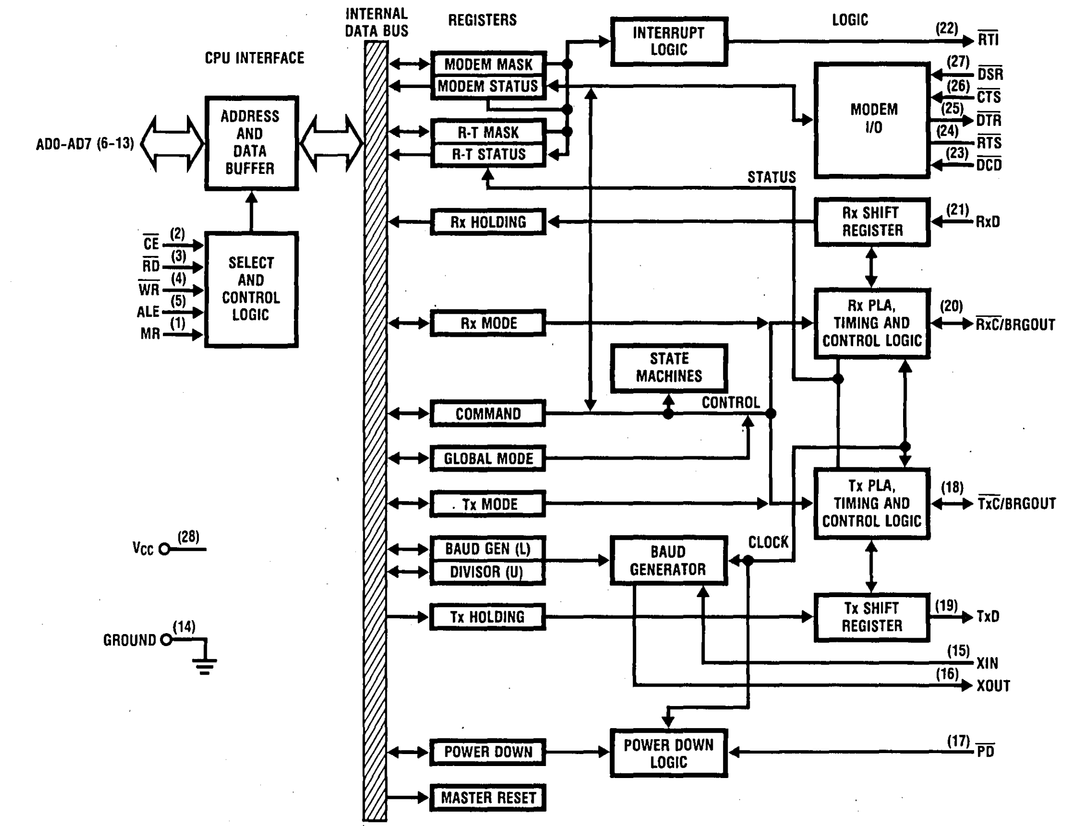
See NS Package ED28A

V Package



See NS Package V28

Block Diagram



TL/C/5593-22

Functional Pin Description

INPUT SIGNALS

Master Reset (MR): active high, Pin 1. This Schmitt trigger input has a 0.5V typical hysteresis. When high, the following registers are cleared: receiver mode, transmitter mode, global mode, R-T status (except for TxBE which is set to one), R-T status mask, modem mask, command (which disables receiver "Rx" and the transmitter "Tx"), power down, and receiver holding. In the modem status register, ΔCTS, ΔDCD, ΔDSR, BRK and ΔBRK are cleared.

Chip Enable ($\overline{\text{CE}}$): active low, Pin 2. Chip enable must be low during a valid read or write pulse in order to select the device. Chip enable is not latched.

Read ($\overline{\text{RD}}$): active low, Pin 3. When Read line is low while the chip is selected the CPU is able to read data or information from selected registers in the NSC858.

Write ($\overline{\text{WR}}$): active low, Pin 4. When Write line is low while the chip is selected the CPU is able to write data or information to selected registers in the NSC858.

Address Latch Enable (ALE): negative edge sensitive, Pin 5. The negative edge (high to low) of ALE latches the address for the register select during a read or write operation.

Power Down ($\overline{\text{PD}}$): active low, Pin 17. When active disables all internal clocks, shuts off the oscillator, clears RxE, TxE, and break control bits in the command register. All other registers retain their data. Unlike software power down, $\overline{\text{PD}}$ also disables the internal ALE, $\overline{\text{CE}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and address data paths for minimum power consumption. Registers cannot be accessed in hardware power down; they may be in software power down.

Receiver Data (RxD): Pin 21. Serial data input from the communications link (peripheral device, modem, or data set). Serial data is received least significant bit (LSB) first. "Mark" is high (1), "space" is low (0).

Data Carrier Detect ($\overline{\text{DCD}}$): active low, Pin 23. Can be used as a modem or general purpose input. When this modem input is low it indicates that the data carrier has been detected by the modem or data set. The $\overline{\text{DCD}}$ signal is a modem control function input whose complement value can be tested by the CPU by reading bit 5 (DCD) of the modem status register. Bit 1 (ΔDCD) of the modem status register indicates whether the $\overline{\text{DCD}}$ input has changed state since the previous reading of the modem status register. $\overline{\text{DCD}}$ can also be programmed to become an auto enable for the receiver. Note: Whenever the DCD bit of the modem

Functional Pin Description (Continued)

status register changes state, an interrupt is generated if the ΔDCD mask and the DSCHG mask bits are set.

Clear to Send ($\overline{\text{CTS}}$): active low, Pin 26. Can be used as a modem or a general purpose input. The $\overline{\text{CTS}}$ inputs complement can be tested by the CPU by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the modem status register. $\overline{\text{CTS}}$ can be programmed to automatically enable the transmitter. Note: Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the ΔCTS mask and the DSCHG mask bits are set.

Data Set Ready ($\overline{\text{DSR}}$): active low, Pin 27. Can be used as a modem or a general purpose input. When this modem input is low it indicates that the modem or data set is ready to establish the communication link and transfer data with the NSC858. The $\overline{\text{DSR}}$ is a modem-control function input whose complement value can be tested by the CPU by reading bit 6 (DSR) of the modem status register. Bit 2 (ΔDSR) of the modem status register indicates whether the ($\overline{\text{DSR}}$) input has changed state since the previous reading of the modem status register. Note: Whenever the DSR bit of the modem status register changes state, an interrupt is generated if ΔDSR mask and the DSCHG mask bits are set.

Power (V_{CC}): Pin 28. +5V supply.

Ground (GND): Pin 14. Ground (0V) supply.

OUTPUT SIGNALS

Transmit Data (TxD): Pin 19. Composite serial data output to the communication link (peripheral, modem or data set) least significant bit first. The TxD signal is set to the marking (logic 1) state upon a master reset. In hardware or software power down this pin will always be a one.

Receiver-Transmitter Interrupt ($\overline{\text{RTI}}$): active low, Pin 22. Goes low when any R-T status register bit and its corresponding mask bit are set. This bit can change states during either hardware or software power down due to a change in modem status information.

Request to Send ($\overline{\text{RTS}}$): active low, Pin 24. Can be used as a modem or a general purpose output. When this modem output is low it informs the modem or data set that the NSC858 is ready to transmit data. The $\overline{\text{RTS}}$ output or general purpose output signal can be set to an active low by programming bit 6 of the command register with a 1. The $\overline{\text{RTS}}$ signal is set high upon a master reset operation. During remote loopback $\overline{\text{RTS}}$ signal reflects the complement of bit 6 of the command register. During local loopback the $\overline{\text{RTS}}$ signal is forced to its inactive state (high). $\overline{\text{RTS}}$ cannot change states during hardware power down; it can during software power down.

Data Terminal Ready ($\overline{\text{DTR}}$): active low, Pin 25. Can be used as a modem or general purpose output. When this modem output is low it informs the modem or data set that the NSC858 is ready to communicate. The $\overline{\text{DTR}}$ output or the general purpose output signal can be set to an active low by programming bit 7 of the command register with a 1. The $\overline{\text{DTR}}$ signal is set high upon a master reset operation. During remote loopback $\overline{\text{DTR}}$ signal reflects the complement of bit 7 of the command register. During local loopback the $\overline{\text{DTR}}$ signal is forced to its inactive state (high). $\overline{\text{DTR}}$ signal cannot change state during hardware power down; it can during software power down.

INPUT/OUTPUT SIGNALS

Address/Data Bus (AD0–AD7): Pins 6–13. The multiplexed bidirectional address/data bus, AD0–AD7 pins, are in the high impedance state when the NSC858 is not selected or whenever it is in hardware power down. AD0–AD3 are latched on the trailing edge of ALE, providing the four address inputs. The rising edge of the $\overline{\text{WR}}$ input enables 8 bits to be written in, through AD0–AD7, to the addressed register. $\overline{\text{RD}}$ input enables 8 bits to be read from a register out through AD0–AD7.

Transmitter Clock/Baud Rate Generator Output ($\overline{\text{TxC}}$/BRGOUT): Pin 18. If the transmitter is programmed for an external clock, $\overline{\text{TxC}}$ is an input. If the transmitter is programmed for an internal clock, then the Baud Rate Generator is used for the transmitter, and it is output at $\overline{\text{TxC}}$/BRGOUT. In either case, $\overline{\text{TxC}}$/BRGOUT signal is running at 1X, 16X, 32X, 64X the data rate, as selected by the clock factor. If this pin is used as an output it will be set to a zero (0) in both hardware and software power down.

Receiver Clock/Baud Rate Generator Output ($\overline{\text{RxC}}$/BRGOUT): Pin 20. If the receiver is programmed for an external clock, RxC is an input. If the receiver is programmed for an internal clock, the Baud Rate Generator is used for the receiver, and it is output at $\overline{\text{TxC}}$/BRGOUT. In either case, $\overline{\text{TxC}}$/BRGOUT signal is running at 1X, 16X, 32X, 64X, the data rate, as selected by the clock factor. If this pin is programmed as an output it will be set to one (1) in both hardware and software power down.

Crystal (XIN, XOUT): Pins 15, 16. These two pins connect the main timing reference. A crystal network can be connected across these two pins, or a square wave can be driven into XIN with XOUT left floating. In hardware and software power down XOUT is set to a 1.

TABLE 1. Register Address Designations

Address				Register	Read/Write
A_3	A_2	A_1	A_0		
0	0	0	0	Rx Holding	R
0	0	0	0	Tx Holding	W
0	0	0	1	Receiver Mode	R/W
0	0	1	0	Transmitter Mode	R/W
0	0	1	1	Global Mode	R/W
0	1	0	0	Command	R/W
0	1	0	1	Baud Rate Generator Divisor Latch (Lower)	R/W
0	1	1	0	Baud Rate Generator Divisor Latch (Upper)	R/W
0	1	1	1	R-T Status Mask	R/W
1	0	0	0	R-T Status	R
1	0	0	1	Modem Status Mask	R/W
1	0	1	0	Modem Status	R
1	0	1	1	Power Down	R/W
1	1	0	0	Master Reset	W

Note: Offset address OD, OE, OF are unused.

Registers

The system programmer may access control of any of the NSC858 registers summarized in Table 1 via the CPU. These 8-bit registers are used to control NSC858 operation and to transmit and receive data.

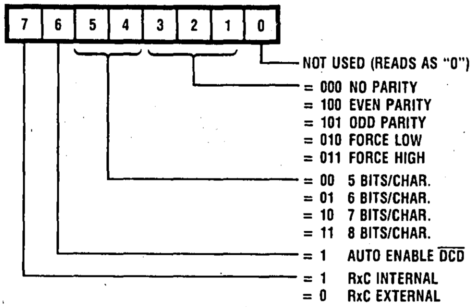
RECEIVER AND TRANSMITTER HOLDING REGISTER

A read to offset location 00 will access the Receiver holding register; a write will access the Transmitter holding register.

RECEIVER MODE REGISTER

The system programmer specifies the data format of the receiver (which may differ from the transmitter) by programming the Receiver mode register at offset location "01." This read/write register programs the parity, bits/character, auto enable option, and clock source. When bit 6 of this register is set high the receiver will be enabled any time the $\overline{DCD}$ signal input is low (provided CR0 = 1). When bit 7 is set to a "1" the receiver clock source is the internal baud rate generator, and $\overline{RxC}$ is then an output. After reset this register is set to "00."

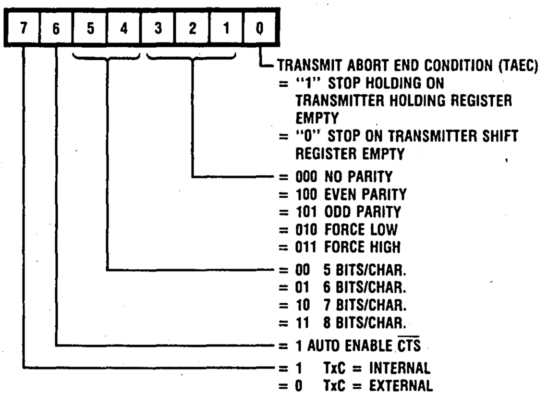
TABLE 2. Receiver Mode Register (Address "01") (Bits RM0–7)



TRANSMITTER MODE REGISTER

The system programmer specifies the data format of the transmitter (which may differ from the receiver) by programming the transmitter mode register at offset location "02."

TABLE 3. Transmit Mode Register (Address "02") (Bits TM0–7)

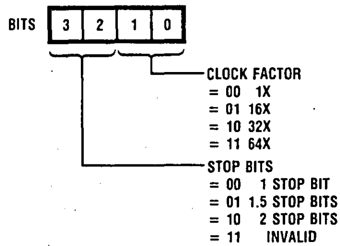


The transmitter mode register is similar in operation to the receiver mode register except for the addition of the Transmit Abort End Condition (TAEC). If this bit is set to a one when a request to disable the transmitter or send a break is pending then the data in the shift register and holding register will be transmitted prior to such action occurring. If TAEC equals 0 then the action will take place after the shift register has been emptied. When bit 6 of this register is set high the transmitter will be enabled any time the $\overline{CTS}$ signal is low (provided CR1 = 1). When bit 7 is set to a "1" the transmitter clock source is the internal baud rate generator, and $\overline{TxC}$ is then an output. After reset this register is set to "00."

GLOBAL MODE REGISTER

This register is used to program the number of stop bits and the clock factor for both the receiver and transmitter. Only the lower four bits of this register are used, the upper four can be programmed as don't cares and they will be read back as zeros. Programming the number of stop bits is for the transmitter only; the receiver always checks for one stop bit. If a 1X clock factor with 1.5 stop bits is selected for the transmitter the number of stop bits will default to 1. After reset this register is set to "00."

TABLE 4. Global Mode Register (Address "03") (Bits GM0–3)

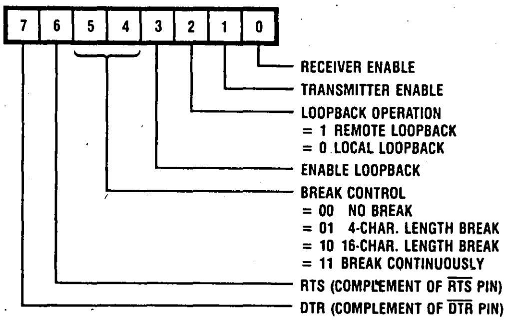


Bits 4–7 are don't care, read as 0s.

COMMAND REGISTER

The Command register is an eight bit read/write register which is accessed at offset location "04." After reset the command register equals "00."

TABLE 5. Command Register (Address "04") (Bits CR0–7)



Registers (Continued)

Bit 0: Receiver Enable, when set to a one the receiver is enabled. If auto enable for the receiver has been programmed then in addition to CR0 = 1, the $\overline{\text{DCD}}$ input must be low to enable receiver.

Bit 1: Transmitter Enable, when set to a one the transmitter is enabled. If auto enable for the transmitter is programmed then in addition to CR1 = 1, the $\overline{\text{CTS}}$ input must be low to enable transmitter.

Bit 2: A zero selects local loopback and a one selects remote loopback.

Bit 3: A one enables either of the diagnostic modes selected in bit 2 of the command register.

Bits 4 and 5: Bits 4 and 5 of the command register are used to program the length of a transmitted break condition. A continuous break must be terminated by the CPU, but the 4 and 16 character length breaks are self clearing. (After the last break character has been sent, bits 4 and 5 will automatically be reset to 0.) Break commands affect the status of bit 6 (TBK) of the R-T Status register (see R-T Status register). Break control bits are cleared by software or hardware power down.

Bits 6 and 7: These two bits control the status of the output pins $\overline{\text{RTS}}$ (pin 24) and $\overline{\text{DTR}}$ (pin 25) respectively. They may be used as modem control functions or be used as general purpose outputs. The output pins will always reflect the complement of the register bits.

R-T STATUS REGISTER

This 8-bit register contains status information of the NSC858 and therefore is a read only register at offset location "08." Each bit in this register can generate an interrupt ($\overline{\text{RTI}}$). If any bit goes active high and its associated mask bit is set then the $\overline{\text{RTI}}$ will go low. $\overline{\text{RTI}}$ will be cleared when all unmasked R-T Status bits are cleared. Bits 0 and 1, receiver ready and transmitter empty are cleared by reading the receiver holding register or writing the transmitter holding register respectively. Bits 2 through 5, transmit underrun, receiver overrun, framing error, parity error are cleared by reading the R-T Status register. Bit two, transmitter underrun will occur when both the transmit holding register and the transmit shift register are empty.

Bit three, overrun error, will occur when the CPU does not read a character before the next one becomes available. Bit four, framing error, occurs when a valid stop bit is not detected. Bit 5 is set when a parity error is detected. Bits three, four and five are affected by receiver only.

Bit 6, Transmit Break (TBK) is set at the beginning of each break character during a break continuously command, or at the beginning of the final break character in a 4 or 16 character programmed break length. It is cleared by reading the R-T Status register. Bit 7, Data Set Change (DSCHG) will be set whenever any of the bits 0–3 of the Modem Status register and their associated mask bit are set. Data Set Change bit is cleared by reading the Modem Status register or is masked off by writing "0" to all modem mask register bits. After reset the R-T Status register equals '02', i.e. all bits except TxBE are reset to zero.

TABLE 6. R-T Status Register (Address "08") (Bits SR0–7)

Bit	
0	RxRDY (RECEIVER DATA READY) 1 = FULL 0 = EMPTY
1	TxBE (TRANSMITTER BUFFER EMPTY) 1 = EMPTY 0 = FULL
2	TxU (TRANSMITTER UNDERRUN 1 = ERROR 0 = NO ERROR
3	OE (RECEIVER OVERRUN ERROR) 1 = ERROR 0 = NO ERROR
4	FE (RECEIVER FRAMING ERROR) 1 = ERROR 0 = NO ERROR
5	PE (RECEIVER PARITY ERROR) 1 = ERROR 0 = NO ERROR
6	TBK (TRANSMITTER BREAK) 1 = BREAK 0 = NO BREAK
7	DSCHG (DATA SET CHANGE) 1 = CHANGE 0 = NO CHANGE

R-T STATUS MASK REGISTER (SM0–7)

This register is used in conjunction with the R-T Status register to enable or disable conditional interrupts. A one in any bit unmasks its associated bit in the R-T Status register, and allows it to generate an interrupt. The mask affects only the interrupt and not the R-T Status bits. This eight bit register is both read and writable at offset location "07." After reset it is set to "0" which disables all interrupts. Each bit in the R-T Status mask register is associated with that bit in the R-T Status register (e.g., SM0 is SR0's mask).

MODEM STATUS

This eight bit read only register which is addressed at offset location "0A" contains modem or general purpose input and receiver break information.

TABLE 7. Modem Status Register (Address "0A") (Bits MS0–7)

Bit	
0	ΔCTS
1	ΔDCD
2	ΔDSR
3	ΔBRK
4	CTS
5	DCD
6	DSR
7	BRK

Registers (Continued)

Each of the four status signals in this register also have an associated delta bit in this register. Each delta bit (bits MS0–3) will be set when its corresponding bit changes states. These four delta bits are cleared when the Modem Status register is read. If any of these four delta bits and associated mask bits are set they will force DSCHG (bit 7) of the R-T Status register high. Bits 4–6, CTS, DCD, DSR can be used as modem signals or general purpose inputs. In either case the value in the register represents the complements of the input pins $\overline{CTS}$ (pin 26), $\overline{DCD}$ (pin 23), and $\overline{DSR}$ (pin 27). Bit 7 (BRK) when set to a one indicates that the receiver has detected a break condition. It is cleared when break terminates. After reset ΔCTS, ΔDCD, ΔDSR, ΔBRK and BRK are cleared.

MODEM MASK REGISTER (MM0–3)

This 4-bit read/write register, which is addressed at offset location "09," contains mask bits for the four delta bits of the Modem Status register (MS0–3). A one ("1") in any of these bits and a one in the associated delta bit of the Modem Status register will set the DSCHG bit of the R-T Status register. Modem Mask bit 0 is associated with Modem Status bit 0, etc. The four (4) most significant bits of this register will read as zeros. After reset the register equals '00'.

POWER DOWN REGISTER (PD0)

This one bit register can both be read and written at offset location "0B." When bit zero is set to a one the NSC858 will be put into software power down. This disables the receiver and transmitter clocks, shuts off the baud rate generator and crystal oscillator, and clears the RxE, TxE, and break control bits in the command register. Registers on chip can still be accessed by the CPU during software power down. Bits 1 through 7 will always read as 0.

MASTER RESET REGISTER

This write only register is addressed at offset location "0C." When writing to this register the data can be any value (don't cares). Resetting the NSC858 by way of the reset register is functionally identical to resetting it by the MR pin.

BAUD RATE GENERATOR DIVISOR LATCH

These two 8-bit read/write registers which are accessed at offset locations "05" (lower) and "06" (upper) are used to program the baud rate divisor. These registers are not affected by reset function and are powered up in a random state.

Functional Description

PROGRAMMABLE BAUD GENERATOR

The NSC858 contains a programmable Baud Generator that is capable of taking any clock input (DC to 4.1 MHz) and dividing it by any divisor from 1 to (2^{16} – 1). The output frequency of the Baud Generator (available at $\overline{TxC}$/BRGOUT or $\overline{RxC}$/BRGOUT, if internal $\overline{TxC}$ or $\overline{RxC}$ is selected) is equal to the clock factor (1X, 16X, 32X, 64X) times the baud rate. The divisor number is determined by the following equation:

$$\text{divisor \#} = \frac{\text{Frequency Input } (f_{BRC})}{[\text{Baud Rate} \times \text{Clock Factor } (1, 16, 32, 64)]}$$

Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 8 and 9 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

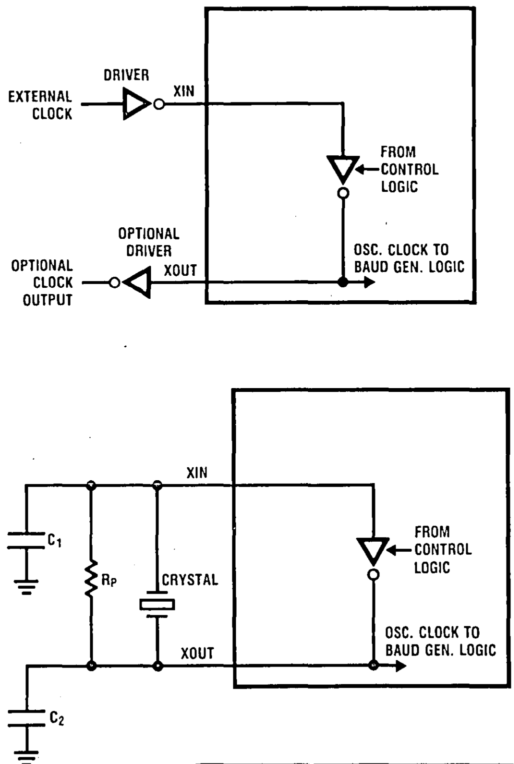
TABLE 8. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 × Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Table 9. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 × Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.317
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

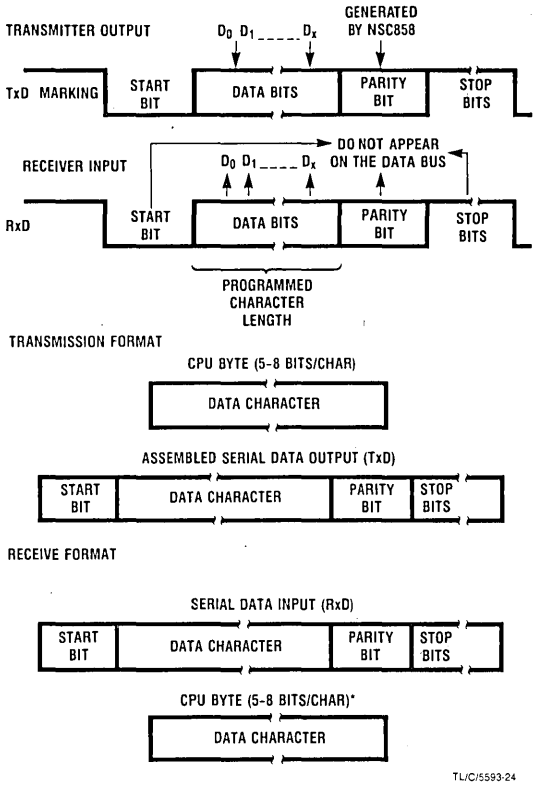
Typical Clock Circuits



CRYSTAL	R_P	C_1	C_2
3.1 MHz	1 MΩ	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	10-30 pF	40-60 pF

TL/C/5593-23

FIGURE 1. Typical Crystal Oscillator Network



TL/C/5593-24

Note: If character length is defined as 5, 6 or 7 bits, the unused bits are set to "0."

FIGURE 2.

RECEIVER AND TRANSMITTER OPERATION

The NSC858 transmits and receives data in an asynchronous communications mode. The CPU must set up the appropriate mode of operation, number of bits per character, parity, number of stop bits, etc. Separate mode registers exist for the independent specification of receiver and transmitter operation. These independent specifications include parity, character length, and internal or external clock source. Only the Global Mode Register, which controls the number of stop bits and the clock factor, exercises common control over the receiver and transmitter (receiver looks for only one stop bit).

TRANSMITTER OPERATION

The Transmitter Holding register is loaded by the CPU. To enable the transmitter, TxE must be set in the Command register. $\overline{\text{CTS}}$ must be low if the auto enable CTS bit is set in the Tx Mode register. The Transmitter Holding register is then parallel loaded into the Transmitter Shift register, and the start bit, parity bit and the specified number of stop bits are inserted. This serialized data is available at the TxD output pad, and changes on the rising edge of $\overline{\text{TxC}}$. The TxD output remains in a mark ("1") condition when no data is being transmitted, with the exception of sending a break ("0").

A break condition is initiated by writing either a continuous or specified length break request to the Command Register. A finite break specification of either 4 or 16 character lengths can be extended by re-writing the break command before the specified break length is completed. Each break character is transmitted as a start bit, logical zero data, logical zero parity (if specified) and logical zero stop bit(s). The number of data and stop bits, plus the presence of a parity bit are determined by the Transmitter and Global Mode registers. Thus, the total number of (all zero) bits in a break character is the same as that for data. The break is terminated by writing "00" to the Break Control bits in the Command Register. The Set Break bits in the Command register are always reset to "00" after the termination of the specified break transmission or if the transmitter is disabled during a break transmission. The TxD output will always return to a mark condition for at least one bit time before transmitting a character after a break condition. Data in the Transmitter Holding register, whether loaded before (on TAEC = 0) or during the break will be transmitted after the break is terminated.

Typical Clock Circuits (Continued)

RECEIVER OPERATION

The NSC858 receives serial data on the RxD input. To enable the receiver, $\overline{\text{DCD}}$ must be low if the $\overline{\text{DCD}}$ Auto Enable bit in the Receiver Mode register is set ("1"). RxE must be set in the Command register. RxD is sampled on the falling edge of RxC. If a high ("1") to low ("0") transition of RxD is detected, RxD is sampled again, for all except the 1X clock factor, at ½ of a bit time later. If RxD is still low, then a valid start bit has been received and character assembly proceeds. If RxD has returned high, then a valid start bit has not been received, and the search for a valid start bit continues. When a character has been assembled in the Receiver Shift Register and transferred to the Receiver Holding Register, the RxRDY bit (and any error bits that may have occurred) in the R-T Status register will be set and $\overline{\text{RTI}}$ will go low (if the proper mask bits are set). After the CPU reads the Receiver Holding register, the RxRDY will go low and the $\overline{\text{RTI}}$ will go inactive ("1").

The receiver will detect a break condition on RxD if an all zero character with zero parity bit (if parity is specified) and a zero stop bit is received. For the break condition to terminate, RxD must be high for one half a bit time. If a break condition is detected, bits 3 and 7 in the Modem Status register (ΔBRK and BRK respectively) will be set. Bit 3 (ΔBRK) will then cause bit 7 (DSCHG) in the R-T Status register to be set which in turn forces $\overline{\text{RTI}}$ to an asserted state ("0"). These interrupts will occur only if the appropriate mask bits are set for the registers in question.

PROGRAMMING THE NSC858

There are two distinct steps in programming the 858. During initialization, the modes, clocks, masks and commands are set up. Then, in operation, Modem I/O takes place, status is monitored, the receiver and transmitter are run as needed.

To initialize the 858, first pulse the MR line or write to the Master Reset register. Then, write to the following registers in any order, except for enabling the Rx and Tx, which must be at the end of the set up procedure. The Global, Receiver and Transmitter Mode registers determine the modes for the Rx and Tx. These latter two registers often will have the same data byte written to them, but are kept independent for flexibility. If the mode registers indicate that the receiver and/or the transmitter use an internal clock, then data (determined by the crystal frequency and desired bit time and clock factor) should be written to the upper and lower Baud Rate Generator Divisor Latches. The Modem Status Mask register enables Data Set change in R-T Status. If interrupts are required, the R-T Status Mask register allows $\overline{\text{RTI}}$ to occur. Write to the Command register to enable the receiver and/or transmitter only when all else is set up.

In operation, the 858 can transmit, receive and handle I/O simultaneously. Modem outputs are written to at the Command register, while the inputs are read at the Modem Status register. Data flow and errors are read at the R-T Status register. When serial data has been shifted in and assembled, the receiver is ready, and the word can be read at the Rx Holding register. When the transmitter buffer is empty, the Tx Holding register can be written to, and the word will be shifted out as serial asynchronous data.

Once the 858 is running, several options may be exercised. Masks can be changed at any time. The Rx and Tx are disabled or enabled, as needed, by writing to the Command register, or toggling the auto enable modem inputs (if used). Both the Rx and Tx should be disabled before either altering any mode or engaging a loopback diagnostic, and they can be re-enabled then or at a later time. Power down is allowed at any time except during loopback, although data may be lost if PD occurs in the middle of a word.

Thus, software for the NSC858 is of two types. The initialization routine is performed once. The operation routines, usually incorporating polling or interrupts, are then run continuously or on demand, depending upon the system or application.

DIAGNOSTIC CAPABILITIES

The NSC858 offers both remote and local loopback diagnostic capabilities. These features are selected through the Command register.

Local Loopback Mode (see *Figure 3*)

1. The transmitter output is internally connected to the receiver input.
2. $\overline{\text{DTR}}$ is connected to $\overline{\text{DCD}}$, and $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$. Both connections are made internally.
3. $\overline{\text{TxC}}$ is connected internally to $\overline{\text{RxC}}$.
4. The DSR is internally held low (inactive).
5. The TxD, $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ outputs are held high.
6. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and $\overline{\text{RxD}}$ inputs are ignored.
7. Except as noted, all other Status, Mode and Command Register bits and interrupts retain their functions and settings.

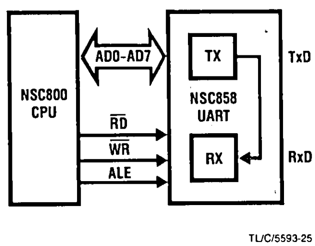
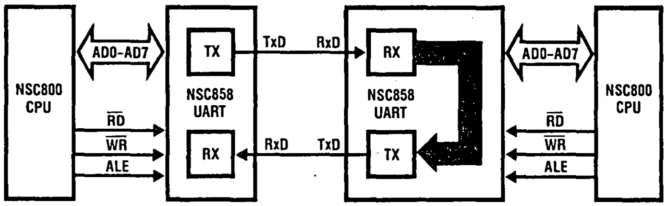


FIGURE 3. Local Loopback

Typical Clock Circuits (Continued)

Remote Loopback Mode (see *Figure 4)*

1. The contents of the Receiver Holding Register, when RxRDY = 1 indicates it is full, are transferred to the Transmitter Holding register, when TxBE = 1 indicates it is empty. After this action, both RxRDY and TxBE are cleared.
2. $\overline{RxC}$ is connected internally to $\overline{TxC}$.
3. Setting the Remote Loopback Mode places all receiver and transmitter flags under control of the remote loopback sequencer. RxRDY and TxBE can be monitored to follow automatic remote loopback data flow, while OE and TxU can indicate system problems.
4. The CPU can read the Receiver Holding register if desired, but this is not necessary. The CPU cannot load the Transmitter Holding Register.
5. Modem Status, all Mode and Command register bits retain their functions and interrupts are generated.



TL/C/5593-26

FIGURE 4. Remote Loopback

Ordering Information

NSC858XX

- **/A+ = A+ Reliability Screening**
- **D = Ceramic Package**
- **J = Cerdip Package (Availability to be announced)**
- **N = Plastic Package**
- **E = Ceramic Leadless Chip Carrier (LCC)**
- **V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)**

Reliability Information

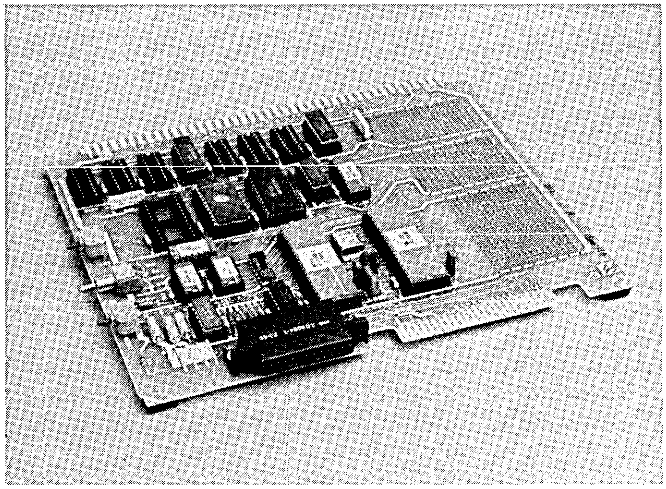
Gate Count 4280
Transistor Count 8450

National Semiconductor

NSC888

NSC800 Evaluation Board

microCMOS



Features

- NSC800™ 8-Bit microCMOS CPU
- Executes Z80™ Instruction Set
- 20 Programmable Parallel I/O Lines
- Two 16-Bit Programmable Counters/Timers
- Powerful 2K x 8 Monitor Program
- Five Levels of Vectored Prioritized Interrupts
- RS232 Interface
- 1K x 8 microCMOS RAM with Sockets for up to 4K x 8 RAM
- Socket for additional 2K x 8, 2716 Compatible Memory Component
- Wire Wrap Area
- Edge Connectors for System Expansion
- Single-Step Operation Mode
- Fully Assembled and Tested

Product Overview

The NSC888 is a self-contained microprocessor board which enables the user to quickly evaluate the performance and features of the NSC800 product family. This fully assembled, tested board requires only the addition of a ±5V supply and an RS232 interface cable to the users terminal to begin NSC800 evaluation.

A powerful system monitor is provided on the board which controls serial communications via the RS232 port. The monitor also includes command functions to load, execute and debug NSC800 programs.

The board includes an NSC800 CPU plus RAM, EPROM, I/O, Timers and interface components yet draws only 30mA from the +5V supply and 3mA from the -5V supply.

Although designed primarily as an assessment vehicle, the NSC888 can be readily programmed and adapted to a variety of uses. Wire wrap area is provided on-board for the user to build up additional circuitry or interfaces, thus tailoring this high-performance, low-power microprocessor board to meet individual needs.

Functional Description

Figure 1 and *Figure 2* provide information on the organization of the NSC888 board. Please refer to these figures for the following discussion.

Central Processor

The powerful NSC800 is the central processor for the NSC888. It provides bus control, clock generation and extensive interrupt capability. Featuring a multiplicity of programmable registers and sophisticated addressing modes, the NSC800 executes the Z80 instruction set.

Memory

- 128 bytes of RAM are provided by the NSC810 RAM-I/O-Timer and are used by the monitor program for the system stack.
- 1024 bytes of RAM are provided by two 1K x 4 NMC6514's. Sockets are provided for six additional NMC6514's, for a total of 4K bytes of RAM.
- A 2K byte EPROM system monitor is provided on-board which includes facilities to load, execute and debug a users program.
- An additional EPROM socket is also on-board which accepts a 2K byte 2716 compatible memory component.

Input/Output

- **Parallel I/O**
  The NSC888 provides 20 programmable parallel I/O lines implemented using the I/O ports of the NSC810 RAM-I/O-Timer. The port bits may be individually defined as input or output, and can also be written to or read from in bytes. The I/O lines are conveniently brought to a 50 contact edge connector for user interface.
- **Serial I/O**
  An RS232 connector and accompanying support circuitry are provided on-board. Two I/O lines from the NSC810 RAM-I/O-Timer are used for the serial communications function, which is controlled exclusively by software. The baud rate is determined upon system initialization by the character bit rate from the users terminal. The maximum baud rate is 2400 baud.

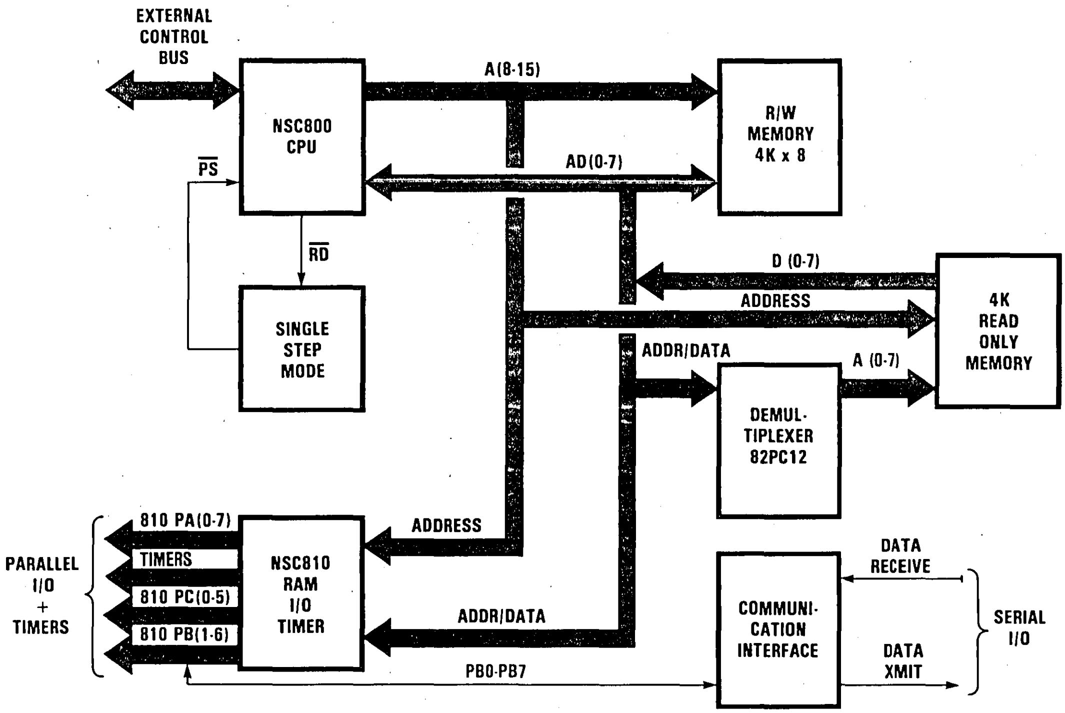


FIGURE 1. NSC888 Functional Block Diagram

SR-O/C/1356-13

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Timers

The NSC888 provides two fully programmable binary 16-bit counters/timers utilizing the NSC810 RAM-I/O-Timer. These signals are also brought to the parallel I/O connector. Each timer may operate in any of six different modes:

- Event Counter
- Accumulative Timer
- Restartable Timer
- One Shot
- Square Wave
- Pulse Generator

Connectors

- **Parallel I/O**
  The parallel I/O lines and timer lines from the NSC810 RAM-I/O-Timer, plus interrupt lines from the CPU are brought to this 50 contact edge connector.

- **System Bus**
  All NSC800 CPU lines except XIN are brought to this 86 contact edge connector. In addition, the -5V line is also brought to the system bus connector.

- **RS232**
  This connector is provided for system interface to the users terminal.

Interrupts

The NSC888 utilizes the powerful interrupt processing capability of the NSC800 CPU. Interrupts are routed via a jumper matrix to the five interrupt inputs of the NSC800. Each input, which may be from the NSC810 I/O ports, NSC810 timers or off board via the system bus connector, generates a unique memory address (see *Table 1*). All interrupts with the exception of NMI can be masked via software. Interrupt lines are also brought to the parallel I/O connector.

Table 1.

Interrupt Input	Memory Address	Type	Priority
NMI	0066H	Non-maskable	Highest
RSTA	003CH	Maskable	
RSTB	0034H	Maskable	
RSTC	002CH	Maskable	
INTR	0038H*	Maskable	Lowest

*mode 1

NSC888 FIRMWARE

The NSC888 system monitor is provided by a preprogrammed EPROM. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. It permits the insertion of break points to facilitate debugging. Programs can be executed starting at any location. The commands supported by the NSC888 system monitor are as follows:

- B - Select a new baud rate
- D - Display memory
- F - Fill memory between ranges
- G - Execute program with break points
- H - Hexadecimal math routine
- J - Non-destructive memory test
- K - Store 16-bit value in memory
- M - Move a block of data
- P - Put ASCII characters in memory
- Q - Query I/O ports
- S - Substitute and/or examine memory
- T - Type memory contents in ASCII
- V - Verify two blocks of data
- X - Examine or modify CPU registers
- Y - Memory search for string

These commands are fully explained in the NSC888 Hardware/Software Users Manual.

Single Step/Power Save

The NSC888 provides a unique single-step mode, utilizing the Power Save input of the NSC800 CPU. This input, when activated, reduces CPU power consumption from 50mW to only 25mW. It also allows the user to single-step through a program, checking and modifying code. This function is controlled via a switch on the board.

Specifications

Microprocessor

CPU-	NSC800
Data Word-	8 bits
Instruction Word-	8, 16, 24, 32 bits
Cycle Time-	2.00μs (minimum instruction time)
System Clock-	2.00MHz
Registers-	14 general purpose (8-bit) 2 index registers (16-bit) 1 stack pointer (16-bit) 1 program counter (16-bit)
Number of Instructions-	158
Address Capability-	64K bytes

Memory

RAM-	1152 bytes on-board plus sockets for an additional 3K bytes
ROM/EPROM-	Sockets for 4K bytes on-board
Access Time-	625ns for opcode fetch 875ns for memory read

Connectors

System Bus-	86-pin double-sided card cage edge connector on 0.156 inch centers

Parallel I/O-	50-pin double-sided edge connector on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O-	Standard RS232 connector
Power	+5V 30mA (27C16 EPROM monitor) or 90mA (2716 EPROM monitor) -5V 3mA
Physical	
Height-	6.75 (17.15cm)
Width-	7.85 (19.94cm)

Order Information

NSC888-	Includes CPU, 1152 bytes of RAM, sockets for additional 3K bytes of RAM, 2K byte monitor with additional socket for 2K byte ROM/EPROM, 20 I/O lines, RS232 interface, wire wrap area.
Documentation-	The NSC888 Hardware/ Software Users Manual and NSC800 Microprocessor Family Handbook are shipped with the NSC888 Evaluation Board

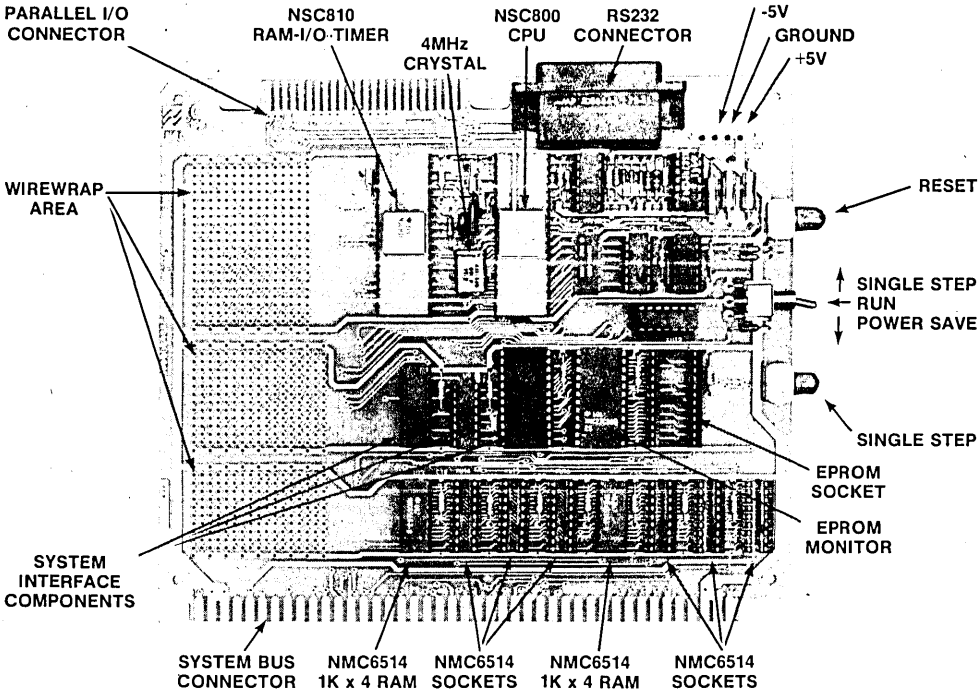

FIGURE 2. NSC888 Evaluation Board

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Section 13

Development Systems Products

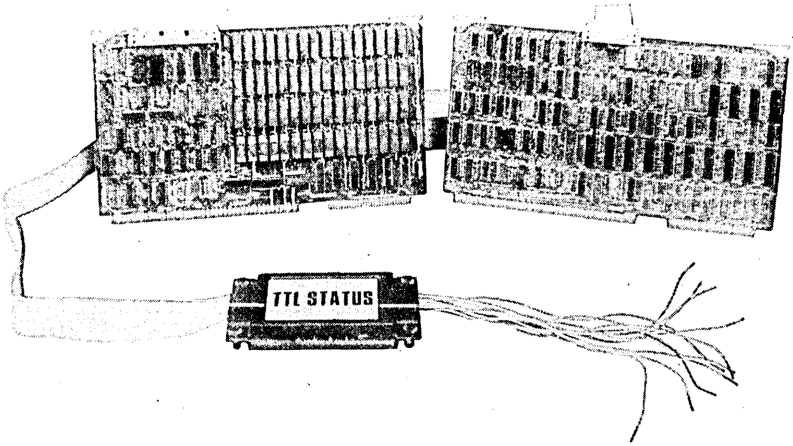
13

Introduction

This section of the databook describes the various development tools available to design and develop microprocessor-based products. Support tools include software packages for applications software development—real-time emulators for fast and efficient hardware and software debugging peripherals packages (such as PROM programmers and printers) and, of course, powerful host systems to bring all of these support packages together.

National offers the STARPLEX II™ and the SYS-16™ Development Systems. STARPLEX II allows the designer to develop 8-bit microprocessor-based products, while the SYS-16 allows the designer to develop NS16000™-based products. Appropriate packages for software development work are available for each of these host systems. Software packages for the STARPLEX II include 8-bit cross-assemblers and compilers (such as the COPS™ cross-assembler for COP400 family microcontrollers), and PASCAL compilers for 8085 and NSC800™ microprocessors. Software for the SYS-16 includes PASCAL and C to support the NS16000 family. To debug the software in the hardware prototype, powerful real-time in-system emulators (ISEs) are available for the appropriate microprocessors.

Integral In-System Emulator (ISE™) Package



- **Real-time emulation of 8-Bit microprocessors**
  - Full Support for 8085 Series, NSC800™ and Z80 Microprocessors
- **Combined with an emulator board, will operate in any STARPLEX™/ STARPLEX II™ Development System**
- **An integral emulation system**
  - Hardware
    - Processor independent
    - 32K byte mapped memory
    - Two 32-bit breakpoint registers, each bit programmable
    - 256 × 40-bit trace memory
    - Memory mapping in 1K byte increments
    - 8-bit user status cable for custom breakpoint and trace operations
    - Real-time counter in microseconds up to 16 seconds.
  - Software
    - Host system resident command driver
    - Host system resident mnemonic assembler and disassembler
    - Coast after breakpoint provided with variable length and user-defined qualifications
- **Easy to use**
  - In-File for Automatic Test
  - Consistent Commands
  - Symbolic Debugger
  - Full Access to STARPLEX/ STARPLEX II Development Systems Facilities (e.g., access to STARPLEX/ STARPLEX II Editor and other utility programs)
- **Optional emulator packages to handle conversion from one target processor to another**

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Product Overview

The Integral ISE consists of two logic boards in standard STARPLEX/STARPLEX II configuration, one bus connector and a cable. In addition to this are manuals and user software. The two logic boards provide all the necessary logic for breakpoints, tracing, and real-time memory mapping. Microprocessor emulation is isolated on a required single optional target board containing all the logic needed to emulate the particular microprocessor. Together with any specified target processor, which is not part of the Integral ISE, the three boards can be installed in any STARPLEX/STARPLEX II Development System. When installed directly in a STARPLEX/STARPLEX II Development System, the Integral ISE supports only single processor emulation.

(From this point on "STARPLEX" will signify "STARPLEX/STARPLEX II".)

There are three very important advantages to this approach to system emulation:

Economy is the prime advantage. The customer needs to purchase exactly what his application requires. For simple single processor applications, the user can install the Integral ISE directly into any STARPLEX Development System without being required to purchase an entire emulation chassis. Since the Trace and Mapped Memory boards are standard logic modules, the customer will require only one set of these boards in most applications, whereas he might have several different types of target modules. In this manner, the user would be allowed to change his target module set-ups for one processor to another quickly and conveniently without changes of any kind to the Trace and Mapped Memory boards.

Convenience is an obvious advantage. The user need only master one software package—a single host software driver program—which supports all the features of the Integral ISE and its entire set of compatible target boards. Specific characteristics of the emulated microprocessor which must be known by the driver program (e.g., register complement, word size, status bits, etc.) are recorded on a "target specific" diskette which is supplied with each different target board. The driver program upon initialization reads the target board status which identifies the target processor device type. This information together with the data contained on the "target specific" diskette allows the software driver to display data to the user in a syntax consistent with each processor type.

The Integral ISE software package is totally integrated into a STARPLEX Development System. All of the ease-of-use concepts that set the STARPLEX above other development systems are designed into the Integral ISE system.

The software is invoked with a single keystroke on a STARPLEX keyboard, as are all other STARPLEX system resources. A fill-in-the-blank menu appears on the CRT and prompts the user to select the microprocessor to be emulated. During the emulation process a portion of the CRT screen is reserved to inform the user of emulation status. This status information includes the type of microprocessor(s) selected for emulation, the state of the emulated microprocessor(s), breakpoint condition mask, and whether or not breakpoints are enabled.

Should the user wish to review the full range of the Integral ISE commands available he can call for "HELP"; the "HELP" key on a STARPLEX keyboard allows the user to display information describing the Integral ISE software functions.

Performance is the final advantage. Unlike other in-system emulators which are installed directly into a development system, National's Integral ISE does not have to compete with the system bus in order to attain real-time emulation, either mapped or unmapped. Even though the Trace and Mapped Memory boards are physically within the development system, they do not interface directly with the system bus. They interface only with the Target Board through a specialized high-speed emulation bus connector. Only the Target Board has the capability of interfacing to the system bus. The Mapped Memory board is dedicated to Integral ISE and does not occupy any STARPLEX Development System address space.

Functional Description

Support Various Microprocessors

The Integral ISE is a flexible solution for users who wish to prototype systems involving one or more types of microprocessors. By changing a target CPU board, Integral ISE can be used to emulate various different microprocessors such as the 8085 NSC800 and Z80 microprocessors.

Powerful Debugging Capability

National Semiconductor's Integral ISE provides all the usual features of a powerful in-system emulator, plus many more that make it the most powerful unit available today. The usual features include: program loading from the host mass storage unit to the Integral ISE program memory; saving programs in the Integral ISE on the host system's mass storage med ium; memory examination and modification; register examination and modification. Some of the additional and more powerful characteristics include:

- Real-Time Emulation of the Target Microprocessor

  Real-time emulation means that the target microprocessor is emulated in an applications system with the same hardware and software timing characteristics that the microprocessor chip will exhibit when it is plugged into the application system. Real-time emulation has been designed into the Integral ISE. Some design characteristics contributing to real-time emulation are:

  — Separation of the Host Development System Function. Separation of Integral ISE from the host development is a major contribution to real-time emulation. Integral ISE uses a separate internal bus from the host system, thus eliminating bus access conflicts between the emulation function and the host control functions. Its internal structure is optimized for microprocessor emulation, and is not compromised by some predefined architecture.

— System Clock Selection. In the early stages of the applications system checkout, where minor timing variations are more easily tolerated, the applications system designer may choose to run the emulator using the Integral ISE system clock. In the final checkout stages, where real-time emulation is much more critical, the designer may choose to run the emulator using the applicaton system's own clock. Integral ISE will support either mode of operation.

— Positioning of the Emulator Processor. Propagation delays in cables and buffers can contribute significant timing errors to the emulation process. For this reason, the emulation processor is located on a cable board only eight inches from the emulation plug to the applications system microprocessor socket. High-speed buffers are used to transmit signals between the emulation processor and the applications system.

— Emulation Processor Selection. Wherever possible an exact copy of the microprocessor being emulated is used as an emulation processor. For example, when an 8085 microprocessor is being emulated, an 8085 is used as the emulation processor. Instruction execution times and control signal timing are therefore identical to the timing that will be experienced in the final system.

- Breakpoint Conditions Provided for

Two breakpoint registers (BPC) can be defined on a 32-bit, maskable word. Each breakpoint register is specified by:

— 16 bits of address
— 8 bits of target CPU status
— 8 bits of user hardware status

Each bit of the 32-bit breakpoint register mask may be specified to compare on "$" or "0", or "don't care". The user can then specify a breakpoint to occur when any one of the following conditions is met:

— If BPC #1 is met
— If BPC #2 is met
— If BPC #1 or BPC #2 is met
— If BPC#1 is met after BPC#2 is met
— If BPC #2 is met after BPC #1 is met

Integral ISE can also be told to "coast" after the breakpoint combination has been satisfied before suspending operation:

— Coast until *n* more BPs are encountered
— Coast until *n* more BPC #1s are encountered
— Coast until *n* more BPC #2s are encountered
— Coast until *n* more read cycles are encountered
— Coast until *n* more write cycles are encountered
— Coast until *n* more instruction fetches are encountered
— *Coast until *n* more memory read cycles are encountered
— *Coast until *n* more memory write cycles are encountered
— *Coast until *n* more memory read or write cycles are encountered
— *Coast until *n* more I/O read cycles are encountered
— *Coast until *n* more I/O write cycles are encountered
— *Coast until *n* more I/O read or write cycles are encountered
— *Coast until *n* more interrupt acknowledges
— *Coast until *n* more serial input data
— *Coast until *n* more serial output data
— Coast until *n* more of all the above

Note: $0 < n < 256$; Those coast options preceded by a * are only available if the target microprocessor puts out the necessary status information.

There are five breakpoint (BP) combinations and sixteen "Coast" combinations, making a total of eighty total possible breakpoint conditions.

- Program Trace

Integral ISE maintains a constant record, in real-time, of the last 256 cycles performed by the target microprocessor. Forty bits of information are recorded for each cycle:

— 16 bits of address
— 8 bits of data
— 8 bits of CPU status
— 8 bits of user-defined status, via the 8-bit status cable

The type of information recorded in the trace memory is selectable in thirteen ways:

— All write cycles only
— All read cycles only
— Instruction fetches only
— *Memory read cycles only
— *Memory write cycles only
— *Memory read or write cycles
— *I/O read cycles only
— *I/O write cycles only
— *I/O read or write cycles
— *Interrupt acknowledges
— *Serial input data only
— *Serial output data only
— All of the above

Note: Those options preceded by a * are only available if the target microprocessor puts out the necessary status information.

Integral ISE generates a Sync Pulse each time data is recorded in the trace memory.

- Target Board Control Features

  The target microprocessor will be placed in an inactive state at the end of the current instruction when one of the following conditions occurs:

  —The user gives a halt-command to the given target
  —A breakpoint is encountered
  —The Integral ISE is in single-step mode

  When a target is halted, the user may take any one or all of the following actions:

  —Examine and change the target's registers, memory, or port
  —Dump trace memory for examination
  —Change emulation specifications
  —Change memory map

- Flexible Memory Mapping

  A 32K mapped memory space is available for the Integral ISE. The applications program may be mapped into Integral ISE memory in 1K blocks. These blocks need not be contiguous. The memory map may be specified and altered under program control, and any segment may be write protected. In addition, data may be copied from the applications system memory to the Integral ISE memory.

- Microsecond Timer

  National Semiconductor's Integral ISE has a 16-second timer which counts in one-microsecond increments. The user may use this timer to measure the time elapsed between any two points of this program. The two points in the program must be defined through breakpoint conditions; the clock starts counting as breakpoint #1 is encountered and stops when breakpoint condition #2 is encountered.

- User Status Cable

  Integral ISE provides the user with a six-foot cable carrying eight probes. The user may hook these probes anywhere in his system and treat the status of these points as part of his breakpoint word and trace a word.

Convenient Software

Several tools are provided to make the Integral ISE a very convenient emulation system to use. Many of the debugging features available for software development, like symbolic debugging, are now available for system development.

- Symbolic Debugging

  Programmers use symbols to reference program and data memory when writing programs, but they are usually required to use absolute hexadecimal addresses when referencing those locations during program debug. Integral ISE allows the designer to use those same symbols to reference program and data memory during program debug. A symbol table is generated when the program is first assembled or compiled in the host development system. That symbol table is passed to the driver program in the host system for use during the debugging operations. During debugging operations, symbols may be added or deleted, and symbol values may be redefined.

- In-Line Assembler

  A one-pass line-by-line assembler is provided to allow modification of object code in the Integral ISE memory or the applications system memory without having to manually convert symbolic instructions to machine language. The in-line assembler accepts program modifications in the assembly language of the target microprocessor, assembles them, and inserts them into the object program at the locations specified by the system programmer.

- Disassembler

  The disassembler reads specified segments of Integral ISE or applications system memory, disassembles them, and displays their contents in the assembly language mnemonics of the target microprocessor. This feature eliminates many of the tedious manual steps normally involved in application debug.

- Automatic Testing

  The application system designer often wishes to perform a predefined sequence of tests on the system over a relatively long period of time. Integral ISE has an automatic testing mode whereby the designer may write a sequence of test steps in a language similar to BASIC, store those tests in the memory of the host system, and initiate the test sequence. Integral ISE will perform the tests in the specified sequence and, if requested, record the results on a disc or a hard copy device of the host system. Branching and conditional branching are also permitted in the test program. This feature is especially useful for rigorous proof that all parts of the applications system are in fact working, for detecting and documenting infrequent failures, and for performing "life" tests.

The list of predefined test sequences resides in a file created by using the Integral ISE software or the development system's Text Editor. Once the file is resident on disc, it can be retrieved, deleted, edited, etc., by the Integral ISE Software Package.

The following commands allow the user to perform automatic testing functions:

DELETE	Deletes a range of lines from the test program.
EXECUTE	Executes the test program.
LIST	Lists the test program.
LOAD FAST INFILE	Loads the specified test program from disc.
SAVE FAST INFILE	Saves the test program on disc.
SCRATCH	Deletes the entire test program.
END	Directive to end test program and return control to command mode.
GOTO	Unconditional branch to another statement in test program.
IF	Conditional branch to another statement in test program.
INPUT	Enables user to interact with test program at run time to specify data values.
PRINT	Prints number and string data on console.
ERROR	Allows errors to occur during testing without halting the test.
CALL	Passes control to a line in an INFILE subroutine.
RETURN	Returns control from an INFILE subroutine.
SET PARAMETER	Sets a specified INFILE parameter to a value.

Command Summary

Initialization and Setup Commands

CHANGE	Change target-specific system configuration characteristics.
HOLD	Enables or disables hold timeout for the selected target processor.
INITIALIZE	Causes a reset of the target board firmware and clears the work registers of the selected target processor.
LATCH	Selects trigger for input validity from the user status cable.
LOCK	Forces all target processors into "hold" state to allow power-down of user system.
RESET	Indicates that the selected target processor registers are to be reset prior to the resumption of emulation.
NORESET	Rescinds the RESET command.
RADIX	Establishes the default input and display mode (binary, octal, decimal of hexadecimal).
WAIT	Enables or disables wait timeout for the selected target processor.

Memory Mapping/Demapping Control

MAP	This command enables or disables use of ISE memory and allows copying betwen ISE and user memory.
GUARD	Write-protects any block of target I/O ports or memory.
UNGUARD	Write-enables any block of target I/O ports of memory.

Breakpoint Control

BREAK	Suspends emulation when the specified break conditions are met in the target system.
TIME	Displays the time interval between occurence of breakpoints A and B, when B occurs after A.

Emulation Commands

RUN	Continues the system emulation until a break condition is satisfied.
STEP	Continues the system emulation in single-step mode.

Trace Control

TRACE	Selects target activity to be recorded into the trace memory.

Memory/Register/Port Modification and Display Commands

CHANGE	Replaces contents of memory locations with new data values or writes values to I/O ports.
DISPLAY	Displays portions of target processor memory, register, I/O port, or trace data.
MOVE	Transfers a region of memory into another region.
SEARCH	Searches a range of memory locations for a specified value and displays the locations where the value is found.

Symbol Table and File Manipulation Commands

DELETE	Deletes the specified symbol(s) from the symbol table file.
LOAD	Fetches an in-file program or load file from disk medium or opens a symbol table file.

SAVE	Creates and saves in-file programs or load files on disk or closes symbol table files.
LIST	Display all or part of the INFILE.

Utility Commands

ECHO	Selects the host processor's echoing device for hard copy history.
PRINT	Displays strings and expressions.
ARCHIVE	Saves the system status on disk for later retrieval.
RESTORE	Restores the system status saved by ARCHIVE.
DIAGNOSTIC	Performs limited testing of Trace and Memory Boards.

Specifications

Environmental

Operating Temperature 10°C (50°F) to 32°C (90°F)

Storage Temperature -40°C (-40°F) to 75°C (167°F)

Power

All boards +5 V_{DC} each

Board Involved	Worst
Target Board	4.2A (21.0W)
Cable Board	1.9A (9.5W)
Integral ISE Set:	
Trace Board	3.6A (18.0W)
Status Board	0.3A (1.5W)
Memory Board	5.5A (27.5W)
Total	15.5A (77.5W)

Memory

Mappable — 32K bytes in 1K byte increments

Trace — 256 × 40 bits

Physical

Target Board
Height — 7.15 in. (18.16 cm)
Width — 12.00 in. (30.48 cm)
Depth — 0.50 in. (1.27 cm)

Cable Board
Height — 9.00 in. (22.86 cm)
Width — 4.55 in. (11.56 cm)
Depth — 0.54 in. (1.37 cm)

Cable Board Housing
Height — 9.75 in. (24.76 cm)
Width — 5.75 in. (14.60 cm)
Depth — 1.62 in. (4.11 cm)

Status Board Housing
Height — 6.00 in. (15.24 cm)
Width — 3.00 in. (7.62 cm)
Depth — 0.50 in. (1.27 cm)

Memory Board
Height — 6.75 in. (17.75 cm)
Width — 12.00 in. (30.48 cm)
Depth — 0.50 in. (1.27

Trace Board
Height — 6.75 in. (17.75 cm)
Width — 12.00 in. (30.48 cm)
Depth — 0.50 in. (1.27 cm)

Cables
Target Board Cables — 72.0 in. (6 ft.)
Cable-Board/User Cable — 15.0 in. (1 ft. 3 in.)

Approximate overall length from STARPLEX base module to the 40-pin connector—96 in (8 ft.)

Prerequisites

Any STARPLEX/STARPLEX II Development System.

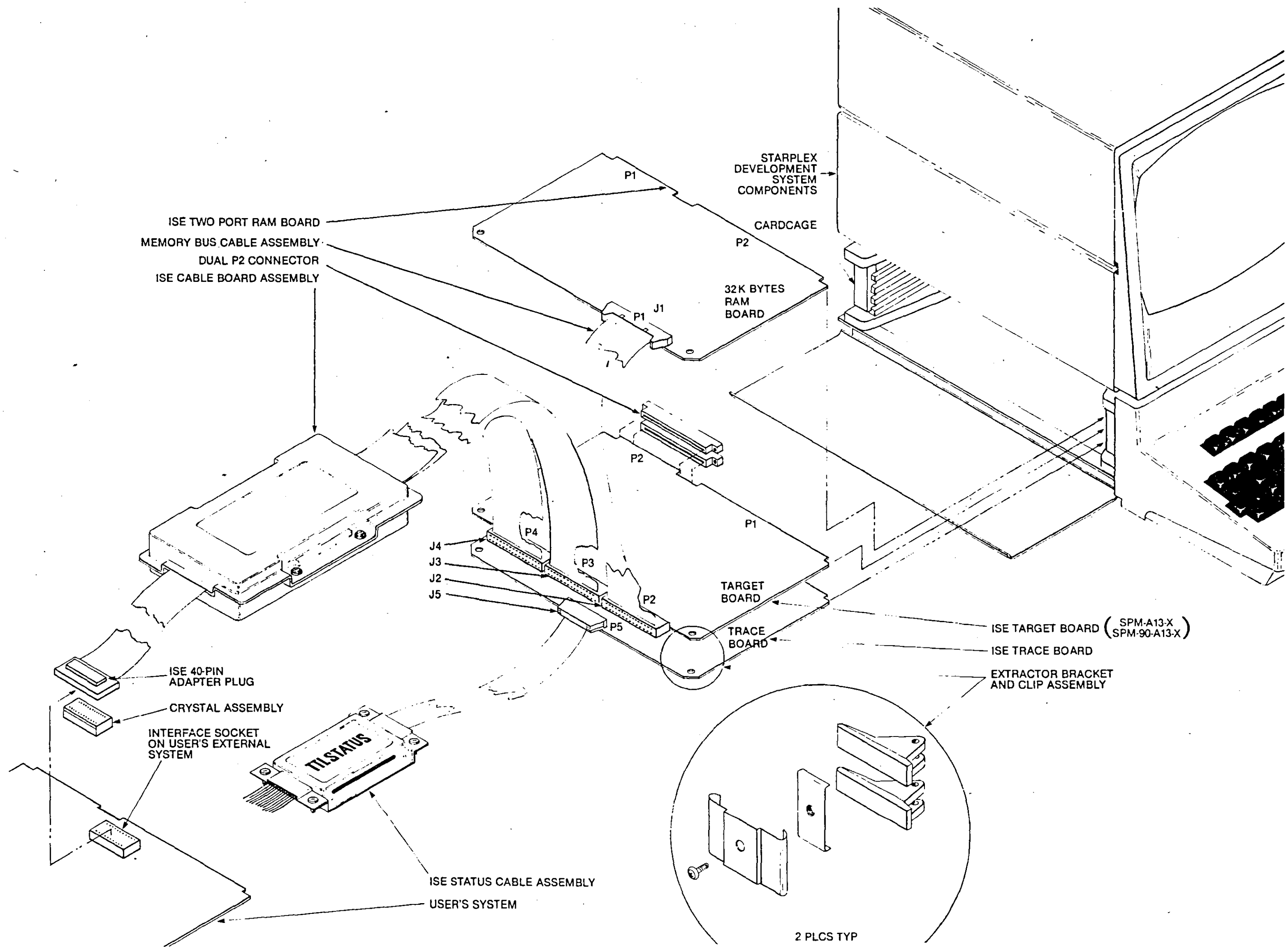


FIGURE 1. Integral ISE Components Installation

Order Information

(Includes One 32K Byte Mapped Memory Board, One Trace Board, Cables, and One ISE TTL Status Cable Pod.)

For STARPLEX Development Systems:

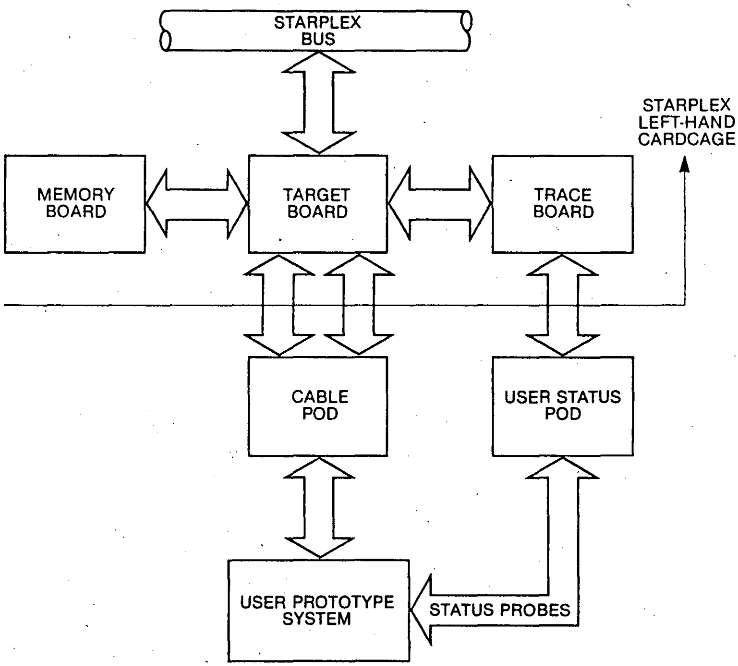
SPM-A13	Integral In-System Emulator Package
SPM-A13-3	8085 Emulator Package
SPM-A13-4	NSC800 Emulator Package
SPM-A13-7	Z80 Emulator Package

For STARPLEX II Development Systems:

SPM-90-A13	Integral In-System Emulator Package
SPM-90-A13-3	8085 Emulator Package
SPM-90-A13-4	NSC800 Emulator Package
SPM-90-A13-7	Z80 Emulator Package

Documentation

420305789-001	8080/8085 Macroassembler Software User's Manual
420306198-001	NSC800 Cross-Assembler Software User's Manual
420306240-001	8085 Integral ISE User's Manual
420306421-001	NSC800 Integral ISE User's Manual
420306692-001	Z80 Integral ISE User's Manual
420308101-001	80CX48 Integral ISE User's Manual



Integral ISE System Configuration
SPM-A13 with SPM-A13-X,
SPM-90-A13 with SPM-90-A13-X
(Total: 3 Boards and 2 Pods)

MOLE™ (Microcontroller On Line Emulator) Development System

MOLE SYSTEM

A MOLE (Microcontroller On Line Emulator) system consists of three components: a MOLE Brain board, a MOLE Personality board, and the user's host CPU. This partitioning provides the microcontroller design engineer with a new concept in flexibility. As an example of this flexibility consider the latitude in choice of host CPU. The host CPU may be National Semiconductor's COP400-PDS, STARPLEX I™ or STARPLEX II™, Intel's MDS800 or INTELLEC™ Series II, or any other CPU operating under CP/M®—even one of many inexpensive personal computers. Software provided by National Semiconductor will run under control of the host computer CP/M operating system.

Further flexibility is provided by the Personality board. This component tailors the system to the emulation of a single microcontroller family or device. For instance, one Personality board supports COPS™ CMOS family, another, the NS455 Terminal Management Processor. These two boards support 21 microcontroller device types.

The Brain board is the pivotal component of the MOLE concept. In conjunction with a CRT terminal and Personality board it provides the user with a freestanding workstation for microcontroller emulation. It ties the system together by communicating with the host CPU, the Personality board and other Brain boards. Multiple Brain boards, tied to a common host, can function as emulators for individual projects where each Brain board is a separate project workstation. They can also function as individual microcontroller emulators within a multicontroller system.

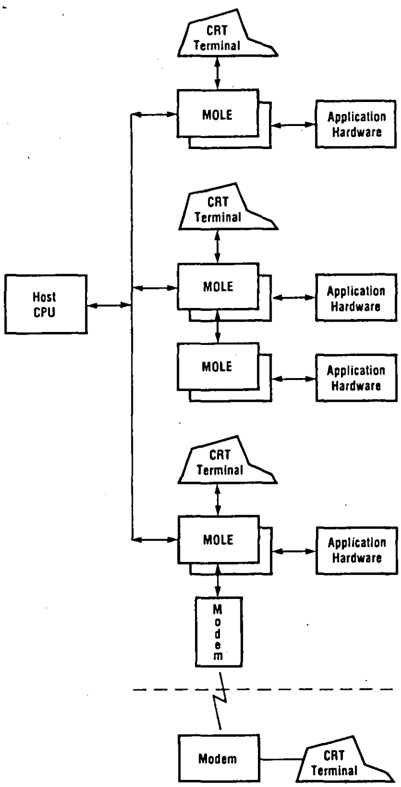
The flexibility of the MOLE concept allows the user to efficiently emulate a wide range of microcontrollers in any application environment.

The MOLE components have been selected to provide maximum utility. The host CPU contributes cost effective bulk storage and high speed processing. Disk editing and assembly operations are handled by the host CPU. The results are down loaded to the Brain board over the RS-232 link. The Brain/Personality board combination then provides full emulation capabilities.

The resident firmware allows the user to: display and alter memory in both hex and mnemonic format; initiate breakpoints, traces and timing on addresses or external events; examine and modify the internal resources of the microcontroller being emulated. Hardware and firmware are provided for programming EPROMs and EEROMs.

Once debugged, the code is transmitted via modem to National Semiconductor for use in creating the tooling required to manufacture the masked microcontroller part.

Thus the MOLE concept provides maximum flexibility to accommodate microcontroller selection and maximum utility for product development.



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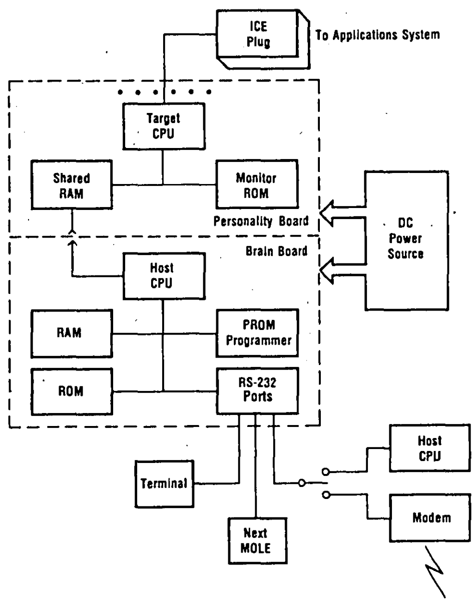
MOLE System Configuration



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MOLE System Block Diagram

MOLE BRAIN BOARD

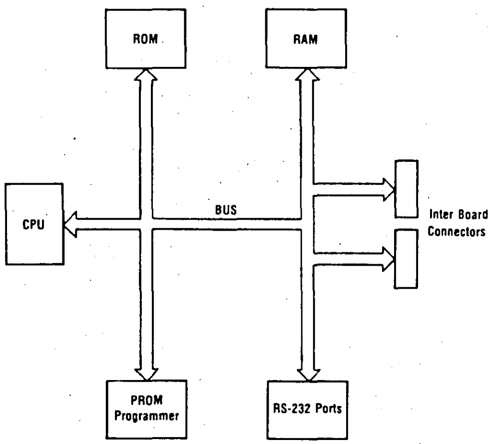
The Brain board is the pivotal component of the MOLE concept. In conjunction with a CRT terminal and Personality board it provides the user with a freestanding workstation for microcontroller emulation. It ties the system together by communicating with the host CPU, a Personality board and other Brain boards. Multiple Brain boards, tied to a common host, can function as emulators for individual projects where each Brain board is a separate workstation. They can also function as individual microcontroller emulators within a multicontroller system.

The choice of host CPU is largely left to the user. The host CPU may be National Semiconductor's COP400-PDS, STARPLEX I or STARPLEX II, Intel's MDS800, INTELLEC Series II, or any other CPU operating under CP/M—even one of many inexpensive personal computers.

The MOLE Brain board uses a NSC800™ microprocessor with 64K RAM and 32K ROM. It has an EPROM/EEROM programmer for on line changes in software. There are three RS-232 ports and a bus to connect the Brain to the MOLE Personality boards for actual emulation of software in the user's application system.

The RS-232 ports are used via the communication routine, in firmware, to interface with a host CPU and a user terminal, plus a printer or other MOLEs. This gives the user great utility during system development.

The bus allows the user access to the entire MOLE family of Personality boards. These Personality boards tailor the MOLE system to each specific microcontroller family. Thus the MOLE concept provides maximum flexibility to accommodate microcontroller selection and maximum utility for product development.



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MOLE Brain Board Block Diagram

- Supports NSC's entire family of MOLE Personality boards
- Single 5V operation
- Ability to interface to a wide variety of host computers
- Full communication control with host computer, a modem or other MOLEs
- Three RS-232 ports
- Auto baud selection (110, 300, 600, 1200, 2400, 4800, 9600, 19200 baud)
- Mask data submission via modem
- Self diagnostics
- Program EPROMS
  - MM2716, NMC27C16
  - MM2732, NMC27C32
  - NMC2764
- Program EEROMS
  - NMC2816

PHYSICAL SIZE
10" × 12"

POWER REQUIREMENTS
+5V DC @ 3.5A
+21V or +25V @ 50mA
(Optional—required only for PROM programming)

WHAT P/N TO ORDER
MOLE-BRAIN

MOLE-BRAIN PACKAGE CONTAINS
MOLE Brain Board
MOLE Brain User's Manual
2 RS-232 Cables
Power Cable
Miscellaneous Hardware

MOLE COPS CMOS FAMILY PERSONALITY BOARD

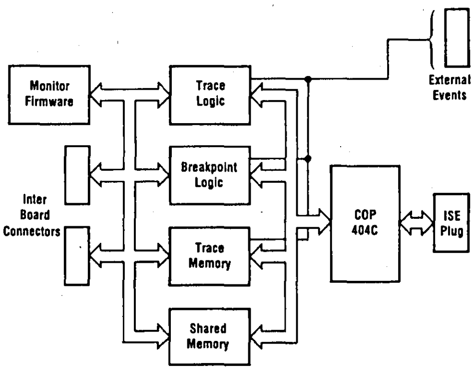
The CMOS COPS Family Personality Board supports the emulation of the COP400 CMOS family of microcontrollers, specifically, the COP444C, COP445C, COP424C, COP425C, COP426C, COP410C, COP411C. The Personality board allows the user to emulate the appropriate CMOS Microcontroller in the end system for fast development of the user's application software and hardware. The Personality Board consists of: a monitor in firmware; the hardware to control the operation of the microcontroller in the emulation system; and an In-System-Emulator cable to connect the emulator to the application system. The ISE™ cable has the same pin configuration as the final masked part.

The Personality board monitor is contained in 32K of ROM and is directly executable by the NSC800 microprocessor on the Brain board. The monitor commands will allow the user to execute the application software, examine internal registers and I/O, examine and change object code, execute time measurement and set trace or breakpoints.

The Personality board also contains shared memory (RAM) for application programs and the necessary hardware logic for trace and breakpoint operation.

As soon as the program is thoroughly tested, the code is sent via modem to National Semiconductor for use in creating the tooling required to manufacture the masked CMOS COPS production part.

The CMOS Personality board is only one of a family of Personality boards that tailor the MOLE system to a specific microcontroller family. Thus, the MOLE concept provides maximum flexibility in microcontroller selection and maximum utility for product development.



MOLE CMOS COPS Family Personality Board Block Diagram

- Supports entire COPS CMOS family
- Single 5V operation
- Firmware monitor directly executed by Brain CPU
- Firmware diagnostics directly executed by Brain CPU
- 2K bytes of shared memory
- 256 deep trace memory
- Eight external event inputs
- Trace on multiple addresses
- Trace on multiple address ranges
- Trace on external events
- Breakpoint on multiple addresses
- Breakpoint on multiple address ranges
- Breakpoint on external events
- List and alter shared memory
- Print and modify internal registers
- Singlestep
- Next—singlestep around subroutine calls
- Trigger output for logic analyzer
- Real time emulation

PHYSICAL SIZE
12″ × 12″

POWER REQUIREMENTS
+5V @ 3.5A

WHAT P/N TO ORDER
MOLE-COPS-PB001

MOLE-COPS-PB001 PACKAGE CONTAINS
MOLE CMOS COPS Personality Board
MOLE CMOS COPS PB Manual
3 Emulator Cables
Power Cable
Miscellaneous Hardware

MOLE NS455 (TMP) PERSONALITY BOARD

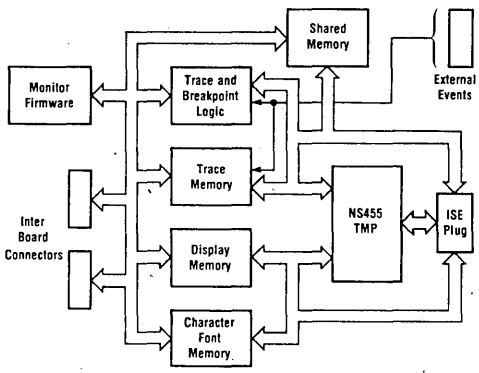
The NS455 Personality board allows the MOLE system to emulate the NS455 Terminal Management Processor. The Personality board consists of a firmware monitor, emulation hardware and an In-System-Emulator, ISE, cable. The ISE cable has the same pin out as the masked part and allows the Personality board to function within the application system.

The NSC800 CMOS microprocessor, located on the Brain board, directly executes the 32K of Personality board monitor firmware. The monitor allows execution of application software, examination and alteration of internal registers, examination and alteration of memory contents and setting of trace and breakpoints. The ISE cable connects these capabilities to the application system. Up to eight external events may be traced and stored in the 2K deep trace memory. Multiple breakpoint and machine code unassembly commands are at the user's disposal.

Application programs of up to 8K bytes in length may be executed from Personality board RAM or user system memory. Video display RAM also may be accessed from the Personality board (2K bytes) or user system memory (64K × 16). Unique character sets may be displayed by accessing a high speed character font memory.

Once debugged, the code is transmitted via modem to National Semiconductor for use in creating the tooling required to manufacture the masked NS455 part.

The NS455 is only one of a family of Personality boards that tailor the MOLE system to a specific microcontroller or microcontroller family. Thus the MOLE concept provides maximum flexibility to accommodate microcontroller selection and maximum utility for product development.



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MOLE NS455 (TMP) Personality Board Block Diagram

- Supports NS455 (TMP) microcontroller
- Single 5V operation
- Firmware monitor directly executed by Brain CPU
- Firmware diagnostics directly executed by Brain CPU
- 8K bytes of shared program memory
- 2K bytes of video display memory
- 2K bytes of character font memory
- 2048 deep trace memory
- Eight external event inputs
- Trace on multiple addresses
- Trace on multiple address ranges
- Trace on external events
- Breakpoint on multiple addresses
- Breakpoint on multiple address ranges
- Breakpoint on external events
- List and alter shared memory
- List and alter display memory
- List and alter character font memory
- Print and modify internal registers
- Singlestep
- Next—singlestep around subroutine calls
- Trigger output for logic analyzer
- Real time emulation

PHYSICAL SIZE
12″ × 12″

POWER REQUIREMENTS
+5V @ 4A

WHAT P/N TO ORDER
MOLE-TMP-PB001

MOLE-TMP-PB001 PACKAGE CONTAINS
MOLE TMP Personality Board
MOLE TMP PB User's Manual
1 Emulator Cable
Power Cable
Miscellaneous Hardware

MOLE SOFTWARE

MOLE supports host software packages for CP/M based systems and COPS-PDS systems. These packages contain all the necessary software for fast and efficient program development. The basic package contains user's manual, target cross assembler, communication program and any microcontroller or host dependent utilities. Host software is supplied in the following disk formats: CP/M IBM-3740, CP/M Intel 8 in. single/double density and PDS-COPS. MOLE software is purchased separately from MOLE hardware.

WHAT P/N TO ORDER FOR COPS DEVELOPMENT

Host Computer	Disk Format	Order Code
PDS II	COPS-PDS 8 in. single density	MSFW-COPS-PDS
STARPLEX I STARPLEX II	8 in. standard (IBM/3740) single density CP/M	MSFW-COPS-CPM
Intel MDS800-SD INTELLEC II-SD	Intel 8 in. single density CP/M	MSFW-COPS-INT-S
Intel MDS800-DD INTELLEC II-DD	Intel 8 in. double density CP/M	MSFW-COPS-INT-D
IBM/3740 CP/M	8 in. standard (IBM/3740) single density CP/M	MSFW-COPS-CPM

WHAT YOU GET

Each COP400 microcontroller package specifically contains:

- USER'S MANUAL
- DISKETTE containing:

ASM400	COP400-Series cross assembler
LINK	Code linkage utility (PDS only)
COMM	MOLE/Host communication program
HEXLM	Code conversion utility (CP/M only)
LMHEX	Code conversion utility (CP/M only)
MASKTR	ROM, OPTION transmittal/checking program (PDS only)

WHAT P/N TO ORDER FOR NS455 DEVELOPMENT

To select NS455 microcontroller development package for your system locate the required disk format and use the adjacent ordering code.

Host Computer	Disk Format	Order Code
STARPLEX I STARPLEX II	8 in. standard (IBM/3740) single density CP/M	MSFW-TMP-CPM
Intel MDS-SD	Intel 8 in. single density CP/M	MSFW-TMP-INT-S
Intel MDS-DD	Intel 8 in. double density CP/M	MSFW-TMP-INT-D
IBM/3740 CP/M	8 in. standard (IBM/3740) single density CP/M	MSFW-TMP-CPM

WHAT YOU GET

Each NS455 microcontroller package contains:

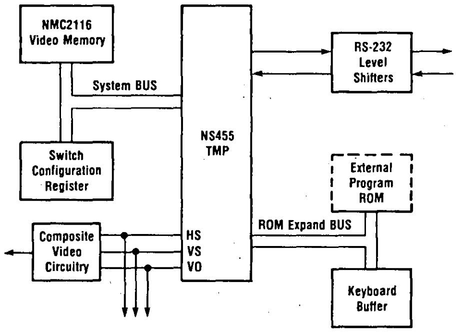
- USER'S MANUAL
- DISKETTE containing:

ASM455	NS455 series cross assembler
COMM	MOLE/Host communication program
HEXLM	Code conversion utility
LMHEX	Code conversion utility
FONT	Character font building utility

NS455 DEMONSTRATION BOARD

The NS455 Demo Board typifies the type of minimum CRT data terminal system possible with a masked NS455 Terminal Management Processor. With the addition of a video monitor, ASCII encoded keyboard and power supply one has a complete data terminal. Alternatively one may write his own program and have the NS455 execute it by going external for program memory.

Through the many Escape sequences programmed into the chip, a user has complete control over terminal operation. In addition, the many cursor and character attribute display options available may be easily evaluated.



TL/DD/6736-6

TMP Demo Board Block Diagram

PART NUMBERS

The TMP (Terminal Management Processor) boards can be ordered by requesting the following part numbers:

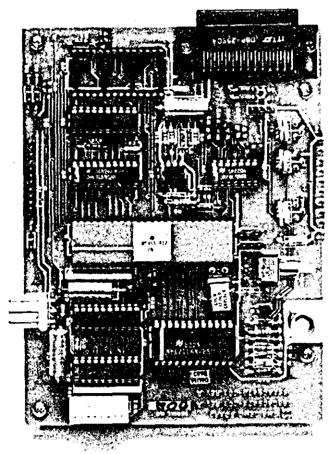
TMP-DEMO-12
(for 5 × 7 character font—12 MHz bandwidth)

TMP-DEMO-18
(for 7 × 9 character font—18 MHz bandwidth)

CONTAINS:
Demo Board
NS455-Series Data Sheet
Demo Board Operating Manual

FEATURES

- Internal masked ROM or external EPROM program execution
- 80 Column × 25 Row display
- 5 × 7 characters with 2 level descenders
- 12 MHz video bandwidth
- BALL or Composite Video Output
- 50/60 Hz operation
- RS232C Serial Interface with Full Duplex 110-19.2K BAUD
- Status Line Display
- 24 Escape Sequences
- 15 Control Sequences

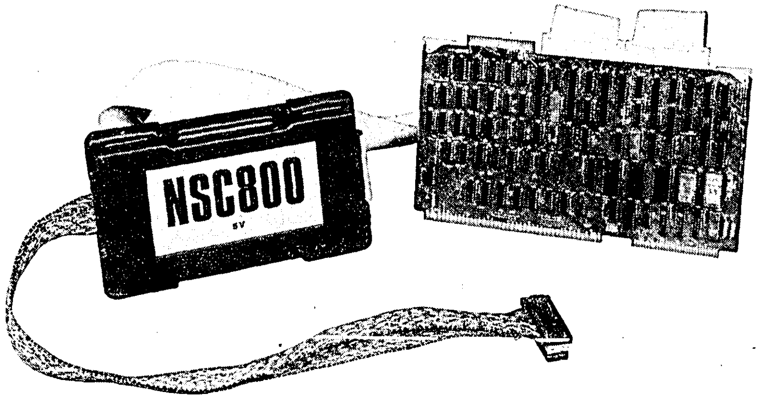


TL/DD/6736-7

TMP Demo Board

National Semiconductor

NSC800™ Emulator Package



- **Real-Time In-System Emulation of NSC800 Microprocessor**
- **Supports Two Modes of Operation**
  - Program Development
  - Single Processor Emulation
- **Plugs Directly Into Any STARPLEX™/STARPLEX II™ Development System**

Product Overview

National's NSC800 Emulator Package gives the designer of NSC800 based systems the kind of sophisticated tool required for efficient microcomputer development. The NSC800 Emulator Package, in conjunction with the Integral ISE™ Package and the STARPLEX/STARPLEX II Development System, provides capabilities that up to now have not been available in this type of instrument.

National's Integral ISE Package is installed directly in any STARPLEX/STARPLEX II Development System. This package consists of two logic boards (TRACE logic and MAPPED MEMORY). These two logic boards provide the user with 32K bytes tracing and memory mapping. These resources are available for the emulation of any processor since the individual emulation packages are the only components dedicated to particular processors. This approach simplifies changing processors since the user needn't learn a new ISE™ language each time he changes emulation packages.

The NSC800 Emulator Package provides the physical and electrical interface between the Integral ISE package, the STARPLEX Development System and an NSC800 based system undergoing development. When installed in a STARPLEX Development System, it connects to the User's System via the Cable Pod and a 40-pin plug to the system under development. In this configuration, the entire system supports two modes of operation. These modes are program development and single processor emulation.

The program development mode permits the user to develop and debug his software even though he has no prototype hardware available. The emulator package provides the clocks and memory necessary for this task. During emulation of a single processor, the user's hardware provides the actual clock signal thus forcing the entire Integral ISE system to operate at the actual clock rate of the user's system.

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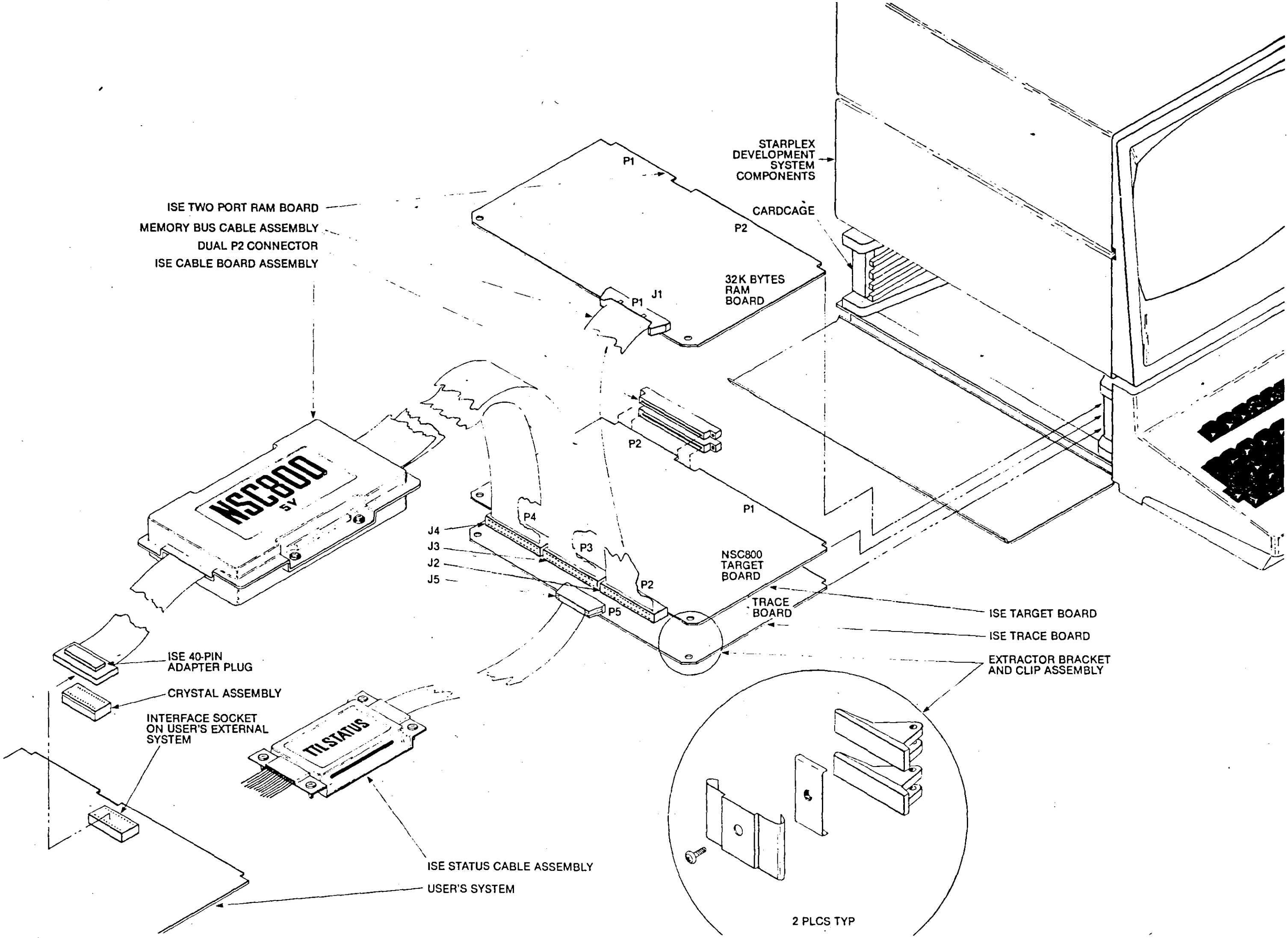
Loading Information for 40-Pin Connector

Pin No.	Output Load (mA)		Input Load (μA)		Time Delay (T_D) Between NSC800 & 40 Pin Plug	Mnemonic
	$V_{OH} = I_{OH}$	$V_{OL} = I_{OL}$	$V_{IH} = I_{IH}$	$V_{IL} = I_{IL}$		
1	−.95	1.6	—	—	0	A_8
2	−.95	1.6	—	—	0	A_9
3	−.95	1.6	—	—	0	A_{10}
4	−.95	1.6	—	—	0	A_{11}
5	−.95	1.6	—	—	0	A_{12}
6	−.95	1.6	—	—	0	A_{13}
7	−.95	1.6	—	—	0	A_{14}
8	−.95	1.6	—	—	0	A_{15}
9	−.95	1.6	—	—	0	CLK
10	—	—	—	—	—	X_{OUT}
11	—	—	—	—	0	X_{IN}
12	−10	48	80	−250	27 ns	AD_0
13	−10	48	80	−250	27 ns	AD_1
14	−10	48	80	−250	27 ns	AD_2
15	−10	48	80	−250	27 ns	AD_3
16	−10	48	80	−250	27 ns	AD_4
17	−10	48	80	−250	27 ns	AD_5
18	−10	48	80	−250	27 ns	AD_6
19	−10	48	80	−250	27 ns	AD_7
20	—	—	—	—	—	GND
21	—	—	20	−200	38 ns	$\overline{NMI}$
22	—	—	20	−200	38 ns	$\overline{RSTA}$
23	—	—	20	−200	38 ns	$\overline{RSTB}$
24	—	—	20	−200	38 ns	$\overline{RSTC}$
25	—	—	20	−200	38 ns	$\overline{INTR}$
26	−.96	1.6	—	—	0	$\overline{INTA}$
27	−.96	1.6	—	—	0	S_1
28	−.96	1.6	—	—	0	$\overline{RFSH}$
29	−.95	1.6	—	—	0	S_O
30	−.95	1.6	—	—	0	ALE
31	−15	64	—	—	9 ns	$\overline{WR}$
32	−15	64	—	—	9 ns	$\overline{RD}$
33	—	—	50	−400	38 ns	$\overline{RESET\ IN}$
34	−.95	1.6	—	—	0	$IO/\overline{M}$
35	−.98	1.8	—	—	0	$\overline{BACK}$
36	—	—	20	−200	43 ns	$\overline{BREQ}$
37	−.96	1.6	—	—	22 ns	RESET OUT
38	—	—	50	−400	30 ns	WAIT
39	—	—	20	−200	0	$\overline{PS}$
40	*	*	*	*	—	V_{CC}

* V_{CC}@ +5V I_{CC} = 1 mA max.



NSC800 Emulator with Integral ISE Components Installation

Specifications

Environmental

Operating Temperature 10°C (50°F) to 32°C (90°F)

Storage Temperature −40°C to −40°F

Power

All Boards $+5V_{DC}$ each

Board Involved	Typical	Worst
NSC800 Target Board	3.6A (18.0W)	4.2A (21.0W)
NSC800 Cable Board	1.4A (7.0W)	1.9A (9.5W)
Integral ISE Set		
Trace Board	2.0A (10.0W)	3.6A (18.0W)
Status Board	0.3A (1.5W)	
Memory Board	2.7A (13.5W)	5.5A (27.5W)
Total:	50.0 W	77.0 W

Physical

Target Board
Height — 7.15 in. (18.16 cm.)
Width — 12.00 in. (30.48 cm.)
Depth — 0.50 in. (1.27 cm.)

Cable Board
Height — 9.00 in. (22.86 cm.)
Width — 4.55 in. (11.56 cm.)
Depth — 0.54 in. (1.37 cm.)

Cable Board Housing
Height — 9.75 in. (24.76 cm.)
Width — 5.75 in. (14.60 cm.)
Depth — 1.62 in. (4.11 cm.)

Status Board Housing
Height — 6.00 in. (15.24 cm.)
Width — 3.00 in. (7.62 cm.)
Depth — 0.50 in. (1.27 cm.)

Memory Board
Height — 6.75 in. (17.75 cm.)
Width — 12.00 in. (30.48 cm.)
Depth — 0.50 in. (1.27 cm.)

Trace Board
Height — 6.75 in. (17.75 cm.)
Width — 12.00 in. (30.48 cm.)
Depth — 0.50 in. (1.27 cm.)

Cables
Target Board Cables — 72.0 in (6 ft.)
Cable-Board/User Cables — 15.0 in (1 ft. 3 in.)
Approximate overall length from STARPLEX base module to the 40-pin connector — 96 in. (8 ft.)

Prerequisites

Any STARPLEX/STARPLEX II Development System and Integral In-System Emulator Package (SPM-A13, SPM-90-A13)

Order Information

(Includes Target Board, Lightweight Plastic Cable Pod, Cables, Software for ISE Host Driver and NSC800 Display Charge for Mnemonic Assembly and Disassembly. SPM-A13-4 also includes NSC800 Cross-Assembler Software.)

For STARPLEX Development Systems:

SPM-A13	Integral In-System Emulator Package
SPM-A13-4	NSC800 (5V) Emulator Package

For STARPLEX II Development Systems:

SPM-90-A13	Integral In-System Emulator Package
SPM-90-A13-4	NSC800 Emulator Package

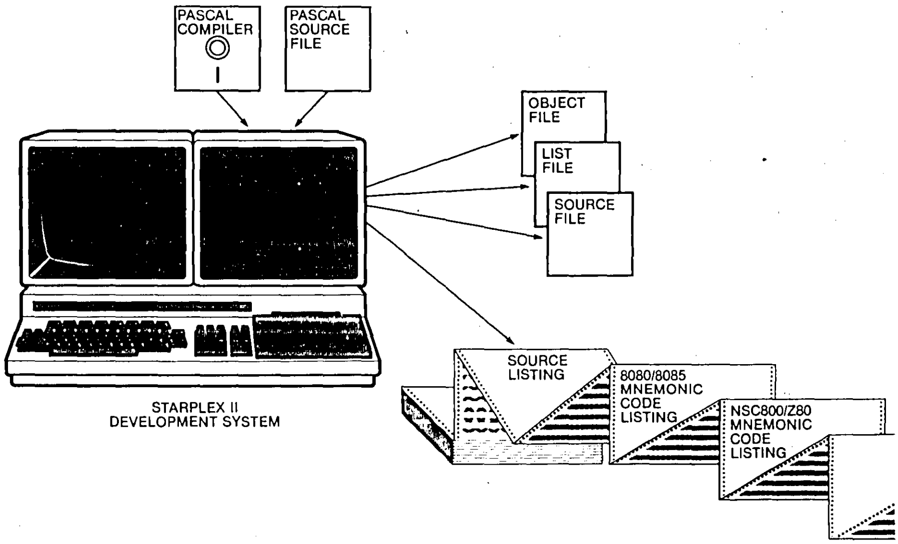
Documentation

420306198-001	NSC800 Assembler Software User's Manual[1]
420306241-001	Integral In-System Emulator (NSC800) User's Manual[2]

1. Included with SPM-A13-4 not SPM-90-A13-4.
2. Included with both SPM-A13-4 and SPM-90-A13-4.

National Semiconductor

PASCAL
PASCAL High Level Language Compiler For STARPLEX II™ Development Systems



- **Executes On All STARPLEX II Development Systems**
- **Compatible With Existing ISO Standard PASCAL**
- **Highly Portable And Extended Source Programs**
- **Code Generation For 8080/8085 and NSC800™/Z80 Microprocessors**
- **Relocatable And Linkable Object Code Output**
- **Reentrant Procedures as Specified by User**
- **Extensions For Easy Hardware Access Via High Level Statements (Absolute Addresses and Input/Output Ports)**

Product Description

PASCAL is a high level language compiler designed for STARPLEX II Development Systems. Available in two versions, this highly efficient and powerful compiler generates relocatable object code for 8080/8085 and NSC800/Z80 microprocessors.

PASCAL has proven to be one of the most popular, effective and powerful program development tools available today. With STARPLEX II PASCAL, programmer productivity is greatly improved because the programmer can concentrate on system development rather than all the details of assembly languages. Since PASCAL uses data structures that are very close to typical microprocessor architectures, it allows for efficient use of the machine. PASCAL programs are efficiently converted to assembly language instructions thus requiring fewer statements. Software development and maintenance costs are significantly reduced.

Free form PASCAL source programs are efficiently and effectively converted into 8080/8085 and NSC800/Z80 assembly language instructions. A given program, when written in PASCAL, requires much fewer statements than would the equivalent program written in assembly language. Thus, software development and maintenance costs are significantly reduced due to the block oriented structure that results naturally from the use of PASCAL. User programming conventions and structured programming techniques are easily accommodated by the free form source statements of PASCAL.

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Functional Description

The STARPLEX II PASCAL compiler is a system program which accepts PASCAL language source modules and produces linkable object modules. Object modules may be linked to form executable PASCAL programs. The STARPLEX II PASCAL compiler is compatible with the International Standards Organization (ISO) standard and has extensions to facilitate access to and manipulation of machine data structures. Code generated by the STARPLEX II PASCAL compiler is native machine code, rather than the intermediate p-code found in other microcomputer PASCAL compilers. The execution speed of programs compiled to machine code is much faster than those complied to p-code, thus maintaining the programming advantages of a high-level language without sacrificing execution speed.

The STARPLEX II PASCAL compiler invocation is similar to that of other STARPLEX II software. In many cases, no changes to existing PASCAL programs are required. STARPLEX II PASCAL has a number of extensions which may be incorporated into existing PASCAL programs to make it faster, smaller, and easier to debug. In many cases, because of STARPLEX II PASCAL's many low-level escapes to the machine level, programs written in STARPLEX II PASCAL can be comparable in speed to programs written in assembly language.

The STARPLEX II PASCAL compiler reads source files containing PASCAL source modules and produces:

- a linkable object module containing object code,
- a listing of the STARPLEX II PASCAL source statements,
- a listing of syntax and semantic errors and warning messages,
- an optional listing of object code in assembly language mnemonics.

Compilation is one step in the formation of an executable PASCAL program. The formation of a complete program involves the following steps:

- Writing the PASCAL "Source Modules" using the TEXT EDITOR.
- Compiling the source files to produce linkable "Object Modules".
- Linking the object modules to create an executable PASCAL "Load Module".

When the source module(s) have been created using the STARPLEX II TEXT EDITOR, choose the correct PASCAL diskette for the type of compilation desired. The 8080/8085 version of the PASCAL compiler can generate code that can be used for an 8080 or 8085 based system, while the NSC800 version of the PASCAL compiler can generate code that can be used for an NSC800 or Z80 based systems.

Extensions

As stated before, the STARPLEX II PASCAL provides many extensions to the ISO standard PASCAL. The following is an overview of the extensions.

1. Direct files: To enhance standard PASCAL's file capabilities, direct (random access) files are implemented, and accessed with the SEEK procedure.

2. Variable-length strings: A special variable-length string type called the LSTRING is implemented in STARPLEX II PASCAL to overcome standard PASCAL's inadequate string-handling capabilities. Special predeclared procedures and functions are available to facilitate use of the feature.

3. Super arrays: A special variable-length array declaration permits both passing arrays of different lengths to a reference parameter, as well as dynamic allocation of arrays of difference lengths.

4. BYTE/WORD types: Predeclared BYTE (0-255) and WORD (0-65535) types are available to facilitate programming at the system level.

5. String reads: Strings can be read as structures rather than character by character as with the standard procedures READ and READLN.

6. Nondecimal numbering: Hexadecimal, octal, and binary numbering are allowed to facilitate programming at the byte and bit level.

7. Address types (segmented and unsegmented): A special address type is implemented to allow manipulation of actual machine addresses.

8. Interface to assembly language: PUBLIC and EXTERN procedures, functions and variables are implemented to allow for low-level interfacing to assembly language and library routines.

9. Separate compliation: MODULES are implemented to allow portions of a program to be compiled at separate times.

10. VALUE section: Variables in a program can be given initial constant values in the VALUE section of a program.

11. Structured function return values: Functions can return values of a structured type, as well as values of simple type.

12. Support for interactive files: A special internal mechanism called "lazy evaluation" allows normal interactive input from terminals.

13. OTHERWISE in CASE statements: An OTHERWISE clause can be used in CASE statements to avoid explicitly specifying each case constant.

14. STATIC attribute for variables: Variables can be given the STATIC attribute to indicate that they are allocated at a fixed location in memory rather than on the stack.

15. ORIGIN attributes: Variables, procedures, and functions can be given the ORIGIN attribute to indicate their absolute location in memory.

16. Underscores in identifiers: Identifiers may contain underscores to improve their readability.

User Interface

Listings

The PASCAL compiler can provide, upon request, source and object listings. Diagnostics will be provided, regardless of list options.

Source listings will include statement numbers with corresponding source statements.

Object listings will show line number with corresponding object code (pseudo-assembly language) as well as relative memory locations and statistics (e.g., resources used) for the compilation.

Diagnostic Messages

Each error and warning flag contains a code number and a brief message. The code number indicates where in the list of error messages, a detailed explanation of that particular error or warning can be found. The brief message indicates an overview explanation of the incorrect condition detected.

Code Generation and Optimization

The STARPLEX II PASCAL compiler handles local optimizations: basic block optimization, competent register allocation, special casing for common constructs, some strength reduction, removal of dead code and of branch-around-branch. This produces smaller, faster and efficient object code.

Predefined Procedures and Functions for Run-Time Support

A number of predefined procedures and functions are included in the PASCAL compiler library which the user can use to facilitate his programming. These procedures and functions perform I/O, data allocation, arithmetic, string, and system operations. The procedures and functions are divided into the following categories:

- I/O routines
- Dynamic allocation routines
- Mathematic routines
- String routines
- Manipulation routines
- Library management routines

While the Library procedures and functions must be declared EXTERN, all the other functions and procedures are predeclared and hence do not have to be declared in the user's program. The use of these procedures and functions therefore do not require extra statement lines in the program itself.

Example of a PASCAL Program

```
                                                              Page 1
                                                            07/22/82
                                                            00:32:51
                          NSC Starplex-II Pascal - version 2.06 - 7/82
PROGRAM shellsort (input, output);
   CONST
     maxlength = 1000;
   TYPE
     index = 1 .. maxlength;
     rowtype = ARRAY [index] OF integer;
   VAR
     inrow : rowtype;
     count : 0 .. maxlength;
     ix : index;

   PROCEDURE sort (VAR row : rowtype; length : index);
     VAR
       jump, m, n : index;
       temp : integer;
       alldone : boolean;
     BEGIN
       jump := length;
       WHILE jump > 1 DO
         BEGIN
           jump := jump DIV 2;
           REPEAT
             alldone := true;
             FOR m := 1 TO length - jump DO
               BEGIN
                 n := m + jump;
                 IF row[m] > row[n]
                   THEN
                     BEGIN
                       temp := row[m];
                       row[m] := row[n];
                       row[n] := temp;
                       alldone := false;
                     END;
               END; (* for *)
           UNTIL alldone;
       END;  (* while *)
   END; (* sort *)


   BEGIN (* main program *)
     count := 0;
     read(inrow[count + 1]);
     WHILE NOT eof DO;
       BEGIN
         count := count + 1;
```

```
                                                   Page 2
                                                 07/22/82
                                                 00:33:33
                  NSC Starplex-II Pascal - version 2.06 - 7/82
            read(inrow[count + 1]);
          END; (* while *)
        IF count  >  0
         THEN
           BEGIN
             sort(inrow, count);
             FOR ix := 1 TO count DO
               write(inrow[ix])
           END
         ELSE write('no input')
     END.  (* shellsort *)


 procedure / function:     SORT


    ** 0001"    DB       01     ; level
    ** 0002"    CALL     RENGQQ
    ** 0005"    DW       0004, 0014     ; return displacement, frame length
L18:
    ** 0009"    CALL     LSAGQQ
    ** 000C"    <B>      0002
    ** 000D"    PUSH     HL
    ** 000E"    LD       HL,0100
    ** 0011"    PUSH     HL
    ** 0012"    LD       HL,E803
    ** 0015"    PUSH     HL
    ** 0016"    CALL     RCIEQQ
    ** 0019"    CALL     ASAGQQ
    ** 001C"    <B>      0008
L19:
I4:
    ** 001D"    CALL     LSAGQQ
    ** 0020"    <B>      0008
    ** 0021"    LD       DE,FEFF
    ** 0024"    LD       A,H
    ** 0025"    ADD      A,A
    ** 0026"    JP       C,I5
    ** 0029"    ADD      HL,DE
    ** 002A"    JP       NC,I5
L21:
    ** 002D"    LD       DE,0100
    ** 0030"    CALL     LSAGQQ
    ** 0033"    <B>      0008
    ** 0034"    CALL     SRDGQQ
    ** 0037"    PUSH     HL
    ** 0038"    LD       HL,0100
    ** 003B"    PUSH     HL
```

Example of a PASCAL Program (Cont'd)

```
    ** 003C"    LD      HL,E803
    ** 003F"    PUSH    HL
    ** 0040"    CALL    RCIEQQ
    ** 0043"    CALL    ASAGQQ
    ** 0046"    <B>     0008
L22:
I8:
L23:
    ** 0047"    LD      HL,0100
    ** 004A"    CALL    ASGGQQ
    ** 004D"    <B>     0010
L24:
    ** 004E"    CALL    LSBGQQ
    ** 0051"    <B>     0002
    ** 0052"    CALL    LSAGQQ
    ** 0055"    <B>     0008
    ** 0056"    CALL    SVBGQQ
    ** 0059"    CALL    ASAGQQ
    ** 005C"    <B>     0012
    ** 005D"    CALL    LSAGQQ
    ** 0060"    <B>     0012
    ** 0061"    LD      DE,FFFF
    ** 0064"    LD      A,H
    ** 0065"    ADD     A,A
    ** 0066"    JP      C,I10
    ** 0069"    ADD     HL,DE
    ** 006A"    JP      NC,I10
    ** 0070"    PUSH    HL
    ** 0071"    PUSH    HL
    ** 0072"    LD      HL,E803
    ** 0075"    PUSH    HL
    ** 0076"    CALL    RCIEQQ
    ** 0079"    CALL    ASAGQQ
    ** 007C"    <B>     000A
    ** 007D"    CALL    LSAGQQ
    ** 0080"    <B>     0012
    ** 0081"    PUSH    HL
    ** 0082"    LD      HL,0100
    ** 0085"    PUSH    HL
    ** 0086"    LD      HL,E803
    ** 0089"    PUSH    HL
    ** 008A"    CALL    RCIEQQ
I11:
L26:
    ** 008D"    CALL    LSBGQQ
    ** 0090"    <B>     0008
    ** 0091"    CALL    LSAGQQ
    ** 0094"    <B>     000A
    ** 0095"    CALL    AEBGQQ
    ** 0098"    PUSH    HL
    ** 0099"    LD      HL,0100
    ** 009C"    PUSH    HL
    ** 009D"    LD      HL,E803
    ** 00A0"    PUSH    HL
    ** 00A1"    CALL    RCIEQQ
    ** 00A4"    CALL    ASAGQQ
    ** 00A7"    <B>     000C
L27:
    ** 00A8"    CALL    LSAGQQ
    ** 00AB"    <B>     000C
```

Example of a PASCAL Program (Cont'd)

```
     ** 00AC"    ADD     HL,HL
     ** 00AD"    EX      DE,HL
     ** 00AE"    DEC     HL,DE
     ** 00AF"    DEC     HL,DE
     ** 00B0"    CALL    LSAGQQ
     ** 00B3"    <B>     0000
     ** 00B4"    CALL    OVBGQQ
     ** 00B7"    CALL    LSAGQQ
     ** 00BA"    <B>     000A
     ** 00BB"    ADD     HL,HL
     ** 00BC"    PUSH    DE
     ** 00BD"    EX      DE,HL
     ** 00BE"    DEC     HL,DE
     ** 00BF"    DEC     HL,DE
     ** 00C0"    CALL    LSAGQQ
     ** 00C3"    <B>     0000
     ** 00C4"    CALL    OVAGQQ
     ** 00C7"    POP     DE
     ** 00C8"    LD      A,D
     ** 00C9"    XOR     H
     ** 00CA"    LD      A,D
     ** 00CB"    JP      M,I4094
     ** 00CE"    LD      A,E
     ** 00CF"    SUB     L
     ** 00D0"    LD      A,D
     ** 00D1"    SBC     A,H
I4094:
     ** 00D2"    ADD     A,A
     ** 00D3"    JP      NC,I12
L30:
     ** 00D6"    CALL    LSAGQQ
     ** 00D9"    <B>     000A
     ** 00DB"    EX      DE,HL
     ** 00DC"    DEC     HL,DE
     ** 00DD"    DEC     HL,DE
     ** 00DE"    CALL    LSAGQQ
     ** 00E1"    <B>     0000
     ** 00E2"    CALL    OVAGQQ
     ** 00E5"    CALL    ASAGQQ
     ** 00E8"    <B>     000E
L31:
     ** 00E9"    CALL    LSAGQQ
     ** 00EC"    <B>     000C
     ** 00ED"    ADD     HL,HL
     ** 00EE"    EX      DE,HL
     ** 00EF"    DEC     HL,DE
     ** 00F0"    DEC     HL,DE
     ** 00F1"    CALL    LSAGQQ
     ** 00F4"    <B>     0000
     ** 00F5"    CALL    OVBGQQ
     ** 00F8"    CALL    LSAGQQ
     ** 00FB"    <B>     000A
     ** 00FC"    ADD     HL,HL
     ** 00FD"    PUSH    DE
     ** 00FE"    EX      DE,HL
     ** 00FF"    DEC     HL,DE
     ** 0100"    DEC     HL,DE
     ** 0101"    CALL    LSAGQQ
     ** 0104"    <B>     0000
     ** 0105"    ADD     HL,DE
```

Example of a PASCAL Program (Cont'd)

```
    ** 0106"    POP     DE
    ** 0107"    LD      (HL),E
    ** 0108"    INC     HL
    ** 0109"    LD      (HL),D
L32:
    ** 010A"    CALL    LSAGQQ
    ** 010D"    <B>     000C
    ** 010E"    ADD     HL,HL
    ** 010F"    EX      DE,HL
    ** 0110"    DEC     HL,DE
    ** 0111"    DEC     HL,DE
    ** 0112"    CALL    LSAGQQ
    ** 0115"    <B>     0000
    ** 0116"    ADD     HL,DE
    ** 0117"    CALL    LSBGQQ
    ** 011A"    <B>     000E
    ** 011B"    LD      (HL),E
    ** 011C"    INC     HL
    ** 011D"    LD      (HL),D
L33:
    ** 011E"    LD      HL,0000
    ** 0121"    CALL    ASGGQQ
    ** 0124"    <B>     0010
L34:
I12:
L35:
    ** 0125"    CALL    LSBGQQ
    ** 0128"    <B>     0012
    ** 0129"    CALL    LSAGQQ
    ** 012C"    <B>     000A
    ** 012D"    INC     HL
    ** 012E"    CALL    ASAGQQ
    ** 0131"    <B>     000A
    ** 0132"    DEC     HL,HL
    ** 0133"    LD      A,L
    ** 0134"    CP      E
    ** 0135"    JP      NZ,I11
    ** 0139"    CP      D
    ** 013A"    JP      NZ,I11
I10:
L36:
    ** 013D"    CALL    LSAGQQ
    ** 0140"    <B>     0010
    ** 0141"    LD      A,L
    ** 0142"    RRA
    ** 0143"    JP      NC,I8
L37:
    ** 0146"    JP      I4
I5:
L38:
I3:
    ** 0149"    CALL    PRAGQQ
    ** 014C"    DB      04
    ** 014D"    DB      00
```

```
procedure / function:    SHELLSOR


    ** 014E"    DB       00      ;level
    ** 014F"    CALL     RENGQQ
    ** 0152"    DW       0000, 0006      ; return displacement, frame length
    ** 0156"    CALL     INIFQQ
L41:
    ** 0159"    LD       HL,0000
    ** 015C"    LD       (COUNT),HL
L42:
    ** 015F"    LD       HL,INPFQQ
    ** 0162"    PUSH     HL
    ** 0163"    LD       HL,(COUNT)
    ** 0166"    ADD      HL,HL
    ** 0167"    EX       DE,HL
    ** 0168"    LD       HL,INROW
    ** 016B"    ADD      HL,DE
    ** 016C"    PUSH     HL
    ** 016D"    LD       HL,0180
    ** 0170"    PUSH     HL
    ** 0171"    LD       HL,FF7F
    ** 0174"    PUSH     HL
    ** 0175"    CALL     RTIFQQ
L43:
I14:
    ** 0178"    LD       HL,INPFQQ
    ** 017B"    PUSH     HL
    ** 017C"    CALL     EOFFQQ
    ** 017F"    LD       A,L
    ** 0180"    RRA
    ** 0181"    JP       C,I15
    ** 0184"    JP       I14
I15:
L45:
    ** 0187"    LD       HL,(COUNT)
    ** 018A"    CALL     INDGQQ
    ** 018D"    DB       01
    ** 018E"    PUSH     HL
    ** 018F"    LD       HL,0000
    ** 0192"    PUSH     HL
    ** 0193"    LD       HL,E803
    ** 0196"    PUSH     HL
    ** 0197"    CALL     RCIEQQ
    ** 019A"    LD       (COUNT),HL
L46:
    ** 019D"    LD       HL,INPFQQ
    ** 01A0"    PUSH     HL
    ** 01A1"    LD       HL,(COUNT)
    ** 01A4"    ADD      HL,HL
    ** 01A5"    EX       DE,HL
    ** 01A6"    LD       HL,INROW
    ** 01A9"    ADD      HL,DE
    ** 01AA"    PUSH     HL
    ** 01AB"    LD       HL,0180
    ** 01AE"    PUSH     HL
    ** 01AF"    LD       HL,FF7F
    ** 01B2"    PUSH     HL
    ** 01B3"    CALL     RTIFQQ
```

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Example of a PASCAL Program (Cont'd)

```
L48:
    ** 01B6"    LD      HL,(COUNT)
    ** 01B9"    LD      DE,FFFF
    ** 01BD"    ADD     A,A
    ** 01BE"    JP      C,I16
    ** 01C1"    ADD     HL,DE
    ** 01C2"    JP      NC,I16
L51:
    ** 01C5"    LD      HL,INROW
    ** 01C8"    PUSH    HL
    ** 01C9"    LD      HL,(COUNT)
    ** 01CC"    PUSH    HL
    ** 01CD"    LD      HL,0100
    ** 01D0"    PUSH    HL
    ** 01D1"    LD      HL,E803
    ** 01D4"    PUSH    HL
    ** 01D5"    CALL    RCIEQQ
    ** 01D8"    PUSH    HL
    ** 01D9"    CALL    SORT
L52:
    ** 01DC"    LD      HL,(COUNT)
    ** 01DF"    CALL    ASAGQQ
    ** 01E2"    <B>     0004
    ** 01E3"    CALL    LSAGQQ
    ** 01E6"    <B>     0004
    ** 01E7"    LD      DE,FFFF
    ** 01EA"    LD      A,H
    ** 01EB"    ADD     A,A
    ** 01EC"    JP      C,I18
    ** 01EF"    ADD     HL,DE
    ** 01F0"    JP      NC,I18
    ** 01F3"    LD      HL, 0100
    ** 01F6"    PUSH    HL
    ** 01F7"    PUSH    HL
    ** 01F8"    LD      HL,E803
    ** 01FB"    PUSH    HL
    ** 01FC"    CALL    RCIEQQ
    ** 01FF"    LD      (IX),HL
    ** 0202"    CALL    LSAGQQ
    ** 0205"    <B>     0004
    ** 0206"    PUSH    HL
    ** 0207"    LD      HL,0100
    ** 020A"    PUSH    HL
    ** 020B"    LD      HL,E803
    ** 020E"    PUSH    HL
    ** 020F"    CALL    RCIEQQ
I19:
L53:
    ** 0212"    LD      HL,OUTFQQ
    ** 0215"    PUSH    HL
    ** 0216"    LD      HL,(IX)
    ** 0219"    ADD     HL,HL
    ** 021A"    EX      DE,HL
    ** 021B"    LD      HL,INROW+FFFE
    ** 021E"    CALL    OVAGQQ
    ** 0221"    PUSH    HL
    ** 0222"    LD      HL,FF7F
    ** 0225"    PUSH    HL
    ** 0226"    PUSH    HL
    ** 0227"    CALL    WTIFQQ
```

Example of a PASCAL Program (Cont'd)

```
     ** 022A"    CALL    LSBGQQ
     ** 022D"    <B>     0004
     ** 022E"    LD      HL,(IX)
     ** 0231"    INC     HL
     ** 0232"    LD      (IX),HL
     ** 0235"    DEC     HL,HL
     ** 0236"    LD      A,L
     ** 0237"    CP      E
     ** 023B"    LD      A,H
     ** 023C"    CP      D
     ** 023D"    JP      NZ,I19
I18:
     ** 0240"    JP      I20
I16:
L55:
     ** 0243"    LD      HL,OUTFQQ
     ** 0246"    PUSH    HL
     ** 0247"    LD      HL,0800
     ** 024A"    PUSH    HL
     ** 024B"    LD      HL,<const>      ;offset = 2
     ** 024E"    PUSH    HL
     ** 024F"    LD      HL,FF7F
     ** 0252"    PUSH    HL
     ** 0253"    PUSH    HL
     ** 0254"    CALL    WTSFQQ
I20:
I13:
     ** 0257"    CALL    PRAGQQ
     ** 025A"    DB      00
     ** 025B"    DB      00


Rom size: 614 decimal
Ram size: 2006 decimal
```

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Prerequisites

Any STARPLEX II Development System with Rev F operating system or later.

Order Information

SFW-90-A300	PASCAL compiler to generate 8080/8085 linkable object code module(s) on STARPLEX II Development Systems.
SFW-90-A320	PASCAL compiler to generate NSC800/Z80 linkable object code module(s) on STARPLEX II Development Systems.

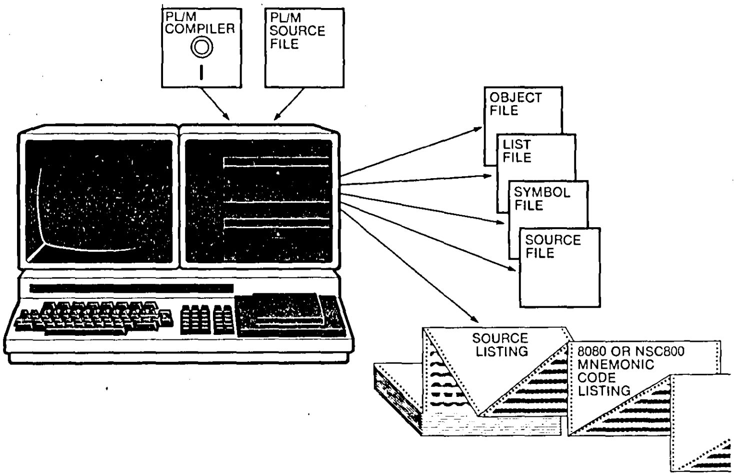
Documentation

420306680-001	STARPLEX II PASCAL Compiler Software Reference Manual (Included with SFW-90-A300 and SFW-90-A320)

National Semiconductor

PLM80

PL/M High Level Language Compiler for STARPLEX™ Development Systems



- **Executes on all STARPLEX/ STARPLEX II™ Development Systems**
- **Code generation for 8080/8085 and NSC800™/Z80 microprocessors**
- **Relocatable and linkable object code output**
- **Reentrant procedures as specified by user**
- **Compatible with existing industry standard PL/M-80**
- **Hardware access via highlevel statements (interrupt systems, absolute addresses, and input/output ports)**

Product Description

PLM80 is a high level language compiler designed for STARPLEX and STARPLEX II Development Systems. Available in two versions, this highly efficient compiler generates relocatable object code for 8080/8085 and NSC800/Z80 microprocessors.

PL/M has proven to be one of the most popular, effective and powerful program development tools available. Programmer productivity and reliability are greatly improved because the programmer can concentrate on system development rather than all the details of assembly languages. Since PL/M uses data structures that are very close to typical microprocessor architectures, it allows for efficient use of the machine. PL/M programs are efficiently converted to assembly language instructions, thus requiring fewer statements. Software development and maintenance costs are significantly reduced.

Free form PL/M source programs are efficiently and effectively converted into 8080/8085 or NSC800/Z80 assembly language instructions. A given program, when written in PL/M, requires fewer statements than would the equivalent program written in assembly language. Thus, software development and maintenance costs are significantly reduced due to the problem oriented structure that results naturally from the use of PL/M. User programming conventions and structured programming techniques are easily accommodated by the free form source statements of PL/M.

Functional Description

The PLM80 Compiler is a STARPLEX System program which accepts STARPLEX PLM80 language source modules and produced linkable object modules. Object modules may be linked to form executable PLM80 programs. The PLM80 compiler is also designed to accept programs written in the industry standard PL/M programming language.

The STARPLEX PLM80 compiler invocation is similar to that of other STARPLEX software. The 8080 version of the compiler in particular has all the features of the existing industry standard PL/M-80

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compiler. In many cases, no changes to existing PL/M-80 programs are required. However, STARPLEX PLM80 has a number of superior enhancements which may be incorporated into existing PL/M-80 programs to make it faster, smaller, and easier to debug. What modification is required can be done very easily.

Compilation is one step in the formation of an executable PLM80 program. The formation of a complete program involves the following steps:

- Writing the PLM80 "Source Modules" using the TEXT EDITOR.
- Compiling the source files to produce "Object Modules."
- Linking the object modules to create an executable PLM80 "Load Module."

When the source module(s) have been created using the TEXT EDITOR for compilation, choose the correct PLM80 diskette for the type of compilation desired. The 8080 version may be used for programs to be executed on 8080 and 8085 based systems. The NSC800 version may be used for NSC800 or Z80 based systems.

Enhancements

Lexical Extensions

PLM80 will allow the underscore character "_" in identifiers and in numeric constants, to aid legibility. For example, NAME_TABLE or 1100_0111B. Unlike the industry standard PL/M "$", which PLM80 also will accept, the underscore is a significant character in identifiers; thus, A_TO_M is a distinct identifier from AT_OM and from ATOM.

PLM80 will accept the ASCII form-feed character as lexically equivalent to a blank; the form-feed, like the EJECT compiler control, will cause a page eject in the listing file.

Explicit Locator References

In the industry standard PL/M, each based variable is associated with a unique pointer. The pointer is specified in the based declaration, and does not appear explicitly in references to the based variable.

Declare Statement Syntax

The industry standard PL/M requires attributes to appear in a specified order within a declaration. This restriction has been relaxed in PLM80.

Declaration of Arrays

The keyword ARRAY has been added for optional use in dimension-specifications.

The industry standard syntax for based array declarations is misleading because the dimension-specifier appears to be "attached" to the wrong variable:

```
DECLARE B BASED P(100) BYTE;
```

creates a 100-byte array b, based on a scalar pointer P. PLM80 will provide a number of superior alternative forms, e.g.,

```
DECLARE B(100) BYTE BASED P;
DECLARE B BASED P ARRAY(100) BYTE:
```

The second of these forms permits the industry standard form to be modified easily, the only difference is the addition of the keyword "ARRAY". It also accepts the standard form without the usage of "ARRAY".

Empty Blocks and Procedures

PLM80 will accept a block or procedure that contains no executable statements. This is not permitted by the industry standard.

Do-Case Extensions

PLM80 will accept case-selectors in the range of a do-case statement, thus permitting the programmer to create sparsely populated case constructs without sacrificing efficiency. Multiple specifiers will be permitted on a single statement, so the programmer need not write duplicate code.

PLM80 will accept an otherwise-clause in the range of a do-case statement. This makes it unnecessary to write out the action for every case if most of them are identical.

PLM80 will do range checking in the case construct. Unspecified or out-of-range cases will cause a jump to the statement following the do-case-block.

Example: The following code executes special statements if I is 6, 28, 496 or 8128. If I has any other value, the statement in the otherwise-clause is executed.

```
DO CASE I;
   6:
  28: DO;          /*  This entire do-block is    */
       ...         /*     executed if I = 6 or 28.  */
      END;
 8128: ...         /*  This statement is executed */
                   /*     if I = 8128.            */
  496: ...         /*  This statement is executed */
                   /*     if I = 496.             */
  OTHERWISE...     /*  This statement is executed */
                   /*     if I has any other value. */
END;
```

Iterative DO

In the industry standard, the expressions in "TO" and "BY" options in an iterative do-statement are evaluated each time the loop is executed. Worse, the time of evaluation depends upon the datatype of the index variable. PLM80 adopts the convention that these expressions are evaluated once, prior to entry to the loop. The values calculated at that time will be preserved and reused. This makes for faster running time.

User Interface

Listings

The PLM80 compiler can provide, upon request, source and object listings. Diagnostics will be provided, regardless of list options.

Source listings will include statement numbers, block nesting depth, diagnostics, a list of the options present for the compilation, and statistics (e.g., resources used) for the compilation.

Object listings will show object code (pseudo-assembly language and actual machine code) and approximate statement numbers.

Compile-Time Diagnostics

For syntax errors, the diagnostic message will appear in the souice listing immediately after the point at which the error was recognized. For example:

```
LINE STMT LEVEL .... + ....1.... + ....2.... + ....3.... + ....4.... + ....5.... +
 13    9    3              z = x + * x;
****  ERROR 21 **** Stmt 9 — near '*' — Syntax error; skipping input to ";"
```

At the end of the source listing for a module, the compiler will list all other diagnostic messages for that module, sorted by statement number. Each message will clear and concise, and will describe the error in detail. For example:

```
****  ERROR 48 **** Stmt  8 — Missing data type attribute
****  ERROR 43 **** Stmt 11 — Undeclared identifier
****  ERROR 54 **** Stmt 13 — Reference to member of undeclared
                              structure
```

Code Generation and Optimization

The PLM80 compiler handles: local optimizations, basic block optimization, efficient register allocation, special casing for common constructs, some strength reduction, removal of dead code and of branch-around-branch. This, in effect, produces smaller, faster and more efficient object code than the industry standard PL/M compiler.

Run-Time Support

The run-time support package contains those built-in procedures that are not compiled as in-line code, procedures for the arithmetic operations not performed in-line, and stack management.

Example PLM80 Program

```
STARPLEX PL/M-80 Rev A-810428   MODULE:SEARCH_MODULE
OPTIONS: FDS1:EXPROG LIST CODE
LINE STMT  LEVEL .... + ....1.... + ....2.... + ....3.... + ....4.... + ....5.... + ....6.... + ....7.... + ....8.... +
  1    1    0    SEARCH_MODULE:
  2                 D O ; /* This module contains a typed procedure named SEARCH. SEARCH *
  3                        * searches the based array BUFFER for the first occurrence of the strind *
  4                        * contained in the based array WORD. If the strind is found, SEARCH *
  5                        * returns the subscript value of the element of BUFFER containing the *
  6                        * first character. Otherwise, SEARCH returns a value greater than the *
  7                        * length of the buffer.                                               */

  9    2    2       SEARCH: PROCEDURE   (BUF_PTR,LENGTH,WORD_,PTR,WORD_LENGTH) ADDRESS PUBLIC;
 10    3    2          DECLARE          (BUF_PTR,LENGTH,WORD_PTR,WORD_LENGTH) ADDRESS,
 11                                     BUFFER BASED BUF_PTR ARRAY(1) BYTE,
 12                                     WORD BASED WORD_PTR ARRAY(1) BYTE,
 13                                     FIRST_CHAR ADDRESS,
 14                                     (I, K) ADDRESS,
 15                                     FOUND BYTE,
 16                                     TRUE LITERALLY '0FFH',
 17                                     FALSE LITERALLY '00H';

 20    4    2          SET_FIRST_CHAR:
 21                      DO FIRST_CHAR = 0 TO LENGTH - 1;
 22    5    3              I = FIRST_CHAR;
 23    6    3              K = 0;
 24    7    3              FOUND = TRUE;

 26    8    3              COMPARE:
 27                          DO WHILE (FOUND = TRUE) AND (K<WORD_LENGTH);
 28    9    5                  IF BUFFER (I) = WORD (K) THEN DO;
 29   11    5                     I = I + 1;
 30   12    5                     K = K + 1;
 31   13    4                   END;
 32   14    4                  ELSE FOUND = FALSE;
 33   15    3              END COMPARE;
 34   16    3          IF FOUND = TRUE THEN RETURN FIRST_CHAR;
 35   18    2          END SET_FIRST_CHAR;

 37   19    2          RETURN LENGTH + 1;

 39   20    1       END SEARCH;
 40   21    0    END SEARCH_MODULE
```

```
00A2'                       ;>>>> STATEMENT 2
00A2'     EB                XCHG
00A3'     22 0006"          SHLD      WORD_LENGTH
00A6'     69                MOV       L,C
00A7'     60                MOV       H,B
00A8'     22 0004"          SHLD      WORD_PTR
00AB'     D1                POP       D
00AC'     E1                POP       H
00AD'     22 0002"          SHLD      LENGTH
00B0'     E1                POP       H
00B1'     D5                PUSH      D
00B2'     22 0000"          SHLD      BUF_PTR
  .         .                 .         .
  .         .                 .         .
  .         .                 .         .
0087'                       ;>>>> STATEMENT 18

0087'                                           $00012:

                            CSEG
                            ORG       0081
0081'     0087'             DW        $00012
                            CSEG
                            ORG       $00012
0087'     2A 0008"          LHLD      $00002
008A'     23                INX       H
008B'     22 0008"          SHLD      $00002

008E'                                           $00003:

                            CSEG
                            ORG       0021
0021'     008E'             DW        $00003

                            CSEG
                            ORG       $00003
008E'     2A 000F"          LHLD      $00005
0091'     EB                XCHG
0092'     2A 0008"          LHLD      $00002
0095'     7B                MOV       A,E
0096'     95                SUB       L
0097'     7A                MOV       A,D
0098'     9C                SBB       H
0099'     D2 0023'          JNC       $00004

009C'                       ;>>>> STATEMENT 19
009C'     2A 0002"          LHLD      LENGTH
009F'     23                INX       H
00A0'     C9                RET

00A1'                       ;>>>> STATEMENT 20
00A1'     C9                RET

00A2'                       ;>>>> STATEMENT 21
00A2'     FB                EI
00A3'     76                HLT
MODULE STATISTICS:

    21 STATEMENTS PROCESSED
     0 DIAGNOSTIC(S) ISSUED

  CODE SEGMENT SIZE                181D (00B5H)
  DATA SEGMENT SIZE                 19D (0013H)
```

Prerequisites

Any STARPLEX /STARPLEX II Development System.

Order Information

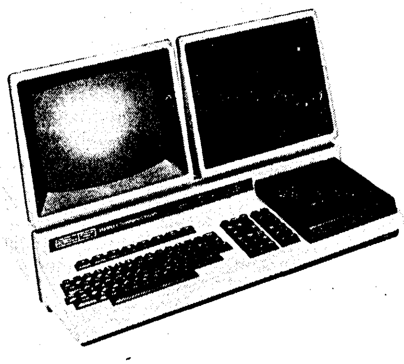
SFW-A50	PLM80, PL/M Compiler to generate 8080/8085 object program on STARPLEX Development System.
SFW-A60	PLM80, PL/M Compiler to generate NSC800/Z80 object program on STARPLEX Development System.
SFW-90-A50	PLM80, PL/M Compiler to generate 8080/8085 object program on STARPLEX II Development System.
SFW-90-A60	PLM80, PL/M Compiler to generate NSC800/Z80 object program on STARPLEX II Development System.

Documentation

420306371-001	STARPLEX PLM80 Compiler Software Reference Manual (Included with SFW-A50, SFW-A60, SFW-90-A50, SFW-90-A60)
420305789-001	8080/8085 Macroassembler Software User's Manual
420306198-001	NSC800 Macroassembler Software User's Manual

National Semiconductor

STARPLEX II™ Development System



■ **A Complete Development System**

- Dual CPU microprocessor-based system in master/slave configuration
  - 128K bytes of Random Access Memory
  - Dual floppy disk drives
  - Video monitor and keyboard controller
  - Two RS232C interfaces
  - Integral CRT keyboard with eight upper/lower case for a total of sixteen user definable keys
  - PROM programmer interface
- Software
  - Disk Operating System
  - Resident Debugger
  - Text Editor
  - Macro Assembler
  - On-board ROM and RAM diagnostics
  - I/O Spooling
  - FORTRAN
  - BASIC
- Options
  - In-System Emulator (ISE™ packages for NSC800™, INS8048 family, 8085 and Z80 microprocessor devices
  - In-System Emulator package for COP400 microcontroller devices
  - PL/M for 8080/8085, PL/M for NSC800/Z80
  - PASCAL compiler for 8080/8085, PASCAL compiler for NSC800/Z80
  - Optional double-sided/double-density disk drives with 2 megabytes of memory expandable to 4 megabytes
  - Cross assemblers (Included with the emulator packages)
  - STARLINK — Interface to Intellec Development System
  - PAL /PROM programmer personality modules

■ **Field-Upgradable from STARPLEX™ 80/41, 80/51 or 80/61 Systems**

- Upgrade kit includes:
  - Z80A Master CPU Board
  - Z80A Slave CPU Board with 64K bytes of RAM
  - Internal RS232C cable and connector
  - Keyboard with user-definable keys
  - Disk-Based Operating System for STARPLEX II

■ **Easy to Use**

- Prompting menus guide operator entries
  - English language explanation of user errors
  - Direct system function keys to PAUSE/CONTINUE/ABORT/DEBUG
  - HELP key for online user assistance
  - Single stroke CRT edit keys

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Product Overview

The STARPLEX II Development System is a general-purpose microcomputer and microprocessor development system. New levels of operating simplicity have been designed into the STARPLEX II system to significantly reduce the amount of time spent on product development. By getting the user into actual application work sooner and with fewer mistakes, the STARPLEX II system allows the user to take full advantage of time spent at the console.

A Complete System

The STARPLEX II design combines all the components required for the entire development task in one complete system. The STARPLEX II package includes a Z80A-based system controller board, a Z80A-based user processor/memory board with 64K bytes of RAM, 64K bytes of system RAM, 1M byte of disk storage controlled by a floppy disk controller, a video monitor and keyboard. The standard STARPLEX II software package includes a disk operating system, Z80 assembler, debugger, editor, linker, loader, FORTRAN, BASIC, on-board ROM diagnostics and utilities. Options available are: in-system emulation packages for real-time debugging of customized hardware and software prototype systems, PAL/PROM programmer personality modules for verifying, copying and programming PROMs or PALs, STARLINK for transferring files between STARPLEX II and Intellec Development System, and cross assemblers.

Easy to Use

The STARPLEX Systems reduce the time a user must spend at a terminal by making many complex functions accessible through single easy keystrokes. System commands are initiated by clearly marked function keys which invoke prompting menus to guide the user through each task. These function keys eliminate the need to memorize system commands and various command options. As a result, there is no need to refer to lengthy documentation, and errors or delays caused by incorrectly entered commands are eliminated. With the user-definable keys on the STARPLEX II System keyboard, the amount of time a user must spend at a terminal is further reduced. Eight function keys are provided with upper and lower case capability for a total of sixteen different keys which are user-definable. These keys may be utilized both in command mode (system) and by an application program running on the system. Thus, while system commands are initiated by clearly marked function keys, which invoke prompting menus to guide the user through each task, many non-system complex functions become accessible through these user-definable keys.

Recognizing that a great deal of the user's time is spent on creating and changing source code, the designers of the STARPLEX II system have devoted special attention to the text editing facility.

A set of special function keys direct the STARPLEX II Editor, allowing corrections to be made with single keystrokes. Also, the powerful "string mode" commands allow search and replacement of character strings as well as block moves. An entire file may be quickly and easily reviewed or altered. The number of mistakes is reduced because the data and changes are immediately displayed. Backup files are automatically created, protecting the user from accidental loss of data. Because the STARPLEX II system is easy to use, learning time is considerably shortened. A first-time user can be productive within a half hour. Also, as users make more efficient use of the system, machine availability is maximized.

Spooled Printer Capability

STARPLEX II supports spooled I/O to a user-selected print or another input or output device. Thus, printing long listings of files, compiler output and similar tasks may now be done at the same time as text editing, compiling, emulation, debugging, etc. The net result is a greater utilization of designer resources and subsequent reduction in program development time.

Resident System Debugger

The system debug utility is resident and always available to the user. This program does not occupy any user space in memory and can be invoked by a single keystroke. Unlike many other debug utilities, the STARPLEX II debugger does not have to be specified prior to program execution and may be invoked at any time.

Full Product Line Support

The STARPLEX II system supports development for the NSC800, NSC16000, INS8048 family (8048, 8049, 8050), Z80A, Z80B, 8085 microprocessors and COP400 microcontroller devices.

Functional Description

Hardware Modules

STARPLEX II components are packaged into modules which form a unified system when placed together. The modules are durable, with housings constructed of ⅛-inch aluminum and front panels of molded lexan foam.

STARPLEX II is designed for easy maintenance. Snap-down doors on the base module make it easy to access the card cages and circuit boards. Interconnecting cables between all modules and boards are routed to the rear of the system and covered by easily removable cable channels. Thus, cables are out of sight and protected from accidental damage. All cables, including the single AC power distribution system, are plug-detachable at both ends, making it easy to disconnect modules and reconfigure the system as the user chooses.

STARPLEX II Electronics

Five printed circuit boards make up the STARPLEX II electronics: the main Z80A-based CPU board, a Z80A-based user processor board which also has 64K bytes of memory, an 8080A-based video monitor/keyboard controller board, an 8080A-based floppy disk controller board and an additional 64K byte memory board.

The Z80A-based CPU board and user slave processor board are designed in a master/slave configuration to give the user processing power and speed that were unobtainable with previous development systems. The main CPU board with the floppy disk controller board and the video/keyboard controller board all have multi-master bus logic allowing them to share the system bus. The floppy disk controller board and the video/keyboard controller board communicate with the main CPU board and user processor board using Direct Memory Access and programmed I/O.

The optional printers and PAL/PROM programmer personality modules communicate with the main CPU/user processor boards through two programmable parallel I/O ports. A pair of RS232C ports on the main CPU board are available and permit both asynchronous and synchronous communications for use with options such as STARLINK.

Individual circuit boards are built to National's high manufacturing quality standards, utilizing techniques such as computer-aided layout and auto insertion. All boards are tested dynamically under system load conditions at elevated temperatures as part of a thorough factory burn-in.

Software

User programs are separated from those of the STARPLEX II operating system. This means that users have much more memory space available, and since the operating system resides in its own environment, accidental interface between user programs and the operating system is virtually eliminated.

The STARPLEX II software is completely thought out from a functional standpoint, carefully engineered to be easy to understand and use, and thoroughly integrated into the total system. Every aspect is designed to assist the user in rapidly developing microprocessor-based systems from the ground up.

The elegance of STARPLEX II software lies in its ability to make the complicated process of program development appear simple to the user.

OPERATING SYSTEM

The operating system provides system housekeeping functions and coordinates access to system resources. It includes a nucleus file manager, an I/O control system and a loader.

The nucleus of the STARPLEX II operating system controls and allocates system resources for the higher-level processes. The nucleus:

- Provides synchronization and communication facilities for higher-level asychronous processes.
- Services all hardware interrupts.
- Provides interval timer functions.
- Is completely device-independent.

File Manager

The file manager organizes, stores and retrieves data and programs stored on the diskettes.

- Maintains a directory.
- Allows multiple file attributes.
- Supports random access.

I/O Control System

The I/O control system is designed to eliminate the need for the user to understand the physical I/O characteristic of each individual device and presents a simplified, logical device-independent architecture.

- Provides overlapped I/O commands.
- Allows files to be accessed by name.
- Handles error conditions.
- Supports spooled I/O to a user-selected print or another input or output device.

Loader

The loader brings programs into main memory at specified locations.

- Provides "load and go" mode.
- Allows controlled load mode — starting address returned to calling program, useful for implementing overlay structures.

DEVELOPMENT SERVICES

The "development services" include a linker, a CRT-oriented editor, utilities, a resident debugger, optional PAL/PROM programmer support macro assemblers, BASIC and FORTRAN IV, optional PL/M for NSC800/Z80 or 8080/8085, and optional PASCAL for NSC800/Z80 or 8080/8085.

Linker

The linker combines relocatable object modules created by the assemblers or compilers into an executable run time module.

- Assigns absolute addresses to load modules.
- Produces a memory map of linked components.
- Searches system and user libraries for unresolved external references.

Editor

The STARPLEX II editor is an easy-to-use CRT-oriented text editor.

- String search and replace.
- Forward and backward paging.
- Block moves.
- Automatic source file backup.
- Traps illegal commands.

Utilities

General utilities provide routine maintenance functions.

- Transfer data files between devices.
- Obtain diskette directory listings.
- Format diskettes.

- Modify file attributes.
- Rename files.
- Print screen.

Debugger

The system debug utility is resident and always available to the user. The debugger does not occupy any user space in memory and may be invoked by a single keystroke. The program debugger simplifies program checkout by allowing program execution to be monitored and altered.

- Allows single step control.
- Permits eight breakpoint assignments.
- Displays program counter and registers at breakpoints.
- Memory references are absolute or relative to one of the relocation registers.

PAL/PROM Programmer Support

The PAL/PROM programmer support software manages the optional PAL/PROM personality module functions.

- Allows PROM code to be listed, verified and copied.
- Data stored in a PROM can be transferred to or from another PROM, a diskette file, memory, the video monitor or keyboard.
- Allows for custom programming of programmable array logic devices (PAL).

Macro Assembler

Individual macro assemblers can assemble 8085, 8048, NSC800, or Z80 mnemonic code and allow operator definition of useful higher-level instructions called "Macros" which are then expanded into a sequence of machine-level instructions. (Macro assembler for NSC800/Z80 is included with the STARPLEX II system. All other cross assemblers are optional.)

- Generates absolute or relocatable object modules.
- Conditional assembly parameters.
- Allows external references.

FORTRAN IV

The FORTRAN IV compiler on the STARPLEX II system meets the ANSI X3.9-1966 standard and includes the following enhancements:

- PEEK and POKE — allow direct access to memory.
- Supports user-written I/O drivers.
- Random access disk I/O.
- Allows assembly language subroutine calls.

BASIC

The STARPLEX II BASIC compiler/interpreter conforms to the Dartmouth-defined BASIC with extensions:

- PEEK and POKE — allow direct access to memory.
- Complete string operators.
- Multi-dimensional arrays.
- Extensive debugging and programming aids — trace, edit, direct mode, renumber.

PL/M for 8080/8085 and NSC800/Z80 (Optional)

PL/M is compatible with the industry standard PL/M, but offers many enhancements to improve program execution time and memory utilization.

- Available for 8080/8085 object code or NSC800/Z80 object code.
- Hardware access via high-level statements.
- Block structure facilitates structured programming techniques.
- Relocatable and linkable output object code.

PASCAL for 8080/8085 and NSC800/Z80 (Optional)

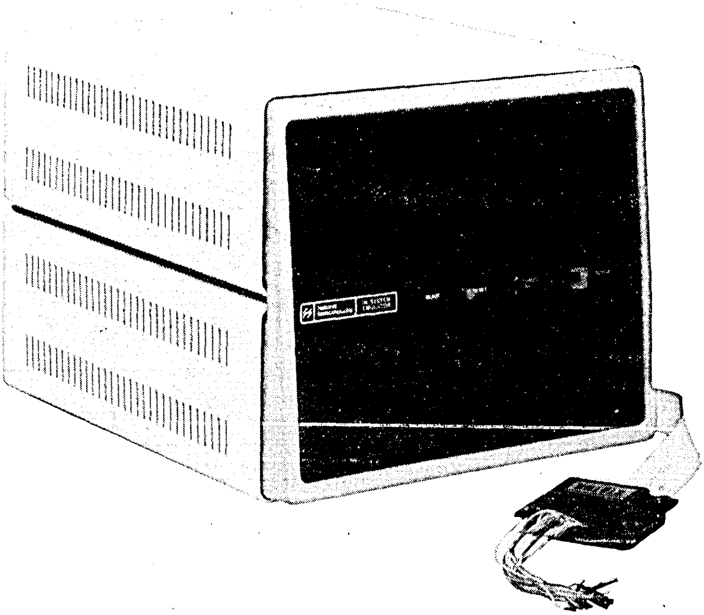
Specifications

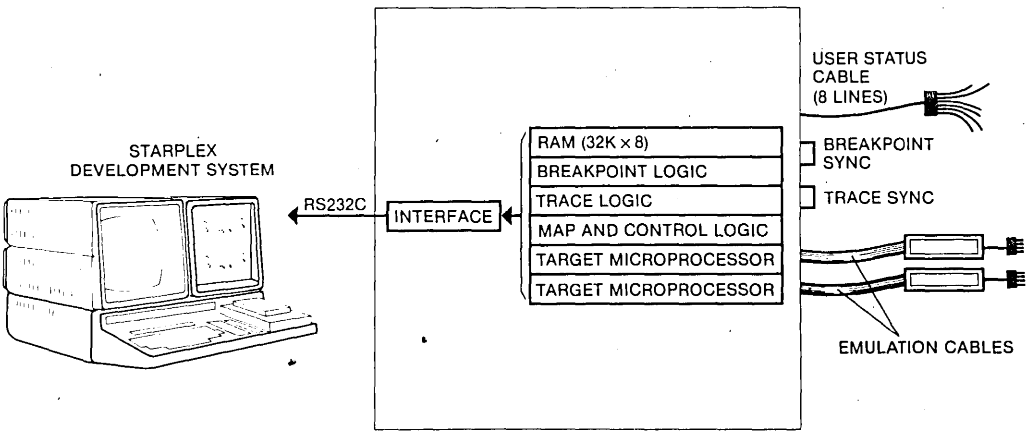
Processor Subsystem:	Z80A-based CPU board Z80A-based user processor/memory with 64K bytes RAM Video monitor/keyboard controller Double-density floppy disk controller Memory board with 64K bytes RAM (128K bytes total RAM)
Floppy Disk Subsystem:	
Configuration	Dual disk drives
Format	IBM-compatible, soft-sectored
Capacity	Double-density, single-sided 512K bytes/drives
Maximum Capacity	Expanded to 4 double-density, double-sided drives with 4 megabyte storage capacity
Keyboard Subsystem:	
System Function	8 single-stroke system control keys
ASCII	58 alphanumeric keys
Programmable	8 user-definable keys with upper/lower case
CRT Subsystem:	
Matrix	7×9 dot
Display Array	80 columns by 25 lines
Phosphor	P2 green
Other	Screen tilted 10° for comfortable viewing
Printers:	
Type	Impact
Speed	120 characters per second
Width	132 columns
Character Type	7×9 dot matrix
Power:	115 VAC, 60 Hz, 10 amps (max) or 230 VAC, 50 Hz, 5 amps (max)
Base Module	644 Watts
Floppy Disk Module	966 Watts
Impact Printers	360 Watts
Video Monitor	34 Watts

Physical:

	Base Module	Floppy Disk Module	Impact Printer	Video Monitor
Height	5.75 in. 14.6 cm	11.5 in. 29.2 cm	8 in. 20.3 cm	11.5 in. 2.92 cm
Width	26 in. 66 cm	13 in. 33 cm	24.5 in. 62.2 cm	13 in. 33 cm
Depth	26 in. 66 cm	19 in. 48.3 cm	18 in. 45.7 cm	19 in. 48.3 cm
Weight	68 lb. 30.8 kg	50 lb. 22.7 kg	60 lb. 27 kg	29 lb. 13.2 kg

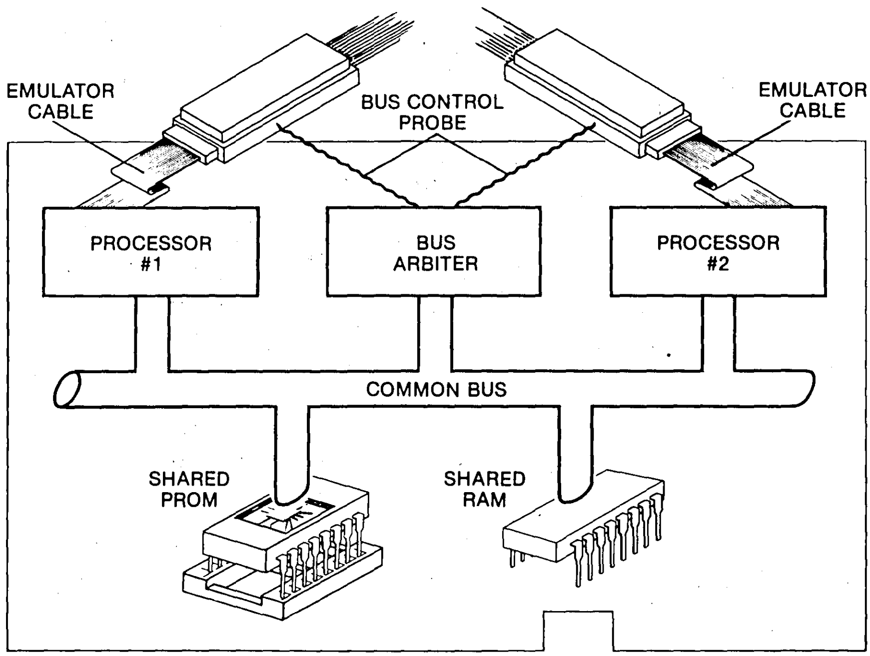
In-System Emulator Module



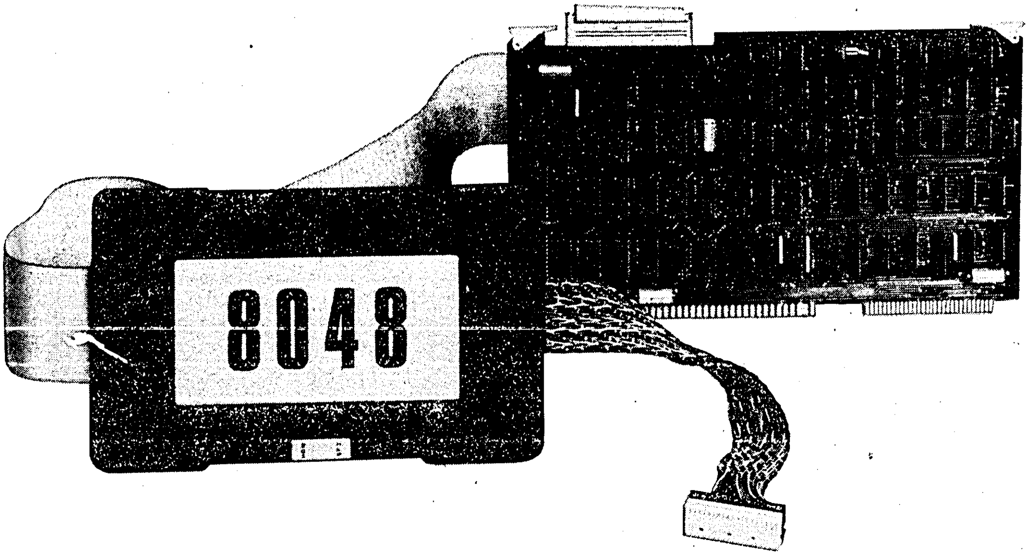


In-System Emulator System Configuration

Application Multiprocessor System Configuration



8048 Family Emulator Package



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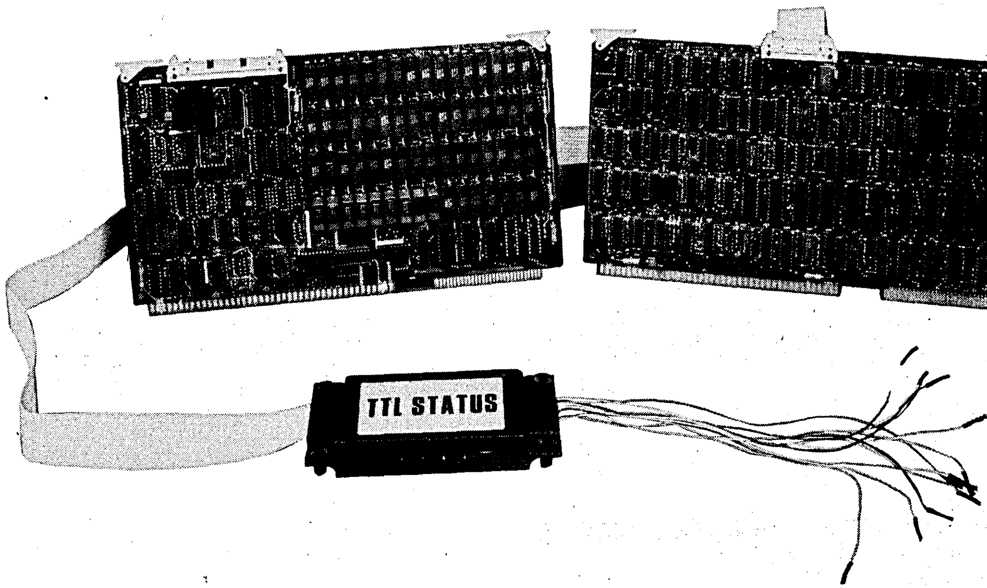
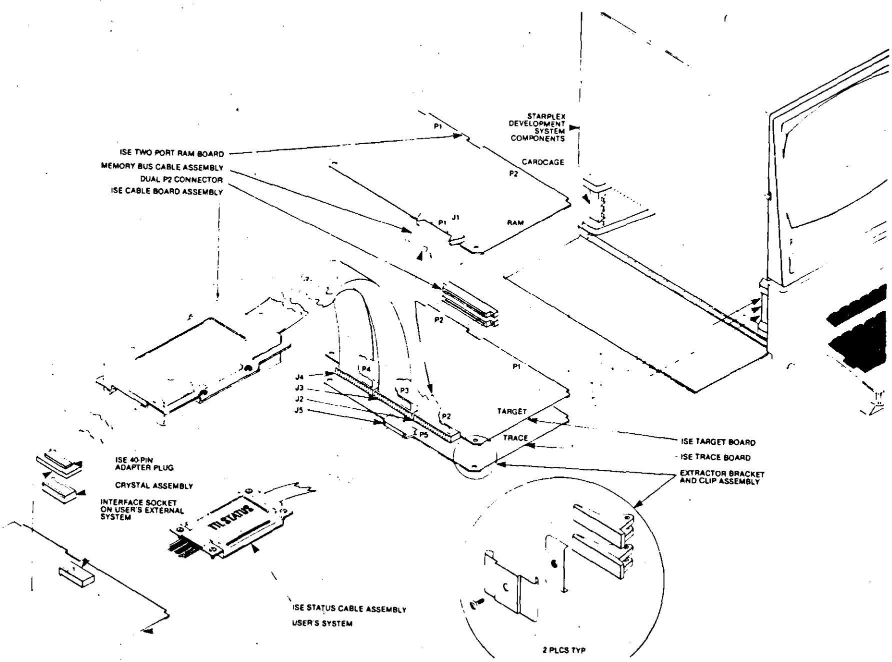
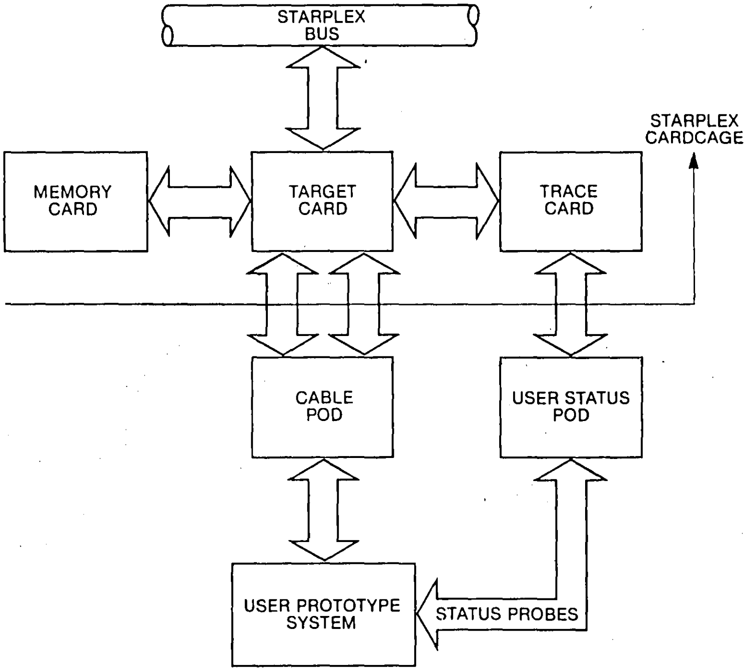
Integral In-System Emulator



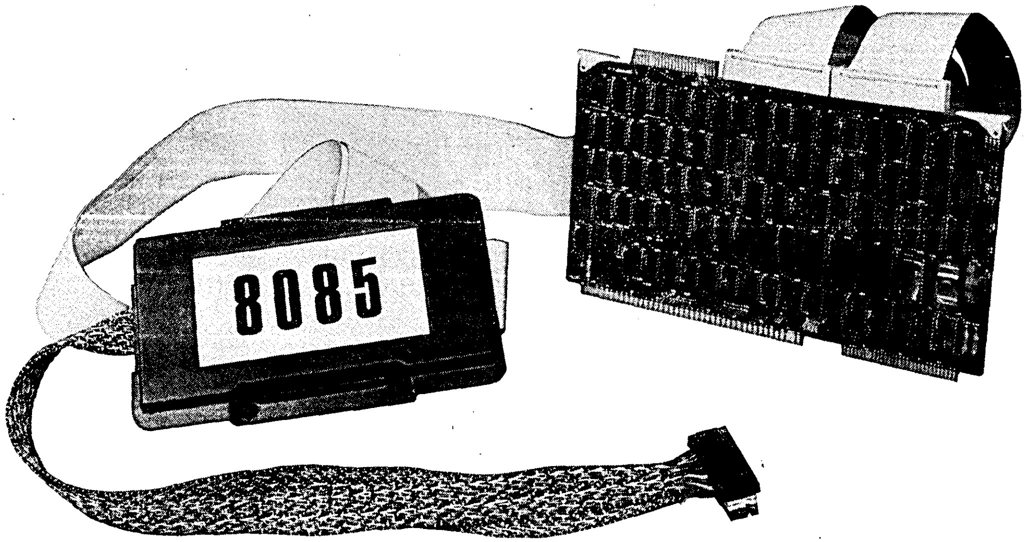
Integral ISE Components Installation



Integral ISE System Configuration (Total: 3 Boards and 2 Pods)



8085 Emulator Package



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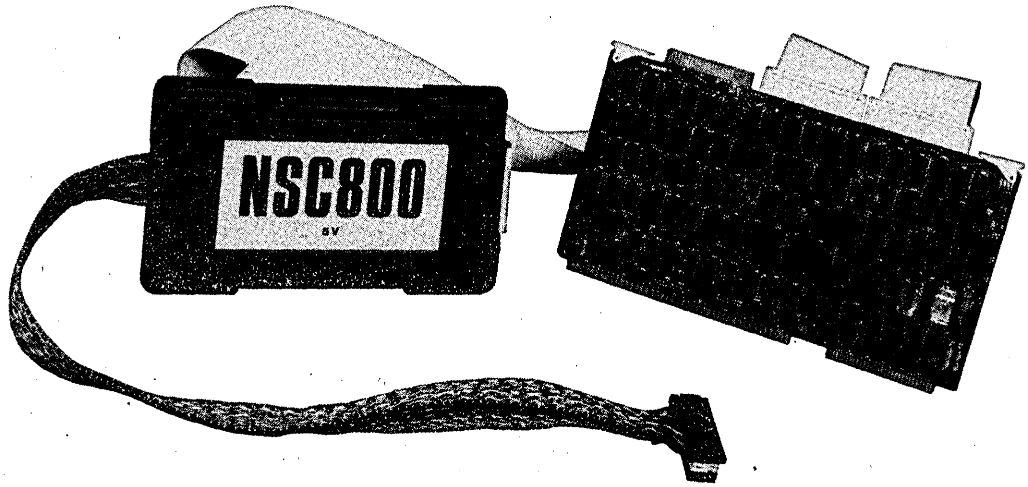
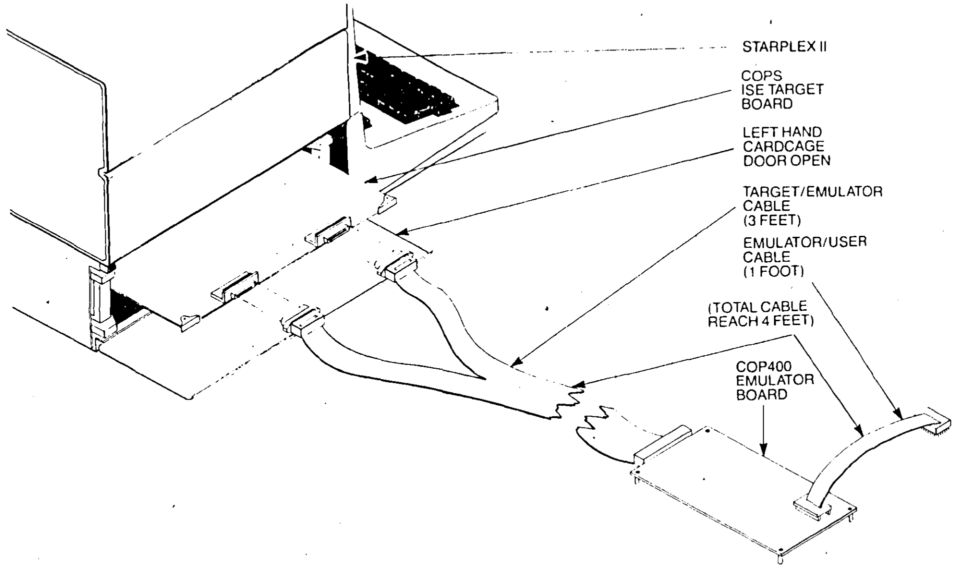
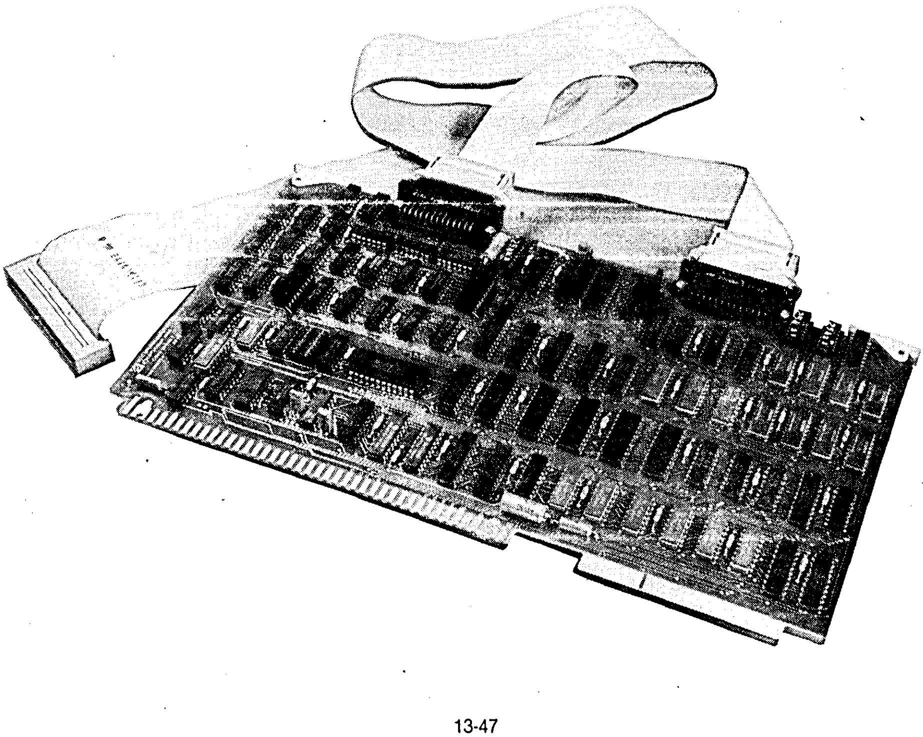
NSC800 Emulator Package



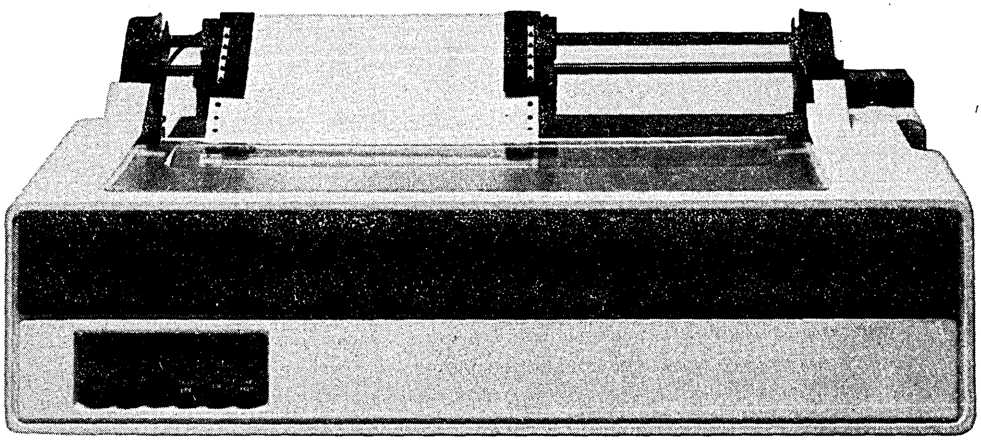
Installation of the COPS ISE Target Board and an Emulator Board



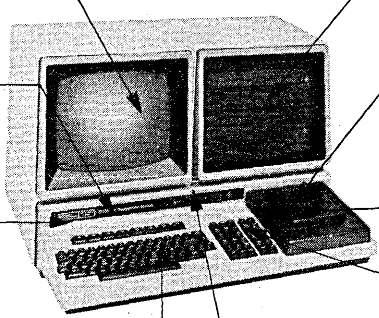
COPS™ In-System Emulator Package



Impact Printer



STARPLEX II Development System



Video Monitor Subsystem
Large screen — measures 12" diagonally
Legible characters — 7×9 dot matrix
24 lines × 80 characters
Soft green phosphor
Variable screen intensity
10° tilted screen for comfortable viewing
Extensive screen control; scrolling, blink, blank, inverse video or alternate characters

User Definable Function Keys
Eight function keys are provided with upper and lower case capability for a total of sixteen different keys which are user definable

Processors Subsystem
Z80-based CPU
Z80-based user processor/memory with 64K byte RAM
Floppy disk controller/formatter
64K byte RAM
Dual 4-slot chassis provides three expansion slots

Disk Subsystem
Dual standard floppy drives give 512K bytes per drive capacity
Uses IBM soft-sectored format
Expanadable to four drives (two million bytes)

PROM Programmer (Optional)
Plug in PROM personality modules — standard PRO-LOG compatible
Programs bipolar PROMs, 2708, 2716 EPROMs, PALs

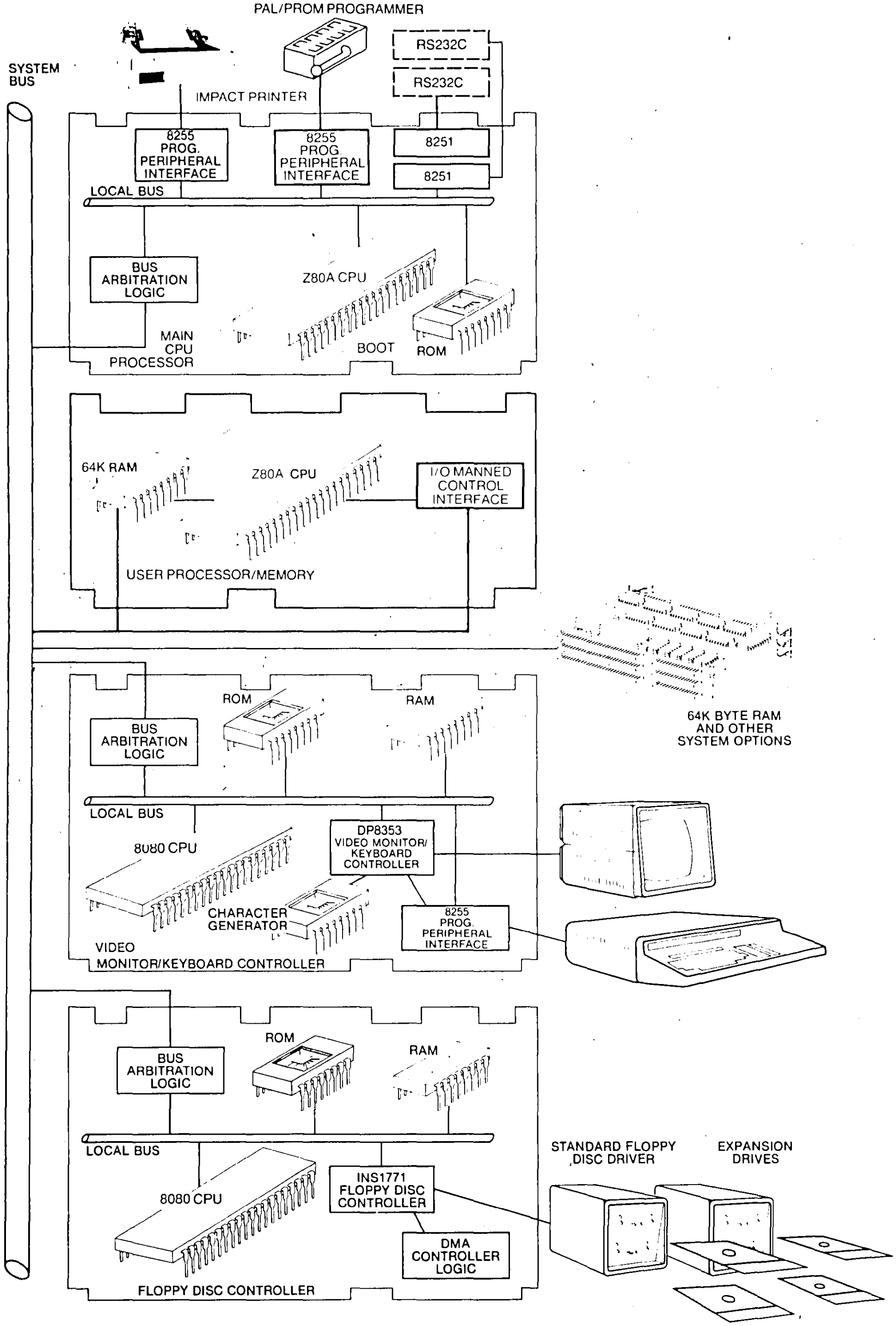
System Function Keypad
9 system control keys
Control program execution

Editor Keypad
5 cursor keys
13 special edit keys

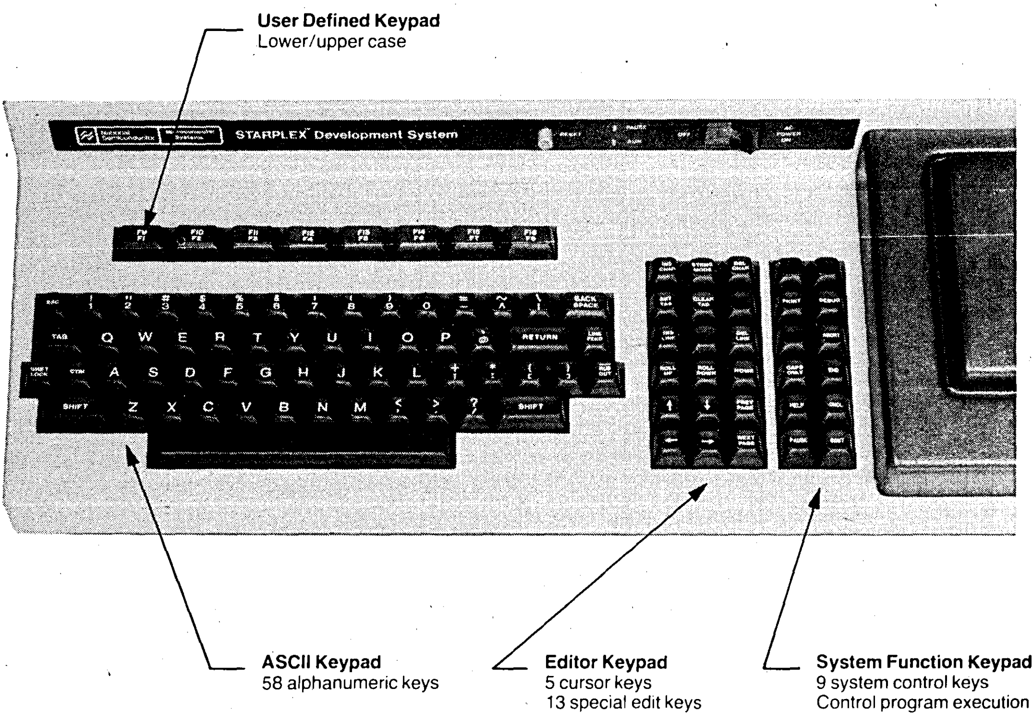
ASCII Keypad
58 alphanumeric keys

System Reset Boot Load Button
Powerful resident bootstrap has built-in micro-diagnostics to check all system facilities on initialization, then automatically switch out of user memory space

STARPLEX II Multiprocessor System



STARPLEX II Keyboard



Standard Configuration

IN THE STANDARD CONFIGURATION, STARPLEX II provides a fully functioning turnkey system including the following features:

- CPU Master
- CPU Slave
- Bootstrap and diagnostic utility
- Two RS232C serial I/O ports
- Real time clock/calendar
- 128K bytes of mappable RAM
- Keyboard base
- Video monitor with 7 × 9 dot matrix and 1920 character display
- Dual floppy disk subsystem with double-density (1 mb) or double-sided double-density (2 mb) disk drives
- Debugger for diagnosing program execution
- Additional utilities for system maintenance
- Expansion slots for Integral ISE™ capability
- BASIC interpreter
- FORTRAN compiler
- Modular construction for versatility in operation
- Expansion capabilities to meet your growing requirements
- Complete operating system including an input/output system with an independent interface to user tasks
- File manager for comprehensive data storage and retrieval file creation, protection, deletion and attribute assignment with use of unique keyboard utility keys
- Screen oriented text editor for creating and editing source statements
- Macro assembler for assembling Z80 mnemonics and user-defined macros
- Linker for linking independent program modules into executable files
- PROM programming capability including interface board and universal software with PAL support

Order Information

SPX-90/51	STARPLEX II Development System with 1 Megabyte Disk Storage (single-sided, double-density drives) (60 Hz)
SPX-90/61	STARPLEX II Development System with 2 Megabyte Disk Storage (double-sided, double-density drives) (60 Hz)

Options

SPM-90-A06-1	STARPLEX II Dual Single Sided, Disk Expansion
SPM-90-A06-2	STARPLEX II Dual Double Sided, Disk Expansion
SPM-90-A08	In-System Emulator Module
SPM-90-A09-2	8048 Emulator Package (includes upgrade kits that convert ISE 8048 to emulate 8049 and 8050)
SPM-90-A13	Integral In-System Emulator Package
SPM-90-A13-3	8085 Emulator Package
SPM-90-A13-4	NSC800 Emulator Package
SPM-90-A13-7	Z80 (4 MHz) Emulator Package
SPM-90-A15	COPS™ Emulator Package
SPM-90-A20	Z80 (6 MHz) Complete ISE Package
SPM-90-A55	Impact Printer
SFW-90-A50	PL/M Compiler for 8080/8085
SFW-90-A60	PL/M Compiler for NSC800/Z80
SFW-90-A200	CP/M Operating System Software Package
SFW-90-A300	PASCAL Compiler for 8080/8085
SFW-90-A320	PASCAL Compiler for NSC800/Z80

Note: To order 50 Hz add the letter "E" to the order.

Documentation

STARPLEX II Development System

420306465-001	STARPLEX II System Hardware Reference Manual
420306383-001	STARPLEX II System Software Reference Manual
420305788-001	STARPLEX II Macro Assembler Software User's Manual
420305790-001	STARPLEX II FORTRAN Compiler Software User's Manual
420305791-001	STARPLEX II BASIC Interpreter Software User's Manual
420305804-001	BLC-8222 Double-Density Floppy Disk Controller Hardware Reference Manual
420305587-001	BLC-8228/8229 Video Monitor/Keyboard Controller Hardware Reference Manual
420305529-001	BLC-032/048/064 32/48/64K RAM Board Hardware Reference Manual
420306183-001	Universal PAL/PROM Programmer User's Manual

STARPLEX II Development System Options

420305869-001	SPM-90-A08 In-System Emulator Reference Manual
420306065-001	SPM-90-A09-2 8048 ISE Target Board User's Manual
420306240-001	SPM-90-A13-3 8085 Integral ISE-User's Manual
420306241-001	SPM-90-A13-4 NSC800 Integral ISE User's Manual
420306692-001	SPM-90-A13-7, Z80 Integral ISE User's Manual
420306254-001	SPM-90-A15 COPS ISE User's Manual

STARPLEX II Development System Software

420306371-001	SFW-90-A50, SFW-90-A60 PLM80 Software Reference Manual
420306680-001	SFW-90-A300, SFW-90-A320 Pascal Compiler Reference Manual

Section 14

CMOS Industrial Microcomputer Boards

14

Introduction

Developing a board-level solution for applications in harsh industrial environments presents a number of challenges for systems designers. In such applications—which include pipeline monitoring and control, mining equipment monitoring and control, food processing, industrial motor control, robotics and process control—a uniform need exists for easily altered or expanded systems that are also impervious to wide temperature fluctuations, electrical noise, vibration, corrosion, washdowns, power failures, and so on.

POWER DISSIPATION

One of the first challenges a designer faces is power dissipation. High power dissipation creates the need for larger, more expensive enclosures, as well as the need for cooling fans, vents/filters, refrigeration systems (in some cases), and large power back-up systems.

Low power drain, on the other hand, means that boards can be inexpensively sealed-off in locations requiring intrinsically safe electronics, washdowns, or resistance to corrosion. Also, low power means increased reliability, portable battery back-up of volatile memory, and the overall reduction in system cost through the elimination of the extra equipment that is required when high power dissipation exists on the PC boards.

A typical CPU board for the MULTIBUS™ has a power dissipation of 20W and an equivalent CPU board for the STD BUS has a power dissipation of 7.5W, but the microCMOS technology that is used in National's SERIES/800 CMOS industrial microcomputer (CIM™) board family allows the power dissipation to be reduced to only 0.3W, with the CPU board still providing sufficient functionality for most applications.

What's more, the large power dissipation difference between NMOS and CMOS increases when a more complex system is considered. At the board level, for instance, CMOS ICs will dissipate 25 to 30 times less than the equivalent NMOS ICs for the same functionality (*Figure 14-1*).

NEW BUS REQUIRED

These new CIM boards needed a new bus. In designing this new bus, National realized it could take advantage of the CMOS bus already developed for the NSC800™ microcomputer and add features that would diminish the systems designer's involvement in putting a system together. What evolved was CIMBUS, a synchronous bus with 64 lines replicating about 30 of the functions of the NSC800's bus, while adding many useful timing and control signals.

In designing a bus for an industrial environment, the designer must take into account the need for an orderly shutdown of equipment in the event of system failure, since a disorderly shutdown could result in injuries or damage to equipment. CIMBUS, therefore, incorporates a system-level, fail-safe timer. This timer informs the rest of the system if the microcomputer hangs up or fails. The other boards will then be reset to a state that allows disengaging machinery in an orderly way.

TEMPERATURE EXTREMES

Using the new microCMOS products, National is able to design boards with an operating temperature range from −40°C to +85°C (typical NMOS boards can only operate from 0°C to 55°C). This more than doubles the operating temperature range.

UNINTERRUPTABLE POWER SUPPLY

The low power requirement of a CMOS industrial microcomputer board system allows National to easily provide an uninterruptable power supply. The heart of this power supply is a voltage regulator board (a DC/DC switching converter that allows the system to be powered by unregulated DC) and a battery charger board (to monitor the discharge rate and output voltage of an external battery and then provide either a fast or float charge). In conjunction with a 10V to 17V battery, these boards provide a portable, low-cost uninterruptable power supply that is simply plugged into the card cage. No additional equipment or hardware design is required by the user since the system is capable of full operation whether or not the primary power source (24 V_{DC}) is present.

MECHANICAL INTEGRITY

To provide for mechanical integrity, the pin-in-socket DIN 41612 connector is used. This provides an ideal mechanical complement to CMOS logic, where steady state currents on the order of μAs are driven through connector pins. These connectors are resistant to both vibration and corrosion.

The traditional approach has been to use the card-edge connector for all bus and I/O interfaces. This was an economical, but, unfortunately, an unreliable solution.

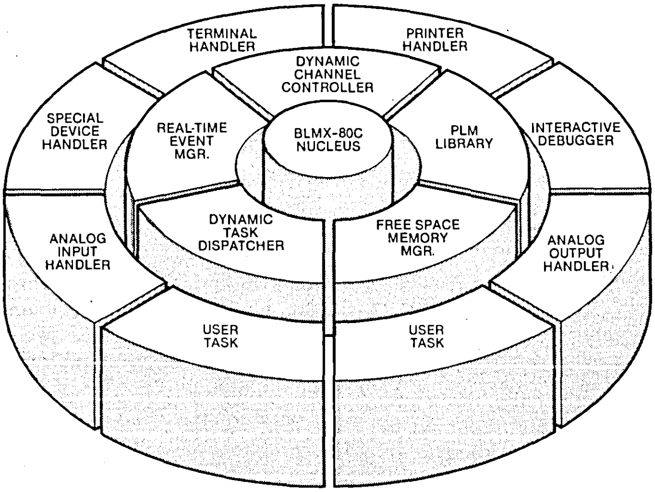
Parameter	MULTIBUS	STD BUS	CIMBUS™
Technology	NMOS	NMOS	microCMOS/CMOS
Temperature Range	0°C to 55°C (32°F to 131°F)	0°C to 55°C (32°F to 131°F)	−40°C to +85°C (−40°F to +185°F)
Board Size	6.75″ × 12.0″ (17.2 cm × 30.5 cm)	4.5″ × 6.5″ (11.4 cm × 16.5 cm)	3.9″ × 6.3″ (10 cm × 16 cm)
Supply Voltage	5 V_{DC}, ±12 V_{DC} (Regulated)	5 V_{DC}, ±12 V_{DC} (Regulated)	10 V_{DC} to 17 V_{DC} (Unregulated)
Power Dissipation	20W	7.5W	0.3W
Speed	4 MHz (Typ)	4 MHz (Typ)	4 MHz
Connector Type	Card-Edge	Card-Edge	Pin-in-Socket

FIGURE 14-1. Typical 8-Bit CPU Board NMOS to CMOS Comparison

National Semiconductor

BLMX-80C
Board-Level, Multitasking Executive for NSC800™-Based Systems

microCMOS



- **Configurability**
  - —Fully user configurable
  - —Menu selection procedure
  - —Hardware independent
- **Compatibility**
  - —NSC800, Z80®
  - —Bus-like structure
- **Reliability**
  - —Small, efficient nucleus
  - —Simple user interface
  - —Standard data structures
- **User-Oriented Support**
  - —Extensive I/O handlers
  - —Analog handlers
  - —Linkable interactive debugger
- **Easy-to-Use**
  - —Prompting menus guide system configuration
  - —Comprehensible system functions
  - —Functional similarity for internal and external calls
  - —Reconfigurable

Product Overview

The BLMX-80C software system is a real-time, multitasking executive, specifically designed for use with National Semiconductor Corporation's CMOS Industrial Microcomputer (CIM™) products, but is equally usable for any NSC800-based system. It has been optimized for real-time applications such as process control, manufacturing monitoring, and data acquisition systems. The BLMX-80C Executive is fully modular and can readily be configured to suit applications needs. It is completely hardware and location independent, thereby providing a fundamental base upon which users can build a wide range of applications systems. In addition, BLMX-80C provides a bus-like structure that helps to integrate software with its underlying hardware through predefined data structures and interconnect procedures. This concept of software-bus architecture ensures maximum quality of standardization for compatibility and future expandability.

The BLMX-80C nucleus requires only 512 bytes of RAM and 2K bytes of ROM. The system contains all major real-time functions including task scheduling, intertask communication and synchronization, interrupt handling and I/O control, as well as many optional features.

BLMX-80C provides support for all CIM CPU boards: CIM-802, CIM-802A, and CIM-804, as well as the CIM-201 Serial I/O Board and the CIM-411 Analog Input Board. Real-time modules include a handler for the System-Level Fail-Safe Timer and cold/warm start initialization. A linkable, interactive, system-level debugger is also supplied.

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Features

The BLMX-80C Board-Level, Multitasking Executive provides users of CIM products with simple and easy-to-use, yet comprehensive tools for creating a wide range of applications. The most notable features of BLMX-80C are:

Structured Environment — The BLMX-80C Executive and its associated modules support and encourage modular, structured programming, thus providing a consistent structure from application to application and allowing experience gained and software written on one system to be easily transferred to another. Frequently, entire programs may be used in multiple applications, *even if different CPU boards are involved.*

Hardware-Oriented Interface — The BLMX-80C Executive provides for an intertask and task/executive communications architecture that is similar to hardware communications. Instead of an array of "mailboxes" (or "message centers"), BLMX-80C incorporates channels. One merely communicates across a channel from his module to the desired destination. This interface is consistent throughout the range of facilities offered, thus reducing the number of concepts to be learned, providing greater control at the task level, and increasing the efficiency of the system and the programming effort.

Library Modules — The BLMX-80C Executive is constructed in a thoroughly modular manner with the full range of facilities being offered in multiple library modules, which allows easy selection of the exact facilities required.

Small Nucleus — The BLMX-80C nucleus was hand-coded in assembly language rather than being compiled from intermediate or high-level languages. The resulting product is therefore smaller and allows the incorporation of more features within the size generally accepted as optimum.

Priority-Oriented Scheduler — The BLMX-80C scheduler ensures that the highest priority task that is ready to execute is given control, which allows the system to be responsive to its external world. Dynamic reprioritization of tasks is supported for the most sophisticated of multitasking systems.

Real-Time Speed — Because BLMX-80C was hand-coded in assembly language, several speed advantages are realized. Task swapping, channel and message management, and I/O interfacing are executed much more quickly than could be expected of a system written in a higher level language.

Direct Interrupt Processing — The BLMX-80C architecture employs interrupt channels that allow device-specific interrupt handling routines to interface directly with the interrupt source. This accomplishes servicing of interrupts without the overhead of task swapping, yet allows the operating system to maintain the integrity of the system. Combining this interrupt service architecture with a device-efficient nucleus results in an operating system that better supports demanding, real-time applications.

Comprehensive I/O Support — The BLMX-80C libraries contain support for a wide variety of I/O boards within the CIM product line, thus simplifying the addition of peripherals to an application system. For applications requiring interfacing to unique devices, the architecture of BLMX-80C allows easy addition of user-written handlers.

User Configurability — BLMX-80C Executive-based applications may be configured from a wide range of facilities, selecting only those that meet the specific requirements of the application system. The resultant system contains only the modules necessary for its use, allowing the BLMX-80C Executive to fit a wide range of applications from small, special-purpose, dedicated applications to large, general-purpose systems.

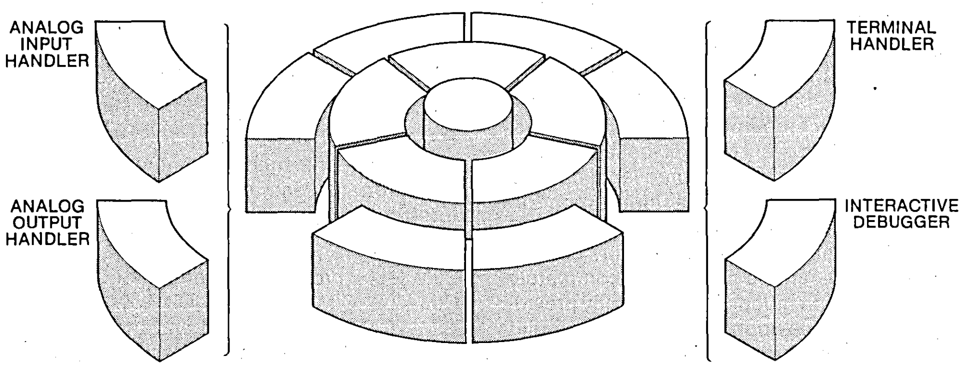


FIGURE 1. Configuration Flexibility Provides Application Freedom

The BLMX-80C Executive, and associated modules, allows the designer the freedom to choose from a wide range of CPU, expansion, and controller boards upon which his application may be built. It allows one to break the ties between the application and the hardware, and thereby gain application freedom and save software development costs.

Event-Driven — In the BLMX-80C Executive, each user task exists in its own "closed environment" — a virtual processor. Each virtual processor can synchronize with external/internal occurrences through events. BLMX-80C supports a wide variety of events, including synchronization with task activities, external device operations, and the real-time clock.

Free Space Manager — The BLMX-80C Executive has an integral free space manager. This feature not only reduces the amount of RAM required in an application system (potentially reduces board count), but also allows active modules more buffer area within any given space constraint.

Time-of-Day Clock — The BLMX-80C Executive has an integral system/time-of-day clock. Included is a real-time clock configurable to a resolution of 10ms. This negates the need to allocate the extra memory required for these features, which are necessary in most application systems.

Debugging Aids — The BLMX-80C Executive has a linkable, system-level, user-oriented, interactive software debugging aid. The debugger allows examination and modification of system message control blocks and execution breakpoints, automatic stack overflow monitoring, and numerous other features that result in simplified task debugging and faster application system development.

Hardware/Software Compatibility — The user of BLMX-80C is guaranteed that his CIM boards and his BLMX-80C device handlers will always be compatible. If changes are necessitated on any item supported by National Semiconductor Corporation, the BLMX-80C user is guaranteed that no compatibility problems will arise.

Facilities

The various facilities offered by the BLMX-80C Executive are provided as independent library modules, thus allowing simple inclusion or exclusion depending on the user's specific requirements. These facilities are described below.

Nucleus — The BLMX-80C nucleus provides real-time scheduling, interrupt handling, intertask communications, task control, free-space management, and time-of-day. The services offered are:
- Task message sending/receiving and synchronization
- External input/output and synchronization
- Task management
- Time control
- Creation and disposal of tasks during run time
- Extended free memory pool management (user space) with granularity control for optimization

Terminal Handler — The BLMX-80C terminal handler provides a data path between a console device (CRT or TTY) and user tasks. The services offered include:
- Terminal input processing with echo capability
- Recognition of termination character
- Recognition of the editing control characters
- Terminal output processing

Analog Handlers — The BLMX-80C analog handler provides a convenient mechanism for obtaining and transmitting analog values between user tasks and the CIM-411 Analog Input Board. The analog handlers offer a full range of services that include:
- Sequential input function for analog input sampling
- Random sequence input function for sampling at user-specified sequence

Fail-Safe Timer Handler — The BLMX-80C System-Level Fail-Safe Timer Handler is implemented as an interrupt handler. It provides the retriggering required to maintain the fail-safe timer on the CIM CPU boards.

Table 1. BLMX-80C Memory Requirements

Module	Memory Requirements[1] (Bytes)					
	Nucleus					Terminal Handler
	Basic Kernel	Timer Manager Option	Dynamic Task Disp. Option	Dynamic Channel Option	Extended Mem. Mgr. Option	
PROM[2]	1574	532	53	80	180	835
RAM[3]	328	—	—	—	—	14

Module	Analog Input Handler	Analog Output Handler	Fail-Safe Timer Handler	Cold/Warm Start Initialization	Static Debugger	Dynamic Debugger
PROM[2]	66	42	50	276	6246	18842
RAM[3]	—	—	—	—	500	2344

Notes:
1. All figures are approximate. Modules whose final size is user-dependent have the minimum requirements listed.
2. Indicates amount of code which can be configured in PROM.
3. Does not include user-defined Message Control Blocks.

Cold/Warm Start Initialization Modules — The linkable BLMX-80C initialization routines provide application-independent initialization. The functions provided include:
— Determination whether a cold start or a restart (warm start) is needed
— System RAM test
— Programmable timer(s) reset
— CPU-dedicated I/O initialization
— Serial I/O UART initialization

The System Generation Process

The BLMX-80C system generation process is, for the most part, accomplished by running a program called SYSCON on a STARPLEX™ Development System. The user merely "fills out forms" presented on STARPLEX, answering questions concerning the CPU board, which library modules are required, location of handlers and user-generated tasks, and assignment of channels for communications between tasks and with the Executive. The resulting files are then merged into object form executable on the application system. The system may then be debugged using the NSC800 In-System Emulator (ISE™) from National Semiconductor Corporation, or the BLMX-80C interactive debugger. The final application system code is then available for PROM programming.

Supported Hardware

CIM-800 Series CPU Boards
CIM-201 Serial I/O Board
CIM-411 Analog Input Board

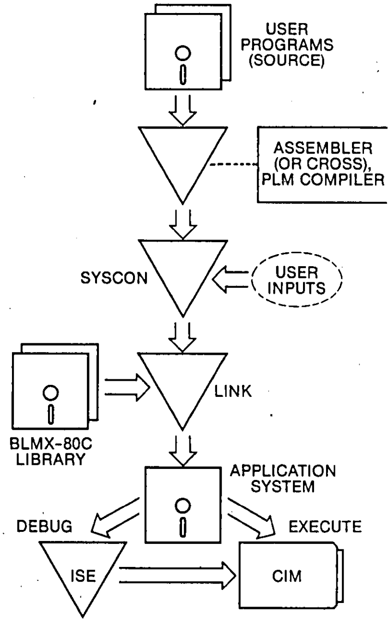


FIGURE 2. System Generation Process

The user is guided through the system generation process by SYSCON. The sophisticated NSC800 In-System Emulator from National Semiconductor Corporation eases the debugging of application-unique software.

BLMX-80C Executive Shipping Package

One diskette containing:
— BLMX-80C Nucleus
— Terminal Handler
— PLM80 Language Interface
— Fail-Safe Timer Handler
— Analog Handlers
— Initialization Library
— Interactive Debugger
— SYSCON (System Configuration Program)

Reference Manuals

BLMX-80C Reference Manual
BLMX-80 System User's Manual

Order Information

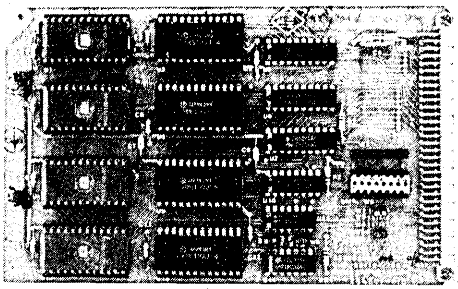
BLMX-80CS	BLMX-80C Executive for NSC800-based CIM CPU boards on a single density diskette
BLMX-80CD	BLMX-80C Executive for NSC800-based CIM CPU boards on a double density diskette

Documentation

BLMX-80CM	Manual set (#920308068-001) including the BLMX-80C System Reference Manual (#420306677-001) and the BLMX-80 System User's Manual (#420306432-001)

microCMOS

CIM™-100/104/108 and CIM-100C/104C/108C Memory Expansion Boards



- Adds RAM and/or PROM to a SERIES/800™ system
- Supports 2k × 8 PROM/RAM and 4k × 8 PROM devices
- Address-assignable on 16k boundaries
- High-performance, low power micro-CMOS technology
- Fits CIM-602/604 card cage
- All required connections for CIMBUS™ compatibility provided on-board
- Single 5 V_{DC} power supply
- −40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges
- Built solely with components burned in to A+ levels

Product Overview

The CIM-100 series of PROM/RAM Memory Expansion Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-100/104/108 and CIM-100C/104C/108C PROM/RAM Memory Expansion Boards are memory expansion boards for the SERIES/800 CMOS Industrial Microcomputers from National Semiconductor Corporation. The CIM-100/104/108 boards are identical except for the amount of factory-installed RAM: the CIM-100 has no RAM installed, the CIM-104 has 8k RAM installed, and the CIM-108 has 16k RAM installed. The CIM-100C/104C/108C boards are functionally identical to the CIM-100/104/108, with the only difference being their operating temperature range (0 to +70°C versus −40°C to +85°C). The CIM-100 series boards allow various combinations of PROM and RAM to be added to a CIMBUS system, up to a maximum of 8k PROM + 8k RAM, 16k PROM, 16k RAM, or 32k PROM. The CIM-100 series memory expansion boards, only 100mm × 160mm (3.9″ × 6.3″) in size, fit the CIM-602/604 series card cages, and are connected to the CIMBUS by 64-pin, pin-in-socket DIN 41612 connectors. See the CIMBUS System Bus Specification Manual for a description of the CIMBUS (order as CIMBUSM or Manual #420306681-001). The use of microCMOS technology gives high performance at low power consumption levels, and, in keeping with the aims of the SERIES/800 line, the CIM-100 series boards are designed for reliable performance over a wide range of harsh environmental conditions.

Functional Description

The CIM-100 series memory expansion boards are shipped with either no RAM (CIM-100/100C), 8k RAM (CIM-104/104C), or 16k RAM (CIM-108/108C) installed. User PROM may be added to the CIM-100 and CIM-104; address boundaries and board configurations are then established by on-board jumpers. The CIM-100 series functional units are:

- CIMBUS interface
- Address buffer
- Chip select circuitry
- Memory array
- Control logic circuitry
- Data buffer

The address buffer receives 16 address bits from the CIM-800 CPU through the CIMBUS interface and transfers the address bits to the internal address bus, the control logic circuitry, and the chip select circuitry. The chip select circuitry then determines which PROM/RAM device in the memory array should be enabled and sends four address bits to a decoder which enables the selected memory.

The memory array consists of two banks, each of which contains four PROM/RAM devices. A 16k byte memory block may be formed from 2k × 8-bit capacity RAM devices in combination with 2k × 8-bit capacity PROM devices. In this example, one memory array bank contains 8k bytes of RAM and the other bank contains 8k bytes of PROM. Other possible configurations with 2k × 8-bit capacity devices are 16k bytes of RAM only or 16k bytes of PROM only.

PROM devices with a 4k × 8-bit capacity may also be used. RAM or PROM devices with 2k × 8-bit capacity cannot be combined with 4k × 8-bit PROM devices. Possible configurations for the 4k × 8-bit PROM devices are 16k bytes of PROM (only one bank used) or 32k bytes of PROM (both banks used).

The memory configuration and address assignments are established by on-board jumpers. When memory is accessed, one PROM/RAM device is enabled by the chip select circuitry and eight bits of memory data are transferred in from or placed out on the board's internal data lines. Data direction depends on whether addressed memory is PROM or RAM and whether the memory request is a read or a write.

The control logic circuitry decides whether the memory access is a read or write cycle. The decision depends on information from the CIMBUS interface and two internal address bits. The data buffer transmits or receives data from the CIM-800 CPU; the CPU determines whether the direction of data movement is to or from the memory array.

Specifications

Memory Capacity

Various combinations to a maximum of 8k PROM + 8k RAM, 16k PROM, 16k RAM, or 32k PROM

Word size—	8 bits	
Compatible Memory Devices—	NMC27C16	(2k × 8-bit PROM)
	6116	(2k × 8-bit RAM)
	NMC27C32	(4k × 8-bit PROM)
Access Time—	515 ns	
Address Selection—	assignable on 16k boundaries within 64k bytes	

System Bus Interface

64-pin, pin-and-socket DIN 41612 connector.

Recommended mating connectors:
Winchester 96S-6033-0531-2
Elco 008257-096-649-124

Power

$V_{CC} = 5\ V_{DC} \pm 5\%$

PROM/RAM Used	Memory Size	Current (Max)
none	0k	1.23 mA
6116	8k	62.00 mA
NMC27C16	8k	27.00 mA
6116	16k	62.50 mA
NMC27C16 + 6116	16k	62.40 mA
NMC27C32	32k	27.00 mA

Environmental

Temperature:
CIM-100/104/108: −40°C to +85°C (−40°F to +185°F)
CIM-100C/104C/108C: 0 to +70°C (+32°F to +158°F)

Humidity: 0 to 90% noncondensing

Physical

Length: 6.30 in. (160 mm)
Width: 3.94 in. (100 mm)
Height: 0.50 in. (13 mm)
Weight: 0.71 oz. (20 gm) (CIM-100)

Order Information

CIM-100/104/108 and CIM-100C/104C/108C PROM/RAM Memory Expansion Boards

CIM-100	No RAM installed
CIM-100C	0 to +70°C (Commercial) version
CIM-104	8k RAM installed
CIM-104C	0 to +70°C (Commercial) version
CIM-108	16k RAM installed
CIM-108C	0 to +70°C (Commercial) version

Documentation

CIM-100M	CIM-100/104/108 and CIM-100C/104C/108C PROM/RAM Memory Expansion Board Hardware Reference Manual (#420305685-001)
CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

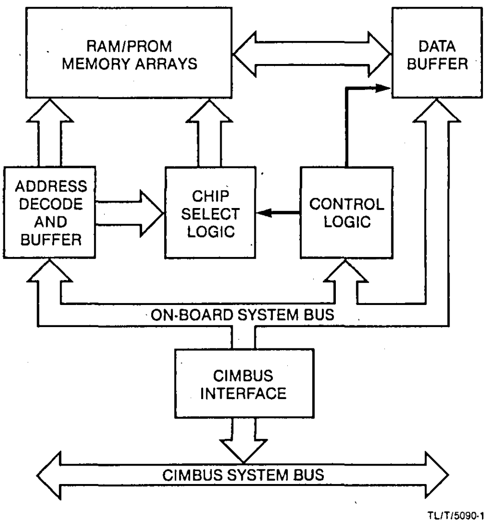
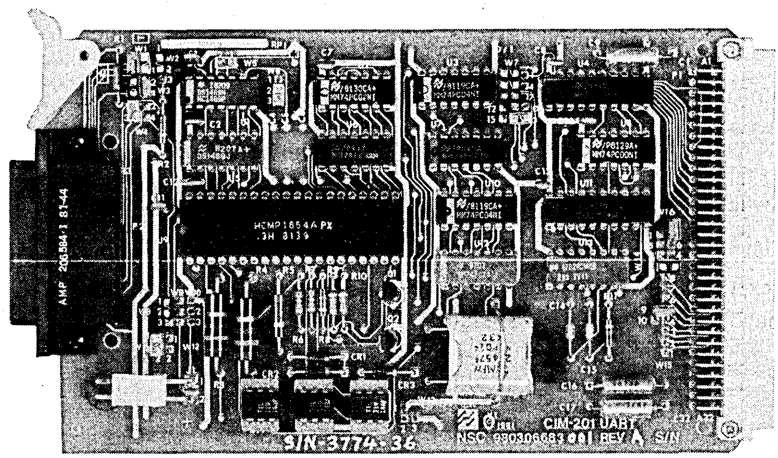


FIGURE 1. CIM-100 Series RAM/PROM Expansion Board Block Diagram

National Semiconductor

microCMOS

CIM™-201 and CIM-201C Serial Input/Output Boards



- Single-channel asynchronous transfer of serial data
- RS-232C or optically isolated 20 mA current loop operation
- Interfaces with wide variety of terminals, computers, printers, and other peripheral equipment
- May be configured as either data set (DCE) or data terminal (DTE)
- Can be used in pairs in demand/ response mode
- User-selectable baud rates from 50 to 153600
- Standard 25-pin "D" connector for serial data
- CIMBUS™-compatible with SERIES/800™ line
- Small 100 mm x 160 mm Eurocard form fits directly into CIM-602/604 card cages
- microCMOS technology gives high reliability at low power consumption
- −40°C to +85°C or 0°C to +70°F (commercial version) operating temperature ranges
- Designed for demanding use under harsh environmental conditions
- Built solely with components burned in to A+ levels

Product Overview

The CIM-201 and CIM-201C Serial I/O Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation and uninterruptable power supplies.

The CIM-201 Serial I/O Board provides the capability for RS232C or current loop controlled asynchronous data transfer between a SERIES/800 system and any compatible peripheral device. Such peripheral devices may include a wide variety of computers, terminals, printers, microwave links, or various kinds of control or instrumentation devices designed for RS232C or current loop operation. The CIM-201C is identical to the CIM-201, with the only difference being its operating temperature range (0°C to +70°C versus −40°C to +85°C).

The CIM-201 may be configured as either a data set (DCE), a device that interfaces with a communication channel such as telephone lines, or as a data terminal (DTE), the source or destination of data such as a CRT display, a computer, or a printer. Additionally, the CIM-201 may be used in pairs in a demand/response mode, where one CIM-201 is configured as a DCE and the other as a DTE.

Baud rates from 50 to 153600 are user-selectable. A configuration interrupt line provides communication between the CIM-201 and the CIMBUS. Transmission or reception by the CIM-201 may be interrupted if necessary; similarly, if the CIM-201 loses transmission (such as loss of carrier detect when connected to a modem), an interrupt flag may be output to the CIMBUS. See the CIMBUS Specification Manual for a description of the CIMBUS (order as CIMBUSM or Manual #420306681-001). RS232C connection is made by a standard 25-pin "D" connector.

If the CIM-201 is used in a current loop configuration, $\pm 15V_{DC}$ power may be obtained from the CIM-610 Voltage Regulator Board. Otherwise, only a single $30V_{DC}$ power source is required.

Like all the other members of the SERIES/800 line, the CIM-201 uses microCMOS technology throughout for high reliability at low power consumption levels. CIMBUS connections are made through pin-in-socket DIN 41612 connectors, which are highly resistant to vibration and corrosion, and eliminate the card edge connector, a primary failure source in many systems. The CIM-201 uses the single-wide Eurocard form factor, measuring only 100 mm x 160 mm (3.9" x 6.3"), and fits into the 8-slot and 18-slot CIMBUS card cages.

Functional Description

The CIM-201 Serial I/O Board transmits and receives asynchronous serial data. It consists of six major functional blocks:

- Address buffer
- Base address
- Baud rate selection
- Universal Asynchronous Receiver/Transmitter (UART)
- Data buffer
- Current loop interface

Address buffer

The address buffer consists of an 8-bit bidirectional transceiver that is always enabled and set to receive. It receives the eight least significant address bits (I/O mapped) from the CIMBUS and passes them on to the base address circuit, the baud rate select circuit, and the UART.

Base address

The base address circuit uses the five most significant address bits from the address buffer to establish, along with a user-selected jumper configuration, the base address for the CIM-201. There are 32 possible base addresses in the range from OOH to F8H in 8-bit increments. The base address is used as a reference to access five functions:

Base address+0 — loads transmitter holding register of the UART
Base address+1 — reads data received from a peripheral
Base address+2 — loads UART control register
Base address+3 — reads UART status register
Base address+4 — loads baud rate select register

Baud rate selection

The main component of the baud rate selection circuitry is a bit rate generator. When selecting a baud rate, the bit rate generator receives four data bits from the CIMBUS data lines and decodes them to select one of thirteen software-selectable baud rates from 50 baud to 9600 baud. Four more baud rates from 19200 baud to 153600 baud may be established by the configuration of on-board jumpers. The output of the baud rate selection circuitry provides the transmit and receive clocks for the UART.

Universal Asynchronous Receiver/Transmitter (UART)

The UART is the central element of the asynchronous serial I/O activity. Configured by the parameters established by the other functional portions of the CIM-201, it directs control signals used in the communication with units external to the SERIES/800 system and does the actual receiving and transmitting of data. It interacts with

- chip initialization and enable signals
- read/write lines
- clock signals
- register select
- external status
- data lines
- request to send, clear to send, and peripheral status interrupt lines
- interrupt line

Aside from its software-selectable functions, the UART can be configured by on-board jumpers to act as either a data set (modem) or a data terminal (terminal).

Data buffer

The data buffer is also an 8-bit bidirectional transceiver. Its function is to receive eight bits of data from the CIMBUS and route the data to internal data lines or to take data from the internal data lines and route it to the CIMBUS. These data bits are either communication data to or from the UART, special data reflecting the condition of the UART status register, or special data setting the configuration of the UART control register.

Current loop interface

The current loop interface circuitry controls the UART when current loop rather than RS232C interfacing is required. The current loop circuitry operates on the standard 20 mA current loop, and isolates the current loop driven device from the CIM system by means of optoisolators.

To facilitate throughput, the Peripheral Status Interrupt (PSI), indicates a status change when activated. For example, the modem Data Carrier Detect line is connected to the PSI input on the UART. If transmission fails because of loss of the carrier on the communications line, the UART sends an interrupt signal to one of the CIMBUS interrupt lines, which can be used by the SERIES/800 system to trigger action appropriate to the situation. This eliminates the need for polling the UART status.

Specifications

Addressing

Base address established by on-board jumpers from 00H to F8H in 8-bit increments.

Serial I/O

Control —	programmable UART
Transmission mode —	asynchronous
Word length —	5, 6, 7, or 8 bits
Parity —	odd, even, or none
Stop bits —	1, 1 1/2, or 2

Baud rates —	50.0	1800.0	
	75.0	2400.0	
	110.0	4800.0	
	134.5	9600.0	
	150.0	19200.0	(jumper-select.)
	200.0	38400.0	"
	300.0	76800.0	"
	600.0	153600.0	"
	1200.0		

Error detection —	framing, data overrun, parity
Interface —	RS232C or 20 mA current loop

Connectors

CIMBUS — Pin-in-socket DIN 41612
Recommended mating connectors:
Winchester 96S-6033-0531-2
Elco 008257-096-649-124

RS-232C — Standard 25-pin "D"
Recommended mating connectors:
3M 3482-1000 (crimp connection)
Cinch DB-19604-432 (solder connection)

Optional power — Two-contact header
Recommended mating connectors:

Vendor	Housing	Contact
Molex	09-50-3021	08-50-0106
Methode	3300-102	3400-111

(Optional power connector provided)

Power

$+5V_{DC}$	61.0mA
$+15V_{DC}$	29.5mA
$-15V_{DC}$	18.0mA

(Includes power for optoisolators used in 20mA current loop operation)

Environmental

Temperature — CIM-201: −40°C to +85°C (−40°F to +185°F)
CIM-201C: 0°C to +70°C (+32°F to +158°F)

Humidity — to 90% noncondensing

Physical —

Length	6.30 in.	(160.0 mm)
Width	3.94 in.	(100.0 mm)
Height	0.73 in.	(18.5 mm)
Weight	1.2 oz.	(32.0 gm)

Order Information

CIM-201	CIM-201 Serial Input/Output Board
CIM-201C	0°C to +70°C (commercial) version

Documentation

CIM-201M	CIM-201 and CIM-201C Serial Input/Output Board Hardware Reference Manual (#420306683-001)
CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

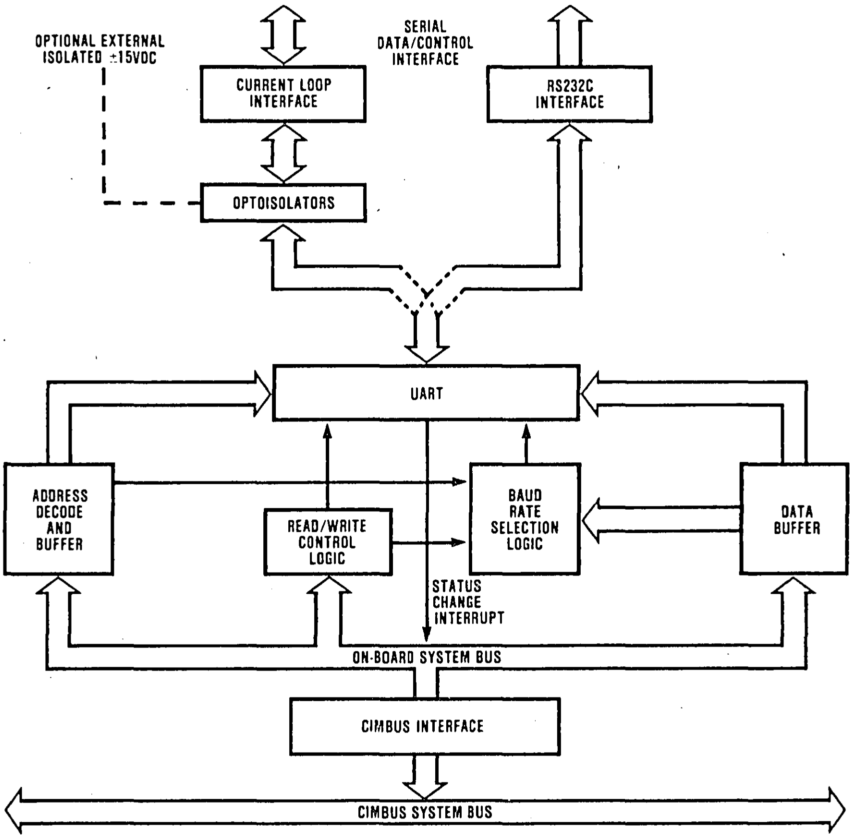


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FIGURE 1. CIM-201 Serial I/O Board Block Diagram

CIM™-203 and CIM-203C Dual Channel Serial I/O Boards

- **Two, totally independent asynchronous serial I/O channels**
- **One channel alternately run in synchronous mode (user-installed option)**
- **Programmable baud rates**
  - **-Async to 19.2k baud**
  - **-Sync to 38.4k baud**
- **Either or both channels can be either RS232C, RS422, or RS423**
- **Each channel may be configured either as data set or data terminal**
- **Two levels of maskable interrupts**
- **CIMBUS™-compatible with SERIES/800™ board line**
- **Small 100mm × 160mm Eurocard form fits directly into CIM-602/604 card cages**
- **microCMOS technology gives high reliability at low power consumption**
- **−40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges**
- **Built solely with components burned in to A+ levels**

Product Overview

The CIM-203 and CIM-203C Dual-Channel Serial I/O Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

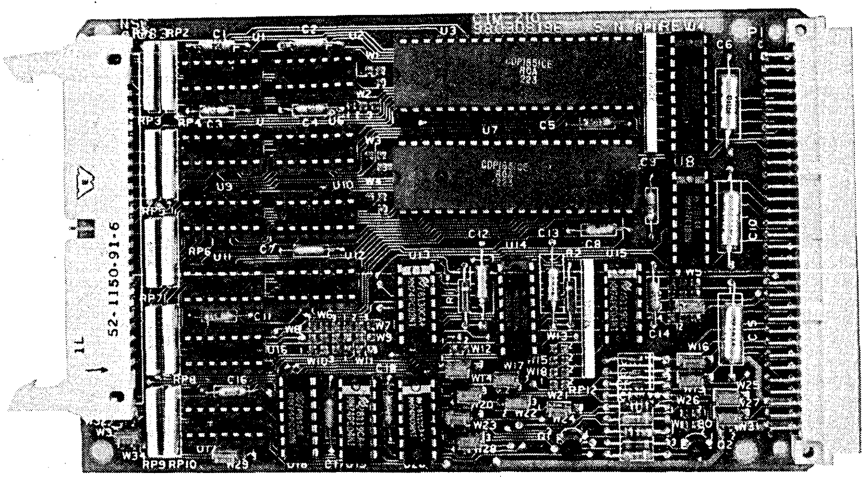
The CIM-203 Dual-Channel Serial I/O Board provides the capabilities for synchronous or asynchronous serial communications over RS232C-, RS422-, or RS423-compatible interfaces between a CIMBUS system and many other systems and peripherals. The board contains two totally separate channels, thus allowing each to be configured and run independent of the other. Baud rates are software-selectable from 50 baud to 19.2k baud, and jumper-selectable above that. The CIM-203 is shipped with two UARTS installed, permitting only asynchronous operation. The user can optionally replace one UART with a USART if a synchronous channel is required. The transceivers installed on the board, as shipped, are for RS232C interfaces. Transceivers appropriate for RS422/423 may be alternately used on either, or both channels. The CIM-203C is identical to the CIM-203, with the only difference being its operating temperature range (0 to +70°C, versus −40°C to +85°C).

The CIM-203 shares the small 100mm × 160mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fits the CIM-602/604 card cages. It is completely CIMBUS-compatible through a pin-and-socket DIN 41612 connector, which provides an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420306681-001) for a description of the CIMBUS.

National Semiconductor

microCMOS

CIM™-210 and CIM-210C Parallel I/O Boards



- 40 bit-programmable I/O lines, with provisions for interchangeable line drivers and terminators
- 4 levels of maskable interrupts
- Fail safe logic sets outputs to a known state if CPU fails
- Small 100mm × 160mm Eurocard form factor fits directly into CIM-602/604 card cages
- Compatible with CIMBUS™ system bus
- microCMOS technology gives high reliability with low-power consumption
- −40°C to +85°C or 0°C to +70°C (commercial version) operating temperature ranges.
- Built solely with components burned in to A+ levels

Product Overview

The CIM-210 and CIM-210C Parallel I/O Boards are members of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. Series/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-210 Parallel I/O Board provides bit-programmable, parallel input and output for a CIMBUS system. Forty lines are furnished, arranged as four 8-bit ports and four 2-bit ports (which also serve as handshake or strobe lines in several of the programmable modes). Sockets on the I/O interface allow each line to be configured for numerous different applications by the insertion of buffers or simple shorting wires (pull-up resistors are already provided). Four levels of maskable interrupts are generated by the interface devices which may be jumpered to any of the eight interrupt lines on the CIMBUS. The CIM-210C is identical to the CIM-210, with the only difference being its operating temperature range (0°C to +70°C, versus −40°C to +85°C).

Like all other members of the SERIES/800 line, the CIM-210 uses microCMOS technology throughout for high reliability at low-power consumption levels. CIMBUS connections are made through pin-and-socket DIN 41612 connectors, which are highly resistant to vibration and corrosion, and eliminate the card edge connector, a primary failure source in many systems. The CIM-210 uses the single-wide Eurocard form factor, measuring only 100mm x 160mm (3.9" x 6.3").

Table 1. CIM-210 I/O Address assignments

I/O Address	Read	Write
BASE+0	Unused	PIO #1 Reset
BASE+1	PIO #1 Status	PIO #1 Control
BASE+2	PIO #1 Port A Input Data	PIO #1 Port A Output Data
BASE+3	PIO #1 Port B Input Data	PIO #1 Port B Output Data
BASE+4	Unused	PIO #2 Reset
BASE+5	PIO #2 Status	PIO #2 Control
BASE+6	PIO #2 Port A Input Data	PIO #2 Port A Output Data
BASE+7	PIO #2 Port B Input Data	PIO #2 Port B Output Data

Functional Description

The CIM-210 Parallel I/O Board consists of six major functional blocks:

- data buffer
- address decode circuit
- control fail circuit
- Parallel Input/Output (PIO) circuit
- interrupt circuit
- input/output buffer section

Data Buffer

The data buffer is an 8-bit bidirectional transceiver. Its function is to receive eight bits of data from the CIMBUS and route the data to internal data lines, or to take data from the internal data lines and route it to the CIMBUS. These data bits are either I/O data to or from the PIOs, special data reflecting the condition of a PIO status register, or special data setting the configuration of a PIO control register.

Address Decode Circuit

The address decode circuit decodes the CIMBUS address lines A0 through A7. Eight I/O locations are required, with the actual base address set by onboard jumpers. The base address can be any location on an even eight-byte boundary from OOH to F8H. The address decode circuit enables the data buffer and either selects one of the two PIOs or clears one of the two PIOs when a valid address is present on the CIMBUS (see Table 1).

Control Fail Circuit

The control fail circuit monitors the CIMBUS fail-safe timer (TMRFS) signal. TMRFS is a low-frequency (1 Hz) clock signal generated by the CPU board. If the TMRFS signal should fail to toggle for 1.6 seconds, or longer (indicating that the CPU has failed, or hung up), the control fail circuit activates on onboard fail signal. This signal, in turn, clears the PIOs (sets all lines to input mode), thus driving all outputs to a known state as determined by the actual buffer used (see Table 3).

Parallel Input/Output (PIO) Circuit

The PIO circuit consists of two PIO chips. A total of 40 input/output lines are available, 20 input/output lines for each PIO. Each PIO is further divided into two ports (port A and port B) and four handshaking lines (RDY A, STB A, RDY B, and STB B). Each port contains eight I/O lines. The remaining four I/O lines connect to the four handshaking lines. (See Table 2.)

Each PIO chip can be programmed to operate in four modes. They are:

- Input mode—data input to port only
- Output mode—data output from port only
- Bidirectional mode—data input and output to port.
- Bit programmable mode—sets individual lines of a port, including handshaking lines, as either inputs or outputs.

Interrupt Circuit

A total of four interrupt lines can be jumpered to any of the eight CIMBUS interrupt lines. The outputs are open drain so they can be jumpered together in groups ranging from one to four.

Interrupts are generated by:

- each port of each PIO
- strobed input and output when programmed
- ports monitored for specific input conditions when the condition is true.

Input/Output Buffer Section

To make the CIM-210 universal in its application, buffer sockets are provided at the I/O interface to allow each line to be configured as required. The buffers may be any device that has the same structure as a 74XX00

Table 2. PIO Operating Modes

Mode	(8) Port A Data Pins	(2) Port A Handshaking Pins	(8) Port B Data Pins	(2) Port B Handshaking Pins
Input	Accept input data	Ready, strobe	Accept input data	Ready, strobe
Output	Output data	Ready, strobe	Output data	Ready, strobe
Bidirectional (Port A only)	Transfer input/ output data	Input hand-shaking for Port A	Must be previously set to bit-programmable mode	Output hand-shaking for Port A
Bit-Programmable	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs

gate. Table 3 lists some of the possible devices. Naturally, simple shorting wires may also be inserted in the sockets, but good design practice may suggest that a 74HC02 be used for inputs to protect the PIOs. Pull-up resistors are already provided on the CIM-210. (The CIM-210 is factory shipped without buffers.)

Table 3. Buffer selection guide

Buffer	Data Inversion	Fail State	Drive High (mA)	Drive Low (mA)
Wires	No	High*	1.6 min	1.15 min
74HC00	Yes	High	3.4 min	3.4 min
74HC08	No	Low	3.4 min	3.4 min
74HC32	No	High	3.4 min	3.4 min
7400	Yes	High	0.4 max	16.0 max
7408	No	Low	0.8 max	16.0 max
7432	No	High	0.8 max	16.0 max
7438	Yes	High*	0.5 max	48.0 max
74L00	Yes	High	0.2 max	3.6 max
74L08	No	Low	0.2 max	3.6 max
74L32	No	High	0.2 max	3.6 max
74LS00	Yes	High	0.4 max	8.0 max
74LS08	No	Low	0.4 max	8.0 max
74LS32	No	High	0.4 max	8.0 max
74LS38	Yes	High*	0.5 max	24.0 max
74S00	Yes	High	1.0 max	20.0 max
74S08	No	Low	1.0 max	20.0 max
74S32	No	High	1.0 max	20.0 max
74C00	Yes	High	1.75 min	8.0 min
74C08	No	Low	1.75 min	8.0 min
74C32	No	High	1.75 min	8.0 min

*Fail state is high due to 10K pullup resistors.

The 40 input and output signals are obtained through a 50-pin ribbon connector. This leaves 10 pins for power and grounds. Main power to the decode and the port chips is from the $5V_{DC}$ power on the back plane. Jumpers are provided for outputting power to the connector on the spare pins. The voltages are: $+5V_{DC}$, $+15V_{DC}$, digital and analog grounds. There are also special jumpers for the buffer sockets. These jumpers are for setting buffer $+5V_{DC}$ or $+15V_{DC}$ power from an internal or external source. The external power may be used for high power applications exceeding the system supply rating. The power to the I/O connector may be used for signal conditioning. The current on any of the supplies should not exceed safe operating limits.

Specifications

Addressing: Base address established by onboard jumpers from 00H to F8H in 8-bit increments (see Table 1).

I/O Capacity: 40 programmable lines (see Table 2)

Interrupts: Four interrupts may originate from either port (2) on both PIOs (2)

Connectors

Parallel I/O: 50-pin locking header
Recomended mating connectors:
3M 3425-7050
Winchester 61-1150-01
AMP 1-499662-0

CIMBUS: Pin-and-socket DIN 41612
Recommended mating connectors:
Winchester 96S-6033-0531-2
Elco 008257-096-649-124

Power $+5V_{DC}$ @ 15mA (sockets empty, as shipped)
$+5V_{DC}$ @ 20mA (sockets contain 74HC08 buffers)
($+5V_{DC}$, $+15V_{DC}$ used externally will draw an additional amount of current from the CIMBUS)

Environmental

Temperature: CIM-210: $-40°C$ to $+85°C$ ($-40°F$ to $+185°F$)
CIM-210C: $0°C$ to $+70°C$ ($+32°F$ to $+158°F$)

Humidity: 0 to 90% noncondensing

Physical

Length: 6.30 in. (160 mm)
Width: 3.94 in. (100 mm)
Height: 0.50 in. (13 mm)
Weight: 3.00 oz. (85 gm)

Order Information

CIM-210	CIM-210 Parallel I/O Board
CIM-210C	0°C to +70°C (commercial) version

Documentation

CIM-210M	CIM-210/-210C Parallel I/O Board Hardware Reference Manual (#420308196-001)
CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

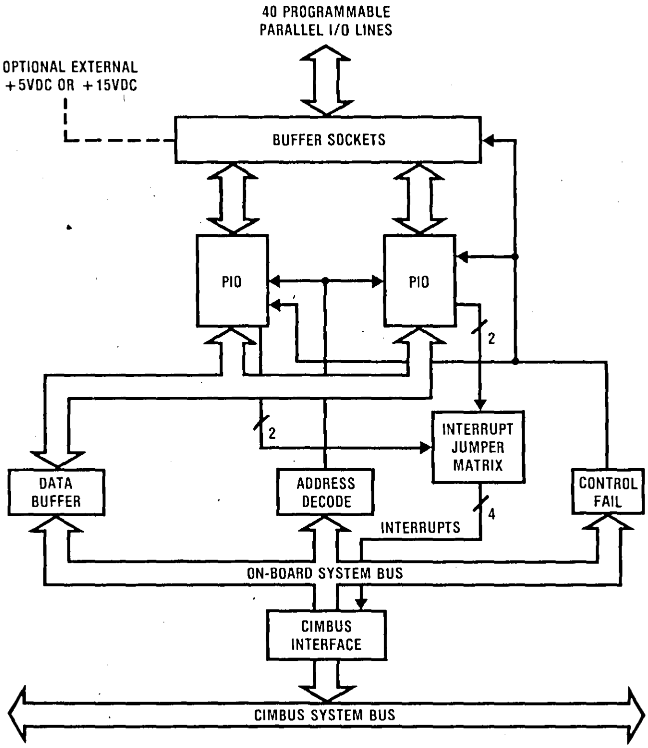


FIGURE 1. CIM-210 Parallel I/O Board Block Diagram

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PRELIMINARY

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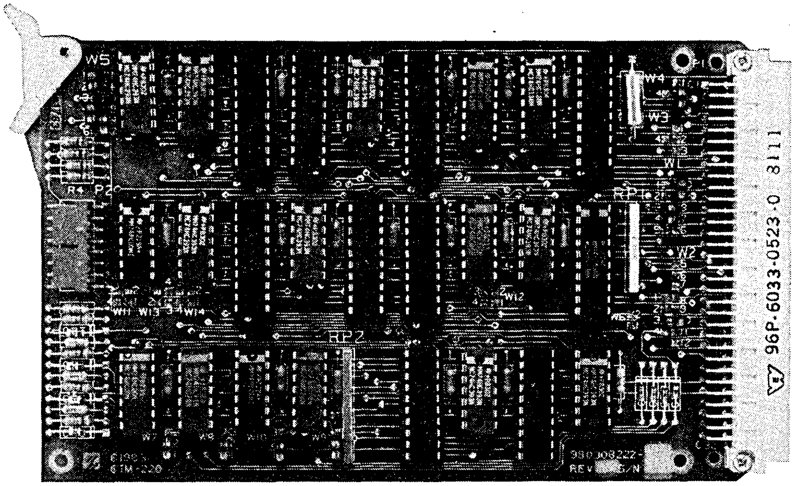
CIM™-220 and CIM-220C Frequency/Period Measurement Boards



- Interface to tachometers and voltage-to-frequency converters
- Four independent input channels
- 16-bit resolution on both frequency and period measurements
  - — Frequency: DC to 5MHz
  - — Period: 64msec to days
- Interface directly with sensors or converters with outputs ranging from:
  - — Max: 4.5V to 15V (absolute value)
  - — Min: ≤0.5V (absolute value)
  - — Periodic or nonperiodic
  - — Unipolar or bipolar
- Four independent interrupts on "end of count"
- CIMBUS™-compatible with SERIES/800™ board line
- Small 100mm × 160mm Eurocard form fits directly into CIM-602/604 card cages
- microCMOS technology gives high reliability with low-power consumption
- −40°C to +85°C or 0°C to +70°C (commercial version) operating temperature ranges
- Built solely with components burned in to A+ levels

Product Overview

The CIM-220 and CIM-220C Frequency/Period Measurement Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-220 Frequency/Period Measurement Board was designed with a multiplicity of applications in mind. Via its flexible architecture, it can be used to interface to tachometers, resolve data from any sensor with a voltage-to-frequency converter on its output, or act as an event counter and/or timer. It is capable of receiving four separate inputs, and calculating either the frequency or the period of each signal. The board's interface logic allows the connection of many devices directly to the CIM-220. The CIM-210C is identical to the CIM-210, with the only difference being its operating range (0°C to +70°C, versus −40°C to +85°C).

The CIM-220 cleverly offers a solution to a major design problem in many applications: that of providing a clean and accurate remote sensor input to the computer. Long lines and electrical noise have always plagued the designer who must measure microvolt full scale interfaces. The traditional answer is to add a current loop converter/transmitter at the sensor, or/and an analog signal conditioning panel at the computer. The CIM-220 allows a simpler and less expensive solution, that, potentially, offers even better resolution. By following the remote sensor with a voltage-to-frequency converter, the interface becomes inherently less susceptable to electrical distance and noise. It has the secondary advantage of replacing an analog-to-digital converter board, often the most expensive portion of the computer, with the CIM-220, Additionally, with the board's 16-bit counters, resolution is increased from typical A/D values of 8 and 12 bits.

The CIM-220 shares the small 100 mm × 160 mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line, and fits the CIM-602/604 card cages. It is completely CIMBUS-compatible through a pin-and-socket DIN 41612 connector, which provides an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420306681-001) for a description of the CIMBUS.

National Semiconductor

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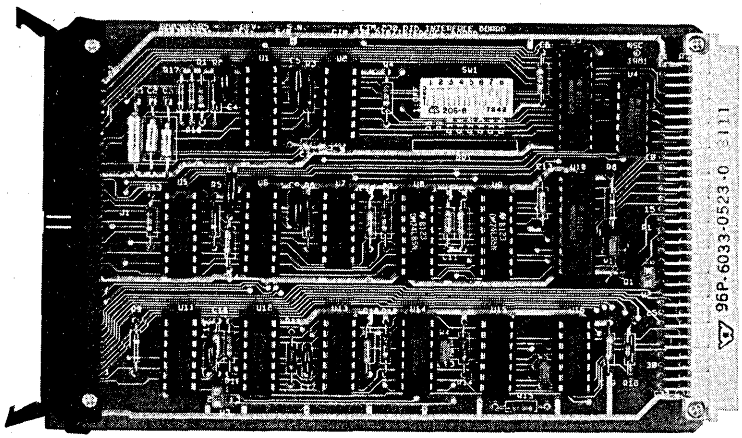
CIM™-230 and CIM-230C Distributed I/O Bus (DIB™) Interface Boards



- **Provides the interface between the CIMBUS™ and the DIB**
- **Small (100 mm × 160 mm) single-wide Eurocard form fits CIM-602/604 card cages**
- **microCMOS technology gives high reliability at low power consumption**
- **−40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges**
- **Built solely with components burned in to A+ levels**
- **DIB offers advantages for many applications**
  —Software I/O routines are the same for all DIB I/O
  —Single 60-pin flat cable used to interface/multi-drop up to 256 input ports and 256 output ports
  —Polarized interface hardware ensures correct connections
  —Switched high voltage/current interfaces remote from card cage
  —Form factor and mounting method for user-designed DIB boards dictated only by application convenience

Product Overview

The CIM-230 and CIM-230C Distributed I/O Bus (DIB) Interface Boards are members of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS™, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh envoronments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The Distributed I/O Bus (DIB) is an isolated interface providing external mapped parallel I/O to a SERIES/800 system. Consisting of a single 60-wire flat cable, it allows simple yet flexible connections to remote, discrete I/O devices such as relays, limit switches, thumbwheels, and indicators. The recommended connectors/cabling provide standard connections to the I/O devices and eliminate physically complicated and error-prone wiring schemes. Similarly, all I/O devices are controlled the same way, which greatly simplifies the task of writing software I/O routines.

The CIM-230 DIB interface board is the interface between the CIMBUS and the DIB. It translates the signals between the two bus systems, accounts for timing differences, and can accommodate up to 256 input and 256 output ports. The CIM-230C is identical to the CIM-230 with the only difference being its operating temperature range (0 to +70°C versus −40°C to +85°C).

Functional Description

CIM-230 DIB Interface Board

The CIM-230 is made up of six functional units: address buffer, address intercept circuit, control logic, data buffer, watchdog timer, and fail-safe circuitry.

The eight high-order CIMBUS address bits are brought into the CIM-230 through the address buffer. These eight bits, which constitute the addresses of the 512 (256 input and 256 output) possible I/O ports, are then placed on the DIB address bus.

The address intercept circuit decodes the buffered address bits and determines whether or not the CIM-230 is being addressed. The CIM-230 address, which is set by on-board jumpers, may be one of three types: a single address, all addresses from 00H to a preset upper limit, or all addresses from a preset lower limit to FFH.

The control logic generates control signals for DIB I/O and a WAIT signal for the CIMBUS, which synchronize the operation of DIB I/O devices with the system processor. When the CIM-230 is addressed, the CIM-230 in turn puts a device address onto the DIB. The addressed device responds with a PORT READY signal, and the data is strobed in from or out to the addressed port. The CIM-230 will generate a CIMBUS WAIT signal, causing the CPU to suspend operation until the port data is received or transmitted.

The data buffer is the holding area for I/O data being passed between the DIB and the CIMBUS. The data buffer is bidirectional and gates the data in the appropriate direction based on a signal from the control logic.

Under normal conditions, the CIMBUS WAIT is cleared when the addressed I/O device responds with its PORT READY signal. In the event that a nonexistent or failed I/O device is addressed, the watchdog timer will lift the WAIT signal after a preset timeout period. The timeout period, based on the CIMBUS clock signal, can be either 4, 8, or 16 clock cycles.

The fail-safe circuitry monitors the system fail-safe timer. If the system fail-safe timer stops for longer than 1.6 seconds, a processor failure is assumed, and the fail signal that is generated can be used to initiate failure-related I/O functions, such as turning off all relay-controlled equipment.

Access to all of the eight interrupts on the CIMBUS is provided to any device on the DIB via the CIM-230.

Distributed Input/Output Bus

The Distributed I/O Bus (DIB) provides a means for discrete, parallel I/O, which is beneficial for many applications. It is a mapped, parallel I/O bus for use outside of a CIMBUS card cage (*Figure 1*), and is intended for use with discrete I/O devices such as relays (solid state or electromechanical), switches, displays/indicators, hexadecimal keypads, and many other relatively "slow" devices. It is not a replacement for common "high-speed" interfaces to such peripherals as video display terminals, printers, and floppy disk drives.

In general, the DIB is an alternative to the typical digital I/O expansion board found in the card cage in many microcomputer architectures. The traditional architecture often has many disadvantages in terms of both the system's design and its manufacture:

1. When there is a large number of I/O devices with which to interface, signal conditioning and cable routing/strain relief become burdensome, and accommodating measures in manufacturing are prone to errors.

2. Switching high voltage/current interfaces tends to introduce noise in the system's backplane unless the necessary steps for isolation, some of which are prohibitive in terms of cost and size, are taken.

3. Because I/O connections are made "directly" to the microcomputer bus, the microcomputer's software must deal "directly" with the uniqueness of each interface. This uniqueness places the burden for making the interface work on the software programming, which often results in massive sets of I/O modules (frequently the reason for the software design costs being much greater than the hardware design costs).

4. If the application calls for a unique interface which is not available off the shelf, then an expansion board which adheres to a set of bus specifications must be designed. The bus specifications will then dictate the bus electrical interface, the form factor, the mounting orientation, and often the allowable power dissipation.

The architecture of the DIB is particularly advantageous for applications with medium to large I/O requirements due to the fact that it corrects the drawbacks listed previously:

1. All DIB I/O is done through the CIM-230, over a single cable, and then to any number and configuration of boards/functions up to a total of 256 input ports and 256 output ports (or 2048 input lines and 2048 output lines).

2. Because the DIB is an isolated bus to remote I/O functions, that functionality will not introduce noise into a CIMBUS system.

3. The CIM-230 is the translator between the CIMBUS and the DIB. One of its duties is to provide a consistent interface to the microcomputer. All differences in timing, signal definition, and interface "protocol" are supplied by either the CIM-230 or the interfacing hardware at the I/O end of the DIB. This consistent interface allows standardization of all DIB-related I/O software routines.

4. The specification for the DIB involves only the timing and functionality for the ribbon cable interface. The form factor and means/location for mounting are left to the designer and can be whatever is convenient for any unique application.

The DIB can be thought of as consisting primarily of buffered or terminated CIMBUS signals such as the address, data, interrupt, and power and ground lines. It also contains several handshake and strobe signals to ensure proper communications through a potentially noisy environment (Table I).

An example of the kind of functionality that is typically put on the DIB is that provided by the CIM-311 Power I/O DIB Board. This board provides an interface to the popular solid state relay racks offered by, and multisourced by, many vendors. In addition, the CIM-311 contains four maskable interrupts.

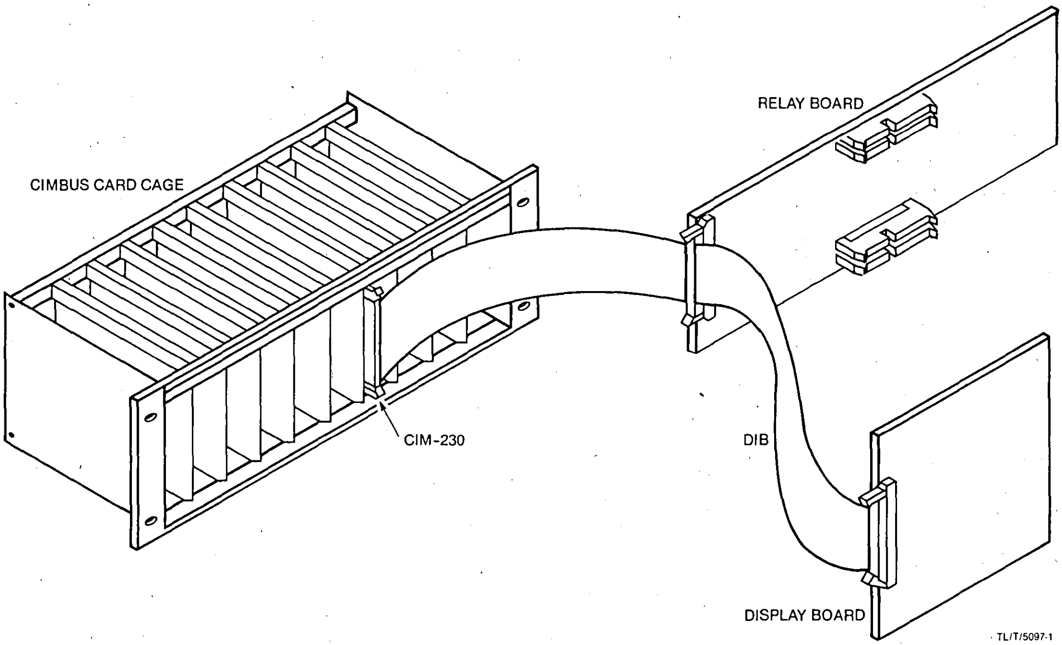


FIGURE 1. The DIB is an external I/O bus which can be extended, through multi-drops, to 256 input and 256 output ports

Specifications

Address Space

Selectable— 00H to preset upper limit
Preset lower limit to FFH
Single address

Factory Setting—00H to BFH, inclusive

Timeout Period

Selectable— 4, 8, or 16 CIMBUS clock cycles

Factory Setting—16 clock cycles

DIB Lines Available

8 Data
8 Address
8 Interrupt
5 Timing + strobes
5 Handshake
24 Power + ground

(See Table I for DIB pin/signal definitions.)

Connectors

CIMBUS	Pin-in-socket DIN 41612 Recommended mating connectors: Winchester 96S-6033-0531-2 Elco 008257-096-649-124
DIB	60-pin locking header Recommended mating connectors: 3M 3334-6060 Amp 88479-9 (Connector provided)

Power	+5 $V_{DC} \pm 0.2$ V_{DC}, 16 mA typical
Environmental	Temperature: CIM-230: −40°C to +85°C (−40°F to +185°F) CIM-230C: 0°C to +70°C (+32°F to +158°F) Humidity: 0 to 90% noncondensing
Physical	Length: 6.30 in. (160 mm) Width: 3.94 in. (100 mm) Height: 0.55 in. (13 mm) Weight: 4 oz. (110 gm)

Order Information

CIM-230	Distributed Input/Output Bus Interface Board
CIM-230C	0 to +70°C (Commercial) version

Documentation

CIM-230M	Distributed I/O Bus (DIB) CIM-230 and CIM-230C DIB Interface Board Hardware Reference Manual (#420306595-001)
CIMBUSM	CIMBUS System Specification (#420306681-001)

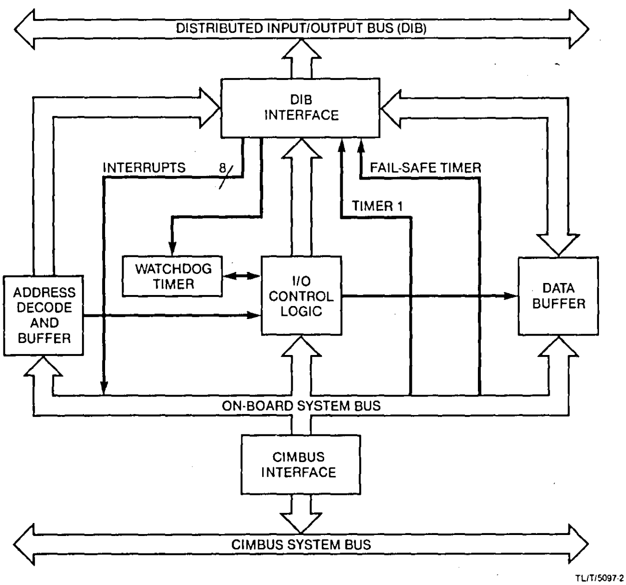


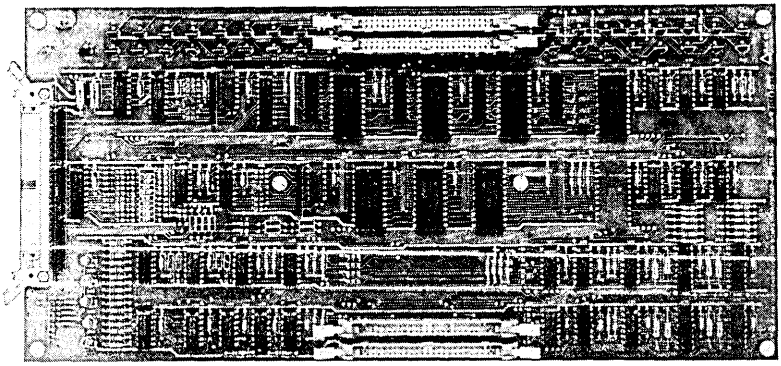
FIGURE 2. CIM-230 DIB Interface Board Block Diagram

Table 1. DIB Pin Assignments

Pin	Mnemonic	Signal Name	Pin	Mnemonic	Signal Name
1	INT1		2	INT2	
3	INT3	INTERRUPT	4	INT4	INTERRUPT
5	INT5	REQUESTS	6	INT6	REQUESTS
7	INT7		8	INT0	
9	RESOUT/	RESET OUT	10	PORTREADY/	PORT READY
11	GND	GROUND FOR +5V	12	IODAOU/	I/O DATA OUT/
13	GND	GROUND FOR +5V	14	GND	GROUND FOR +5V
15	OUTCK/	OUTPUT CLOCK/	16	IODAIN/	I/O DATA IN/
17	OUTEN	OUTPUT ENABLE	18	INPEN	INPUT ENABLE
19	GND		20	FAIL/	FAIL/
21	GND		22	M1	INSTRUCTION FETCH
23	GND		24	ADR15	
25	GND		26	ADR14	
27	GND		28	ADR13	
29	GND	GROUND FOR +5V	30	ADR12	ADDRESS
31	GND		32	ADR11	LINES
33	GND		34	ADR10	
35	GND		36	ADR9	
37	GND		38	ADR8	
39	GND		40	GND	
41	DAT7		42	GND	
43	DAT6		44	GND	
45	DAT5		46	GND	
47	DAT4	DATA	48	GND	GROUND FOR +5V
49	DAT3	LINES	50	GND	
51	DAT2		52	GND	
53	DAT1		54	GND	
55	DAT0		56	GND	
57	+5V	+5V DC POWER	58	+5V	+5V DC POWER
59	IGND	ISOLATED GROUND	60	IGND	ISOLATED GROUND

microCMOS

CIM™-311 and CIM-311C Power I/O DIB™ Boards



- **Allows the instant addition of popular solid state relay racks to a CIMBUS™ system**
  - Provides high voltage/current switching
  - Isolates switching-induced noise from the computer bus
  - Provides terminal strips for interface connections
- **Four maskable interrupts on positive or negative-going signals, or on any change of state**
- **Interfaces to a CIMBUS system via the Distributed I/O Bus (DIB)**
- **−40°C to +85°C or 0°C to 70°C (commercial version) operating temperature ranges**
- **microCMOS and CMOS technology provides high reliability**
- **Built solely with components burned in to A+ levels**

Product Overview

The CIM-311 and CIM-311C Power I/O DIB Boards are members of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-311 Power I/O DIB Board permits the instant addition of the popular models of solid state relay racks available from numerous vendors to a

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CIMBUS system. It interfaces via the Distributed Input/Output Bus, versus the CIMBUS, and therefore does not reside in a CIMBUS card cage (see Figure 1). Instead, it mounts wherever it is convenient for the application, and does so in the same fashion as the solid state relay rack, via six threaded standoffs. The CIM-311C is identical to the CIM-311, with the only difference being its operating temperature range (0°C to +70°C versus −40°C to +85°C). The Distributed Input/Output Bus (DIB) is detailed in the DIB Specification and CIM-230 DIB Board Hardware Reference Manual (#420306595-001).

The ability to easily add solid state relays (SSRs) is important to an industrial-oriented microprocessor-based system. These devices provide an isolated, and highly reliable interface to the real world. Generally, the SSRs are available in various ratings for AC input, AC output, DC input, and DC output. Industrial-type barrier strips are provided on the SSR racks for connection to the devices to be monitored or controlled.

In addition, the CIM-311 can generate up to four maskable interrupts on positive-going signals, negative-going signals, or any change of state from the SSRs. The board measures 6.6 in x 14.0 in (167 mm x 356 mm).

Functional Description

The CIM-311 Power I/O DIB Board is made up of six functional blocks:

- DIB interface
- Address decode and buffer
- I/O control logic
- Data buffers
- Interrupt logic
- I/O interface

DIB Interface

The interface to the Distributed I/O Bus (DIB) is via a 60-pin locking header. This is a high-density connection that is resistant to vibration and corrosion. This connector allows for convenient mass termination without cable dressing, allowing easy implementation of the DIB mutlidrop feature. The connector is keyed to prevent incorrect insertion.

Address Decode and Buffer

The CIM-311 can be set for any address on a four-byte boundary within the 256 CIMBUS I/O port range with onboard jumpers. Each address which falls within the selected range represents both an 8-bit input port and an 8-bit output port, with the actual direction determined by the I/O control logic.

I/O Control Logic

The I/O control logic receives the specific address from the address logic, if it falls within the selected range, and then provides activation strobes and/or logic levels to select the required function on the CIM-311 board. This circuitry determines whether the required function is input or output, and which of the onboard resources are involved (I/O, interrupts, or power/processor fail).

Data Buffer

The data buffer consists primarily of bidirectional transceivers. Data direction and input/output clocking is controlled by the I/O control logic.

Interrupt Logic

The interrupt logic provides for four optional interrupts from one input port. As selected by user-installed jumpers, any or all of input lines 0, 1, 2, or 3 (each port has eight lines) of port 0 (each board has four input/output ports) can generate interrupts. The user can also select whether the interrupt is generated on a positive-going signal, a negative-going signal, or any change of state.

If masks are desired for these interrupts, bits 4, 5, 6, and 7 of output port 3 are utilized. This reduces the number of possible output lines by four.

The interrupts can be connected to any of the eight CIMBUS interrupts via the DIB through the CIM-230 DIB Interface Board.

Interface Drivers And Receivers

On-board buffers/latches and level translation logic provide the interface to the SSR racks.

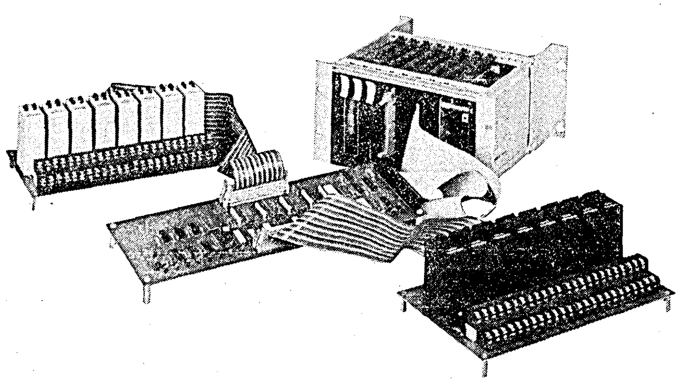

FIGURE 1. Example of a CIMBUS system utilizing 32 solid state relay inputs and 32 outputs. Both the input rack and the output rack connect to the CIM-311, which, in turn, interfaces to a CIMBUS system via the DIB.

CPU Interface

Each CIM-311 (there can be up to 64 on the DIB) has four unique I/O addresses, as set by user-selected jumper placement. Each address represents both eight input lines and eight output lines, or two I/O ports. The interface for the CPU is as if the I/O ports are located on the CPU board, due to the CIM-230 DIB Interface Board providing the translation between the CIMBUS and the DIB. A single NSC800 I/O instruction is all that is required to drive or access any port.

Output Operations

Each time the CPU executes an output instruction for a CIM-311, the value of every bit in the data byte must first be formulated. If a bit is set (logical "1"), the corresponding SSR is energized, or remains energized. If a bit is reset (logical "0"), the corresponding SSR is deenergized, or remains deenergized.

If the CPU board in the CIMBUS system should fail or hang up for any reason, the CIM-230 DIB Interface Board will assert the FAIL/ signal. This forces all CIM-311 outputs to a deenergized state.

Input Operations

For input operations, the meaning for each bit is reversed. The CPU executes an input instruction with the desired port address. If a bit in the received data byte is reset, the SSR is energized; if it is set, the SSR is not energized.

The device providing the excitation to the SSR will dictate whether one read of the port values is adequate to determine the intended state of the interface. Some devices generate "contact bounce" for a longer period of time than the typical SSR can filter out (values of 5 to 20 milliseconds of debounce are generally provided). This may require several iterations of reading the port and scanning the bit values.

Specifications

Ports	4 input ports and 4 output ports
Lines per Port	8
Input Characteristics	Logical 1 = $5V_{DC} \pm 5\%$ Logical 0 = $0V_{DC}$, 5 mA sink min. required from SSR
Output Characteristics	Logical 1 = 5 to $24V_{DC}$ Logical 0 = $0V_{DC}$, 80 mA sink supplied to SSR
Address Selection	Any 4-byte boundary in 256
Interrupts	
Number Available—	4 (input port 0, lines 0, 1, 2, 3)
Masks—	Available for each interrupt (output port 3, bits 4, 5, 6, 7)
Generation Condition —	Postive-going input, negative-going input, or any change in state (user-selectable)
Compatible SSR Racks	
Configurations —	8, 16, 24, and 32 input/output lines
Recommended Vendor —	Opto 22 PBXXY (XX varies with the number of lines, Y varies with the configuration; ie. PB24 provides 24 lines with single-density modules, PB24Q provides 24 lines with quad-density modules)
Potential Second Sources —	Crydom MS-XXY Gordos Arkansas PB-XX Potter & Brumfield 2IO-XX Preferred Electronics MSXX (XX varies with the number of lines, Y varies with the configuration) (Contact manufacturer directly)
Mounting Provisions —	6 1-inch threaded standoffs (6-32 screws)
Connectors	
DIB —	60-pin locking header Recommended mating connector: 3M 3334-6060 Amp 1-499662-1 (Connector provided)
SSR Rack Interface —	50-contact, double sided, edge connector Recommended mating connector: 3M 3415-0001 Amp 2-86792-3
Power —	$+5V_{DC} \pm 5\%$, 30 mA (supplied via the DIB) (Power for the SSRs must be supplied to each rack)
Environmental	
Temperature —	CIM-311: −40°C to +85°C (−40°F to +185°F) CIM-311C: 0°C to +70°C (+32°F to +158°F)
Humidity —	0 to 90%, noncondensing
Physical	Length: 14.00 in. (356 mm) Width: 6.59 in. (167 mm) Height: 2.13 in. (54 mm) Weight: 19.8 oz. (562 gm)

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Order Information

CIM-311	Power I/O DIB Board
CIM-311C	0°C to +70°C (commercial version)

Documentation

CIM-311M	CIM-311 and CIM-311C Power I/O DIB Board Hardware Reference Manual (#420306601-001)
CIM-230M	Distributed I/O Bus (DIB) and CIM-230 DIB Interface Board Hardware Reference Manual (#420306595-001)

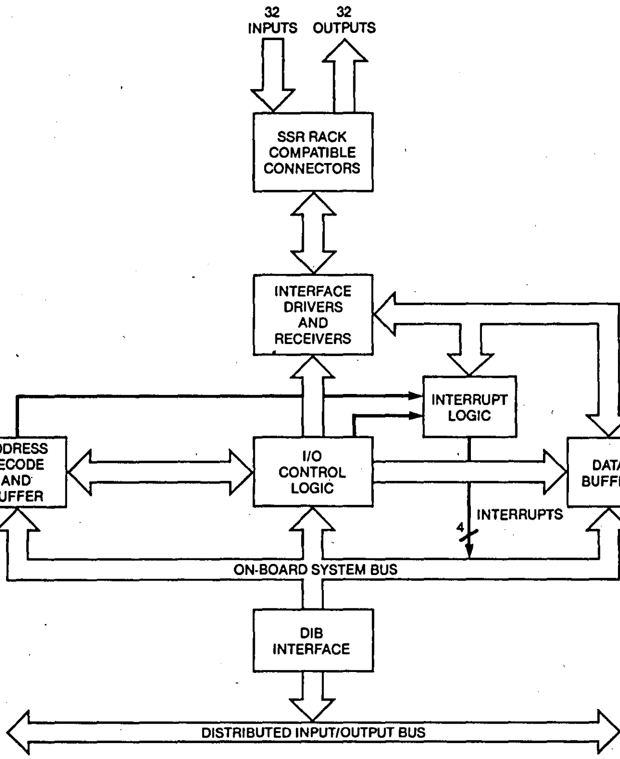

FIGURE 2. CIM-311 Power I/O DIB Board Block Diagram TLT5112-1

National Semiconductor

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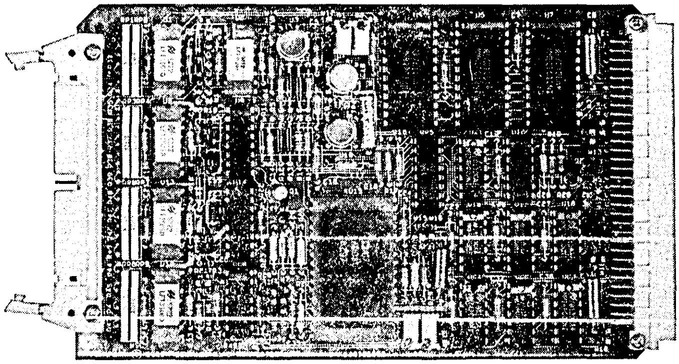
CIM™-411 and CIM-411C Analog Input Boards



- 32 single-ended, 16 differential, or 8 differential and 16 single-ended channels
- CPU program scan control: interrupt, hold, poll, or hold and poll
- Continuously adjustable input ranges between 1 to 2 and 10 to 20, or 4 mA to 20 mA current loop
- 12-bit resolution
- 50 μs conversion time
- microCMOS technology gives high reliability at low power consumption
- −40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges
- CIMBUS™-compatible with SERIES/800™ line
- Small (100 mm × 160 mm) single-wide Eurocard form fits CIM-602/604 card cages
- Built solely with components burned in to A+ levels

Product Overview

The CIM-411 and CIM-411C Analog-To-Digital Converter Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-411 A/D board provides analog-to-digital input for a SERIES/800 system. Under program control, it will bring 12 bits of converted analog data into the system in an interrupt, hold, poll, or hold and poll mode. The CIM-411 is capable of receiving 32 single-ended inputs, 16 differential inputs, or a combination of 8 differential and 16 single-ended inputs. Conversion time is 50 μs with a full-scale input sensitivity selectable in two ranges, ±0.5V to ±0.7V or ±5.0V to ±7.0V differential, or 0.5V to 0.7V or 5.0V to 7.0V

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single-ended; 4mA to 20mA current loop inputs are also supplied. Gain is continuously adjustable from X1 to X2 or X10 to X20. The CIM-411C is identical to the CIM-411, with the only difference being the operating temperature range (0 to +70°C versus −40°C to +85°C).

The CIM-411 shares the small 100 mm × 160 mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fits the CIM-602/604 card cages. It is completely CIMBUS-compatible through a pin-in-socket DIN 41612 connector, which provides an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420306681-001) for a description of the CIMBUS. The CIM-610 Voltage Regulator Board, if used, provides the ±15 V_{DC} power for the A/D converter.

Functional Description

Input Capacity

The CIM-411 supports up to 32 single-ended inputs, 16 differential inputs, or 8 differential and 16 single-ended inputs. The single-ended inputs can be configured for inverting or non-inverting inputs. Via user-installed resistors, the board can also be configured to convert up to 16 current loop inputs.

Gain

Two gain ranges (1 to 2, 10 to 20) for all input channels can be selected by jumpers. The specific gain desired within that range is set by a potentiometer. The input ranges allowed for each gain are tabulated below.

Gain	Single-Ended	Differential
1	0V to 10V	−7V to +7V
2	0V to 5V	−5V to +5V
10	0V to 0.7V	−0.7V to +0.7V
20	0V to 0.5V	−0.5V to +0.5V

Resolution

Full 12-bit resolution is accomplished by a successive approximation analog-to-digital converter. For bipolar operation (differential input), 11 bits plus a sign bit are provided.

Accuracy

High quality components are used to achieve 12-bit resolution with an accuracy of ± 1/2 LSB at 25°C. Offset and gain are adjustable for calibration at any fixed temperature between −40°C and +85°C.

Speed

The A/D conversion speed is 50 μs per channel (typical), including sample-and-hold, settling times, and programming interface. This provides 20,000 samples per second.

Operational Description

The CIMBUS microcomputer board communicates with the CIM-411 A/D board through four I/O ports. Port addresses are I/O-mapped (jumper selectable), and writing channel selection code to port 3 connects the desired analog channel to the amplifier. One bit of the channel selection code word is reserved to start the conversion timing chain.

Port 3 Format

7	6	5	4	3	2	1	0
Start Bit	X	X	← Channel Number →				

X = don't care

The separate start conversion bit allows channel selection and amplification to begin independently of the start of conversion. The start conversion bit can also be used to put the CPU in hold mode during the conversion process. A hardware time delay is initiated before the follow-and-hold circuit is activated to allow channel selection and amplifier settling time. A second hardware timer delay allows the follow-and-hold circuit to settle. The A/D converter then begins its successive approximation conversion process.

An end of conversion signal from the A/D converter latches the digital data from the conversion. The end of conversion signal can also be used to bring the CPU out of hold mode, to generate an interrupt if hold mode was not selected, or to generate a status byte that the CPU can poll to identify when valid data is available. The status byte and latched digital data can then be read from ports 1 (status and four most significant data bits) and 2 (least significant data byte). A subsequent read to port 0 clears the latched data and status byte so that the next conversion can begin. Clearing the data in ports 1 and 2 is not necessary as this data is updated after each conversion.

Port 1 Format

7	6	5	4	3	2	1	0
← Status →				Data 11 (MSB)	Data 10	Data 9	Data 8

Port 2 Format

7	6	5	4	3	2	1	0
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0 (LSB)

Specifications

Analog Input

Scan Mode—	Under CIMBUS CPU program control: interrupt, hold, or hold and poll
Channels—	32 single-ended, 16 differential, or 8 differential and 16 single-ended
Digital Resolution—	12 bits
Full-Scale Voltage Range—	0.5V to 0.7V or 5.0V to 10.0V single-ended, ±0.5V to ±0.7V or ±5.0V to ±7.0V differential (based on amplifier gain)
Current Range—	4 mA to 20 mA (via user-installed 250Ω resistors)
Gain—	Continuously adjustable from X1 to X2 or X10 to X20; range is jumper-selectable
Sample and Hold—	Yes; hold settling time = 5 μs
Throughput Rate—	Up to 20,000 conversions/second
Conversion Speed—	50 μs typical (including sample-and-hold, settling times, and programming interfaces)
Calibration Accuracy—	Adjustable to ±½ LSB
Operating Accuracy—	0.1% full-scale range
Tempco—	$[15 + (50)(\text{Reading}) + \frac{150}{\text{Gain}}]\mu V/^\circ C$ (Referenced to temperature at calibration)
CMRR—	48db minimum >80db typical (at up to ±10V common mode voltage)
Input Impedance—	1 MΩ single-ended or differential
Input Current—	10 mA at ±7V input
Overvoltage Protect—	±15V maximum on analog inputs
Monotonicity—	Guaranteed over the operating temperature range

Digital Output

8 bits of port 2 (LSB), 4 lower bits of port 1 (MSB), 4 upper bits of port 1 (conversion status)

Connectors

Analog Input—	50-pin locking header Recommended mating connector: 3M 3425-6050
CIMBUS—	Pin-in-socket DIN 41612 Recommended mating connectors: Winchester 96S-6033-0531-2 Elco 008257-096-649-124

Power	$+5\ V_{DC}$ @ 125 mA $+15\ V_{DC}$ @ 45 mA $-15\ V_{DC}$ @ 45 mA
Environmental	Temperature: CIM-411: −40°C to +85°C (−40°F to +185°F) CIM-411C: 0 to +70°C (+32°F to +158°F) Humidity: 0 to 90% noncondensing
Physical	Length: 6.30 in. (160 mm) Width: 3.94 in. (100 mm) Height: 0.73 in. (18.5 mm) Weight: 1.5 oz. (41 gm)

Order Information

CIM-411	Analog Input Board
CIM-411C	0 to +70°C (commercial) version

Documentation

CIM-411M	CIM-411 and CIM-411C Analog Input Boards Hardware Reference Manual (#420306590-001)
CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

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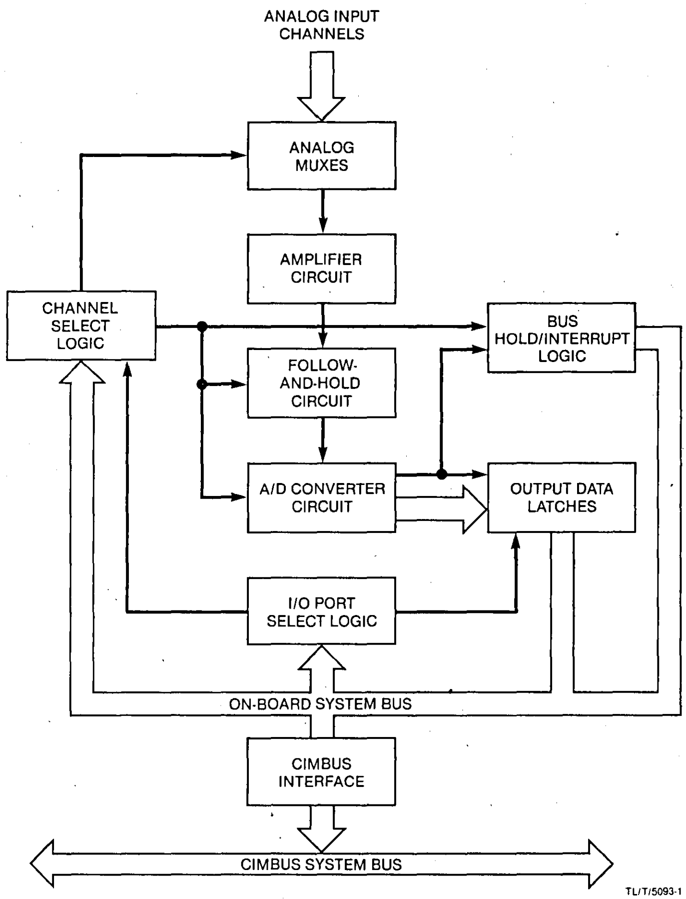
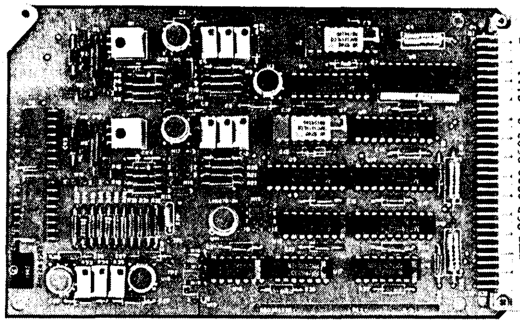


FIGURE 1. CIM-411 Analog Input Board Block Diagram

National Semiconductor

CIM™-421 and CIM-421C Analog Output Boards

microCMOS



- Two output channels
- 12-bit resolution
- Voltage or current-mode outputs
  - —0V to +10V
  - —−10V to +10V
  - —4 mA to 20 mA current loop
- microCMOS technology gives high reliability at low power consumption
- −40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges
- CIMBUS™-compatible with SERIES/800™ line
- Small (100 mm × 160 mm) single-wide Eurocard form fits CIM-602/604 card cages
- Built solely with components burned in to A+ levels

Product Overview

The CIM-421 and CIM-421C Analog Output Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-421 analog output board provides the capability for digital-to-analog output from a CIMBUS system. Under program control of the CIMBUS microcomputer board, it will convert 12 bits of digital data to an analog signal of 0V to +10V, −10V to +10V, or 4 mA to 20 mA on either of two available output channels. The CIM-421C is identical to the CIM-421, with the only difference being the operating temperature range (0 to +70°C versus −40°C to +85°C).

The CIM-421 shares the small 100 mm × 160 mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fits the CIM-602/604 card cages. It is completely CIMBUS compatible through pin-in-socket DIN 41612 connectors, which provide an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420206681-001) for a description of the CIMBUS. The CIM-610 voltage regulator board supplies the +5V and ±15 V_{DC} power for the D/A converter.

Functional Description

The CIM-421 analog output board receives 12-bit data words and converts them to an analog output that can be directed to either of two output channels. The analog output can be unipolar (0V to +10V) or bipolar (−10V to +10V), with the mode of operation determined by on-board jumpers. The output voltage may also be converted to a 4 mA to 20 mA current loop as a jumper-selectable option. The base address for the CIM-421 (factory-set at D0H) is established by jumper connections and may be on any 4-byte boundary in the range from 00H to FCH.

The operation of the CIM-421 may be considered in six major functional units:

- Base address select
- Digital-to-analog converter (DAC) select
- Data bus buffer
- Digital-to-analog converters
- DAC voltage amplifier
- DAC current output

The base address select circuitry decodes the six most significant bits of the CIMBUS address to determine whether the CIM-421 is being addressed. If it is, the base address circuitry also enables the DAC select, data bus buffer, and write pulse to the DAC.

When a valid address is present on the CIMBUS, the DAC select circuitry enables one of the two DACs for operation according to the addressing scheme shown below.

Address	Control Bit = 0	Control Bit = 1	DAC Updated
Base + 0	Load MS 4 Bits and Control Bit		No
Base + 1	Load 12 Bits into DAC 1	Load LS Byte into DAC 1	Yes
Base + 2	Load 12 Bits into DAC 2	Load LS Byte into DAC 2	Yes

Base + 0 Format

7	6	5	4	3	2	1	0
Control Bit	X	X	X	Data 11 (MSB)	Data 10	Data 9	Data 8

X = don't care

Base +1 and Base +2 Format

7	6	5	4	3	2	1	0
Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0 (LSB)

A full 12-bit write to either DAC is accomplished by first writing the most significant four bits (right justified) into Base + 0 with the control bit OFF (logical 0). The lower eight bits are then written into either Base + 1 or Base + 2 (depending upon which DAC is to be updated). Upon completion of this write, the full 12 bits will be written into the selected DAC. If normal operation following this update involves only changing the least significant eight bits, a second write to Base + 0 with the control bit ON (logical 1) will provide 12-bit updates after only a write to Base + 1 or Base + 2. Each DAC has a 12-bit register which holds the data until new data is written by the CPU.

The output from the DACs is a voltage from 0V to 2.5V.

The output of the DAC is then input to a DAC voltage amplifier corresponding to the selected DAC. Here the DAC output is amplified by a factor of 4 for unipolar operation (analog output 0V to + 10V) or by a factor of 8 for bipolar operation (analog output − 10V to + 10V).

If selected (unipolar operation only), the DAC current output circuitry will produce an analog output from 4 mA to 20 mA.

Specifications

Number of Channels— 2

Channel Resolution— 12 bits including sign

Slew Rate— 4V/μs

Accuracy—

Output Range	Absolute Error @ 25°C	Tempco
0V to +10V	1 LSB	0.003% Reading/°C
−10V to +10V	2 LSB	0.006% Reading/°C
4mA to 20mA	2 LSB	0.008% Reading/°C

Monotonicity— Guaranteed over operating temperature range

Digital Input— Unipolar (binary): 0V = 000H; most positive voltage = FFFH
Bipolar (offset binary): most negative voltage = 000H; 0V = 800H; most positive voltage = FFFH

Voltage Output—0V to +10V @ 5 mA; 2.44 mV resolution
−10V to +10V @ 5 mA; 4.88 mV resolution

Current Output—4 mA to 20 mA; 3.9 μA resolution

Current Mode Supply Voltage—10 V_{DC} (0Ω to 500Ω load)
30 V_{DC} (0Ω to 1500Ω load)

Connectors

CIMBUS— Pin-and-socket DIN 41612
Recommended mating connectors:
Winchester 96S-6033-0531-2
Elco 008257-096-649-124

Analog Output— 8-pin, terminal housing
Recommended mating connector:
Molex 22-01-2087
(Connectors provided)

Power +5 V_{DC} ± 5% @ 30 mA
+15 V_{DC} ± 5% @ 25 mA
−15 V_{DC} ± 5% @ 20 mA

Environmental Temperature:
CIM-421: −40°C to +85°C (−40°F to +185°F)
CIM-421C: 0 to +70°C (+32°F to +158°F)
Humidity: 0 to 90% noncondensing

Physical Length: 6.30 in. (160 mm)
Width: 3.94 in. (100 mm)
Height: 0.5 in. (13 mm)
Weight: 4.2 oz. (120 gm)

Order Information

CIM-421 Analog Output Board

CIM-421C 0 to +70°C (commercial) version

Documentation

CIM-421M CIM-421 and CIM-421C Analog Output Boards Hardware Reference Manual (#420306638-001)

CIMBUSM CIMBUS System Specification (#420306681-001)

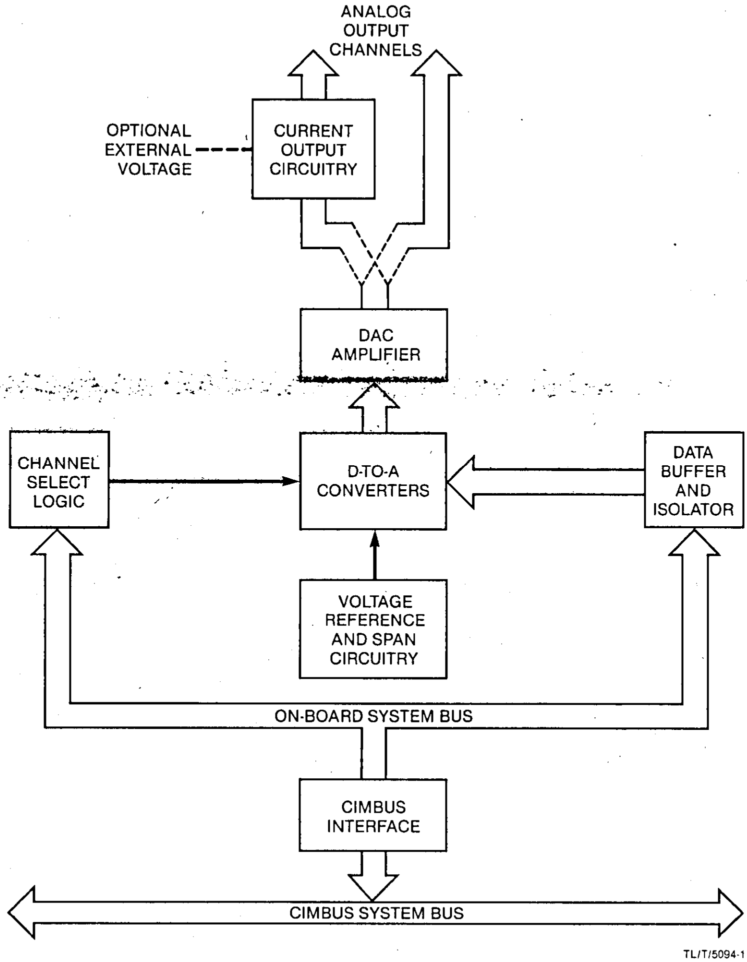


FIGURE 1. CIM-421 Analog Output Board Block Diagram

CIM™-510 and CIM-510C Clock/Calendar Boards

- Real-time clock
  - 10 milliseconds through month counters
  - 24-hour clock
  - 4-year calendar
- Provisions for up to 32K × 8 battery-backed RAM
- Put whole system and/or peripherals in POWER SAVE mode for a, or up to a, specified time
- Battery backup via CIMBUS BAT line or user-installed on-board battery
- Compare and compare/interval interrupts
- CIMBUS™-compatible with SERIES/800™ board line
- Small 100mm × 160mm Eurocard form fits directly into CIM-602/604 card cages
- microCMOS technology gives high reliability with low-power consumption
- −40°C to +85°C or 0°C to +70°C (commercial version) operating temperature ranges
- Built solely with components burned in to A+ levels

Product Overview

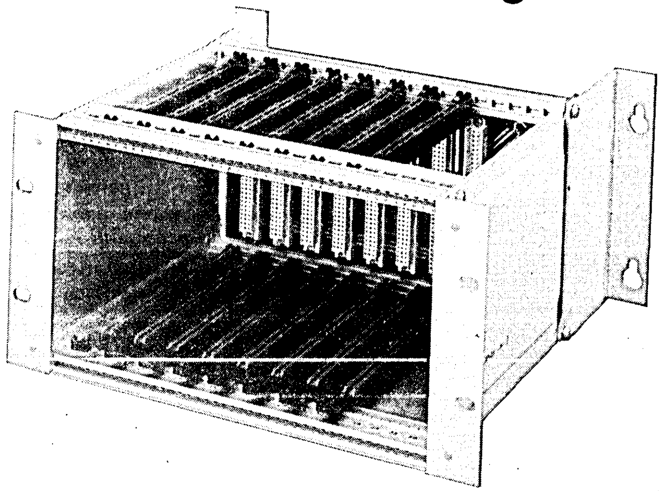
The CIM-510 and CIM-510C Clock/Calendar Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-510 Clock/Calendar Board provides real-time clock, battery-backed RAM, and POWER SAVE functions for a CIMBUS system. The real-time clock features are provided by a MM58167A, and include access to a 24-hour clock with 10 millisecond resolution, and a four-year calendar. A 28-pin socket on the board will support byte-wide static RAMs ranging from 2K×8 to 32K×8. Battery backup for the RAM, and the other critical circuitry on the CIM-510, is either provided by the BAT (battery) line on the CIMBUS, or a user-installed on-board battery. The CIM-510 has the capability to assert the CIMBUS PWRS/(power save) signal, which puts all boards equipped with this feature in a standby mode. Power savings in this mode generally run from 55% to 70%. The board can be programmed to release the system from this mode at a specified time, or after a specified length of time. An external override is also allowed. The CIM-510C is identical to the CIM-510, with the only difference being its operating temperature range (0°C to +70°C, versus −40°C to +85°C).

The CIM-510 shares the small 100 mm×160 mm (3.9″×6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fits the CIM-602/604 card cages. It is completely CIMBUS-compatible through a pin-and-socket DIN 41612 connector, which provides an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420306681-001) for a description of the CIMBUS.

microCMOS

CIM™-602/604 CIMBUS™ Card Cages



- Two versions
  CIM-602: 8 slots, 10.5 inches wide
  CIM-604: 18 slots, 19 inches wide
- Backplane and power supply connectors included
- Prototyping slots included in CIM-604
- Full access to active system components/signals available with CIM-640 Extender Board
- Provisions for front or rear mounting
- NEMA enclosure and RETMA chassis-compatible
- −40°C to +85°C (−40°F to +185°F) operating temperature range
- CIMBUS-compatible with SERIES/800™ line

Product Overview

The CIM-602/604 card cages are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-602/604 card cages are the standard enclosures for SERIES/800 systems. The CIM-602 is 10.5 in. (267 mm) wide and has 8 backplane slots; the CIM-604 is 19 in. (483 mm) wide and has 18 backplane slots. Both versions contain all the power and board connectors required by the CIMBUS specification, both are compatible with NEMA enclosures and RETMA cabinets, and both may be either front or rear mounted. When fully enclosed, both the CIM-602 and CIM-604 provide a rigid, durable, environment-resistant enclosure for a SERIES/800 system.

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Functional Description

The CIM-602/604 card cages are constructed of extruded aluminum and are compatible with NEMA enclosures and RETMA rack-mounting, and may be either front or rear mounted. Both provide connectors for interfaces to regulated or unregulated DC power, batteries, power distribution, and AC status sensing. All boards plug into the backplane via two-piece, pin-in-socket DIN 41612 connectors. The only difference between the CIM-602 and the CIM-604 is that the CIM-602 contains backplane slots for 8 CIMBUS boards while the CIM-604 can accommodate 18 boards.

All external connections to regulated/unregulated DC power, DC power distribution, AC status sensing, alarm relay output, external battery charging voltage, and an external reset pushbutton are made through keyed, pin-in-socket connectors located on the back of the card cage backplane.

Optionally available to support CIMBUS systems is the CIM-610 voltage regulator board. The P1 connector in the card cage is reserved for the CIM-610. The voltage regulator board supplies not only the $+5\ V_{DC}$ and $\pm 15\ V_{DC}$ required by CIMBUS boards but also provides monitoring of the amplitude and frequency of the prime AC power, CPU RAM battery backup power, power-fail sensing circuitry, and support for an external battery in conjunction with the CIM-611 battery charger board.

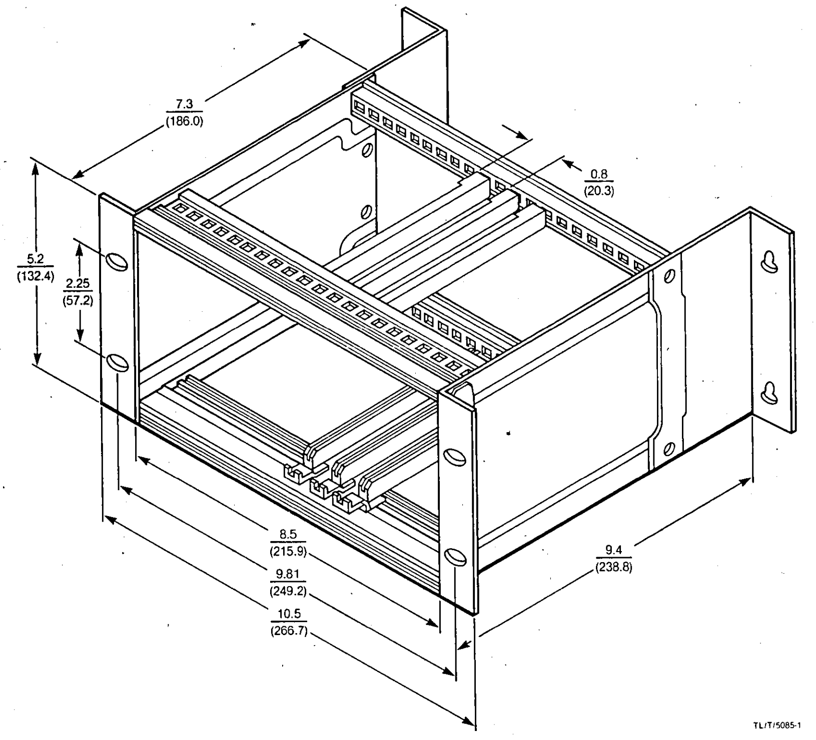

FIGURE 1. CIM-602 Card Cage Dimensions [inches/(millimeters)]

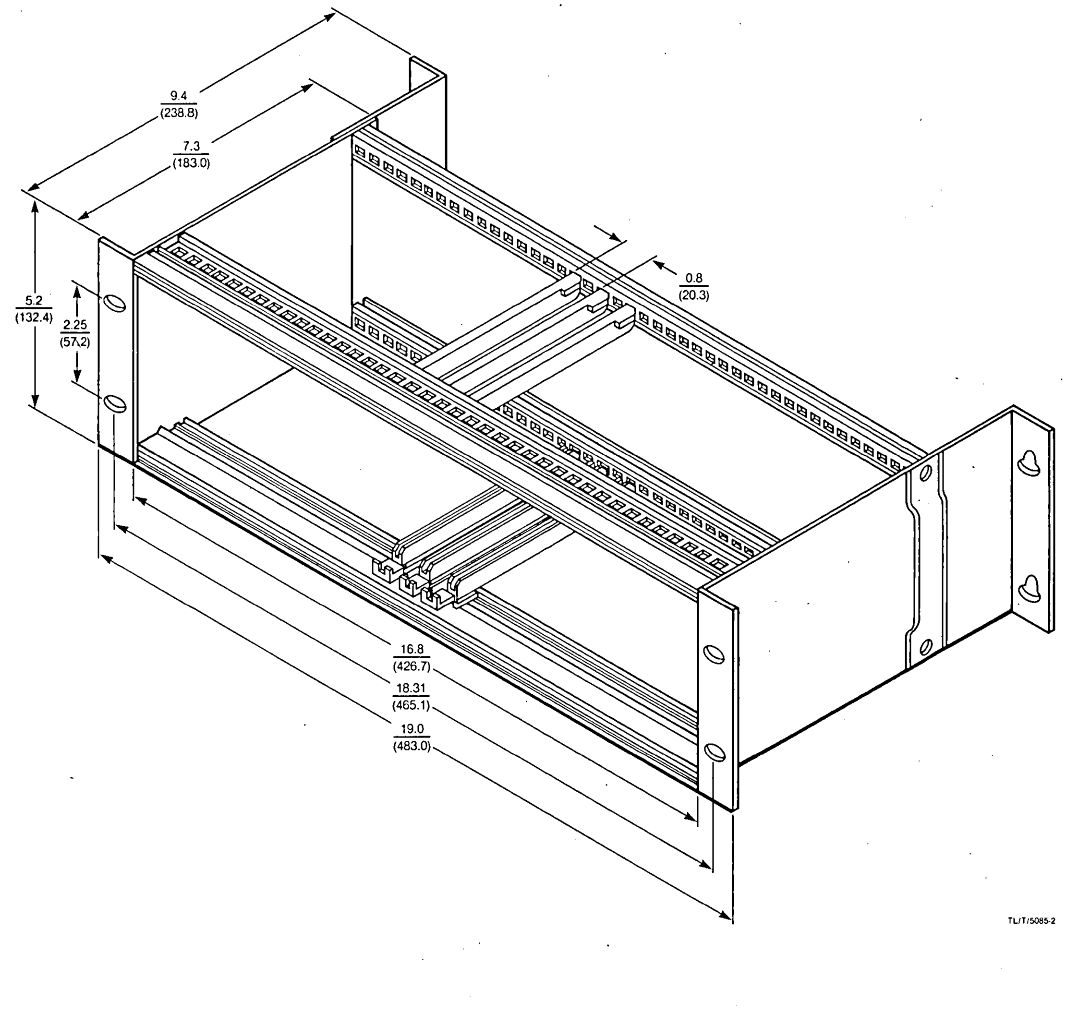

FIGURE 2. CIM-604 Card Cage Dimensions [inches/(millimeters)]

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Specifications

Bus Connectors

CIMBUS— Pin-in-socket DIN 41612
Recommended mating connectors:

Vendor	Male	Female
Winchester	96P-6033-0523-0	96S 6033-0531-2
Elco	008257-096-000-124	008257-096-649-124
Vero	17-2624C	17-2876D

External Voltages— 3, 4 and 6 contact pin-in-socket connectors
Recommended mating connectors:
Molex 03-09-10xx (xx different for each connector)
(Mating connectors are provided with each card cage.)

Environmental Temperature: $-40°C$ to $+85°C$ ($-40°F$ to $+185°F$)
Humidity: to 90% noncondensing

Physical
Height: 5.2 in. (132 mm)
Width: 10.5 in. (267 mm) CIM-602
19.0 in. (483 mm) CIM-604
Depth: 7.3 in. (186 mm) without rear mounting bracket
9.4 in. (239 mm) with rear mounting bracket
Weight: 2.2 lb. (1.0 kg) CIM-602
3.7 lb. (1.7 kg) CIM-604

Order Information

CIM-602 CIM-602 CIMBUS card cage (8 backplane slots)

CIM-604 CIM-604 CIMBUS card cage (18 backplane slots)

Documentation

CIM-602M CIM-602/604 CIMBUS Card Cage Hardware Reference Manual (#420306640-001)

CIMBUSM CIMBUS System Bus Specification (#420306681-001)

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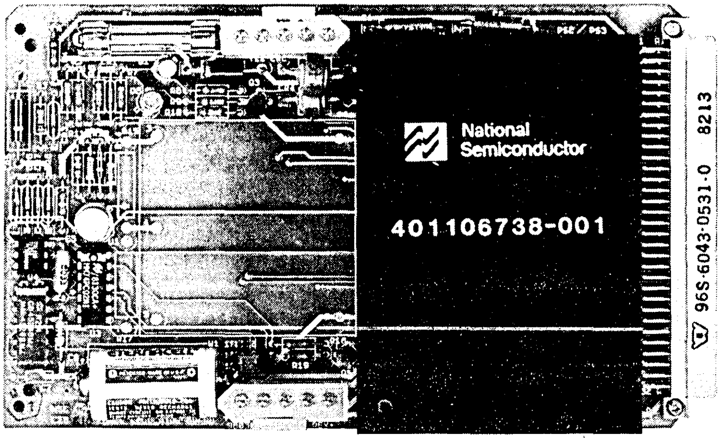
CIM™-610 and CIM-610C Voltage Regulator Boards

microCMOS



- Supplies +5, +15, and −15 V_{DC} to CIMBUS™ interface
- Accepts unregulated DC input from 10.5 to 17.0 volts
- Detects both AC and DC power failures
- Provides RAM backup power from on-board lithium battery
- Self-protects against overloads, transients, and shorts
- Provides connectors for direct mounting of CIM-611 Battery Charger Board
- microCMOS technology gives high reliability at low power consumption
- −40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges
- CIMBUS-compatible with SERIES/800™ line
- Small (100mm × 160mm) single-wide Eurocard form fits CIM-602/604 card cages
- Built solely with components burned in to A+ levels

Product Overview

The CIM-610 and CIM-610C Voltage Regulator Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-610 Voltage Regulator Board, operating on power input from either a system battery or an unregulated DC source in the range from 10.5 to 17.0

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volts, supplies +5, +15, and $-15V_{DC}$ to a SERIES/800 system through the CIMBUS interface. It is entirely self-protected from overloads, transients, or short circuits, and contains both AC and DC power failure detection circuitry. In the event of power failure, the system automatically inhibits any transactions with RAM until the $+5V_{DC}$ power supply is backed up and stable. The CIM-800 CPU Board RAM backup voltage during power failure is provided from an on-board lithium battery. Other elements of the power failure circuitry allow the user to select emergency options such as sounding an alarm, interrupting the CPU, or switching other boards in the CIMBUS system to the Power Save mode. The CIM-610C is identical to the CIM-610, with the only difference being the operating temperature range (0 to +70°C versus −40°C to +85°C).

Connectors are provided so that the CIM-611 Battery Charger Board may be mounted directly on the CIM-610 Voltage Regulator Board. The CIM-611 serves the function of keeping an external system battery fully charged. The CIM-610 and CIM-611 used together provide a virtually uninterruptable power source for a CIMBUS system.

The CIM-610 shares the small 100mm × 160mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fits the CIM-602/604 card cages. It is completely CIMBUS compatible through a pin-in-socket DIN 41612 connector which provides an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420306681-001) for a description of the CIMBUS and the CIM-610/611 Hardware Reference Manual (#420306590-001) for complete descriptions of the CIM-610 Voltage Regulator Board and the CIM-611 Battery Charger Board.

Functional Description

The voltage regulator portion of the CIM-610 Voltage Regulator Board receives power from sources external to the CIMBUS system, either an unregulated DC source in the range from 10.5 to 17.0 volts or a system battery in the event of a power failure. The externally supplied voltage is converted to +5, +15, and $-15V_{DC}$ and distributed to the system via the CIMBUS. Diodes in the power source and battery lines select whichever source is registering the higher voltage. Normally, the DC power source is selected; if the supply voltage drops or fails entirely, the system battery takes over. A fuse, transient suppressor, and capacitor in the power input lines to the voltage regulator protect it from voltage spikes and current overloads.

The CIM-610 contains power failure detect circuitry for both AC and DC sources. Line voltage of either $110V_{RMS}$ at 60 Hz of $220V_{RMS}$ at 50 Hz is stepped down to $12V_{RMS}$ by a user-supplied external filament transformer and input to the power failure circuit. If the sampled AC voltage drops below $8.5V_{RMS}$ (i.e., $85V_{RMS}$ or $170V_{RMS}$) or the AC frequency drops below 45 Hz, the CIM-610 declares an AC power failure. The DC power failure circuit monitors the $+5V_{DC}$ output from the voltage regulator. A DC voltage below 4.8V is considered a power failure.

The actions taken by the CIM-610 in the event of a power failure are jumper-selectable by the user. Available options are generation of a CIMBUS power fail signal, which can be used to trigger the CPU to reset all system outputs and put important data into battery-backed RAM; generation of a CIMBUS power save signal, which will place other elements on the CIMBUS in power save mode; triggering of an external alarm; or some combination of any of these actions.

The CIM-610 also contains a RAM backup circuit that is activated by a power failure. An on-board lithium battery will supply 0.6 Amp-hour of current with less than 0.5mA drawing current. This will support the RAM on the CIM-800 CPU board during the power down time.

The CIM-610 uses the standard CIMBUS form factor (100mm × 160mm), and can therefore be plugged directly into a CIM-602/CIM-604 card cage. The P1 connector/slot in these card cages is reserved for this purpose.

The CIM-611 Battery Charger Board, if installed on the CIM-610 (see *Figure 1*), monitors the external battery voltage and supplies charging current to the external battery at a rate appropriate to its state of discharge.

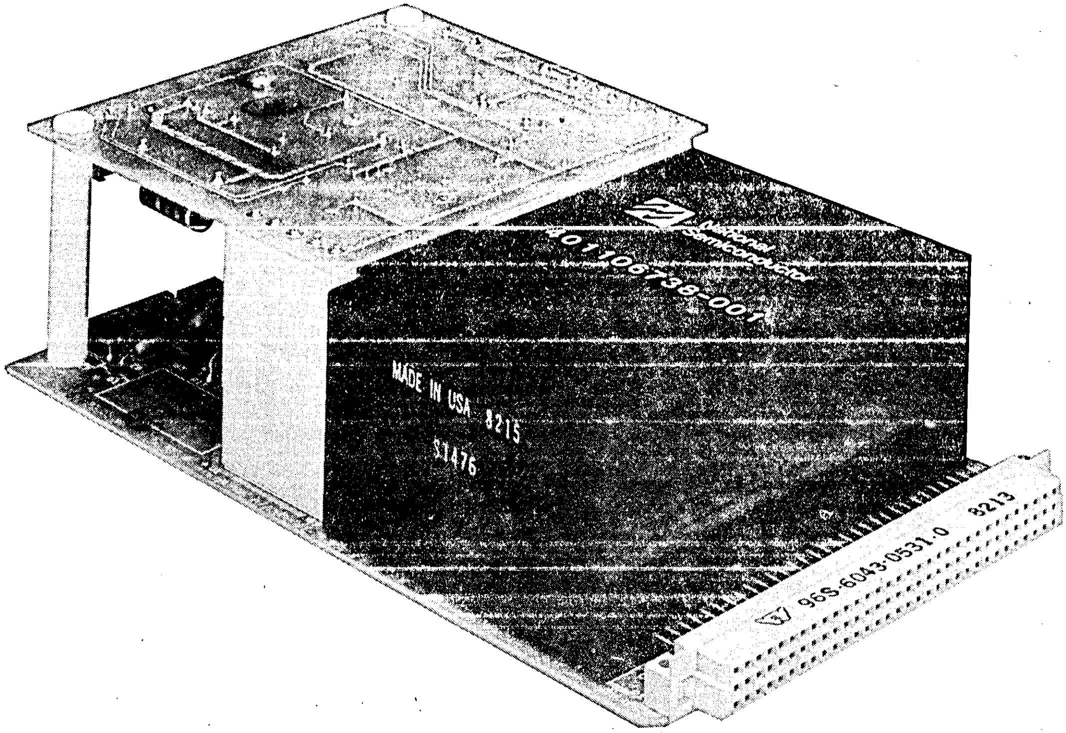

FIGURE 1. CIM-611 Battery Charger Board Installed on the CIM-610 Voltage Regulator Board

Specifications

DC Power Input

Voltage —	+10.5 to 17.0V_{DC}
Current (max.) —	2.0Amp steady state
Startup transient —	12.0Amp for 20μs (full load)
Isolation —	1500V_{DC} galvanic isolation between input and output

External (System) Battery

Voltage —	+10.5 to 17.0V_{DC}
Current (max.) —	2.0Amp steady state
Startup transient —	12.0Amp for 20μs (full load)
Charge rate —	0.3Amp fast charge; 20mA trickle charge
Recommended source —	Gates Energy Products, Inc. 12V_{DC} Sealed Lead Acid Battery Model No. 0800-0008GG

RAM (On-Board) Backup

Type —	Nonrechargeable lithium
Voltage —	+2.8V_{DC}
Maximum Continuous Current —	0.5mA
Capacity —	0.6Amp-hour at −40°C to +25°C 0.4Amp-hour at +85°C
Shelf Life —	10 years

AC Power Input

Voltage —	8.5 to 13.0V_{RMS}
Frequency —	45-60Hz
Recommended filament transformer —	Stancor P-8683 (60Hz)

External Alarm Interface

Open Circuit Voltage —	24V_{DC} maximum
Current Sinking —	200mA maximum

DC Power Output

	+5V_{DC}	+15V_{DC}	−15V_{DC}
Tolerance (Steady State)	±200mV	±200mV	±200mV
Ripple (RMS)	15mV	2mV	2mV
Current (−20°C to +70°C)	1.50A	200mA	200mA
(−40°C to −20°C and +70°C to +85°C)	0.75A	100mA	100mA

Connectors

CIMBUS — Pin-and-socket DIN 41612
Recommended mating connectors:
Winchester: 96P-6033-0523-0
Elco: 008257-096-000-124

Environmental

Temperature:
CIM-610: −40°C to +85°C (−40°F to +185°F)
CIM-610C: 0 to +70°C (+32°F to +158°F)
Humidity: 0 to 90% noncondensing

Physical

Length	6.30 in.	(160 mm)
Width	3.94 in.	(100 mm)
Height	1.97 in.	(50 mm)
Weight	4.3 oz.	(121 gm)

Order Information

CIM-610	Voltage Regulator Board
CIM-610C	0 to +70°C (commercial) version

Documentation

CIM-610M	CIM-610 and CIM-610C Voltage Regulator Boards CIM-611 and CIM-611C Battery Charger Boards Hardware Reference Manual (#420306590-001)
CIMBUSM	CIMBUS System Specification (#420306681-001)

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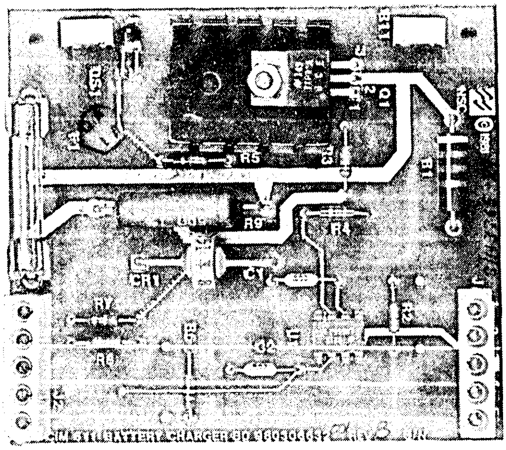
CIM™-611 and CIM-611C Battery Charger Boards



- Mounts directly on CIM-610 Voltage Regulator Board
- Automatically adjusts charge current to state of battery discharge
- Two charge rates — trickle and "fast"
- Temperature compensated charge rate across temperature range
- −40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges
- Built solely with components burned in to A+ levels

Product Overview

The CIM-611 and CIM-611C Battery Charger Boards are members of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-611 Battery Charger Board mounts directly on the CIM-610 Voltage Regulator Board and requires only a single $+24V_{DC}$ power supply. It monitors the state of discharge of the external system battery and automatically provides a fast or trickle charge as required. The use of the CIM-611 and an external battery in conjunction with the CIM-610 Voltage Regulator Board creates an effectively uninterruptable system power supply. The CIM-611C is identical to the CIM-611, with the only difference being the operating temperature range (0 to +70°C versus −40°C to +85°C). See the CIM-610/611 Hardware Reference Manual (#420306590-001) for a complete description of the CIM-610 Voltage Regulator Board and CIM-611 Battery Charger Board.

Functional Description

The CIM-611 Battery Charger Board mounts directly on the CIM-610 Voltage Regulator Board, and all connections to the CIM-611 are made through the

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CIM-610. The CIM-611 charges the external system battery, automatically adjusting the charge current according to the battery's state of discharge.

An external +24 V_{DC} power supply provides the charging current for the CIM-611. The CIM-611 constantly monitors the battery voltage and compares it to a +15 V_{DC} reference generated by the CIM-610. If the battery voltage is greater than 14.8V, the battery is considered to be charged, and only trickle charge current flows. If the battery voltage drops below 13.8V, the charge rate switches to fast and remains in that condition until the battery voltage again reaches 14.8V.

Fast charge current as established during manufacture is 0.3 Amps; however, the user can increase the fast charge rate to 1.0 Amps by adding a "fast charge" resistor in parallel with a series resistor in the +24 V_{DC} input line.

The CIM-611 is factory-set to switch to fast charge at a battery output voltage of 13.8V_{DC} at 25°C, and back to trickle charge at 14.8V_{DC} at 25°C. On-board potentiometers allow the user to alter these adjustments if necessary. As the temperature changes, on-board temperature compensation circuitry automatically adjusts these trip points at a 18mV/°C rate (increasing temperatures lower the trip points).

The CIM-611 accommodates batteries with a voltage range of 10.5 to 14.8V and the ability to accept charge current at the rate of 0.3 Amps.

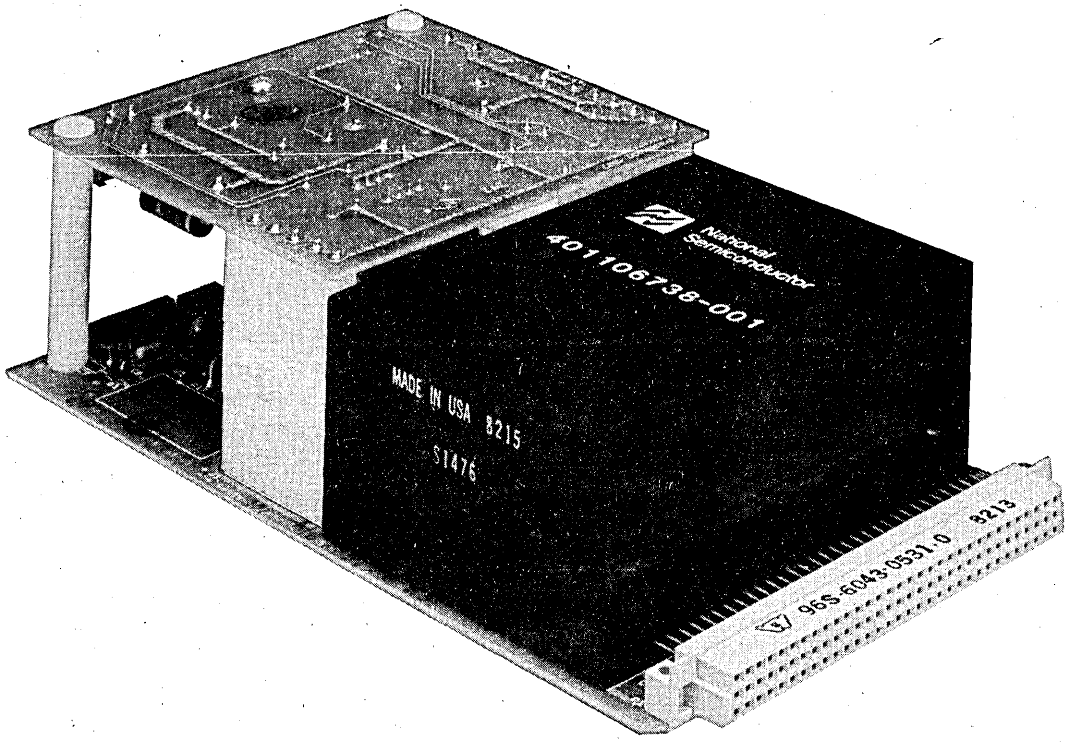

FIGURE 1. CIM-611 Battery Charger Board Installed on the CIM-610 Voltage Regulator Board.

Specifications

External Battery

Voltage —	+10.5 to 17.0 V_{DC}
Current (max.) —	2.0 Amp steady state
Startup transient —	12.0 Amp for 2.0 μs (full load)
Charge rate —	0.3 Amp fast charge; 20 mA trickle charge
Recommended source —	Gates Energy Products, Inc. 12 V_{DC} Sealed Lead Acid Battery Model No. 0800-0008GG

+24 V_{DC} Input

Voltage range —	23.0 to 28.0 V
Current (max.) —	0.3 Amp without "fast charge" resistor 1.0 Amp with "fast charge" resistor

Battery Charging Output

Voltage range —	+10.5 to +14.8 V
Current (max.) —	0.3 Amp without "fast charge" resistor 1.0 Amp with "fast charge" resistor
Trip Points —	Trickle to fast at 13.8 V_{DC} at 25°C Fast to trickle at 14.8 V_{DC} at 25°C (User adjustable)
Temperature Compensation —	−18mV/°C

Environmental

Temperature:
CIM-611: −40°C to +85°C (−40°F to +185°F)
CIM-611C: 0 to +70°C (+32°F to +158°F)

Humidity: 0 to 90% noncondensing

Physical

Length	3.25 in.	(83 mm)
Width	3.66 in.	(93 mm)
Height	1.19 in.	(30 mm)
Weight	0.5 oz.	(13 gm)

Order Information

CIM-611	Battery Charger Board
CIM-611C	0 to +70°C (commercial) version

Documentation

CIM-610M	CIM-610 and CIM-610C Voltage Regulator Boards CIM-611 and CIM-611C Battery Charger Boards Hardware Reference Manual (#420306590-001)
CIMBUSM	CIMBUS System Specification (#420306681-001)

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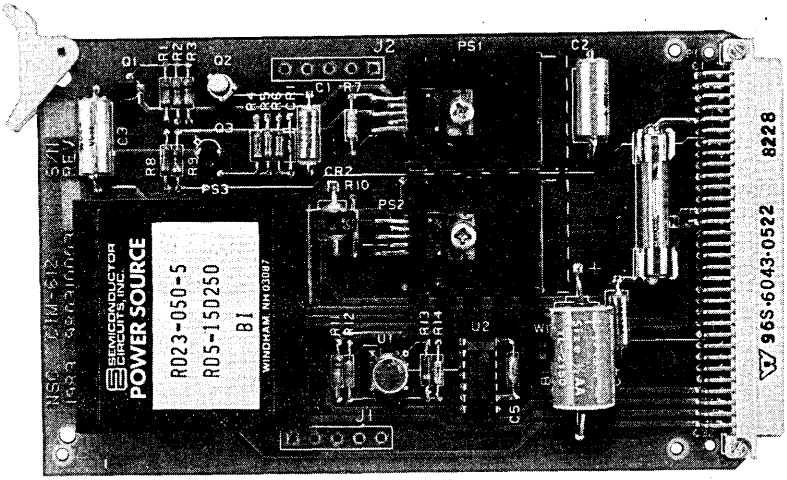
CIM™-612 and CIM-612C Voltage Regulator Boards



- Supplies +5, +15, and −15 V_{DC} to CIMBUS™ interface
- Accepts unregulated DC input from 5.5 to 8.0V
- Detects DC power failures
- Provides RAM backup power from on-board lithium battery
- Self-protects against overloads, transients, and shorts
- microCMOS technology gives high reliability at low power consumption
- −40°C to +85°C or 0 to +70°C (commercial version) operating temperature ranges
- CIMBUS compatible with SERIES/800™ line
- Small (100mm x 160mm) single-wide Eurocard form fits CIM-602/604 card cages
- Built solely with components burned in to A+ levels

Product Overview

The CIM-612 and CIM-612C Voltage Regulator Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-612 Voltage Regulator Board, operating on power input from an unregulated DC source in the range from 5.5 to 8.0V, supplies +5, +15, and −15 V_{DC}

to a SERIES/800 system through the CIMBUS interface. It is entirely self-protected from overloads, transients, or short circuits, and contains DC power failure detection circuitry. In the event of power failure, the system automatically inhibits any transactions with RAM until the +5 V_{DC} power supply is backed up and stable. The CIM-800 CPU Board RAM backup voltage during power failure is provided from an on-board lithium battery.

The CIM-612C is identical to the CIM-612, with the only difference being the operating temperature range (0 to +70°C, versus −40°C to +85°C). Both share the small 100mm × 160mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fit the CIM-602/604 card cages. They are completely CIMBUS compatible through a pin-in-socket DIN 41612 connector which provides an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420306681-001) for a description of the CIMBUS and the CIM-612/612C Hardware Reference Manual (#420310003-001) for a complete description of the CIM-612 Voltage Regulator Board.

Functional Description

The voltage regulator portion of the CIM-612 Voltage Regulator Board receives power from an external, unregulated DC source in the range from 5.5 to 8.0V. The voltage is converted to +5, +15, and −15 V_{DC} and distributed to the system via the CIMBUS. A fuse, transient suppressor, and capacitor in the power input lines to the voltage regulator protect it from voltage spikes and current overloads.

A DC power failure detection circuit on the board monitors the output of the 5 V_{DC} regulator. A DC voltage below 4.5V is considered a power failure. When this happens, the CPU is informed by an interrupt. This allows the CPU to place the system in a safe/known condition, and store vital data in battery-backed RAM. After the interrupt (ranges from tens to hundreds of milliseconds depending on the external DC power source and the load on the CIM-612), the CIM-612 inhibits all transactions with RAM in the system to prevent data from being scrambled by noise potentially generated during the power down/up sequence.

The CIM-612 also contains a RAM backup circuit that is activated by a power failure. An on-board lithium battery will supply 0.6 Amp-hour of current with less than 0.5mA drawing current. This will support the RAM on the CIM-800 CPU board during the power down time.

The CIM-612 uses the standard CIMBUS form factor (100mm × 160mm), and can therefore be plugged directly into a CIM-602/CIM-604 card cage. The P1 connector/slot in these card cages is reserved for this purpose.

Specifications

DC Power Input

Voltage —	+5.5 to 8.0 V_{DC}
Current (max.) —	1.0 Amp steady state
Startup transient —	2.0 Amp for 1 sec (full load)

RAM (On-Board) Backup

Type —	Nonrechargeable lithium
Voltage —	+3.4 V_{DC}
Maximum Continuous Current —	0.5 mA
Capacity —	0.63 Amp-hour across full temperature range
Shelf Life —	10 years

DC Power Output

	$+5V_{DC}$	$+15V_{DC}$	$-15V_{DC}$
Tolerance (Steady State) —	±200mV	±200mV	±200mV
Ripple (RMS) —	15mV	2mV	2mV
Current —	0.5A	100mA	100mA

Connectors

CIMBUS —	Pin-and-socket DIN 41612 Recommended mating connectors: Winchester: 96P-6033-0523-0 Elco: 008257-096-000-124

Environmental

Temperature:

CIM-612:	−40°C to +85°C (−40°F to +185°F)
CIM-612C:	0 to +70°C (+32°F to +158°F)
Humidity:	0 to 90% noncondensing

Physical

Length: 6.30 in. (160 mm)
Width: 3.94 in. (100 mm)
Height: 1.97 in. (50 mm)
Weight: 7.0 oz. (198 gm)

Order Information

CIM-612	Voltage Regulator Board
CIM-612C	0 to +70°C (commercial) version

Documentation

CIM-612M	CIM-612/612C Voltage Regulator Board Hardware Reference Manual (#420310003-001)
CIMBUSM	CIMBUS System Specification (#420306681-001)

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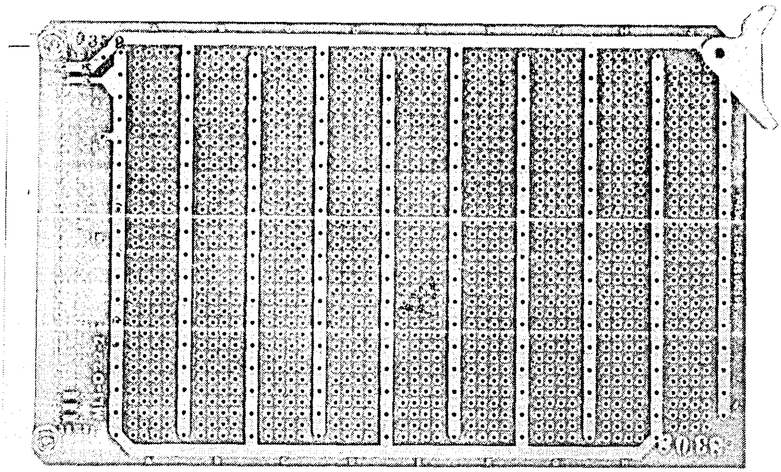
CIM™-630 Prototyping Board



- Permits addition of user-designed circuitry to a CIMBUS™ system
- Capacity for 32 16-pin DIPs
- Plugs directly into CIM-602/604 card cages

Product Overview

The CIM-630 Prototyping Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-630 Prototyping Board, with a capacity of up to 32 16-pin DIPs, is a convenient, economical way for CIMBUS system users to include their own custom-designed circuitry. Completely compatible with the CIM-602/604 card cages, it plugs directly into the user's system.

Physical Description

The CIM-630 Prototyping Board accepts up to 32 16-pin DIPs or an equivalent mix of 14-, 16-, 18-, 22-, 24-, 28-, and 40-pin configurations. It has a pin-in-socket DIN 41612 connector built in, and plugs directly into the CIM-602/604 card cages.

Specifications

Connectors	Pin-and-socket DIN 41612 Recommended mating connectors: Winchester 96S-6033-0531-2 Elco 008257-096-649-124		
Environmental	Temperature:	-40°C to +85°C (-40°F to +185°F) (Assumes user-installed circuitry meets this specification.)	
	Humidity:	0 to 90% noncondensing	
Physical	Length:	6.30 in.	(160 mm)
	Width:	3.94 in.	(100 mm)
	Height:	0.90 in.	(23 mm)
	Weight:	0.50 oz.	(14 gm)

Order Information

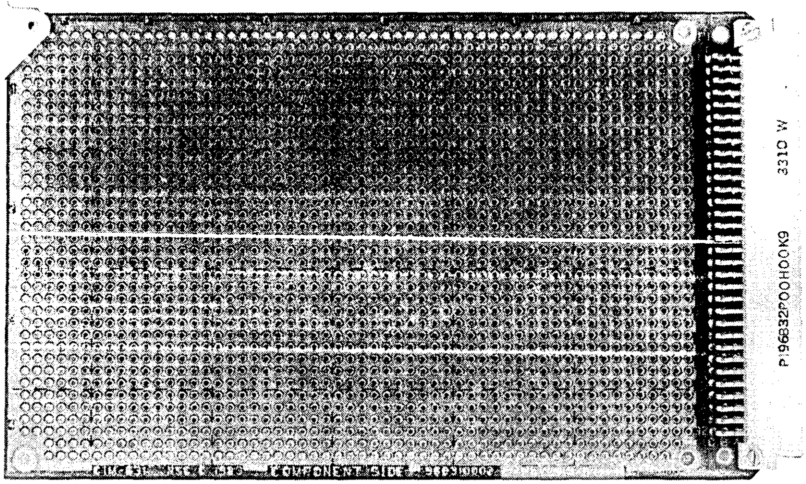
CIM-630	Prototyping Board

Documentation

CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

microCMOS

CIM™-631 Prototyping Board



- Permits addition of user-designed circuitry to a CIMBUS™ system
- Capacity for 63 16-pin DIPs
- Plugs directly into CIM-602/604 card cages

Product Overview

The CIM-631 Prototyping Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-631 Prototyping Board, with a capacity of up to 63 16-pin DIPs, is a convenient, economical way for CIMBUS system users to include their own custom-designed circuitry. Completely compatible with the CIM-602/604 card cages, it plugs directly into the user's system.

Physical Description

The CIM-631 Prototyping Board accepts up to 63 16-pin DIPs or an equivalent mix of 14-, 16-, 18-, 22-, 24-, 28-, and 40-pin configurations. It has a pin-and-socket DIN 4612 connector built in, and plugs directly into the DIM-602/604 card cages.

The primary difference between the CIM-631 and the CIM-630 is that the CIM-631 does not have power and ground traces throughout the board (as does the CIM-630). In comparison to the CIM-630, this increases the amount of wirewraps which must be made, but also results in nearly double the number of devices which may be installed. It also allows these devices to be placed "on grid", to match the production version of the design prototyped on the CIM-631.

Specifications

Connectors

Pin-and-socket DIN 41612

Recommended Mating Connectors:

Winchester 96S-6033-0531-2

Elco 008257-096-649-124

Environmental

Temperature:	– 40°C to + 85°C (– 40°F to + 185°F) (Assumes user-installed circuitry meets this specification.)
Humidity:	0 to 90% noncondensing

Physical

Length:	6.30 in.	(160 mm)
Width:	3.94 in.	(100 mm)
Height:	0.90 in.	(23 mm)
Weight:	0.50 oz.	(14 gm)

Order Information

CIM-631	Prototyping Board

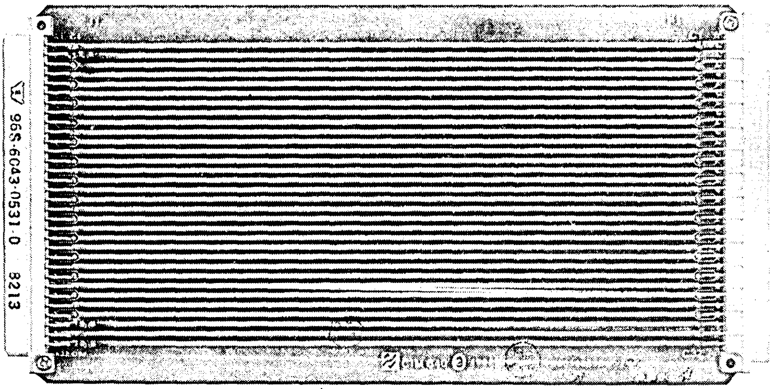
Documentation

CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

National Semiconductor

microCMOS

CIM™-640 Extender Board



- **Complete access to a CIMBUS™ board for troubleshooting or debugging**
- **Power isolation allows removal/insertion of boards without loss of data or functions as well as current measurement in a powered system**
- **Easily accessible test points for fast examination of bus and control signals**

Product Overview

The CIM-640 Extender Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-640 Extender Board provides a means of extending CIMBUS boards away from the CIM-602/604 card cage to permit testing and debugging. Test points for examining bus and control signals are easily accessible, and the power lines contain jumpered openings for power removal at the extender board.

Physical Description

The CIM-640 Extender Board offers the SERIES/800 user the means to extend boards beyond the card cage for testing and debugging. Test points for bus and control signals are easily accessible.

In addition, the power traces on the CIM-640 have jumpered openings so that user can remove power at the board under examination rather than having to power down an entire system. The jumpered points in the power traces can also be used to insert instrumentation to measure the current to a board under power.

Specifications

Connectors Pin-and-socket DIN 41612
Recommended mating connectors:

Vendor	Backplane	Board
Winchester	96P-6033-0523-0	96S-6033-0531-2
Elco	008257-096-000-124	008257-096-649-124

Environmental Temperature: -40° C to +85° C (-40° F to +185° F)
Humidity: 0 to 90% noncondensing

Physical
Length: 7.30 in. (185 mm)
Width: 3.94 in. (100 mm)
Height: 0.50 in. (13 mm)
Weight: 0.50 oz. (14 gm)

Order Information

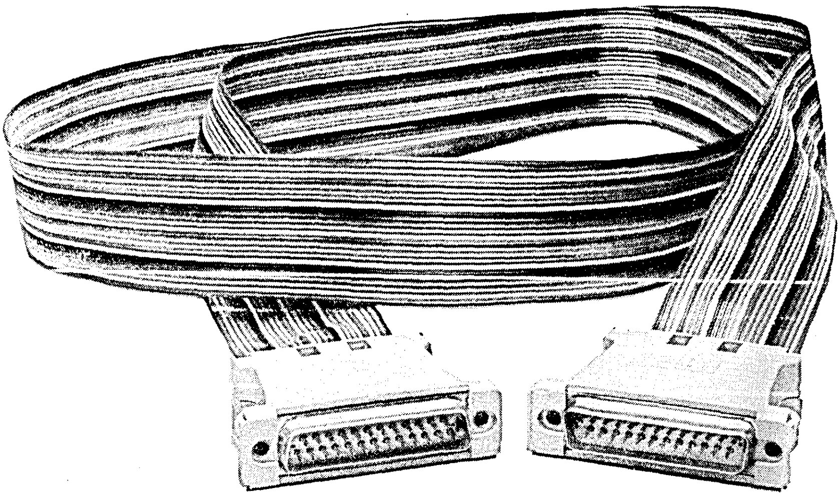
CIM-640 Extender Board

Documentation
CIMBUSM CIMBUS System Bus Specification (#420306681-001)

National Semiconductor

microCMOS

CIM™-653 Serial I/O Cable



- Allows instant addition of a RS232C or 20mA current loop device to a CIMBUS™ system
- Compatible with the CIM-201 Serial I/O Board
- Supports full 25-line interface

Product Overview

The CIM-653 Serial I/O Cable is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-653 Serial I/O Cable is a convenient way for CIMBUS system users to add a serial device to their system. It is fully compatible with the CIM-201 Serial I/O Board, and therefore, supports interfaces to terminals, modems, or any device compatible with RS232C or 20 mA current loop serial links.

Physical Description

The CIM-653 Serial I/O Cable is a ribbon cable 48 inches (122 cm) long (including the connectors). Both connectors are male, 25-pin "D" connectors. All 25 lines defined by EIA RS232C are included, with each line tied to the same pin on each connector (i.e., pin 1 to pin 1, pin 2 to pin 2, etc.).

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Specifications

Connectors
Standard DB25P
Recommended Mating Connector: Standard DB25S

Environmental	Temperature: 0°C to +70°C (+32°F to +158°F) Humidity: 0 to 90% noncondensing
Physical	Length: 48 in. (122 mm) Weight: 3.8 oz. (108 gm)

Order Information

CIM-653	Serial I/O Cable (compatible with CIM-201 Serial I/O Board)

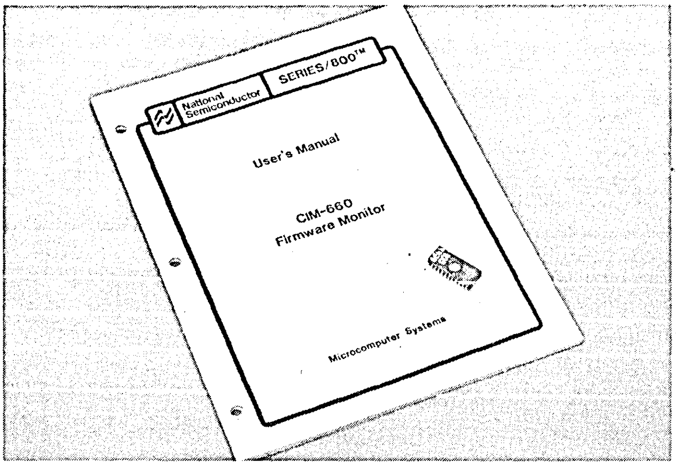
Documentation

CIM-201M	CIM-201 Serial I/O Board Hardware Reference Manual (#420306683-001)

National Semiconductor

microCMOS

CIM™-660 Firmware Monitor



- Single-chip system monitor for CIM-800 boards
- Display contents of memory or processor registers
- Modify contents of memory or processor registers
- Modify user programs dynamically
- Upload and download hex files
- Move blocks of data
- Perform hexadecimal arithmetic
- Search memory for specified data byte
- Execute user programs from monitor
- Insert breakpoints in user programs
- Input or output a byte of data
- Resides in a single NMC27C32 EPROM

Product Overview

The CIM-660 Firmware Monitor is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-660 Firmware Monitor is a single-chip (EPROM) system monitor that plugs into a socket provided on the CIM-800 Series Boards. Containing a complete software system, the CIM-660 provides the user all the functions usually associated with a microcomputer system monitor or debugging program and allows interactive program modification, testing, and execution.

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Functional Description

The CIM-660 Firmware Monitor is a single-chip, self-contained system monitor and software debugging program that gives the user the capability to modify, test, and execute his programs interactively with a CIM-800 Microcomputer system. Input is made from a keyboard, and output may be routed to either a CRT display or a printer.

After the system is powered up, the baud rate is established by repeatedly pressing the RETURN key on the CRT display until the following message appears:

```
CIM-800 MONITOR REV. B
>
```

When the caret prompt (>) appears, the CIM-660 is in a command interpret mode, ready to accept a system command from the user. Commands then available are:

DISPLAY	Displays contents of memory between two specified addresses in hexadecimal and ASCII
EXAMINE REGISTERS	Examine and modify CPU registers
FIND	Searches memory between two specified addresses for a specified byte
GO	Transfers control to a specified address
INPUT	Displays the contents of input ports between two specified addresses
MOVE	Moves a specified block of data to a specified destination address
OUTPUT	Outputs a specified byte to a specified output port
READ	Input a hex file over a serial link
SUBSTITUTE	Examine and modify the contents of a specified memory address
VERIFY	Used after a MOVE command to verify that the move was made
WRITE	Output a hex file over a serial link
+	Add two 16-bit hexadecimal numbers
−	Subtract a 16-bit hexadecimal number with a second 16-bit number
*	Multiply two 16-bit hexadecimal numbers
/	Divide a 32-bit hexadecimal number by a 16-bit number

Specifications

Memory Requirements

PROM Address Space 0000H-0FFFH

Environmental

Temperature:	-40°C to +85°C (-40°F to +185°F)
Humidity	0 to 90% noncondensing

Hardware Requirements

CIM-800	CPU Board
CIM-201	Serial I/O Board
CIM-602/604	Card Cage (or equivalent)
CIM-653	RS232 Serial I/O Cable Assembly (or equivalent)
CIM-610	Voltage Regulator Board (or other supply of $+5V_{DC}$ and $+15V_{DC}$)

Video Display Terminal (or equivalent)

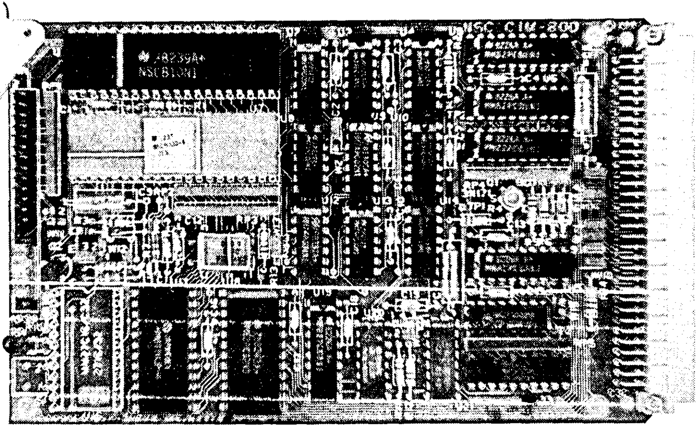
Order Information

CIM-660 Firmware Monitor

Documentation

CIM-660M	CIM-660 Firmware Monitor User's Manual (#420306641-001)
CIMBUSM	CIMBUS System Bus Specification (#420306681-001)

CIM™-802A/804 and CIM-802AC/804C Industrial Microcomputers



- NSC800™-based computer board
- microCMOS technology gives NMOS performance at CMOS power consumption levels
- NSC800 CPU—more than 158 instruction types programmable in Z80 code
- 4 MHz or 2 MHz operation in harsh environments
- −40°C to +85°C or 0°C to +70°C (commercial version) operating temperature ranges
- Battery backup/operation
- 2 16-bit counters/timers with prescalers
- 22 programmable I/O lines
- System-level fail-safe timer
- 2K bytes static RAM; 2K or 4K bytes PROM with "shadow" capability under software control
- 12 vectored interrupts
- Built solely with components burned in to A+ levels

Product Overview

The CIM-802A/804 and CIM-802AC/804C Microcomputer Boards are members of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the microCMOS NSC800 microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80 instruction set. The complete line is compatible with the CIMBUS™, a documented scheme for board interconnnection (see the CIMBUS specification). The microCMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-802A, CIM-804, CIM-802AC, and CIM-804C are the board level computers that are the heart of the SERIES/800 CMOS Industrial Microcomputer board line. Featuring NSC's microCMOS technology, these computers provide highly reliable performance over a wide range of harsh environmental conditions at low power consumption, and is eminently suitable for remote station and process control applications.

These are complete computers based on the NSC800 central processing unit, and include 22 programmable I/O lines, twelve priority vectored interrupts, 2K bytes of static RAM, provisions for 2K or 4K bytes of ROM, and two 16-bit programmable timers. The NSC800 CPU, which is programmable in Z80 code, has an instruction set containing more than 158 instruction types. The CPU board is easily expandable via the CIMBUS for operation with other products in the SERIES/800 line, such as memory expansion, A/D and D/A conversion, serial I/O, and a battery charger. See the CIMBUS specification manual for a description of CIMBUS characteristics (order as CIMBUSM or Manual #420306681-001).

Power consumption of the computer is very low (magnitudes less than equivalent NMOS functionality), which results in increased reliability and eliminates the need for separate cooling fans and filtering systems. CIMBUS connections are made through two-piece, pin-in-socket DIN 41612 connectors, which are highly resistant to vibration and corrosion, and eliminate the card edge connector, a primary failure source in many systems. The CPU board is small, measuring only 100 mm x 160 mm (3.9″ x 6.3″), and fits into the CIM-602 (8-slot) or CIM-604 (18-slot) CIMBUS card cages to make a tidy, durable system.

The CIM-802A and CIM-804 are functionally identical with the exception of their operating speeds: the CIM-802A executes at 2 MHz (minimum instruction execution time of 2 microseconds), the CIM-804 executes at 4 MHz (1 microsecond minimum instruction execution time). The CIM-802AC and the CIM-804C are functionally identical to the CIM-802A and the CIM-804, with the only difference being their operating temperature range (0°C to +70°C, versus −40°C to +85°C).

Functional Description

Central Processor

- CPU—NSC800 microprocessor
- Maximum addressing range—64K bytes
- Data word—8 bits
- Instruction word—8, 16, or 24 bits
- Addressing modes—direct, register, indexed register, register indirect, and immediate
- Instruction types—more than 158, programmable in Z80 code
- Registers
  - 14 general purpose, A, B, C, D, E, H, and L and A', B', C', D', E', H', and L'; A (accumulator) and F (flag), A' and F' selected separately. Other registers may be used singly or in pairs; AF, BC, DE, HL and A'F', B'C', D'E', H'L'.
  - 2 16-bit index register pairs IX and IY may be indexed ±255 from symbolic location
  - 1 16-bit program counter (PC)
  - 1 16-bit stack pointer (SP) used discretely or automatically to implement subroutine CALL and RETurn instructions
  - 1 8-bit refresh register (R)
  - 1 8-bit interrupt register (I)

Memory

The 2K private static RAM (6116) is a byte-wide, low power device requiring only a few microwatts to retain data, and uses special write inhibit logic to protect its contents in a power-down or standby mode. An additional 128 bytes of RAM are available from the NSC810 RAM I/O Timer. The 2K static RAM is mapped at addresses F000H-F7FFH; the additional 128 bytes at F800H-F87FH.

Sockets are provided on the CPU board for either the 27C16 (2K bytes) or the 27C32 (4K bytes) EPROM. Two Berg jumpers provide all the logic changes necessary for using either type of EPROM. Assigned addresses for ROM are 0000H-07FFH (27C16) or 0000H-0FFFH (27C32). The PROM may be turned off (shadowed), under software control, to allow using memory mapped into the same space. This provides a convenient way to "bury" diagnostics and/or bootloaders.

Memory expansion to a maximum of 64K bytes is possible using the CIM-100 Series Memory Expansion Boards.

Input/Output

All on-board input/output functions are memory-mapped through the NSC810 RAM I/O Timer with a base address of F8XXH.

- Interrupts—arbitrated through a priority interrupt controller
  - 1 nonmaskable interrupt
  - 3 restart maskable interrupts available to user
  - 8 priority vectored interrupts
- Three programmable I/O ports
  - Port A, 8 lines available to user
  - Port B, 8 lines, 4 generally reserved for CPU board use
  - Port C, 6 lines, 2 generally reserved for CPU board use

  (Some system configurations may allow use of all 22 I/O lines. I/O pin-out is different than CIM-802.)
- Timers
  - 2 16-bit programmable counters/timers; timer prescale 1/2/64 (64 on timer TO only)
  - 8 ms and 0.5 second timers jumperable as interrupts

Fail-Safe Timer

The fail-safe timer is a software timer implemented through Port B of the NSC810. If the user chooses to implement this feature, the CPU must be programmed to toggle bit 4 of Port B based on the 0.5 second on-board timer. This provides a 1Hz signal to the CIMBUS that is used to retrigger a monostable multivibrator (one-shot) on any expansion board. If the CPU should fail, the CIMBUS signal TMRFS will no longer be output. The expansion board(s) will then set their outputs to a known quiescent state, ensuring an orderly shutdown without a CPU. An on-board LED indicates the state of TMRFS and also allows for a quick visual inspection of the health of the CPU board.

CIM-660 Firmware Monitor

The CIM-660 Firmware Monitor is available in a preprogrammed NMC27C32 EPROM. This comprehensive monitor includes facilities to load, execute, and debug programs based on the CIM CPU boards. The monitor allows the user to examine and modify any RAM location or CPU register. It also allows the movement of blocks of data within memory and initiation of user programs with optional breakpoints. Files can be uploaded and downloaded over a serial link using the industry-standard hexadecimal format. The user can employ the monitor to search memory to find the location of an 8- or 16-bit string. The CIM-660 will calculate the sum, difference, product, and quotient (with remainder) of any 4-, 8-, or 16-bit set of numbers. Additionally, the monitor can be used to exercise all available I/O ports within the system. The CIM-660, in conjunction with a CIM-201 Serial I/O Board, incorporates a baud rate search to determine the rate at which the CRT/TTY is running. The following commands are supported in the CIM-660 Firmware Monitor:

- D — Display contents of memory
- E — Examine CPU registers
- F — Find bit stream in memory
- G — Execute program (with optional breakpoints)
- I — Input data from I/O port
- M — Move block of data
- O — Output data to I/O port
- R — Input a hexfile over a serial link
- S — Examine and/or substitute value in memory
- V — Verify result of move command
- W — Output a hexfile over a serial link
- + — Add two 16-bit hex numbers
- − — Subtract one 16-bit hex number from another
- * — Multiply two 16-bit hex numbers
- / — Divide a 32-bit hex number by a 16-bit hex number

Real-Time Software

The BLMX-80C real-time multitasking executive requires only 2K bytes of EPROM and 512 bytes of RAM in its minimum configuration. Facilities such as the following are included: priority-based system resource allocation, intertask communication and control, interrupt-driven control for standard I/O devices, time-of-day clock, free space memory manager, and interrupt and event handling. Optional linkable and relocatable modules for console control (CRT or TTY), fail-safe timer interface, analog I/O board interface, and interactive system-level debugging are provided with the BLMX-80C package. User configurability is aided on the STARPLEX™ Development System by the menu-driven SYSCON System Configuration program that is also provided with BLMX-80C.

System Development Capability

The development cycle for CIMBUS-based products may be significantly reduced using the STARPLEX Development System from National Semiconductor Corporation. The convenience of a comprehensive operating system combined with system prompts that guide even inexperienced users through complex tasks creates an ideal software development environment. An In-System Emulator (ISE)™ available for the NSC800 allows the development and debugging of software directly on the CIM-802 board.

Specifications

Microprocessor

CPU — NSC800

Data word — 8 bits

Instruction word — 8, 16, or 24 bits

Product	Clock Speed	CPU Speed	Min. Instruction Execution Time
CIM-802A	4 MHz	2 MHz	2 μs
CIM-804	8 MHz	4 MHz	1 μs

Registers — 14 general purpose
2 index
Program counter
Stack pointer
Refresh register
Interrupt register

Number of instructions — 158 instruction types, providing for more than 600 executable instructions (Z80 code compatible)

Address capacity — Memory - 64K bytes
I/O - 256 input
256 output

Memory

RAM — 2K bytes static RAM (6116) plus 128 bytes in NSC810 RAM I/O Timer

ROM — Sockets for 2K bytes (27C16) or 4K bytes (27C32) ROM

Expansion — VIA memory expansion boards to 64K

Access time — 350 ns.

Address assignments —

Address Range	Assignment
0000H–07FFH	On-board PROM (using 27C16)
0800H–0FFFH	Off-board (unassigned) if 27C16 PROM is used. On-board EPROM if 27C32 PROM is used

1000H–EFFFH	Off-board (unassigned)
F000H–F7FFH	On-board RAM (2K byte RAM, battery backup available)
F800H–F87FH	On-board RAM (NSC810 128 byte RAM, not backed up during power failure)
F880H–F8FFH	NSC810 I/O port and timer control access (memory-mapped)
F900H–FFFFH	Reserved

Connectors

CIMBUS — Pin-in-socket DIN 41612
Recommended mating connectors:
Winchester 96S-6033-0531-2
Elco 008257-096-649-124

Parallel I/O — Right-angle header
Recommended mating hardware:
3M 3399-7026 (Connector)
3M 3350/26 (Cable)

Power $+5V_{DC} \pm 5\%$

Product	EPROM Used	Normal Operation	Power Save	Battery Backup
CIM-802A	27C16	60 mA	25 mA	10 μA
CIM-802A	27C32	60 mA	25 mA	10 μA
CIM-804	27C16	85 mA	25 mA	10 μA
CIM-804	27C32	85 mA	25 mA	10 μA

Environmental

Temperature —CIM-802A/804: −40°C to +85°C (−40°F to +185°F)
CIM-802AC/804C: 0°C to +70°C (−32°F to +158°F)

Humidity — 0 to 90% noncondensing

Physical —

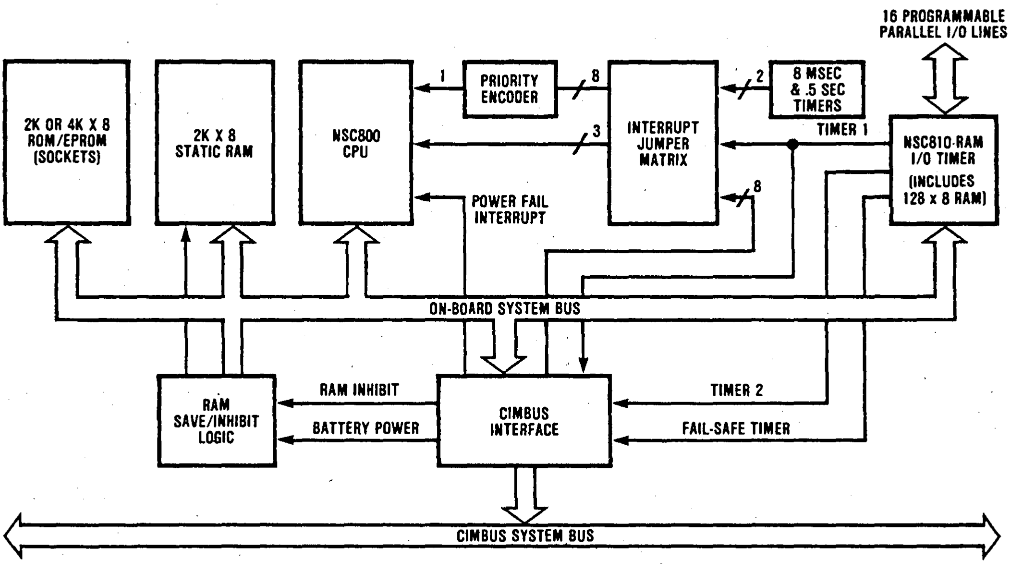
Length	6.30 in.	(160 mm)
Width	3.94 in.	(100 mm)
Height	0.50 in.	(13 mm)
Weight	1.4 oz.	(36 gm)

Order Information

CIM-802A	CMOS Industrial Microcomputer with 2MHz NSC800
CIM-802AC	0°C to +70°C (commercial) version
CIM-804	CMOS Industrial Microcomputer with 4 MHz NSC800
CIM-804C	0°C to +70°C (commercial) version

Documentation

CIM-804M	CIM-802A/802AC and CIM-804/804C Board Level Computer Hardware Reference Manual (#420308205-001)
CIMBUSM	CIMBUS System Bus Specification (#420306681-001)



TL/T/5092-1

FIGURE 1. CIM-804 CPU Board Block Diagram

Section 15

Military/Aerospace

15

INTRODUCTION TO THE RELIABILITY MILITARY/AEROSPACE PROGRAMS

History

In the mid 1960's the various government agencies responsible for semiconductor reliability saw that screenable defects were resulting in an in-equipment failure rate of about 1% per thousand hours. In-depth failure analysis allowed them to determine what the predominate failure mechanisms were. The Solid State Applications Branch of the Air Force's Rome Air Development Center (RADC) was assigned the task of developing a screening procedure which would remove the infant mortality failures which had led to the high failure rate previously encountered. Working closely with other semiconductor reliability experts, the RADC staff developed MIL-STD-883, which was first issued in 1968. The objective of MIL-STD-883 was to create an economically feasible, standardized integrated circuit screening flow which would achieve an in-equipment failure rate of 0.08% per thousand hours for Class B and 0.004% per thousand hours for Class A (which was later superseded by Class S). Over the years this standard has grown and matured with a number of new test methods added as reliability information and failure analysis results became more detailed. These developments have led to one of the strongest and most comprehensive screening specs available, MIL-STD-883.

Purpose and Structure

MIL-STD-883 states: this standard establishes uniform methods and procedures for testing microelectronic devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations, and physical and electrical tests. What does this mean to the semiconductor user? To understand this, one must subdivide MIL-STD-883 into two primary areas: 1) Detailed how-to specifications (methods 1001 through 4007) and 2) Screening and qualification and/or quality conformance testing requirements (methods 5001 through 5009). By examining each of these areas the thrust of MIL-STD-883 will become apparent.

Detailed How-to Specifications

MIL-STD-883 is a collection of environmental, mechanical, visual, and electrical test methods. These methods define tests which enable manufacturers and users to screen for specific reliability concerns. The tests covered include moisture resistance, high temperature storage, neutron irradiation, shock and acceleration tests, visual radiography, and dimensional tests, to mention only a few. In the electrical test section, there are tests to examine load conditions, power supplies, short circuit currents, and other tests. Each of these tests is designed to look at specific reliability and quality concerns that affect semiconductor products.

Screening Flows

The overall reliability requirements for a system depend upon a number of factors, including cost-effectiveness. For example, a deep space probe, where component replacement is impossible once the system is launched, requires very high reliability, despite the inherent cost of complex screening. On the other hand, a ground-based radio unit can use a less stringent reliability testing sequence, since a failed component can be easily replaced at moderate cost. In line with this range of needs, MIL-STD-883 established three distinct product assurance levels to provide reliability commensurate with the product's intended application. The three levels are Class S (intended for critical applications, such as space), Class B (intended for less critical applications, such as airborne or ground systems), and Class C (intended for easily replaceable systems, which has since been eliminated).

National and MIL-M-38510

A major thrust exists among integrated circuit users, suppliers, and the U.S. Government to avoid proliferation of military procurement specifications by turning instead to standardized high reliability microcircuits. National Semiconductor endorses and supports this trend.

One major program to which National is heavily committed is the JAN MIL-M-38510 IC program. This is a standardization program administered by the U.S. Defense Department which allows a user to purchase a broad line of standard products from a variety of qualified suppliers.

There is only one MIL-M-38510 program. National is committed to supplying only QPL devices, and discourages any "pseudo-38150" alternates.

There are two levels specified within MIL-M-38510 — Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems.

MIL-M-38510

The Defense Electronic Supply Center (DESC) administers the integrated circuit standardization program known as MIL-M-38510 (sometimes referred to as the JAN IC Program). The specification set used to define the program consists of four documents: general specification MIL-M-38510, which is an overall definition of the processing and testing to be performed; detail specifications (referred to as "slash sheets"), each of which defines the performance parameters for a unique generic device or a family of devices; MIL-STD-883, which defines specific screening procedures; and MIL-STD-976, which defines line certification requirements.

When a user orders a MIL-M-38510 device, he is guaranteed that he will get a device fully conformant with the detail specification and which has also met all of the general testing and processing requirements. DESC requires semiconductor suppliers to become formally qualified under the MIL-M-38510 program and to be listed on the current Qualification Products List (QPL) before they are allowed to legally ship JAN devices.

Advantages to the User

The JAN 38510 program has numerous advantages for the integrated circuit user.

- A single explicit specification eliminates guesswork concerning device electrical characteristics or processing flow.
- The rigorous schedule of quality conformance testing that is a mandatory part of the MIL-M-38510 program assures the user of long-term stability.
- Since the electrical characteristics of the devices are at least as tight as the "standard industry data sheet" parameters, device performance will meet the vast majority of system design requirements. Additionally, min./max. limits replace many data sheet typicals, making circuit design and worst case design analysis decisions easier.
- The user is spared the expense of researching and preparing his own procurement document.
- The user is spared the expense of qualification testing. The QPL tells him which suppliers have qualified the device he requires.
- The QPL gives the user a choice of qualified suppliers for devices that are fully interchangeable. In addition, the presence of several sources guarantees competitive pricing that is typically lower than for devices to a user's own specifications.
- Since MIL-M-38510 is a standard program, procurement lead times will be shorter. With a large number of programs using JAN devices, distributors and manufacturers are able to establish inventories of JAN devices. National in particular is committed to maintaining finished goods and work-in-process inventories to support our customers' needs.
- Spare parts will be readily available without excessive minimum order requirements.
- Standard parts with volume requirements will remain in production longer.
- Device markings are consistent from one manufacturer to another.
- The program is extremely cost-effective. A user can purchase a few devices for engineering evaluation and prototyping and know that they will be identical to the devices he will get during production. When the cost factors associated with spec. writing, supplier qualification, maintaining voluminous parts control documentation, and the more intangible benefits of device availability are totaled, use of JAN ICs is overwhelmingly the most cost-effective approach.

Advantages to the Supplier

What motivates a supplier like National Semiconductor to be so heavily committed to the MIL-M-38510 program? National has the *broadest* range of reliability processed products available in the semiconductor industry. A program such as MIL-M-38510 helps to standardize the processing required and to minimize the number of individual user specifications. This allows National to concentrate more resources on this program, thereby improving product quality and availability.

The Most Frequently Asked Questions and Answers about MIL-M-38510

There are many questions which are frequently asked regarding the MIL-M-38510 program. We would like to answer some of them.

Q. WHAT MUST A MANUFACTURER DO TO GET HIS PARTS LISTED ON THE QPL?

A. There are two things which a manufacturer is required to do. First, he must get his facilities (including wafer fab, assembly, and rel processing areas) certified by DESC. This requires that each fab area used for QPL devices must be approved. Second, for each specific device and package combination listed on the QPL, the manufacturer must perform extensive qualification testing and provide detailed device information to DESC. This data is typically supplied in two phases.

In the first phase, the manufacturer must supply detailed information concerning the device construction and electrical characteristics. Once this data has been verified by DESC to confirm that the manufacturer's device meets the MIL-M-38510 requirements, the manufacturer is listed on Part II of the QPL. At this point the manufacturer is legally able to supply full JAN qualified devices meeting ALL of the MIL-M-38510 requirements. The manufacturer must then perform the full qualification testing of Method 5005 of MIL-STD-883 as specified in paragraph 4.4 of MIL-M-38510. Once this data has been reviewed and accepted by DESC, the manufacturer is listed on Part I of the QPL.

Q. IS THERE ANY DIFFERENCE IN DEVICES PRODUCED WHILE A MANUFACTURER IS LISTED ON PART II OF THE QPL AND THOSE PRODUCED AFTER PART I QUALIFICATION IS COMPLETED?

A. There is absolutely *no difference*. A supplier must meet all of the device screening and quality conformance requirements no matter what his QPL status.

Q. HOW DOES A USER KNOW WHAT DEVICES ARE COVERED BY SLASH SHEET SPECIFICATIONS?

A. Supplement 1 to MIL-M-38510 contains a listing of the slash sheet specifications and a cross reference to the generic part type. This is updated as new slash sheets are released. National's Reliability Handbook also contains a cross reference.

Q. HOW CAN A USER OBTAIN COPIES OF THE QPL, SUPPLEMENT 1 OF MIL-M-38510, MIL-M-38510 ITSELF, AND MIL-STD-883?

A. Copies of these and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

Q. WHAT ABOUT THOSE DEVICES FOR WHICH NO DETAIL SPECIFICATION EXISTS?

A. The ultimate aim of a standardization program must be to furnish *all* parts. Requests for addition of a part to MIL-M-38510 should be made to DESC Directorate of Engineering, Dayton, Ohio 45444, indicating a need for slash sheets and/or suppliers to be qualified for the additional devices. National has a form (available through local sales offices) which may be used for this purpose. In addition, if only some parts are available, a user can still see significant savings on those that are available.

Q. HOW IS A JAN QPL DEVICE MARKED?

A. Tables I and II explain the details of the marking for JAN ICs.

TABLE I. MIL-M-38510 PART MARKING

JM38510/XXXXXYYY

- the Lead Finish
  A = Solder Dipped
  B = Tin Plate
  C = Gold Plate
  X = Any lead finish above is acceptable
- the Device Package (see Table II)
- the Screening Level S or B
- the Device Number on the Slash Sheet
- the Slash Sheet Number
- MIL-M-385810
- The JAN prefix (which may be applied only to a fully conformant device per paragraphs 3.6.2.1 and 3.6.7 of MIL-M-38510)

TABLE II. JAN PACKAGE CODES

38510 PACKAGE DESIGNATION	MICROCIRCUIT INDUSTRY DESCRIPTION
A	14-pin 1/4″ × 1/4″ (metal) flatpack
B	14-pin 3/16″ × 1/4″ flatpack
C	14-pin 1/4″ × 3/4″ dual-in-line
D	14-pin 1/4″ × 3/8″ (ceramic) flatpack
E	16-pin 1/4″ × 7/8″ dual-in-line
F	16-pin 1/4″ × 3/8″ (metal or ceramic) flatpack
G	8-pin TO-99 can or header
H	10-pin 1/4″ × 1/4″ (metal) flatpack
I	10-pin TO-100 can or header
J	24-pin 1/2″ × 1-1/4″ dual-in-line
K	24-pin 3/8″ × 5/8″ flatpack
M	12-pin TO-101 can or header
P	8-pin 1/4″ × 3/8″ dual-in-line
Q	40-pin 8/16″ × 2-1/16″ dual-in-line
R	26-pin 1/4″ × 1-1/16″ dual-in-line
S	20-pin 1/4″ × 1/2″ flatpack
V	18-pin 3/8″ × 1-15/16″ dual-in-line
W	22-pin 3/8″ × 1-1/8″ dual-in-line
X, Y, Z	Unassigned — Reserved for identifying special packages whose dimensions are carried in the detail specifications.

Q. ARE DEVICES CALLED "M38510, JAN PROCESSED, JAN EQUIVALENT, ETC." REALLY QPL PRODUCTS?

A. *Absolutely not.* There is only one QPL product — it is a JM38510 marked device. "JAN Equivalent" is expressly forbidden by paragraphs 3.1 and 3.6.7 of MIL-M-38510. MIL-M-38510 does provide for the production of devices when no qualified sources exist, but this may be done only with prior DESC approval, and products produced under this provision must meet all requirements of MIL-M-38510 other than qualification.

Q. HOW LONG CAN A SUPPLIER REMAIN ON PART II OF THE QPL?

A. For Class B, a manufacturer can remain on Part II for two years or until 90 days after another supplier becomes qualified for the same device package, screening level, and lead finish combination on Part I of the QPL. Class S devices may remain on Part II for one year after another manufacturer reaches Part I.

Q. WHEN ANOTHER SUPPLIER OBTAINS PART I QUALIFICATION, ARE THE OTHER QUALIFIED SUPPLIERS REMOVED FROM PART II IMMEDIATELY?

A. No. The supplier is given 90 days before being removed from Part II for a Class B device and one year for a Class S device. During that time a supplier may legally accept orders for those devices. After the end of the 90-day or one year period, he may no longer accept orders but may complete and ship those orders received prior to that time, no matter how long it takes him to complete them.

Q. IS A SUPPLIER EVER REMOVED FROM PART I QUALIFICATION?

A. Generally not. As long as a supplier continues to manufacture the device, maintains appropriate facility approvals, and submits all required reports and information to DESC within stipulated time limits, he will retain QPL I listing. Violation of these requirements can be cause for removal from QPL.

Q. CAN AN AUTHORIZED DISTRIBUTOR SHIP JAN DEVICES FROM HIS SHELVES IF THE MANUFACTURER HAS LOST HIS QPL LISTING FOR THOSE DEVICES?

A. Yes. As long as those devices were ordered by the authorized distributor while the manufacturer had QPL listing for those devices, the distributor may subsequently ship those devices from his shelves.

Q. CAN A MANUFACTURER LEGALLY SHIP JAN QPL MATERIAL HE ASSEMBLED AND TESTED BEFORE HE RECEIVED A QPL LISTING?

A. Yes. The manufacturer must assemble and screen parts to prove his ability to comply with the specifications before he can be placed on QPL. As a result, his first lot of material, which is fully conformant to QPL product requirements, will have a date code that is earlier than the date he is placed on the QPL. However, the manufacturer may *not* begin to assemble and test unless he has a line certification and an approval to proceed with qualification.

Q. WHAT IS THE RELATIONSHIP BETWEEN MIL-M-38510 AND MIL-STD-883?

A. MIL-M-38510 defines complete program requirements and the detail device electrical performance parameters. The device processing requirements are specified in MIL-STD-883.

Q. SUPPOSE DEVICES ARE KEPT ON A MANUFACTURER'S OR DISTRIBUTOR'S SHELVES FOR A PERIOD OF TIME; MUST THEY EVER BE RETESTED TO VALIDATE THAT THEY STILL MEET SLASH SHEET CHARACTERISTICS?

A. Yes. Devices held by a manufacturer or by his authorized distributor which have a date code older than 24 months must be retested by the manufacturer in accordance with Group A sampling requirements prior to shipment to a customer or return to inventory.

Q. WHY SHOULD A USER SPECIFY "X" IN THE LEAD FINISH DESIGNATION FOR A PART TYPE?

A. A manufacturer who receives an order for a specific lead finish for which he is qualified but has no inventory at the time of order may not be able to fill the order in a timely manner, even though he might have substantial inventory of another lead finish. Unless a user has a specific reason for wanting a particular lead finish, he should allow his suppliers the flexibility of shipping whatever finish is available.

Q. WHAT DATA IS A MANUFACTURER REQUIRED TO SHIP WITH A JAN PART?

A. A certificate of conformance is all that is required. However, he must retain all data for three years.

Q. CAN A DEVICE FOR WHICH THERE IS NO SLASH SHEET BE PROCESSED TO MIL-M-38510?

A. Since MIL-M-38510 invokes a combination of the processing requirements of MIL-STD-883 and the detail device performance parameters contained in each individual slash sheet, the answer is obviously no. However, National's 883B/RETS™ program does provide parts which meet all of the screening requirements of the MIL-STD-883 specification and which have been subjected to all of the MIL-M-38510 controls (except for domestic assembly).

TABLE III. SAMPLE MIL-M-38510 LISTING

GOVERNMENT DESIGNATION				TEST REPORT NUMBER	MANUFACTURER'S NAME
DEVICE TYPE*	DEVICE CLASS	CASE OUTLINE	LEAD MATERIAL AND FINISH		
M38510/008					
01	S only	A	C	38510-953-81	National Semiconductor Corp.
01	B	C	A	38510-953-81	National Semiconductor Corp.
02		D	B	38510-30-7T	
03	B	C	A B	38510-520-83	National Semiconductor Corp.

*"M38510" is the military designator for MIL-M-38510. The QPL shows this notation even though the parts are fully qualified devices and are marked JM38510/XXXXXYYY.

Q. WHAT DOES A QPL LISTING LOOK LIKE AND HOW DO YOU READ IT?

A. Sample QPL listings are shown in Table III.

JM38510/00801SAC
JM38510/00801BCA
JM38510/00801BCB
JM38510/00801BDA
JM38510/00801BDB
JM38510/00802BCA
JM38510/00802BCB
JM38510/00802BDA
JM38510/00802BDB
JM38510/00803BCA
JM38510/00803BCB

Q. WHAT QUALITY CONFORMANCE TESTS ARE CONDUCTED? ARE ALL DEVICES IN A GENERIC FAMILY EVENTUALLY SUBJECTED TO QUALITY CONFORMANCE TESTING?

A. For B level devices quality conformance tests must be conducted as follows:

Group A—Each inspection lot or sublot.

Group B—Each inspection lot for each package type and lead finish on each detail specification.

Group C—Periodically at 3-month intervals on one device type or one inspection lot from each mircocircuit group in which a manufacturer has qualified device types (die related tests).

Group D—Periodically at a 6-month interval for each package type for which a manufacturer holds qualifications (package related tests).

Different devices within a generic family are chosen for successive quality conformance tests until all of the devices have been subjected to testing. The sequence is then repeated. The manufacturer must submit attributes data to DESC for all quality conformance tests performed.

Q. HOW IS AN INSPECTION LOT DEFINED?

A. For Class B devices, each inspection lot shall consist of microcircuits of a single device type, in a single package type and lead finish, or may consist of inspection sublots of several different device types, in a single package type and lead finish, defined by a single detail specification. Each inspection lot shall be manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and case with the same material requirements, and sealed within the same period not exceeding 6 weeks.

Q. WHAT IS NATIONAL SEMICONDUCTOR'S COMMITMENT TO MIL-M-38510?

A. National Semiconductor is convinced that the level of standardization offered by a program like MIL-M-38510 is the key to long-term military component procurement viability. We have a corporate commitment to MIL-M-38510. We believe that the program will be of significant benefit in lessening the problem of product obsolescence, for the volume provided will help to keep many key devices in production. We believe that the program will make possible the procurement of devices in small quantities with reasonable lead times for long-term spares or field maintenance requirements.

National Semiconductor will continue to maintain a broad base of line certifications and an extensive list of Class B and Class S device qualifications. We will continue to work with the Department of Defense, concerned users, and other semiconductor manufacturers to update and redefine the applicable specifications. We feel that this level of support is essential if MIL-M-38510 is to remain the strongest standardization program available.

In addition, we will continue to add capacity and to build up substantial inventories of a large spectrum of products to ensure the availability and the lead times that are needed for key military programs.

National Mil/Aero Standardization Programs

Your customer has imposed upon you requirements for product reliability that you must meet on every single component you buy. In most cases, these requirements mandate that you buy JAN MIL-M-38510 parts where they are available, and that all other devices must be as close to JAN as is achievable. We don't consider this unreasonable. In fact, we believe that this is the only reasonable and intelligent approach.

To meet this objective, we designed our 883B/RETS program around requirements that were already imposed for the MIL-M-38510 program.* We realize that there are many so-called standardization programs available in the marketplace which lack the compliance that you need. Our 883B/RETS program is totally compliant. We invite you to make this comparison between what we offer and what you need. Our screening flow, our 5% PDA, our quality conformance test frequency, and the other items that you consider important, match exactly the requirements defined in MIL-M-38510.** If they did not, we could not offer ***Total Standardization***.

Standardization provides the manufacturing efficiencies needed by the semiconductor manufacturers if they are to meet military semiconductor needs. To the user, standardization offers the highest guarantee of quality and reliability through production consistency and uniformity. The most significant benefit of standardization to the Department of Defense, however, is that it ensures the availability of component level spares to key programs with the pricing, delivery, and reliability needed for the field support and maintenance of our key defense electronics systems.

National's MIL-M-38510 Emphasis

To implement this view of standardization, we have based our entire approach to military screening upon the Class S and Class B requirements of MIL-M-38510. We are convinced that to do less than this would be to provide an inferior product, one that does not meet the true needs of the Department of Defense. Our 883B/RETS microcircuits are processed through the most comprehensive and compliant Class B screening program offered by any semiconductor manufacturer. We have tried to emulate MIL-M-38510 to the fullest extent possible, with the same production controls, calibration schedules, rework and resubmission procedures, operator certification requirements, and all of the other key elements of MIL-M-38510. The procedures that we employ in the production of MIL-M-38510 devices are used for all of the military devices we manufacture.

Our 883S/RETS™ microcircuits are processed through a screening flow that matchs the MIL-M-38510 Class S flow exactly. Our commitment to MIL-M-38510 Class S is such that once qualified for a given device type we will sell that part only as a JAN Class S part. Class S QPL listing will result in the immediate removal from production of the 883S/RETS version of the device.

*Requirements that were subsequently incorporated into MIL-STD-883

**and MIL-STD-883.

National's Commitment

But compliance flows are obviously meaningless unless the capacity is in place to support them. We have the industry's largest screening capacity. Over the past few years we have reinvested substantial sums in additional capital equipment in both buildings and the equipment with which to fill those buildings. Our Tucson, Arizona plant was the first plant in the entire industry to be totally dedicated to the production of military integrated circuits. We will continue to add capacity for military assembly and test, even during those periods when others turn away from the military marketplace in pursuit of what they view to be the more attractive commercial market. We feel that a commitment to the needs of the military/aerospace user community should not be based upon the conditions encountered in the commercial marketplace. We have no plans for other than a continued long-term commitment to military/aerospace component production and screening. And we will not deviate from the highest standards of quality and reliability in our execution of that commitment. There are no shortcuts to semiconductor reliability. It can only be achieved through rigid adherence to established standards.

However, we also acknowledge the quite obvious fact that through refinement and redefinition, standards are subject to change. As those changes occur, we will update our current procedures to reflect the changes that find their way into MIL-M-38510 and MIL-STD-883. We will, where our understanding of semiconductor reliability and screening indicates the need, actively pursue those changes that we feel will allow our industry to provide a better product to the systems manufacturers. We will also steadfastly resist those changes which we feel sacrifice reliability to the less important question of expediency.

National's Standard Programs

MIL-M-38510 is the key military standardization program for ICs. National is equally committed to the support of the requirements of the space segment of the market for MIL-M-38510 Class S devices. To support these needs we have established dedicated Class S assembly and test facilities. The realization that users could not obtain all the device types they required through these programs led National's Military/Aerospace Products Group to the development of two of the strongest and most compliant in-house programs in the industry. National programs for 883B/RETS and 883S/RETS microcircuits provide the systems manufacturer with an easy mechanism for obtaining those devices not listed on the MIL-M-38510 QPL. In response to other user needs, National also developed a program for radiation hardened devices (both CMOS and linear), a comprehensive program for radiation susceptibility testing for Class S devices, and a program for the production of devices in leadless chip carriers (LCCs).

RETS and Burn-In

One of the primary advantages of MIL-M-38510 is its clear definition and standardization of electrical test and burn-in requirements. One of the major drawbacks seen in the standard reliability screening programs of most semiconductor manufacturers is that electrical testing is invariably performed to some document that is not available to the user. The user has the right to know what he is buying. At National that testing is never vague or undefined. Both in-house programs (883B/RETS and 883S/RETS) are based upon a document called the RETS (an acronym for Reliability Electrical Test Specification. The RETS is a simplified but complete description of the testing performed as part of National's standard Rel electrical test programs, and is controlled by our QA department. The burn-in circuits and electrical test parameters for the MIL-M-38510 Class S and Class B devices produced by National Semiconductor are defined by the applicable detail specification.

Ordering ICs from National

Ordering National Semiconductor High Reliability integrated circuits is very simple. National sales offices and sales representatives can provide price and delivery information on our entire line of JM38510 Class B, JM38510 Class S, 883B/RETS and 883S/RETS microcircuits. A large percentage of these devices are available from inventory at either the factory or at one of our many distributors.

Ordering to Control Specifications

We also acknowledge the fact that many military systems manufacturers must, for contractual purposes, maintain their own specifications for many of the devices that they purchase. We have no objection to the use of contractor prepared procurement specifications, for we have found that the majority of these documents are written in compliance with the requirements of MIL-M-38510. Where this is true, we have found that they are also totally compatible with our in-house standardization programs. Where drawings submitted to National differ from the requirements outlined in MIL-M-38510, we welcome the opportunity to work with our customers to develop specifications which do meet the intent of MIL-M-38510.

Where customer specifications and our 883B/RETS product specifications correspond, we have the ability to expedite delivery by adding the customer part number in addition to the basic 883B/RETS part number. Customers who understand our program and wish to use the program in their parts procurement may order by placing "M/O" after their part number on their purchase order, thus allowing us to mark their part number on our 883B/RETS devices without the lengthy delay normally required for a comprehensive specifications review cycle. We have tried to provide programs that offer the maximum level of flexibility within the constraints of standardization.

Standardization is the key to cost-effective procurement of high reliability semiconductor devices. National Semiconductor Corporation is committed to that standardization.

Military Processing: A Corporate Commitment

The National Semiconductor Military/Aerospace Products Division draws upon the total resources of National Semiconductor. National is one of the world's largest manufacturers of semiconductor products, offering the largest number of product types available from any single source in the industry. This product line is growing faster than that of any other worldwide semiconductor manufacturer. Each new product is carefully evaluated for possible military/aerospace usage potential, and new product designs must comply with the reliability and quality constraints required by that segment of the industry. All new product designs are targeted to full military temperature range operation.

In addition, a dedicated Reliability Engineering Department within the Military/Aerospace Products Division coordinates burn-in circuit design, test tape development, test fixturing, support documentation, and new product release paperwork to ensure the earliest possible introduction of fully compliant 883B/RETS versions of the new products introduced by the company.

We are able to do this well, for National is no newcomer to this business. Founded in Danbury, Connecticut in 1959, National acquired an entire new management team in 1967 and moved corporate headquarters to Santa Clara, California. The new management team focused its attention on the transistor product line, and rapidly made that line profitable. Then the company's talents were turned to the development of linear, digital, and MOS integrated circuits — the fastest-growing segments of the semiconductor marketplace. Finally, an OEM representative and distributor network was established to develop and service a broad customer base, and facilities were added around the world to provide competitive products to worldwide markets.

The Reliability Test Department was initially formed in 1968 and reported at that time to the Director of Quality Assurance. The Rel Department developed the same rapid growth rate that the company as a whole had shown. From a small staff occupying several thousand square feet in Santa Clara, these reliability test operations grew until today they employ over 3000 people worldwide. Well over 200,000 square feet are devoted to the testing and assembly of high reliability products. During 1981, the Military/Aerospace Products Group became the Military/Aerospace Products Division. The company is currently involved in a number of military research and development programs, including a Phase I VHSIC contract.

VHSIC involvement was natural since National's technological leadership has enabled the company to consistently be one of the major suppliers of military/aerospace semiconductors. Having continued to develop a high technology image through the development of Megarad hardened CMOS and linear device types, and the development of Tricode™ logic, National is now expanding technology frontiers in the areas of memory, microprocessor, and data acquisition products. As a result of all this innovation, National has become the only company in the entire semiconductor industry capable of providing high reliability devices from all of the following product lines:

linear
hybrid
CMOS logic
Megarad CMOS logic
bipolar memory
MOS RAMs
CMOS RAMs
MOS EPROMs
CMOS EPROMs
MOS EEPROMs
data acquisition devices
standard TTL
low power TTL
low power Schottky
standard Schottky
interface devices
bipolar microprocessors
MOS microprocessors
CMOS microprocessors
COPS™ microcontrollers
high-speed CMOS Schottky
advanced low power Schottky
advanced Schottky

National Semiconductor has wafer fabrication plants in Santa Clara, California; Salt Lake City, Utah; Arlington, Texas; and Danbury, Connecticut. Many of these fabrication plants, along with our assembly and test lines in Santa Clara, California and Tucson, Arizona, have been fully certified for the production of Class S and Class B MIL-M-38510 circuits.

To support the requirements of the Class S marketplace, we have our own SEM and radiation testing facilities. Our screening capabilities are backed up by one of the most extensive failure analysis labs in the industry.

National is the leader in the military/aerospace integrated circuit market. We have achieved that leadership by offering an unmatched combination of technology, product breadth, understanding, commitment and capacity.

883B/883S/RETS Screening Flows

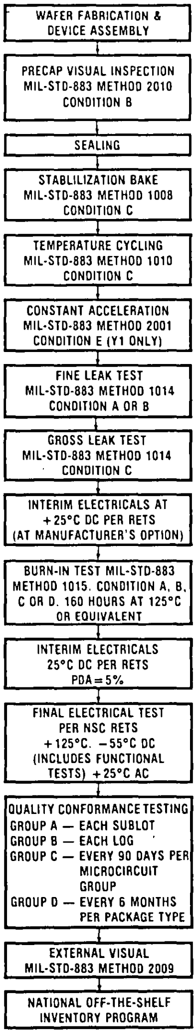
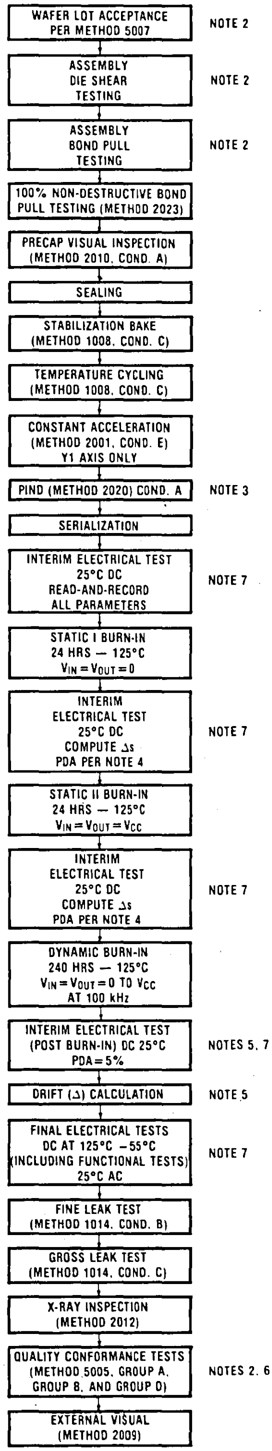


FIGURE 1: NATIONAL'S 883B/RETS CLASS B SCREENING FLOW



NOTES:
1. ALL METHODS REFERENCED ARE MIL-STD-883 TEST METHODS.
2. THESE TESTS ARE PERFORMED ON A SAMPLE BASIS. ALL OTHER TESTS ARE PERFORMED 100%.
3. ACCEPTANCE CRITERIA SHALL BE IN ACCORDANCE WITH MIL-M-38510.
4. THE PDA FOR STATIC I AND STATIC II BURN-IN SHALL BE 5% TOTAL.
5. THE PDA INCLUDES ∆ FAILURES.
6. GROUP A AND BOND PULL AND DIE SHEAR TESTING OF GROUP B MAY BE PERFORMED ON-LINE.
7. ALL ELECTRICAL TESTING SHALL BE IN ACCORDANCE WITH THE APPLICABLE RETS OR THE APPLICABLE MIL-S-38510 DETAIL SPECIFICATION.

FIGURE 2: NATIONAL'S 883S/RETS CLASS S SCREENING FLOW

CD40XX, 54CXX Product Availability

The following list of products represents what is currently available for 883B. As new products are brought on board, notification will take place through news releases. For further data on the products and families, please contact your local sales office.

PACKAGE CROSS REFERENCE

NSC ORDER NUMBER	RCA EQUIVALENT DESIGNATION	MOTOROLA EQUIVALENT DESIGNATION	PACKAGE
CD40XXMJ/883B	CD40XXAF	MC140XXAL	Cavity DIP (J)
CD40XXMD*/883B	CD40XXAD	—	Cavity DIP (D)
CD40XXMW/883B	CD40XXAK	—	Cavity Flatpack (W)
CD40XXMF*/883B	—	—	Cavity Flatpack (F)
CD40XXME*/883B	CD40XXAL	MC140XXAZ	Leadless Ceramic Pack (E)

*Contact marketing for current status.

For B series, NSC order number is CD40XXBMX/883B.

INDUSTRY ID	NSC ID
CD4000MJ/883	MM4600AJ/883
CD4000MW/883	MM4600AW/883
CD4001BMJ/883	MM4601BJ/883
CD4001BMW/883	MM4601BW/883
CD4001MJ/883	MM4601AJ/883
CD4001MW/883	MM460AW/883
CD4002BMJ/883	MM4602BJ/883
CD4002BMW/883	MM4602BW/883
CD4002MJ/883	MM4602BJ/883
CD4002MW/883	MM4602AW/883
CD4006BMJ/883	MM4606BJ/883
CD4006BMW/883	MM4606BW/883
CD4006MJ/883	MM4606AJ/883
CD4006MW/883	MM4606AW/883
CD4007MJ/883	MM4607AJ/883
CD4007MW/883	MM4607AW/883
CD4008BMJ/883	MM4608BJ/883
CD4008BMW/883	MM4608BW/883
CD4009MJ/883	MM4609AJ/883
CD4009MW/883	MM4609AW/883
CD4010MJ/883	MM4610AJ/883
CD4010MW/883	MM4610AW/883
CD40106BMJ/883	MM54C14J/883
CD40106BMW/883	MM54C14W/883
CD4011BMJ/883	MM4611BJ/883
CD4011BMW/883	MM4611BW/883
CD4011MJ/883	MM4611AJ/883
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MM54C93J/883	MM54C93J/883
MM54C941J/883	MM54C941J/883
MM54C95J/883	MM54C95J/883

54HC/54HCT Product Availability

The following list of products represents what is currently available for 883B. As new products are brought on board, notification will take place through news releases. For further data on the products and families, please contact your local sales office.

PACKAGE CROSS REFERENCE

NSC ORDER NUMBER	MOTOROLA EQUIVALENT DESIGNATION	PACKAGE
54HC/HCTXXJ/883B	54HC/HCTXXBCAJC	Cavity DIP (J-14)
54HC/HCTXXJ/883B	54HC/HCTXXBEAJC	Cavity DIP (J-16)
54HC/HCTXXJ/883B	54HC/HCTXXBRAJC	Cavity DIP (J-20)
54HC/HCTXXJ/883B	54HC/HCTXXBJAJC	Cavity DIP (J-24)
54HC/HCTXXW/883B	—	Cavity Flatpack (W)
54HC/HCTXXE*/883B	54HC/HCTXXBZAJC	Leadless Ceramic Pack (E)

*Contact marketing for current status.

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RADIATION HARDENED TECHNOLOGIES FROM NATIONAL SEMICONDUCTOR

For many years, military, aerospace and satellite programs have depended on bipolar transistor and integrated circuit technology in the fabrication of airborne systems. Development of bipolar technology is an outgrowth, in part, of avionics and space applications needs. Despite their relatively high immunity or resistance to high levels of both constant and burst radiation in the form of gamma rays, x-rays, cosmic rays, and so on, bipolar devices have two drawbacks: a susceptibility to damage from neutron fluxes, and high power consumption, which adds to the power supply requirements and subtracts from the usable payload of spacecraft and missiles. In addition, recent decreases in bipolar feature sizes and changes in bipolar design and fabrication techniques have led to bipolar devices which exhibit the same level of susceptibility to ionizing radiation that had historically been seen in MOS devices. The spacecraft and missile industry has long needed a radiation hardened logic technology with low power consumption that would readily lend itself to reliable fabrication processes with reasonable repeatability. The purpose of this brochure is to provide some information to the potential user regarding National Semiconductor's solutions to radiation problems.

CMOS Radiation Hardened Products

Over the years, the development of sophisticated space, satellite and military systems and mission requirements fostered an active search for a radiation hardened logic circuit technology that consumes less power and offers a higher degree of circuit integration on a single silicon chip. Metal oxide semiconductor (MOS) devices, particularly complementary MOS (CMOS), provided just such an alternative. But standard CMOS devices, even those qualified to MIL-M-38510 (JAN) requirements, proved sensitive to relatively low levels of gamma (or total dose) radiation, as low in many cases as 3×10^3 rads (Si)[1]. Early generations of mass-producible specifically radiation hardened CMOS devices were able to withstand only 10^5 rads (Si), while many space, satellite and missile systems require circuitry resistance levels at least ten times higher, 10^6 rads (Si).

National Semiconductor developed a solution to this problem: a complete line of megarad hardened CMOS logic products utilizing a radiation hardening process that is compatible with volume processing. Products hardened to withstand 10 megarads [devices capable of tolerating total dose radiation of 10^7 rads (Si)] are the result of an intensive multi-year research and development program in cooperation with Sandia Laboratories (Albuquerque, NM). This program has enabled National Semiconductor to offer radiation hard versions of virtually our entire metal-gate CMOS product line.

Devices ranging in complexity from simple gates to large scale integration (LSI) random access memories have been hardened using the processes we developed. The achievement of this level of radiation resistance in a mass production CMOS process required that we implement major modifications to the basic commercial process, in the gate oxidation, substrate and P-tub surface concentrations, and metallization. We are currently in the process of research and development efforts aimed at extending these radiation improvements into complex metal gate devices (such as analog-to-digital converters and gate arrays), and into silicon gate processes. This will enable us to provide radiation hardened devices within our 54HC logic family, our P²CMOS memories and microprocessors, and our M²CMOS gate arrays.

Bipolar vs. CMOS

Bipolar devices and CMOS devices respond differently to different forms of radiation as a result of basic differences in both structure and operation. As Figure 1 shows, bipolar devices depend upon the diffusion of minority carriers for current flow through the base region. When bipolar devices are subject to neutron irradiation, the resulting crystal damage decreases minority carrier lifetime, causing severe performance degradation. On the other hand, bipolar devices are usually relatively insensitive to surface effects resulting from charge buildup in the oxide layer. Thus ionizing radiation has little effect on many bipolar structures. However, some

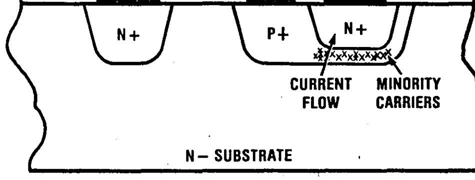

FIGURE 1: BIPOLAR IC TRANSISTOR

1. One rad (Si) is the quantity of any type of ionizing radiation which imparts 100 ergs of energy per gram of silicon.

recently developed bipolar technologies contain unhardened parasitic MOS structures as a result of the oxide isolations and walled emitter processes that they utilize.

CMOS devices (see Figure 2) are surface effect devices. The equivalent operating elements, gate, source and drain, are at the surface, and the flow of current occurs horizontally across the device, very close to the silicon/silicon-dioxide interface. Their characteristics are determined by electrostatic conditions at the silicon/silicon-dioxide interface. Carriers originate in the source region, and CMOS devices depend upon majority carriers for their operation. They are therefore not seriously affected by the minority carrier lifetime degradation resulting from neutron irradiation. They are, however, susceptible to charge in the oxide or at the oxide-substrate interface. Although gamma radiation will ionize both the oxide and the substrate, the resulting ionic charge cannot become trapped in the relatively conductive substrate as easily as it can be trapped in the insulating oxide. CMOS devices are therefore much more susceptible than bipolar devices to degradation from gamma radiation.

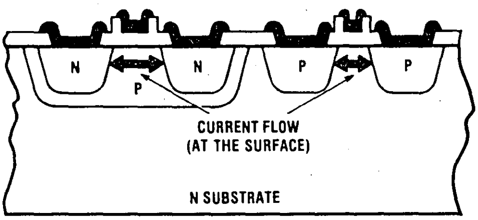

FIGURE 2: CMOS IC TRANSISTOR

CMOS IC Transistor Structures

Complementary MOS, or CMOS, combines two types of MOS devices, P-channel and N-channel structures, into a single functioning unit. The lower power dissipation and high stability resulting from this complementary combination is particularly attractive in the design of portable battery-powered electronic units, or for applications where a battery provides standby power.

MOS structures, both N- and P-types, perform in two modes; enhancement and depletion. In an N-channel enhancement mode MOS device, for example, the gate controls the current flow between the source and drain. In this device, when a positive voltage is applied to the gate with respect to the source, a field is set up across the gate dielectric, producing a negatively charged conductive path, a channel, between the source and the drain. This is known as an enhancement mode device because zero gate to source voltage turns off the device. In the alternative mode, depletion, current flows despite the gate voltage being zero, because sufficient charge is present at the silicon/silicon-dioxide interface to induce a conductive path between the device source and drain regions. The P-channel MOS transistor is similar to the N-channel alternative, except that negative voltage applied to the gate, with respect to source, induces a positively charged conductive path between source and drain to turn the device on.

Conventional CMOS logic circuits are produced with only enhancement mode N- and P-channel devices. The process is designed to give turn on (threshold) voltage values for both types of devices which insure proper circuit performance. Figure 3 illustrates the cross section of a CMOS structure connected in a simple inverter configuration. To form the standard metal gate CMOS structure, a lightly doped P-tub is formed by diffusion into an N-type substrate with the tub becoming the substrate for the N-channel transistor. The N+ and P+ impurities are diffused into P-tub and N-substrates to become the N- and P-channel transistors' source and drain regions, respectively. These diffusions also serve as contacting regions to the positively biased N-substrate and the normally grounded P-tub regions (V_{DD} and V_{SS}, respectively).

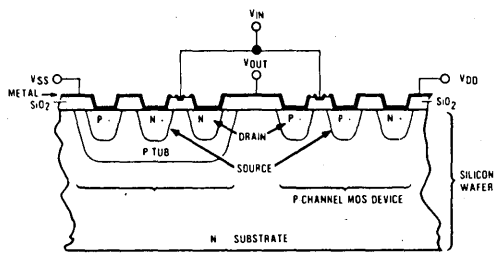

FIGURE 3: CMOS TRANSISTOR STRUCTURE IN SIMPLE INVERTER CONFIGURATION

A gate oxide is grown such that a thin film of dielectric oxide material bridges all source/drain regions. Finally, contact apertures are etched to the source/drain regions and an aluminum film evaporated and etched to form gate electrodes, contacts to device terminals, and interconnecting conductor lines.

Effects of Ionizing Radiation

A CMOS transistors' radiation resistance is primarily determined by formation of the gate structures in both P-channel and N-channel devices. The gate structures are used to turn the MOS devices on or off; that is, to enable or prevent a flow of current from the source to the

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drain. Ionizing radiation induces unwanted positive charge into the gate oxide structure, resulting in lower threshold voltages for both actual circuit devices and parasitic field oxide devices by as much as 30V or more. Figure 4 shows the charge buildup mechanisms in an N-channel gate oxide during irradiation under worst-case bias. In establishing a radiation hardened CMOS process, it is necessary to incorporate processing steps which minimize these radiation-induced shifts in critical locations of the IC structure.

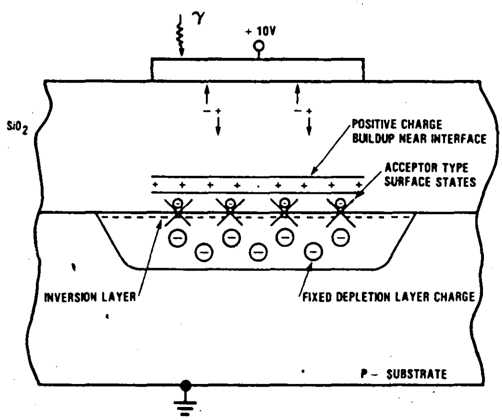

FIGURE 4: CHARGE BUILDUP MECHANISMS IN AN N-CHANNEL GATE OXIDE DURING IRRADIATION UNDER WORST-CASE BIAS

The impact of radiation-induced oxide charge on operating CMOS devices is to decrease the N-channel threshold voltage, V_{TN}, and increase the magnitude of the P-channel threshold voltage, V_{TP}. The most serious problem occurs when sufficient reduction in V_{TN} occurs to cause the N-channel device to go from enhancement to depletion mode operation. This results in excessive power supply current drain and loss of circuit functionality. The most severe stress on an N-channel device occurs when its gate is positively biased during irradiation. This causes positive charge in the oxide to be driven closer to the Si-SiO_2 interface where it is more effective in causing inversion at the P-type substrate surface.

In normal operation, positive bias cannot appear between the gate and substrate of P-channel devices because the substrate is already at the most positive circuit potential, V_{DD}. The absolute value of V_{TP} always increases with exposure to irradiation, and the magnitude of the shift is usually smaller than the V_{TN} shift. The effect of the V_{TN} is less deleterious to circuits, however, since the devices will never reach depletion mode.

CMOS Process Modification

Gate Oxidation

To minimize both the radiation-induced positive oxide charge and formation of Si-SiO_2 interface states, a dry oxidation step is used. The gate oxide is thermally grown in a dry oxygen atmosphere at 1000°C, followed by a nitrogen anneal at 850°C. This cycle has been empirically found to produce oxides having a high degree of resistance to ionizing radiation effects as well as excellent pre-radiation MOS characteristics.[2] The need to thermally grow gate oxides at 1000°C in dry oxygen for optimal radiation hardness is one of the more intriguing aspects of this experimentally deduced cycle.

Metallization

A by-product of the E-beam aluminum evaporation process commonly used in commercial IC fabrication is soft X-radiation. This radiation produces the same type of positive charge in the gate oxide and interface states which a radiation hardened oxide should resist. Although these harmful effects in the gate oxide can be removed by an anneal cycle, the annealled devices are significantly less resistant to subsequent ionizing radiation. Use of a non-E-beam metallization technique circumvents the problem of high threshold shifts due to irradiation under zero and negative gate bias associated with soft X-ray damage. For this reason, induction heated evaporation of aluminum is used to fabricate radiation hardened CMOS products.

Substrate and P-Tub Surface

The deleterious effect of ionizing radiation on V_{TN} and V_{TP} values in a CMOS device can be minimized through process modification. In anticipation of these threshold voltage shifts, radiation hardened CMOS devices are designed with the initial value of V_{TN} as high as possible and V_{TP} as close to zero as possible without sacrificing pre-radiation circuit performance. Both the substrate resistivity and the P-tub surface concentration have been modified with the initial value of V_{TN} being increased to 1.8 volts from the standard value of 1.3 volts and V_{TP} being changed from the standard −1.7 volts to −1.3 volts.

2. *W. R. Dawes, Jr., G. F. Derbenwich and B. L. Gregory, "Process Technology for Radiation Hardened CMOS Integrated Circuits," IEEE Journal of Solid State Circuits, SC-11, No. 4, p. 459, August 1976.*

Performance Characteristics

Extended Total Dose Rate [to 10^8 Rads (Si)]

Data generated in the course of our testing indicates that the resistance of our CMOS products extends at least one order of magnitude above the 10^7 level we now offer. Figure 5 illustrates measured shifts from pre-irradiation values in P-and N-channel threshold voltage, V_{TP} and V_{TN}, respectively, up to total dose levels of 10^8 rads (Si). Of special interest is the change in slope of the V_{TN} versus dose characteristic at levels just above the 10^6 rads (Si). At this level, a reduction in the net positive charge trapped in the gate oxide is observed. This causes V_{TN} to return toward its initial value as dose level is increased even further while increases in V_{TP} still remain within reasonable limits for satisfactory circuit operation.

The distributions of the V_{TN} and V_{TP} data are found to be normal both before and after irradiation. The mean value of V_{TN} and V_{TP}, and the standard deviation from the mean for both N- and P-channel devices, remain fairly constant from the unirradiated state through 10^6 rads (Si) dosage. The values shown remain well above the 300mV V_{TN} lower limit, below which the device would tend toward N-channel depletion mode behavior with a risk of lost circuit functionality as well as excessive supply current drain.

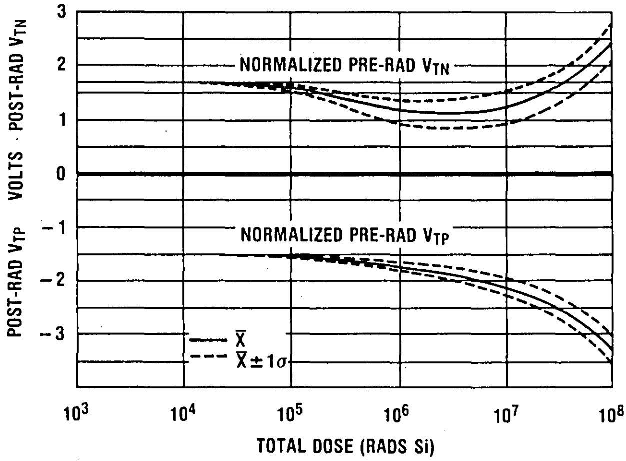

FIGURE 5: VARIATION OF V_{TN} AND V_{TP} WITH RADIATION

Figure 6 illustrates the supply quiescent current (I_{SS}) variation as a function of dose. Since I_{SS} is a function of die size, curves have been plotted for three levels of integration, SSI, MIS, and LSI. In all cases, the leakage level at 10^6 rads (Si) does not increase by more than an order of magnitude from the initial value. The 30μA reading at 10^6 rads (Si) for LSI is far below the high temperature (125°C) specification of 600μA for standard devices. Similar comparisons can be made for MSI and SSI.

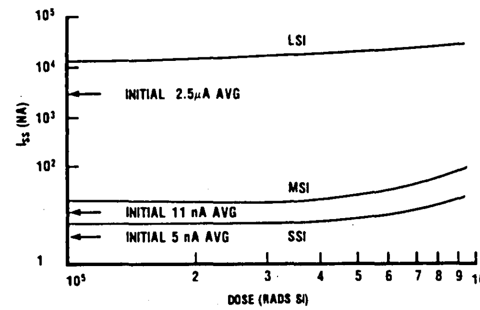

FIGURE 6: I_{SS} VS. DOSE

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Figure 7 illustrates circuit propagation delay, t_{PD}, as a function of dose. The plot, similar to Figure 6, is divided into three categories (LSI, MSI, and SSI). The propagation delay value at 10^6 rads (Si) for all three categories increased roughly 20–25% from the initial value, well within desirable operating tolerances. In Figures 5 through 7, the biasing conditions during irradiation were: $V_{DD} = 10V$, $V_{IN} = 10V$, $V_{SS} = 0V$.

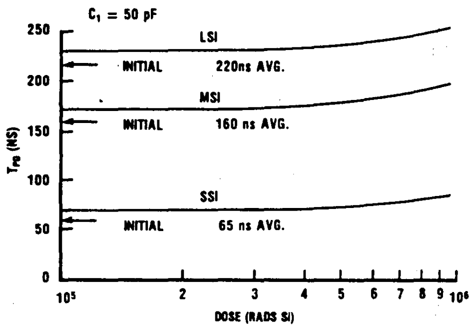

FIGURE 7: t_{PD} VS. DOSE

Hardness Assurance and Reliability

Sampling plans have been established to ensure radiation hardness to 10^5, 10^6, or 10^7 rads (Si), as applicable, since ionizing radiation degrades IC performance and irradiated devices cannot be used for production (thus making 100% screening impossible). In addition, an ongoing program has been established to evaluate the reliability characteristics of radiation hardened CMOS circuits. 476 devices of the CD4001AD-RH, CD4011AD-RH, and MM54C200-RH types were initially tested and operated for over 800,000 hours without a failure. This corresponds to a failure rate less than 0.125%/1000 hours at 125°C with a 60% confidence level. The continuing testing is aimed at verifying 10,000 hours per device of reliable operation.

Table I outlines National Semiconductor's Radiation Hardness Assurance Sampling Plan, which is totally compliant with MIL-STD-883, Method 1019. This plan is used to assure hardness of devices built from a given wafer or inspection lot. Sample devices are assembled in accordance with sampling plan A or B. Sample devices are tested, irradiated, and retested, and must pass the appropriate post-radiation electrical limits for the lot to be qualified. The production units are capable of meeting MIL-M-38510 electrical test limits, when available, as well as National's RETS limits.

TABLE I. HARDNESS ASSURANCE PLAN

I. Plan A — Class B only: Qualification to 1×10^5, 1×10^6, or 1×10^7 rads (Si)	
Sample Size per QCI Inspection Lot	11
Accept Level	0 Rejects
Reject Level	1 Reject
II. Plan B — Class B or S: Qualification to 1×10^5, 1×10^6, or 1×10^7 rads (Si)	
Sample	Each wafer
Sample Size (Devices/Wafer)	4
Accept Level	0 Rejects per wafer
Reject Level	1 Reject per wafer
III. Product Flow (per MIL-STD-883, Method 1019):	
A. Assemble sample devices in appropriate production package.	
B. Read-and-record electrical parameters (pre-radiation).	
C. Irradiate to applicable total gamma dose.	
D. Read-and-record electrical parameters (post-radiation).	
E. Evaluate performance per applicable specification.	

TABLE II-A. PRE- AND POST-RADIATION SPECIFICATION 10^5 RADS (Si)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1) −55°C Min	−55°C Max	+25°C Min	+25°C Max	+1215°C Min	+1215°C Max	UNITS
I_{DD}	Gate	5 10 15	$V_{IN} = V_{DD}$ or V_{SS} All Valid Input Combinations		0.02 0.04 0.075		0.02 0.04 0.075		0.2 0.4 0.75	μA
	Buffer F/F	5 10 15			0.3 0.4 0.5		0.3 0.4 0.5		3.0 4.0 5.0	μA
	MSI	5 10 15			0.3 0.4 0.5		0.3 0.4 0.5		3.0 4.0 5.0	μA
	LSI	5 10 15			10 20 40		10 20 40		150 300 600	μA
V_{OL}		5 10 15	$V_{IN} = V_{DD}$ or V_{SS} $\lvert IO \rvert < 10\mu A$		0.05 0.05 0.05		0.05 0.05 0.05		0.05 0.05 0.05	V
V_{OH}		5 10 15	$V_{IN} = V_{DD}$ or V_{SS} $\lvert IO \rvert < 10\mu A$	4.95 9.95 14.95		4.95 9.95 14.95		4.95 9.95 14.95		V
V_{IL}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V, $\lvert IO \rvert < 10\mu A$ VO = 1.5V, 13.5V		1.5 3.0 4.0		1.5 3.0 4.0		1.5 3.0 4.0	V
	Unbuffered	5 10 15	VO = 1.5V, 3.5V VO = 3V, 7V $\lvert IO \rvert < 10\mu A$ VO = 4V, 11V		1.5 3.0 4.0		1.5 3.0 4.0		1.5 3.0 4.0	V
V_{IH}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V $\lvert IO \rvert < 10\mu A$ VO = 1.5V, 13.5V	3.5 7.0 11		3.5 7.0 11		3.5 7.0 11		V
	Unbuffered	5 10 15	VO = 1.5V, 3.5V VO = 3V, 7V $\lvert IO \rvert < 10\mu A$ VO = 4V, 11V	3.5 7.0 11		3.5 7.0 11		3.5 7.0 11		V
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		± 10		± 10		± 45	nA
I_{OL}/I_{OH}			Per Applicable Rel Electrical Test Spec (RETS)	Published Data Sheet Limit						
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}			Per Applicable Rel Electrical Test Spec (RETS)	Published Data Sheet Limit						
Functionality			Devices Will Pass Functional Test per Applicable Truth Table							

NOTE 1: For further device parameters, see individual device specifications.
NOTE 2: These limits allow no degradation from the published data sheet limits.

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TABLE II-B. POST-RADIATION SPECIFICATION 10^6 RADS (SI)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1)						UNITS
				−55°C		+25°C		+1215°C		
				Min	Max	Min	Max	Min	Max	
I_{DD}	Gate	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations		0.5 0.75 1.0		0.5 0.75 1.0		5.0 7.5 1.0	μA
	Buffer F/F	5 10 15			0.25 0.5 1.0		0.25 0.5 1.0		5.0 7.5 10.0	μA
	MSI	5 10 15			3.0 4.0 5.0		3.0 4.0 5.0		30.0 40.0 50.0	μA
	LSI	5 10 15			25 50 100		25 50 100		300 400 500	μA
V_{OL}		5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$		0.25 0.25 0.25		0.25 0.25 0.25		0.25 0.25 0.25	V
V_{OH}		5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$	4.75 9.75 14.75		4.75 9.75 14.75		4.75 9.75 14.75		V
V_{IL}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V, $\|IO\| < 10\mu A$ VO = 1.5V, 13.5V		1.0 2.0 2.5		1.0 2.0 2.5		1.0 2.0 2.5	V
	Unbuffered	5 10 15	VO = 1V, 4V VO = 2V, 8V $\|IO\| < 10\mu A$ VO = 2.5V, 12.5V		1.0 2.0 2.5		1.0 2.0 2.5		1.0 2.0 2.5	V
V_{IH}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V $\|IO\| < 10\mu A$ VO = 1.5V, 13.5V	4.0 8.0 12.5		4.0 8.0 12.5		4.0 8.0 12.5		V
	Unbuffered	5 10 15	VO = 1V, 4V VO = 2V, 8V $\|IO\| < 10\mu A$ VO = 2.5V, 12.5V	4.0 8.0 12.5		4.0 8.0 12.5		4.0 8.0 12.5		V
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		± 100		± 100		± 100	nA
I_{OL}/I_{OH}			Per Applicable Rel Electrical Test Spec (RETS)	Minimum Limit is 75% of Published Data Sheet Limit						
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}			Per Applicable Rel Electrical Test Spec (RETS)	Maximum Limit is 125% of Published Data Sheet Limit						
Functionality		Devices Will Pass Functional Test per Applicable Truth Table								

NOTE 1: For other device parameters, see individual device specifications.

TABLE II-C. POST-RADIATION SPECIFICATION 10^7 RADS (Si)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1) −55°C Min	−55°C Max	+25°C Min	+25°C Max	+1215°C Min	+1215°C Max	UNITS
I_{DD}	Gate	5	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations		3.0		3.0		10	μA
		10			4.0		4.0		15	
		15			5.0		5.0		20	
	Buffer F/F	5			3.0		3.0		5.0	μA
		10			4.0		4.0		10	
		15			5.0		5.0		20	
	MSI	5			5.0		5.0		50	μA
		10			7.5		7.5		75	
		15			10.0		10.0		100	
	LSI	5			50		50		500	μA
		10			100		100		750	
		15			200		200		1000	
V_{OL}		5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert IO \rvert < 10\mu A$		0.5		0.5		0.5	V
		10			0.5		0.5		0.5	
		15			0.5		0.5		0.5	
V_{OH}		5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert IO \rvert < 10\mu A$	4.5		4.5		4.5		V
		10		9.5		9.5		9.5		
		15		14.5		14.5		14.5		
V_{IL}	Buffered	5	VO = 0.5V, 4.5V		1.0		1.0		1.0	V
		10	VO = 1V, 9V, $\lvert IO \rvert < 10\mu A$		2.0		2.0		2.0	
		15	VO = 1.5V, 13.5V		2.5		2.5		2.5	
	Unbuffered	5	VO = 1V, 4V		1.0		1.0		1.0	V
		10	VO = 2V, 8V $\lvert IO \rvert < 10\mu A$		2.0		2.0		2.0	
		15	VO = 2.5V, 12.5V		2.5		2.5		2.5	
V_{IH}	Buffered	5	VO = 0.5V, 4.5V	4.0		4.0		4.0		V
		10	VO = 1V, 9V $\lvert IO \rvert < 10\mu A$	8.0		8.0		8.0		
		15	VO = 1.5V, 13.5V	12.5		12.5		12.5		
	Unbuffered	5	VO = 1V, 4V	4.0		4.0		4.0		V
		10	VO = 2V, 8V $\lvert IO \rvert < 10\mu A$	8.0		8.0		8.0		
		15	VO = 2.5V, 12.5V	12.5		12.5		12.5		
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		± 100		± 100		± 100	nA
I_{OL}/I_{OH}			Per Applicable Rel Electrical Test Spec (RETS)	Minimum Limit is 65% of Published Data Sheet Limit						
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}			Per Applicable Rel Electrical Test Spec (RETS)	Maximum Limit is 140% of Published Data Sheet Limit						
Functionality			Devices Will Pass Functional Test per Applicable Truth Table							

NOTE 1: For other device parameters, see individual device specifications.

TABLE III. POST-RADIATION SPECIFICATION COMPARISON (25°C)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1) 10^5 Rads (Si) Min	10^5 Rads (Si) Max	10^6 Rads (Si) Min	10^6 Rads (Si) Max	10^7 Rads (Si) Min	10^7 Rads (Si) Max	UNITS
I_{DD}	Gate	5	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations		0.02		0.5		3.0	μA
		10			0.04		0.75		4.0	
		15			0.075		1.0		5.0	
	Buffer F/F	5			0.3		0.25		3.0	μA
		10			0.4		0.5		4.0	
		15			0.5		1.0		5.0	
	MSI	5			0.3		3.0		5.0	μA
		10			0.4		4.0		7.5	
		15			0.5		5.0		10.0	
	LSI	5			10		25		50	μA
		10			20		50		100	
		15			40		100		200	
V_{OL}		5	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$		0.05		0.25		0.5	V
		10			0.05		0.25		0.5	
		15			0.05		0.25		0.5	
V_{OH}		5	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$	4.95		4.75		4.5		V
		10		9.95		9.75		9.5		
		15		14.95		14.75		14.5		
V_{IL}	Buffered	5	VO = 0.5V, 4.5V		1.5		1.0		1.0	V
		10	VO = 1V, 9V, $\|IO\| < 10\mu A$		3.0		2.0		2.0	
		15	VO = 1.5V, 13.5V		4.0		2.5		2.5	
	Unbuffered	5	VO = Note 2 $\|IO\| < 10\mu A$		1.5		1.0		1.0	V
		10			3.0		2.0		2.0	
		15			4.0		2.5		2.5	
V_{IH}	Buffered	5	VO = 0.5V, 4.5V	3.5		4.0		4.0		V
		10	VO = 1V, 9V $\|IO\| < 10\mu A$	7.0		8.0		8.0		
		15	VO = 1.5V, 13.5V	11		12.5		12.5		
	Unbuffered	5	VO = Note 2 $\|IO\| < 10\mu A$	3.5		4.0		4.0		V
		10		7.0		8.0		8.0		
		15		11		12.5		12.5		
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		±10		±100		±100	nA
I_{OL}/I_{OH}			Per Applicable Rel Electrical Test Spec (RETS)	Data Sheet Limit		75% of Data Sheet		60% of Data Sheet		
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}			Per Applicable Rel Electrical Test Spec (RETS)		Data Sheet		125% of Data Sheet		140% of Data Sheet	
Functionality			Devices Will Pass Functional Test per Applicable Truth Table							

NOTE 1: All 10^5 rads (Si) limits allow no degradation from published data sheet limits.

NOTE 2: At 10^5 rads (Si), VO will be 10% or 90% of V_{DD}; at 10^6 or 10^7 rads (Si), VO will be 1V or 4V at V_{DD} = 5V, 2V or 8V at V_{DD} = 10V, and 2.5V or 12.5V at V_{DD} = 15V.

Dose Rate Performance

When CMOS ICs are subjected to large bursts of ionizing radiation, hole-electron pairs are created in the silicon substrate. The resultant current flowing through the high resistivity P- and N-substrates can cause voltage differences which may impair circuit performance in one of the following ways.

One: LATCH-UP

A CMOS circuit contains the structural elements required to form a four-layered Schockley diode switching device as illustrated in Figure 8. The emitter-base junctions of the lateral PNP and vertical NPN which comprise the Schockley diode are normally prevented from becoming forward-biased by the circuit metallization. Because of this, the Schockley diode will be in the off state during normal circuit operation and will pose no threat to reliable circuit performance.

Sufficiently high values of burst radiation can cause currents to flow through substrate resistances, R_{N-} and R_{P-}, to cause forward-biasing of the parasitic PNP and NPN emitter-base junctions and turn on the Schockley diode. The excessive flow of supply current which accompanies turn-on of the Schockley diode has been found to occur in the range of 10^8 to 10^{11} rads (Si)/sec on many CMOS circuits.

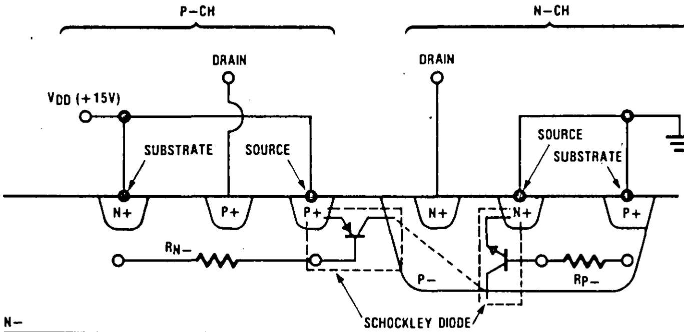

FIGURE 8: CROSS SECTION OF CMOS CIRCUIT ELEMENTS WHICH MAY LEAD TO LATCH-UP DURING IONIZING RADIATION BURSTS

The basic circuit required for latch-up to occur is illustrated in Figure 9. It consists of a parasitic bipolar NPN and PNP transistor sharing a common collector-base junction. The two requirements necessary for turn on of this device are:

1. The product of the common emitter current gains of the two devices, β and β_{PNP} must satisfy the relationship $(\beta_{NPN})(\beta_{PNP}) \geq 1$, and
2. The emitter-base junction of the two transistors must remain forward-biased to about 0.6V or greater after the NPNP device has been turned on.

In normal operation, condition No. 1 may be met, but condition No. 2 will not be met, permitting latch-up-free operation.

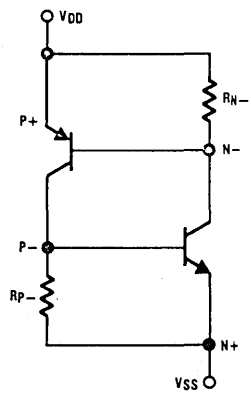

FIGURE 9: LATCH-UP EQUIVALENT CIRCUIT FOR BULK CMOS STRUCTURE

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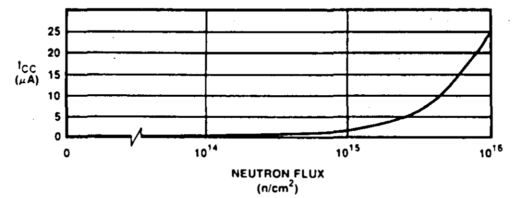
This problem can be completely eliminated by reducing to less than unity the product of the common emitter current gains of the NPN and PNP devices comprising the Schockley diode. One technique which has been successfully employed to eliminate the latch-up problem has been the use of neutron irradiation to lower minority carrier lifetime in the silicon substrate which directly affects parasitic bipolar current gains. As the values in Table IV indicate, neutron treatment of parts which exhibit latch-up at 3×10^8 and 3×10^9 rads (Si)/sec resulted in latch-up-free operation up to the limit of the burst simulation equipment, 10^{10} rads (Si)/sec.

TABLE IV. LATCH-UP PERFORMANCE

DEVICE	V_{DD}	DOSE REQUIRED FOR LATCH-UP		UNITS
		CONTROL (NON-NEUTRON TREATED)	NEUTRON TREATED*	
CD4006	10V	$>9.4 \times 10^9$	$>9.4 \times 10^9$	Rads (Si)/sec
CD4011	10V	3.1×10^9	$>9.4 \times 10^9$	Rads (Si)/sec
CD4012	10V	2.0×10^9	$>2.4 \times 10^9$	Rads (Si)/sec
CD4053	10V	3.2×10^8	$>9.4 \times 10^9$	Rads (Si)/sec
MM54C200	5V	$>2.2 \times 10^{10}$	$>8.8 \times 10^{11}$	Rads (Si)/sec

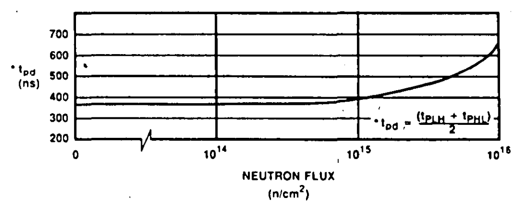
*Neutron treated parts were subjected to a neutron flux of 1×10^{14} neutrons (fast)/cm^2.

By treating wafers with neutron fluxes on the order of 10^{14}/cm^2, this enhanced circuit performance is obtained without sacrificing parametric performance. This is illustrated in Figures 10 and 11, which plot supply drain and propagation delay, respectively, versus neutron flux and show no significant degradation at the 10^{14}/cm^2 level.



DEVICE USED: MM54C200D/RH
(256-BIT RAM)

FIGURE 10: DEVICE QUIESCENT SUPPLY CURRENT VS. NEUTRON FLUX



DEVICE USED: MM54C200D/RH
(256-BIT RAM)

FIGURE 11: PROPAGATION DELAY VS. NEUTRON FLUX

Another very successful method that has been used to reduce susceptibility to dose rate induced latch-up has been to use low resistivity substrate material with a high resistivity epitaxial layer. This structure introduces a low impedance shunt across R_{N-} in Figure 9, and hence prevents latch-up. Using this technique, devices can be supplied which do not latch-up even when exposed to dose rates of 10^{12} rads/sec.

Two: DATA-UPSET

This effect results in the loss of stored data in a circuit after being subjected to burst radiation. It is typically of most concern in circuits such as memories and shift registers, where stored data bits are not directly coupled to circuit inputs. The problem is again caused by electron hole pair generation during ionizing burst radiation exposure. The resulting photo currents can cause a current flow across a normally reverse-biased PN junction. This current flow can upset the logic level stored at a node associated with the PN junction.

Table V shows the effect that neutron treatment of an MM54C200D/RH 256-bit static RAM has on the dose rate at which upset occurs. The effect of neutron fluxes on data upset is not nearly as dramatic as it is in the case of latch-up. Although neutron fluxes in excess of 10^{15}/cm^2 cause significant alterations in semiconductor material properties and circuit electrical parameters, Figures 10 and 11 indicate that the circuits tested would still meet data sheet requirements after irradiation in excess of 2×10^{15}/cm^2. At this level the tolerance to data upset exhibits about a

TABLE V. DATA UPSET PERFORMANCE

NEUTRON FLUX (N·FAST/cm⁶)	DOSE RATE NEEDED TO INDUCE DATA UPSET		UNITS
	CD4006D 18-BIT SHIFT REGISTER $V_{DD} = 10V$	MM54C200D (MEMORY ENABLED) 256-BIT RAM, $V_{DD} = 5V$	
0 (control)	4.7×10^8	1.76×10^8	Rads (Si)/sec
1×10^{14}	4.7×10^8	2.00×10^8	Rads (Si)/sec
1×10^{15}	—	5.00×10^8	Rads (Si)/sec
1×10^{16}	—	1.17×10^9	Rads (Si)/sec

threshold improvement over untreated devices. Almost an entire order of magnitude improvements in data upset tolerance can be obtained with treatment at $10^{16}/cm^2$ if the user can tolerate the degraded propagation delay and increased supply current drain occurring at this level.

Rad Hard CMOS Reliability

Radiation hardness, however, is of no value to the system user if it is accomplished at the sacrifice of device reliability. To confirm device reliability, each of 476 units from five lots were subjected to 2.016 hours of burn-in at 125°C. The total device hours were 804,384, which represents a projected 0.11%/1000 hours failure rate at a 60% confidence level. This falls well within the reliability requirements of even the most stringent programs.

In addition to this initial sampling, 100% burn-in screening, as well as operating life testing, has been performed on many lots that have been produced for various customers. The results of this additional testing have continued to demonstrate that rad hard devices are reliable. 10,000-hour life tests are currently underway to further establish long-term reliability. The results of this testing and further testing across our entire rad hard product line will be added to the existing data as they become available.

Radiation Hardened Linear Devices

Although most bipolar logic devices tend to be inherently hard when exposed to total-dose gamma radiation, many bipolar linear devices will begin to degrade when exposed to relatively low levels of such radiation. The causes are similar to those seen in MOS radiation exposure-related failures. Linear devices are more susceptible to low current β degradation than most bipolar technologies. A major cause of of low current β degradation is surface leakage across the emitter-base junction. This surface leakage, like MOS characteristics, is related to the oxide and interface charges which are induced by high levels of radiation.

The solution to linear radiation problems, however, is quite different from what we have described above for CMOS devices. Total modification of the fabrication process is needed in order to achieve megarad hardness on linear devices. We have developed megarad versions of the LM108A and LM101A. We have extensive research and development currently underway in this area, for we feel that a broad line of rad hard linear devices is essential if systems designers are to achieve total systems hardness.

Ordering Information

National Semiconductor's Radiation Hardened CMOS devices are available in three different levels of hardness, one of which is sure to satisfy the needs of your program. The levels available are 1×10^5 rads (Si), 1×10^6 rads (Si), and 1×10^7 rads (Si), with post-radiation test limits as defined in Table II-A, II-B, or II-C of this brochure (as applicable). Each of these can be obtained in either a bottom-brazed flatpack or in a side-brazed dual-in-line package, both of which have solder-sealed lids. In addition, these devices may be obtained with either Class S or Class B screening.* National Semiconductor's 883B/RETS and 883S/RETS microcircuits (which are described in more detail in other brochures) are fully compliant with the 100% screening requirements of Method 5004 and MIL-STD-883 for the applicable screening level and have met the applicable quality conformance requirements of Method 5005 of MIL-STD-883.

**National Semiconductor has qualified a number of Radiation Hardened devices in accordance with MIL-M-38510, and*

Ordering is quite simple. Parts may be ordered using one of the following part number structures (as applicable).

CD4093BM W / R H 6 S

- S — Screening Level
  - S = Class S
  - B = Class B
- 6 — Radiation Hardness Level
  - 5 = 1 x 10^5 rads (Si)
  - 6 = 1 x 10^6 rads (Si)
  - 7 = 1 x 10^7 rads (Si)
- H — Indicates Hardness Type
  - H = Total dose hardened
  - E = Dose rate hardened
- R — Indicates Radiation Hardened Device
- W — Package Type
  - J = Side-brazed DIP
  - W = Bottom-brazed flat
  - E = Leadless chip carrier
- CD4093BM — Basic Device

J M38510 H 055 03 S F C

- C — Lead Finish
  - A = Solder DIP
  - B = Tin plate
  - C = Gold plate
- F — Package Type
  - A = 14-pin metal flat
  - C = 14-pin dual-in-line
  - D = 14-pin ceramic flat
  - E = 16-pin dual-in-line
  - F = 16-pin flat
- S — Screening Level
  - S = Class S
  - B = Class B
- 03 — Device on Detail Specification
- 055 — Detail Specification Number
- H — Radiation Level
  - M = 2500 rads (Si)
  - D = 1 x 10^4 rads (Si)
  - R = 1 x 10^5 rads (Si)
  - H = 1 x 10^6 rads (Si)
  - No MIL-M-38510 indicator exists for 10^7 rads
- M38510 — MIL-M-38510
- J — JAN Mark

In addition, we are willing to evaluate contractor-prepared prints for radiation hardened devices.

Radiation Susceptibility Testing

National Semiconductor has also recognized that there is a need on some programs for data relative to the actual hardness level of the product used, even where that product has not been specifically hardened. To address that need, National has developed a radiation susceptibility test program. The intent of this program is to provide, in advance of actual assembly of product, radiation tolerance data which will allow the user to determine whether those devices meet the radiation limits required by his program. Since the testing need not be done to a specific limit, this program is able to provide specific device data for those programs whose radiation tolerance limits are classified. Details on this program will be provided on request.

NATIONAL SEMICONDUCTOR'S MEGARAD RADIATION HARDENED PRODUCT LIST

The following device types were released as of December 1, 1983 by National Semiconductor as radiation hardened products to the 10^5, 10^6, 10^7 rads (Si) levels. These parts will be processed to National's 883S/RETS™ or 883B/RETS flow in the bottom-brazed flat ("F"), side-brazed dual-in-line ("D"), or ceramic ("J") and ("W") package configurations. This list supersedes and replaces all previously published lists.

IN DEVELOPMENT		
CD4006B MSI	MM54C08 SSI	MM54C30 SSI
CD4030B MSI	MM54C10 SSI	MM54C32 SSI
MM54C00 SSI	MM54C20 SSI	MM54C221 MSI
MM54C02 SSI		

RAD HARD CMOS

DEVICE	SERIES	DEVICE	SERIES	DEVICE	SERIES	DEVICE
CD4000 MSI	A	CD4030 SSI	A	CD4082 SSI	B	MM54C89 MSI
CD4001 SSI	A/B	CD4031 MSI	A/B	CD4093 SSI	B	MM54C160 MSI
CD4002 SSI	A/B	CD4034 MSI	B	CD4094 MSI	B	MM54C161 MSI
CD4006 MSI	A	CD4035 MSI	A/B	CD4099 MSI	B	MM54C162 MSI
CD4007 SSI	A/UB	CD4040 MSI	A/B	CD40106 SSI	B	MM54C163 MSI
CD4008 MSI	A/B	CD4041 SSI	A	CD40160 MSI	B	MM54C173 MSI
CD4009 SSI	A	CD4042 MSI	A/B	CD40161 MSI	B	MM54C174 MSI
CD4010 SSI	A	CD4043 MSI	A/B	CD40162 MSI	B	MM54C175 MSI
CD4011 SSI	A/B	CD4044 MSI	A/B	CD40163 MSI	B	MM54C192 MSI
CD4012 SSI	A/B	CD4046 MSI	B	CD40174 MSI	B	MM54C193 MSI
CD4013 MSI	A/B	CD4047 MSI	B	CD40192 MSI	B	MM54C200 LSI
CD4014 MSI	A/B	CD4048 SSI	A/B	CD40193 MSI	B	MM54C240 MSI
CD4015 MSI	A/B	CD4049 SSI	A/UB	CD4510 MSI	B	MM54C244 MSI
CD4016 MSI	A/B	CD4050 SSI	A/B	CD4512 MSI	B	MM54C374 MSI
CD4017 MSI	A/B	CD4051 MSI	A/B	CD4514 MSI	B	MM54C901 SSI
CD4018 MSI	A/B	CD4052 MSI	A/B	CD4516 MSI	B	MM54C902 SSI
CD4019 SSI	A/B	CD4053 MSI	A/B	CD4518 MSI	B	MM54C903 SSI
CD4020 MSI	A/B	CD4066 SSI	A/B	CD4520 MSI	B	MM54C904 SSI
CD4021 MSI	A/B	CD4069 SSI	A/UB	CD4528 MSI	B	MM54C905 MSI
CD4022 MSI	A/B	CD4070 SSI	B	CD4538B MSI	B	MM54C906 SSI
CD4023 SSI	A/B	CD4071 SSI	B	CD4584 SSI	B	MM54C907 SSI
CD4024 MSI	A/B	CD4072 SSI	B	CD4724 MSI		MM54C914 MSI
CD4025 SSI	A/B	CD4073 SSI	B	MM54C04 SSI		MM54C941 MSI
CD4027 MSI	A/B	CD4075 SSI	B	MM54C14 SSI		MM70C95 SSI
CD4028 MSI	A/B	CD4076 MSI	B	MM54C42 MSI		MM70C96 MSI
CD4029 MSI	A/B	CD4081 SSI	B	MM54C85 MSI		MM70C97 SSI
				MM54C86 SSI		MM70C98 MSI
				CD4515 MSI		MM78C29 MSI
						MM78C30 MSI

For additional information regarding these or National's upcoming radiation hardened products, please contact Kirk Lemon, Military/Aerospace Marketing Manager, at (408) 721-5999 — Mailstop D3684.

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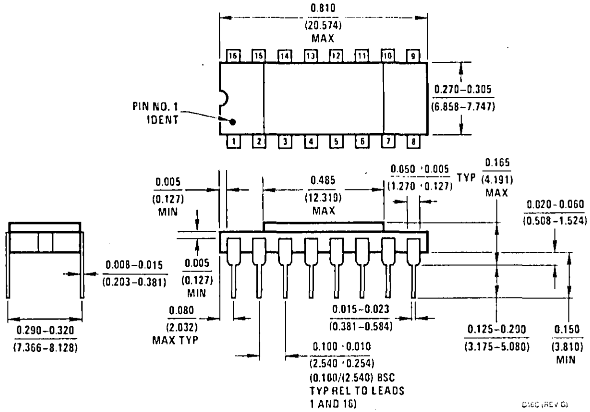
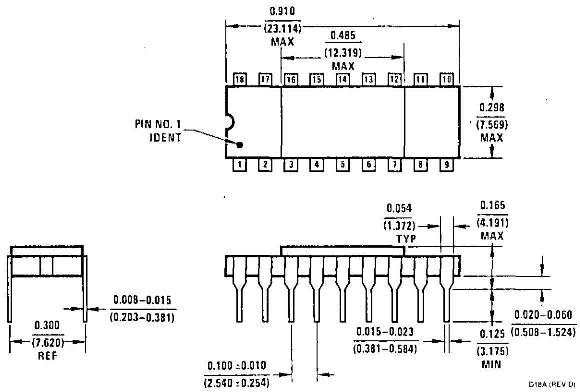
Section 16

Physical Dimensions

16



NS Package D16C
16-Lead Hermetic DIP (D)



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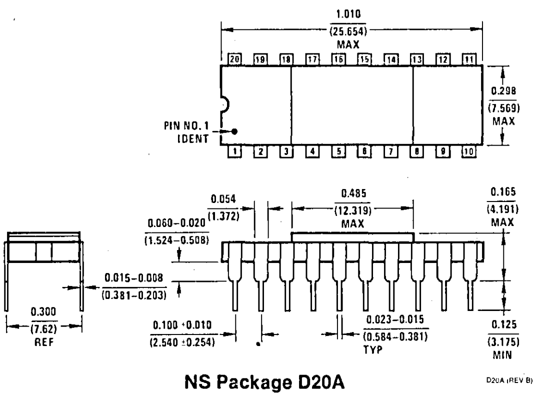

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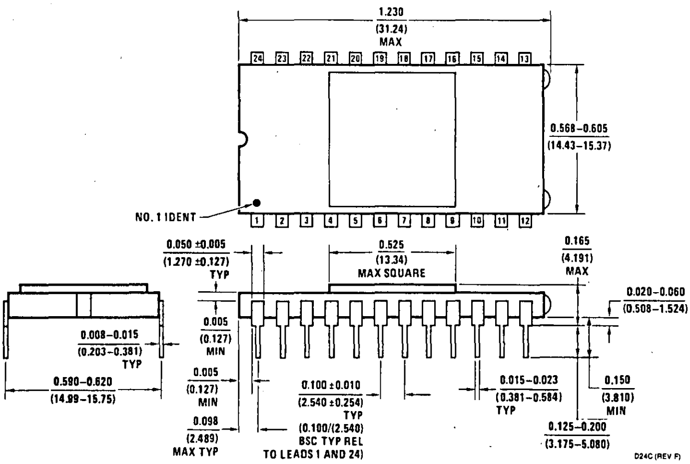

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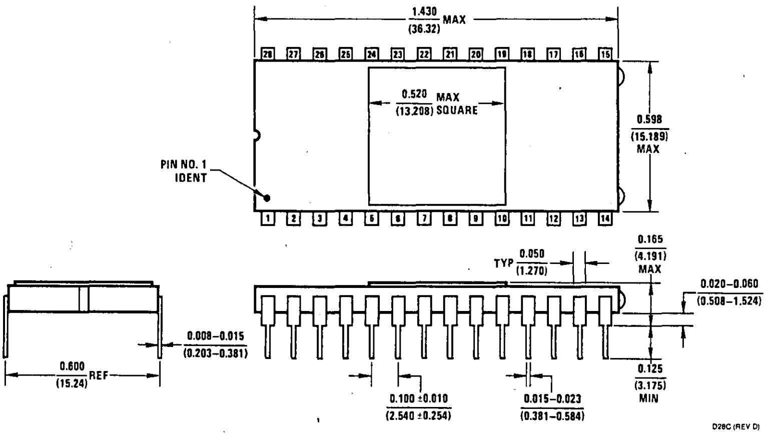

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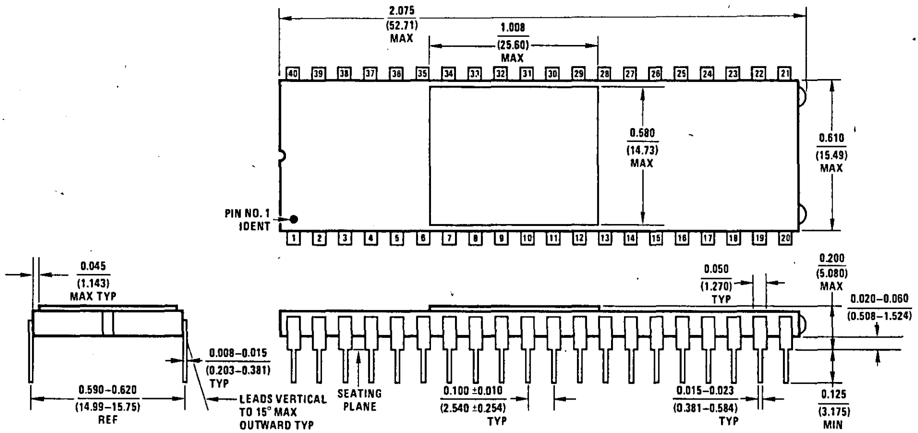

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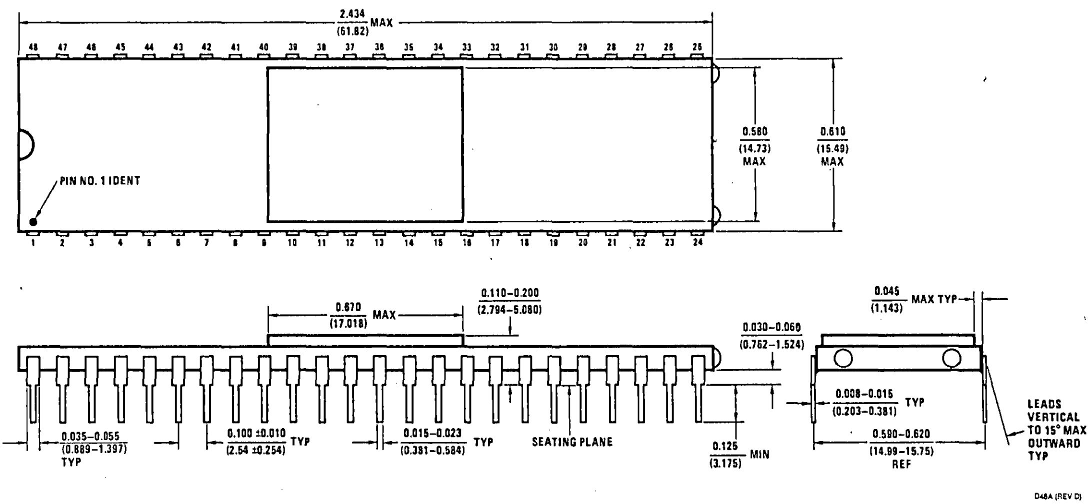

NS Package D48A
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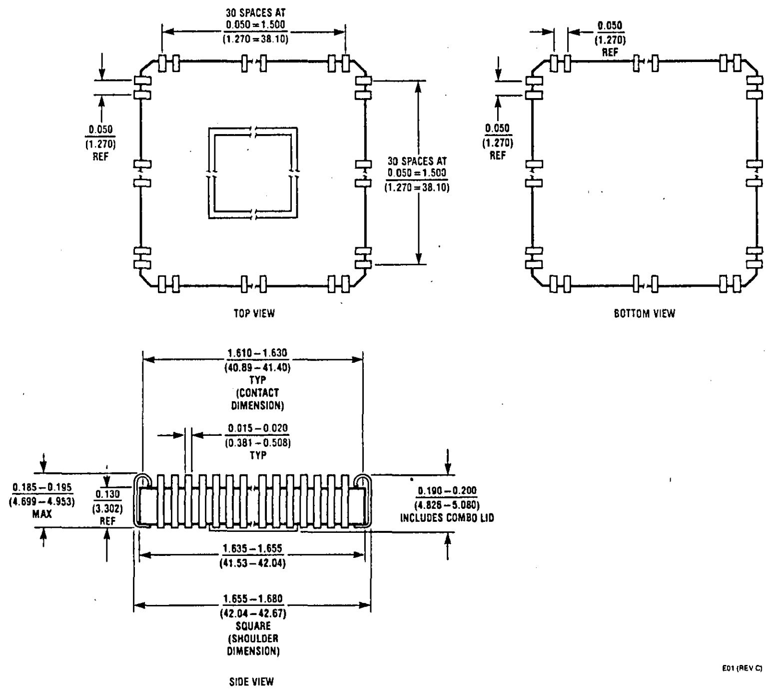
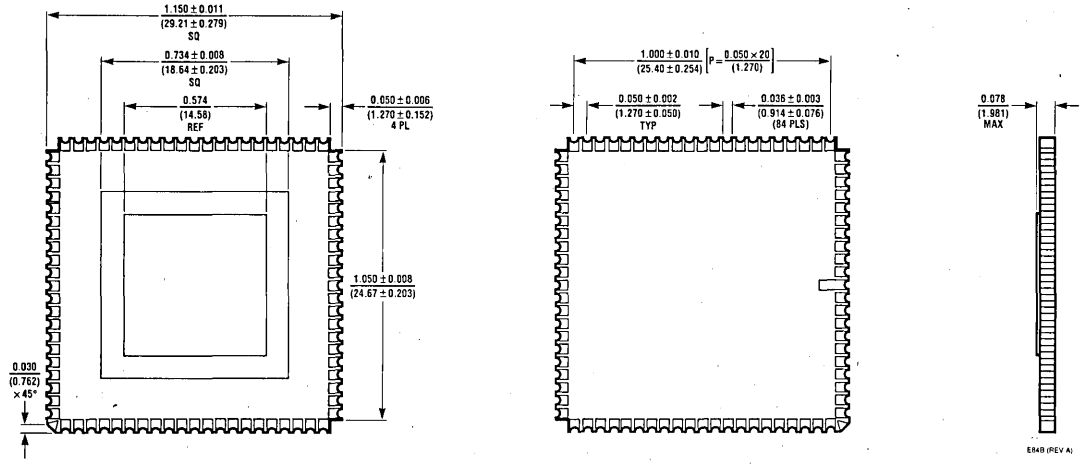
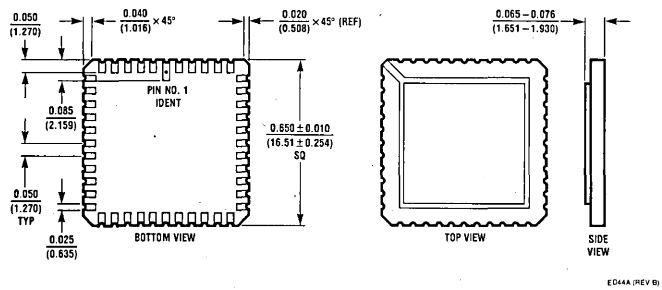


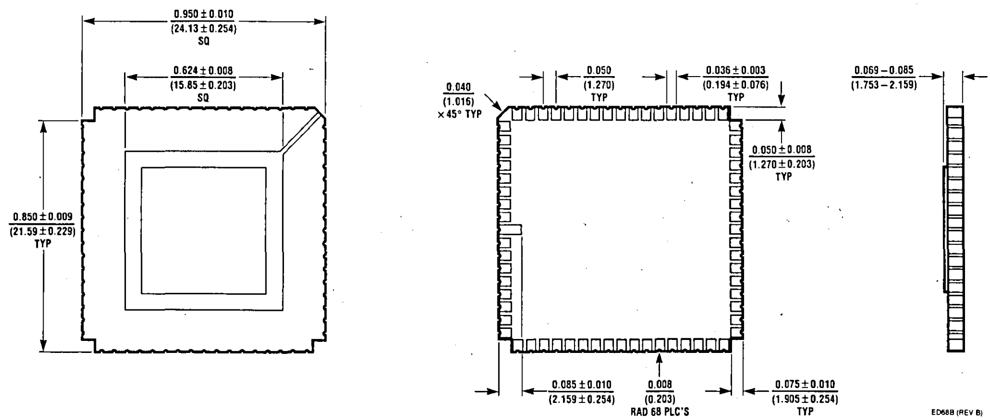
NS Package E01
124-Lead Ceramic Chip Carrier



NS Package E84B
84-Lead Chip Carrier (Type B)



NS Package ED44A
44-Pin Hermetic Leadless Package



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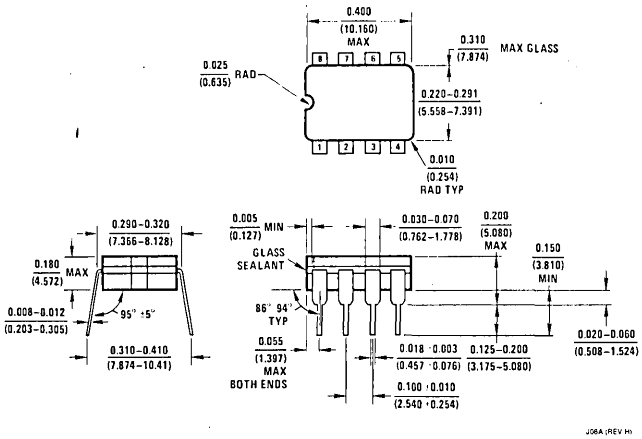
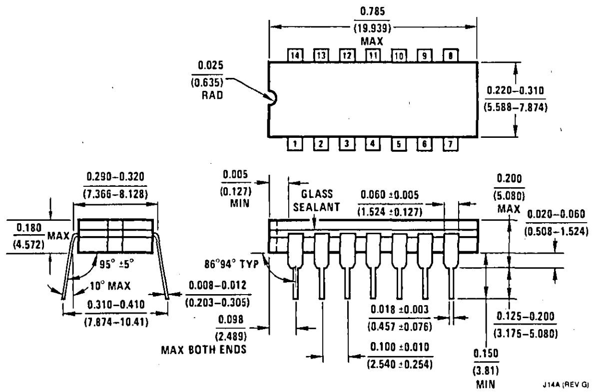
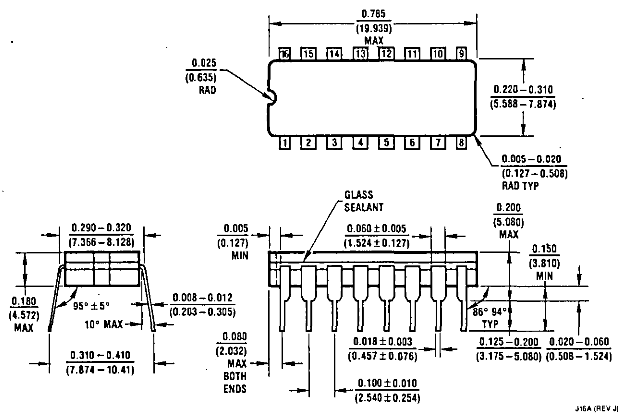
68-Lead Chip Carrier (Type B)



NS Package J08A
8-Lead CERDIP (J)



NS Package J14A
14-Lead CERDIP (J)



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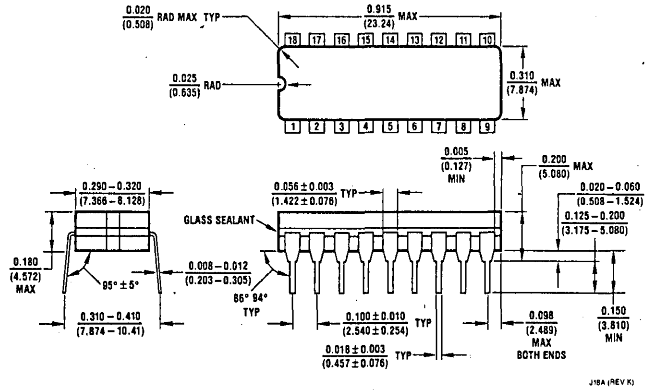

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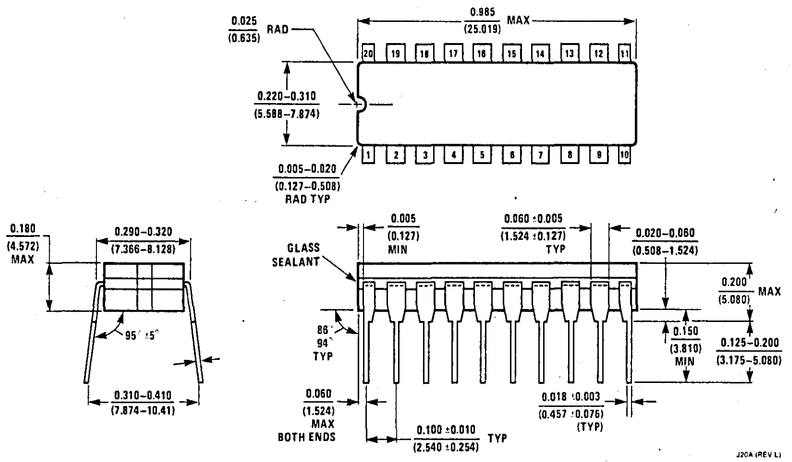
18-Lead CERDIP (J)



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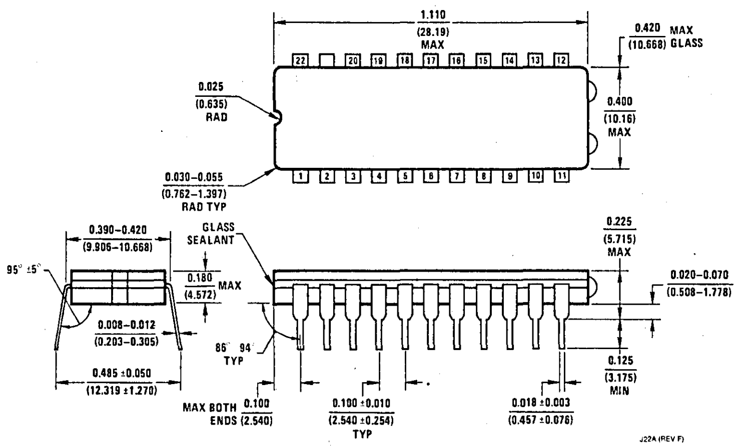
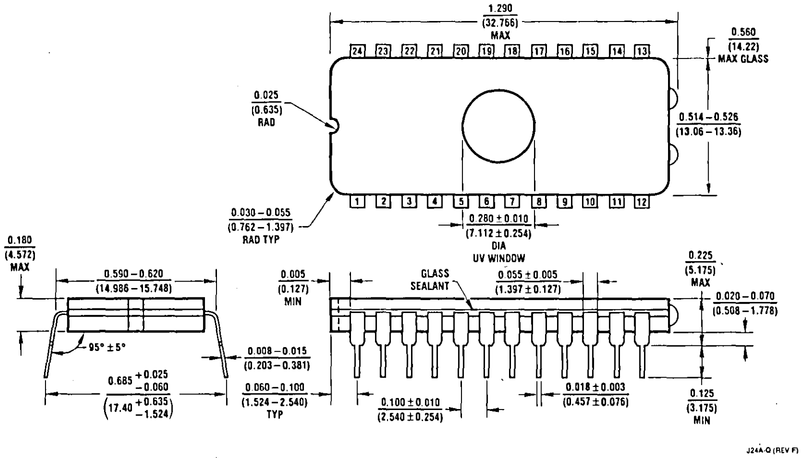
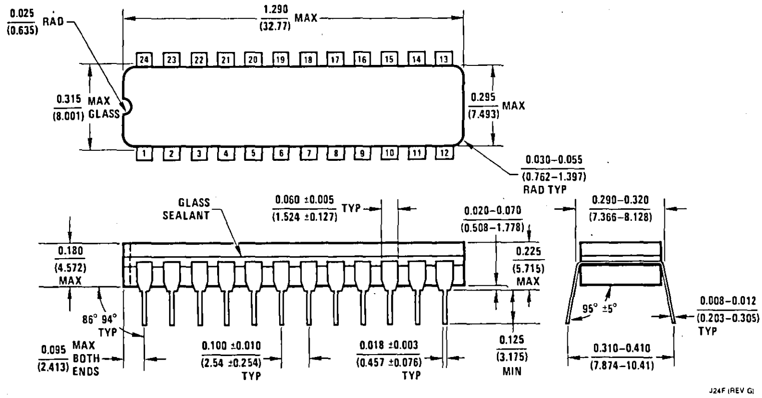
20-Lead CERDIP (J)



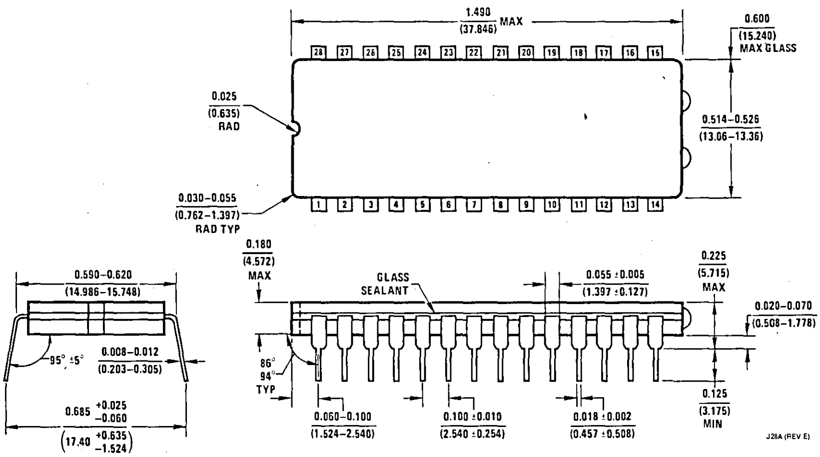
NS Package J22A
22-Lead CERDIP (J)



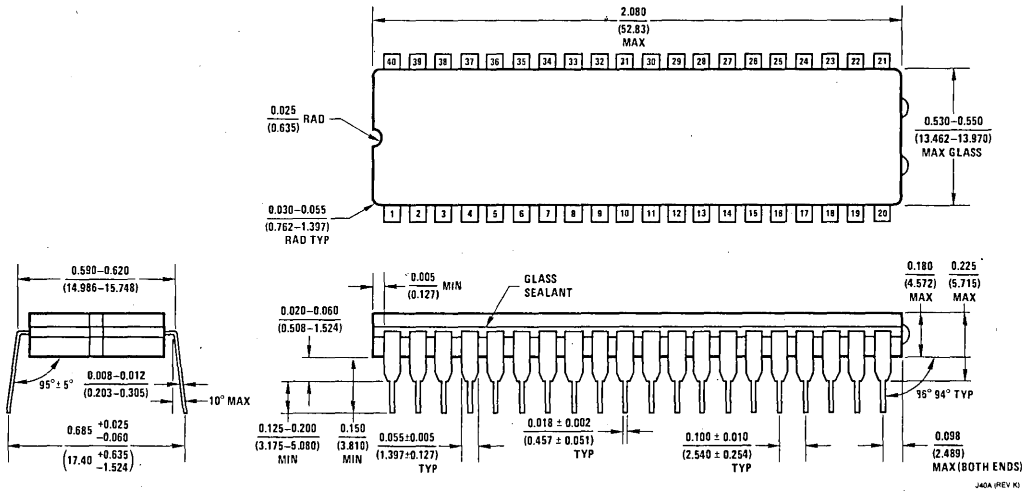
NS Package J24A-Q
24-Lead EPROM CERDIP (JQ)
Small Window



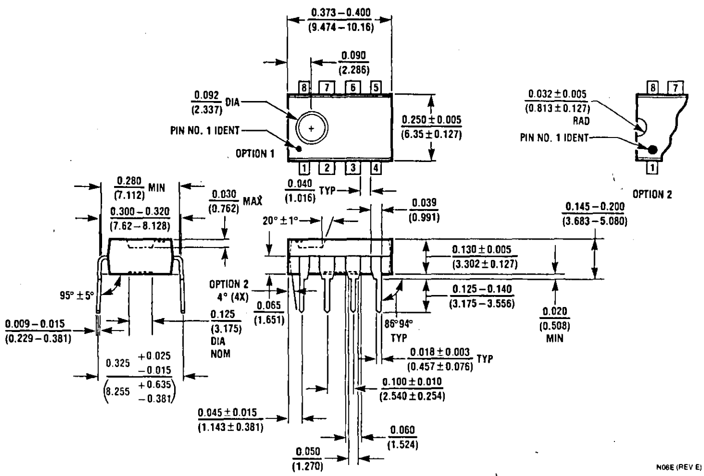
NS Package J24F
24-Lead CERDIP (J)
0.300 Centers



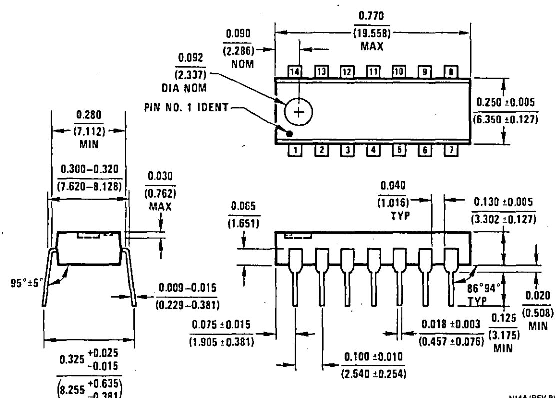
NS Package J28A
28-Lead CERDIP (J)



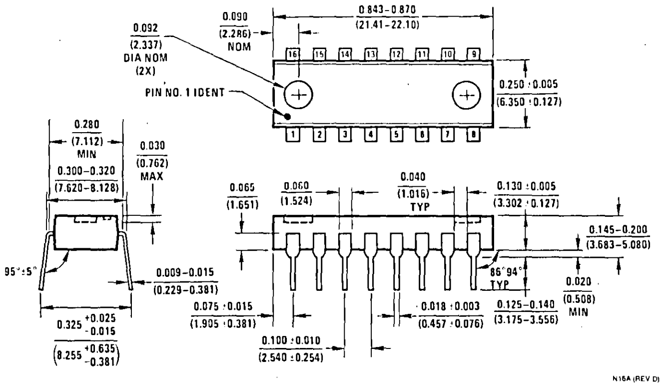
NS Package J40A
40-Lead CERDIP (J)



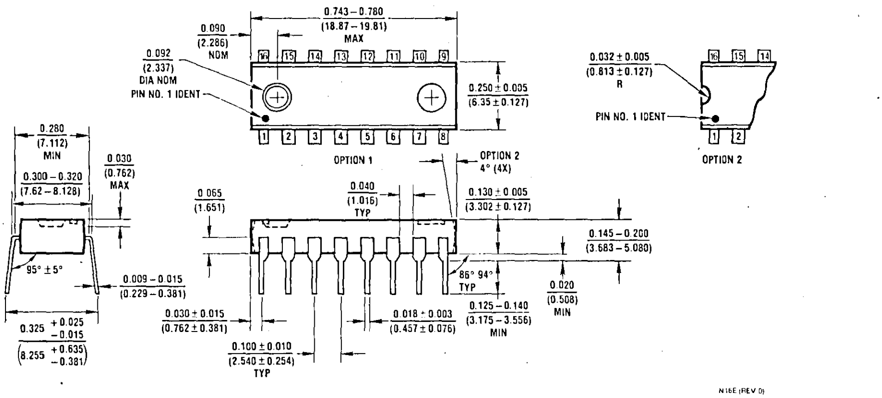
NS Package N08E
8-Lead Molded DIP (N)



NS Package N14A
14-Lead Molded DIP (N)



NS Package N16A
16-Lead Molded DIP (N)



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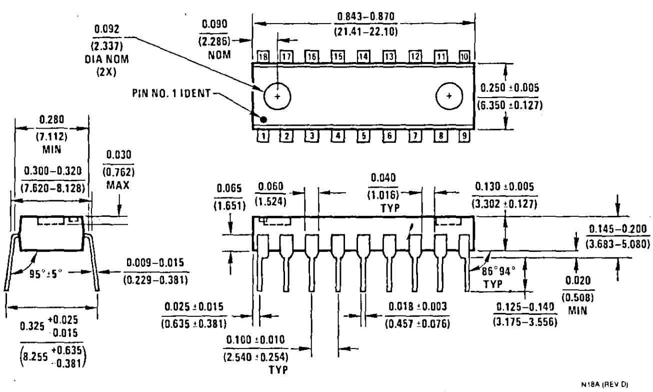
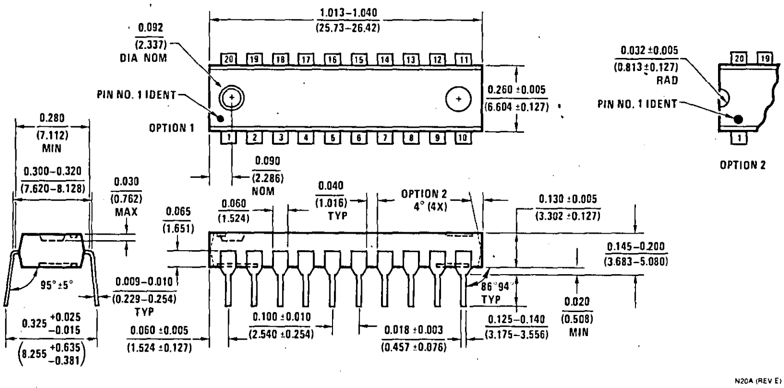
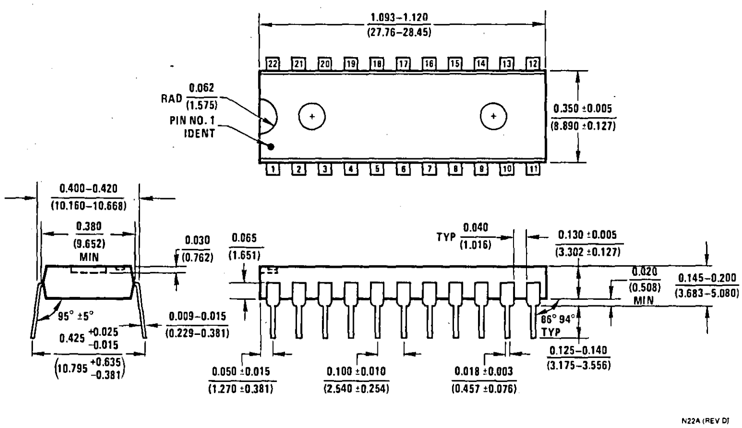


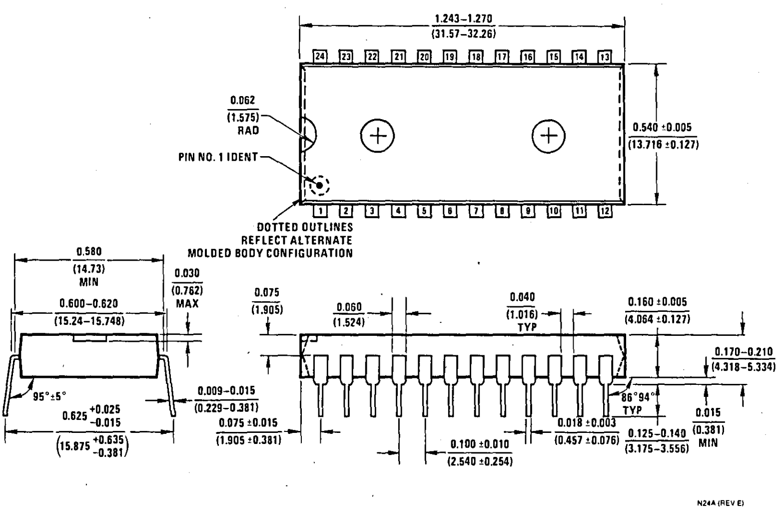
NS Package N18A
18-Lead Molded DIP (N)



NS Package N20A
20-Lead Molded DIP (N)



NS Package N22A
22-Lead Molded DIP (N)



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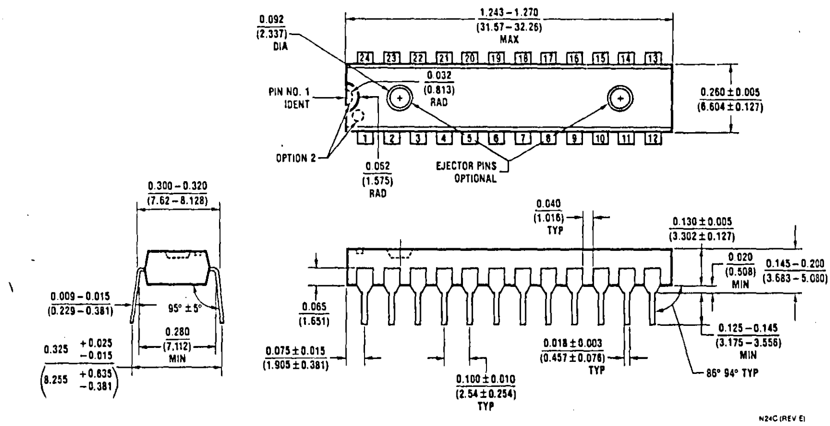
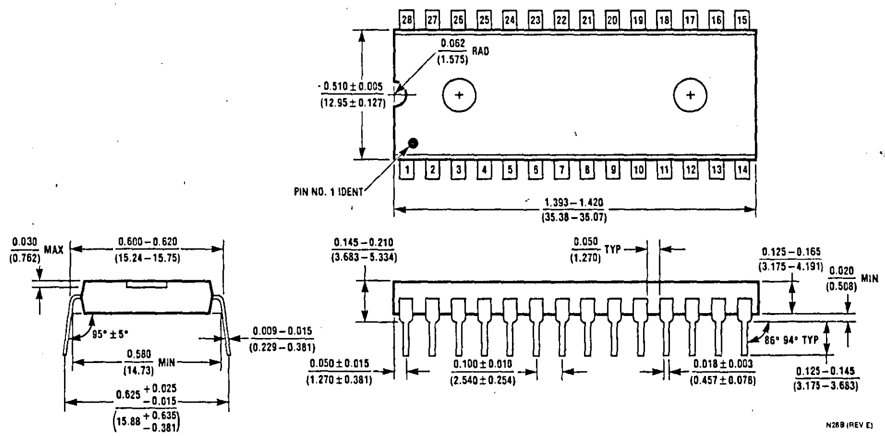
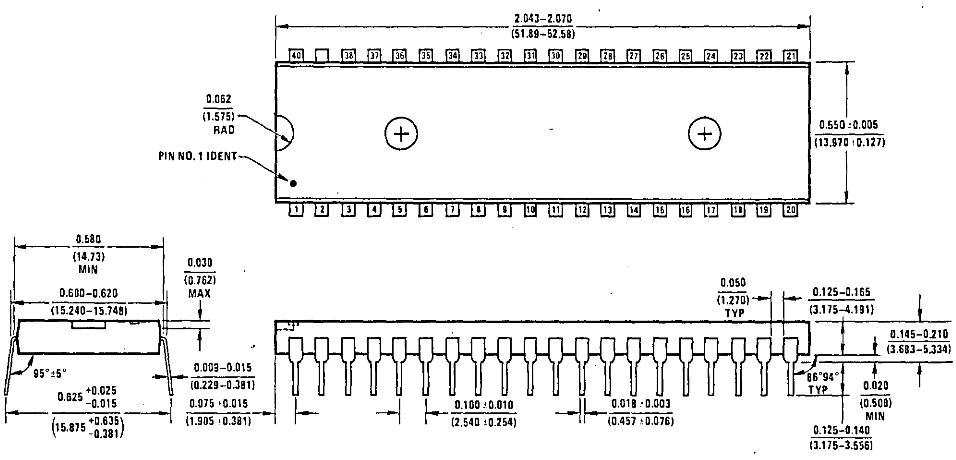
24-Lead Molded DIP (N)



NS Package N24C
24-Lead Skinny DIP (SD) Molded DIP (N)
0.300 Centers



NS Package N28B
28-Lead Molded DIP (N)



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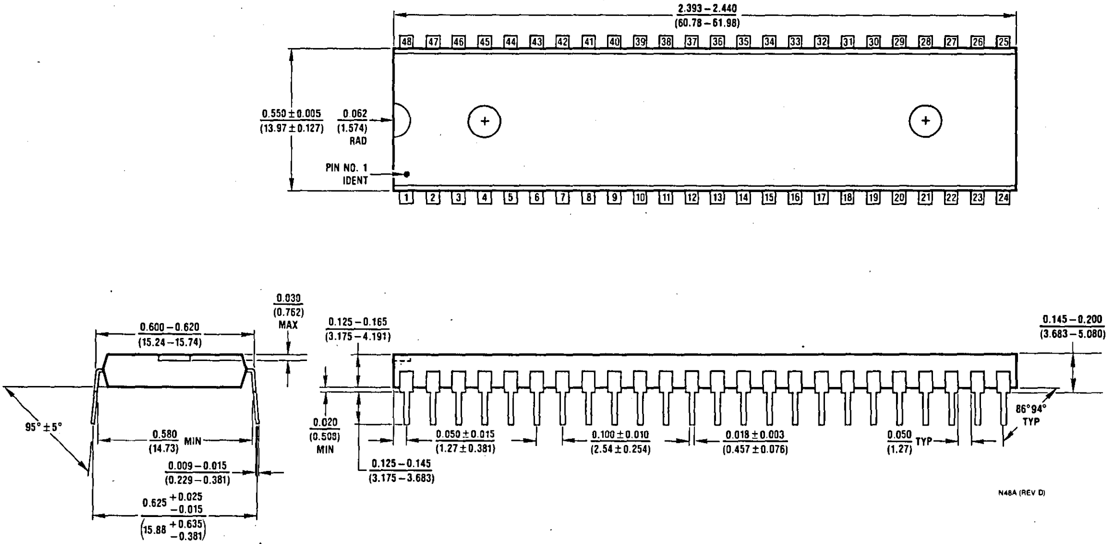
40-Lead Molded DIP (N)



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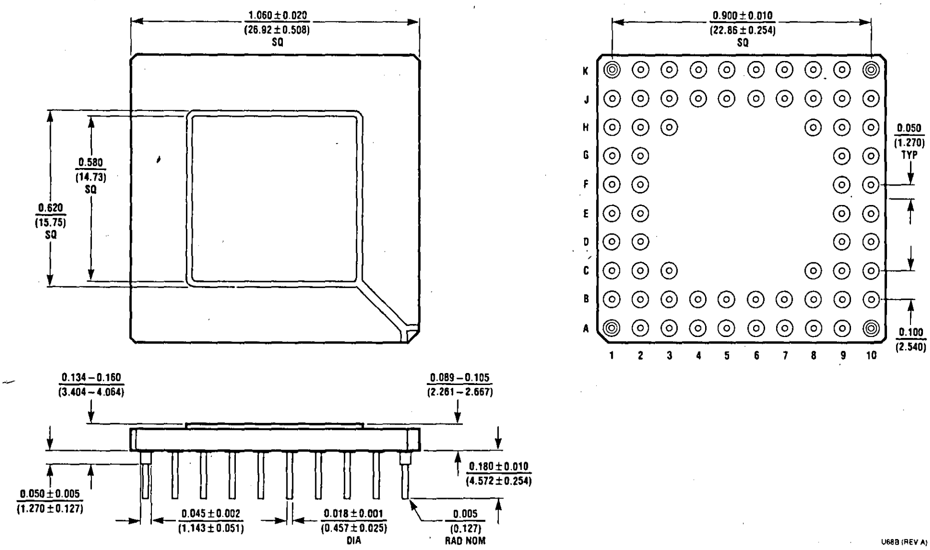
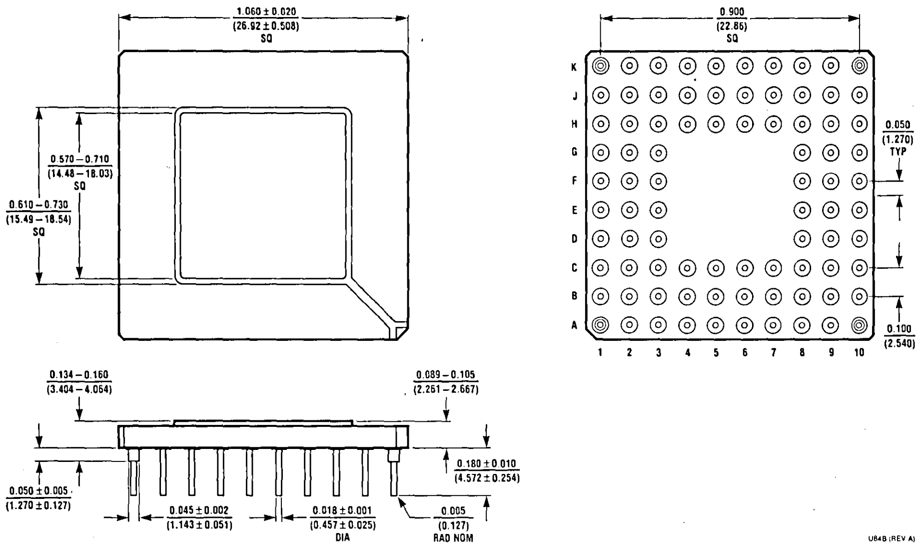
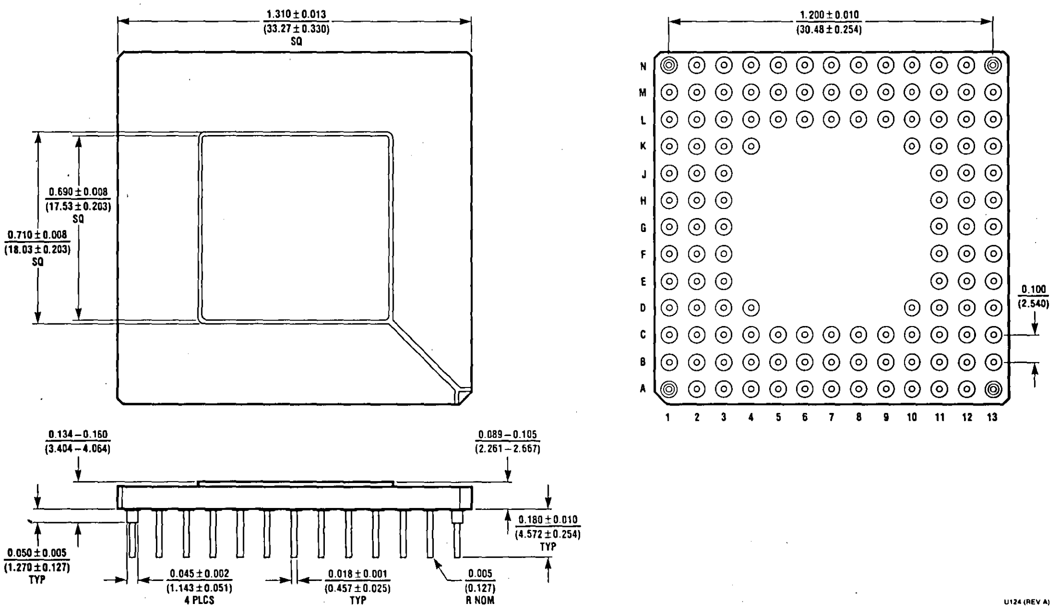


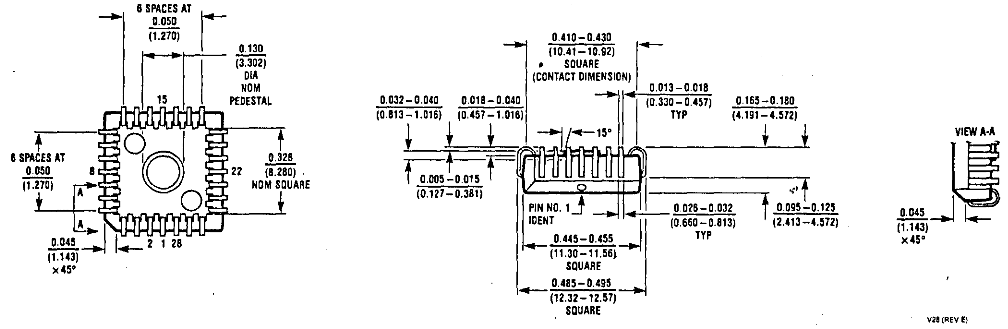
NS Package U68B
68-Pin Hermetic Grid Array Package
Ceramic Cavity Up



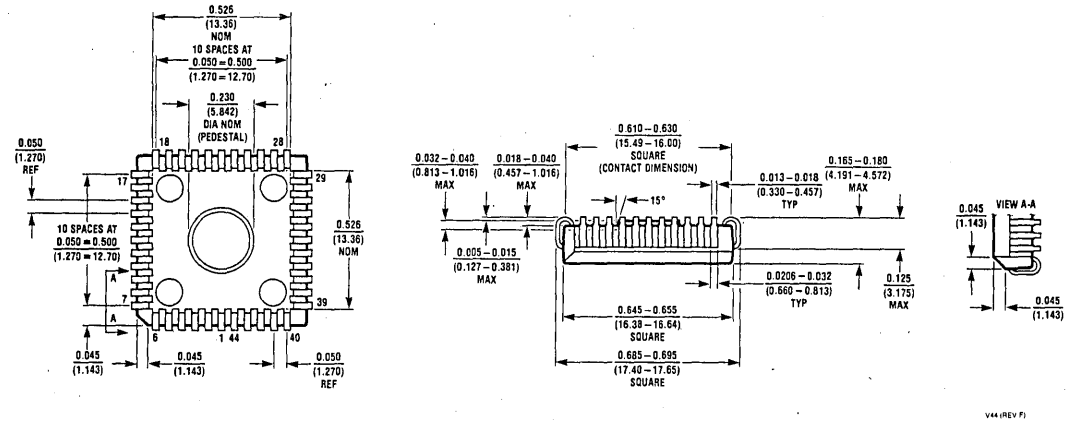
NS Package U84B
84-Pin Hermetic Grid Array Package



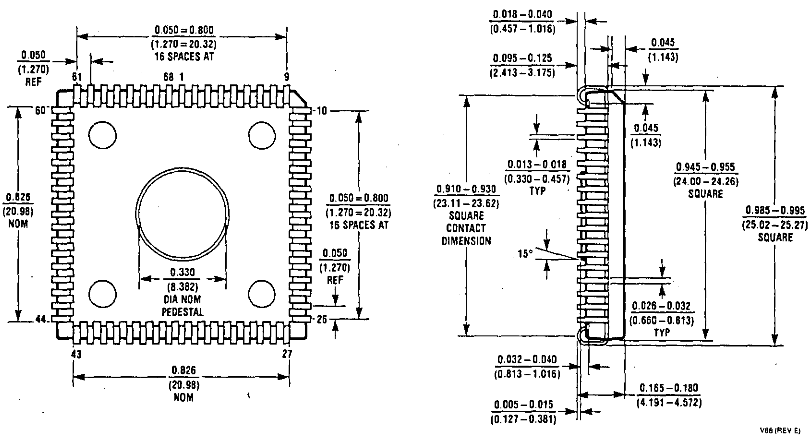
NS Package U124
124-Pin Hermetic Grid Array Package



NS Package V28
28-Lead Plastic Chip Carrier



NS Package V44
44-Lead Plastic Chip Carrier



NS Package V68
68-Lead Plastic Chip Carrier

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