1984

LOGIC DATABOOK

VOLUME II

National Semiconductor

LOGIC
DATABOOK
VOLUME II

NATIONAL SEMICONDUCTOR CORPORATION

- *ALS (Advanced Low Power Schottky)*
- *AS (Advanced Schottky)*
- *LS (Low Power Schottky)*
- *S (Schottky)*
- *TTL (Transistor-Transistor Logic)*
- *L (Low Power)*

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Introduction

This volume of the 1984 Logic Databook contains complete information on National Semiconductor's extensive bipolar logic families. Included in this publication are National's newer 5V bipolar families, AS and ALS, designed for use together in systems where both high speed and low power are important considerations. The AS family provides the fastest saturated logic circuits on the market, whereas ALS, at only one milliwatt per gate, minimizes power dissipation. Together, the two technologies provide the optimum power/speed solution. Additionally, the ALS/AS circuits are guaranteed over a ± 10% power supply range for both AC and DC.

Einleitung

Dieser Band des Logik-Datenbuchs 1984 enthält die vollständigen Informationen über das umfangreiche Spektrum der bipolaren Logikfamilien von National Semiconductor. Enthalten sind in diesem Buch auch die neueren 5-V-Bipolar-Familien von National, die AS- und ALS-Typen, die beide für die Verwendung in Systemen konzipiert sind, bei denen hohe Arbeitsgeschwindigkeit und geringe Stromaufnahme eine wichtige Rolle spielen. Die AS-Familie ist die schnellste Logik-Typenreiche in gesättigter Schaltungstechnik auf dem Markt, während die ALS-Familie mit nur 1 mW pro Gattor eine sehr geringe Verlustleistung aufweist. Insgesamt bieten die beiden Schaltungstechniken eine optimale Lösung in bezug auf das Geschwindigkeits-Leistungs-Verhältnis. Darüber hinaus sind die Gleich- und Wechselspannungs-Parameter über einen Betriebsspannungs-Bereich von ± 10% garantiert.

Introduction Bipolaire

Cette édition 1984 du Databook Logique contient une information exhaustive sur les familles logiques bipolaires de National Semiconductor. Dans cet ouvrage, figurent les plus récentes familles bipolaires 5 V de National, la AS et la ALS, concues toutes les deux pour etre utilisées dans les systèmes où se posent des problèmes de vitesse et de consommation.

La famille AS regroupe les circuits les plus rapides du marché en logique saturée, tandis que la famille ALS, avec une consommation de seulement 1 mW par porte, permet de minimiser la consommation. À elles deux, ces deux technologies fournissent le meilleur rapport consommation/vitesse. De plus, les circuits ALS/AS sont garantis à la tension d'alimentation à plus ou moins 10% que ce soit en alternatif ou en continu.

Introduzione

Il volume LOGIC DATABOOK 1984 contiene informazioni complete sulle famiglie logiche bipolari della National Semiconductor. Nella pubblicazione vengono descritte le nuovissime famiglie AS ed ALS. Progettate per essere utilizzate in sistemi, ove velocita e ridotti assorbimenti siano caratteristiche di primaria importanza. La famiglia AS e constituita da circuiti logici satura ti, i piu veloci presenti oggi sul mercato; le ALS, peraltro, con una dissipazione di un solo milliwatt per gate, e realizzata per minimizzare gli assorbimenti. Le due famiglie, insieme, rappresentano la soluzione ottimale per velocita/assorbimento. Oltre a cio, i dispositivi AS/ALS hanno i parametri sia AC che DC, caraterizzati da una variazione della tensione di alimentazione ± 10%.

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Section 1
Introduction to Bipolar Logic

1

Section Contents

Guide to Bipolar Logic Device Families

Since the introduction of the first saturating logic bipolar integrated circuit family (DM54/DM74), there have been many developments in the process and manufacturing technologies as well as circuit design techniques which have produced new generations (families) of bipolar logic devices. Each generation had advantages and disadvantages over the previous generations. Today National provides six bipolar logic families.

TTL	(DM54/DM74)
Low Power	(DM54L/DM74L)
Low Power Schottky	(DM54LS/DM74LS)
Advanced Low Power Schottky	(DM54ALS/DM74ALS)
Schottky	(DM54S/DM74S)
Advanced Schottky	(DM54AS/DM74AS)

TTL LOGIC (DM54/DM74)

TTL logic was the first saturating logic integrated circuit family introduced, thus setting the standard for all the future families. It offers a combination of speed, power consumption, output source and sink capabilities suitable for most applications. This family offers the greatest variety of logic functions. The basic gate (see *Figure 1*) features a multiple-emitter input configuration for fast switching speeds, active pull-up output to provide a low driving source impedance which also improves noise margin and device speed. Typical device power dissipation is 10 mW per gate and the typical propagation delay is 10 ns when driving a 15 pF/400Ω load.

LOW POWER (DM54L/DM74L)

The low power family has essentially the same circuit configuration as the TTL devices. The resistor values, however, are increased by nearly tenfold, which results in tremendous reduction of power dissipation to less than 1/10 of the TTL family. Because of this reduction of power, the device speed is sacrificed. The propagation delays are increased threefold. These devices have a typical power dissipation of 1 mW per gate and typical propagation delay of 33 ns, making this family ideal for applications where power consumption and heat dissipation are the critical parameters.

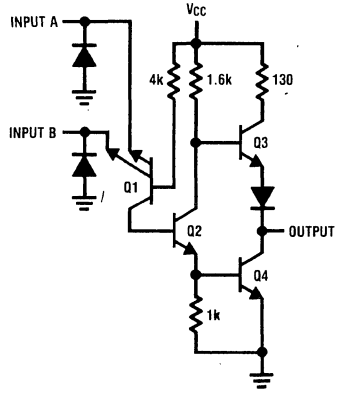


FIGURE 1. DM5400/DM7400

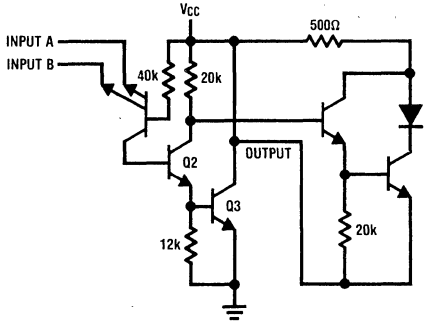


FIGURE 2. DM54L00/DM74L00

LOW POWER SCHOTTKY (DM54LS/DM74LS)

The low power Schottky family features a combined fivefold reduction in current and power when compared to the TTL family. Gold doping commonly used in the TTL devices reduces switching times at the expense of current gain. The LS process overcomes this limitation by using a surface barrier diode (Schottky diode) in the baker clamp configuration between the base and collector junction of the transistor. In this way, the transistor is never fully saturated and recovers quickly when base drive is interrupted. Using shallower diffusion and soft-saturating Schottky diode clamped transistors, higher current gains and faster turn-on times are obtained. The LS circuits do not use the multi-emitter inputs. They use diode-transistor inputs which are faster and give increased input breakdown voltage; the input threshold is ~0.1V lower than TTL. Another commonly used input is the vertical substrate PNP transistor. In addition to fast switching, it exhibits very high impedance at both the high and low input states, and the transistor's current gain (B) significantly reduces input loading and provides better output performance. The output structure is also modified with a Darlington transistor pair to increase speed and improve drive capability. An active pull-down transistor (Q3) is incorporated to yield a symmetrical transfer characteristic (squaring network). This family achieves circuit performance exceeding the standard TTL family at fractions of its power consumption. The typical device power dissipation is 2 mW per gate and typical propagation delay is 10 ns while driving a 15 pF/2 kΩ load.

SCHOTTKY (DM54S/DM74S)

This family features the high switching speed of unsaturated bipolar emitter-coupled logic, but consumes more power than standard TTL devices. To achieve this high speed, the Schottky barrier diode is incorporated as a clamp to divert the excess base current and to prevent the transistor from reaching deep saturation. The Schottky gate input and internal circuitry resemble the standard TTL gate except the resistor values are about one-half the TTL value. The output section has a Darlington transistor pair for pull-up and an active pull-down squaring network. This family has power dissipation of 20 mW per gate and propagation delays three times as fast as TTL devices with the average time of 3 ns while driving 15 pF/280Ω load.

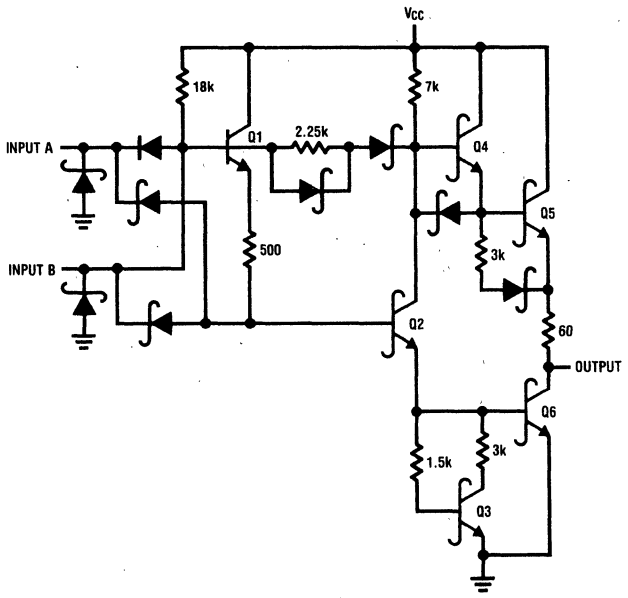


FIGURE 3. DM54LS00/DM74LS00

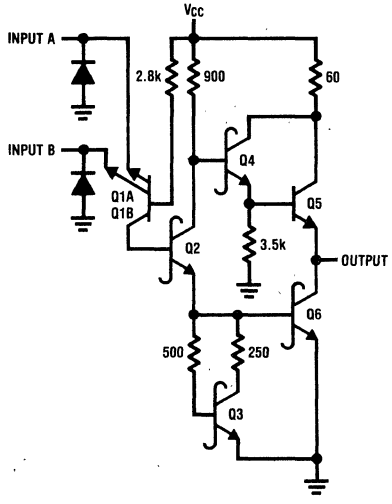


FIGURE 4. DM54S00/DM74S00

ADVANCED LOW POWER SCHOTTKY (DM54ALS/DM74ALS)

The advanced low power Schottky family is one of the most advanced TTL families. It delivers twice the data handling efficiency and still provides up to 50% reduction in power consumption compared to the LS family. This is possible because of a new fabrication process where components are isolated by a selectively grown thick-oxide rather than the P-N junction used in conventional processes. This refined process, coupled with improved circuit design techniques, yields smaller component geometries, shallower diffusions, and lower junction capacitances. This enables the devices to have increased f_T in excess of 5 GHz and improved switching speeds by a factor of two, while offering much lower operating currents.

In addition to the pin-to-pin compatibility of the ALS family, a large number of MSI and LSI functions are introduced in the high density 24-pin 300 mil DIP. These devices offer the designers greater cost effectiveness with the advantages of reduced component count, reduced circuit board real-estate, increased functional capabilities per device and improved speed-power performance.

The basic ALS gate schematic is quite similar to the LS gate. It consists of either the PNP transistor or the diode inputs, Darlington transistor pair pull-up and active pull-down (squaring network) at the output. Since the shallower diffusions and thinner oxides will cause ALS devices to be more susceptible to damage from electrostatic discharge, additional protection via a base-emitter shorted transistor is included at the input for rapid discharge of high voltage static electricity. Furthermore, the inputs and outputs are clamped by Schottky diodes to prevent them from swinging excessively below ground level. A buried N^+ guard ring around all input and output structures prevents crosstalk. The ALS family has a typical power dissipation of 1 mW per gate and typical propagation delay time of 4 ns into a 50 pF/2 kΩ load.

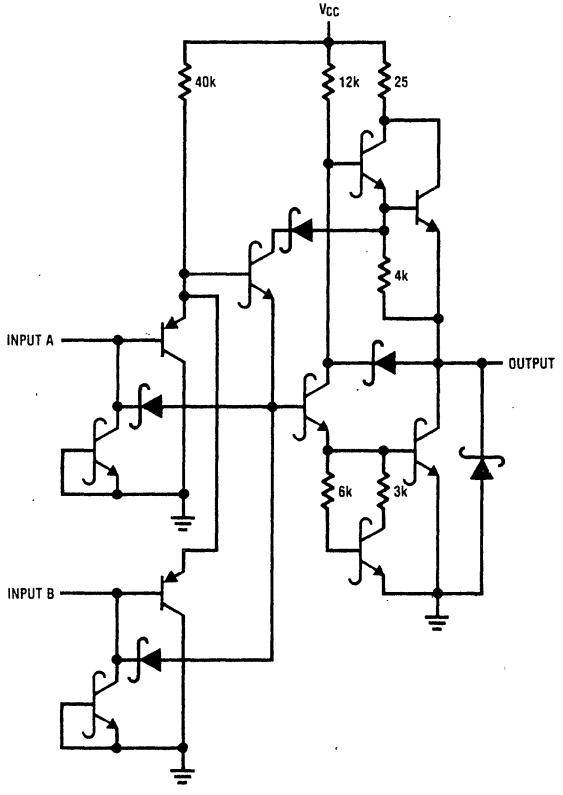


FIGURE 5. DM54ALS00/DM74ALS00

ADVANCED SCHOTTKY (DM54AS/DM74AS)

This family of devices is designed to meet the needs of the system designers who require the ultimate in speed. Utilizing Schottky barrier diode clamped transistors with shallower diffusions and advanced oxide-isolation fabrication techniques, the AS family achieves the fastest propagation delay that bipolar technology can offer. The AS family has virtually the same circuit configuration as the ALS family. It has PNP transistor or diode inputs with electrostatic protection base-emitter shorted transistors. The output totem-pole consists of a Darlington pair transistor pull-up and an active pull-down squaring network. The inputs and outputs are Schottky clamped to attenuate critical transmission line reflections. In addition, the circuit contains the "Miller Killer" network at the output section to improve output rise time and reduce power consumption during switching at high repetition rates. The AS family yields typical power dissipation of 7 mW per gate and propagation delay time of 1.5 ns when driving a 50 pF/2 kΩ load.

SELECTING A FAMILY

Two factors should be considered when choosing a logic family for application, speed and power consumption. New logic families were created to improve the speed or lower the power consumption of the previous families. The following tables rate each family.

Speed		Power Consumption	
Fastest	AS	Low	L
↓	S	↓	ALS
	ALS		LS
	LS		AS
	TTL		TTL
Slowest	L	High	S

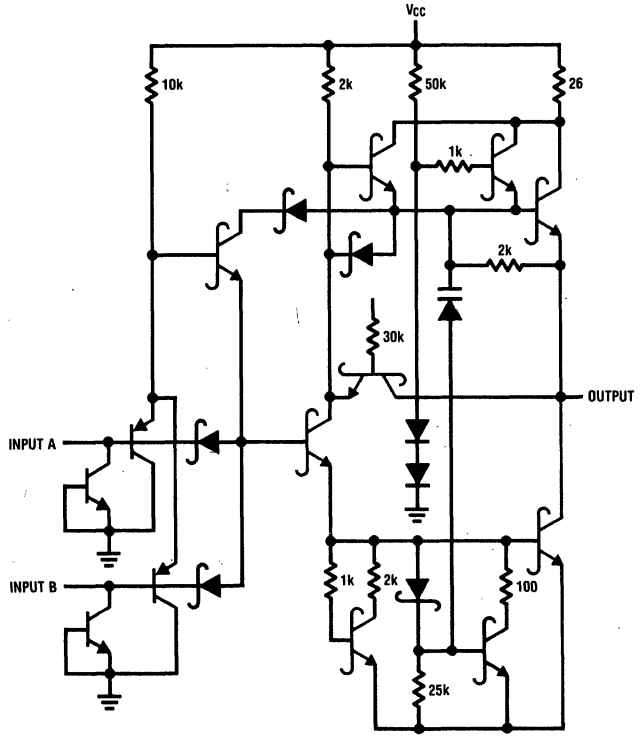


FIGURE 6. DM54AS00/DM74AS00

Bipolar Logic Family Electrical Characteristics Over Operating Temperatures

		TTL	L-TTL	LS	ALS	S	AS	Units
DM5400/DM7400								
2-Input NAND	t_{PLH}*	11	35	8	4	3	2.5	ns
	t_{PHL}*	7	31	8	4	3	1.5	ns
	t_r*	12	66	13	10	6	5	ns
	t_f*	5	30	3	6	3	3	ns
	I_{OH}	−400	−200	−400	−400	−1000	−2000	μA
Mil/Com	I_{OL}	16	2/3.6	4/8	4/8	20	20	mA
	I_{IH}	40	10	20	20	50	20	μA
	I_{IL}	−1.6	−0.18	−0.36	−0.20	−2	−0.50	mA
Min	I_{OS}	−20	−3	−20	−30	−40	−30	mA
Max	I_{OS}	−100	−15	−100	−112	−100	−112	mA
	I_{CCH}	8	0.8	1.6	0.85	16	3.2	mA
	I_{CCL}	22	2.04	4.4	3.0	36	16.1	mA
Mil	V_{OH}	2.4	2.4	2.5	$V_{CC}-2$	2.5	$V_{CC}-2$	V
Com	V_{OH}	2.4	2.4	2.7	$V_{CC}-2$	2.7	$V_{CC}-2$	V
Mil	V_{OL}	0.4	0.3	0.4	0.4	0.5	0.5	V
Com	V_{OL}	0.4	0.4	0.5	0.5	0.5	0.5	V
	V_{IH}	2	2	2	2	2	2	V
Mil	V_{IL}	0.8	0.7	0.7	0.8	0.8	0.8	V
Com	V_{IL}	0.8	0.7	0.8	0.8	0.8	0.8	V
	V_I	−1.5	N/A	−1.5	−1.5	−1.2	−1.2	V
Mil	NM-H	400	400	500	500	500	500	mV
Com	NM-H	400	400	700	700	700	700	mV
Mil	NM-L	400	400	300	400	400	300	mV
Com	NM-L	400	300	300	300	300	300	mV
Gate Power × Delay Product		100	20	20	4	60	30	pJ
DM5474/DM7474								
D Flip-Flop	t_{PLH}*	14	50	17	5	8	6	ns
(CLK to Q)	t_{PHL}*	20	60	22	8	9	6	ns
(PS or	t_{PLH}*	14	40	17	7	6	4.5	ns
CLR to Q)	t_{PHL}*	20	60	22	10	12	6	ns
(CLK HI)	t_W	30	75	25	12	8	4	ns
(PS or CLR LOW)	t_W	30	75	20	15	9	4	ns
	$t_{SET\text{-}UP}$	20	50	25	15	3	3/2	ns
	t_{HOLD}	5	15	0	0	2	2/1	ns
	t_r*	13	64	9	17	4	5	ns
	t_f*	6	19	6	9	3	3	ns
	f_{MAX}*	25	11	33	34	95	125	MHz
	I_{OH}	−400	−200	−400	−400	−1000	−2000	μA
Mil/Com	I_{OL}	16	2/3.6	4/8	4/8	20	20	mA
(CLK/D)	I_{IH}	80/40	20/10	20	20	100/50	20	μA
(PS/CLR)	I_{IH}	40/120	20/30	40	40	100/150	40	μA
(CLK/D)	I_{IL}	−3.2/−1.6	−0.36/−0.18	−0.4	−0.2	−4/−2	−0.5	mA
(PS/CLR)	I_{IL}	−1.6/−3.2	−0.18/−0.36	−0.8	−0.4	−4/−6	−1.0	mA
Min	I_{OS}	−20/−18	−3	−20	−30	−40	−30	mA
Max	I_{OS}	−55	−15	−100	−112	−100	−112	mA
	I_{CC}	15	3	8	4	50	16	mA
Mil	V_{OH}	2.4	2.4	2.5	$V_{CC}-2$	2.5	$V_{CC}-2$	V
Com	V_{OH}	2.4	2.4	2.7	$V_{CC}-2$	2.7	$V_{CC}-2$	V
Mil	V_{OL}	0.4	0.3	0.4	0.4	0.5	0.5	V
Com	V_{OL}	0.4	0.4	0.5	0.5	0.5	0.5	V
	V_{IH}	2	2	2	2	2	2	V
Mil/Com	V_{IL}	0.8	0.7	0.7/0.8	0.8	0.8	0.8	V
	V_I	−1.5	N/A	−1.5	−1.5	−1.2	−1.2	V
Mil	NM-H	400	400	500	500	500	500	mV
Com	NM-H	400	400	700	700	700	700	mV
Mil	NM-L	400	400	400	400	300	300	mV
Com	NM-L	400	300	300	300	300	300	mV

Note: See Test Waveforms in this section for loading conditions. t_r and t_f are measured from 10% to 90% of waveform.

Note: NM-H is noise margin high. NM-L is noise margin low.

*Typical values. Other values are limit values.

Bipolar Logic Family Output Source/Sink Capability: 54/74 Families

Output			TTL	L-TTL	LS	ALS	S	AS	Units
Standard	Mil	I_{OH}	−0.4	−0.2	−0.4	−0.4	−1	−2	mA
	Com		−0.4	−0.2	−0.4	−0.4	−1	−2	mA
	Mil	I_{OL}	16	2	4	4	20	20	mA
	Com		16	3.6	8	8	20	20	mA
Buffered	Mil	I_{OH}	−0.8	−0.2	−0.4	−1	−1	−12	mA
	Com		−0.8	−0.2	−0.4	−2.6	−1	−15	mA
	Mil	I_{OL}	16	2	4	12	20	32	mA
	Com		16	3.6	8	24	20	48	mA
Bus Driver	Mil	I_{OH}	−2	N/A	−1	−12	−2*	−48	mA
	Com		−5.2	N/A	−2.6	−15	−6.5	−48	mA
	Mil	I_{OL}	32	N/A	12	12	20	40	mA
	Com		32	N/A	24	24-48	20	48	mA

Fan-In and Fan-Out

	TTL	L-TTL	LS	ALS	S	AS	Units
Input Load: High	1	0.25	0.5	0.5	1.25	0.5	U. L.
Low	1	0.1125	0.225	0.125	1.25	0.3125	U. L.
Output Drive: High	10	2.25	5	5	12.5	12.5	U. L.
Low	10	5	10	10	25	50	U. L.

Note: UNIT LOAD (U. L.) Standard is referenced with respect to standard TTL device loading. It is defined as:
1 U. L. = 40 μA (HIGH STATE)
1 U. L. = 1.6 mA (LOW STATE)

IC Device Testing

Understanding the intent and practice of IC device testing is vital to insuring both the quality and proper usage of integrated circuits. All National Semiconductor data sheets list the AC and DC parameters with min and/or max limits, along with forcing functions. Understanding when a part fails the limit, and which forcing functions are really tighter, is critical when determining if an IC device is good or bad.

All of National's databook parameters are defined and guaranteed for "worst-case testing." Input loading currents (fan-in) are tested at the input and V_{CC} levels that most increase that loading, while the output drive capability (fan-out) is tested at the input and V_{CC} levels that most decrease that capability. I_{CC} is tested with the input conditions and V_{CC} level that yield the greatest I_{CC} value, and V_{CLAMP} is tested such that the negative voltage is maximized for the given clamp current. The fan-in and fan-out specs are contained in the I_{IH}, I_{OH} and I_{IL}, I_{OL} values. To guarantee these fan-in and fan-out limits at 10, the I_{OL} must be at least 10 times the I_{IL} and the I_{OH} must be at least 10 times the I_{IH}. Be aware that the fan-in and fan-out specifications are valid only within a given device family. The standard input loading and output drives are shown in Table I.

Notice that the I_{OL} is at least 10 times the I_{IL} and that the I_{OH} is greater than 10 times the I_{IH}. Also notice that these are "standard" drive and load currents for single sink outputs and inputs. Certain devices may have multiple load inputs where the input line goes to several input structures and has, say, 2 or 3 times the normal I_{IL} and I_{IH} loading. Certain other devices will have "triple sink" outputs that can drive 3 times the standard I_{OL} and I_{OH} currents. These devices are generally bus drivers, or drivers intended to drive highly capacitive loads. Finally, there are certain devices that have PNP inputs that reduce the I_{IL} loading to typically $-200\ \mu A$, thus allowing an increased DC fan-in of 20. One must therefore be careful when interfacing many different types of devices, even in the same family, and not simply go the "fan-out of 10" rule.

When dealing with any kind of device specification, it is important to note that there exists a *pair* of test conditions that define that test: the forcing function and the limit. Forcing functions appear under the column labeled "Conditions" and define the external operating constraints placed upon the device tested. The actual test limit de-fines how well the device responds to these constraints.For example, take the parameter $V_{OH(min)}$ for the DM74LS00. It is tested at $V_{CC(min)} = 4.75V$ commercial, using an $I_{OH} = -400\ \mu A$. If we required an $I_{OH} = -800\ \mu A$, this would be a "tighter" test, as the output voltage drops with increased I_{OH}. Hence, a device that would pass the $-800\ \mu A$ I_{OH} would also pass the $-400\ \mu A$ I_{OH}, but not necessarily the other way around. Furthermore, V_{OH} tracks with V_{CC}, which is why $V_{CC(min)}$ is the worst-case testing, and not $V_{CC(max)}$. Finally, forcing inputs to threshold represents the most difficult testing because this puts those inputs as close as possible to the actual switching point and guarantees that the device will meet the V_{IH}/V_{IL} spec.

TABLE I. Fan-In/Fan-Out

Device Family	Input Loading	Output Drive
TTL	$I_{IL} = -1.6$ mA $I_{IH} = 40\ \mu A$	$I_{OL} = 16$ mA $I_{OH} = -400\ \mu A$
Low Power Schottky	$I_{IL} = -400\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Advanced Low Power Schottky	$I_{IL} = -100\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Schottky	$I_{IL} = -2$ mA $I_{IH} = 50\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -1$ mA
Advanced Schottky	$I_{IL} = -500\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -2$ mA
Low Power	$I_{IL} = -180\ \mu A$ $I_{IH} = 10\ \mu A$	$I_{OL} = 2$ mA (Mil) $I_{OL} = 3.6$ mA (Com) $I_{OH} = -200\ \mu A$

Tables II and III show the "direction" of the looser/tighter testing for most common DC parameters. Notice that one can tighten either the forcing function or the limit, or both. Tightening either one is sufficient to insure a tighter test. Also notice the difference between max and min limits. For I_{OS} (double-ended limits), even though -20 mA is more positive than -100 mA, and is mathematically the max limit, the magnitude of the number is the determining factor when deciding which is the max limit. The negative sign simply implies the direction that the current is going, with a negative current leaving the device, and a positive current entering the device. Table II shows the direction of tighter forcing functions, while Table III shows the direction of tighter limits.

TABLE II. Looser/Tighter Forcing Functions Example: DM74LS00

Condition	Test	Looser	Nominal	Tighter	Units
I_{IK}	V_{IK}	−17	−18	−19	mA
I_{OH}	V_{OH}	−350	−400	−450	μA
I_{OL}	V_{OL}	3	4	5	mA
V_I	I_I	6.5	7	7.5	V
V_{IH}	I_{IH}	2.6	2.7	2.8	V
V_{IL}	I_{IL}	0.5	0.4	0.3	V
V_O	I_{OS}	0.1	0.0	−0.1	V
V_{CC}	I_{CC}	5.0	5.5	6.0	V

TABLE III. Looser/Tighter Test Limits Example: DM74LS00

Parameter	Looser	Nominal	Tighter	Units
$V_{IH(min)}$	2.1	2.0	1.9	V
$V_{IL(max)}$	0.7	0.8	0.9	V
$V_{IK(max)}$	−1.6	−1.5	−1.4	V
$V_{OH(min)}$	2.6	2.7	2.8	V
$V_{OL(max)}$	0.6	0.5	0.4	V
$I_{I(min)}$	6.5	7.0	7.5	V
$I_{IH(max)}$	50	40	30	μA
$I_{IL(max)}$	−450	−400	−390	μA
$I_{OS(max)}$	−110	−100	−90	mA
$I_{OS(min)}$	−10	−20	−30	mA
$I_{CCH(max)}$	1.7	1.6	1.5	mA
$I_{CCL(max)}$	4.5	4.4	4.3	mA

Following are the test set-ups that are used to test the DC parametrics. In each case, the gate connection, equivalent circuit schematic and resultant voltage/current plot are shown.

The indicated graphs are typical of LS products and are similar to other bipolar logic families. The schematics shown are for single inversion devices and represent generalized circuits.

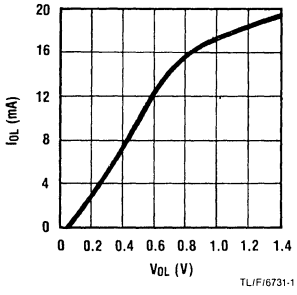
OUTPUT VOLTAGE LOW LEVEL (V_{OL})

Both inputs are connected to logic "1" values (assuming an inverting gate) and forced at the V_{IH} spec. V_{CC} minimum is used, and I_{OL} is forced on the output. The resulting V_{OL} is measured. For typical LS products, the military and commercial test points are indicated on the V_{OL} vs I_{OL} graph. In each case, the device must not exceed the V_{OL} spec when the I_{OL} current is being forced.

OUTPUT VOLTAGE HIGH LEVEL (V_{OH})

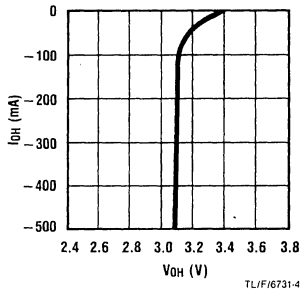
One input is tied high (any value above 2.0V) and the other input is forced at the V_{IL} threshold (assuming a single inversion gate). The minimum V_{CC} value is used. Each input is tested independently and the I_{OH} current is forced. The resulting V_{OH} is measured. The V_{OH} vs I_{OH} graph shows the military and commercial V_{OH}/I_{OH} test points for standard LS products.

V_{OL} vs I_{OL}
Typical LS Device Curve

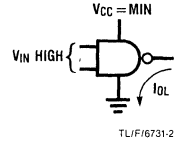


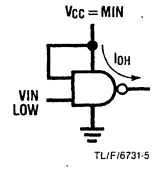
	I_{OL}	V_{OL}
Mil:	4.0 mA	0.40V
Com:	8.0 mA	0.50V

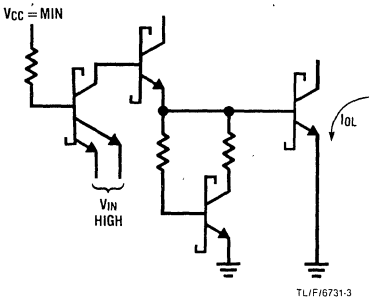
V_{OH} vs I_{OH}
Typical LS Device Curve

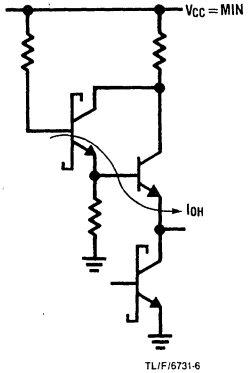


	I_{OH}	V_{OH}
Mil:	−400 μA	2.5V
Com:	−400 μA	2.7V









INPUT CURRENT HIGH LEVEL (I_{IH})

I_{IH} tests the input leakage in the high state. For MET, diode, and PNP inputs, the test set-up consists of all inputs except the one under test tied high (greater than V_{IH}). The remaining input has the V_{IH} value forced upon it, and the resultant I_{IH} is measured. This test checks for emitter-to-collector inverse transistor action for MET inputs, and reverse bias leakage for diode and PNP inputs.

For MET inputs, there is also an additional set-up for I_{IH} testing that checks for emitter-to-emitter transistor action. This is done with all the other inputs tied to ground.

MAXIMUM INPUT CURRENT (I_I)

I_I or BV_{IN} testing is the same as the emitter-to-collector leakage test (I_{IH}) and guarantees that the input will not pass more than the specified current at the stated specification (100 μA at 7V for LS).

INPUT CURRENT LOW LEVEL (I_{IL})

One input at a time is tested with the other inputs tied to a solid "1" value. V_{CC} is set to the maximum value and the V_{IL} value is forced. I_{IL} is then measured.

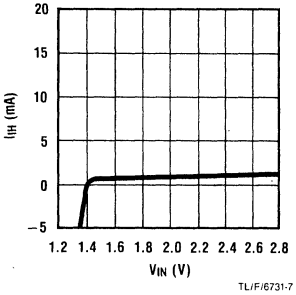
$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1} \quad \text{Standard Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{SH})]}{R1} \quad \text{Diode Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1 \times \beta} \quad \text{PNP Inputs}$$

I_{IL} is intended to measure the value of the base pull-up resistor on the input, and to guarantee the maximum input load an IC presents.

I_{IN} vs V_{IN} (High State)
Typical LS Device Curve



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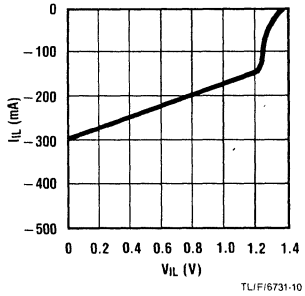
I_{IH}	V_{IH}
20 μA	2.7V

I_{IN} vs V_{IN} (Low State)
Typical LS Device Curve



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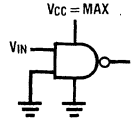
I_{IL}	V_{IL}
−400 μA	0.40V



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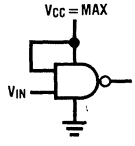

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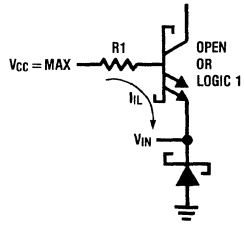

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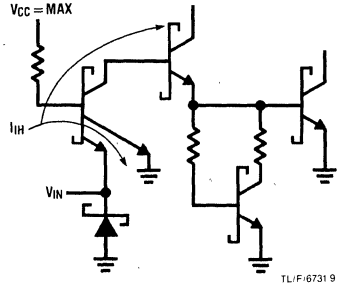

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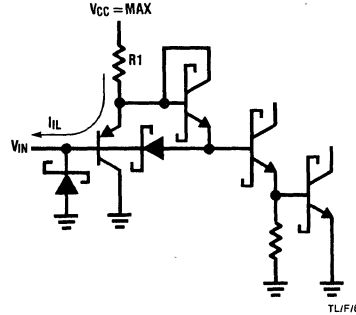

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OUTPUT SHORT CIRCUIT CURRENT (I_{OS})

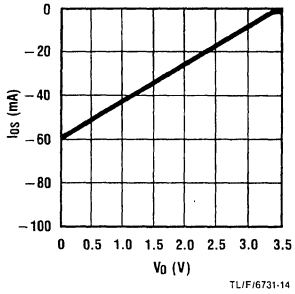
I_{OS} is measured with $V_{CC(max)}$ and the 0V forced on the output while it is in the high state. The resultant current is measured. The purpose of this test is to check the I_{OS} resistor that forms the Darlington's collector pull-up. This parameter is important as it reflects both the maximum current the device will draw and the maximum drive it will provide when it is switching from low to high.

Caution must be taken when measuring TTL, LS and S outputs as the power dissipated on the die will be substantial. I_{OS} shorts should not be maintained in excess of one second or damage to the device may result.

SUPPLY CURRENT HIGH LEVEL (I_{CCH}) AND SUPPLY CURRENT LOW LEVEL (I_{CCL})

Both I_{CCH} and I_{CCL} are tested using the V_{CC} maximum value. The inputs are set to the values necessary to achieve the output in the desired state. All outputs are left open, neither sourcing nor sinking current. The goal of this test is to guarantee the maximum quiescent operating power that the device will draw.

V_O vs I_{OS}
Typical LS Device Curve



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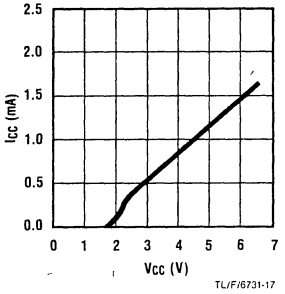
	Min	Max
I_{OS}	−20	−100

I_{CCL} vs V_{CC}
Typical LS Device Curve



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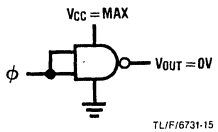
I_{CC}	Volts
1.6 mA	5.25V



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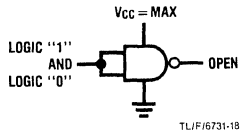

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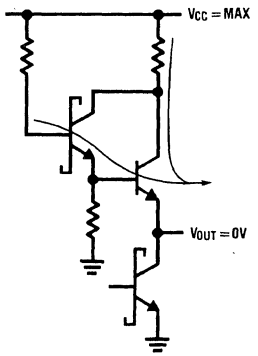

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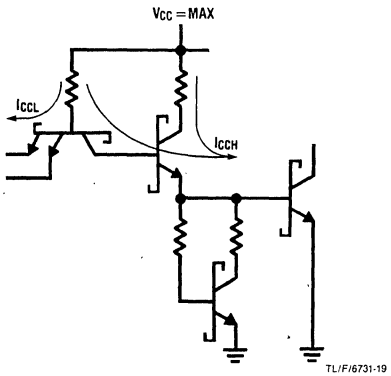


TL/F/6731-19

INPUT CLAMP VOLTAGE (V_{IC} OR V_{IK})

V_{CLAMP} (V_{IK}) is measured with all but one input tied high and the I_{IK} current forced on the remaining input. V_{CC} is set to the minimum and the V_{IK} voltage is measured.

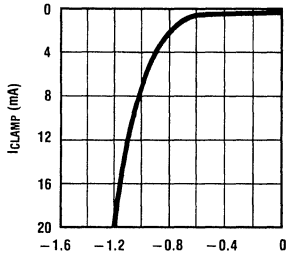
OUTPUT TRI-STATE CURRENT HIGH LEVEL (I_{OZH}) AND OUTPUT TRI-STATE CURRENT LOW LEVEL (I_{OZL})

TRI-STATE I_{SINK} and I_{SOURCE} are measured with the output control input tied to the appropriate threshold value (usually $V_{IL} = 0.8V$) and with $V_{CC(max)}$. This is to insure that the output will have the greatest drive capability and the TRI-STATE® control can effectively "turn off" the output under these conditions.

TRI-STATE I_{SINK}: Output is set in the high state and then TRI-STATE mode. $V_{OZL} = 0.4V$ is then applied. The current drawn out of the device is then measured.

TRI-STATE I_{SOURCE}: Output is set in the low state and then TRI-STATE mode. $V_{OZH} = 2.7V$ is then applied. The current drawn into the device is then measured.

V_{CLAMP} vs I_{CLAMP}
Typical LS Device Curve



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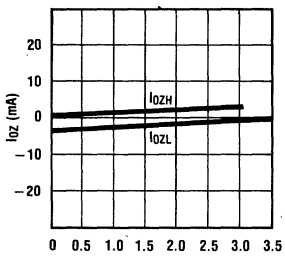
I_{CLAMP}	V_{CLAMP}
−18 mA	−1.5V

I_{OZH} vs V_{OZH}
(TRI-STATE I_{SOURCE}),
I_{OZL} vs V_{OZL}
(TRI-STATE I_{SINK})
Typical LS Device Curve



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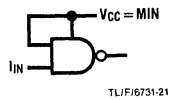
	I_{OZ}	V_{OZ}
I_{OZL}	−20 μA	0.4V
I_{OZH}	20 μA	2.7V



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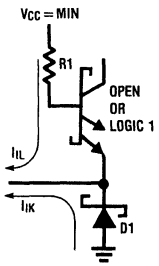

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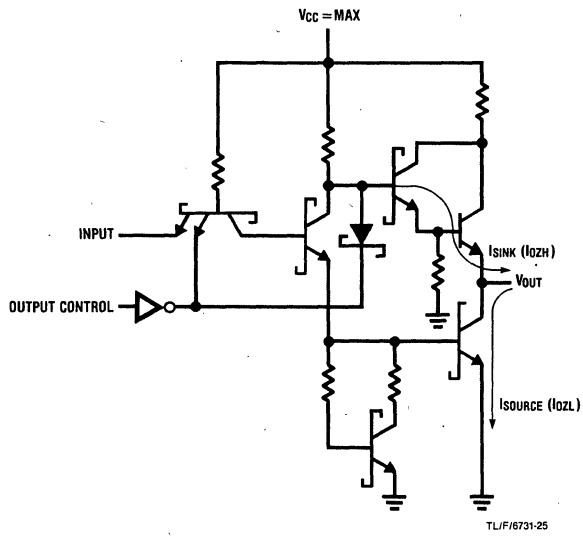

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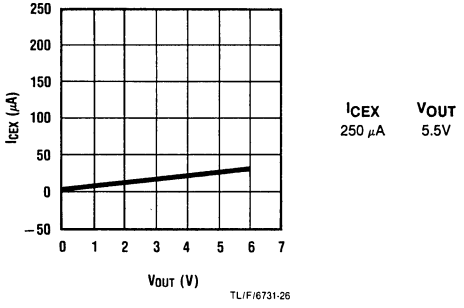
HIGH LEVEL OUTPUT CURRENT (OPEN-COLLECTOR DEVICES ONLY)

I_{CEX} is tested with the output in the high state. V_{CC} is set to 5.0V and the specified voltage (5.5V for LS) is applied to the output. The inputs are at the threshold values (0.8V and 2.0V, depending upon the logic to put output in the high state) and the resulting I_{CEX} leakage current is measured.

I_{CEX} vs V_{OUT}
(Open-Collector Device)
Typical LS Device Curve



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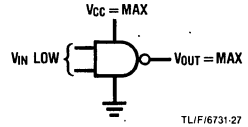

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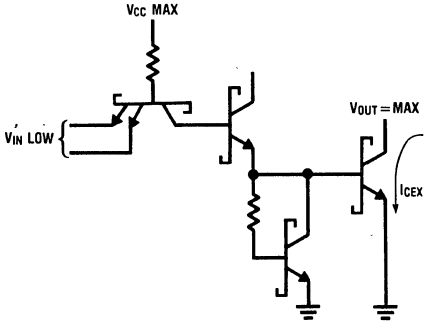

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AC SWITCHING CHARACTERISTICS

The AC switching characteristics are generally measured in units of time (commonly in nanoseconds), and define how long it takes for the signal to propagate from the input to the output. The definitions used in determining the pass/fail status of each limit are not the same for AC as they are for DC. The distinction lies in the fact that for DC operation there exists one characteristic V-I curve on which the device must operate. Devices are good if they operate on the correct side of the limit, and bad if they operate on the wrong side of the limit. When dealing with certain AC parameters (f_{MAX}, t_{SET-UP}, t_{HOLD}, $t_{RELEASE}$, t_{PW}), the device can, and usually does, operate on both sides of the databook limit. The limit really implies a boundary that all devices are guaranteed to exceed. Depending upon the parameter, the device will either operate at all values above and some below the limit, or it will operate at all values below and some above the limit. In each case, the device is only guaranteed to operate for all values on one side of the limit. Although the device will also operate beyond the limit, it is not guaranteed to. Furthermore, device operation beyond the limit is not considered a failure. For instance, take the f_{MAX} parameter with a min limit of 25 MHz. All devices are guaranteed to operate at all frequencies below 25 MHz and will operate in excess of 25 MHz, although this is not guaranteed. Now, take the example of t_{SET-UP} with a minimum limit of 25 ns. All of the devices are guaranteed to operate with a set-up time of 25 ns and longer, and will operate with set-up times below 25 ns, although this is not guaranteed either. Be aware that both of these specifications are listed in the minimum column in the databook, but the interpretation of what is failing differs significantly.

Propagation delays (called prop delays and denoted by the symbols t_{PHL} and t_{PLH}) are specified as maximum limits, and guarantee the maximum time one must wait to insure that the correct data has appeared at the device's output. Prop delay specifications often show "typical" limits. These "typical" limits are representative of the general distribution of a manufacturer and not of any one lot of product purchased. Each propagation delay is specified from one input to one output only.

Input set-up and hold times (including $t_{RELEASE}$) specify how long one input must be stable at a particular logic level prior to an action occurring at another input. For example, take the DM54/74LS74 positive-edge-triggered D flip-flop. The "set-up 1" specification defines how long a logic "1" must be present *and* stable at the DATA input prior to the positive edge of the CLOCK to insure that the device will recognize that data as a "1." There also exists a "hold 1" specification which specifies how long a logic "1" must be held after the active edge of CLOCK for the device to recognize that logic "1." Both the set-up and hold times must always be met or the device will not necessarily bring in the proper data. Set-up times are generally positive, while hold times may be either positive or negative, usually negative. The meaning of a negative hold time is that the data may be removed from the input prior to the active edge of CLOCK, and the CLOCK will still bring in the desired data. Set-up and hold times are specified as minimum values, since this defines the minimum time data must be stable prior to any change at the CLOCK input. Removing the data sooner than the minimum time may cause improper action on the part of the device.

$t_{RELEASE}$ is specified on devices where there is an input that must be set inactive prior to the active edge of CLOCK. Such inputs are usually overriding inputs like CLEAR and PRESET. With CLEAR active, it will prevent the device from switching on the CLOCK signal. $t_{RELEASE}$ is defined as the time it takes for the CLEAR input to "release" the device for clocking action, and is specified as a minimim. This represents the maximum delay required between CLEAR going inactive and the active edge of CLOCK to insure proper device operation.

All devices that have a CLOCK input also have a specification that defines the maximum speed that the CLOCK can be driven, called f_{MAX}. This specification is defined as a minimum specification and states that all of the devices will be able to operate at frequencies up to 25 MHz. For the DM54/74LS74 with an f_{MAX} of 25 MHz, all of the devices are guaranteed to operate at all clock frequencies, up to and including 25 MHz. Although no devices are guaranteed to operate above f_{MAX} (only below it), most devices will operate beyond the maximum specification. The minimum limit does *not* state that the device will not operate below f_{MAX} or that any devices that do are bad, but rather that all the devices will operate up to the limit.

Table IV shows the direction of the tighter testing for the more common AC parameters. All prop delays (those AC parameters that have the symbols t_{PLH} or t_{PHL}) have simple min/max limits. The device is guaranteed to operate within the bounds of the min/max limits, and any operation outside these limits denotes a device failure. $t_{SET\text{-}UP}$, t_{HOLD}, f_{MAX}, and $t_{RELEASE}$ parameters have limits that denote guaranteed operation boundaries (i.e., the device is guaranteed to operate up to the boundary) but no guarantee is made concerning the device operation (or lack of it) beyond the boundary.

For detailed information on the AC waveforms, please see the test waveforms in this section.

TABLE IV. Looser/Tighter AC Test Limits Example: DM74LS74

Test	From	Looser	Nominal	Tighter	Units
$f_{max(min)}$		24	25	26	MHz
$t_{PLH(max)}$	CLR, PRE, CLK	26	25	24	ns
$t_{PHL(max)}$	CLR, PRE, CLK	31	30	29	ns
$t_{W(min)}$	CLOCK HIGH	21	20	19	ns
$t_{W(min)}$	PRE, CLR LOW	26	25	24	ns
$t_{SET\text{-}UP(min)}$	DATA HIGH	21	20	19	ns
$t_{SET\text{-}UP(min)}$	DATA LOW	21	20	19	ns
$t_{HOLD(min)}$	All DATA	1	0	−1	ns

Glossary of Terms

DC Operating Conditions and Characteristics

GENERAL DEFINITIONS

I: Current is the flow of electric charge from one potential to another through a conductor. The unit of measure is the Ampere, or Amp, abbreviated A. One Amp is equal to the current flowing through one ohm of resistance when one volt is applied across that resistance. Common units found in the semiconductor industry are the milliampere, abbreviated mA, equal to 0.001 A and the microampere, abbreviated μA, equal to 0.000001A. Negative current is defined as current flowing out of a device terminal and positive current is defined as current flowing into a device terminal.

V: Voltage, or the electromotive force which causes current to flow through a conductor. One Ampere of current flowing through one ohm of resistance develops a potential difference of one volt across that resistance. The unit of measure is the Volt, abbreviated V, and a common unit is the millivolt, abbreviated mV, equal to 0.001V.

INPUT CURRENT PARAMETERS

I_I Maximum High Level Input Current: Current flowing into an input when that input has the maximum voltage specified for the family applied to it. This test is used to guarantee the minimum reverse breakdown voltage of the input structure.

I_{IH} High Level Input Current: The current flowing into an input when that input has a high level voltage equal to the minimum high level output voltage specified for the family. This test is used to check the emitter-to-emitter leakage and the inverse transistor action of a multi-emitter transistor input, the input leakage of a diode, PNP transistor, or C-B short type of input, and to guarantee the fan-in specified for the family.

I_{IK} Input Clamp Current: The current flowing out of an input when that input is pulled below ground. This test is used to guarantee the integrity of the input clamp diode. The input clamp diode is used to limit the voltage swings on the input by clamping the negative excursions to a level equal to one diode drop below ground. This serves to reduce ringing on an incoming signal. Pulling the input below ground for an extended length of time can cause parasitic transistor action to occur between adjacent tanks on the die which can cause erroneous data to occur on the outputs of the device. To prevent this, voltages on the inputs during operation (other than high speed ringing) should be limited to no more than 0.5V below ground at all times.

I_{IL} Low Level Input Current: The current flowing out of an input when a low level voltage equal to the maximum low level output voltage specified for the family is applied to the input. This test is used to check the input pullup resistor on an MET or a diode input and to guarantee the specified fan-in of the family.

I_T+ Current at Positive-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the positive going threshold voltage is applied to the input.

I_T- Current at Negative-going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the negative going threshold voltage is applied to the input.

OUTPUT CURRENT PARAMETERS

I_{CEX} Output Leakage Current: The current flowing into an open collector output when input conditions have been applied that, according to the product specification, will cause the output to be in the logic high state. This test checks the reverse breakdown of the output transistor.

I_O(off) Off-State Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This parameter is usually specified for open collector outputs intended to drive devices other than logic circuits, such as displays. Any leakage current applied to a display may cause the display to be activated.

I_{OH} High Level Output Current: The current flowing out of an output with input conditions applied that, according to the product specification, will establish a logic high level at the output. This test guarantees the current sourcing (drive) capability of the output and the fan-out specified for the family.

I_{OL} Low Level Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will establish a logic low level at the output. This test guarantees the current sinking capability of the output and the fan-out specified for the family.

I_{OS} Output Short-Circuit Current: The current out of an output when that output is shorted to ground, or another specified potential, with input conditions applied that, according to the product specification, will establish a logic high level at the output.

I_{OZ} High-Impedance State Output Current: These tests guarantee that the device will not excessively load a bus line when the device output is put into the TRI-STATE® mode.

I_{OZH} (or I_{SINK}): The current flowing into an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic low level at the output.

I_{OZL} (or I_{SOURCE}): The current flowing out of an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic high level at the output.

DC Operating Conditions and Characteristics (Continued)

SUPPLY CURRENT PARAMETERS

I_{CCH} Supply Current (outputs in the high state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic high level at the output(s).

I_{CCL} Supply Current (outputs in the low state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic low level at the output(s).

I_{CCZ} Supply Current (outputs in the high-impedance state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a high impedance state at the output.

INPUT VOLTAGE PARAMETERS

BV_{IN} Input Breakdown Voltage: The maximum voltage that the device is guaranteed to be able to withstand without exceeding the maximum input current specification.

V_F Input Forward Voltage: The voltage applied to the input of a device that causes the input structure to become forward biased; usually equal to the maximum output low voltage specified for the family.

V_{IH} High Level Input Voltage: The minimum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic high level.

V_{IK} Input Clamp Voltage: The input clamp voltage specification checks the quality of the input diode whose purpose is to damp out ringing. This is not intended to be an operating condition and if this voltage is allowed to persist for any length of time, parasitic transistor action will occur between adjacent geometry tanks and circuit performance will be degraded, in some cases to the point of failure.

V_{IL} Low Level Input Voltage: The maximum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic low level.

V_R Input Reverse Voltage: The voltage applied to an input of a device that causes the input structure to become reverse biased; usually equal to the minimum high level output voltage specified for the family.

V_T+ Positive-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_T-.

V_T- Negative-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_T+.

OUTPUT VOLTAGE PARAMETERS

V_{OH} High Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} Low Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

V_O(off) Off State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

V_O(on) On State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

AC Operating Conditions and Characteristics

INPUT PARAMETERS

f_{MAX} Maximum Clock Frequency: The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic levels at the output with input conditions established that should cause changes of output logic level in accordance with the specification. Unless otherwise specified, this test is performed with no restrictions on input rise and fall times or duty cycle.

NOTE: A minimum value is specified that is the highest frequency at which all devices are guaranteed to function correctly.

t_H Hold Time: The interval during which a signal must be maintained at a given data input after an active transition at another given input.

NOTE: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.

t_W Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of a pulse waveform.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_{REC} Recovery Time: The time interval needed to switch a memory-type device from a write mode to a read mode and to obtain valid data signals at the output.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the device is guaranteed.

t_{REL} Release Time: The time interval between one control input going inactive and another input going active after which the inactive input no longer has any influence on the device operation.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_S Set-Up Time: The time interval during which a stable signal must be maintained at a specified input terminal before an active transition at another specified input terminal.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_R Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude.

t_F Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude.

OUTPUT PARAMETERS

t_{PZH} Output Enable Time to a High Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined high state.

t_{PZL} Output Enable Time to a Low Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined low state.

t_{PHZ} Output Disable Time from a High State: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined high state to the high impedance (off) state.

t_{PLZ} Output Disable Time from a Low Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined low state to the high impedance (off) state.

t_{WOUT} Output Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of an output waveform.

NOTE: This is usually only specified for monostable elements.

t_{PLH} Propagation Time, Low to High: The time between the specified voltage reference points on the input and output waveforms with the output changing from a low logic level to a high logic level.

t_{PHL} Propagation Delay, High to Low: The time between the specified voltage reference points on the input and output waveforms with the output changing from a high logic level to a low logic level.

t_{TLH}, t_r Transition Time, or Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude, or from 0.6V to 2.6V.

t_{THL}, t_f Transition Time, or Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude, or from 2.6V to 0.6V.

EXPLANATION OF DEVICE FUNCTIONS

Circuit Complexity

SSI: Small Scale Integration; the lowest level of complexity in integrated circuits.

MSI: Medium Scale Integration; small subsystems integrated into a single microcircuit.

LSI: Large Scale Integration; large subsystems or small systems integrated into a single microcircuit.

AC Operating Conditions and Characteristics (Continued)

Functional Descriptions

Buffer: A logic gate with high output drive capability, or fan-out. Buffers are used where a single circuit must drive a large number of loads.

Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exclusive-NOR gate, which produces a high level output only when its two inputs are identical.

Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9.

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.

Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.

Driver: Same as Buffer, above.

Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.

Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, and Exclusive-OR and Exclusive-NOR gates are built.

Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data, present at the input, is passed directly to the output, similar to the operation of a gate.

One-Shot: Monostable multivibrator; a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.

Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.

Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

Other Terms

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.

Open Collector: Output configuration that has no internal pullup. This configuration enables outputs that are connected together (wired-OR) to assume opposite states without incurring damage.

Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.

Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.

Totem Pole: An output configuration that contains an internal pullup structure, usually a transistor pullup allowing higher output drive capability than is available with open collector outputs.

TRI-STATE: A registered trademark for a circuit configuration in which the device output can be switched 'off' during which time the output presents a very high impedance to the bus it is connected to. This allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in the function tables found in NSC data sheets:

H	=	high logic level (steady state)
L	=	low logic level (steady state)
↑	=	transition from low to high logic level
↓	=	transition from high to low logic level
X	=	irrelevant (any level, including transitions)
Z	=	off (high impedance) state of a TRI-STATE output
a...h	=	the level of steady state inputs at inputs A through H respectively
Q_0	=	the level of Q before the indicated steady state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of Q before the indicated steady state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↑ or ↓
⎍	=	one high level pulse
⎎	=	one low level pulse
toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

AC Operating Conditions and Characteristics (Continued)

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect on the output. If the output is shown as a pulse, ⎍ or ⎍, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. As an example, below is the function table for a 4-bit bidirectional universal shift register, similar to the DM54LS194.

The first line of the table represents "asynchronous" clearing of the register and indicates that if CLEAR is low, all four outputs will be reset low regardless of the states of the other inputs. In the succeeding lines, CLEAR is inactive (high) and consequently has no effect.

The second line indicates that so long as the CLOCK input remains low (while CLEAR is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of CLEAR high and CLOCK low was established. Since on all the other lines of the table only the rising edge of the CLOCK is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the CLOCK remains high or on the high-to-low transition of the CLOCK.

The third line of the table represents "synchronous" parallel loading of the register and indicates that if S1 and S0 are both high, then regardless of the levels at the SERIAL inputs, the data present at A will transfer to QA, the data present at B will transfer to QB, and so forth, following a low-to-high transition on CLOCK.

The fourth and fifth lines represent the "synchronous" loading of high and low level data, respectively, from the SHIFT RIGHT SERIAL input and the shifting one bit to the right of previously entered data; data previously at QA is now at QB, data previously at QB and QC is now at QC and QD respectively, and the data previously at QD has been shifted out of the register. This entry of data and shifting takes place on the low-to-high level transition of CLOCK when S1 is low and S0 is high and as shown, the levels at the PARALLEL inputs, A through D, have no effect.

The sixth and seventh lines represent the "synchronous" loading of high and low level data respectively, from the SHIFT LEFT SERIAL input and the shifting one bit to the left of previously entered data; data previously at QD is now at QC, data previously at QC and QB is now at QB and QA respectively, and the data previously at QA has been shifted out of the register. This entry of serial data and shifting to the left takes place on the low-to-high level transition of CLOCK when S1 is high and S0 is low and as seen, the levels at the PARALLEL inputs, A through D, have no effect.

The last line indicates that so long as both MODE inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady state combination of CLEAR high and both MODE inputs low was established.

Function Table

Clear	Mode		Inputs							Outputs			
			Clock	Serial		Parallel							
	S1	S0		Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Designing with TTL

National Semiconductor
Application Note 363
Walt Sirovy
June 1984

54/74 series TTL has been used for more than a decade with excellent results, and continues to be a standard choice for design engineers because of the wide performance range and system optimization possible from the different families available. 54/74 logic comes in 7 different speed/power families (standard TTL, LS, S, ALS, AS, and L) that allow a design engineer to select device performance to suit his needs. Understanding the differences and the general limitations of all these families will go a long way toward insuring that a system will operate as intended with the minimum of corrections and redesigning.

FAMILY COMPATIBILITY: Intermixing Logic Types in One Design

Family interchangeability is a beneficial characteristic of the different TTL families and provides the designer with the ability to customize specific areas of his design in order to accomplish the task of achieving both high performance and the lowest power consumption possible. However, interchangeability is not simply a matter of replacing, say, an S00 for an LS00 to improve the speed and replacing an LS00 for an S00 for power savings. One must also look at the DC and AC characteristics to insure that the replacement device will be compatible with the existing circuit. The DC problems include input loading and compatible output drive capabilities. The AC problems include insuring that the new device speeds will be acceptable to the rest of the system. The different logic families also generate different amounts of noise and have different noise immunity. Finally, measure points for the AC parameters of the different families, although very similar, do vary some, and this will require attention.

SUPPLY RAILS: Why Not to Exceed the Specs

All bipolar logic (both junction and oxide isolated) is made up of selectively located regions of differently doped materials that form transistors, resistors, and diodes. Because of this, certain overall requirements are necessary to insure that the IC will be able to perform its task without interference from its environment. The first characteristic of bipolar devices is that the two power rails (V_{CC} and ground) represent the two voltage extremes that should be used in any system. Certain exceptions exist, primarily inputs and open-collector outputs that are pulled up to higher voltages than V_{CC}. However, while it is occasionally permissible to exceed the V_{CC} specification, it is never permissible to drive any input or output more than 0.5V below the ground reference. This limitation is due to the method used to electrically isolate the many circuit elements that are present on a bipolar IC. Oxide isolated devices use an oxide layer surrounding the various transistor and resistor tanks to provide an insulating barrier, while the original junction isolated devices use reverse biased PN junctions to provide that barrier. In both cases, the circuit is built on a P-type substrate that uses reverse biased PN junctions to separate the different circuit elements. The ground pin is electrically connected to the substrate and must be the most negative voltage on the device. When an input or output pin is taken below ground, the normally reverse biased isolation regions between the elements become forward biased and electrically connect these elements together, thus eliminating the integrity of the circuit. This may or may not result in actual damage to the device depending upon the magnitude of the violating signal and the specifics of the device being violated. This holds true for both junction and oxide isolated logic. Oxide isolated logic may provide more margin before failing (thereby "working" in some marginal designs), but it is nevertheless subject to the same kind of limitations as junction isolated logic.

IMPROPER GROUNDING: Noise Immunity, Floating Grounds

Bipolar logic uses the ground rail as the signal reference. Consequently, any modulation on the ground line will be directly added to the signal voltage. The logic "0" input noise margin is guaranteed as the difference between the V_{OL} and V_{IL} specification, and the logical "1" input noise margin is guaranteed as the difference between the V_{OH} and V_{IH} specification. This noise margin is intended to be protection against a reasonable amount of noise present. Insufficient grounding techniques can cause significant I_R and I_L drops on the ground line between two ICs and result in a "floating" ground line. This is due to the large currents that are present on ground and V_{CC} during high speed switching and means that the two devices are not using the same reference point. Any voltage drop in the ground line is added to the signal and ends up consuming some of the noise margin. Eventually, the mismatch caused by the floating ground will exceed the total noise margin and cause erroneous data to propagate through the system. The solutions to this problem are many and varied, but all of them revolve around improving the system grounding and include such ideas as providing separate signal and power grounds.

V_{CC} NOISE AND DECOUPLING: Providing Clean Power

The V_{CC} power rail is also susceptible to both I_R and I_L voltage drops. The problems that arise from the V_{CC} line are not the same as the problems that arise from the ground line. Since the V_{OH} level tracks the V_{CC} almost exactly, any voltage loss on the V_{CC} line is directly transferred to the V_{OH} level. However, the noise margin for the logic high state is typically 700 mV for commercial and 500 mV for military product, versus 400 mV and 300 mV for commercial and military product, respectively, for the logic low level. The main consequences of a drooping V_{CC} line now become I_{OL}/I_{OH} drive capability, and the AC performance in critical applications. Although bipolar devices are only guaranteed to operate over a given V_{CC} range (5V ± 10%), these devices typically function to V_{CC} values as low as 4V. Be aware that if the device does indeed function down to 4V, the AC and DC characteristics will be compromised, some quite severely.

Designing in a good power distribution system will insure that all the devices in the circuit will perform the same, regardless of their physical location. Properly decoupling the V_{CC} against both high and low frequency noise will

help eliminate any problems with individual device operation. High frequency noise (100 MHz and above) comes primarily from two sources, while low frequency noise (less than 25 MHz) results from primarily one source.

Sources of High Frequency Noise on the V_{CC} Line

1) High frequency noise results from the device rapidly switching logic levels. The bulk of the switching current from a low to high transition shows up in I_{CC} current surges, while the bulk of the switching current from a high to low transition shows up in ground current surges.

2) Noise is transmitted through the changing magnetic fields that result from the changing electric fields in a switching line and are picked up on adjacent signal paths.

Note that the frequency causing the noise is not the signal's frequency, but the frequency of the signal's slew rate. For instance, in an S00 that is switching 0V to 3V at 1 MHz, the slew rate of the output is typically about 1 ns/V, which is a frequency of around 160 MHz. The faster the slew rate, the higher the frequency, until one has an ideal square wave with infinite frequency. It is this frequency component that gives rise to the strong magnetic fields associated with switching bipolar devices.

Sources of Low Frequency Noise on the V_{CC} Line

1) Low frequency noise results from the change in the I_{CC} current demand as devices change state. For instance, gates, flip-flops, and registers will draw different I_{CC} currents, depending upon the state of the outputs.

The most commonly used method for countering these noise problems is to decouple the V_{CC} line. With this approach, capacitors are used to stabilize the V_{CC} line and filter out the unwanted frequency components. A small value capacitor (i.e., 0.1 μF) is used near the device to insure that the transient currents arising from device switching and magnetic coupling are minimized. A large value capacitor (i.e., 50 μF to 100 μF) is used on the board in general to accommodate the continually changing I_{CC} requirements of the total V_{CC} bus line. The following table shows a rough "rule of thumb" approach to determining how many capacitors to use for a given number of ICs. Be aware that the table is not a hard and fast rule, and that you must always evaluate your particular application to insure that there is sufficient V_{CC} decoupling. When using these guidelines, be sure that the devices are located near each other and near the capacitor. If the capacitor is too far away, I_R and I_L drops will diminish the capacitor's effect. All capacitors (especially the 0.01 μFs) must be high frequency RF capacitors. Disk ceramics are acceptable for this application. Keep in mind that, in synchronous systems, since a majority of the devices will be switching at once, alter your power distribution system accordingly.

Device Family	Number of Capacitors
AS, S, ALS, LS, H	1 Cap per 1 device
TTL, L	1 Cap per 2 devices

TYING ALL UNUSED INPUTS TO A SOLID LOGIC LEVEL

Unused inputs on TTL devices float at threshold, anywhere from 1.1V to 1.5V, depending upon the device and its family. While this usually simulates a "high", many application problems can be traced to open inputs. Inputs floating at threshold are very susceptible to induced noise (transmitted from other lines) and can easily switch the state of the device. A good design rule is to tie unused inputs to a solid logic level. Inputs are usually tied to V_{CC} through a 1 kΩ to 5 kΩ resistor, since tying them to ground means supplying the I_{IL} current instead of the I_{IH} current. I_{IL} is several orders of magnitude greater than I_{IH}. The resistor is recommended to protect the input against V_{CC} voltage surges and to protect the system against the possibility of the input shorting directly to ground. A single 1k resistor can handle up to 10 inputs.

TERMINATIONS: Why Terminate a Transmission Line?

Whenever signals change voltage levels, a wavefront is created that propagates according to the characteristics of the transmission line being used. If the overall length of the signal path is short compared with the signal's wavelength (1/frequency), then none of the complications of transmission lines are present. However, if the length of the signal path is long in comparison, then the wavefront will be significantly affected by the geometry and composition of that transmission line.

Fortunately, when dealing with a single board layout, the distances are usually short enough that one need not worry about the difficulties of terminating or impedance matching the line. However, if one is driving between boards or over long distances, he must be aware of the characteristics involved. When dealing with transmission lines it is necessary to know the impedance of the line. Every time the signal wavefront encounters a discontinuity (a point where the impedance changes, whether from a branch, junction or because of a change of environment), the opportunity for reflections and standing waves is present. These waves can easily cause the loss of the signal's integrity, having the ability to build voltages that are large enough to destroy an IC. Proper line termination will insure that the signal propagates down the line and is totally absorbed at the receiving end, thus preventing these waves from occurring.

Listed below is a guideline to the types of transmission lines to use when sending signals over various distances.

- 0" to 12" — Single wire conductor OK. Use point-to-point routing and avoid parallel routing if possible. Ground plane recommended, but not mandatory. Space conductors as far apart as possible to reduce line to line capacitance.
- 12" to 6' — Dense ground plane required with wire routed as closely as possible. Twisted-pair lines or coaxial cable mandatory for clock lines and recommended for all sensitive control lines.
- Over 6' — Use fully terminated transmission lines. Avoid the use of radially distributed lines and avoid sharp bends in the line. Be aware that transmission lines have complex impedances and are not simply resistive in nature.

BUS DRIVERS: On Board vs Off Board

Many of the TRI-STATE® buffers and flip-flops are intended to connect directly to the system bus and must be able to drive heavily capacitive loads. Keeping this in mind, all of National's LS TRI-STATE devices have "triple-sink" capability; that is, the I_{OL} and I_{OH} drive currents have been tripled. However, these devices are intended to drive single board buses. Driving off the board with these devices can easily lead to serious problems.

When using standard logic bus drivers on a single board, be aware that many of the octal and bus oriented devices have PNP inputs to reduce DC loading. PNP inputs on 54S/74S devices tend to be more capacitive than the corresponding diode or emitter inputs, and as such, compromise the AC loading of the bus. Careful attention must be given to both DC and AC loading when driving heavily loaded buses. PNP inputs on LS/AS/ALS operate at significantly lower currents and do not significantly increase capacitive load.

It is strongly recommended that any time a bus line leaves a board, interface bus drivers be used. These devices (see National's 1983 Interface/Bipolar LSI/Bipolar Memory/Programmable Logic Databook) are specifically designed to impedance match different kinds of transmission lines and have the necessary current drive to handle the job. Using an ordinary logic device will usually yield poor results. If one must drive a transmission line with a logic device, there are some guidelines that should be followed to minimize the problems that can result.

1) Take care to properly terminate the bus. Be aware that every time a signal passes through a different impedance, an interface is created and that any impedance mismatch will result in reflections.

2) Never drive off the board with a bistable element like a flip-flop or a latch. This is because those devices are very susceptible to reflected waves changing their state. By buffering the output of the latch with another device, the reflected wave can affect the output of the buffer, but not the latch. This means that when the wave finally dies out, the latch will still have the proper data and the buffer will "snap back" to the proper output.

3) Be sure to carry an adequate ground plan with the signals and to shield the bus. Carrying a good ground plan (use multiple ground lines spaced around the connector if possible) will reduce the problem of floating ground, and the shielding will help protect the signal lines for induced noise. Using twisted-pair transmission lines for critical signals helps to eliminate the capacitive coupling that can degrade signals, or even cause false signals.

4) It is best to buffer any clock or control lines that depend upon fast, clean switching. Buffering at both the sending and receiving end will go a long way toward insuring that the clock can accomplish its goals.

5) Use devices with Schmitt inputs to add to the noise margin of the receiving device. This will help increase the noise rejection of the system. Decouple each receiver separately, connecting the capacitor directly between ground and V_{CC}. Make sure that the device ground is tied directly to the bus ground.

6) If using open-collector devices to drive the bus, add a pull-up resistor on the input to the receiving device if the I_{OL} current of the driving device can handle it. A resistance in the 300Ω range will significantly improve the signal's rise time.

AC LOADING: What Do AC Loads Look Like, and Why?

The standard AC load for all of the logic families, except ALS and AS, is built around a diode chain to ground and a pull-up resistor to V_{CC} with added capacitance. This load is designed to look like the standard logic circuit input structure, and to simulate the appearance of switching in an actual application. For ALS and AS, the load is built around a resistor to ground and added capacitance. This is primarily for the requirements of high speed device testing. There also exists a set of standardized military AC loads that were designed to approximate the input structure, while using no switches for the TRI-STATE parameters. Please see waveforms in this section. In the final analysis of these loads, it must be kept in mind that they represent a standard that can be used to determine the quality of an IC. No load will be able to predict exactly how a device will perform in a circuit or the speeds that a device can achieve in a good test jig with the spec load, as compared to the speeds that a device will produce in an application.

OPEN-COLLECTOR DEVICES: What They Are, How to Use Them

Open-collector devices are totem pole outputs where the upper output (usually a Darlington transistor) is left out of the circuit. As such, these devices have no active logic high drive and cannot be used to drive a line high. The advantage to open-collector devices is that a number of outputs can be directly tied together. If one were to tie two complete totem pole outputs together, then at some time one output would be driving high while the other output was driving low. The result is that one device will be dumping excessive current directly into the other device. The resulting power dissipation in both devices can easily degrade the lifetime of the device. Since open-collector devices only have active drive in one state, if two connected devices drive to opposite states, the low state will always predominate and there will be no degradation to either device. Open-collector specifications are obvious by the lack of a V_{OH} specification. The only V_{OH}/I_{OH} specification is the leakage limits, and these are specified at $V_{OH} = 5.5V$.

When dealing with open-collector devices, it must be noted that each output requires a resistive pull-up, usually tied to V_{CC}. (By using high voltage outputs, one can tie the resistor pull-up to a voltage higher than V_{CC}.) Designers often try to get away with tying the output to an input and relying on the I_{IL} current to pull up the output. This is unwise, as it is just like leaving inputs floating: the input is very susceptible to noise and can easily give false signals. Shown below are two equations that can be used to determine the min/max range of the pull-up resistor.

$$R_{MAX} = \frac{(V_{CC(MIN)} - V_{OH})}{(N1 \bullet I_{OH} + N2 \bullet I_{IH})}$$

$$R_{MIN} = \frac{(V_{CC(MIN)} - V_{OL})}{(I_{OL} - N2 \bullet I_{IL})}$$

where: N1 = the number of open-collector devices tied together,
N2 = the number of inputs being driven on the line.

If the maximum resistance is exceeded, then it is possible for the total leakage currents from all of the inputs and outputs to pull the V_{OH} level below the spec value. Likewise, if the R_{MIN} value is exceeded, then the driving device may not be able to pull down the signal line to a solid V_{OL}. Either of these two cases can easily result in false logic levels being propagated through the system.

Designer's Encyclopedia of Bipolar One-Shots

National Semiconductor
Application Note 372
Kern Wong
May 1984

INTRODUCTION

National Semiconductor manufacturers a broad variety of industrial bipolar monostable multivibrators (one-shots) in TTL and LS-TTL technologies to meet the stringent needs of systems designers for applications in the areas of pulse generation, pulse shaping, time delay, demodulation, and edge detection of waveforms. Features of the various device types include single and dual monostable parts, retriggerable and non-retriggerable devices, direct clearing input, and DC or pulse-triggered inputs. Furthermore, to provide the designer with complete flexibility in controlling the pulse width, some devices also have Schmitt trigger input, and/or contain internal timing components for added design convenience.

DESCRIPTION

One-shots are versatile devices in digital circuit design. They are actually quite easy to use and are best suited for applications to generate or to modify short timings ranging from several tens of nanoseconds to a few microseconds. However, difficulties are constantly being experienced by design and test engineers, and basically fall into the categories of either pulse width problems or triggering difficulties.

The purpose of this note is to present an overall view of what one-shots are, how they work, and how to use them properly. It is intended to give the reader comprehensive information which will serve as a designer's guide to bipolar one-shots.

Nearly all malfunctions and failures on one-shots are caused by misuse or misunderstanding of their fundamental operating rules, characteristic design equations, parameters, or more frequently by poor circuit layout, improper bypassing, and improper triggering signal.

In the following sections all bipolar one-shots manufactured by National Semiconductor are presented with features tables and design charts for comparisons. Operating rules are outlined for devices in general and for specific device types. Notes on unique differences per device and on special operating considerations are detailed. Finally, truth tables and connection diagrams are included for reference.

DEFINITION

A one-shot integrated circuit is a device that, when triggered, produces an output pulse width that is independent of the input pulse width, and can be programmed by an external Resistor-Capacitor network. The output pulse width will be a function of the RC time constant. There are various one-shots manufactured by National Semiconductor that have diverse features, although, all one-shots have the basic property of producing a programmable output pulse width. All National one-shots have True and Complementary outputs, and both positive and negative edge-triggered inputs.

OPERATING RULES

In all cases, R and C represented by the timing equations are the external resistor and capacitor, called R_{EXT} and C_{EXT}, respectively, in the data book. All the foregoing timing equations use C in pF, R in Kohms, and yield t_W in nanoseconds. For those one-shots that are not retriggerable, there is a duty cycle specification as-

1

TTL AND LS-TTL ONE-SHOT FEATURES

Device Number	# Per IC Package	Re-trigger	Reset	Capacitor Min Max in μF	Resistor Min Max in Kohms	Timing Equation* for $C_{EXT} > 1000$ pF
DM54121	One	No	No	0 1000	1.4 30	$t_W = KRC \cdot (1 + 0.7/R)$
DM74121	One	No	No	0 1000	1.4 40	$K = 0.55$
DM54LS122	One	Yes	Yes	None	5 180	$t_W = KRC$
DM74LS122	One	Yes	Yes	None	5 260	$K = 0.45$
DM54123	Two	Yes	Yes	None	5 25	$t_W = KRC \cdot (1 + 0.7/R)$
DM74123	Two	Yes	Yes	None	5 50	$K = 0.34$
DM54LS123	Two	Yes	Yes	None	5 180	$t_W = KRC$
DM74LS123	Two	Yes	Yes	None	5 260	$K = 0.45$
DM54LS221	Two	No	Yes	0 1000	1.4 70	$t_W = KRC$
DM74LS221	Two	No	Yes	0 1000	1.4 100	$K = 0.7$
DM8601	One	Yes	No	None	5 25	$t_W = KRC \cdot (1 + 0.7/R)$
DM9601	One	Yes	No	None	5 50	$K = 0.32$
DM8602	Two	Yes	Yes	None	5 25	$t_W = KRC \cdot (1 + 1/R)$
DM9602	Two	Yes	Yes	None	5 50	$K = 0.31$

*The above timing equations hold for all combinations of R_{EXT} and C_{EXT} for all cases of $C_{EXT} > 1000$ pF within specified limits on the R_{EXT} and C_{EXT}.

sociated with them that defines the maximum trigger frequency as a function of the external resistor, R_{EXT}.

In all cases, an external (or internal) timing resistor (R_{EXT}) connects from V_{CC} or another voltage source to the "R_{EXT}/C_{EXT}" pin, and an external timing capacitor (C_{EXT}) connects between the "R_{EXT}/C_{EXT}", and "C_{EXT}" pins are required for proper operation. There are no other elements needed to program the output pulse width, though the value of the timing capacitor may vary from 0.0 to any necessary value.

When connecting the R_{EXT} and C_{EXT} timing elements, care must be taken to put these components absolutely as close to the device pins as possible, electrically and physically. Any distance between the timing components and the device will cause time-out errors in the resulting pulse width, because the series impedance (both resistive and inductive) will result in a voltage difference between the capacitor and the one-shot. Since the one-shot is designed to discharge the capacitor to a specific fixed voltage, the series voltage will "fool" the one-shot into releasing the capacitor before the capacitor is fully discharged. This will result in a pulse width that appears much shorter than the programmed value. We have encountered users who have been frustrated by pulse width problems and had difficulty to perform correlations with commercial test equipment. The nature of such problems are usually related to the improper layout of the DUT adapter boards. (See *Figure 6* for a PC layout of an AC test adapter board.) It has been demonstrated that lead length greater than 3 cm from the timing component to the device pins can cause pulse width problems on some devices.

For precise timing, precision resistors with good temperature coefficient should be used. Similarly, the timing capacitor must have low leakage, good dielectric absorption characteristics, and a low temperature coefficient for stability. Please consult manufacturers to obtain the proper type of component for the application.

For small time constants, high-grade mica glass, polystyrene, polypropylene, or polycarbonate capacitor may be used. For large time constants, use a solid tantalum or special aluminum capacitor.

In general, if a small timing capacitor is used that has leakage approaching 100 nA or if the stray capacitance from either terminal to ground is greater than 50 pF, then the timing equations or design curves which predict the pulse width would not represent the programmed pulse width which the device generates.

When an electrolytic capacitor is used for C_{EXT}, a switching diode is often suggested for standard TTL one-shots to prevent high inverse leakage current (*Figure 1*). In general, this switching diode is not required for LS-TTL devices; it is also not recommended with retriggerable applications.

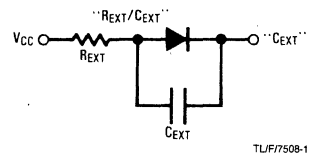


FIGURE 1

It is never a good practice to leave any unused inputs of a logic integrated circuit "floating". This is particularly true for one-shots. Floating uncommitted inputs or attempts to establish a logic HIGH level in this manner will result in malfunction of some devices.

Operating one-shots with values of the R_{EXT} outside the recommended limits is at the risk of the user. For some devices it will lead to complete inoperation, while for other devices it may result in either output pulse widths different from those values predicted by design charts or equations, or with modes of operation and performance quite difference from known standard characterizations.

To obtain variable pulse width by remote trimming, the following circuit is recommended (*Figure 2*). "R_{REMOTE}" should be placed as close to the one-shot as possible.

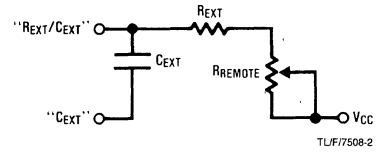


FIGURE 2

V_{CC} and ground wiring should conform to good high frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.001 μF to 0.1 μF bypass capacitor (disk or monolithic type) from the V_{CC} pin to ground is necessary on each device. Furthermore, the bypass capacitor should be located so as to provide as short an electrical path as possible between the V_{CC} and ground pins. In severe cases of supply-line noise, decoupling in the form of a local power supply voltage regulator is necessary.

For retriggerable devices the retrigger pulse width is calculated as follows for positive-edge triggering:

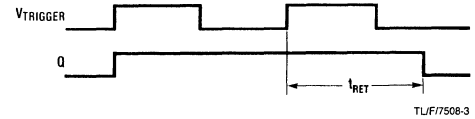


FIGURE 3

$$t_{RET} = t_W + t_{PLH} = K \cdot (R_{EXT})(C_{EXT}) + t_{PHL}$$

(See tables for exact expressions for K and t_W; K is unity on most HCMOS devices.)

SPECIAL CONSIDERATIONS AND NOTES:

The 9601 is the single version of the dual 9602 one-shot. With the exception of an internal timing resistor, R_{INT}, the 'LS122 has performance characteristics virtually identical to the 'LS123. The design and characteristic curves for equivalent devices are not depicted individually, as they can be referenced from their parent device.

National's TTL-'123 dual retriggerable one-shot features a unique logic realization not implemented by other manufacturers. The "CLEAR" input does not trigger the device, a design tailored for applications where it is desired only to terminate or to reduce the timing pulse width.

The 'LS221, even though it has pin-outs identical to the 'LS123, is not functionally identical. It should be remembered that the 'LS221 is a non-retriggerable one-shot, while the 'LS123 is a retriggerable one. For the 'LS123 device, it is sometimes recommended to externally ground its "C_{EXT}" pin for improved system performance. The "C_{EXT}" pin on the 'LS221, however, is not an internal connection to the device ground. Hence, grounding this pin on the 'LS221 device will render the device inoperative.

Furthermore, if a polarized timing capacitor is used on the 'LS221, the positive side of the capacitor should be connected to the "C_{EXT}" pin. For the 'LS123 part, it is the contrary, the negative terminal of the capacitor should be connected to the "C_{EXT}" pin of the device (*Figure 4*).

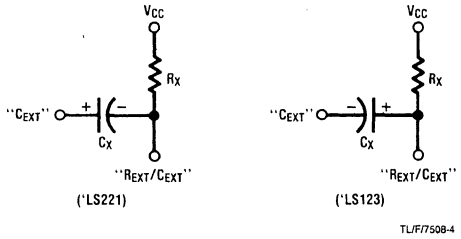


FIGURE 4

The 'LS221 trigger on "CLEAR": This mode of trigger requires first the "B-Input" be set from a Low-to-High level while the "CLEAR" input is maintained at logic Low level. Then, with the "B" Input at logic High level, the "CLEAR" input, whose positive transition from LOW-to-HIGH will trigger an output pulse ("A" input is LOW).

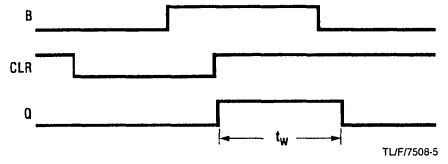


FIGURE 5

AC Test Adapter Board

The compact PC layout below is a universal one-shot test adapter board. By wiring different jumpers, it can be configured to accept all one-shots made by National Semiconductor. The configuration shown below is dedicated for the '123 device. It has been used successfully for functional and pulse width testing on all the '123 families of one-shots on the Teradyne AC test system.

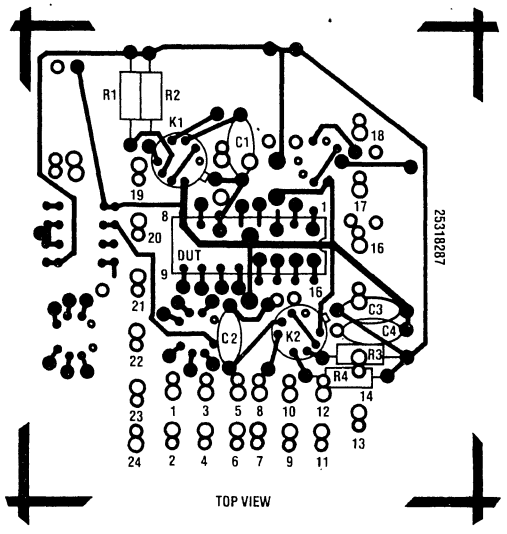


FIGURE 6a. AC Test Adapter

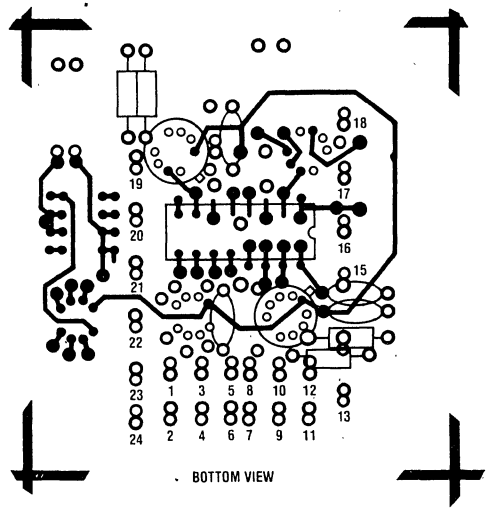


FIGURE 6b. AC Test Adapter

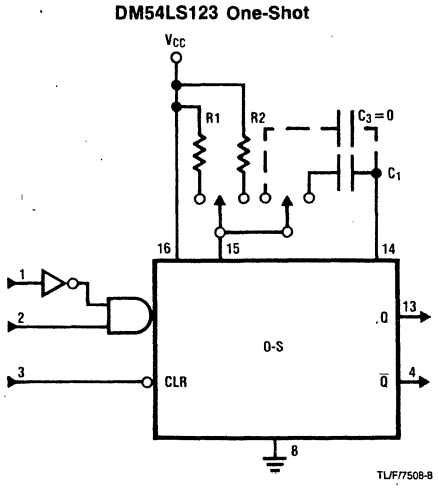
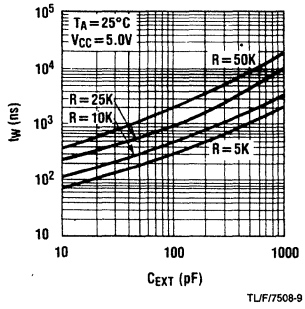


FIGURE 7a. Timing Components and I/O Connections to D.U.T.

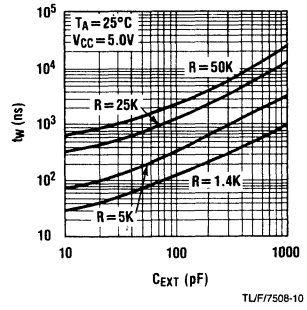
Typical Output Pulse Width vs Timing Components

Timing equations listed in the features tables hold all combinations of R_{EXT} and C_{EXT} for all cases of $C_{EXT} > 1000$ pF. For cases where the $C_{EXT} < 1000$ pF, use the graphs shown below.

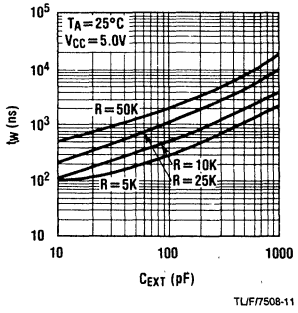
DM9602



DM74121



DM74123



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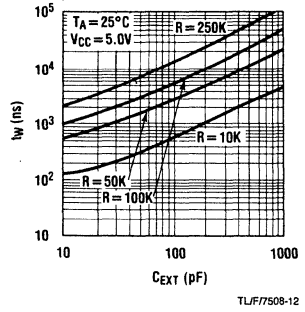
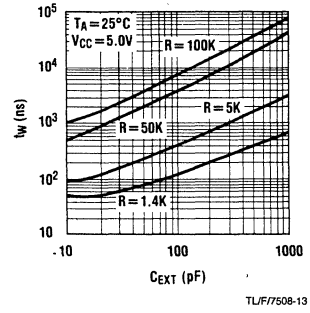


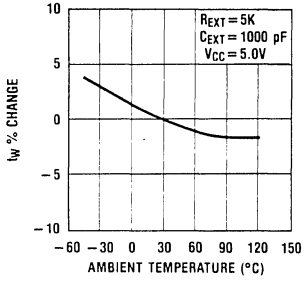
DM74LS221



Typical Output Pulse Width Variation vs Ambient Temperature

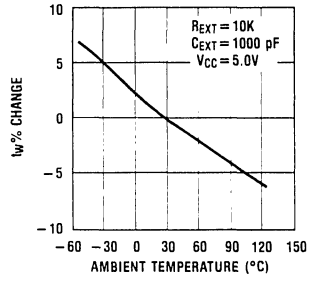
The graphs shown below demonstrate the typical shift in the device output pulse widths as a function of temperature. It should be noted that these graphs represent the temperature shift of the device after being corrected for any temperature shift in the timing components. Any shift in these components will result in a corresponding shift in the pulse width, as well as any shift due to the device itself.

DM74121



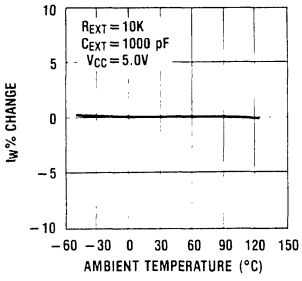
TL/F/7508-14

DM9602



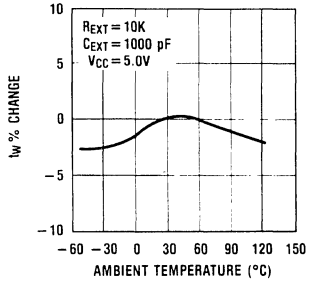
TL/F/7508-15

74LS221



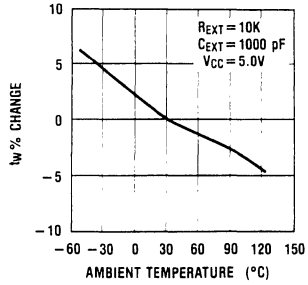
TL/F/7508-16

DM74LS123



TL/F/7508-17

DM74123



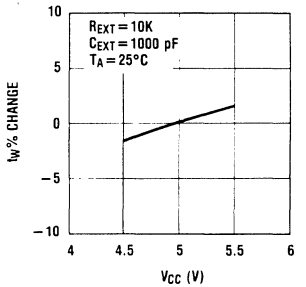
TL/F/7508-18

Typical Output Pulse Width Variation vs Supply Voltage

The following graphs show the dependence of the pulse width on V_{CC}.

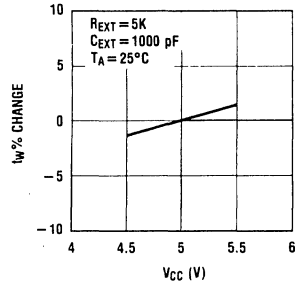
As with any IC applications, the device should be properly bypassed so that large transient switching currents can be easily supplied by the bypass capacitor. Capacitor values of 0.001 μF to 0.10 μF are generally used for the V_{CC} bypass capacitor.

DM9602



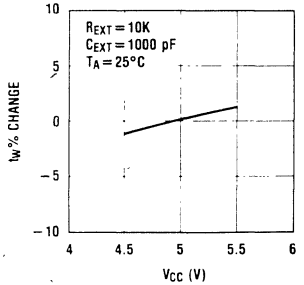
TL/F/7508-19

DM74121



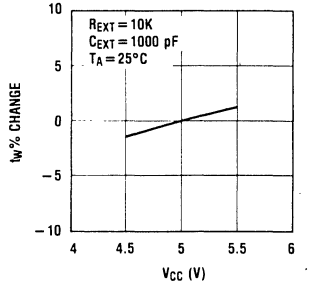
TL/F/7508-20

DM74123



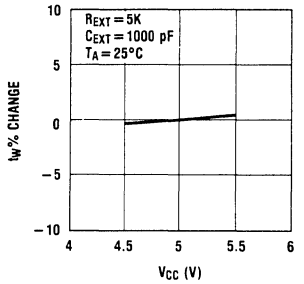
TL/F/7508-21

DM74LS123



TL/F/7508-22

DM74LS221

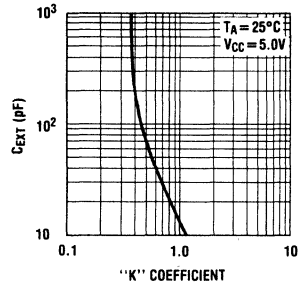


TL/F/7508-23

Typical "K" Coefficient Variation vs Timing Capacitance

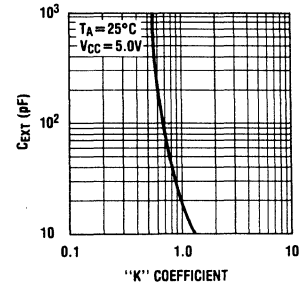
For certain one-shots, the "K" coefficient is not a constant, but varies as a function of the timing capacitor C_{EXT}. The graphs below detail this characteristic.

DM9602



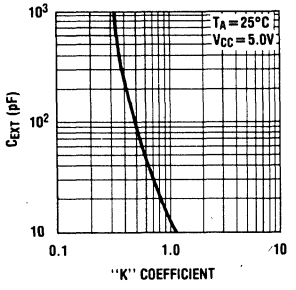
TL/F/7508-24

DM74121



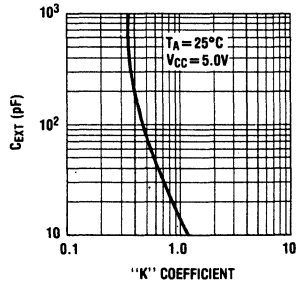
TL/F/7508-25

DM74123



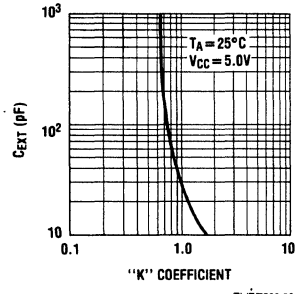
TL/F/7508-26

DM74LS123



TL/F/7508-27

DM74LS221

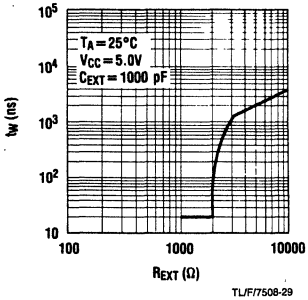


TL/F/7508-28

Typical Output Pulse Width vs Minimum Timing Resistance

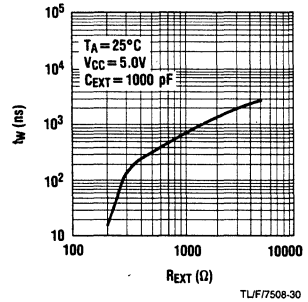
The plots shown below demonstrate typical pulse widths and limiting values of the true output as a function of the external timing resistor, R_{EXT}. This information should evaporate those years of mysterious notions and numerous concerns about operating one-shots with lower than recommended minimum R_{EXT} values.

DM9602



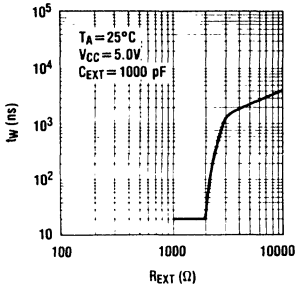
TL/F/7508-29

DM74121



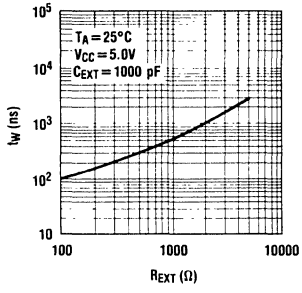
TL/F/7508-30

DM74123



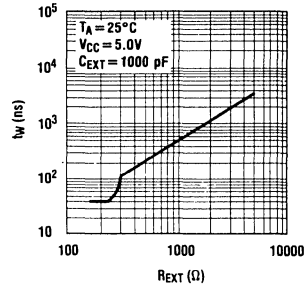
TL/F/7508-31

DM74LS123



TL/F/7508-32

DM74LS221



TL/F/7508-33

Function Tables

'121 One-Shots

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

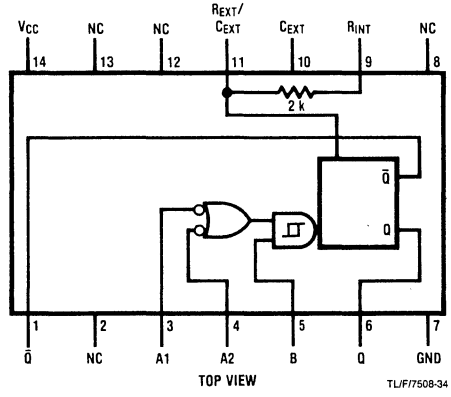
'122 Retriggerable One-Shots with Clear

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams

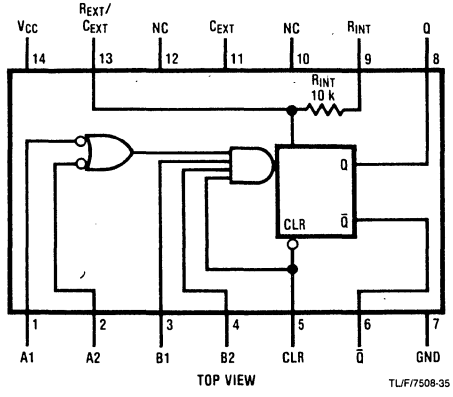
54121 (J, W); 74121 (N)



TOP VIEW

TL/F/7508-34

54LS122 (J, W); 74LS122 (N)



TOP VIEW

TL/F/7508-35

Function Tables (Continued)

'123 Dual Retriggerable One-Shots with Clear

'123

Inputs			Outputs	
A	B	CLEAR	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

'LS123

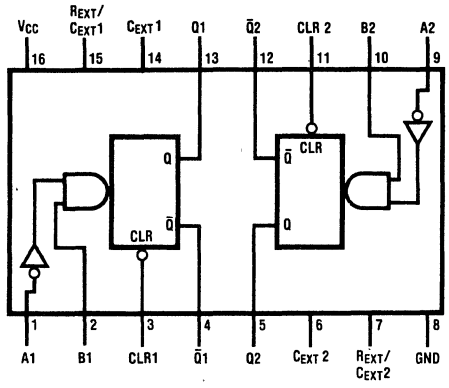
Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8602

Pin Numbers			Operation
A	B	CLEAR	
↓	L	H	Trigger
H	↑	H	Trigger
X	X	L	Reset

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

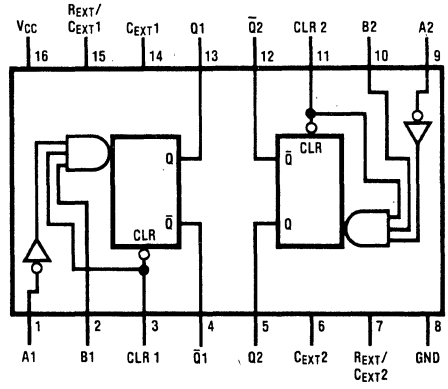
Connection Diagrams (Continued)



TOP VIEW

TL/F/7508-36

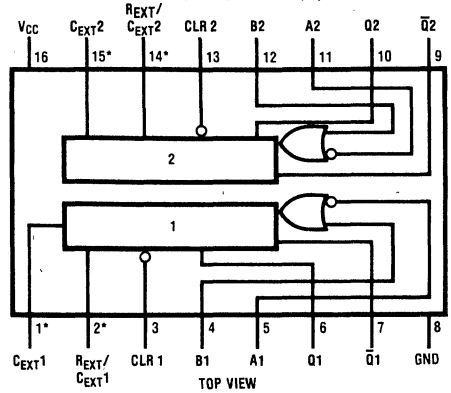
54LS123 (J, W); 74LS123 (N)



TOP VIEW

TL/F/7508-37

9602 (J, W); 8602 (N)



TOP VIEW

*Pins for external timing.

TL/F/7508-38

Function Tables (Continued)

'221 Dual One-Shots with Schmitt Trigger Inputs

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

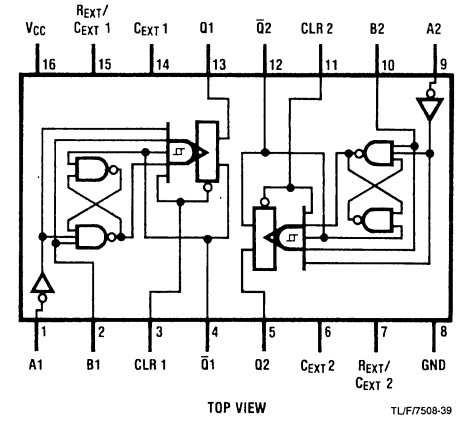
8601

Inputs				Outputs	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

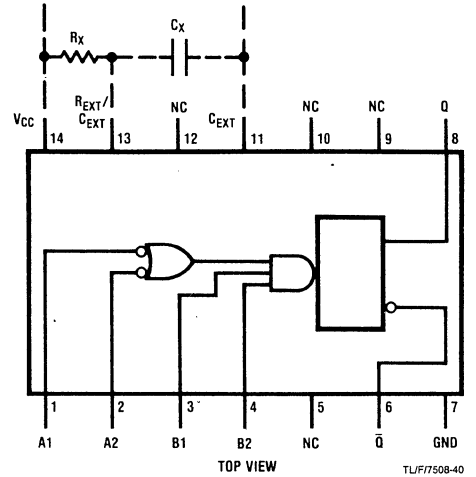
Connection Diagrams (Continued)

54LS221 (J, W); 74LS221 (N)



TOP VIEW TL/F/7508-39

9601 (J, W); 8601 (N)



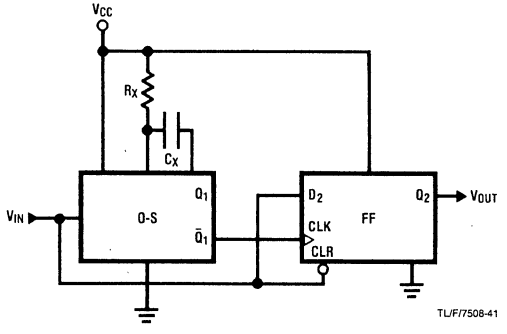
TOP VIEW TL/F/7508-40

Applications

The following circuits are shown with generalized one-shot connection diagram.

Noise Discriminator (*Figure 8*)

The time constant of the one-shot (O-S) can be adjusted so that an input pulse width narrower than that determined by the time constant will be rejected by the circuit. Output at Q_2 will follow the desired input pulse, with the leading edge delayed by the predetermined time constant. The output pulse width is also reduced by the amount of the time constant from R_X and C_X.



TL/F/7508-41

FIGURE 8. Noise Discriminator

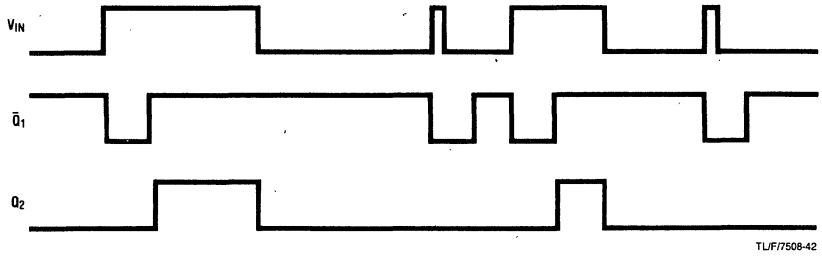
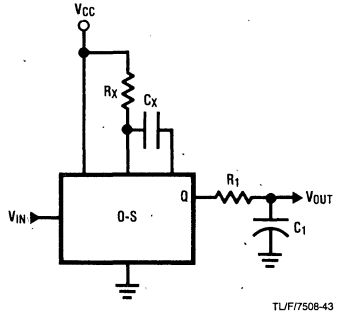


FIGURE 8. Noise Discriminator (Continued)

Frequency Discriminator (*Figure 9*)

The circuit shown in *Figure 9* can be used as a frequency-to-voltage converter. For a pulse train of varying frequency applied to the input, the one-shot will produce a pulse constant width for each triggering transition on its input. The output pulse train is integrated by R_1 and C_1 to yield a waveform whose amplitude is proportional to the input frequency. (Retriggerable device required.)



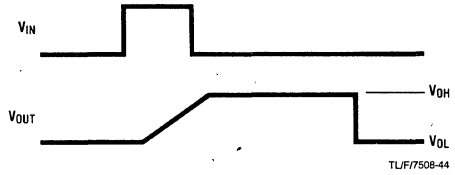
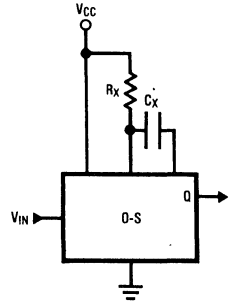


FIGURE 9. Frequency Discriminator

Envelope Detector (*Figures 10a and 10b*)

An envelope detector can be made by using the one-shot's retrigger mode. The time constant of the device is selected to be slightly longer than the period of each cycle within the input pulse burst. Two distinct DC levels are present at the output for the duration of the input pulse burst and for its absence (see *Figure 10a*). The same circuit can also be employed for a specific frequency input as a Schmitt trigger to obviate input trigger problems associated with hysteresis and slow varying, noisy waveforms (see *Figure 10b*). (Retriggerable device required.)



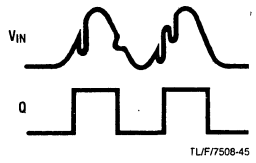


FIGURE 10b. Schmitt Trigger

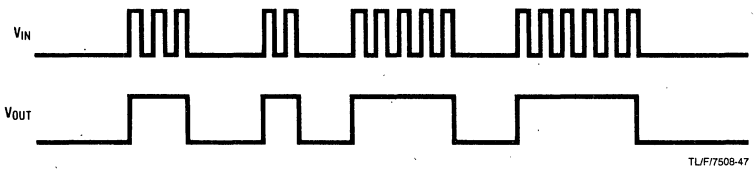
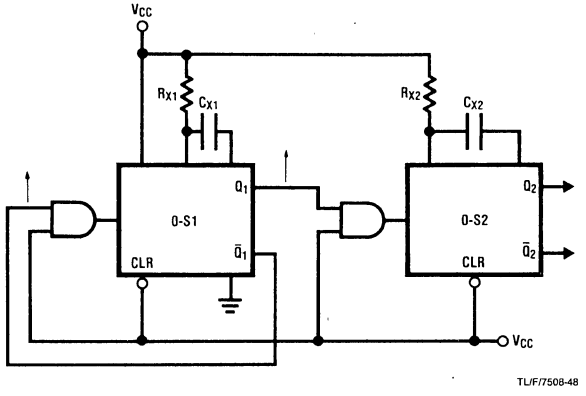


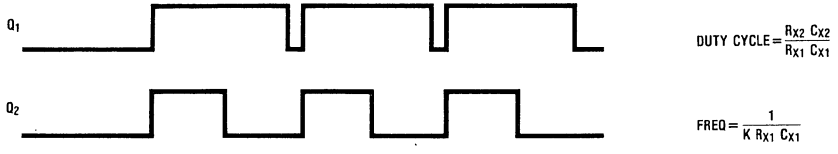
FIGURE 10a. Envelope Detector (Retriggerable Device Required)

Pulse Generator (*Figure 11*)

Two one-shots can be connected together to form a pulse generator capable of variable frequency and independent duty cycle control. The R_{X1} and C_{X1} of O-S1 determine the frequency developed at output Q_1. R_{X2} and C_{X2} of O-S2 determine the output pulse width at Q_2. (Retriggerable device required.)



TL/F/7508-48



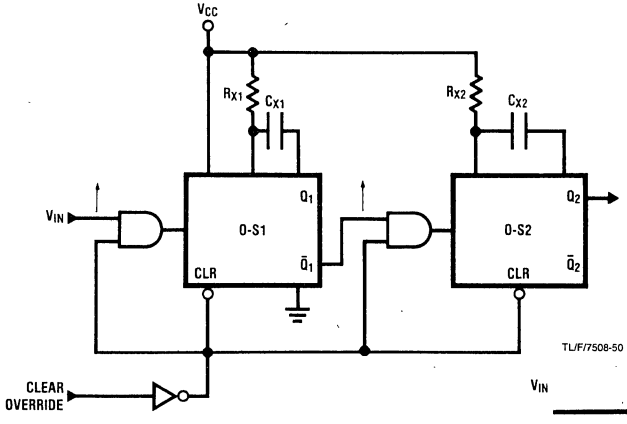
TL/F/7508-49

FIGURE 11. Pulse Generator (Retriggerable Device Required)

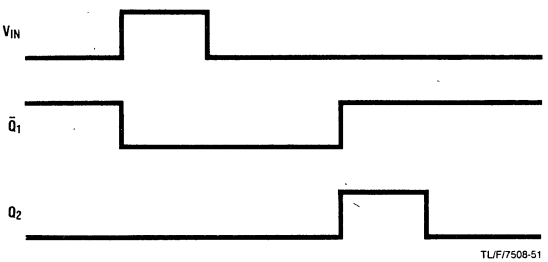
Note: K is the multiplication factor dependent of the device. Arrow indicates edge-trigger mode.

Delayed Pulse Generator with Override to Terminate Output Pulse (*Figure 12*)

An input pulse of a particular width can be delayed with the circuit shown in *Figure 12*. Preselected values of R_{X1} and C_{X1} determine the delay time via O-S1, while preselected values of R_{X2} and C_{X2} determine the output pulse width through O-S2. The override input can additionally serve to modify the output pulse width.



TL/F/7508-50



TL/F/7508-51

FIGURE 12. Delayed Pulse Generator with Override to Terminate Output Pulse

Missing Pulse Detector (*Figure 13*)

By setting the time constant of O-S1 through R_{X1} and C_{X1} to be at least one full period of the incoming pulse period, the one-shot will be continuously retriggered as long as no missing pulse occurs. Hence, $\overline{Q}_1$ remains LOW until a pulse is missing in the incoming pulse train, which then triggers O-S2 and produces an indicating pulse at Q_2. (Retriggerable device required.)

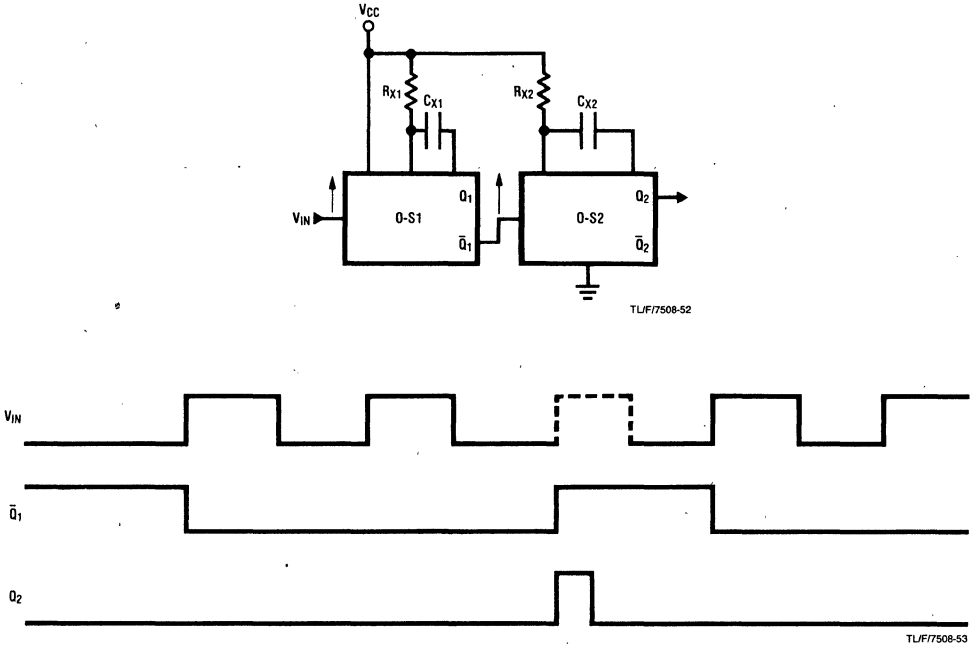


FIGURE 13. Missing Pulse Detector (Retriggerable Device Required)

Pulse Width Detector (*Figure 14*)

The circuit of *Figure 14* produces an output pulse at V_{OUT} if the pulse width at V_{IN} is wider than the predetermined pulse width set by R_X and C_X.

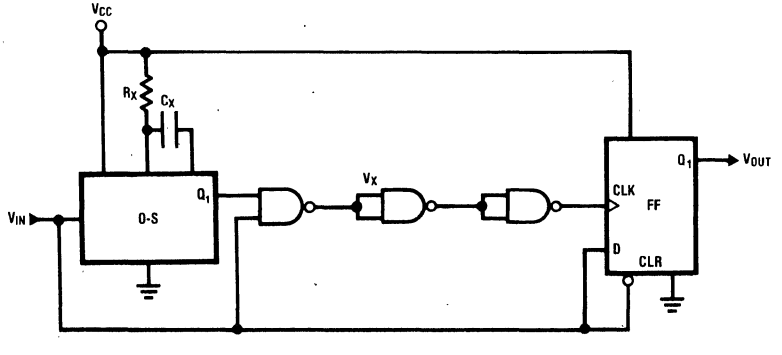


FIGURE 14. Pulse Width Detector

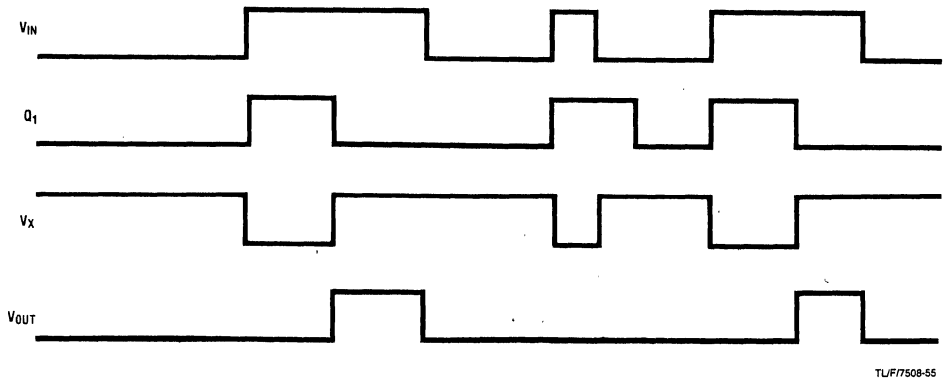
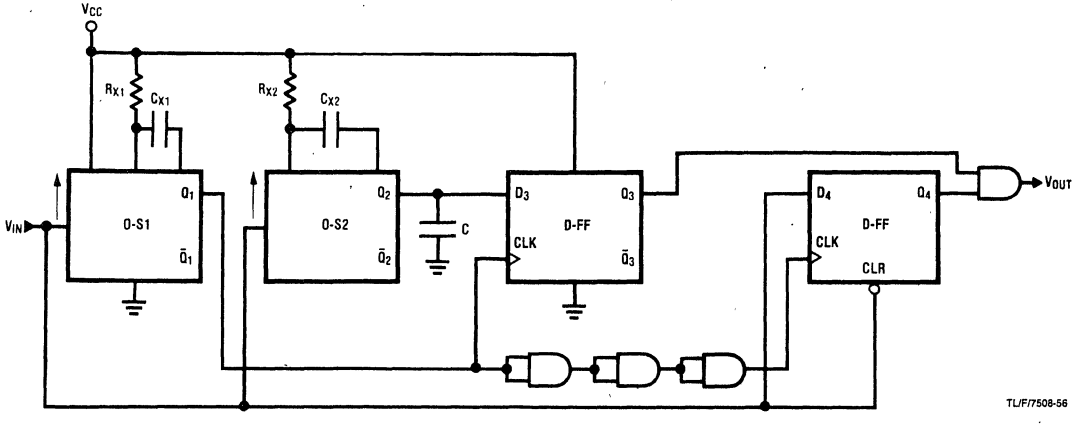


FIGURE 14. Pulse Width Detector (Continued)

Band Pass Filter (*Figure 15*)

The band pass of the circuit is determined by the time constants of the two low-pass filters represented by O-S1 and O-S2. With the output at Q_2 delayed by C, the D-flip flop (D-FF) clocks HIGH only when the cutoff frequency of O-S2 has been exceeded. The output at Q_3 is gated with the delayed input pulse train at Q_4 to produce the desired output. (Retriggerable device required.)



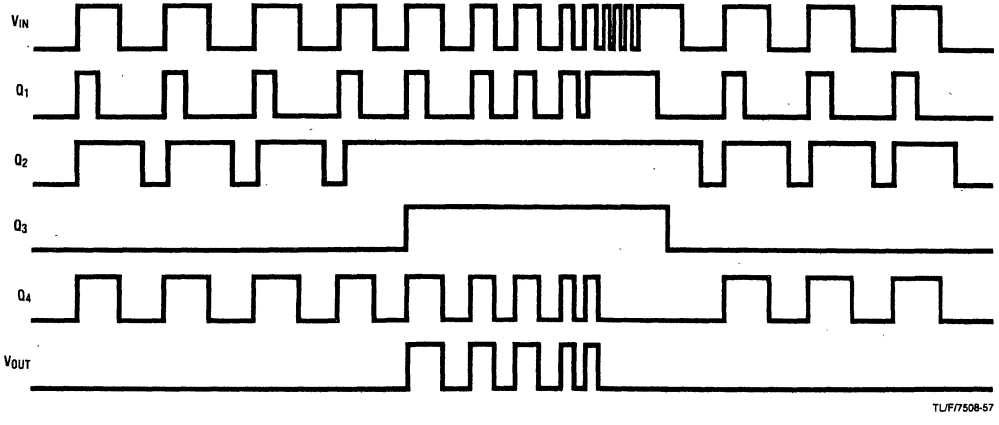


FIGURE 15. Band Pass Filter (Retriggerable Device Required)

FM Data Separator (*Figure 16*)

The data separator shown in *Figure 16* is a two-time constant separator that can be used on tape and disc drive memory storage systems. The clock and data pulses must fall within prespecified time windows. Both the clock and data windows are generated in this circuit. There are two data windows; the short window is used when the previous bit cell had a data pulse in it, while the long window is used when the previous bit cell had no data pulse.

If the data pulse initially falls into the data window, the −SEP DATA output returns to the NAND gate that generates the data window, to assure that the full data is allowed through before the window times out. The clock windows will take up the remainder of the bit cell time.

Assume all one-shots and flip-flops are reset initially and the +READ DATA has the data stream as indicated.

With O-S1 and O-S2 inactive, +CLK WINDOW is active. The first +READ DATA pulse will be gated through the second AND gate, which becomes −SEP CLK for triggering of the R-S FF and the one-shots. With the D-FF off, O-S1 will remain reset. The −SEP CLK pulse will trigger O-S2, whose output is sent to the OR gate, and its output becomes +DATA WINDOW to enable the first AND gate. The next pulse on +READ DATA will be allowed through the first AND gate to become −SEP DATA. This pulse sets the R-S FF, whose HIGH output becomes the data to the D-FF. The D-FF is clocked on by O-S2 timing out and +CLK WINDOW becoming active. $\overline{Q_4}$ will hold O-S2 reset and allow O-S1 to trigger on the next clock pulse.

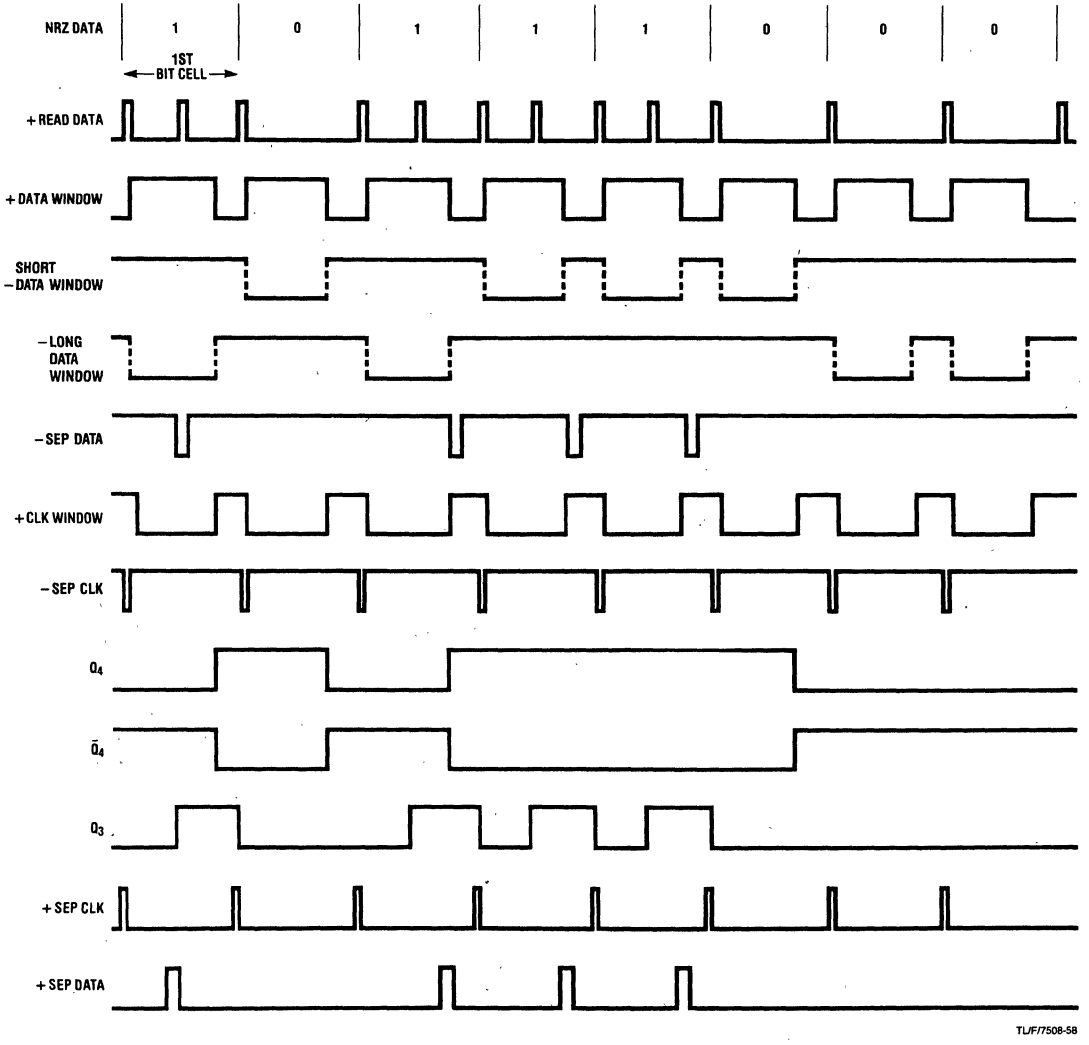


FIGURE 16. FM Data Separator

The next clock pulse (the second bit cell) is ANDed with +CLK WINDOW and becomes the next −SEP CLK, which will reset the R-S FF and trigger O-S1. As O-S1 becomes active, the +DATA WINDOW becomes active, enabling the first AND gate. With no data bit in the second bit cell, the R-S FF will remain reset, enabling the D-FF to be clocked off when +DATA WINDOW falls. When the D-FF is clocked off, Q_4 will hold O-S1 reset and allow O-S2 to be triggered.

The third clock pulse (bit cell 3) is ANDed with +CLK WINDOW and becomes −SEP CLK, which continues resetting the R-S FF and triggers O-S2. When O-S2 becomes active, +DATA WINDOW enables the first AND gate, allowing the data pulse in bit cell 3 to become −SEP DATA. This −SEP DATA will set the R-S FF, which enables the D-FF to be clocked on when +DATA WINDOW falls. When this happens, Q_4 will hold O-S2 reset and allow O-S1 to trigger. This procedure continues as long as there is clock and data pulse stream present on the +READ DATA line.

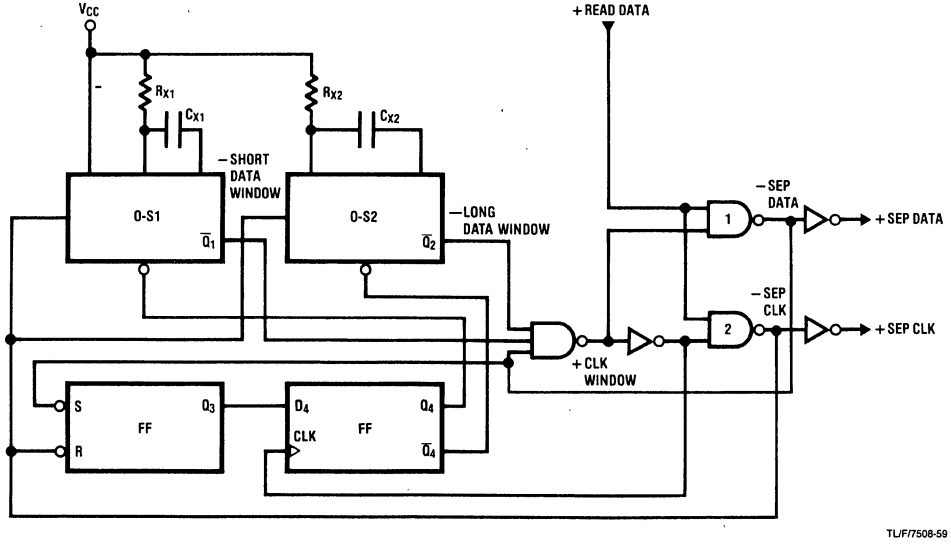


FIGURE 16. FM Data Separator (Continued)

Phase-Locked Loop VCO (*Figure 17*)

The circuit shown in *Figure 17* represents the VCO in the data separation part of a rotational memory storage system which generates the bit rate synchronous clocks for write data timing and for establishing the read data windows.

The op-amp that performs the phase-lock control operates by having its inverting input be driven by two sources that normally buck one another. One source is the one-shot, the other source is the phase detector flip-flop. When set, the one-shot, through an inverter, supplies a HIGH-level voltage to the summing node of the op-amp and the phase detector FF, also through an inverter, supplies a cancelling LOW-level input.

It is only when the two sources are out of phase with each other, that is one HIGH and the other LOW, that a positive- or negative-going phase error will be applied to the op-amp to effect a change in the VCO frequency. *Figure 17* illustrates the process of phase-error detection and correction when synchronizing to a data bit pattern. The rising edge of each pulse at DATA+PLO clocks the one-shot LOW and the phase detector FF HIGH. Since both outputs are still bucking each other, no change will be observed at the phase-error summing node. When the one-shot times out, if this occurs after the 2F clock has reset the phase detector FF to a LOW output, a positive pulse will be seen at the summing node until both the one-shot and the FF are reset. Any positive pulse will be reflected by a negative change in

the op-amp output, which is integrated and reduces the positive control voltage at the VCO input in direct proportion to the duration of the phase-error pulse. A negative phase-error pulse occurs when the phase detector FF remains set longer than the one-shot.

Negative phase-error pulse causes the integrated control voltage to swing positive in direct proportion to the duration of the phase-error pulse. It is recommended that a clamping circuit be connected to the output of the op-amp to prevent the VCO control voltage from going negative or more positive than necessary. A back-to-back diode pair connected between the op-amp and the VCO is highly recommended, for it will present a high impedance to the VCO input during locked mode. This way, stable and smooth operation of the PLO circuit is assured.

2F Bit Rate Synchronous Read/Write Clock

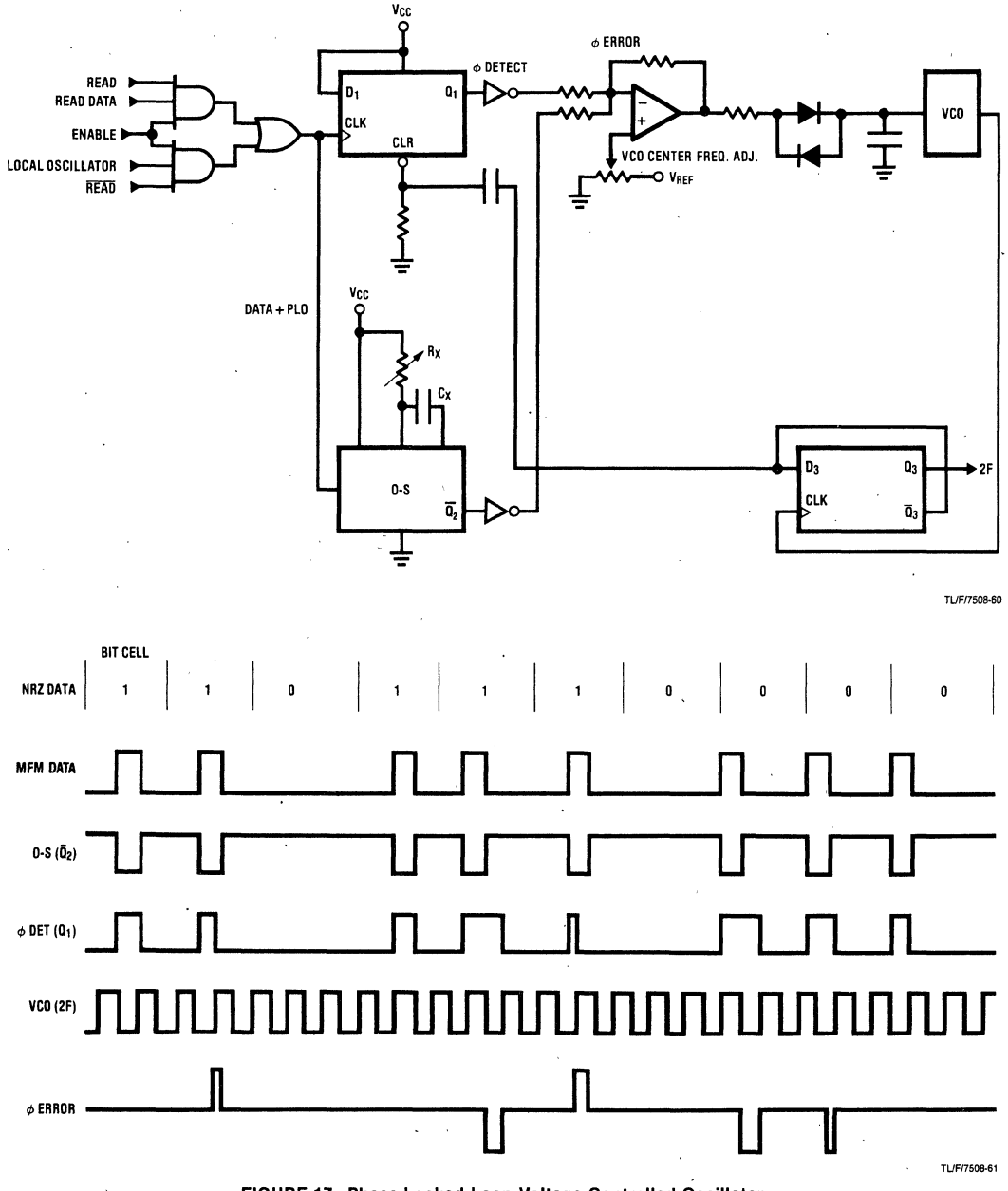


FIGURE 17. Phase-Locked Loop Voltage Controlled Oscillator

A FINAL NOTE

It is hoped that this brief note will clarify many pertinent and subtle points on the use and testing of one-shots. We invite your comments to this application note and solicit your constructive criticism to help us improve our service to you.

ACKNOWLEDGEMENT

The author wishes to thank Stephen Wong, Bill Llewellyn, Walt Sirovy, Dennis Worden, Stephen Yuen, Weber Lau, Chris Henry and Michelle Fong for their help and guidance.

Functional Index/Selection Guide

* Several methods are used to represent typical values. For propagation delay typical values, the average of the typical values of the two delays are used.

$$\left[\frac{t_{PHL(TYP)} + t_{PLH(TYP)}}{2}\right]$$

For power dissipation, the average of the typical values of current for all states the outputs can achieve is used. (I_{CCL}, I_{CCH}, I_{CCZ}). This current value is multiplied by nominal supply voltage (5V), and in some case divided by the number of gates, bits, etc. All other typical values are singular typicals.

Adders

Description	Device Type	Typ* Carry Time (ns)	Typ* Add Time (ns)	Typ* Power Diss. /Bit (mW)	Package Avail.		Page
					Mil	Com	
Single 4-Bit Full Adders	54/74LS283	12	15	24	J,W	N	4-298
	54/74S283	8.5	11	110	J,W	N	5-147
	54/74LS83A	12	15	24	J,W	N	4-93
	54/7483	12	20	73	J,W	N	6-113

Arithmetic Logic Units, Carry Look-Ahead Generators

Description	Device Type	Typ* Carry Time (ns)	Typ* Add Time (ns)	Typ* Power Diss. Total (mW)	Package Avail.		Page
					Mil	Com	
4-Bit ALU/ Function Generators	54/74AS181B	5	5	675	J	N	3-85
	54/74S181	7	14	600	J,W	N	5-100
	54/74181	12.5	18	455	J,W	N	6-245
	54/74S381	10	12	525	J,W	N	5-165
	54/74AS881B	5	5	675	J	N	3-256
Carry Look-Ahead Generator	54/74AS182	5	N/A	115	J	N	3-93
	54/74S182	9	N/A	345	J,W	N	5-108
	54/74AS264	6	N/A	140	J	N	3-124
	54/74AS282	6	N/A	130	J	N	3-132

Buffers/Clock Drivers with Totem-Pole Outputs

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Dual 4-Input NAND Buffers	54ALS40	12	−1	4	3.5	J		2-58
	74ALS40	24	−2.6	4	3.5		N	2-58
	54LS40	12	−1.2	10	4.3	J,W		4-53
	74LS40	24	−1.2	10	4.3		N	4-53
	54/74S40	60	−3	4	44	J,W	N	5-33
	54/7440	48	−1.2	10.5	26	J,W	N	6-63
	54ALS1020	12	−1	4	3.6	J		2-287
	74ALS1020	24	−2.6	4	3.6		N	2-287
Quad 2-Input NAND Buffers	54ALS37	12	−1	5	5	J		2-54
	74ALS37	24	−2.6	5	5		N	2-54
	54LS37	12	−1.2	10	4.3	J,W		4-49
	74LS37	24	−1.2	10	4.3		N	4-49
	54/7437	48	−1.2	10.5	27	J,W	N	6-62
	54ALS1000	12	−1	5	3.5	J		2-271
	74ALS1000	24	−2.6	5	3.5		N	2-271
	54AS1000	40	−40	2	8.5	J	N	3-267
	74AS1000	48	−48	2	8.5	J	N	3-267

Buffers/Clock Drivers with Totem-Pole Outputs (Continued)

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Quad 2-Input NOR Buffers	54ALS28	12	−1	3.7	4.5	J		2-46
	74ALS28	24	−2.6	3.7	4.5		N	2-46
	54ALS1002	12	−1	3.7	4.5	J		2-273
	74ALS1002	24	−2.6	3.7	4.5		N	2-273
	54AS1036	40	−40	2	9.7	J		3-277
	74AS1036	48	−48	2	9.7		N	3-277
Quad 2-Input OR	54ALS1032	12	−1	5.5	5.7	J		2-289
	74ALS1032	24	−2.6	5.5	5.7		N	2-289
	54AS1032	40	−40	2.5	14	J		3-273
	74AS1032	48	−48	2.5	14		N	3-273
Quad 2-Input AND	54ALS1008	12	−1	5.6	4.7	J		2-281
	74ALS1008	24	−2.6	5.6	4.7		N	2-281
	54AS1008	40	−40	2.5	12	J		3-271
	74AS1008	48	−48	2.5	12		N	3-271
Triple 3-Input NAND	54ALS1010	12	−1	4	3.6	J		2-283
	74ALS1010	24	−2.6	4	3.6		N	2-283
Triple 3-Input AND	54ALS1011	12	−1	6.4	4.75	J		2-285
	74ALS1011	24	−2.6	6.4	4.75		N	2-285
Hex Buffers	54ALS1034	12	−12	4.5	4.6	J		2-291
	74ALS1034	24	−15	4.5	4.6		N	2-291
	54AS1034	40	−40	2.5	11.9	J		3-275
	74AS1034	48	−48	2.5	11.9		N	3-275
Hex Inverter Buffers	54ALS1004	12	−12	2.6	3.3	J		2-277
	74ALS1004	24	−15	2.6	3.3		N	2-277
	54AS1004	40	−40	1.7	8.5	J		3-269
	74AS1004	48	−48	1.7	8.5		N	3-269

Buffers/Clock Drivers with Open-Collector Outputs

Description	Device Type	High-Level Output Voltage (V)	Low-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Quad 2-Input NAND Buffers	54ALS38	5.5	12	14.5	3.5	J		2-56
	74ALS38	5.5	24	14.5	3.5		N	2-56
	54LS38	5.5	12	15	4.3	J,W		4-51
	74LS38	5.5	24	15	4.3		N	4-51
	54/7438	5.5	48	12.5	24.4	J,W	N	6-64
	54LS26	15	4	16	2	J,W		4-41
	74LS26	15	8	16	2		N	4-41
	54/7426	15	16	13.5	10	J,W	N	6-54
	54L26	15	2	33	1	J,W		7-23
	74L26	15	3.6	33	1		N	7-23
	54ALS1003	5.5	12	14.5	3.5	J		2-275
	74ALS1003	5.5	24	14.5	3.5		N	2-275

Buffers/Clock Drivers with Open-Collector Outputs (Continued)

Description	Device Type	High-Level Output Voltage (V)	Low-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Quad 2-Input NOR Buffers	54ALS33	5.5	12	13.5	4.5	J		2-52
	74ALS33	5.5	24	13.5	4.5		N	2-52
Hex Buffers/ Drivers	5407	30	30	13	21	J,W		6-30
	7407	30	40	13	21		N	6-30
	5417	15	30	13	21	J,W		6-48
	7417	15	40	13	21		N	6-48
	54ALS1035	5.5	12	12.5	4.6	J		2-293
	74ALS1035	5.5	24	12.5	4.6		N	2-293
Hex Inverter Buffers/ Drivers	5406	30	30	12.5	26	J,W		6-28
	7406	30	40	12.5	26		N	6-28
	5416	15	30	12.5	26	J,W		6-46
	7416	15	40	12.5	26		N	6-46
	54ALS1005	5.5	12	12.5	3.3	J		2-279
	74ALS1005	5.5	24	12.5	3.3		N	2-279

Buffer Gates with TRI-STATE® Totem-Pole Outputs

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Quad Buffers	54LS125A	−1	12	10	14.4	J,W		4-140
	74LS125A	−2.6	24	10	14.4		N	4-140
	54125	−2	16	11	40	J,W		6-157
	74125	−5.2	16	11	40		N	6-157
	54LS126A	−1	12	10	14.4	J,W		4-143
	74LS126A	−2.6	24	10	14.4		N	4-143
	54126	−2	16	11	45	J,W		6-160
	74126	−5.2	16	11	45		N	6-160
Hex Buffers	54LS365A	−1	12	10	10.8	J,W		4-320
	74LS365A	−2.6	24	10	10.8		N	4-320
	54365	−2	32	10.5	51.6	J,W		6-309
	74365	−5.2	32	10.5	51.6		N	6-309
	54LS367A	−1	12	10	10.8	J,W		4-326
	74LS367A	−2.6	24	10	10.8		N	4-326
	54367	−2	32	12	51.6	J,W		6-315
	74367	−5.2	32	12	51.6		N	6-315
Hex Inverter Buffers	54LS366A	−1	12	10	10.8	J,W		4-323
	74LS366A	−2.6	24	10	10.8		N	4-323
	54366	−2	32	10.5	51.6	J,W		6-312
	74366	−5.2	32	10.5	51.6		N	6-312
	54LS368A	−1	12	10	10.8	J,W		4-329
	74LS368A	−2.6	24	10	10.8		N	4-329
	54368	−2	32	10.5	51.6	J,W		6-318
	74368	−5.2	32	10.5	51.6		N	6-318
	70L98	−1	2	30	3	J,W		7-91
	80L98	−1	3.6	30	3		N	7-91

Buffer Gates with TRI-STATE Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Octal Buffers	54ALS465	– 12	12	6.6	8.6	J,W		2-184
	74ALS465	– 15	24	6.6	8.6		N	2-184
	54LS465	– 2.6	12	14.5	10	J,W		4-348
	74LS465	– 5.2	24	14.5	10		N	4-348
	54ALS467	– 12	12	6.6	9.1	J,W		2-184
	74ALS467	– 15	24	6.6	9.1		N	2-184
	54LS467	– 2.6	12	14.5	10	J,W		4-348
	74LS467	– 5.2	24	14.5	10		N	4-348
Octal Inverter Buffers	54ALS466	– 12	12	4.8	7.5	J,W		2-184
	74ALS466	– 15	24	4.8	7.5		N	2-184
	54LS466	– 2.6	12	9.5	8	J,W		4-348
	74LS466	– 5.2	24	9.5	8		N	4-348
	54ALS468	– 12	12	4.7	7.5	J,W		2-184
	74ALS468	– 15	24	4.7	7.5		N	2-184
	54LS468	– 2.6	12	9.5	8	J,W		4-348
	74LS468	– 5.2	24	9.5	8		N	4-348
12-Input NAND Gate/Buffer	54/74S134	– 6.5	20	4.5	45	J,W	N	5-60
Quad Inverter Transceivers	54ALS242	– 12	12	5.6	16.3	J		2-144
	74ALS242	– 15	24	5.6	16.3		N	2-144
	54AS242	– 12	48	3.5	33.8	J		3-105
	74AS242	– 15	64	3.5	33.8		N	3-105
	54LS242	– 12	12	11	31.8	J,W		4-258
	74LS242	– 15	24	11	31.8		N	4-258
	54S242	– 12	48	4.5	112.5	J,W		5-128
	74S242	– 15	64	4.5	112.5		N	5-128
Quad Transceivers	54ALS243	– 12	12	6	23.3	J		2-144
	74ALS243	– 15	24	6	23.3		N	2-144
	54AS243	– 12	48	4	45.8	J		3-105
	74AS243	– 15	64	4	45.8		N	3-105
	54LS243	– 15	12	12	34.5	J,W		4-258
	74LS243	– 15	24	12	34.5		N	4-258
	54S243	– 12	48	5	139.6	J,W		5-128
	74S243	– 15	64	5	139.6		N	5-128
Octal Inverter Bus Buffers/ Drivers	54AS231	– 12	40	3.5	18.5	J		3-102
	74AS231	– 15	48	3.5	18.5		N	3-102
	54ALS240	– 12	12	2.6	6.5	J		2-141
	74ALS240	– 15	24	2.6	6.5		N	2-141
	54AS240	– 12	48	3.5	19.2	J		3-105
	74AS240	– 15	64	3.5	19.2		N	3-105
	54LS240	– 12	12	10	14.2	J,W		4-255
	74LS240	– 15	24	10	14.2		N	4-255
	54S240	– 12	48	5	56.3	J,W		5-125
	74S240	– 15	64	5	56.3		N	5-125
	54S940	– 12	48	5	56.3	J,W		5-169
	74S940	– 15	64	5	56.3		N	5-169
	54ALS1240	– 12	8	9	5.9	J		2-295
	74ALS1240	– 15	16	9	5.9		N	2-295

Buffer Gates with TRI-STATE Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Octal Bus Buffers/ Drivers	54ALS241	−12	12	4.3	8.6	J		2-141
	74ALS241	−15	24	4.3	8.6		N	2-141
	54AS241	−12	48	4	24.6	J		3-105
	74AS241	−15	64	4	24.6		N	3-105
	54LS241	−12	12	10	14.2	J,W		4-255
	74LS241	−15	24	10	14.2		N	4-255
	54S241	−12	48	5	67.2	J,W		5-125
	74S241	−15	64	5	67.2		N	5-125
	54ALS244	−12	12	4.3	8.5	J		2-147
	74ALS244	−15	24	4.3	8.5		N	2-147
	54AS244	−12	48	4	24.1	J		3-105
	74AS244	−15	64	4	24.1		N	3-105
	54LS244	−12	12	10	24.6	J,W		4-261
	74LS244	−15	24	10	24.6		N	4-261
	54S244	−12	48	5	67.2	J,W		5-125
	74S244	−15	64	5	67.2		N	5-125
	54S941	−12	48	5	67.2	J,W		5-169
	74S941	−15	64	5	67.2		N	5-169
	54ALS1241	−12	12	9	5.9	J		2-295
	74ALS1241	−15	24	9	5.9		N	2-295
	54ALS1244	−12	12	9	5.9	J		2-303
	74ALS1244	−15	24	9	5.9		N	2-303
Octal Transceivers	54ALS245	−12	12	9	21.7	J		2-150
	74ALS245	−15	24	9	21.7		N	2-150
	54AS245	−12	32	5.5	49.1	J		3-111
	74AS245	−15	48	5.5	49.1		N	3-111
	54LS245	−12	12	8	36.3	J,W		4-264
	74LS245	−15	24	8	36.3		N	4-264
	54ALS623	−12	12	9	20	J		2-225
	74ALS623	−15	24	9	20		N	2-225
	54AS623	−12	48	5	49.2	J		3-181
	74AS623	−15	64	5	49.2		N	3-181
	54ALS645	−12	12	5	21.7	J		*
	74ALS645	−15	24	5	21.7		N	*
	54AS645	−12	48	5.5	49.2	J		3-189
	74AS645	−15	64	5.5	49.2		N	3-189
	54LS645	−12	12	8	36	J,W		4-354
	74LS645	−15	24	8	36		N	4-354
	54ALS1243	−12	8	7	19	J		2-299
	74ALS1243	−15	16	7	19		N	2-299
	54ALS1245	−12	8	9	14	J	N	2-306
	74ALS1245	−15	16	9	14	J	N	2-306
	54ALS1623	−12	8	7.5	8.9	J		2-315
	74ALS1623	−15	16	7.5	8.9		N	2-315
	54ALS1645	−12	8	7.5	14.4	J		2-322
	74ALS1645	−15	16	7.5	14.4		N	2-322

*Request Data Sheet

Buffer Gates with TRI-STATE Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Octal Inverter Transceivers	54ALS620	– 12	12	8	14.6	J		2-219
	74ALS620	– 15	24	8	14.6		N	2-219
	54AS620	– 12	48	5.5	32.7	J		3-181
	74AS620	– 15	64	5.5	32.7		N	3-181
	54ALS640	– 12	12	5	15.4	J		*
	74ALS640	– 15	24	5	15.4		N	*
	54AS640	– 12	48	4	32.9	J		3-189
	74AS640	– 15	64	4	32.9		N	3-189
	54ALS1242	– 12	12	5	10.9	J		2-299
	74ALS1242	– 15	24	5	10.9		N	2-299
	54ALS1620	– 12	8	7.5	11.3	J		2-309
	74ALS1620	– 15	16	7.5	11.3		N	2-309
	54ALS1640	– 12	8	5.5	11.3	J		2-322
	74ALS1640	– 15	16	5.5	11.3		N	2-322
Octal Trans-ceivers with True and Inverting Outputs	54AS230	– 12	48	3.5	20.8	J		3-102
	74AS230	– 15	64	3.5	20.8		N	3-102
	54ALS643	– 12	12	5	19.4	J		*
	74ALS643	– 15	24	5	19.4		N	*
	54AS643	– 12	48	4	44.4	J		3-189
	74AS643	– 15	64	4	44.4		N	3-189
	54ALS1643	– 12	8	8	13.8	J		2-322
	74ALS1643	– 15	16	8	13.8		N	2-322
Octal Trans-ceivers with Register Storage	54AS646	– 12	32	5	93.8	J		3-194
	74AS646	– 15	48	5	93.8		N	3-194
	54AS652	– 12	32	5	93.8	J		3-199
	74AS652	– 15	48	5	93.8		N	3-199
Octal Inverter Transceivers with Register Storage	54AS648	– 12	32	6	81.3	J		3-194
	74AS648	– 15	48	6	81.3		N	3-194
	54AS651	– 12	32	6	81.3	J		3-199
	74AS651	– 15	48	6	81.3		N	3-199
Octal Inverting Transceivers/ MOS Drivers	54/74AS2620	– 2	1	4.5	38.3	J	N	3-279
	54/74ALS2640					J	N	2-330
	54/74AS2640	– 2	1	5.5	34.6	J	N	3-282
Octal Bus Transceivers/ MOS Drivers with True and Inverting Outputs	54/74ALS2643					J	N	2-322
	54/74AS2643					J	N	3-282
Octal Bus Transceivers/ MOS Drivers	54/74AS2623	– 2	1	5.5	51	J	N	3-279
	54/74ALS2645					J	N	2-322
	54/74AS2645	– 2	1	5.5	47	J	N	3-282
Octal Transceivers with Open Collector Outputs	54AS621	N/A	48	13	52	J		3-181
	74AS621	N/A	64	13	52		N	3-181
	54AS641	N/A	48	11	42	J		3-189
	74AS641	N/A	64	11	42		N	3-189
Octal Inverter Transceivers with Open Collector Outputs	54AS622	N/A	48	13	27	J		3-181
	74AS622	N/A	64	13	27		N	3-181
	54AS642	N/A	48	12	28	J		3-189
	74AS642	N/A	64	12	28		N	3-189

*Request Data Sheet

Buffer Gates with Open-Collector Outputs

Description	Device Type	High-Level Output Voltage (V)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Octal Transceivers with Open-Collector Outputs	54ALS621	5.5	12	23	16.9	J		2-222
	74ALS621	5.5	24	23	16.9		N	2-222
	54ALS641	5.5	12	17.5	18.1	J		*
	74ALS641	5.5	24	17.5	18.1		N	*
	54ALS1621	5.5	8	18	8.4	J		2-312
	74ALS1621	5.5	16	18	8.4		N	2-312
	54ALS1641	5.5	8	18	14.4	J		2-326
	74ALS1641	5.5	16	18	14.4		N	2-326
Octal Inverter Transceivers with Open-Collector Outputs	54ALS622	5.5	12	22	7.8	J		2-222
	74ALS622	5.5	24	22	7.8		N	2-222
	54ALS642	5.5	12	20	6.6	J		*
	74ALS642	5.5	24	20	6.6		N	*
	54ALS1622	5.5	8	19	9.7	J		2-312
	74ALS1622	5.5	16	19	9.7		N	2-312
	54ALS1642	5.5	8	19	12.5	J		2-326
	74ALS1642	5.5	16	19	12.5		N	2-326
Octal Transceivers with True and Inverting Open-Collector Outputs	54ALS644	5.5	12	19.8	12.8	J		*
	74ALS644	5.5	24	19.8	12.8		N	*
	54ALS1644	5.5	8	23	13.8	J		2-326
	74ALS1644	5.5	16	23	13.8		N	2-326

Buffer Gates with TRI-STATE and Open Collector Outputs

Description	Device Type	High-Level Output Voltage (V)	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
							Mil	Com	
Octal Transceivers	54ALS639	5.5	– 12	12	10	18.3	J		*
	74ALS639	5.5	– 15	24	10	18.3		N	*
	54AS639	5.5	– 12	48	7	44	J		3-186
	74AS639	5.5	– 15	64	7	44		N	3-186
	54ALS1639	5.5	– 12	8	14	14.4	J		2-318
	74ALS1639	5.5	– 15	16	14	14.4		N	2-318
Octal Inverter Transceivers	54ALS638	5.5	– 12	12	10	12.3	J		*
	74ALS638	5.5	– 15	24	10	12.3		N	*
	54AS638	5.5	– 12	48	5.1	28.3	J		3-186
	74AS638	5.5	– 15	64	5.1	28.3		N	3-186
	54ALS1638	5.5	– 12	8	13.5	14.4	J		2-318
	74ALS1638	5.5	– 15	16	13.5	14.4		N	2-318

*Request Data Sheet

Code Converters

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Avail.		Page
				Mil	Com	
6-Bit Binary to 6-Bit BCD Converters	54/74185A 8899	25 31	280 350	J,W	N N	6-253 6-381
6-Bit BCD to 6-Bit Binary or 4-Line to 4-Line BCD 9's/BCD 10's Converters	54/74184 8898	25 31	280 350	J,W	N N	6-253 6-381

Comparators

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Avail.		Page
				Mil	Com	
4-Bit Magnitude Comparator	54/74LS85 54/7485 54/74L85 72/8200	20 21 70 20	52 275 20 175	J,W J,W J,W J,W	N N N N	4-97 6-117 7-54 6-334
6-Bit Magnitude Comparators	71/8131 71/8136 71/8160	20 20 21	250 250 205	J,W J,W J,W	N N N	6-326 6-329 6-332
8-Bit Identity Comparator	54/74ALS520 54/74ALS521	13.5 13.5	60 60	J J	N N	2-188 2-188
8-Bit Identity Comparator with Open-Collector Outputs	54/74ALS518 54/74ALS519 54/74ALS522 54/74ALS689	18.2 18 19 11	55 55 45 60	J J J J	N N N N	2-188 2-188 2-188 2-238
10-Bit Magnitude Comparators	71/8130	21	240	J,W	N	6-324
12-Bit Address Comparator	54/74ALS679 54/74ALS680	18 18	85 67	J J	N N	2-233 2-267
16-Bit Address Comparator	54/74ALS677 54/74ALS678	22 18	105 85	J J	N N	2-228 2-228

Counters, Asynchronous (Ripple Clock)/Negative-Edge-Triggered

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Avail.		Page
						Mil	Com	
4-Bit Binary	54/74LS93	32	None	High	39	J,W	N	4-104
	54/7493A	32	None	High	160	J,W	N	6-124
	54/74L93	6	None	High	20	J,W	N	7-60
	54/74177	35	Yes	Low	150	J,W	N	6-233
	54/74LS197	30	Yes	Low	60	J,W	N	4-242
	54/74S197	100	Yes	Low	375	J,W	N	5-119
	54/74197	40	Yes	Low	240	J,W	N	6-282
	54/74LS293	32	None	High	45	J,W	N	4-306
Decade	54/74LS90	32	Set-to-9	High	40	J,W	N	4-104
	54/7490A	32	Set-to-9	High	160	J,W	N	6-124
	54/74L90	6	Set-to-9	High	20	J,W	N	7-60
	54/74176	35	Yes	Low	150	J,W	N	6-233
	54/74LS196	30	Yes	Low	60	J,W	N	4-242
	54/74S196	100	Yes	Low	375	J,W	N	5-119
	54/74LS290	32	None	High	45	J,W	N	4-302
Divide by 12	54/74LS92	32	None	High	39	J,W	N	4-104
	54/7492A	32	None	High	160	J,W	N	6-124
Dual 4-Bit Decade	54/74LS390	25	None	High	75	J,W	N	4-341
Dual 4-Bit Binary	54/74LS393	25	None	High	75	J,W	N	4-345

Counters, Synchronous/Positive-Edge-Triggered

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Avail.		Page
						Mil	Com	
4-Bit Binary	54/74ALS161	25	Sync	Async-L	60	J	N	2-103
	54/74AS161		Sync	Async-L	200	J	N	3-70
	54/74LS161A	25	Sync	Async-L	93	J,W	N	4-178
	54/74S161	40	Sync	Async-L	475	J,W	N	5-87
	54/74161A	25	Sync	Async-L	305	J,W	N	6-202
	54/74ALS163	25	Sync	Sync-L	60	J	N	2-103
	54/74AS163		Sync	Sync-L	200	J	N	3-70
	54/74LS163A	25	Sync	Sync-L	93	J,W	N	4-178
	54/74S163	40	Sync	Sync-L	475	J,W	N	5-87
	54/74163A	25	Sync	Sync-L	93	J,W	N	6-202
	75/8556	25	Sync	Sync-L	375	J,W	N	6-366
	93/8316	25	Sync	Async-L	305	J,W	N	6-426
	76L76	6	Sync	Async-L	33	J,W	N	7-121

Counters, Synchronous/Positive-Edge-Triggered (Continued)

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Avail.		Page
						Mil	Com	
4-Bit Binary Up/Down	54/74ALS169	25	Sync	None	75	J	N	2-118
	54/74AS169		Sync	None	230	J	N	3-77
	54/74LS169A	25	Async	None	100	J	N	4-200
	54/74ALS191	25	Async	None	60	J	N	2-126
	54/74LS191	20	Async	None	90	J,W	N	4-221
	54/74191	20	Async	None	325	J,W	N	6-259
	54/74ALS193	25	Async	Async-H	60	J	N	2-134
	54/74LS193	25	Async	Async-H	85	J,W	N	4-227
	54/74193	20	Async	Async-H	325	J,W	N	6-265
	54/74L193	6	Async	Async-H	40	J,W	N	7-82
	75/85L63	6	Async	Async-H	40	J,W	N	7-111
Decade	54/74ALS160	25	Sync	Async-L	60	J	N	2-103
	54/74AS160		Sync	Async-L	200	J	N	3-70
	54/74LS160A	25	Sync	Async-L	93	J,W	N	4-178
	54/74S160	40	Sync	Async-L	475	J,W	N	5-87
	54/74160A	25	Sync	Async-L	305	J,W	N	6-202
	54/74ALS162	25	Sync	Sync-L	60	J	N	2-103
	54/74AS162		Sync	Sync-L	200	J	N	3-70
	54/74LS162A	25	Sync	Sync-L	93	J,W	N	4-178
	54/74S162	40	Sync	Sync-L	475	J,W	N	5-87
	54/74162A	25	Sync	Sync-L	305	J,W	N	6-202
	93/8310	25	Sync	Async-L	305	J,W	N	6-411
	76/86L75	6	Sync	Async-L	33	J,W	N	7-121
Decade Up/Down	54/74ALS168	25	Sync	None	75	J	N	2-118
	54/74AS168		Sync	None	230	J	N	3-77
	54/74LS168A	25	Sync	None	100	J,W	N	4-200
	54/74ALS190	20	Async	None	110	J	N	2-126
	54/74LS190	20	Async	None	100	J,W	N	4-221
	54/74190	20	Async	None	325	J,W	N	6-259
	54/74ALS192	20	Async	Async-H	60	J	N	2-134
	54/74LS192	25	Async	Async-H	85	J,W	N	4-227
	54/74192	20	Async	Async-H	325	J,W	N	6-265
	54/74L192	6	Async	Async-H	40	J,W	N	7-82
	75/85L60	6	Async	Async-H	40	J,W	N	7-111
Modulo-N Divider	75/8520	15	Sync	None	250	J,W	N	6-346

Data Selectors/Multiplexers

Description	Device Type	Type of Output	Data Inver. Output	Typ* Prop. Delay Time (ns)		Typ* Power Diss. Total (mW)	Package Avail.		Page
				Data to Out	From Enable		Mil	Com	
Quad 2 to 1 Line	54/74ALS157	Standard	N/A	4.3	6.3	39	J	N	2-100
	54/74AS157	Standard	N/A	3.5	5.5	95	J	N	3-66
	54/74LS157	Standard	N/A	9	14	49	J,W	N	4-173
	54/74S157	Standard	N/A	5	8	250	J,W	N	5-82
	54/74157	Standard	N/A	9	14	150	J,W	N	6-199
	54/74L157A	Standard	N/A	40	60	15	J,W	N	7-72
	54/74ALS257	TRI-STATE	N/A	4.2	6	33	J	N	2-159
	54/74AS257	TRI-STATE	N/A	3.5	4	83	J	N	3-120
	54/74LS257B	TRI-STATE	N/A	12	12	50	J,W	N	4-283
	54/74S257	TRI-STATE	N/A	5	41	320	J,W	N	5-138
	93/8322	Standard	N/A	9	14	150	J,W	N	6-437
	71/81L22	Standard	N/A	40	60	15	J,W	N	7-94
	71/8123	TRI-STATE	N/A	9.5	N/A	200	J,W	N	6-321
	71/81L23	TRI-STATE	N/A	40	N/A	20	J,W	N	7-94
Quad 2 to 1 Line (Inverting)	54/74ALS158	Standard	4.2	N/A	6.1	11.5	J	N	2-100
	54/74AS158	Standard	2.5	N/A	4	78	J	N	3-66
	54/74LS158	Standard	7	N/A	12	24	J,W	N	4-173
	54/74S158	Standard	4	N/A	7	195	J,W	N	5-82
	54/74ALS258	TRI-STATE	4.2	N/A	6	29.2	J	N	2-159
	54/74AS258	TRI-STATE	3	N/A	4.5	58.5	J	N	3-120
	54/74LS258B	TRI-STATE	12	N/A	12	35	J,W	N	4-283
	54/74S258	TRI-STATE	4	N/A	14	280	J,W	N	5-138
Quad 2 to 1 Line with Storage	54/74LS298	Standard	N/A	20	N/A	65	J,W	N	4-310
Dual 4 to 1 Line	54/74ALS153	Standard	N/A	16.5	14.5	37.5	J	N	2-97
	54/74AS153	Standard	N/A	8.7	7.6	105	J	N	3-63
	54/74LS153	Standard	N/A	14	22	31	J,W	N	4-162
	54/74S153	Standard	N/A	6	9.5	225	J,W	N	5-79
	54/74153	Standard	N/A	10.5	20	170	J,W	N	6-187
	54/74ALS253	TRI-STATE	N/A	8	4.5	35	J	N	2-156
	54/74AS253	TRI-STATE	N/A	5	5.5	116.7	J	N	3-117
	54/74LS253	TRI-STATE	N/A	15	25	38	J,W	N	4-280
	54/74S253	TRI-STATE	N/A	6	12	275	J,W	N	5-135
	54/74253	TRI-STATE	N/A	13.5	20	170	J,W	N	6-302
	93/8309	Standard	12	20	20	135	J,W	N	6-408
Dual 4 to 1 Line (Inverting)	54/74ALS352	Standard	6		4.5	32.5	J	N	2-171
	54/74AS352	Standard	3		4.5	122.5	J	N	3-141
	54/74LS352	Standard	15	N/A	18	31	J,W	N	4-314
	54/74ALS353	TRI-STATE	6	N/A	4.5	37.5	J	N	2-174
	54/74AS353	TRI-STATE	3	N/A	6	130	J	N	3-144
	54/74LS353	TRI-STATE	15	N/A	15	38	J,W	N	4-317

Data Selectors/Multiplexers (Continued)

Description	Device Type	Type of Output	Data Inver. Output	Typ* Prop. Delay Time (ns)		Typ* Power Diss. Total (mW)	Package Avail.		Page
				Data to Out	From Enable		Mil	Com	
8 to 1 Line	54/74ALS151	Standard	9.3	7.8	11	37.5	J	N	2-94
	54/74AS151	Standard	2.8	3.5	5	130	J	N	3-60
	54/74LS151	Standard	11	18	27	30	J,W	N	4-158
	54/74S151	Standard	4.5	8	9	225	J,W	N	5-75
	54/74151A	Standard	8	16	22	145	J,W	N	6-179
	54/74ALS251	TRI-STATE	9.4	7.6	7	47	J	N	2-152
	54/74AS251	TRI-STATE	2.8	3.5	4.5	140	J	N	3-113
	54/74LS251	TRI-STATE	17	21	21	35	J,W	N	4-276
	54/74S251	TRI-STATE	4.5	8	14	275	J,W	N	5-131
	54/74251	TRI-STATE	11	18	17	155	J,W	N	6-298
	93/8312	Standard	9	16	17	135	J,W	N	6-422
16 to 1 Line	54/74150	Standard	11	N/A	18	200	J,W	N	6-179

Decoders/Demultiplexers

Description	Device Type	Type of Output	Typ* Select Time (ns)	Typ* Enable Time (ns)	Typ* Power Diss. Total (mW)	Package Avail.		Page
						Mil	Com	
Dual 2 to 4 Line	54/74LS139	Totem	22	19	34	J,W	N	4-152
	54/74S139	Totem	7.5	6	300	J,W	N	5-68
	54/74LS155	Totem	18	15	30	J,W	N	4-168
	54/74155	Totem	21	16	250	J,W	N	6-194
	54/74LS156	Open-Collector	33	26	31	J,W	N	4-168
	54/74156	Open-Collector	33	18	250	J,W	N	6-194
3 to 8 Line	54/74ALS138	Totem	8.5	9	25	J	N	2-91
	54/74LS138	Totem	22	21	31	J,W	N	4-152
	54/74S138	Totem	8	7	225	J,W	N	5-68
	54/74AS138	Totem	5.4	5.5	80	J	N	3-57
	72/8223	Totem	25	N/A	140	J,W	N	6-341
3 to 8 Line Decoder with Address Register	54/74ALS131	Totem	8.5	10	25	J	N	2-77
	54/74AS131	Totem	5.4	5.5	80	J	N	3-49
3 to 8 Line Decoder with Address Latch	54/74ALS137	Totem	11	10	25	J	N	2-87
	54/74AS137	Totem	7	5.5	80	J	N	3-54
4 to 10 Line BCD to Decimal	54/74LS42	Totem	17	N/A	35	J,W	N	4-55
	54/7442	Totem	17	N/A	140	J,W	N	6-71
	54/74L42A	Totem	67	N/A	15	J,W	N	7-27
	93/8301	Totem	20	N/A	125	J,W	N	6-405
4 to 16 Line	54/74LS154	Totem	23	19	45	J,W	N	4-165
	54/74154	Totem	19.5	17.5	170	J,W	N	6-190
	93/8311	Totem	19.5	17.5	170	J,W	N	6-418
1 of 10 Decoder	93/8301	Totem	19.5	N/A	125	J,W	N	6-405

Decoder/Drivers, Display

Description	Device Type	Output Sink Current (mA)	Off-State Output Voltage (V)	Typ* Power Diss. Total (mW)	Blanking	Package Avail.		Page
						Mil	Com	
BCD to	54/7446A	40	30	320	Ripple	J,W	N	6-77
7-Segment	54LS47	12	15	35	Ripple	J,W		4-58
Decoder/	74LS47	24	15	35	Ripple		N	4-58
Drivers	54/7447A	40	15	320	Ripple	J,W	N	6-77
	54LS48	2	5.5	125	Ripple	J,W		4-58
	74LS48	6	5.5	125	Ripple		N	4-58
	54/7448	6.4	5.5	265	Ripple	J,W	N	6-77
	54LS49	4	5.5	40	Direct	J,W		4-58
	74LS49	8	5.5	40	Direct		N	4-58
	54LS247	12	5.5	35	Ripple	J,W		4-267
	74LS247	24	5.5	35	Ripple		N	4-267
	54LS248	2	5.5	125	Ripple	J,W		4-267
	74LS248	6	5.5	125	Ripple		N	4-267
	54LS249	4	5.5	40	Direct	J,W		4-267
	74LS249	8	5.5	40	Direct		N	4-267
BCD to	54/7442	16	5.5	140	Invalid	J,W	N	6-71
Decimal	54/7445	80	30	215	Invalid	J,W	N	6-74
Decoder/	54/74141	7	60	80	Invalid	J,W	N	6-166
Driver	54/74145	80	15	215	Invalid	J,W	N	6-169
Nixie Driver	54/7441A	7	70	105	None	J,W	N	6-68

Error Detection/Correction

Description	Device Type	Byte-Write	Output	Package Avail.		Page
				Mil	Com	
32-Bit	54/74ALS632	Yes	TRI-STATE	J	N	*
Parallel	54/74ALS633	Yes	Open-Collector	J	N	*
	54/74ALS634	No	TRI-STATE	J	N	*
	54/74ALS635	No	Open-Collector	J	N	*

Flip-Flops, Gated

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF(mW)	Package Avail.		Page
							Mil	Com	
54/7470	Yes	Yes	35	20	0	65	J,W	N	6-95
54/74L71	Yes	Yes	11	0	0	3.8	J,W	N	7-36
54/7472	Yes	Yes	20	20	0	45	J,W	N	6-98
54/74L72	Yes	Yes	20	0	0	3.8	J,W	N	7-39
75/8512	Yes	No	28	15	0	110	J,W	N	6-343
75/8544	No	No	N/A	N/A	N/A	44	J,W	N	6-356
76/8613	No	Yes	30	24	0	73	J,W	N	6-373

*Request Data Sheet

Flip-Flops, Single and Dual J-K Edge Triggered

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF(mW)	Package Avail.		Page
							Mil	Com	
54/74LS73A	Yes	No	45	25	5	10	J,W	N	4-73
54/74LS76A	Yes	Yes	45	20	0	10	J,W	N	4-83
54/74LS78A	Yes	Yes	45	20	0	10	J,W	N	4-90
54/74LS107A	Yes	No	45	20	0	10	J,W	N	4-116
54/74ALS109	Yes	Yes	50	15	0	6	J	N	2-65
54/74AS109	Yes	Yes	125	3	1	28.8	J	N	3-37
54/74LS109A	Yes	Yes	33	25	0	10	J,W	N	4-119
54/74109	Yes	Yes	33	10	6	45	J,W	N	6-145
54/74ALS112	Yes	Yes	40	25	0	6	J	N	2-68
54/74AS112	Yes	Yes	200			95	J	N	3-40
54/74LS112A	Yes	Yes	45	20	0	10	J,W	N	4-122
54/74S112	Yes	Yes	125	6	0	75	J,W	N	5-48
54/74ALS113	No	Yes	40	25	0	6	J	N	2-71
54/74AS113	No	Yes	200			95	J	N	3-43
54/74LS113A	No	Yes	45	20	0	10	J,W	N	4-125
54/74S113	No	Yes	125	6	0	75	J,W	N	5-52
54/74ALS114	Yes	Yes	40	25	0	6	J	N	2-74
54/74AS114	Yes	Yes	175			95	J	N	3-46
54/74LS114A	Yes	Yes	45	20	0	10	J,W	N	4-128
54/74S114	Yes	Yes	125	6	0	75	J,W	N	5-55
90/8024	Yes	Yes	40	15	10	45	J,W	N	6-397

Flip-Flops, Dual D Edge Triggered with Preset and Clear

Device Type	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF(mW)	Package Avail.		Page
					Mil	Com	
54/74ALS74	30	15	0	6	J	N	2-60
54/74AS74	125	2	1	26.3	J	N	3-29
54/74LS74A	33	20	0	10	J,W	N	4-76
54/74S74	110	3	2	75	J,W	N	5-41
54/7474	25	20	5	43	J,W	N	6-104
54/74L74	6	50	15	4	J,W	N	7-45

Flip-Flop, Octal D Edge Triggered with TRI-STATE Outputs

Device Type	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF(mW)	Package Avail.		Page
					Mil	Com	
54/74ALS374	50	10	4	10.8	J	N	2-180
54/74AS374	200	3	3	50.3	J	N	3-150
54/74LS374	50	20	0	15.9	J,W	N	4-332
54/74S374	100	5	2	60.9	J,W	N	5-158
54/74ALS534	50	10	0	10.4	J	N	2-195
54/74AS534	200	3	2	50.3	J	N	3-157
54/74ALS564	50	15	4	8.5	J	N	2-202
54/74ALS574	50	15	4	8.5	J	N	2-209
54/74AS574	200	3	3	50.4	J	N	3-164
54/74AS575	160	3	3	53	J	N	3-167
54/74ALS576	50	15	4	8.5	J	N	2-212
54/74AS576	160	3	3	52.5	J	N	3-170
54/74AS577	160	3	3	50.4	J	N	3-174
54/74ALS874	50	15	4	10.8	J	N	2-259
54/74AS874	160	2.5	1	62.5	J	N	3-236
54/74ALS876	50	15	4	10.8	J	N	2-263
54/74AS876	160	2.5	1	58	J	N	3-240
54/74AS878	160	3	3	62.5	J	N	3-244
54/74AS879	160	3	3	59	J	N	3-248

Flip-Flops, Single and Dual, Pulse Triggered

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF(mW)	Package Avail.		Page
							Mil	Com	
54/7473	No	Yes	35	0	0	50.0	J,W	N	6-101
54/74L73	No	Yes	11	0	0	3.8	J,W	N	7-42
54/7476	Yes	Yes	20	0	0	50.0	J,W	N	6-110
54/74L78	Yes	Yes	11	0	0	3.8	J,W	N	7-51
54/74107	No	Yes	20	0	0	50.0	J,W	N	6-142

Gates, AND with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Dual 4-Input	54/74ALS21	9	2.2	J	N	2-40
	54/74AS21	3.3	12.5	J	N	3-19
	54/74LS21	7.8	4.5	J,W	N	4-37
Triple 3-Input	54/74ALS11	9	2.1	J	N	2-27
	54/74AS11	3.3	12.9	J	N	3-15
	54/74LS11	7.8	4.3	J,W	N	4-23
	54/74S11	4.8	31	J,W	N	5-21
	54/7411	11	18	J,W	N	6-38
	54/74L11	42.5	2	J,W	N	7-19
Quad 2-Input	54/74ALS08	6.5	2.2	J	N	2-21
	54/74AS08	3.3	12.9	J	N	3-11
	54/74LS08	7.8	4.3	J,W	N	4-17
	54/74S08	4.8	31	J,W	N	5-15
	54/7408	15	19	J,W	N	6-32
	54/74L08	45	2	J,W	N	7-15

Gates, AND with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Triple 3-Input	54/74ALS15	17	1.5	J	N	2-36
	54/74LS15	19	4.3	J,W	N	4-33
	54/74S15	6	28	J,W	N	5-23
Quad 2-Input	54/74ALS09	17	2.2	J	N	2-23
	54/74LS09	19	4.3	J,W	N	4-19
	54/74S09	6.5	31	J,W	N	5-17
	54/7409	18.5	19.4	J,W	N	6-34

Gates, AND-OR-INVERT with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
2-Wide 4-Input	54/74LS55	7.5	2.75	J,W	N	4-71
	54/74L55	43	1.5	J,W	N	7-34
Dual 2-Wide 2-Input	54/74LS51	7.5	2.75	J,W	N	4-67
	54/74S51	3.5	28	J,W	N	5-35
	54/7451	10.5	14	J,W	N	6-88
	54/74L51	43	1.5	J,W	N	7-30
4-Wide 4-2-3-2 Input	54/74S64	3.5	29	J,W	N	5-37
4-Wide 2-Input	54/7454	10.5	23	J,W	N	6-93
4-Wide 2-3-3-2 Input	54/74LS54	11	4.5	J,W	N	4-69
	54/74L54	43	1.5	J,W	N	7-32

Gates, AND-OR-INVERT with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
4-Wide 4-2-3-2	54/74S65	5.5	36	J,W	N	5-39

Gates, Expandable

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Dual 2-Wide AND-OR-INVERT Gates	54/7450	10.5	14	J,W	N	6-85
4-Wide AND-OR-INVERT Gates	54/7453	10.5	23	J,W	N	6-90

Gates, NAND and Inverters with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Dual 4-Input NAND Gates	54/74ALS22	19	1.3	J	N	2-42
	54/74LS22	10	2	J,W	N	4-39
	54/74S22	5	17.5	J,W	N	5-27
Triple 3-Input NAND Gates	54/74ALS12	18	1.3	J	N	2-29
	54/74LS12	21	2	J,W	N	4-25
Quad 2-Input NAND Gates	54/74ALS01	17	1.3	J	N	2-11
	54/74LS01	21	2	J,W	N	4-7
	54/7401	32	10	J,W	N	6-18
	54/74L01	41	1	J,W	N	7-5
	54/74ALS03	17	1.3	J	N	2-15
	54/74LS03	22	2	J,W	N	4-11
	54/74S03	7	17.5	J,W	N	5-9
	54/7403	10	22	J,W	N	6-22
	54/74L03	41	1	J,W	N	7-9
	90/8012C	20	11	J,W	N	6-393
Hex Inverters	54/74ALS05	18	1.5	J	N	2-19
	54/74LS05	21	2	J,W	N	4-15
	54/74S05	7	17.5	J,W	N	5-13
	54/7405	22	10	J,W	N	6-26
	54/74L05	46	1.2	J,W	N	7-13

Gates, NAND and Inverters with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Dual 4-Input NAND Gates	54/74ALS20	6.5	1.3	J	N	2-38
	54/74AS20	2	8.7	J	N	3-17
	54/74LS20	8	2	J,W	N	4-35
	54/74S20	4.5	19	J,W	N	5-25
	54/7420	10	10	J,W	N	6-50
	54/74L20	33	1	J,W	N	7-21
	9004C	10	11	J,W	N	6-391
Triple 3-Input NAND Gates	54/74ALS10	7	1.3	J	N	2-25
	54/74AS10	2	14	J	N	3-13
	54/74LS10	8	2	J,W	N	4-21
	54/74S10	4.5	19	J,W	N	5-19
	54/7410	10	10	J,W	N	6-36
	54/74L10	33	1	J,W	N	7-17
	9003C	10	11	J,W	N	6-389
Quad 2-Input NAND Gates	54/74ALS00	3.5	1.25	J	N	2-9
	54/74AS00	2	8	J	N	3-5
	54/74LS00	8	2	J,W	N	4-5
	54/74S00	4.5	19	J,W	N	5-5
	54/7400	10	10	J,W	N	6-16
	54/74L00	33	1	J,W	N	7-3
	9002C	10	11	J,W	N	6-387

Gates, NAND and Inverters with Totem-Pole Outputs (Continued)

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Hex Inverters	54/74ALS04	3.5	1.5	J	N	2-17
	54/74AS04	2	7.1	J	N	3-9
	54/74LS04	8	2	J,W	N	4-13
	54/74S04	4.5	19	J,W	N	5-11
	54/7404	10	10	J,W	N	6-24
	54/74L04	33	1	J,W	N	7-11
	9016C	10	11	J,W	N	6-395
8-Input NAND Gates	54/74ALS30	6.5	1.9	J	N	2-48
	54/74AS30	2	9.8	J	N	3-23
	54/74LS30	10	2.4	J,W	N	4-45
	54/74S30	4.5	19	J,W	N	5-29
	54/7430	10	10	J,W	N	6-58
	54/74L30	33	1	J,W	N	7-25
13-Input NAND Gate	54/74ALS133	7	2	J	N	2-83
	54/74S133	6	19	J,W	N	5-58
Hex Non-Inverter	54/74AS34	4.5	12	J	N	3-27

Gates, NAND with Passive Pull-Ups

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Quad 2-Input	80L06	115	1.8		N	7-89

Gates, Exclusive NOR, OR with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Quad 2-Input Exclusive NOR Gates	54/74LS266	10	18	J,W	N	4-292
	54/74ALS811		9.1	J	N	2-250
	54/74AS811			J	N	3-213
Quad 2-Input Exclusive OR Gates	54/74LS136	18	7.6	J,W	N	4-149
	54/74S136	12	63	J,W	N	5-66
	54/74ALS136			J	N	2-85
	54/74AS136			J	N	3-52

Gates, Exclusive NOR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Quad 2-Input Exclusive NOR Gates	54/74ALS810	N/A	N/A	J	N	2-247
	54/74AS810	N/A	N/A	J	N	3-210

Gates, NOR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Dual 4-Input NOR Gate with Strobe	54/7425	10.5	23	J,W	N	6-52
Triple 3-Input NOR Gates	54/74ALS27	5.5	2.5	J	N	2-44
	54/74AS27	2	12.2	J	N	3-21
	54/74LS27	10	4.5	J,W	N	4-43
	54/7427	8.5	22	J,W	N	6-56
Quad 2-Input NOR Gates	54/74ALS02	5	1.9	J	N	2-13
	54/74AS02	2	10.1	J	N	3-7
	54/74LS02	10	2.75	J,W	N	4-9
	54/74S02	5	29	J,W	N	5-7
	54/7402	10	14	J,W	N	6-20
	54/74L02	33	1.5	J,W	N	7-7

Gates, OR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. /Gate(mW)	Package Avail.		Page
				Mil	Com	
Quad 2-Input OR Gates	54/74ALS32	5.5	2.8	J	N	2-50
	54/74AS32	3.5	14.9	J	N	3-25
	54/74LS32	10	5	J,W	N	4-47
	54/74S32	5	35	J,W	N	5-31
	54/7432	12	24	J,W	N	6-60
Quad 2-Input Exclusive OR Gates	54/74ALS86	7	3.75	J	N	2-63
	54/74AS86			J	N	3-32
	54/74LS86	10	7.5	J,W	N	4-101
	54/74S86	9	62.5	J,W	N	5-45
	54/7486	14	41	J,W	N	6-121
	54/74L86	30	7.5	J,W	N	7-57
	54/74LS386	10	7.5	J,W	N	4-338
Quad Exclusive OR/NOR Gates	54/74S135	8.5	82	J,W	N	5-63

Latches

Description	Device Type	No. of Bits	Clear	Outputs	Typ* Prop. Delay Time (ns)	Typ Power Diss. Total (mW)	Package Avail.		Page
							Mil	Com	
Addressable Latches	54/74LS259	8	Low	Q	17	110	J,W	N	4-289
	54/74259	8	Low	Q	21	150	J,W	N	6-306
	93/8334	8	Low	Q	21	280	J,W	N	6-440
DG (Clocked) Latches	54/74LS75	4	None	Q,$\overline{Q}$	11	32	J,W	N	4-80
	54/7475	4	None	Q,$\overline{Q}$	15	160	J,W	N	6-107
	54/74L75A	4	None	Q,$\overline{Q}$	52	17.5	J,W	N	7-48
	54/74LS77	4	None	Q	10	35	J,W	N	4-87
$\overline{S}$,$\overline{R}$ Latches	54/74LS279	4	None	Q	12	19	J,W	N	4-295
TRI-STATE Counters/ Latches	75/85L52	4	High	Q	95	38	J,W	N	7-104
	75/85L54	4	High	Q	95	38	J,W	N	7-104
Dual 4-Bit Latches	54/74ALS880	4	None	$\overline{Q}$	9	88.3	J	N	2-271
	54/74AS880	4	None	$\overline{Q}$	6	391.5	J	N	3-252

Latches (Continued)

Description	Device Type	No. of Bits	Clear	Outputs	Typ* Prop. Delay Time (ns)	Typ Power Diss. Total (mW)	Package Avail.		Page
							Mil	Com	
Octal Latch	54/74ALS273	8	Low	Q	12	50	J	N	2-163
TRI-STATE Octal Latches	54/74ALS373	8	None	Q	10	70	J	N	2-177
	54/74AS373	8	None	Q	6	300	J	N	3-147
	54/74LS373	8	None	Q	17	120	J,W	N	4-332
	54/74S373	8	None	Q	12	525	J,W	N	5-158
	54/74ALS573	8	None	Q	9	68.3	J	N	2-206
	54/74AS573	8	None	Q	4.5	293	J	N	3-161
	54/74AS845	8	Low	Q	4.3	218	J	N	3-227
TRI-STATE Inverting Octal Latches	54/74ALS533	8	None	$\overline{Q}$	10	75.8	J	N	2-192
	54/74AS533	8	None	$\overline{Q}$	5	328	J	N	3-154
	54/74ALS563	8	None	$\overline{Q}$	13	68.3	J	N	2-199
	54/74ALS580	8	None	$\overline{Q}$	9	68.3	J	N	2-216
	54/74AS580	8	None	$\overline{Q}$	4.5	330	J	N	3-178
	54/74AS846	8	Low	$\overline{Q}$	4.8	222	J	N	3-227
Dual 4-Bit TRI-STATE Latches	54/74ALS873	4	Low	Q	10	68.3	J	N	2-255
	54/74AS873	4	Low	Q	4.5	330	J	N	3-232
							J	N	
9-Bit Bus Interface D Latches with TRI-STATE Outputs	54/74AS843	9	Low	Q	4.3	251	J	N	3-222
9-Bit Inverting Bus Interface D Latches with TRI-STATE Outputs	54/74AS844	9	Low	$\overline{Q}$	4.8	242	J	N	3-222
10-Bit Bus Interface D Latches with TRI-STATE Outputs	54/74AS841	10	Low	Q	4.3	250	J	N	3-218
10-Bit Inverting Bus Interface D Latches with TRI-STATE Outputs	54/74AS842	10	Low	$\overline{Q}$	4.3	260	J	N	3-218

Line Drivers

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Avail.		Page
						Mil	Com	
Dual 4-Input NAND	54/74S140	60	– 40	4	43.8	J	N	5-73
Hex 2-Input NAND	54ALS804	12	– 1	2.7	3.3	J	N	2-241
	74ALS804	24	– 2.6	2.7	3.3	J	N	2-241
	54AS804A	40	– 40	2	7.7	J	N	3-204
	74AS804A	48	– 48	2	7.7	J	N	3-204
Hex 2-Input NOR	54ALS805	12	– 12	3	4.1	J	N	2-243
	74ALS805	24	– 15	3	4.1	J	N	2-243
	54AS805A	40	– 40	1.6	9.6	J	N	3-206
	74AS805A	48	– 48	1.6	9.6	J	N	3-206
Hex 2-Input AND	54ALS808	12	– 12	4.3	4.6	J	N	2-245
	74ALS808	24	– 15	4.3	4.6	J	N	2-245
	54AS808A	40	– 40	3	10.6	J	N	3-208
	74AS808A	48	– 48	3	10.6	J	N	3-208
Hex 2-Input OR	54ALS832	12	– 12	4	5.6	J	N	2-253
	74ALS832	24	– 15	4	5.6	J	N	2-253
	54AS832A	40	– 40	2.50	12.9	J	N	3-216
	74AS832A	48	– 48	2.50	12.9	J	N	3-216

Multipliers

Description	Device Type	Package Avail.		Page
		Mil	Com	
4-Bit by 4-Bit Parallel Binary Multipliers	78/8875A	J,W	N	6-376
	78/8875B	J,W	N	6-376

One Shots, Retriggerable

Description	Device Type	No. of Inputs		Dir. Clear	Output Pulse Range (ns)	Typ* Total Power Diss. (mW)	Package Avail.		Page
		Pos	Neg				Mil	Com	
Single	54/74LS122	2	2	Yes	45 ns-inf.	30	J,W	N	4-131
	96/8601	2	2	Yes	50 ns-inf.	90	J,W	N	6-444
Dual	54/74LS123	1	1	Yes	90 ns-inf.	60	J,W	N	4-135
	54/74123	1	1	Yes	45 ns-inf.	230	J,W	N	6-152
	96/8602	1	1	Yes	72 ns-inf.	195	J,W	N	6-448

One Shots with Schmitt-Trigger Inputs

Description	Device Type	No. of Inputs		Dir. Clear	Output Pulse Range(ns)	Typ* Total Power Diss. (mW)	Package Avail.		Page
		Pos	Neg				Mil	Com	
Single	54/74121	1	2	Yes	40ns-28 s	90	J,W	N	6-148
Dual	54LS221	1	1	Yes	20ns-49 s	65	J,W	N	4-250
	74LS221	1	1		20ns-49 s	23		N	4-250

Parity Generators/Checkers

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. Total(mW)	Package Avail.		Page
				Mil	Com	
8-Bit Odd/Even Parity Generators/ Checkers	54/74180	35	170	J,W	N	6-242
9-Bit Odd/Even Parity Generators/ Checkers	54/74S280	13	335	J,W	N	5-143
	72/8220	34	130	J,W	N	6-337
	54/74AS280	7.3	135	J	N	3-129
9-Bit Parity Generator Checker with Bus Driver Parity I/O Port	54/74AS286	9.3	160	J	N	3-136

Priority Encoders

Description	Device Type	Typ* Prop. Delay Time(ns)	Typ* Power Diss. Total(mW)	Package Avail.		Page
				Mil	Com	
Cascadable Octal Priority Encoders	54/74148	12	190	J,W	N	6-172
	93/8318	12	190	J,W	N	6-433
Full BCD Priority Encoders	54/74147	10	225	J,W	N	6-172

Register Files

Description	Device Type	Typ* Address Time (ns)	Typ* Read Enable Time (ns)	Data Input Rate (MHz)	Typ* Power Diss. Total (mW)	Package Avail.		Page
						Mil	Com	
4 Words of 4 Bits	54/74LS170	27	15	20	125	J,W	N	4-208
	74170	30	15	20	635	J,W	N	6-220
4 Words of 4 Bits with TRI-STATE Outputs	54/74LS670	24	19	20	135	J,W	N	4-357
	75/8542	24	19	30	400	J,W	N	6-352

Registers, Other

Description	Device Type	Typ* Clock Freq. (MHz)	Asyn. Clear	Typ* Power Diss. Total (mW)	Package Avail.		Page
					Mil	Com	
Quad Bus Buffer Registers	75/85L51	15	High	28	J,W	N	7-100
	54/74LS173A	40	High	85	J,W	N	4-212
	54/74173	30	High	250	J,W	N	6-224
Quad D-Type Registers	54/74ALS175	60	Low	47.5	J	N	2-123
	54/74AS175	160	Low	395	J	N	3-82
	54/74LS175	40	Low	55	J,W	N	4-216
	54/74S175	90	Low	300	J,W	N	5-96
	54/74175	40	Low	150	J,W	N	6-228
Quad Multiplexers with Storage	54/74LS298	30	None	65	J,W	N	4-310
	54/74L98	15	None	30	J,W	N	7-69
Hex D-Type Registers	54/74ALS174	60	Low	50	J	N	2-123
	54/74AS174	160	Low	395	J	N	3-82
	54/74LS174	40	Low	80	J,W	N	4-216
	54/74S174	90	Low	450	J,W	N	5-96
	54/74174	40	Low	225	J,W	N	6-228
8-Bit Universal Shift/Storage Registers	54ALS299	30	Low	100	J	N	2-166
	74ALS299	40	Low	100	J	N	2-166
	54/74S299	60	Low	700	J,W	N	5-152
	75/8546	22	None	400	J,W	N	6-359
Octal D-Type Registers	54/74ALS374	50	None	86	J	N	2-180
	54/74AS374	200	None	402	J	N	3-150
	54/74LS374	50	None	128	J	N	4-332
	54/74S374	100	None	487	J,W	N	5-158
	54/74ALS534	50	None	83	J	N	2-195
	54/74AS534	200	None	328	J	N	3-157
	54/74ALS574	40	None	68	J	N	2-209
	54/74AS574	160	None	403	J	N	3-164
	54/74AS575	160	None	383	J	N	3-167
	54/74ALS576	50	None	68	J	N	2-212
	54/74AS576	160	None	420	J	N	3-170
	54/74AS577	160	None	420	J	N	3-174
	54/74ALS874	50	Low	87	J	N	2-259
	54/74AS874	160	Low	500	J	N	3-236
	54/74ALS876	50	None	87	J	N	2-263
	54/74AS876	160	None	500	J	N	3-240
	54/74AS878	160	Low	500	J	N	3-244
	54/74AS879	160	Low	500	J	N	3-248

Registers, Other (Continued)

Description	Device Type	Typ* Clock Freq. (MHz)	Asyn. Clear	Typ* Power Diss. Total (mW)	Package Avail.		Page
					Mil	Com	
8-Bit Dual Rank Shift Register	54/74LS952 54/74LS962	36 36	None None	305 305	J,W J,W	N N	4-361 4-367
Successive Approximation Registers	2502C 2503C 2504C	21 21 21	None None None	325 300 450	J,W J,W J,W	N N N	6-5 6-5 6-5

Registers, Shift

Description	Device Type	No. of Bits	Typ* Shift Freq. (MHz)	Ser. Data Input	Asyn. Clear	Modes				Typ* Power Diss. Total (mW)	Package Avail.		Page
						S-R	S-L	Load	Hold		Mil	Com	
Parallel-In Parallel-Out (Bidirectional)	54/74LS194A	4	25	D	Low	x	x	x	x	75	J,W	N	4-234
	54/74S194	4	90	D	Low	x	x	x	x	450	J,W	N	5-112
	54/74194	4	36	D	Low	x	x	x	x	195	J,W	N	6-274
	54/74AS194	4		D	Low	x	x	x	x	133	J	N	3-97
	54/74198	8	35	D	Low	x	x	x	x	360	J,W	N	6-289
Parallel-In Parallel-Out	54/7495	4	36	D	None	x	x	x	x	195	J,W	N	6-133
	54/74L95	4	14	D	None	x	x	x	x	24	J,W	N	7-66
	54/74AS95	4		D	None	x	x	x	x	130	J	N	3-34
	54/7496	5	15	D	None	x		x		240	J,W	N	6-137
	54/74LS195A	4	39	J-$\overline{K}$	Low	x		x		70	J,W	N	4-238
	54/74S195	4	90	J-$\overline{K}$	Low	x		x		375	J,W	N	5-116
	54/74AS195	4		J-$\overline{K}$	Low	x		x			J	N	3-100
	54/74195	4	39	J-$\overline{K}$	Low	x		x		195	J,W	N	6-278
	54/74199	8	35	J-$\overline{K}$	Low	x		x	x	360	J,W	N	6-289
	93/8300	4	39	J-$\overline{K}$	Low	x		x	x	356	J,W	N	6-401
Parallel-In Serial-Out	76/86L90	8	14	D	None	x		x	x	30	J,W	N	7-125
	54/74LS165	8	30	D	None	x		x	x	125	J,W	N	4-192
	54/74165	8	20	D	None	x		x	x	200	J,W	N	6-212
	54/74L165A	8	14	D	None	x		x	x	30	J,W	N	7-78
	54/74ALS165	8	60	D	None	x		x	x	80	J	N	2-110
	54/74LS166	8	35	D	Low	x		x	x	110	J,W	N	4-196
	54/74166	8	35	D	Low	x		x	x	360	J,W	N	6-216
	54/74ALS166	8	60	D	Low	x		x	x	80	J	N	2-214
Serial-In Parallel-Out	54/74LS164	8	36	Gated D	Low	x				80	J,W	N	4-189
	54/74164	8	36	Gated D	Low	x				175	J,W	N	6-208
	54/74L164A	8	14	Gated D	Low	x				30	J,W	N	7-75
	76/86L70	8	14	Gated D	Low	x				30	J,W	N	7-118

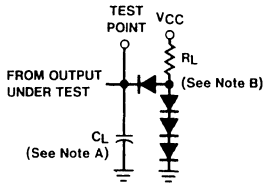
Schmitt-Triggers with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typical* Hysteresis (V)	Package Avail.		Page
				Mil	Com	
Dual 4-Input	54/74LS13	15	0.8	J,W	N	4-27
NAND Schmitt	54/7413	16.5	0.8	J,W	N	6-40
Triggers	54/74ALS13		0.8	J	N	2-31
Quad 2-Input	54/74LS132	15	0.8	J,W	N	4-146
NAND Schmitt	54/74132	15	0.8	J,W	N	6-164
Triggers	54/74ALS132		0.8	J	N	2-80
Hex Schmitt	54/74LS14	15	0.8	J,W	N	4-30
Trigger	54/7414	15	0.8	J,W	N	6-43
Inverters	54/74ALS14		0.8	J	N	2-33

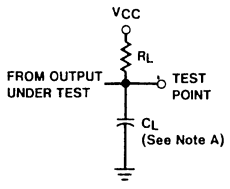
DM54/74, 54S/74S Test Waveforms

Parameter Measurement Information

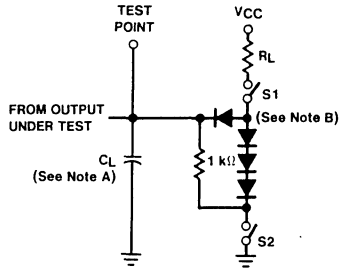
Load Circuit for Bi-State Totem-Pole Outputs



Load Circuit for Open-Collector Outputs

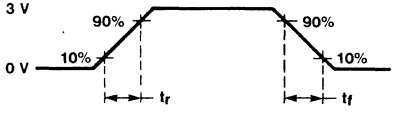


Load Circuit for TRI-STATE Outputs



Note A. C_L includes probe and jig capacitance.
Note B. All diodes are 1N916 or 1N3064.

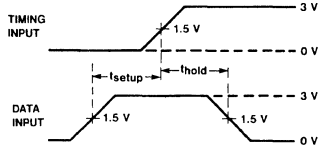
Input Waveform



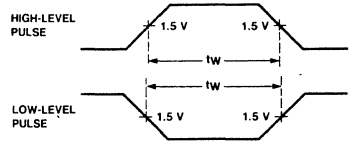
54/74 $t_r \leq 7$ ns, $t_f \leq 7$ ns
54S/74S $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns

Generator: Zout $\approx 50\ \Omega$
PRR $\leq$ 1 MHz

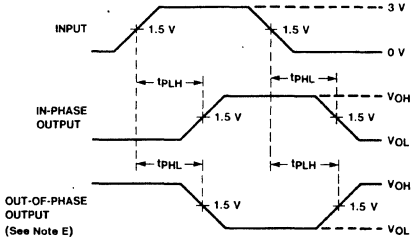
Voltage Waveforms Setup and Hold Times



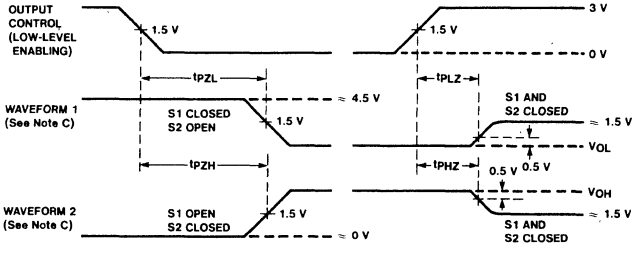
Voltage Waveforms Pulse Widths



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs

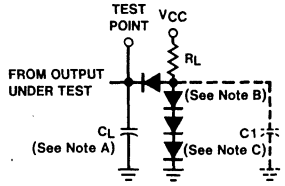


Note C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
Note D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Note E. When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

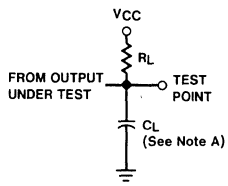
DM54L/74L, 54LS/74LS Test Waveforms

Parameter Measurement Information

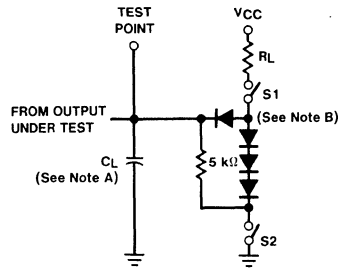
Load Circuit for Bi-State Totem-Pole Outputs



Load Circuit for Open-Collector Outputs

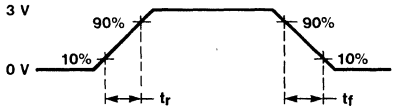


TRI-STATE Outputs



Note A. C_L includes probe and jig capacitance.
Note B. All diodes are 1N916 or 1N3064.
Note C. C1 (30 pF) is used for testing Series 54L/74L devices only.

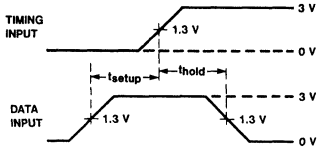
Input Waveform



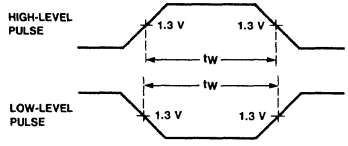
54LS/74LS: $t_r \leq 6$ ns, $t_f \leq 6$ ns
54L/74L gates and inverters: $t_r \leq 60$ ns, $t_f \leq 60$ ns
54L/74L flip-flops and MSI: $t_r \leq 25$ ns, $t_f \leq 25$ ns

Generator: Zout ≈ 50 Ω
PRR ≤ 1 MHz

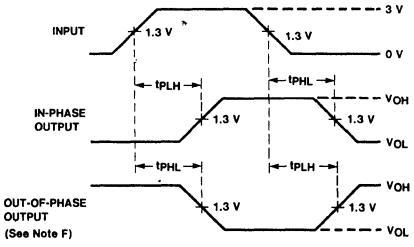
Voltage Waveforms Setup and Hold Times



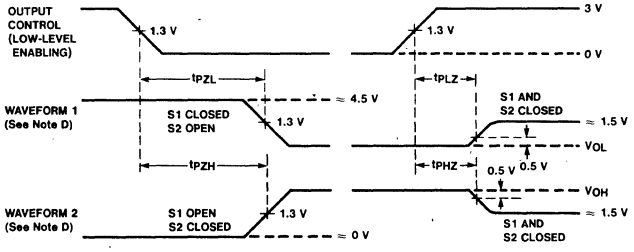
Voltage Waveforms Pulse Widths



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



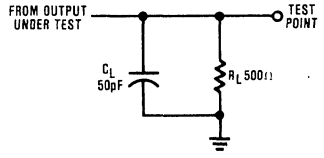
Note D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
Note E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
Note F. When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

Group 1 Test Waveforms DM54ALS/74ALS, 54AS/74AS

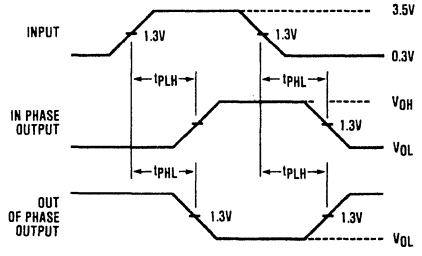
54ALS00, 02, 04, 08, 10, 11, 20, 21, 27, 28, 30, 32, 37, 40, 133, 138, 151, 153, 157, 158, 352, 520, 521, 804, 805, 808, 832, 1000, 1002, 1004, 1008, 1010, 1011, 1020, 1032, 1034

54AS00, 02, 04, 08, 10, 11, 20, 21, 27, 30, 32, 34, 151, 153, 157, 158, 181, 182, 280, 352, 804, 805, 808, 832, 881, 1000, 1002, 1004, 1008, 1010, 1011, 1020, 1032, 1034

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



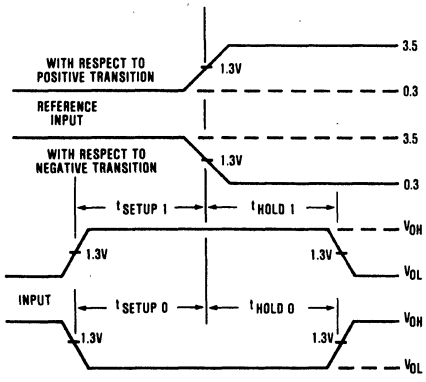
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.

Group 2 Test Waveforms DM54ALS/74ALS, 54AS/74AS

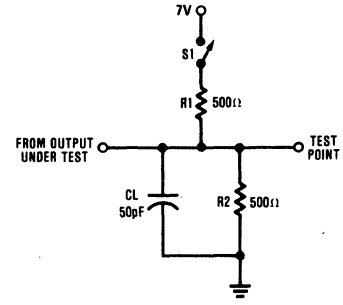
54ALS373, 374, 533, 534, 573, 574, 576, 580, 873, 874, 876, 880

54AS373, 374, 533, 534, 573, 574, 576, 577, 580, 646, 648, 651, 652, 873, 874, 876, 878, 879, 880

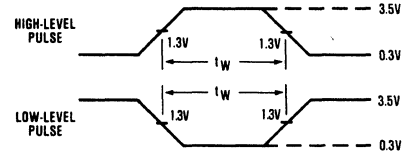
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



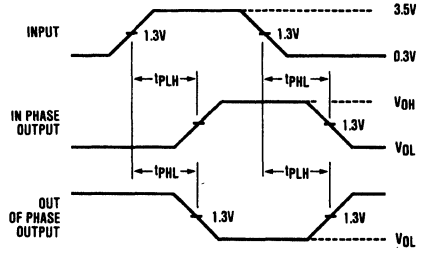
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



VOLTAGE WAVEFORMS PULSE WIDTHS

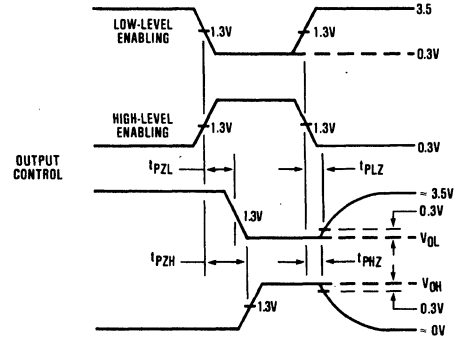


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS



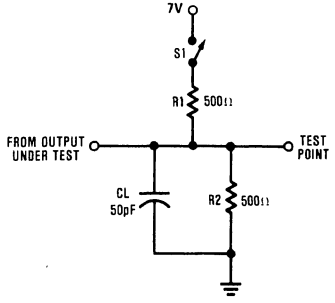
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.

Group 3 Test Waveforms DM54ALS/74ALS, 54AS/74AS

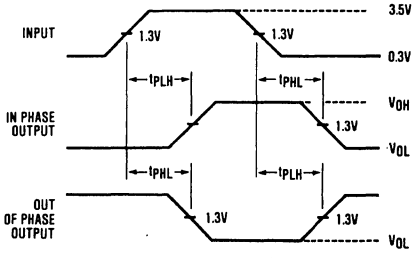
54ALS240, 241, 242, 243, 244, 251, 253, 257, 258, 353, 640, 641, 642, 643, 644, 645, 1240, 1241, 1242, 1243, 1244

54AS230, 231, 240, 241, 242, 243, 244, 245, 251, 253, 257, 258, 353, 640, 641, 642, 643, 644, 645, 1240, 1241, 1242, 1243, 1244

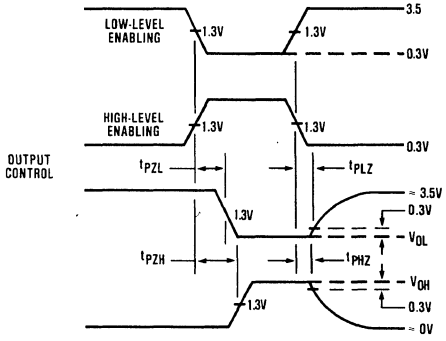
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS



Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED

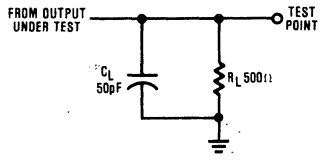
OTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.

Group 4 Test Waveforms DM54ALS/74ALS, 54AS/74AS

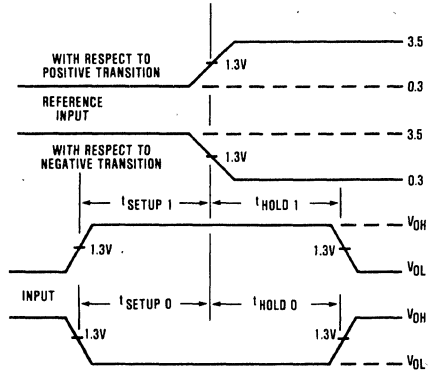
54ALS74, 109, 112, 113, 114, 131, 137, 160, 161, 162, 163, 168, 169, 174, 175, 273

54AS74, 109, 112, 113, 114, 160, 161, 162, 163, 168, 169, 174, 175, 273

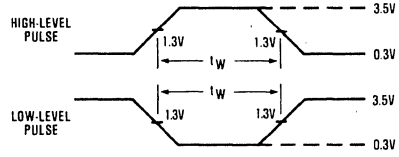
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



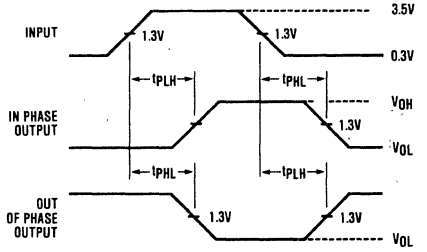
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

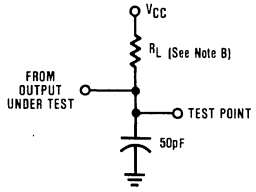


NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.

Group 5 Test Waveforms DM54ALS/74ALS, 54AS/74AS

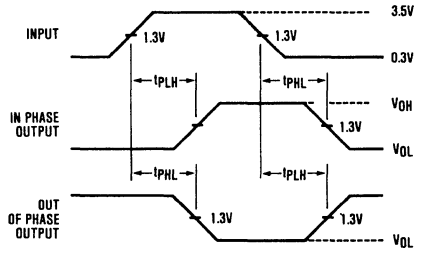
54ALS01, 03, 05, 09, 12, 15, 22, 33, 38, 518, 519, 522, 689, 1003, 1005, 1035

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



NOTES: A. C_L includes probe and jig capacitance
B. R_L = 2KΩ for standard outputs
R_L = 667Ω for buffered outputs

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.

Section 2

Advanced Low Power Schottky

2

Section Contents

Section Contents (Continued)

Section Contents (Continued)

Section Contents (Continued)

National Semiconductor

ADVANCED LOW POWER SCHOTTKY

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (1) 7V
Input Voltage, V_I: All Inputs 7V
I/O Ports 5.5V
Off State (High Level) Voltage Applied to Open-Collector Outputs 7V
High Level Voltage Applied to 3-State Outputs 5.5V
Operating Free-Air Temperature Range:
DM54ALS −55°C to 125°C
DM74ALS 0°C to 70°C
Storage Temperature Range −65°C to 150°C

Recommended Operating Conditions

Parameter		Standard Output			Buffer Output			Bus Driver Output			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	54/74ALS	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	54/74ALS	2			2			2			V
Low Level Input Voltage, V_{IL}	54/74ALS			0.8			0.8			0.8	V
High Level Output Current, I_{OH} (2)	54ALS			−0.4			−1			−12	mA
	74ALS			−0.4			−2.6			−15	mA
High Level Output Voltage, V_{OH} (3)	54/74ALS			5.5			5.5			5.5	V
Low Level Output Current, I_{OL}	54/74ALS			4			12			12	mA
	74ALS			8			24			24/48	mA
Operating Free-Air Temperature, T_A	54ALS	−55		125	−55		125	−55		125	°C
	74ALS	0		70	0		70	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Parameter		Conditions		Standard Output			Buffer Output			Bus Driver Output			Unit
				Min	Typ(4)	Max	Min	Typ(4)	Max	Min	Typ(4)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5			−1.5			−1.5	V
V_{OH}	High Level Output Voltage (2)	V_{CC} = 4.5V, I_{OH} = MAX					2.4	3.2		2	3.2		V
		V_{CC} = 4.5V, I_{OH} = −3mA								2.4	3.2		V
		I_{OH} = −0.4mA		V_{CC}−2V			V_{CC}−2V			V_{CC}−2V			V
I_{OH}	High Level Output Current (3)	V_{CC} = 4.5V V_{OH} = 5.5V				0.1			0.1			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX	74ALS		0.35	0.5		0.35	0.5		0.35	0.5	V
			54/74ALS		0.25	0.4		0.25	0.4		0.25	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V				0.1			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V			−0.02	−0.2		−0.05	−0.2		−0.05	−0.2	mA
I_O	Output Current (5)	V_{CC} = 5.5V V_O = 2.25V		−30		−110	−30		−110	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 2.7V							20			20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 0.4V	I/O Ports						−0.2			−0.2	mA
			Non-I/O						−20			−20	μA
I_{CC}	Supply Current (7)	V_{CC} = 5.5V											mA

NOTE 1: Voltage values are with respect to network ground terminal.
NOTE 2: Does not apply to open-collector outputs.
NOTE 3: Applies only to open-collector outputs.
NOTE 4: All typical numbers are at V_{CC} = 5V, T_A = 25°C.
NOTE 5: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
NOTE 6: Applies only to TRI-STATE outputs.
NOTE 7: Refer to individual data sheet for I_{CC} limits.

National Semiconductor

DM54ALS00A/DM74ALS00A Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

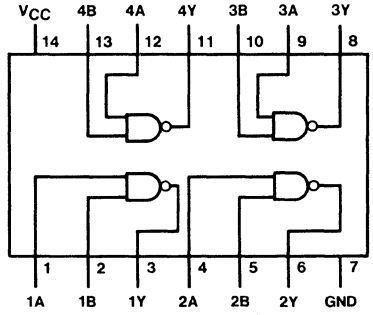
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6270-1

54ALS00A (J) 74ALS00A (J,N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

2

Recommended Operating Conditions

Parameter	DM54ALS00A			DM74ALS00A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS00			DM74ALS00			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		14	3		11	ns
T_{PHL}, Propagation delay time. High to low level output		2		10	2		8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54LS01/DM74LS01 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

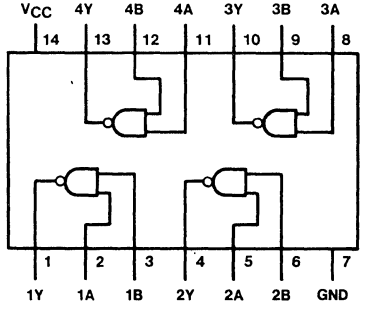
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits, The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6174-1

54ALS01 (J) **74ALS01 (J,N)**

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS01			DM74ALS01			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$ $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS01			DM74ALS01			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	$V_{CC} = 4.5$ to $5.5V$ $R_L = 2K\ \Omega$, $C_L = 50$ pF.	23		59	23		54	ns
T_{PHL}, Propagation delay time. High to low level output		4		29	4		28	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS02/DM74ALS02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

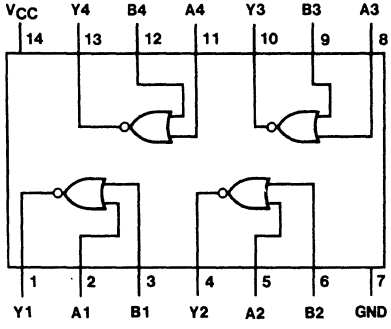
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6175-1

54ALS02 (J) **74ALS02 (J,N)**

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

2

Recommended Operating Conditions

Parameter	DM54ALS02			DM74ALS02			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.85	2.2	mA
			Outputs Low		2.16	4.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS02			DM74ALS02			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		14	3		12	ns
T_{PHL}, Propagation delay time. High to low level output		3		11	3		10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS03A/DM74ALS03A Quad 2-Input NAND Gates with Open Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

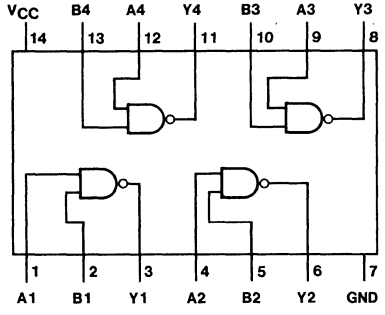
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6176-1

54ALS03A (J) **74ALS03A (J,N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS03A			DM74ALS03A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS03A			DM74ALS03A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 2K Ω, C_L = 50 pF.	23		59	23		54	ns
T_{PHL}, Propagation delay time. High to low level output		5		26	5		22	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS04A/DM74ALS04A Hex Inverters

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

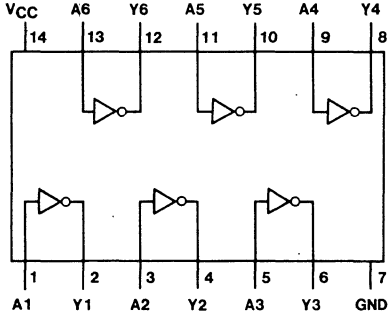
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6177-1

54ALS04A (J) 74ALS04A (J,N)

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS04A			DM74ALS04A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	4.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS04A			DM74ALS04A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		14	3		11	ns
T_{PHL}, Propagation delay time. High to low level output		2		12	2		8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS05A/DM74ALS05A Hex Inverters with Open Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

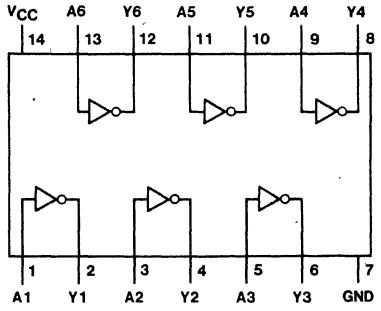
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	7V
Output Voltage	
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6178-1

54ALS05A (J) **74ALS05A (J,N)**

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS05A			DM74ALS05A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	4.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS05A			DM74ALS05A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 2K Ω, C_L = 50 pF.	23		59	23		54	ns
T_{PHL}, Propagation delay time. High to low level output		4		19	4		14	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS08/DM74ALS08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

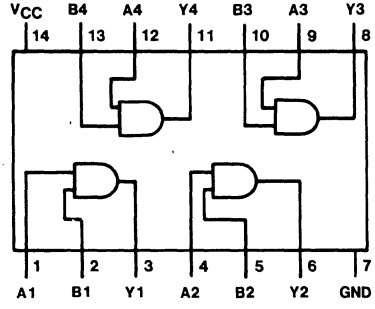
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6271-1

54ALS08 (J) 74ALS08 (J,N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

2

Recommended Operating Conditions

Parameter	DM54ALS08			DM74ALS08			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.3	2.4	mA
			Outputs Low		2.2	4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS08			DM74ALS08			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	4		16	4		14	ns
T_{PHL}, Propagation delay time. High to low level output		3		12	3		10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS09/DM74ALS09 Quad 2-Input AND Gates with Open Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

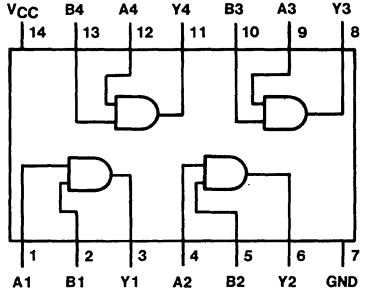
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6179-1

54ALS09 (J) 74ALS09 (J,N)

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS09			DM74ALS09			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.3	2.4	mA
			Outputs Low		2.2	4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS09			DM74ALS09			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 2K Ω, C_L = 50 pF.	23		59	23		54	ns
T_{PHL}, Propagation delay time. High to low level output		5		17	5		15	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS10A/DM74ALS10A Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

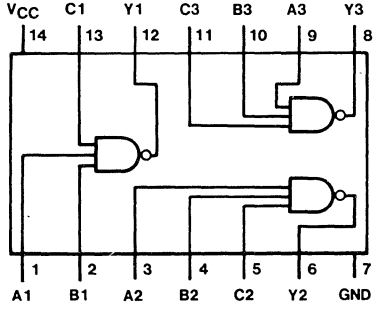
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6180-1

54ALS10A (J) 74ALS10A (J,N)

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS10A			DM74ALS10A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS10A			DM74ALS10A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		3	2	4	11	ns
T_{PHL}, Propagation delay time. High to low level output		2		12	2	6	0	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS11A/DM74ALS11A Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

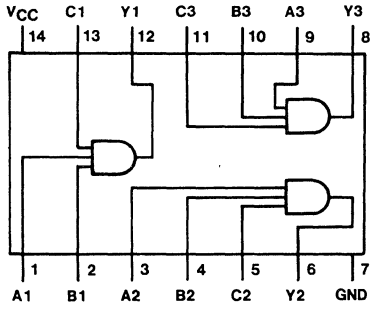
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6181-1

54ALS11A (J) 74ALS11A (J,N)

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS11A			DM74ALS11A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}		V_{CC} = 5.5V	Outputs High		1	1.8	mA
			Outputs Low		1.6	3	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS11A			DM74ALS11A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		16	2		13	ns
T_{PHL}, Propagation delay time. High to low level output		2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS12A/DM74ALS12A Triple 3-Input NAND Gates with Open Collector Outputs

General Description

This device contains three independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

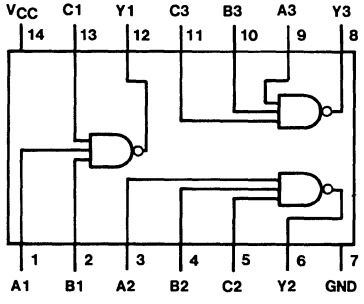
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6182-1

54ALS12A (J) 74ALS12A (J,N)

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS12A			DM74ALS12A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}		$V_{CC} = 5.5V$	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS12A			DM74ALS12A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	$V_{CC} = 4.5$ to $5.5V$, $R_L = 500\ \Omega$, $C_L = 50$ pF.	23		59	23		54	ns
T_{PHL}, Propagation delay time. High to low level output		5		22	5		18	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

PRELIMINARY

DM54ALS13/DM74ALS13 Dual 4-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains two independent gates, each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts

Absolute Maximum Ratings (Note 1)

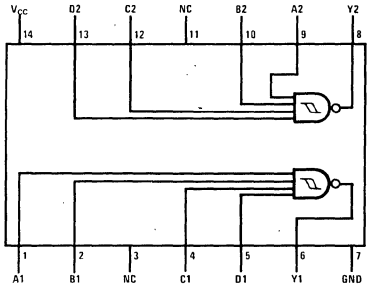
Supply Voltage	7V
Input Voltage	7V
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



DM54ALS13 (J) **DM74ALS13 (N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54ALS13			DM74ALS13			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4		2	1.4		2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.7		1.2	0.8		1.2	V
Hys	Input Hysteresis (Note 1)	0.5			0.5			V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-Min}	DM54	V_{CC} − 2	3.4		V
			DM74	V_{CC} − 2	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+Max}	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			0.03		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			0.034		mA
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				4	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS13			DM74ALS13			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			13			13		ns

Note 1: V_{CC} = 5V.
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

PRELIMINARY

DM54ALS14/DM74ALS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates, each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts

Absolute Maximum Ratings (Note 1)

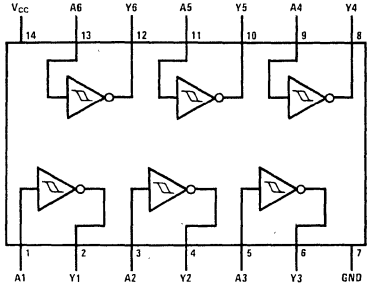
Supply Voltage	7V
Input Voltage	7V
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6183-1

DM54ALS14 (J) **DM74ALS14 (N)**

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = high logic level
L = low logic level

Recommended Operating Conditions

Symbol	Parameter	DM54ALS14			DM74ALS14			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4		2	1.4		2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.7		1.2	0.8		1.2	V
Hys	Input Hysteresis (Note 1)	0.5			0.5			V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	V_{CC} − 2	3.4		V
			DM74	V_{CC} − 2	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			0.03		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			0.034		mA
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				12	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS14			DM74ALS14			Units
			Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2kΩ, C_L = 50 pF		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			8			8		ns

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54ALS15/DM74ALS15 Triple 3-Input AND Gates with Open Collector Outputs

General Description

This device contains three independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

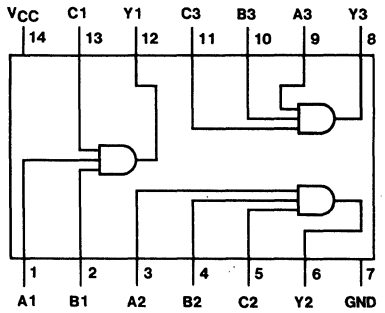
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6183-1

54ALS15 (J) 74ALS15 (J,N)

Function Table

$$Y = ABC$$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS15			DM74ALS15			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		1.0	1.8	mA
			Outputs Low		1.66	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS15			DM74ALS15			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	$V_{CC} = 4.5$ to $5.5V$ $R_L = 2K\ \Omega$, $C_L = 50$ pF.	20		50	20		45	ns
T_{PHL}, Propagation delay time. High to low level output		6		23	6		20	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS20A/DM74ALS20A Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

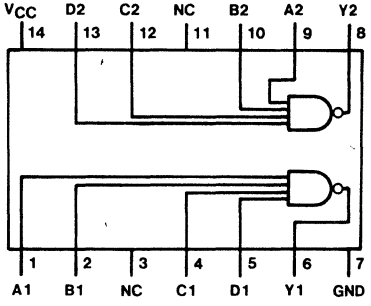
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6184-1

54ALS20A (J) **74ALS20A (J, N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS20A			DM74ALS20A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}		V_{CC} = 5.5V	Outputs High		0.22	0.4	mA
			Outputs Low		0.81	1.5	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS20A			DM74ALS20A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		13	3		11	ns
T_{PHL}, Propagation delay time. High to low level output		3		12	3		10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS21/DM74ALS21 Dual 4-Input AND Gates

General Description

This device contains two independent gates each of which performs the logic AND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

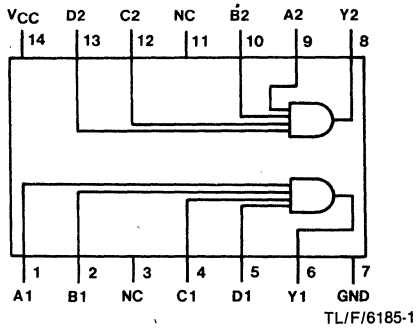
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6185-1

54ALS21 (J) 74ALS21 (J,N)

Function Table

Y = ABCD

Inputs				Output
A	B	C	D	Y
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS21			DM74ALS21			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.67	1.2	mA
			Outputs Low		1.10	2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS21			DM74ALS21			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	6		30	6		26	ns
T_{PHL}, Propagation delay time. High to low level output		3		12	3		10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS22B/DM74ALS22B Dual 4-Input NAND Gates with Open Collector Outputs

General Description

This device contains two independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

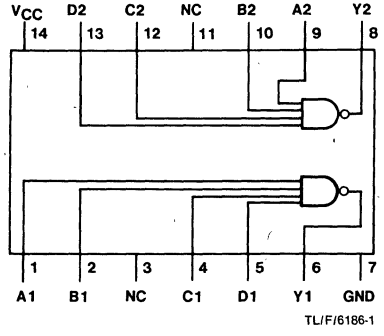
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6186-1

54ALS22B (J) **74ALS22B (J,N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS22B			DM74ALS22B			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.22	0.4	mA
			Outputs Low		0.80	1.5	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS22B			DM74ALS22B			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	$V_{CC} = 4.5$ to $5.5V$, $R_L = 2K\ \Omega$, $C_L = 50$ pF.	23		50	23		45	ns
T_{PHL}, Propagation delay time. High to low level output		4		21	4		18	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS27/DM74ALS27 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

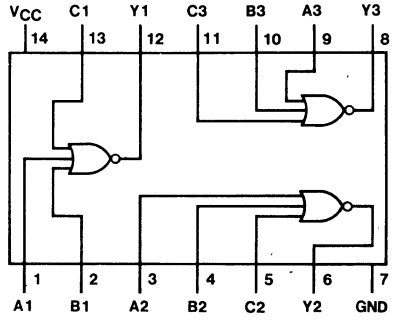
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6187-1

54ALS27 (J) 74ALS27 (J,N)

Function Table

$$Y = \overline{A+B+C}$$

Inputs			Output
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS27			DM74ALS27			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.97	1.8	mA
			Outputs Low		2	4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS27			DM74ALS27			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	4		22	4		15	ns
T_{PHL}, Propagation delay time. High to low level output		3		10	3		9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS28A/DM74ALS28A Quadruple 2-Input NOR Buffers

General Description

This device contains four independent gates each of which performs the logic NOR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS28.
- Improved Line Receiving Characteristics.

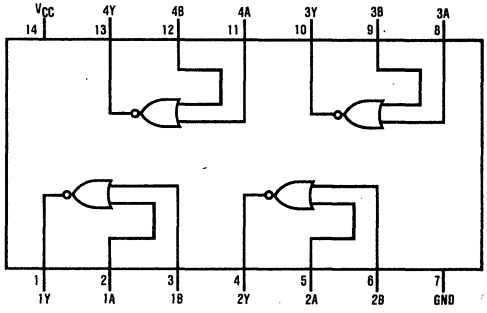
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS28A	−55°C to 125°C
DM74ALS28A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6188-1

54ALS28A (J) **74ALS28A (J,N)**

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS28A			DM74ALS28A			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.8	9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS28A			DM74ALS28A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low level output		2		10	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS30A/DM74ALS30A 8 Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

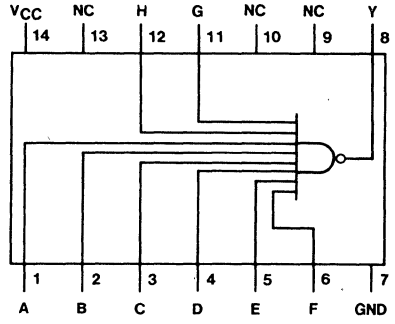
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6189-1

54ALS30A (J) **74ALS30A (J,N)**

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs A thru H	Output Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS30A			DM74ALS30A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.22	0.36	mA
			Outputs Low		0.54	0.90	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS30A			DM74ALS30A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		12	3		10	ns
T_{PHL}, Propagation delay time. High to low level output		3		15	3		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS32/DM74ALS32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

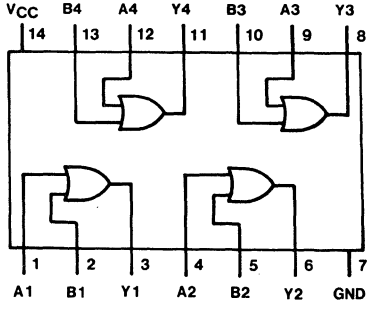
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6190-1

54ALS32 (J) 74ALS32 (J,N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS32			DM74ALS32			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.9	4	mA
			Outputs Low		2.6	4.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS32			DM74ALS32			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		16	3		14	ns
T_{PHL}, Propagation delay time. High to low level output		3		13	3		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS33A/DM74ALS33A Quadruple 2-Input NOR Buffers with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NOR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS33.
- Improved Line Receiving Characteristics.

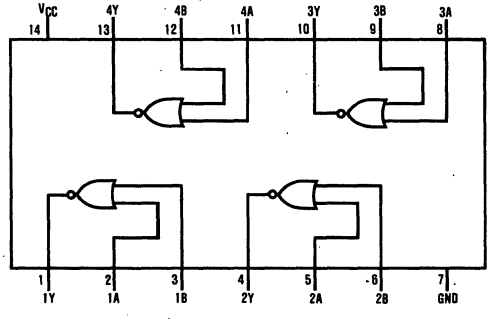
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS33A	−55°C to 125°C
DM74ALS33A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6191-1

54ALS33A (J) **74ALS33A (J, N)**

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS33A			DM74ALS33A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.8	9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS33A			DM74ALS33A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5V to 5.5V R_L = 667 Ω C_L = 50 pF	5		40	5		33	ns
T_{PHL}, Propagation delay time. High to low level output		2		18	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS37A/DM74ALS37A Quadruple 2-Input NAND Buffers

General Description

This device contains four independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS37.
- Improved Line Receiving Characteristics.

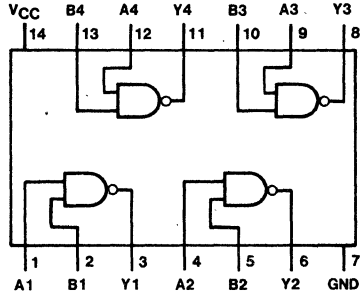
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS37A	−55°C to 125°C
DM74ALS37A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6192-1

54ALS37A (J) 74ALS37A (J,N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS37A			DM74ALS37A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = -2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.0	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS37A			DM74ALS37A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low level output		2		10	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS38A/DM74ALS38A Quadruple 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS38.
- Improved Line Receiving Characteristics.

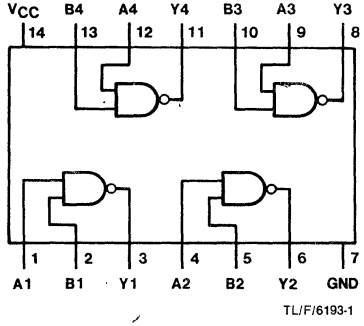
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS38A	−55°C to 125°C
DM74ALS38A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6193-1

54ALS38A (J) 74ALS38A (J,N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS38A			DM74ALS38A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	VCC = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.0	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS38A			DM74ALS38A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 667 Ω, C_L = 50 pF	5		40	5		33	ns
T_{PHL}, Propagation delay time. High to low level output		2		18	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS40A/DM74ALS40A Dual 4-Input NAND Buffers

General Description

This device contains two independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS40.
- Improved Line Receiving Characteristics.

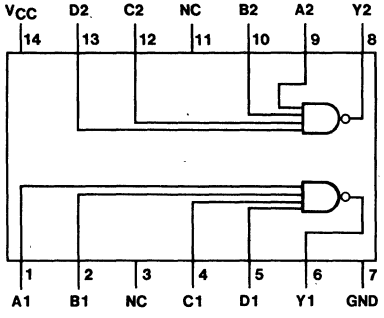
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS40A	−55°C to 125°C
DM74ALS40A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6194-1

54ALS40A (J) 74ALS40A (J,N)

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54ALS40A			DM74ALS40A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Sym	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = -2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.43	0.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			2.4	3.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS40A			DM74ALS40A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low level output		2		10	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS74A/DM74ALS74A Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-For-Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS74 at Approximately Half the Power.

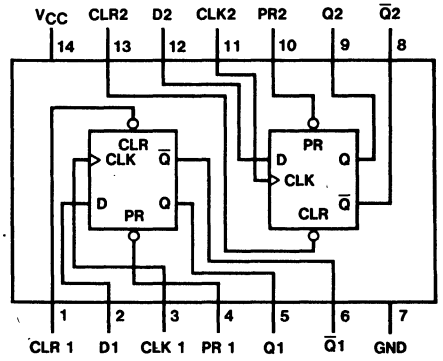
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/L/6109-1

54ALS74A (J) 74ALS74A (J,N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Q_0 = Previous Condition of Q
* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54ALS74A			DM74ALS74A			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock frequency, f_{CLOCK}		0		30	0		34	MHz
Width of Clock Pulse, T_W	High	16.5			14.5			ns
	Low	16.5			14.5			ns
Pulse Width T_W, Preset & Clear	Low	15			15			ns
Data Setup Time, T_{SU}	Data	15↑			15↑			ns
	PRE or CLR Inactive	10↑			10↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage		$I_{OH} = -400\mu A$ $V_{CC} = 4.5$ to 5.5V		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
				74 ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Max High Input Current	Clock, D	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
		Preset, Clear					0.2	mA
I_{IH}	High Level Input Current	Clock, D	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
		Preset, Clear					40	μA
I_{IL}	Low Level Input Current	Clock, D	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
		Preset, Clear					−0.4	mA
I_O	Output Drive Current		$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$			2.4	4	mA

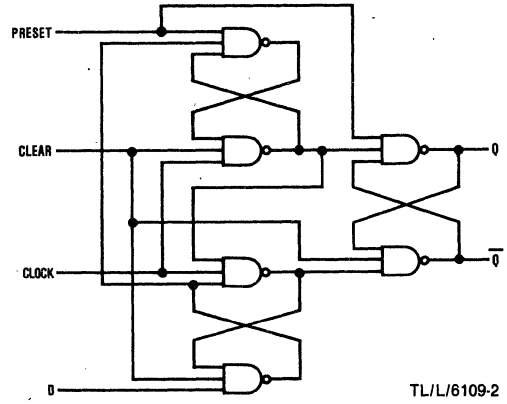
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS74A			DM74ALS74A			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			34			MHz
T_{PLH}	Preset or clear	Q		3		15	3		13	ns
T_{PHL}				5		17	5		15	ns
T_{PLH}	Clock	Q		5		18	5		16	ns
T_{PHL}				5		20	5		18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/L/6109-2

National Semiconductor

DM54ALS86/DM74ALS86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

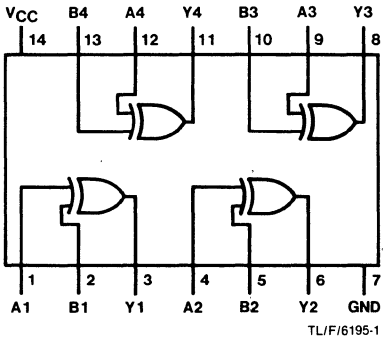
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6195-1

54ALS86 (J) **74ALS86 (J, N)**

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

2

Recommended Operating Conditions

Parameter	DM54ALS86			DM74ALS86			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, All inputs at 4.5V			3.9	5.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions		DM54ALS86			DM74ALS86			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Propagation Delay Time, Low to High Level Output	(Note 2)	A or B to Y	3		22	3		17	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output		Other Input Low	2		14	2		12	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		A or B to Y	3		22	3		17	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output		Other Input High	2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: V_{CC} = 4.5 to 5.5V, R_L = 500Ω, C_L = 50 pF

National Semiconductor

DM54ALS109A/DM74ALS109A Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS109A is a dual edge-triggered flip flop. Each flip flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or $\overline{K}$ is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The J$\overline{K}$ design allows operation as a D flip flop by tying the J and $\overline{K}$ inputs together.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS109 at Approximately Half the Power.

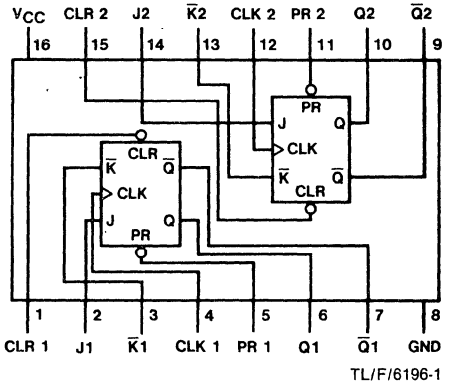
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6196-1

54ALS109A (J) **74ALS109A (J,N)**

Function Table

Inputs					Outputs	
PR	CLR	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition, Q_0 = Previous Condition of Q
* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54ALS109A			DM74ALS109A			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, fCLOCK		0		30	0		34	MHz
Pulse Width T_W	Clock High	16.5			14.5			ns
	Clock Low	16.5			14.5			ns
Pulse Width T_W, Preset & Clear		15			15			ns
Data Setup Time, T_{SU}	J or $\overline{K}$	15↑			15↑			ns
	PRE or CLR inactive	10↑			10↑			
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage		$I_{OH} = -400\mu A$ $V_{CC} = 4.5$ to 5.5V		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
				74ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Input Current Max High	Clock, J, $\overline{K}$	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
		Preset, Clear					0.2	
I_{IH}	High Level Input Current	Clock, J, $\overline{K}$	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
		Preset, Clear					40	
I_{IL}	Low Level Input Current	Clock, J, $\overline{K}$	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
		Preset, Clear					−0.4	
I_O	Output Drive Current		$V_{CC} = 5.5V$ $V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$			2.4	4	mA

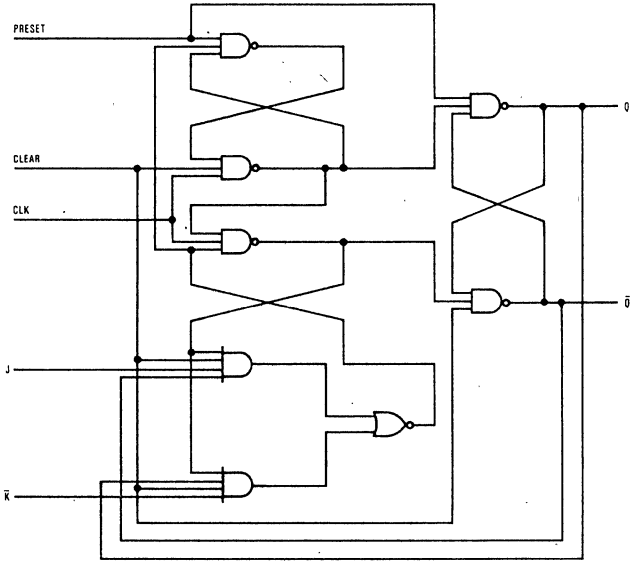
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS109A			DM74ALS109A			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			34			MHz
T_{PLH}	Preset or clear	Q		3		15	3		13	ns
T_{PHL}				5		17	5		15	ns
T_{PLH}	Clock	Q		5		18	5		16	ns
T_{PHL}				5		20	5		18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6196-2

National Semiconductor

DM54ALS112A/DM74ALS112A Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS112A is a dual edge-triggered flip-flop. Each flip flop has individual J, K, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The JK design allows operation as a D flip flop by tying the J and K inputs together.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS112 at Approximately Half the Power.

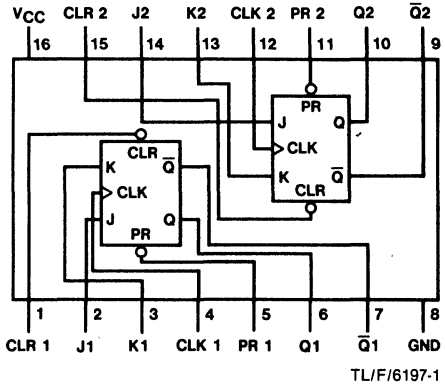
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6197-1

54ALS112A (J) **74ALS112A (J, N)**

Function Table

Inputs					Outputs	
PR	CLR	CK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	H	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↓ = Negative Edge Transition, Q_0 = Previous Condition of Q
* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54ALS112A			DM74ALS112A			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, fCLOCK		0		25	0		30	MHz
Pulse Width T_W	Clock High	20			16.5			ns
	Clock Low	20			16.5			ns
Pulse Width T_W, Preset or Clear Low		15			10			ns
Data Setup Time, T_{SU}	J or K	25↓			22↓			ns
	PRE or CLR inactive	22↓			20↓			
Data Hold Time, T_H		0↓			0↓			ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage		$I_{OH} = -0.4$ mA, $V_{CC} = 4.5$ to 5.5V		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$, $V_{IH} = 2V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
				74ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$	J, K, CLK			0.1	mA
				$\overline{PRE}$ or $\overline{CLR}$			0.2	
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
		Preset, Clear					40	
I_{IL}	Low Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
		Preset, Clear					−0.4	
I_O	Output Drive Current		$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$			2.5	4.5	mA

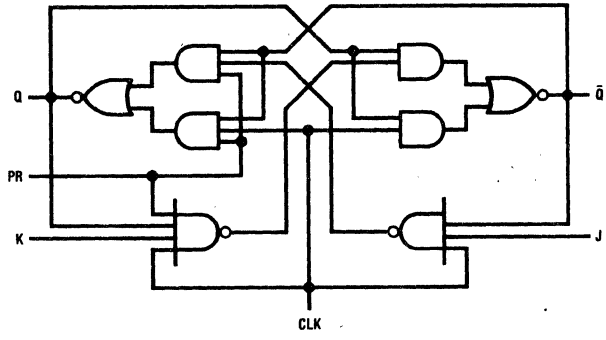
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS112A			DM74ALS112A			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3		20	3		15	ns
T_{PHL}				4		22	4		18	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3		18	3		15	ns
T_{PHL}				5		23	5		19	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6197-2

National Semiconductor

DM54ALS113A/DM74ALS113A Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

General Description

The DM54ALS113A is a dual edge-triggered flip-flop. Each flip-flop has individual J, K, clock, and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset inputs will set Q output upon the application of low level signal.

The JK design allows operation as a D flip-flop by tying the J and K inputs together.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS-TTL Counterpart.
- Improved AC Performance Over LS113 at Approximately Half the Power.

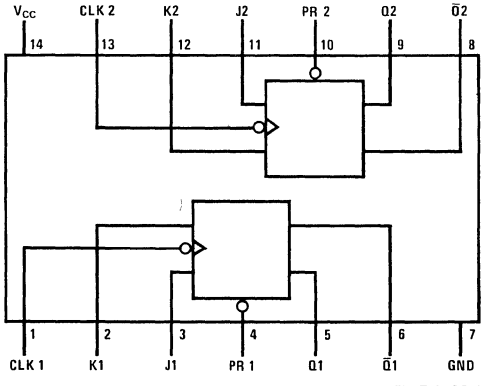
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6198-1

54ALS113A (J) **74ALS113A (J, N)**

Function Table

Inputs				Outputs	
PR	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	H	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↓ = Negative Edge Transition, Q_0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54ALS113A			DM74ALS113A			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, fCLOCK		0		25	0		30	MHz
Pulse Width T_W	Clock High	20			16.5			ns
	Clock Low	20			16.5			ns
Pulse Width T_W, Preset		15			10			ns
Data Setup Time, T_{SU}	J or K	25↓			22↓			ns
	PRE inactive	22↓			20↓			
Data Hold Time, T_H		0↓			0↓			ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage		$I_{OH} = -0.4$ mA $V_{CC} = 4.5$ to 5.5V		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
				74ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$	J, K, CLK			0.1	mA
				$\overline{PRE}$			0.2	
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
		Preset					40	
I_{IL}	Low Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
		Preset					−0.4	
I_O	Output Drive Current		$V_{CC} = 5.5V$ $V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$			2.5	4.5	mA

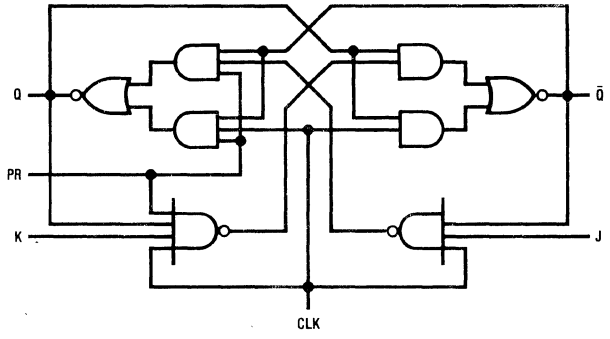
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS113A			DM74ALS113A			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Preset	Q or $\overline{Q}$		3		17	3		14	ns
T_{PHL}				4		20	4		16	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3		18	3		15	ns
T_{PHL}				5		23	5		19	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6198-2

National Semiconductor

DM54ALS114A/DM74ALS114A Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Common Clear

General Description

The DM54ALS114A is a dual edge-triggered flip-flop. Each flip-flop has individual J, K, clock, and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset and common clear inputs will set or clear Q outputs, respectively, upon the application of low level signal.

The JK design allows operation as a D flip-flop by tying the J and K inputs together.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S114 at Approximately Half the Power.

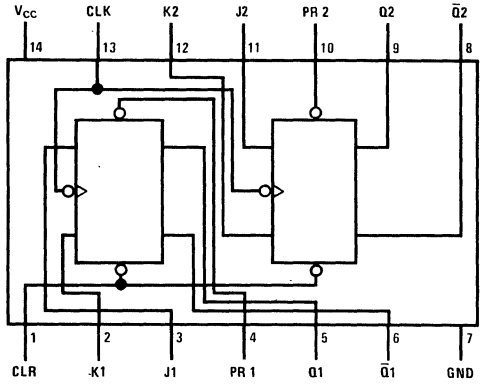
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6199-1

54ALS114A (J) **74ALS114A (J, N)**

Function Table

Inputs					Outputs	
PR	CLR	CK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	H	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↓ = Negative Edge Transition, Q_0 = Previous Condition of Q

* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54ALS114A			DM74ALS114A			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, fCLOCK		0		25	0		30	MHz
Pulse Width T_W	Clock High	20			16.5			ns
	Clock Low	20			16.5			ns
Pulse Width T_W, Preset or Clear Low		15			10			ns
Data Setup Time, T_{SU}	J or K	25↓			22↓			ns
	PRE or CLR inactive	22↓			20↓			
Data Hold Time, T_H		0↓			0↓			ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage		$I_{OH} = -0.4$ mA $V_{CC} = 4.5$ to 5.5V		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
				74ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Max High Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
		Preset, Clear					0.2	
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
		Preset, Clear					40	
I_{IL}	Low Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
		Preset, Clear					−0.4	
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$		−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$			2.5	4.5	mA

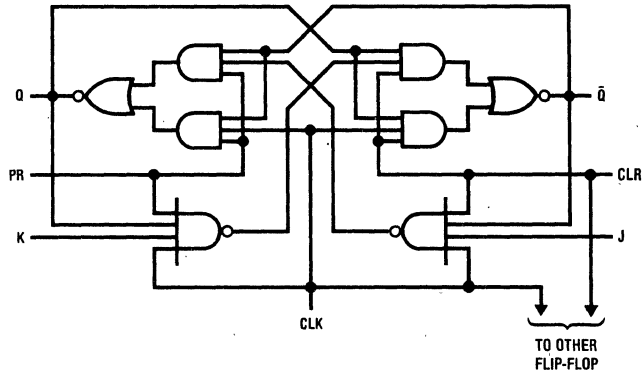
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS114A			DM74ALS114A			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3		20	3		15	ns
T_{PHL}				4		22	4		18	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3		18	3		15	ns
T_{PHL}				5		23	5		19	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6199-2

National Semiconductor

DM54ALS131/DM74ALS131
3-Line to 8-Line Decoder/Demultiplexer with Address Register

General Description

The ALS131 is a three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock transitions from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or clock inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The ALS131 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

Features

- Combines Decoder and 3-Bit Address Register.
- Incorporates 3 Enable Inputs to Simplify Cascading.
- Switching Specification Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

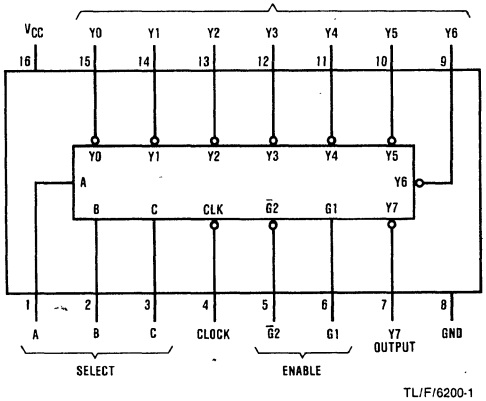
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS131	−55°C to 125°C
DM74ALS131	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6200-1

54ALS131 (J) **74ALS131 (J,N)**

Function Table

Inputs						Outputs							
			Select										
CLK	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	L	H	H	H
↑	H	L	H	H	L	H	H	H	H	H	L	H	H
↑	H	L	H	H	H	H	H	H	H	H	H	L	H
L	H	L	X	X	X	Output corresponding to stored							
H	H	L	X	X	X	address, L; all others, H.							

H = High Level, L = Low Level, X = Don't Care
↑ = Transition from Low to High Level

Recommended Operating Conditions

Parameter		DM54ALS131			DM74ALS131			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, F_{CLOCK}		0		40	0		50	MHz
Width of Clock Pulse, T_W (High or Low)		12.5			10			ns
Setup Time, T_{SU}	A, B, C	15↑			10↑			ns
Hold Time, T_H	A, B, C	0↑			0↑			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4$mA $V_{CC} = 4.5$ to 5.5V		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$mA		0.25	0.4	V
			74ALS $I_{OL} = 8$mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$			5	11	mA

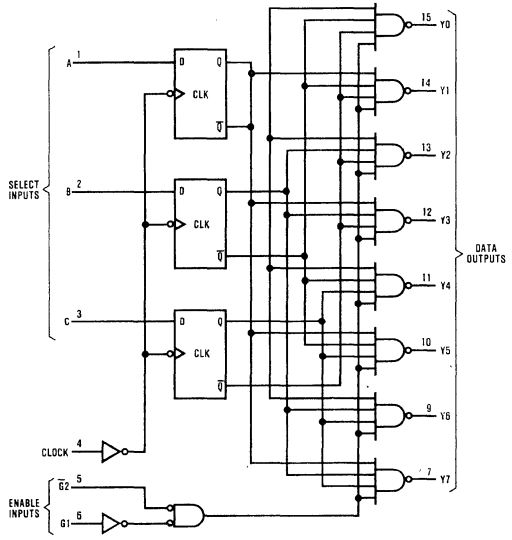
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	Conditions	DM54ALS131			DM74ALS131			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}		V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF	40			50			MHz
T_{PLH}	$\overline{G2}$		5		18	5		15	ns
T_{PHL}			5		18	5		15	
T_{PLH}	G1		7		24	7		20	
T_{PHL}			6		20	6		17	
T_{PLH}	Clock		8		28	8		25	
T_{PHL}			7		24	7		20	

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6200-2

National Semiconductor

PRELIMINARY

DM54ALS132/DM74ALS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts

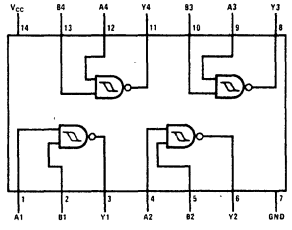
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6707-1

DM54ALS132 (J) **DM74ALS132 (N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high logic level
L = low logic level

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Recommended Operating Conditions

Symbol	Parameter	DM54ALS132			DM74ALS132			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.4		2	1.4		2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.7		1.2	0.8		1.2	V
Hys	Input Hysteresis (Note 2)	0.5			0.5			V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-Min}$	DM54	$V_{CC}-2$	3.4		V
			DM74	$V_{CC}-2$	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_I = V_{T+Max}$	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			0.03		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			0.034		mA
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				8	mA

Note 2: V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	DM54ALS132			DM74ALS132			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		11			11		ns

National Semiconductor

DM54ALS133/DM74ALS133 13-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings (Note 1)

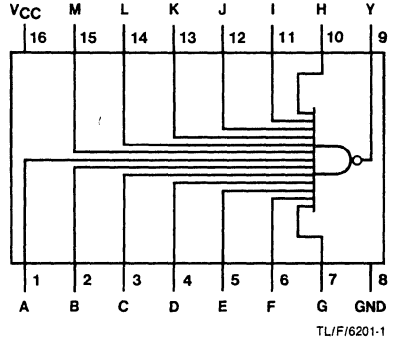
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6201-1

54ALS133 (J) 74ALS133 (J,N)

Function Table

$$Y = \overline{ABCDEFGHIJKLM}$$

Inputs	Output
A thru M	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS133			DM74ALS133			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4mA		0.25	0.4	V
			74 ALS I_{OL} = 8mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.24	0.34	mA
			Outputs Low		0.56	0.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS133			DM74ALS133			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3		14	3		11	ns
T_{PHL}, Propagation delay time. High to low Level Output		5		28	5		25	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS136/DM74ALS136 Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-OR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC(min)} - V_{OH}}{N1\,(I_{OH}) + N2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC(max)} - V_{OL}}{I_{OL} - N3\,(I_{IL})}$$

Where N1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor.

N2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor.

N3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

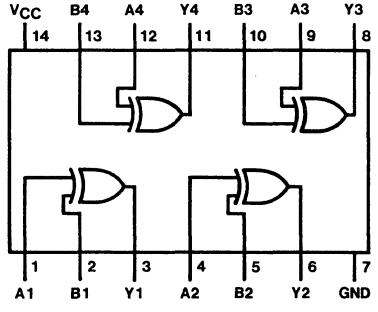
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



DM54ALS136 (J) **DM74ALS136 (N)**

Function Table

$$Y = A \oplus B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high logic level

L = low logic level

Recommended Operating Conditions

Symbol	Parameter	DM54ALS136			DM74ALS136			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54/74ALS		0.25	0.4	V
			DM74ALS		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			3.9	5.9	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS136			DM74ALS136			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF	20		55	20		50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Other Input Low	3		18	3		15	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF	20		55	20		50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Other Input High	3		15	3		12	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: I_{CC} is measured with all inputs at 4.5V and the outputs open.

National Semiconductor

DM54ALS137/DM74ALS137 3-Line to 8-Line Decoder/Demultiplexer with Address Latches

General Description

The ALS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the ALS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from lc to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The ALS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

Features

- Combines Decoder and 3-Bit Address Latch.
- Incorporates 3 Enable Inputs to Simplify Cascading.
- Low Power Dissipation . . . 28 mW Typ.
- Switching Specifications Guaranteed over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

Absolute Maximum Ratings (Note 1)

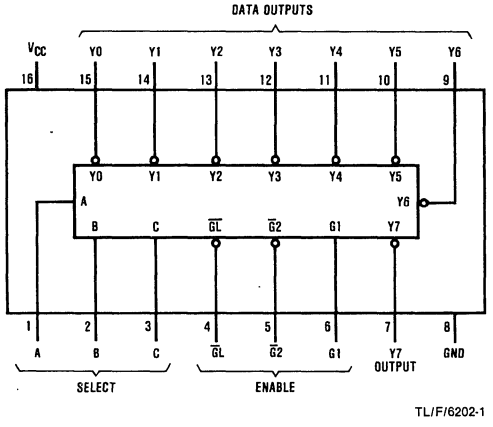
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS137	−55°C to 125°C
DM74ALS137	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6202-1

54ALS137 (J) 74ALS137 (J,N)

Function Table

Inputs						Outputs							
Enable			Select										
GL	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

L = Low State, H = High State, X = Don't Care

Recommended Operating Conditions

Parameter		DM54ALS137			DM74ALS137			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Width of Enabling Pulse, T_W	$\overline{G}$ Low	15			10			ns
Setup Time, T_{SU}	A, B, C	15↑			10↑			ns
Hold Time, T_H	A, B, C	5↑			5↑			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4mA$ $V_{CC} = 4.5$ to $5.5V$		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$	Enable			0.1	mA
			A, B, C			0.1	
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$	Enable			20	μA
			A, B, C			20	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$	Enable			−0.1	mA
			A, B, C			−0.1	
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$			5	11	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

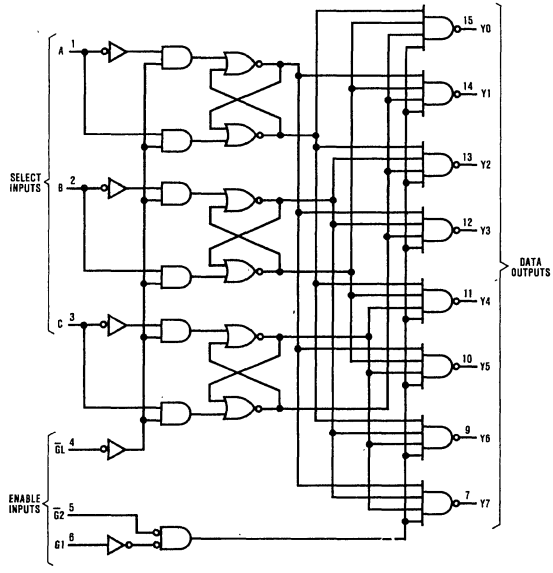
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	Conditions	DM54ALS137			DM74ALS137			Unit
			Min	Typ	Max	Min	Typ	Max	
T_{PLH}	A, B, C	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF.	5		25	5		20	ns
T_{PHL}			6		25	6		20	
T_{PLH}	$\overline{G2}$		4		15	4		12	
T_{PHL}			5		18	5		15	
T_{PLH}	G1		5		21	5		17	
T_{PHL}			5		19	5		15	
T_{PLH}	$\overline{GL}$		7		27	7		22	
T_{PHL}			7		25	7		20	

Note 1: See Section 1 for test waveforms and output load.

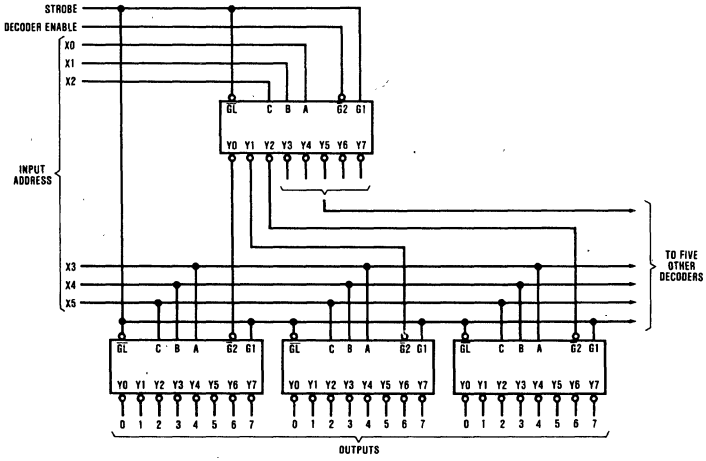
2

Logic Diagrams

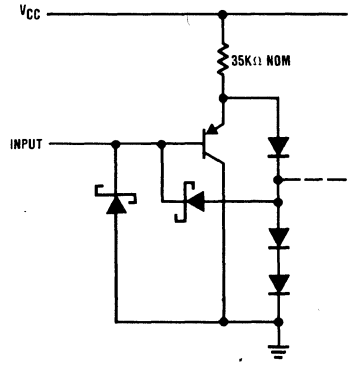


TL/F/6202-2

Logic Diagrams (Continued)



TL/F/6202-3



TL/F/6202-4

National Semiconductor

DM54ALS138/DM74ALS138 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The ALS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

This decoder/demultiplexer features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high-speed:
  Memory decoders
  Data transmission systems
- 3-to-8-line decoder incorporates 3 enable inputs to simplify cascading and/or data reception.
- Low Power Dissipation . . . 23 mW Typ.
- Switching Specification Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

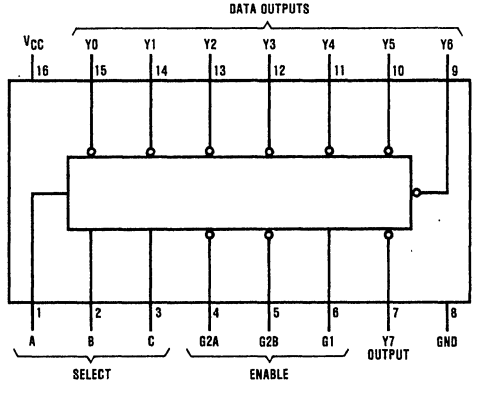
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/L/6111-1

54ALS138 (J) **74ALS138 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS138			DM74ALS138			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4mA$ $V_{CC} = 4.5$ to $5.5V$		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4$ mA		0.25	0.4	V
			74ALS $I_{OL} = 8$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$			5	10	mA

Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

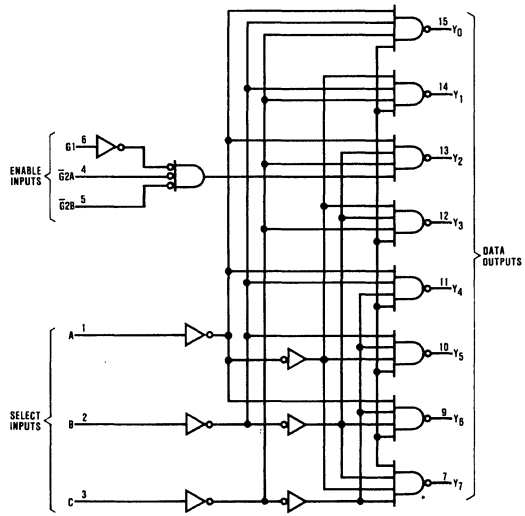
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	Conditions	DM54ALS138			DM74ALS138			Unit
			Min	Typ	Max	Min	Typ	Max	
T_{PLH}	A, B, C	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF.	6		27	6		22	ns
T_{PHL}			6		22	6		18	
T_{PLH}	Enable		4		20	4		17	
T_{PHL}			5		20	5		17	

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/L/6111-2

National Semiconductor

DM54ALS151/DM74ALS151 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. A Strobe input is provided which, when at the high level, disables all data inputs and forces the Y output to the low state and the W output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

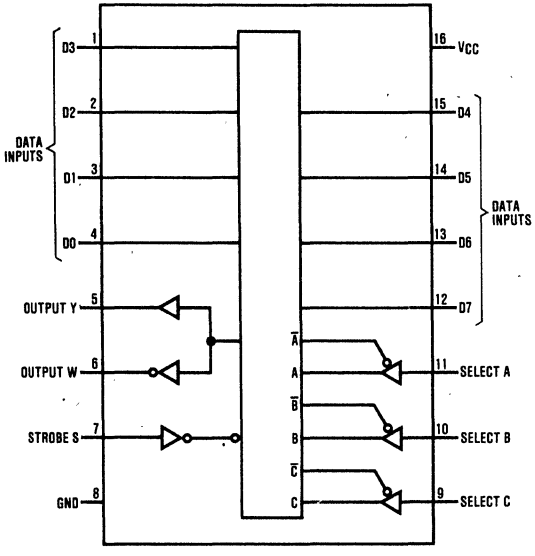
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS151	−55°C to 125°C
DM74ALS151	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6203-1

54ALS151 (J) **74ALS151 (J,N)**

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level L = Low Level X = Don't Care
D0 thru D7 = the level of the respective D input

Recommended Operating Conditions

Parameter	DM54ALS151			DM74ALS151			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 4.5V Select Inputs = 4.5V Strobe Inputs = 4.5V			7.5	12	mA

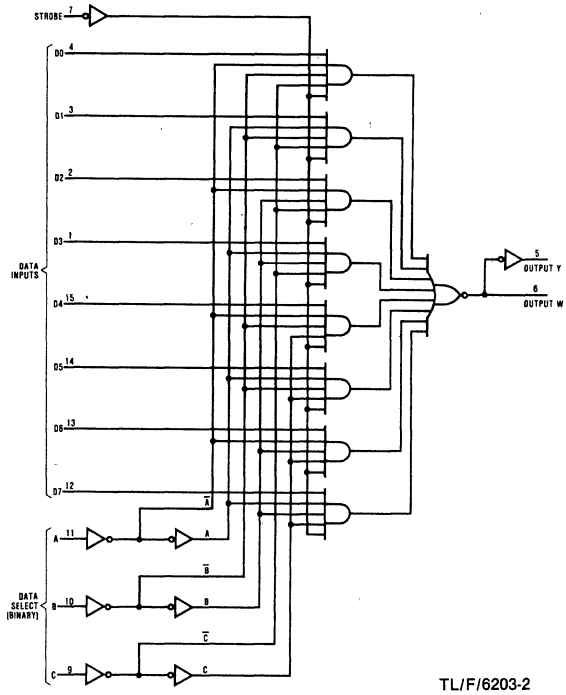
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS151			DM74ALS151			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V C_L = 50 pF R_L = 500 Ω	4		21	4		18	ns
t_{PHL}, High to low Level Output				8		28	8		24	ns
t_{PLH}, Low to high Level Output		W		7		28	7		24	ns
t_{PHL}, High to low Level Output				7		26	7		23	ns
t_{PLH}, Low to high Level Output	Data	Y		3		12	3		10	ns
t_{PHL}, High to low Level Output				5		18	5		15	ns
t_{PLH}, Low to high Level Output		W		3		18	3		15	ns
t_{PHL}, High to low Level Output				4		18	4		15	ns
t_{PLH}, Low to high Level Output	Strobe	Y		4		21	4		18	ns
t_{PHL}, High to low Level Output				4		23	4		19	ns
t_{PLH}, Low to high Level Output		W		5		23	5		19	ns
t_{PHL}, High to low Level Output				5		26	5		23	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6203-2

National Semiconductor

DM54ALS153/DM74ALS153 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and a non-inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the low state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

Absolute Maximum Ratings (Note 1)

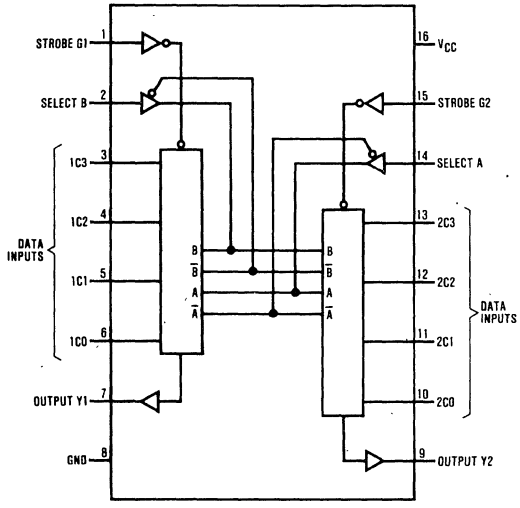
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS153	−55°C to 125°C
DM74ALS153	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6204-1

54ALS153 (J) **74ALS153 (J,N)**

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS153			DM74ALS153			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 4.5V Select Inputs = 4.5V Strobe Inputs = 4.5V			7.5	14	mA

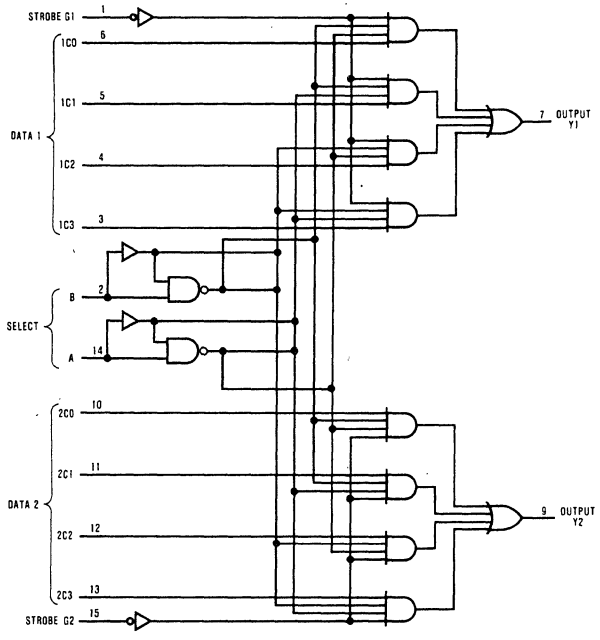
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS153			DM74ALS153			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	5		25	5		21	ns
t_{PHL}, High to low Level Output				5		25	5		21	ns
t_{PLH}, Low to high Level Output	Data	Y		3		12	3		10	ns
t_{PHL}, High to low Level Output				4		18	4		15	ns
t_{PLH}, Low to high Level Output	Strobe	Y		5		22	5		18	ns
t_{PHL}, High to low Level Output				5		22	5		18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6204-2

National Semiconductor

PRELIMINARY

DM54ALS/DM74ALS157,158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The ALS 157 presents true data whereas the ALS 158 presents inverted data to minimize propagation delay time.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

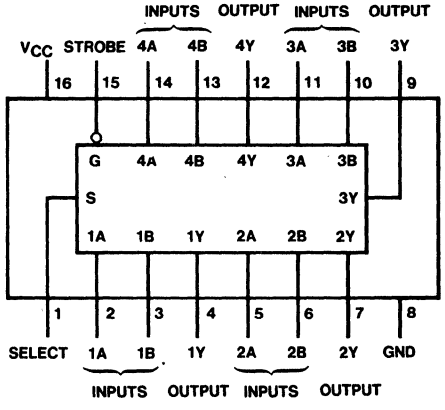
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6205-1

54ALS157 (J) **74ALS157 (J,N)**
54ALS158 (J) **74ALS158 (J,N)**

Function Table

Inputs				Output Y	
Strobe	Select	A	B	ALS157	ALS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS157,158			DM74ALS157,158			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
		I_{OH} = Max		2.4	3.3		
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V	A or B			0.1	mA
			$\overline{A}$/B or $\overline{G}$			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	A or B			20	μA
			$\overline{A}$/B or $\overline{G}$			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	A or B			−0.1	mA
			$\overline{A}$/B or $\overline{G}$			−0.1	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	54/74ALS157		7.8		mA
			54/74ALS158		2.3		mA

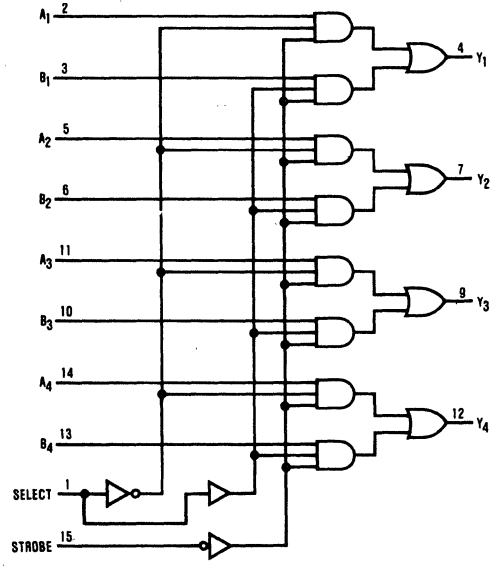
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

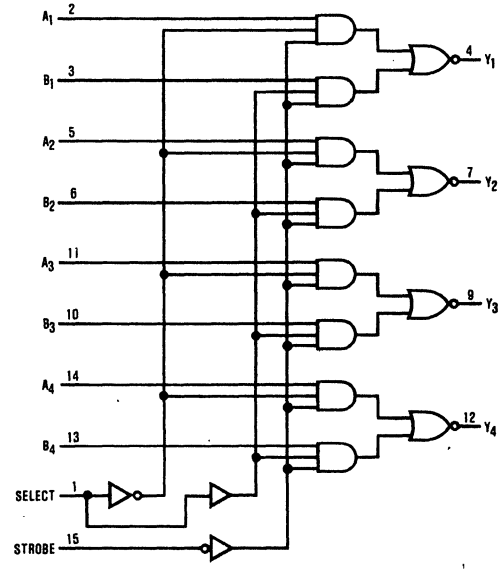
Parameter		From (Input)	To (Output)	Conditions	DM54ALS157,158			DM74ALS157,158			Unit
					Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Data	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω		3.5			3.5		ns
	158					3.5			3.5		
T_{PHL}, Propagation Delay Time. High to Low Level Output	157					5			5		
	158					5			5		
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Strobe	Y			6			6		
	158					6			6		
T_{PHL}, Propagation Delay Time. High to Low Level Output	157					6.5			6.5		
	158					6.5			6.5		
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Select	Y			6			6		
	158					6			6		
T_{PHL}, Propagation Delay Time. High to Low Level Output	157					6.5			6.5		
	158					6.5			6.5		

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams



TL/F/6205-2



TL/F/6205-3

National Semiconductor

DM54ALS/DM74ALS160A, 161A, 162A, 163A Synchronous Four-Bit Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The ALS160A and ALS162A are four-bit decade counters, while the ALS161A and ALS163A are four-bit binary counters. The ALS160A and ALS161A clear asynchronously, while the ALS162A and ALS163A clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outupts to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The ALS160A and ALS161A clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The ALS162A and ALS163A clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the ALS162A and ALS163A are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count enable inputs (P and T) and a ripple carry output. Both count enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the ALS160A through ALS163A may occur regardless of the logic level on the clock.

The ALS160A through ALS163A feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Shottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously programmable.
- Internal look ahead for fast counting.
- Carry output for n-bit cascading.
- Synchronous counting.
- Load control line.
- ESD inputs.

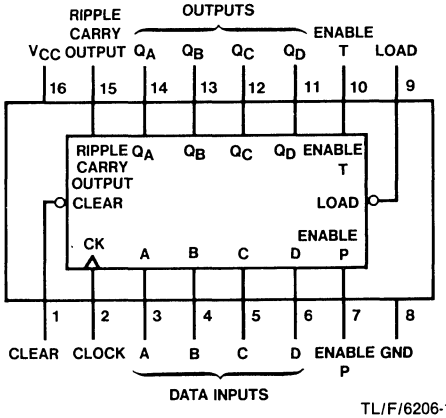
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6206-1

54ALS160A (J) **74ALS160A (J,N)**
54ALS161A (J) **74ALS161A (J,N)**
54ALS162A (J) **74ALS162A (J,N)**
54ALS163A (J) **74ALS163A (J,N)**

Recommended Operating Conditions

Parameter			DM54ALS 160A, 161A, 162A, 163A			DM74ALS 160A, 161A, 162A, 163A			Unit
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}			2			2			V
Low Level Input Voltage, V_{IL}					0.8			0.8	V
High Level Output Current, I_{OH}					−0.4			−0.4	mA
Low Level Output Current, I_{OL}					4			8	mA
Clock Frequency, f_{CLOCK}			0		25	0		30	MHz
t_{SETUP}, Set-Up Time	Data; A, B, C, D		20↑			15↑			ns
	En P, En T	ALS160A/161A	25↑			20↑			ns
		ALS162A/163A	30↑			25↑			ns
	Load		20↑			15↑			ns
	$\overline{\text{Clear}}$ (Only for 162A and 163A)	Low	20↑			15↑			ns
		High	10↑			10↑			ns
Set-Up 1 (Only for 160A and 161A)	$\overline{\text{Clear}}$ Inactive		10	4		10	4		ns
t_{HOLD}, Hold Time	Data; A, B, C, D		0↑	−3		0↑	−3		ns
	En P, En T		0↑	−3		0↑	−3		ns
	Load		0↑	−4		0↑	−4		ns
	Clear (Only for 162A and 163A)		0↑	−7		0↑	−7		ns
Hold 0 (Only for 160A and 161A)	Clear		0	−4		0	−4		ns
Width of Clock or Clear Pulse, t_W	CLK High or Low		20			16.5			ns
	ALS160A/161A CLR Low		20			15			ns
Width of Load Pulse			20			15			ns

Note 1: The symbol (↑) indicates that the rising edge of the clock is used as reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4mA$ $V_{CC} = 4.5$ to $5.5V$		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 4mA$		0.25	0.4	V
			74ALS $I_{OL} = 8mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$	LOAD, CLK ENT			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$ $V_{IH} = 2.7V$	DATA, CLR, EN P			20	μA
			CLK, LOAD, EN T			40	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$	DATA, CLR, CLK, EN P			−0.1	mA
			LOAD, ENT			−0.2	
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$			12	21	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS 160A, 161A, 162A, 163A			DM74ALS 160A, 161A, 162A, 163A			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			$V_{CC} = 4.5$ to $5.5V$ $R_L = 500\ \Omega$ $C_L = 50$ pF	25			30			MHZ
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Ripple Carry		8		30	8		26	ns
T_{PHL}, Propagation delay time. High to low level output.				7		25	7		23	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		4		18	4		15	ns
T_{PHL}, Propagation delay time. High to low level output.				6		20	6		17	ns
T_{PLH}, Propagation delay time. Low to high level output. (Only for 160A, 161A)	En T	Ripple Carry		3		16	3		13	ns
T_{PLH}, Propagation delay time. Low to high level output. (Only for 162A, 163A)				3		20	3		17	ns

Switching Characteristics (Continued) over recommended operating free air temperature range (Note 1).

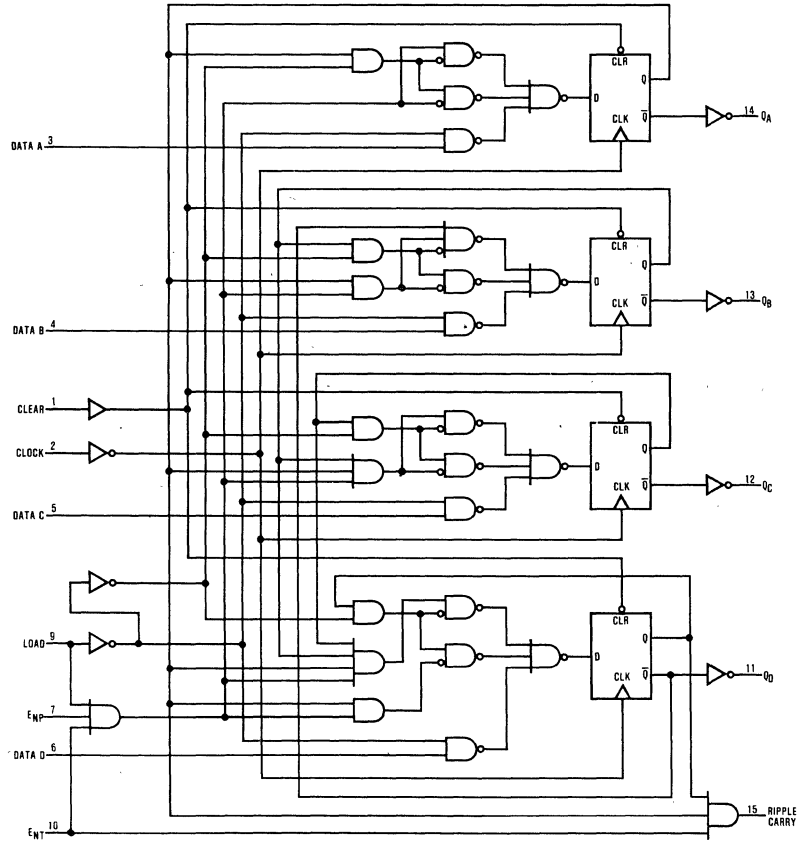
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS 160A, 161A, 162A, 163A			DM74ALS 160A, 161A, 162A, 163A			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PHL}, Propagation delay time. Low to high level output.	En T	Ripple Carry		3		16	3		13	ns
T_{PHL}, Propagation delay time. High to low level output. (Only for 160A, 161A)	Clear	Any Q		8		27	8		24	ns
		Ripple Carry		11		31	11		28	

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

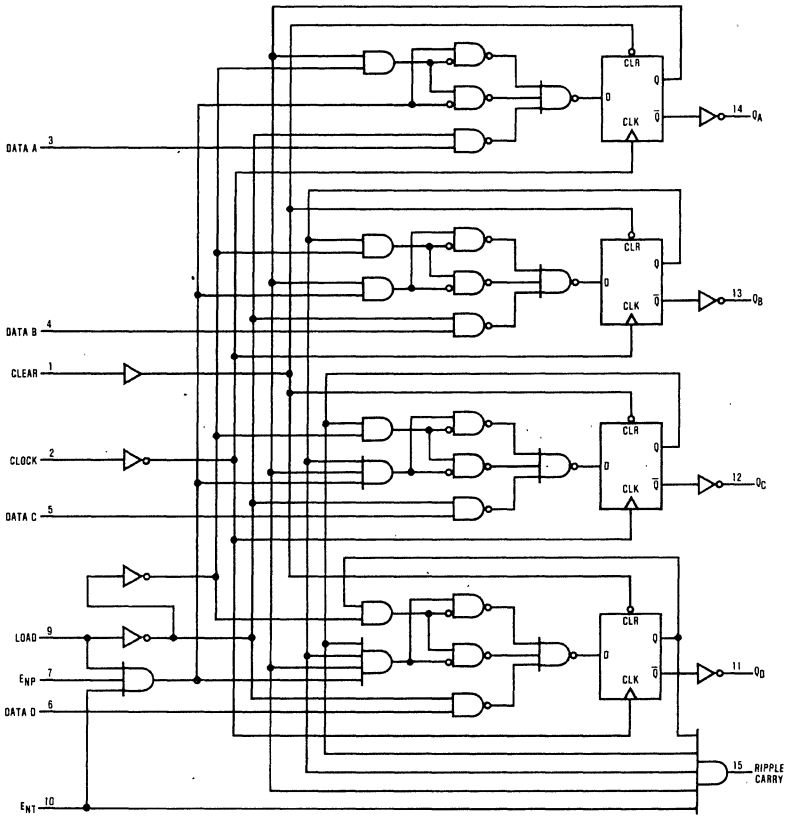
ALS160A



TL/F/6206-2

Logic Diagrams (Continued)

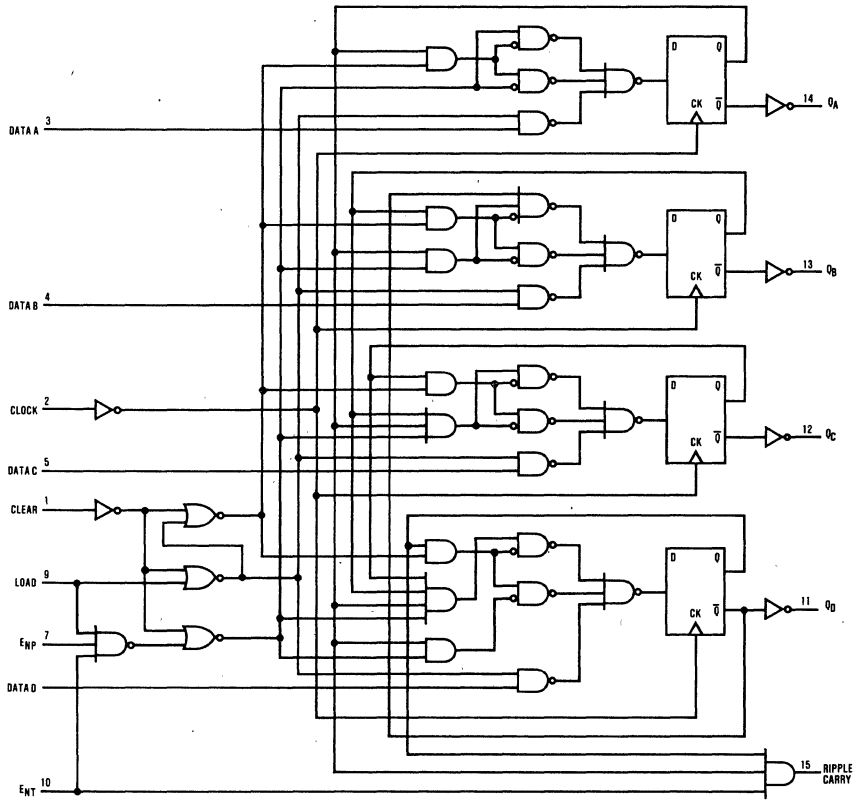
ALS161A



TL/F/6206-3

Logic Diagrams (Continued)

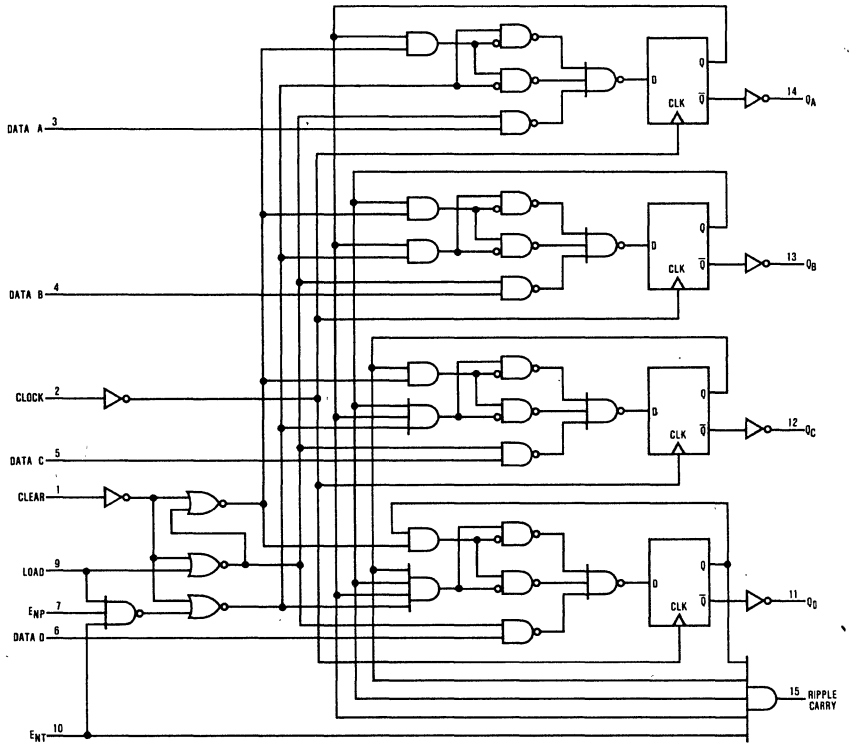
ALS162A



TL/F/6206-4

Logic Diagrams (Continued)

ALS163A



TL/F/6206-5

National Semiconductor

PRELIMINARY

DM54ALS165/DM74ALS165 8-Bit Parallel In/Serial Out Shift Register

General Description

The DM54/74ALS165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output, $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The DM54/74ALS165 also features a clock inhibit function and a complemented serial output, $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

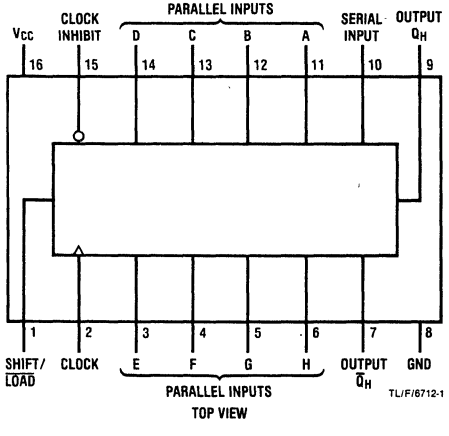
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

DM54ALS165 (J) DM74ALS165 (N)

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	L	H	X	H	Q_{An}	Q_{Gn}
H	↑	L	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady-state), L = low level (steady-state).

X = don't care (any input, including transitions).

↑ = transition from low-to-high level.

a...h = the level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Recommended Operating Conditions

Symbol	Parameter		DM54ALS165			DM74ALS165			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLOCK}	Clock Frequency								MHz
t_W	Pulse Duration	CLK High							ns
		CLK Low							
t_{SU}	Set-Up Time	SH/$\overline{LD}$							ns
		Data							
t_H	Hold Time								ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

Parameter	Conditions	DM54ALS165			DM74ALS165			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5V, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = 5.5V, V_I = 0.4V			−0.1			−0.1	mA
I_O (Note 2)	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5V (Note 3)		16			16		mA

Switching Characteristics

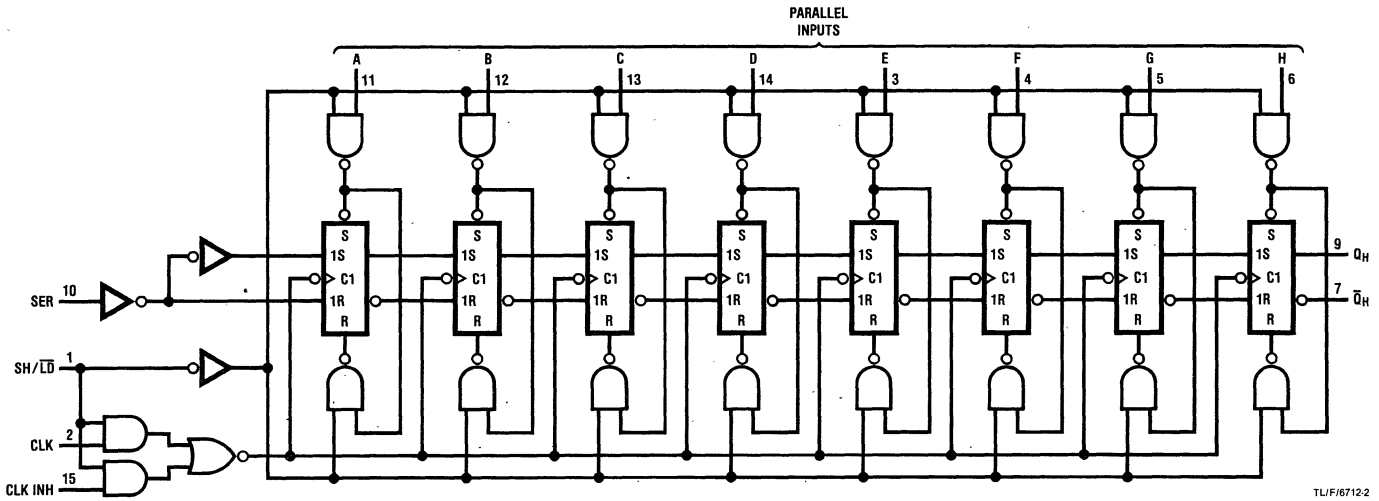
Parameter	Input	Output	Conditions	DM54ALS165			DM74ALS165			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
f_{MAX}			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max		60			60		MHz
t_{PLH}	CLK	Q_H			12			12		ns
t_{PHL}	CLK	Q_H			13			13		ns

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

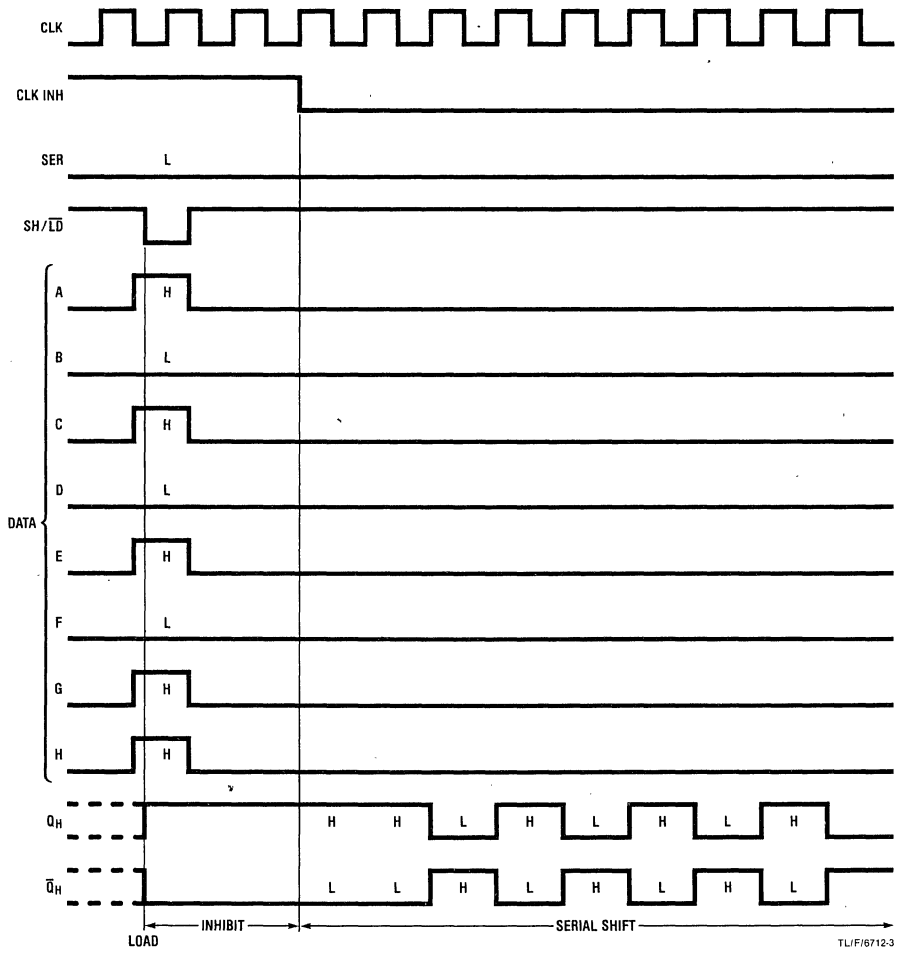
Note 3: With 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0V to 4.5V.

Logic Diagram



Timing Diagram

Typical Shift, Load, and Inhibit Sequences



National Semiconductor

PRELIMINARY

DM54ALS166/DM74ALS166 8-Bit Parallel Load Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or clock inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Features

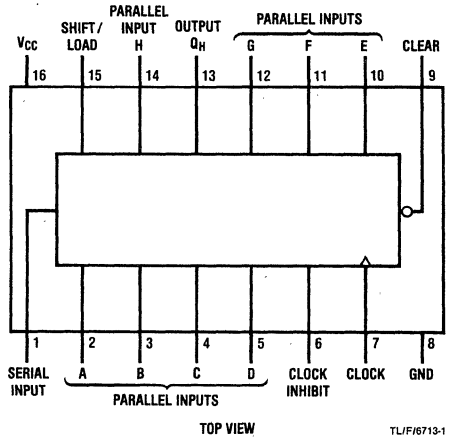
- Synchronous load
- Direct overriding clear
- Parallel-to-serial conversion

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



DM54ALS166 (J) DM74ALS166 (N)

Recommended Operating Conditions

Symbol	Parameter		DM54ALS166			DM74ALS166			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLOCK}	Clock Frequency								MHz
t_W	Pulse Duration	$\overline{CLR}$ Low							ns
		CLK High							
		CLK Low							
t_{SU}	Set-Up Time before CLK↑	SH/$\overline{LD}$							ns
		Data							
		$\overline{CLR}$ Inactive							
t_H	Hold Time, Data after CLK↑								
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

Parameter	Conditions	DM54ALS166			DM74ALS166			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5V, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = 5.5V, V_I = 0.4V			−0.1			−0.1	mA
I_O (Note 2)	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5V (Note 3)		16			16		mA

Switching Characteristics

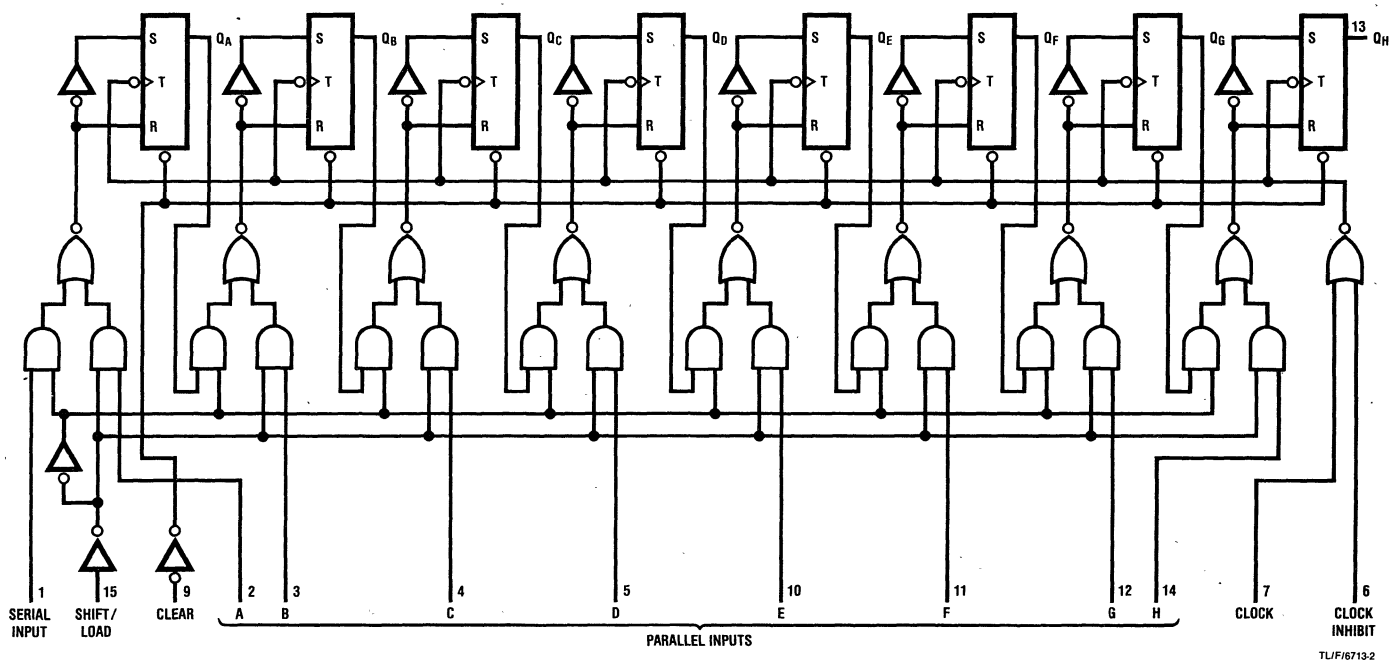
Parameter	Input	Output	Conditions	DM54ALS166			DM74ALS166			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
f_{MAX}			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max		60			60		MHz
t_{PHL}	$\overline{CLR}$	Q_H			10			10		ns
t_{PLH}	CLK	Q_H			12			12		ns
t_{PHL}	CLK	Q_H			13			13		ns

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: With 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0V to 4.5V.

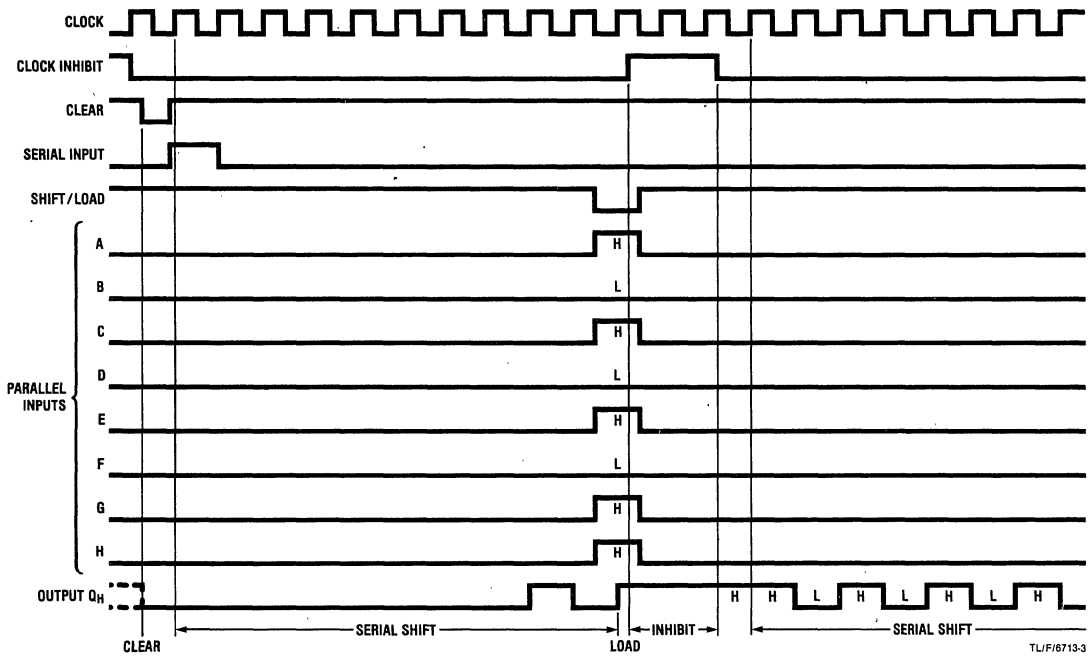
Logic Diagram



TL/F/6713-2

Timing Diagram

Typical Clear, Shift, Load, Inhibit, and Shift Sequences



Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady-state), L = low level (steady-state).

X = don't care (any input, including transitions).

↑ = transition from low-to-high level.

a...h = the level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

National Semiconductor

DM54ALS/DM74ALS168B, 169B Synchronous Four-Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The ALS168B is a four-bit decade up/down counter and the ALS169B is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously Programmable.
- Internal Look Ahead for Fast Counting.
- Carry Output for N-bit Cascading.
- Synchronous Counting.
- Load Control Line.
- ESD Inputs.

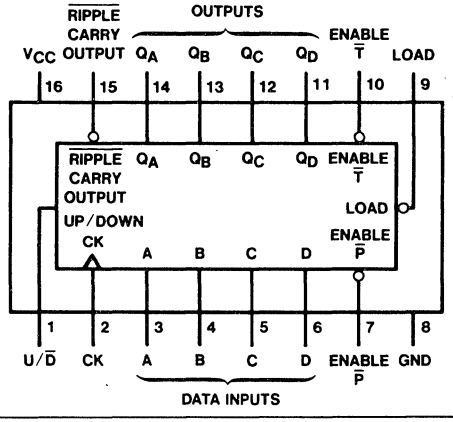
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54ALS168B (J) **74ALS168B (J,N)**

54ALS169B (J) **74ALS169B (J,N)**

TL/F/6207-1

Recommended Operating Conditions

Parameter		DM54ALS168B, 169B			DM74ALS168B, 169B			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, f_{CLOCK}		0		25	0		30	MHz
tsetup, Set-up time	Data; A, B, C, D	20↑	6		15↑	6		ns
	En $\overline{P}$, En $\overline{T}$	25↑	8		20↑	8		ns
	$\overline{Load}$	20↑	8		15↑	8		ns
	U/$\overline{D}$	20↑	10		15↑	10		ns
thold, Hold time	Data; A, B, C, D	0↑	−3		0↑	−3		ns
	En $\overline{P}$, En $\overline{T}$	0↑	−3		0↑	−3		ns
	$\overline{Load}$	0↑	−4		0↑	−4		ns
	U/$\overline{D}$	0↑	−4		0↑	−4		ns
Width of Clock Pulse, T_W		20			16.5			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −.4mA V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 4.5V V_{IH} = 2.7V	U/$\overline{D}$, CLK, LOAD, Data, EN $\overline{P}$, EN $\overline{T}$			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V	U/$\overline{D}$, CLK, LOAD, Data,			−0.2	mA
			EN $\overline{P}$ | EN $\overline{T}$			−0.2	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}		V_{CC} = 5.5V			15	25	mA

Note 1: The symbol (↑) indicates that the rising edge of the clock is used as reference.

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

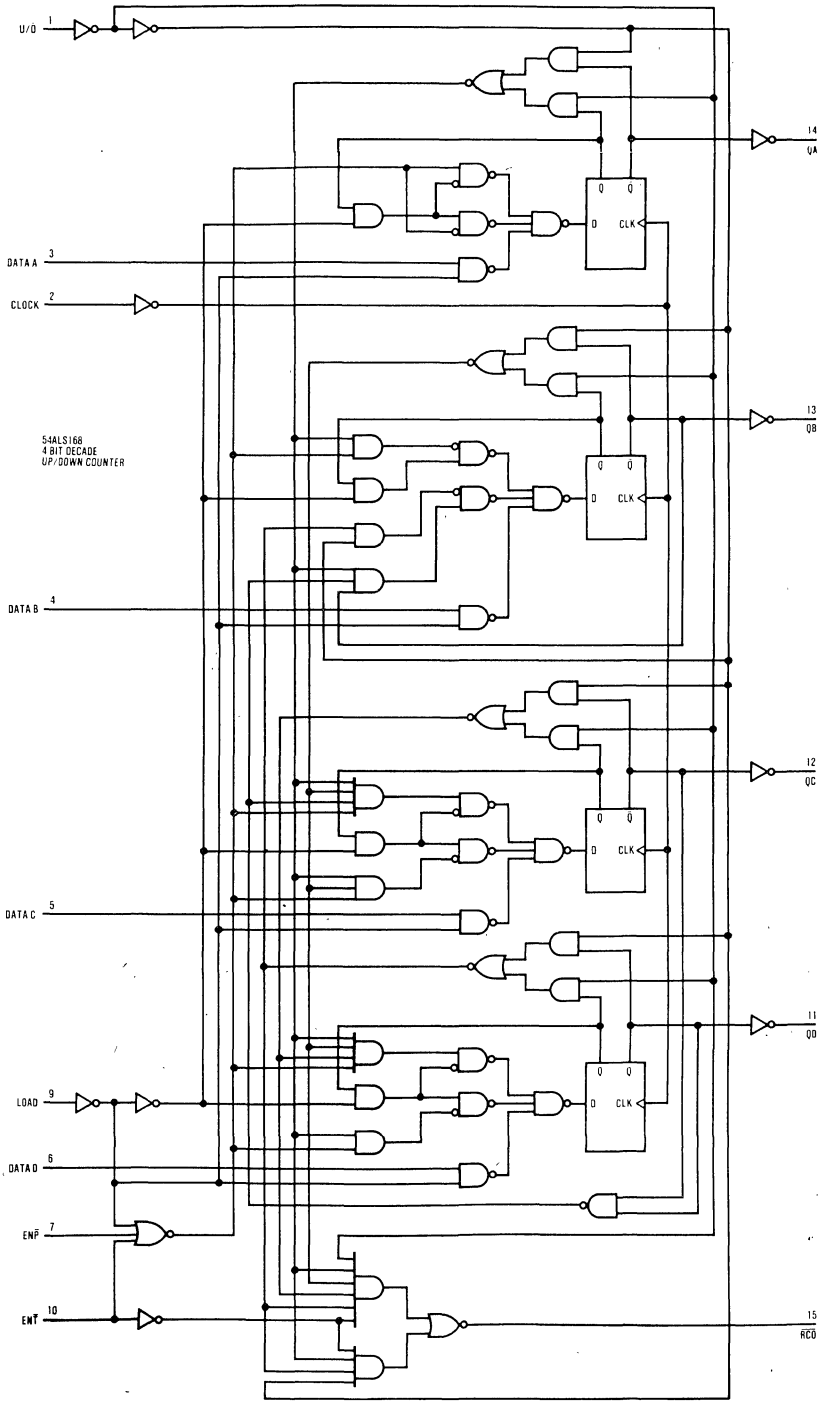
Parameter	From	To	Conditions	DM54ALS168B, 169B			DM74ALS168B, 169B			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	25			30			MHz
T_{PLH}, Propagation delay time. Low to high level output.	Clock	$\overline{\text{Ripple}}$ Carry		3		15	3		13	ns
T_{PHL}, Propagation delay time. High to low level output.				6		22	6		18	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		2		15	2		13	ns
T_{PHL}, Propagation delay time. High to low level output.				5		20	5		16	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	$\overline{\text{Ripple}}$ Carry		2		15	2		12	ns
T_{PHL}, Propagation delay time. High to low level output.				3		16	3		13	ns
T_{PLH}, Propagation delay time. Low to high level output.	U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry		5		21	5		18	ns
T_{PHL}, Propagation delay time. High to low level output.				5		21	5		18	ns

NOTE 1: See Section 1 for test waveforms and output load.

NOTE 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for ALS168B or 15 for ALS169B), the ripple carry output will be out of phase.

Logic Diagrams

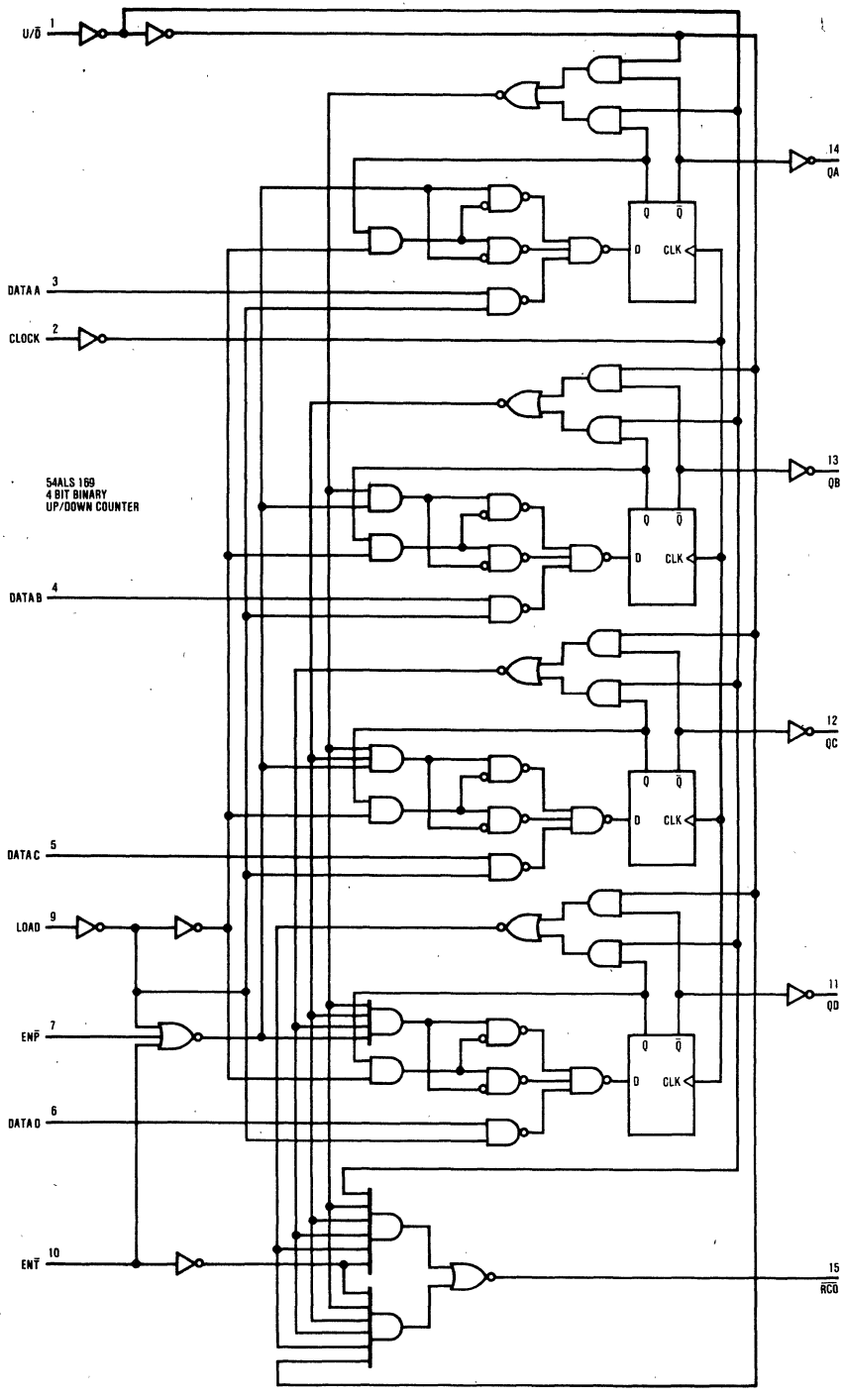
DM54ALS/DM74ALS168B



TL/F/6207-2

Logic Diagrams (Continued)

DM54ALS/DM74ALS169B



TL/F/6207-3

National Semiconductor

DM54ALS/DM74ALS174,175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Pin and Functional compatible with LS family counterpart.
- Typical clock frequency maximum is 80 MHz.
- Switching performance guaranteed over full temperature and V_{CC} supply range.
- 54ALS174 contains six flip-flops with separate D inputs and Q outputs.
- 54ALS175 contains four flip-flops with separate D inputs and both Q and $\overline{Q}$ outputs.

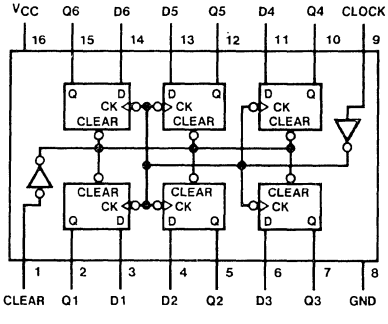
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS174/175	−55°C to 125°C
DM74ALS174/175	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

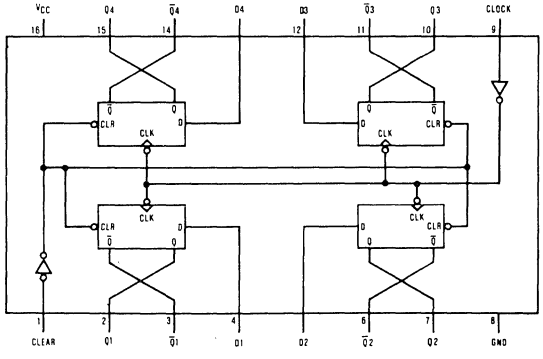
Dual-In-Line Package



TL/L/6112-1

54ALS174 (J) 74ALS174 (J,N)

Dual-In-Line Package



TL/L/6112-2

54ALS175 (J) 74ALS175 (J,N)

Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
* applies to 54ALS175/74ALS175 only

Recommended Operating Conditions

Parameter		DM54ALS174,175			DM74ALS174,175			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Pulse Width, t_W	Clock High or Low	12.5			10			ns
	$\overline{\text{Clear}}$ Low	15			10			
Setup Time, t_{SETUP} (Note 1)	Data Input	15↑			10↑			ns
	$\overline{\text{Clear}}$ Inactive State	8↑			6↑			
Data Hold Time, t_{HOLD} (Note 1)		0↑			0↑			ns
Clock Frequency, f_{CLOCK}		0		40	0		50	MHz

Note 1: The symbol ↑ indicates that the rising edge of the clock is used as reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18mA$					−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\mu A$ $V_{CC} = 4.5$ to $5.5V$			$V_{CC}-2$	$V_{CC}-1.6$		V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 4mA$	DM54/74		0.25	0.4	V
			$I_{OL} = 8mA$	DM74		0.35	0.5	
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$					0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$					20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$					−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V = 2.25V$			−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Clock = 4.5V Clear = GND D Inputs = 4.5V		ALS174		11	19	mA
				ALS175		8	14	

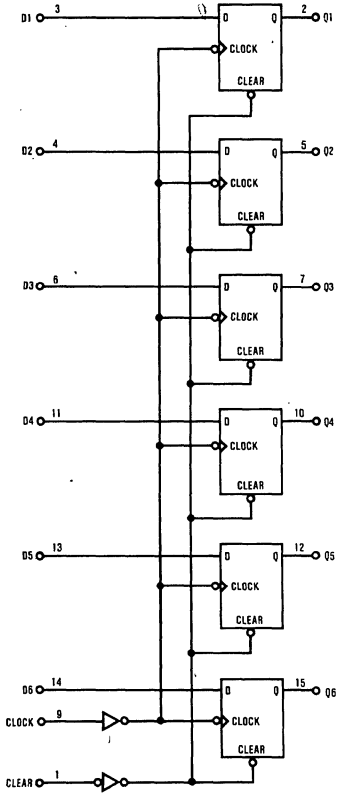
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	54ALS174,175			74ALS174,175			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}, Maximum Clock Frequency	$R_L = 500\Omega$ $C_L = 50pF$	40			50			MHz
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clear (175 Only)	$R_L = 500\ \Omega$ $C_L = 50pF$	5		20	5		18	ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clear	$R_L = 500\ \Omega$ $C_L = 50pF$	8		26	8		23	ns
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clock	$R_L = 500\ \Omega$ $C_L = 50pF$	3		17	3		15	ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clock	$R_L = 500\ \Omega$ $C_L = 50pF$	5		20	5		17	ns

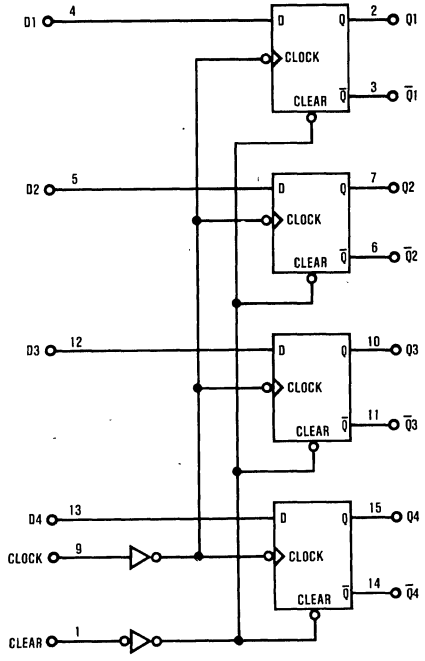
Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams



TL/F/6112-3

54ALS174/74ALS174



TL/F/6112-4

54ALS175/74ALS175

National Semiconductor

DM54ALS190/DM74ALS190, DM54ALS191/DM74ALS191 Synchronous 4-Bit Up/Down Decade and Binary Counter

General Description

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high level transition of the clock input if the enable input (G) is low. A high at G inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (G and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable set-up and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{U}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control

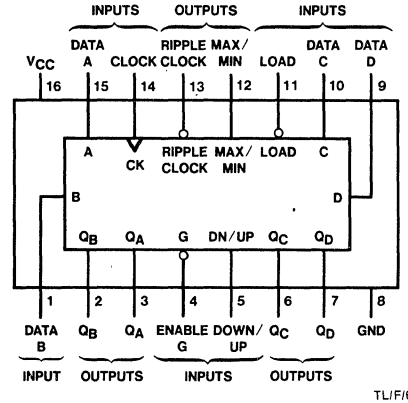
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram (Dual-In-Line Package)

DM54ALS190 (J) **DM74ALS191 (J, N)**
DM54ALS190 (J) **DM74ALS191 (J, N)**



TL/F/6208-1

Recommended Operating Conditions

Symbol	Parameter			DM54ALS190, 191			DM74ALS190, 191			Units
				Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage			2			2			V
V_{IL}	Low-Level Input Voltage					0.8			0.8	V
I_{OH}	High-Level Output Current					−0.4			−0.4	mA
I_{OL}	Low-Level Output Current					4			8	mA
f_{CLOCK}	Clock Frequency	'ALS190		0		20	0		25	MHz
		'ALS191		0		25	0		30	MHz
t_W	Pulse Duration	CLK High or Low	'ALS190	25			20			ns
			'ALS191	20			16.5			ns
		$\overline{LOAD}$ low		25			20			ns
t_{SU}	Set-Up Time	Data Before $\overline{LOAD}$↑		25			20			ns
		G Before CLK↑		25			20			ns
		D/$\overline{U}$ Before CLK↑		20			20			ns
		$\overline{LOAD}$ Inactive Before CLK↑		20			20			ns
t_H	Hold Time	Data After $\overline{LOAD}$↑		5			5			ns
		G After CLK↑		0			0			ns
		D/$\overline{U}$ After CLK↑		0			0			ns
T_A	Operating Free Air Temperature			−55		125	0		70	ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM54ALS190, 191			DM74ALS190, 191			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 4 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8 mA						0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	G or CLK			−0.2			−0.2	mA
			All Others			−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, All Inputs at 0V			12	22		12	22	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Switching Characteristics (Note 1).

Parameter		From (Input)	To (Output)	Conditions	DM54ALS190, 191			DM74ALS190, 191			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
f_{MAX}	'ALS190			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	20			25			MHz
	'ALS191				25			30			MHz
t_{PLH}, Propagation Delay Time, Low to High Level Output		$\overline{LOAD}$	Any Q		8		34	8		30	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					8		34	8		30	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		A, B, C, D	Any Q		4		25	4		21	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					4		25	4		21	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		CLK	$\overline{RCO}$		5		24	5		20	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					5		24	5		20	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		CLK	Any Q		3		22	3		18	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					3		22	3		18	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		CLK	Max/Min		8		34	8		31	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					8		34	8		31	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		D/$\overline{U}$	$\overline{RCO}$		15		42	15		37	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					10		33	10		28	ns

Switching Characteristics (Continued) (Note 1).

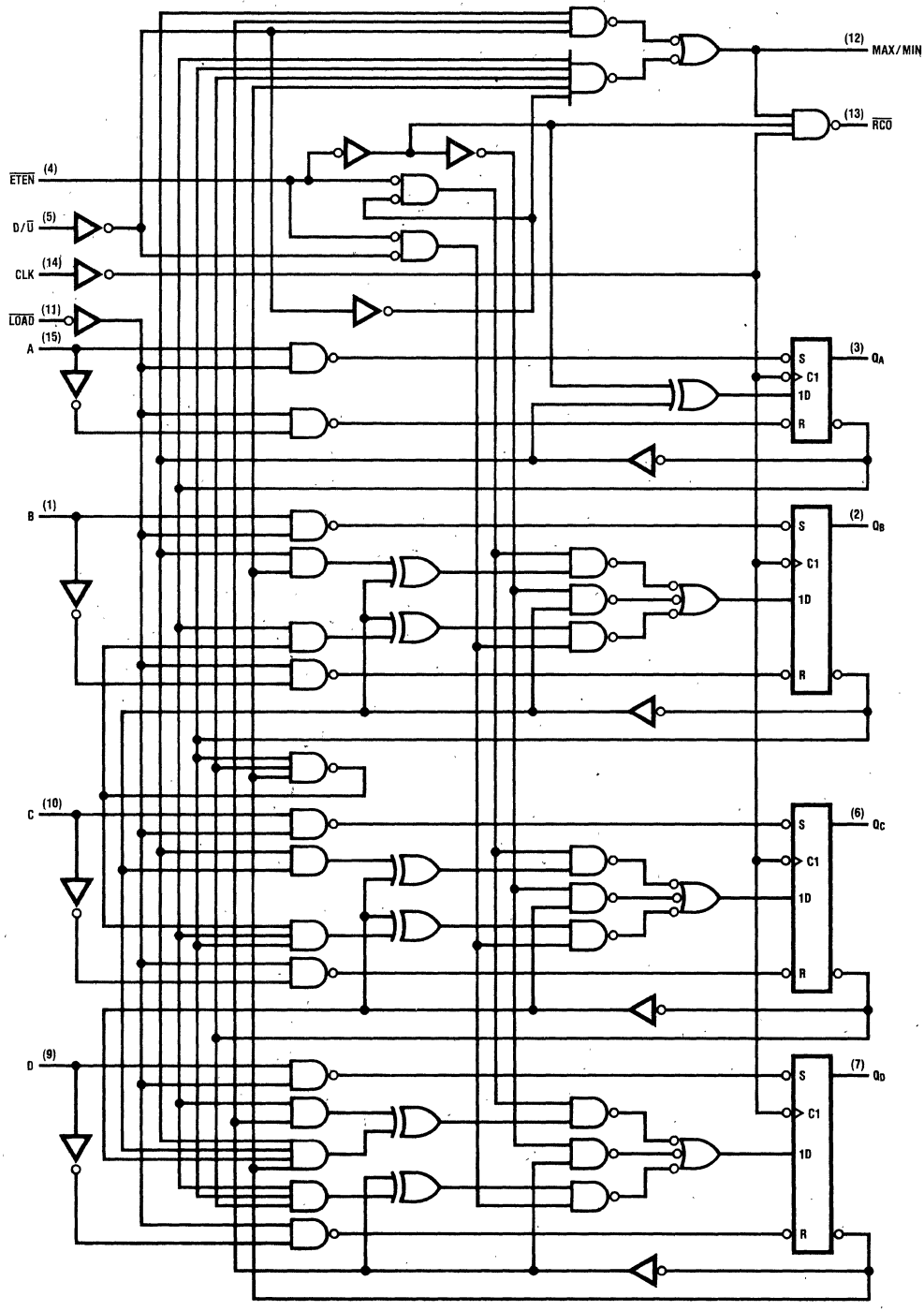
Parameter	From (Input)	To (Output)	Conditions	DM54ALS190, 191			DM74ALS190, 191			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PLH}, Propagation Delay Time, Low to High Level Output	D/$\overline{U}$	Max/Min	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	8		30	8		25	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output				8		30	8		25	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output	G	$\overline{RCO}$		4		21	4		18	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output				4		21	4		18	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Logic Diagrams (positive logic)

ALS190



Pin numbers shown are for J and N packages.

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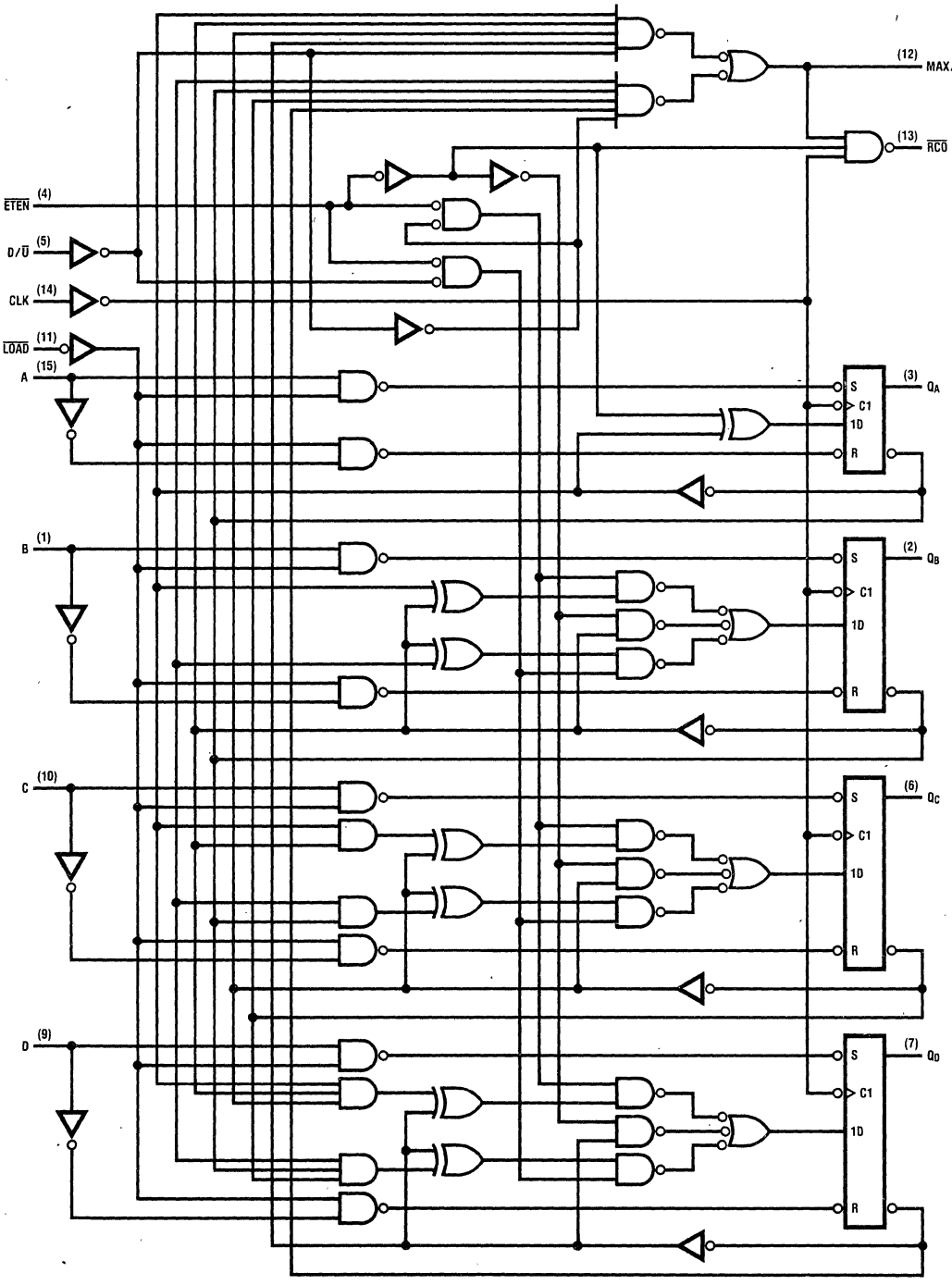
Logic Diagrams (Continued) (positive logic)

ALS191



Pin numbers shown are for J and N packages.

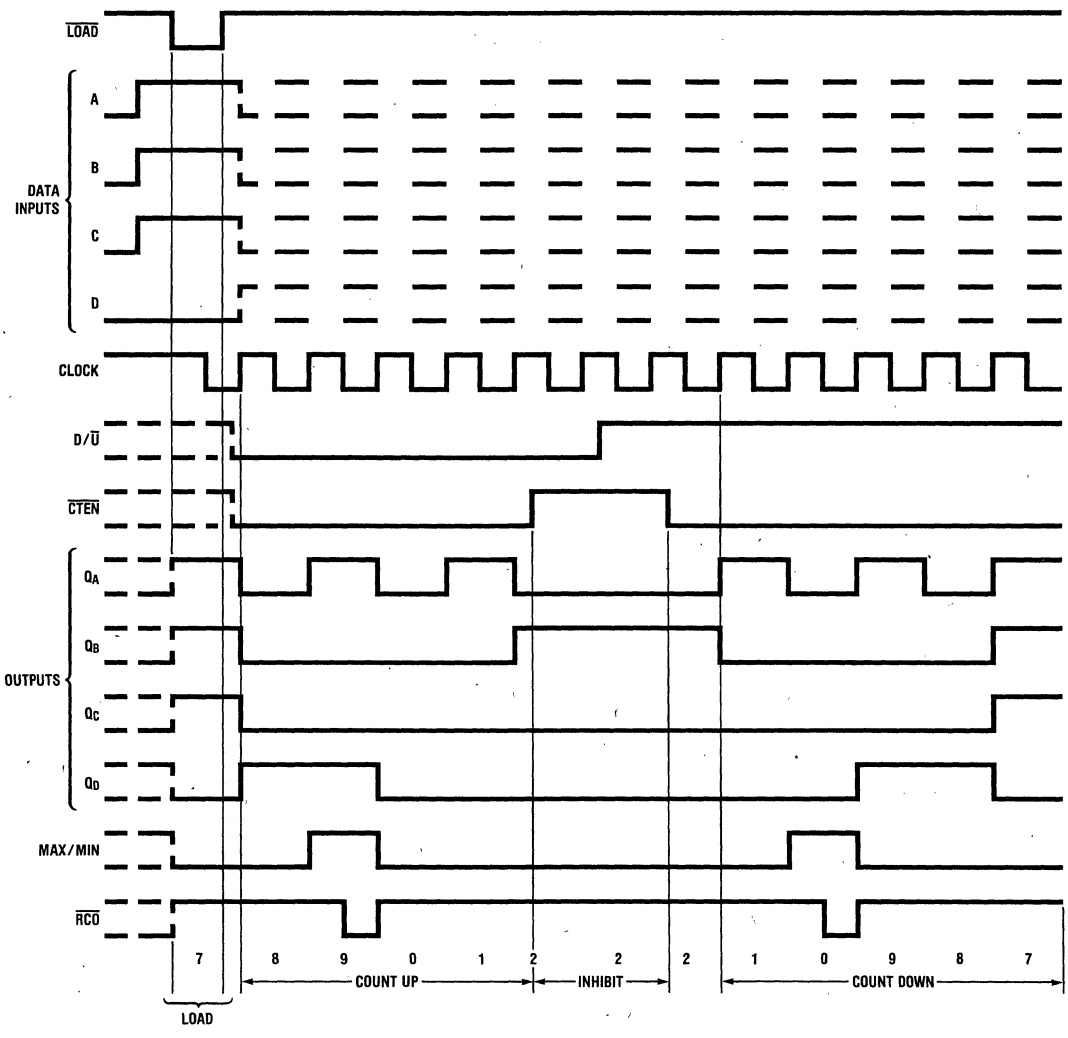
TL/F/6208-3

Timing Diagrams

'ALS190 Typical Load, Count, and Inhibit Sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



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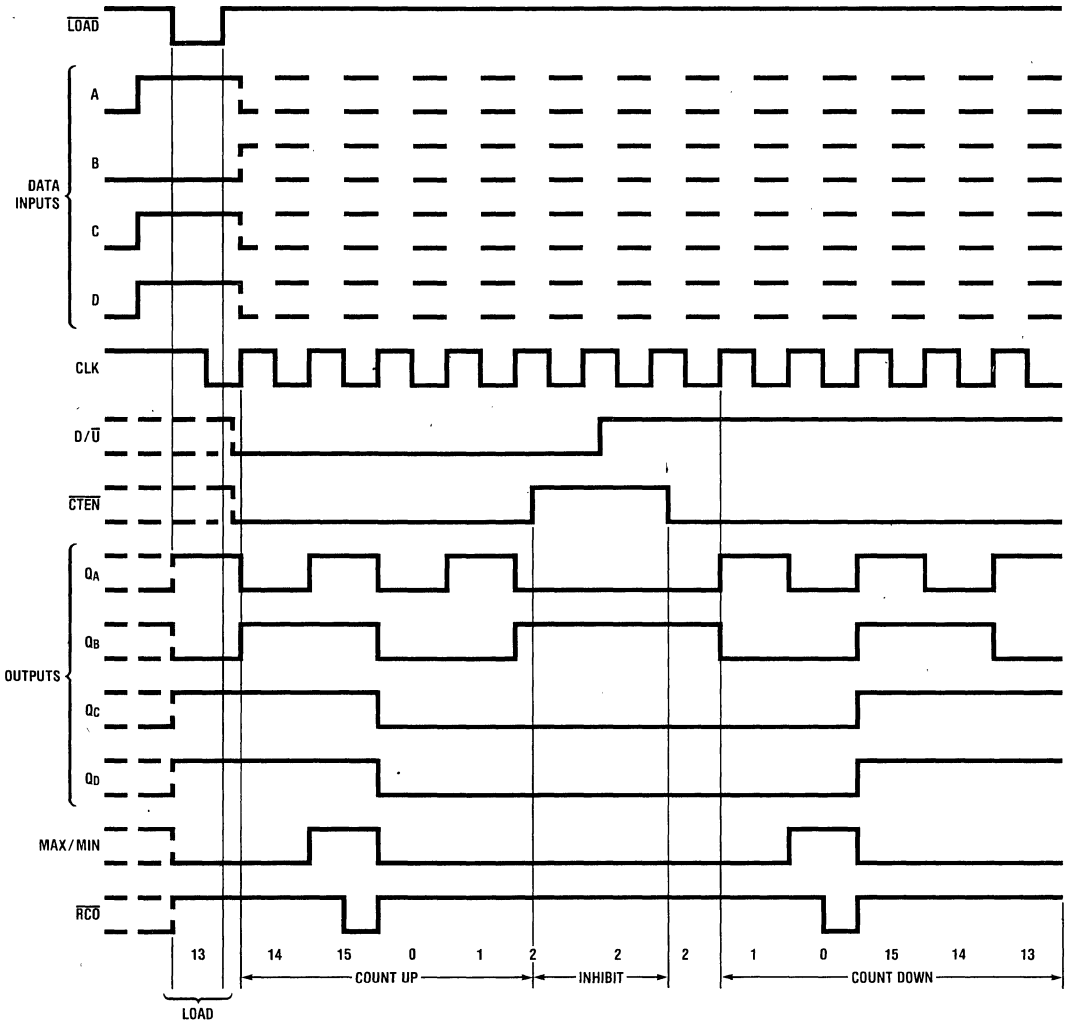
Timing Diagrams (Continued)

'ALS191 Typical Load, Count, and Inhibit Sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



TL/F/6208-5

National Semiconductor

DM54ALS192/DM74ALS192, DM54ALS193/DM74ALS193 Synchronous 4-Bit Up/Down Counters (Dual Clock with Clear)

General Description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high level transition of either count (clock) input (up or down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts
- Look ahead circuitry enhances cascaded counters
- Fully synchronous in count mode
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear

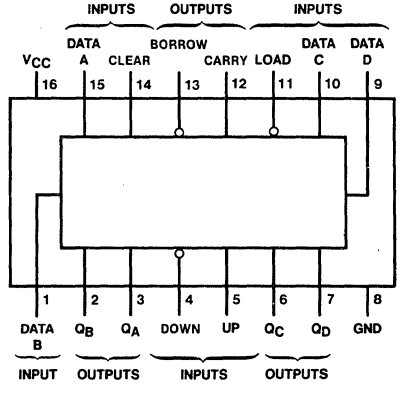
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram (Dual-In-Line Package)

DM54ALS192 (J) **DM74ALS192 (J, N)**
DM54ALS193 (J) **DM74ALS193 (J, N)**



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Note: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$.

Recommended Operating Conditions

Symbol	Parameter			DM54ALS192, 193			DM74ALS192, 193			Units
				Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
I_{OH}	High Level Output Current					−0.4			−0.4	mA
I_{OL}	Low Level Output Current					4			8	mA
f_{CLOCK}	Clock Frequency	'ALS192		0		20	0		25	MHz
		'ALS193		0		25	0		30	MHz
t_W	Pulse Duration	CLR High		10			10			ns
		$\overline{LOAD}$ Low		25			20			ns
		UP or DOWN High or Low	'ALS192	25			20			ns
			'ALS193	20			16.5			ns
t_{SU}	Set-Up Time	Data Before $\overline{LOAD}$↑		25			20			ns
		CLR Inactive Before UP↑ or DOWN↑		20			20			ns
		$\overline{LOAD}$ Inactive Before UP↑ or DOWN↑		20			20			ns
		Up High Before Down↑		17			17			ns
		Down High Before Up↑		15			15			ns
t_H	Hold Time	Data after $\overline{LOAD}$↑		5			5			ns
		Up High After DOWN↑		5			5			ns
		DOWN High After UP↑		8			8			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range.

Symbol	Parameter	Conditions		DM54ALS192, 193			DM74ALS192, 193			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 4 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8 mA						0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	UP, DOWN			−0.2			−0.2	mA
			All Others			−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 3)			12	22		12	22	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5V.

Switching Characteristics (Note 4)

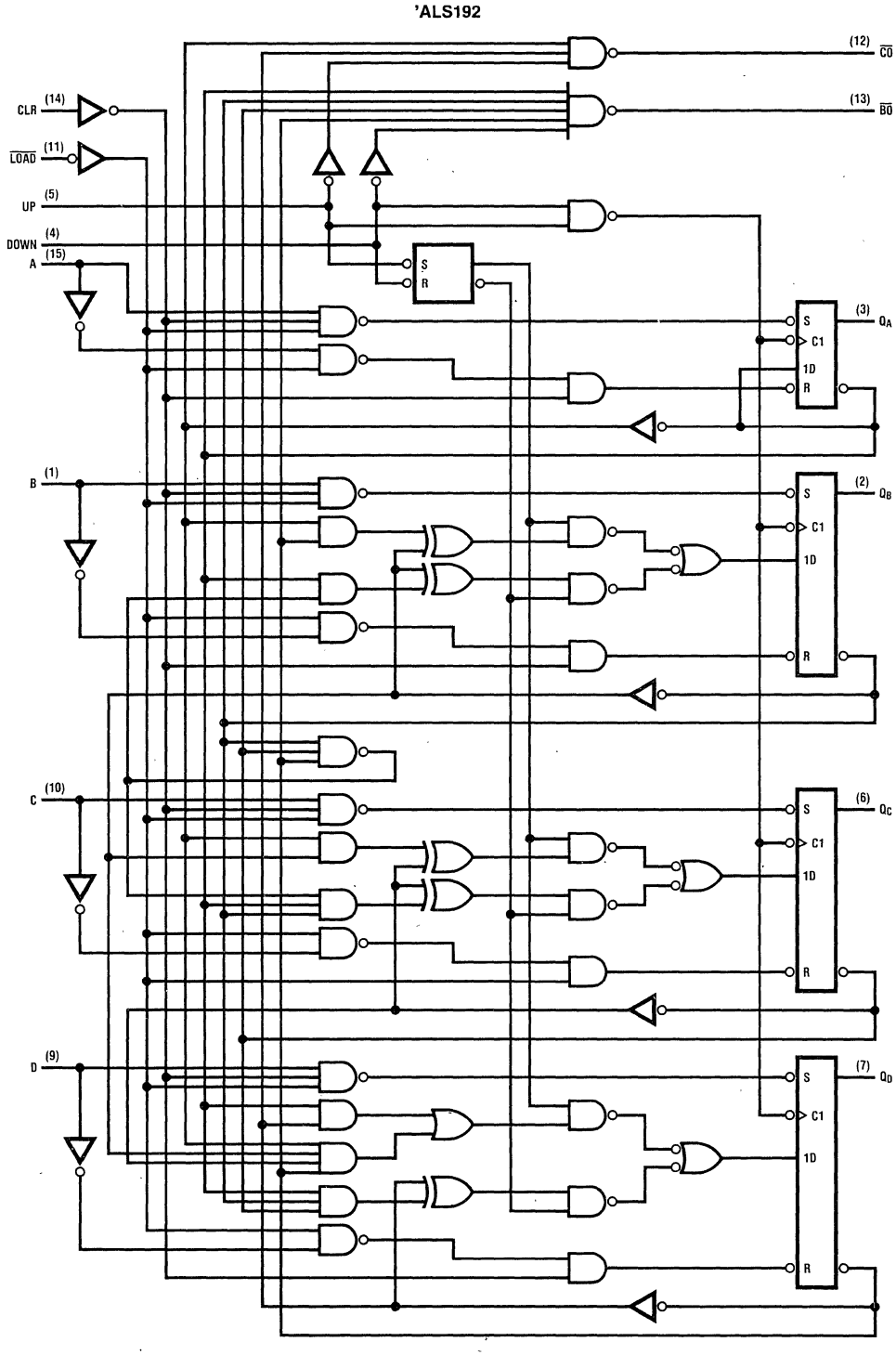
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter		From (Input)	To (Output)	Conditions	DM54ALS192, 193			DM74ALS192, 193			Units
					Min	Typ	Max	Min	Typ	Max	
f_{MAX}	'ALS192			$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$, $T_A =$ Min to Max	20			25			MHz
	'ALS193				25			30			MHz
t_{PLH}, Propagation Delay Time, Low to High Level Output		Up	C0		4		19	4		16	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					5		21	5		18	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		Down	B0		4		19	4		16	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					5		21	5		18	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		Up or Down	Any Q		4		23	4		19	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					4		20	4		17	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output		$\overline{LOAD}$	Any Q		8		35	8		30	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output					8		31	8		28	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output		CLR	Any Q		5		20	5		17	ns

Note 4: See Section 1 for test waveforms and output load.

Logic Diagrams (positive logic)

'ALS192



Pin numbers shown are for J and N packages.

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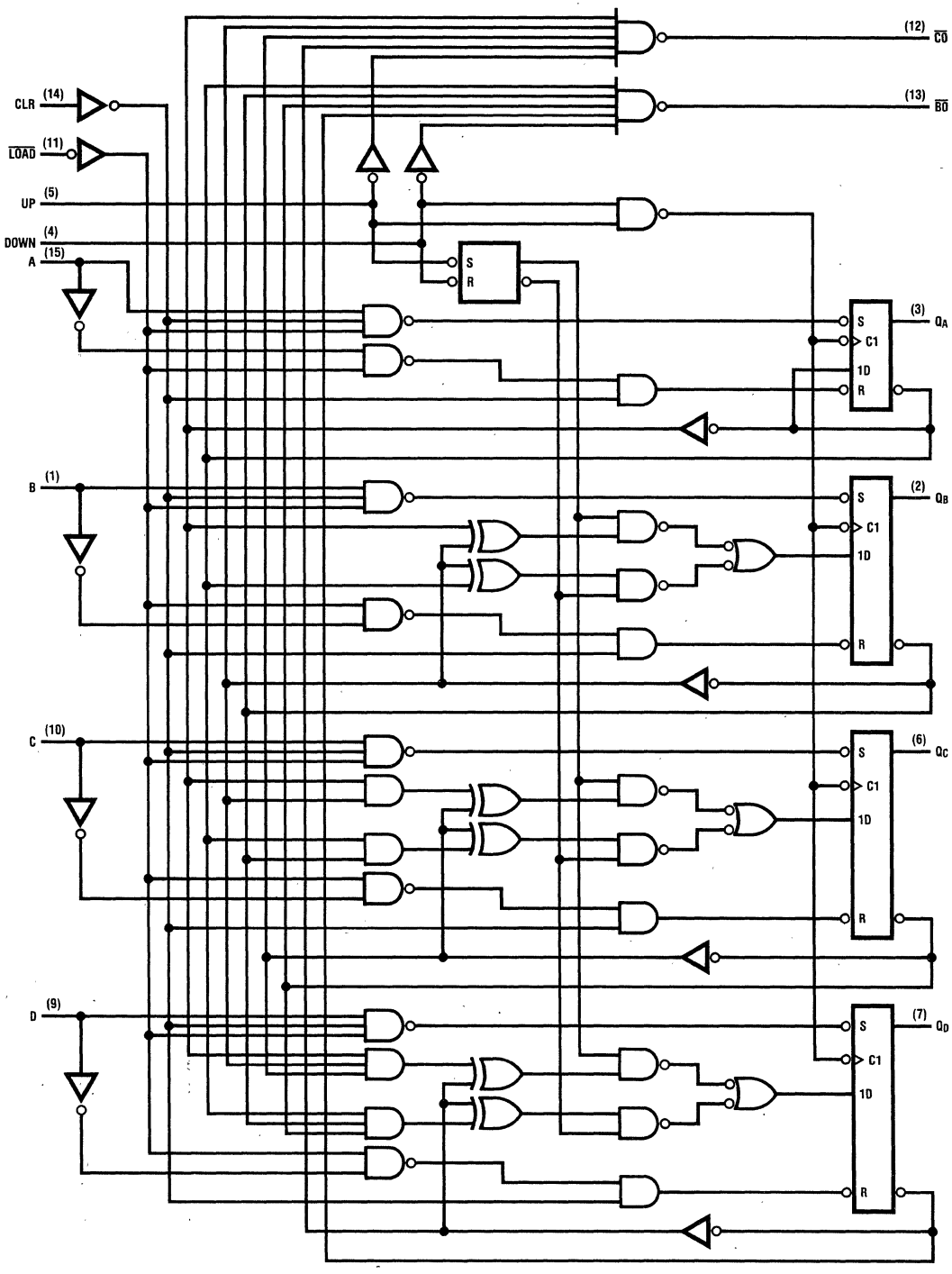
Logic Diagrams (Continued) (positive logic)

'ALS193



Pin numbers shown are for J and N packages.

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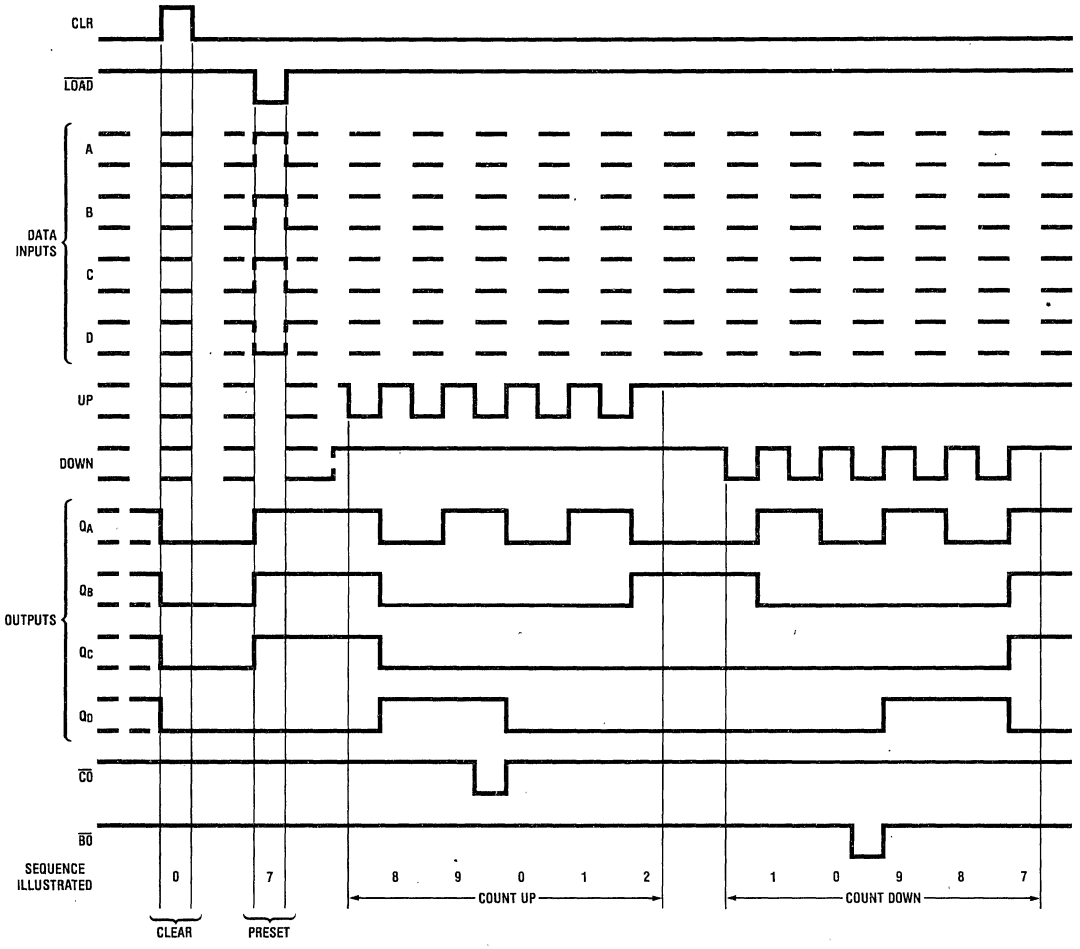
Timing Diagrams

'ALS192 Typical Clear, Load and Count Sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



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Note A: Clear overrides load, data, and count inputs.

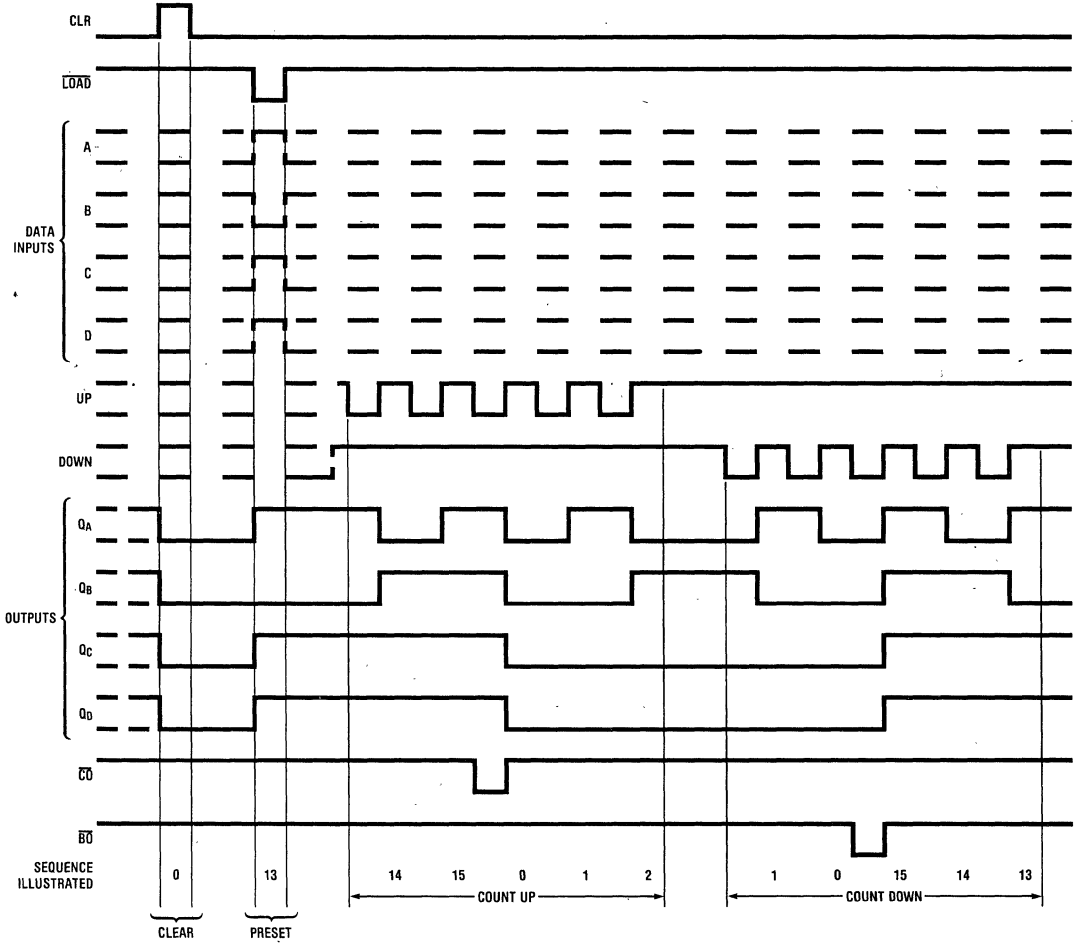
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

'ALS193 Typical Clear, Load and Count Sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



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Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

DM54ALS240A/DM74ALS240A, DM54ALS241A/DM74ALS241A Octal TRI-STATE® Bus Drivers

General Description

These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers. The ALS240A control inputs symmetrically enable the respective outputs when set logic low, while the ALS241A has complementary enable gating. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

The -1 versions of the DM74ALS devices are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the DM54ALS devices.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current:
  54ALS = 12 mA, 74ALS = 24 mA, 74ALS-1 = 48 mA

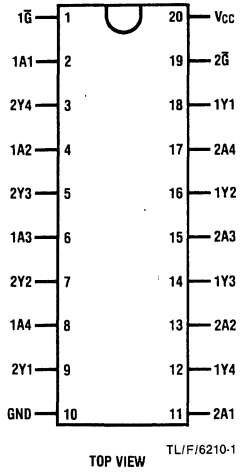
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

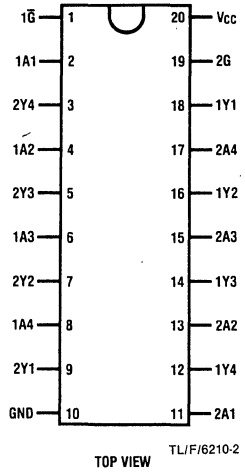
Dual-In-Line Package



TOP VIEW TL/F/6210-1

DM54ALS240A (J)
DM74ALS240A (J, N)

Dual-In-Line Package



TOP VIEW TL/F/6210-2

DM54ALS241A (J)
DM74ALS241A (J, N)

Function Table

Enable Input		Data Buffer Output
G	$\overline{G}$	
H	L	Active
L	H	TRI-STATE

Recommended Operating Conditions

Symbol	Parameter	DM54ALS240A, 241A			DM74ALS240A, 241A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS240A-1, DM74ALS241A-1			—			48	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS240A, 241A			DM74ALS240A, 241A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS240A Outputs High			4	10		4	10	mA
		Outputs Low			13	23		13	23	mA
		Outputs TRI-STATE			14	25		14	25	mA
		V_{CC} = 5.5V, ALS241A Outputs High			9	17		9	15	mA
		Outputs Low			15	28		15	26	mA
		Outputs TRI-STATE			17	32		17	30	mA

'ALS240A Switching Characteristics over recommended operating free air temperature range

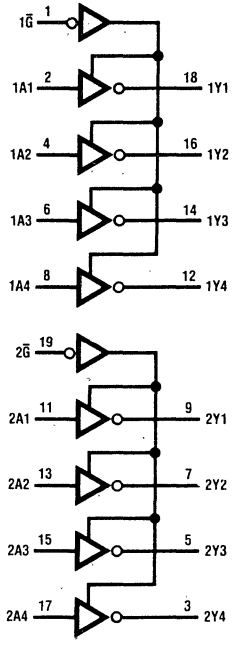
Parameter	From (Input)	To (Output)	Conditions	54ALS240A			74ALS240A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	2		12	2		9	ns
t_{PHL}				2		11	2		9	ns
t_{PZH}	$\overline{G}$	Y		5		15	5		13	ns
t_{PZL}				5		20	5		18	ns
t_{PHZ}	$\overline{G}$	Y		2		12	2		10	ns
t_{PLZ}				3		18	3		12	ns

'ALS241A Switching Characteristics over recommended operating free air temperature range

Parameter	From (Input)	To (Output)	Conditions	54ALS241A			74ALS241A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	3		14	3		11	ns
t_{PHL}				3		13	3		10	ns
t_{PZH}	$1\overline{G}$	Y		7		25	7		21	ns
t_{PZL}				7		25	7		21	ns
t_{PHZ}	$1\overline{G}$	Y		2		12	2		10	ns
t_{PLZ}				3		20	3		15	ns
t_{PZH}	2G	Y		7		25	7		21	ns
t_{PZL}				7		25	7		21	ns
t_{PHZ}	2G	Y		2		12	2		10	ns
t_{PLZ}				3		20	3		15	ns

Logic Diagrams

DM54/74ALS240A



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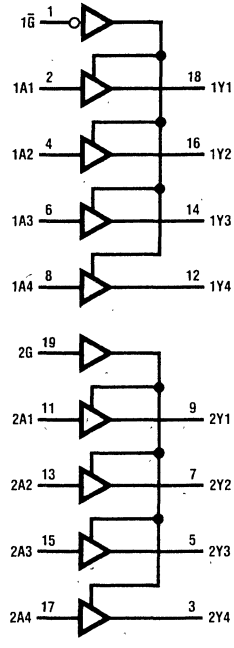
DM54/74ALS241A



TL/F/6210-4

National Semiconductor

DM54ALS242A/DM74ALS242A, DM54ALS243A/DM74ALS243A Quad Bi-Directional Bus Drivers

General Description

These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The ALS242A has inverting buffers, while the ALS243A has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

The -1 versions of the DM74ALS devices are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the DM54ALS devices.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current:
  54ALS = 12 mA, 74ALS = 24 mA, 74ALS-1 = 48 mA

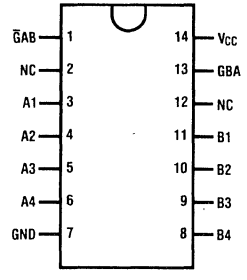
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6211-1

TOP VIEW

DM54ALS242A (J) DM74ALS242A (J, N)
DM54ALS243A (J) DM74ALS243A (J, N)

Function Table

Inputs		'ALS242A	'ALS243A
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

Recommended Operating Conditions

Symbol	Parameter	DM54ALS242A, 243A			DM74ALS242A, 243A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS242A-1, DM74ALS243A-1			—			48	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS242A, 243A			DM74ALS242A, 243A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (5.5V for I/O Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS242A Active Outputs High			10	20		10	16	mA
		Active Outputs Low			14	26		14	21	mA
		Outputs TRI-STATE			15	27		15	22	mA
		V_{CC} = 5.5V, ALS243A Active Outputs High			15	30		15	25	mA
		Active Outputs Low			20	35		20	30	mA
		Outputs TRI-STATE			21	37		21	32	mA

'ALS242A Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	To (Output)	Conditions	54ALS242A			74ALS242A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	3		15	3		11	ns
t_{PHL}				2		14	2		10	ns
t_{PZH}	$\overline{G}$AB	B		4		22	4		18	ns
t_{PZL}				7		25	7		21	ns
t_{PHZ}	$\overline{G}$AB	B		2		16	2		14	ns
t_{PLZ}				4		28	4		22	ns
t_{PZH}	GBA	A		4		22	4		18	ns
t_{PZL}				7		25	7		21	ns
t_{PHZ}	GBA	A		2		16	2		14	ns
t_{PLZ}				4		28	4		22	ns

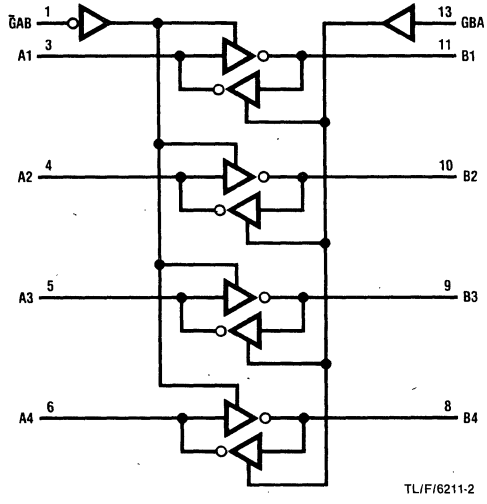
'ALS243A Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	To (Output)	Conditions	54ALS243A			74ALS243A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	4		15	4		11	ns
t_{PHL}				4		15	4		11	ns
t_{PZH}	$\overline{G}$AB	B		7		25	7		20	ns
t_{PZL}				7		25	7		20	ns
t_{PHZ}	$\overline{G}$AB	B		2		16	2		14	ns
t_{PLZ}				3		27	3		22	ns
t_{PZH}	GBA	A		7		25	7		20	ns
t_{PZL}				7		25	7		20	ns
t_{PHZ}	GBA	A		2		16	2		14	ns
t_{PLZ}				3		27	3		22	ns

Note 1: See Section 1 for test waveforms and output loads.

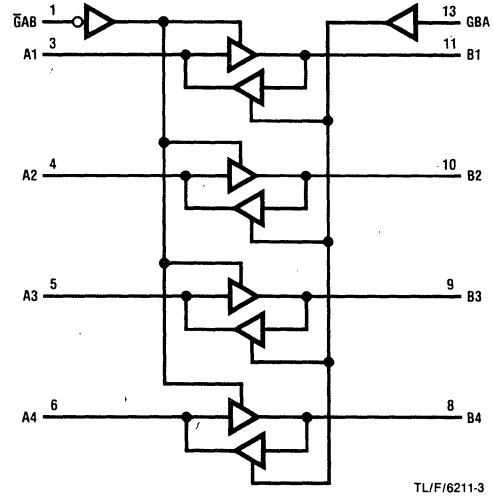
Logic Diagrams

DM54/74ALS242A



TL/F/6211-2

DM54/74ALS243A



TL/F/6211-3

National Semiconductor

DM54ALS244A/DM74ALS244A Octal TRI-STATE® Bus Driver

General Description

This octal TRI-STATE bus driver is designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers, and both control inputs enable the respective outputs when set logic low. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

The -1 versions of the DM74ALS devices are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the DM54ALS devices.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current:
  54ALS = 12 mA, 74ALS = 24 mA, 74ALS-1 = 48 mA

Absolute Maximum Ratings (Note 1)

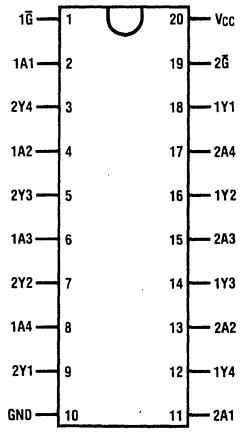
Supply Voltage, V_{CC}	7V
Input Voltage	7V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6212-1

TOP VIEW

DM54ALS244A (J) **DM74ALS244A (J, N)**

Function Table

Enable Input $1\overline{G}$ or $2\overline{G}$	Data Buffer Outputs
L	Active
H	TRI-STATE

Recommended Operating Conditions

Symbol	Parameter	DM54ALS244A			DM74ALS244A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS244A-1			—			48	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise specified)

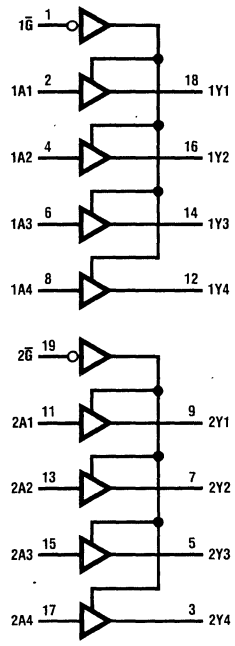
Symbol	Parameter	Conditions		DM54ALS244A			DM74ALS244A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs High			9	15		9	15	mA
		Outputs Low			15	24		15	24	mA
		Outputs TRI-STATE			17	27		17	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

Parameter	From (Input)	To (Output)	Conditions	54ALS244A			74ALS244A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	3		13	3		10	ns
t_{PHL}				3		13	3		10	ns
t_{PZH}	$\overline{G}$	Y		7		25	7		20	ns
t_{PZL}				7		25	7		20	ns
t_{PHZ}	$\overline{G}$	Y		2		12	2		10	ns
t_{PLZ}				3		18	3		13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6212-2

National Semiconductor

DM54ALS245A/DM74ALS245A Octal TRI-STATE® Bus Transceivers

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data transmits either from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode so that the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Non-inverting logic output
- Glitch free bus during power up and down
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω 50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- PNP inputs to reduce input loading
- Switching specifications guaranteed over full temperature and V_{CC} range

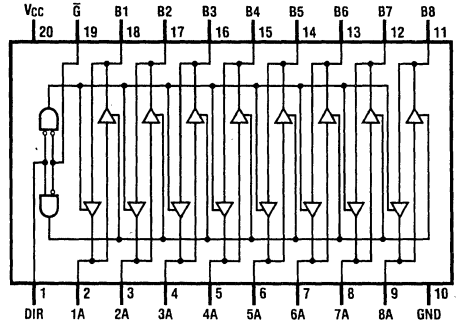
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6213-1

DM54ALS245A (J) DM74ALS245A (J, N)

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

Recommended Operating Conditions

Symbol	Parameter	DM54ALS245A			DM74ALS245A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS245A-1 Option Only						48	mA

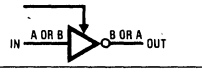
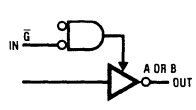
Electrical Characteristics over recommended operating free air temperature range

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA					−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3$ mA			2.4	3.2		V
		$V_{CC} = 4.5V$, I_{OH} = Max			2	2.3		V
		$I_{OH} = -0.4$ mA, $V_{CC} = 4.5V$ to 5.5V			$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 12$ mA			0.25	0.4	V
			74ALS $I_{OL} = 24$ mA			0.35	0.5	V
			74ALS-1 $I_{OL} = 48$ mA				0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$	$V_{IN} = 7V$	Control Inputs			0.1	mA
			$V_{IN} = 5.5V$	A or B Ports			0.1	
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$					20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$					−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$			−30		−112	mA
I_{CC}	54ALS245A Supply Current	$V_{CC} = 5.5V$	Outputs High			30	48	mA
			Outputs Low			38	60	mA
			TRI-STATE			38	63	mA
I_{CC}	74ALS245A Supply Current	$V_{CC} = 5.5V$	Outputs High			30	45	mA
			Outputs Low			36	55	mA
			TRI-STATE			38	58	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter (Propagation Delay Time)	Circuit Configuration	DM54ALS245A			DM74ALS245A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	High-to-Low Level Output		3		15	3		10	ns
t_{PHL}	High-to-Low Level Output		3		13	3		10	ns
t_{PZL}	Output Enable to Low Level		5		25	5		20	ns
t_{PZH}	Output Enable to High Level		5		25	5		20	ns
t_{PLZ}	Output Disable from Low Level		4		18	4		15	ns
t_{PHZ}	Output Disable from High Level		2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to 5.5V, $R_L = 500\Omega$, $C_L = 50$ pF.

National Semiconductor

DM54ALS251/DM74ALS251 TRI-STATE® 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. An Output Control input is provided which, when at the high level, places both outputs in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

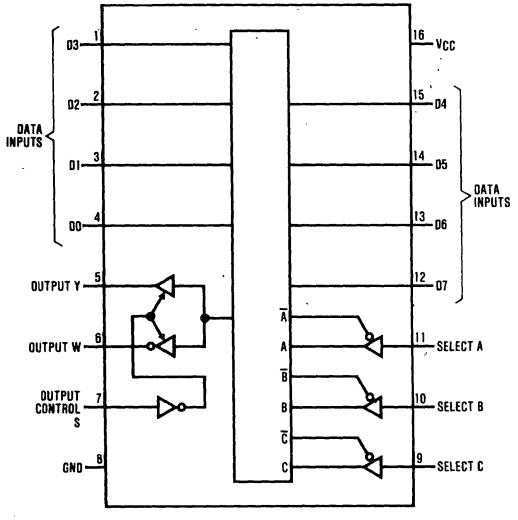
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS251	−55°C to 125°C
DM74ALS251	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6214-1

54ALS251 (J) **74ALS251 (J,N)**

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level, X = Don't Care
Z = High Impedance (Off)
D0 thru D7 = The Level of the Respective D Input

Recommended Operating Conditions

Parameter	DM54ALS251			DM74ALS251			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = 400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Data Inputs = 4.5V, Select Inputs = 4.5V, Control Inputs = 4.5V	Enabled		7	10	mA
			Disabled		9.4	14	

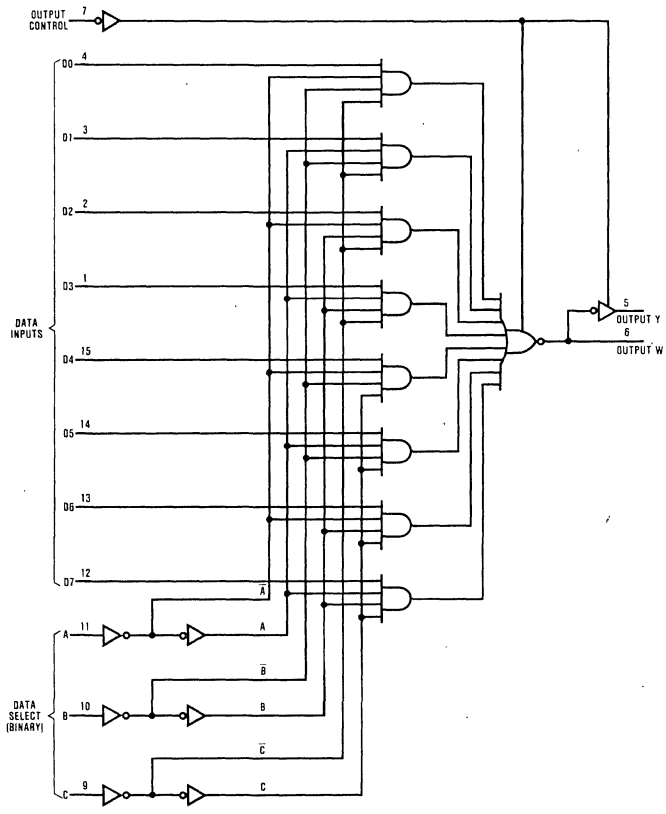
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS251			DM74ALS251			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	5		21	5		18	ns
t_{PHL}, High to low Level Output				8		28	8		24	ns
t_{PLH}, Low to high Level Output		W		8		28	8		24	ns
t_{PHL}, High to low Level Output				7		26	7		23	ns
t_{PLH}, Low to high Level Output	Data	Y		2		12	2		10	ns
t_{PHL}, High to low Level Output				3		18	3		15	ns
t_{PLH}, Low to high Level Output		W		3		18	3		15	ns
t_{PHL}, High to low Level Output				3		18	3		15	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y		3		18	3		15	ns
t_{ZL}, Output Enable Time to Low Level				3		18	3		15	ns
t_{ZH}, Output Enable Time to High Level		W		3		18	3		15	ns
t_{ZL}, Output Enable Time to Low Level				3		18	3		15	ns
t_{HZ}, Output Disable Time From High Level		Y		2		12	2		10	ns
t_{LZ}, Output Disable Time From Low Level				1		12	1		10	ns
t_{HZ}, Output Disable Time From High Level		W		2		12	2		10	ns
t_{LZ}, Output Disable Time From Low Level				1		12	1		10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6214-2

National Semiconductor

DM54ALS253/DM74ALS253 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and a non-inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up TRI-STATE Feature

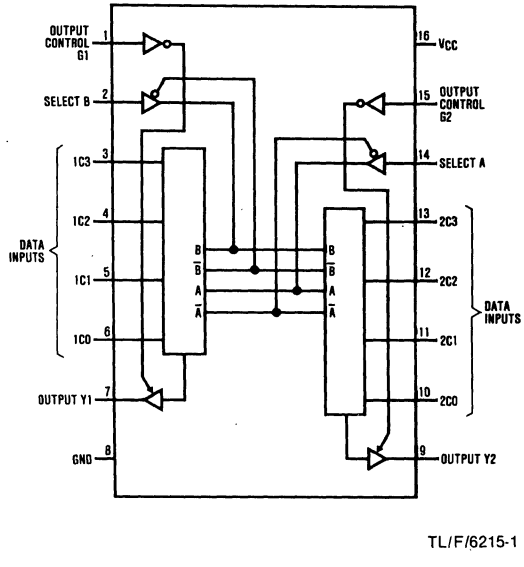
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS253	−55°C to 125°C
DM74ALS253	0° to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6215-1

54ALS253 (J) **74ALS253 (J,N)**

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Recommended Operating Conditions

Parameter	DM54ALS253			DM74ALS253			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = 400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Output High Output Low Disabled			 6.5 6.5 7.5	 12 12 14	mA

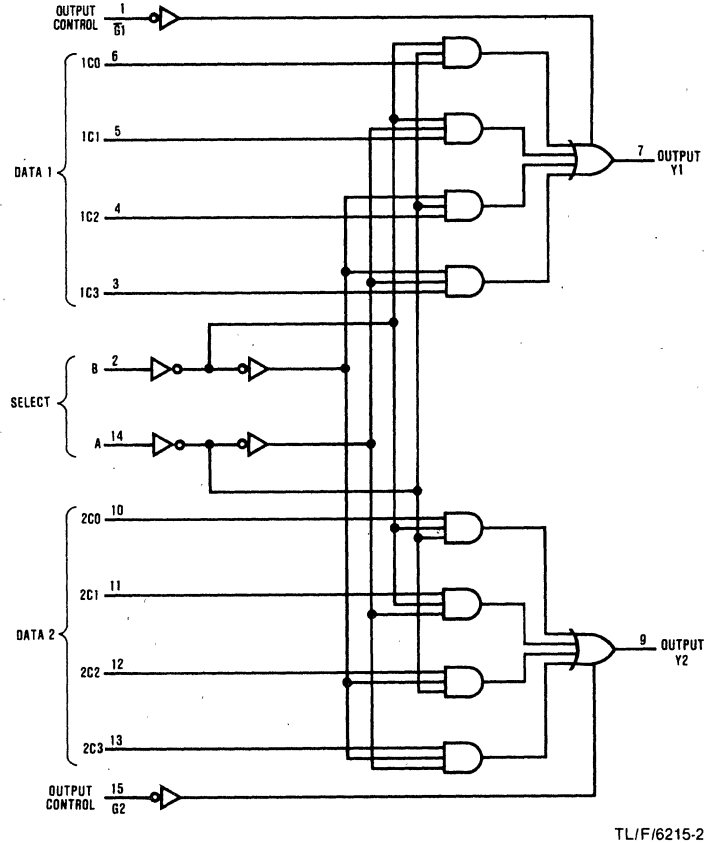
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS253			DM74ALS253			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V C_L = 50 pF R_L = 500 Ω	5		25	5		21	ns
t_{PHL}, High to low Level Output				5		25	5		21	ns
t_{PLH}, Low to high Level Output	Data			2		12	2		10	ns
t_{PHL}, High to low Level Output				3		17	3		14	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y		3		17	3		14	ns
t_{ZL}, Output Enable Time to Low Level				4		19	4		16	ns
t_{HZ}, Output Disable Time From High Level				2		12	2		10	ns
t_{LZ}, Output Disable Time From Low Level				2		16	2		14	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6215-2

National Semiconductor

DM54ALS/DM74ALS257, 258 TRI-STATE® Quad 1-of-2-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The ALS257 presents true data whereas the ALS258 presents inverted data to minimize propagation delay time.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

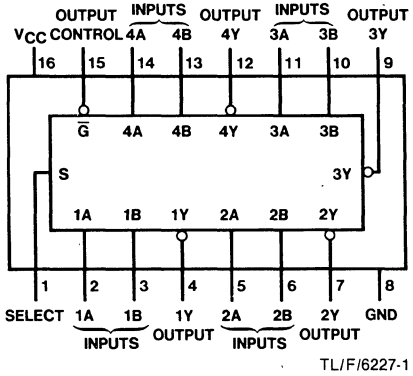
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6227-1

54ALS258 (J) **74ALS258 (J,N)**

Function Table

Inputs				Output Y	
Output Control	Select	A	B	ALS257	ALS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

Recommended Operating Conditions

Parameter	DM54ALS257,258			DM74ALS257,258			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free-air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54ALS I_{OH} = −1mA	2.4	3.2		V
				74ALS I_{OH} = −2.6mA	2.4	3.3		V
			$I_{OH} = -0.4$ mA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
				74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current		$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current		$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current		V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied		$V_{CC} = 5.5V$, $V_{IH} = 2V$, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		$V_{CC} = 5.5V$, $V_{IH} = 2V$, V_O = 0.4V				−20	μA
I_{CCH}	Supply Current	ALS257	V_{CC} = 5.5V, Outputs Open	Outputs High		3	6	mA
		ALS258				2.5	4	mA
I_{CCL}	Supply Current	ALS257		Outputs Low		8	12	mA
		ALS258				7	11	mA
I_{CCZ}	Supply Current	ALS257		Outputs Disabled		9	14	mA
		ALS258				8	13	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS257			DM74ALS257			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Propagation Delay Time, Low to High Level Output	Data	Any Y	$V_{CC} = 4.5$ to $5.5V$ $C_L = 50$ pF $R_L = 500\Omega$	2		12	2		10	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output				3		14	3		12	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output	Select	Any Y		7		21	7		18	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output				6		25	6		22	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Any Y		4		20	4		16	ns
t_{ZL}, Output Enable Time to Low Level				5		22	5		18	ns
t_{HZ}, Output Disable Time from High Level	Output Control	Any Y		2		12	2		10	ns
t_{LZ}, Output Disable Time from Low Level				4		18	4		15	ns

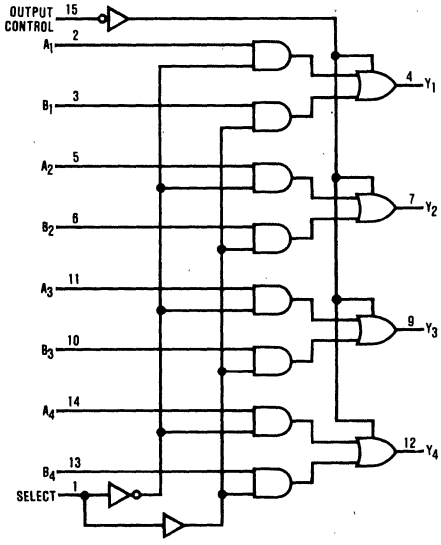
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS258			DM74ALS258			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Propagation Delay Time, Low to High Level Output	Data	Any Y	$V_{CC} = 4.5$ to $5.5V$ $C_L = 50$ pF $R_L = 500\Omega$	2		10	2		8	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output				2		9	2		7	ns
t_{PLH}, Propagation Delay Time, Low to High Level Output	Select	Any Y		8		23	8		20	ns
t_{PHL}, Propagation Delay Time, High to Low Level Output				5		28	5		25	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Any Y		5		20	5		18	ns
t_{ZL}, Output Enable Time to Low Level				5		20	5		18	ns
t_{HZ}, Output Disable Time from High Level	Output Control	Any Y		2		12	2		10	ns
t_{LZ}, Output Disable Time from Low Level				5		20	5		18	ns

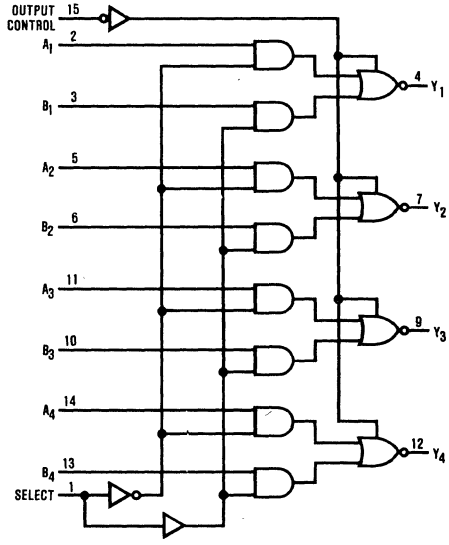
Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams



TL/F/6227-2

54/74ALS257



TL/F/6227-3

54/74ALS258

National Semiconductor

DM54ALS273/DM74ALS273
Octal D-Type Edge-Triggered Flip-Flops With Clear

General Description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input. The outputs are buffer type and are, thus, guaranteed at I_{OL} 12/24 mA.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Buffer-Type Outputs and Improved AC Offer Significant Advantage Over 'LS273.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-For-Pin Compatible with 'LS273.

Absolute Maximum Ratings (Note 1)

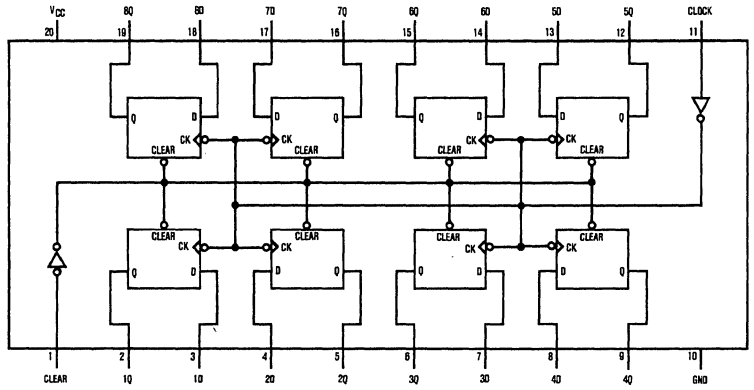
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS273	−55°C to 125°C
DM74ALS273	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6216-1

54ALS273 (J) **74ALS273 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS273			DM74ALS273			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	16.5			14			ns
	Low	16.5			14			ns
Width of Clear Pulse, T_W	Low	10			10			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
	Clear Inactive	15↑			15↑			ns
Data Hold Time, T_H		0↑			0↑			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1$mA	2.4	3.2		V
			74ALS $I_{OH} = -2.6$mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	20	mA
			Outputs Low		19	29	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS273			DM74ALS273			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF.	30			35			MHz
T_{PHL}	Clear	Any Q		4		21	4		18	ns
T_{PLH}	Clock	Any Q		2		16	2		12	ns
T_{PHL}				3		17	3		15	ns

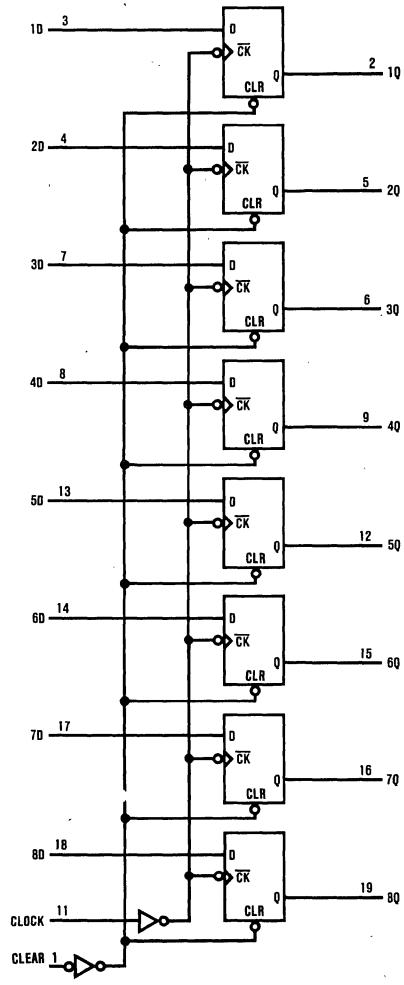
Note 1: See Section 1 for test waveforms and output load.

Function Table (Each Flip-Flop)

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6216-2

National Semiconductor

PRELIMINARY

DM54ALS299/DM74ALS299 TRI-STATE® 8-Bit Universal Shift/Storage Registers

General Description

This Schottky TTL 8-bit universal register features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  - Hold (Store)
  - Shift Left
  - Shift Right
  - Load Data
- Operates with outputs enabled or at Hi-Z
- TRI-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Applications:
  - Stacked or push-down registers
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart

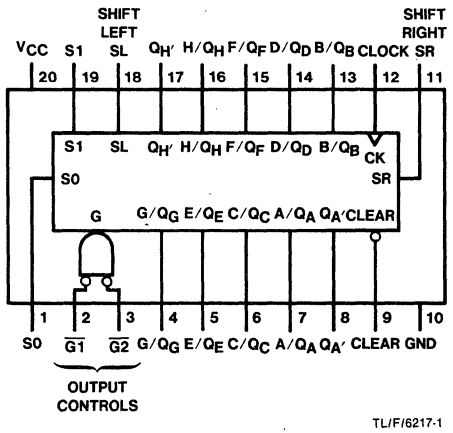
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6217-1

DM54ALS299 (J) **DM74ALS299 (N)**

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

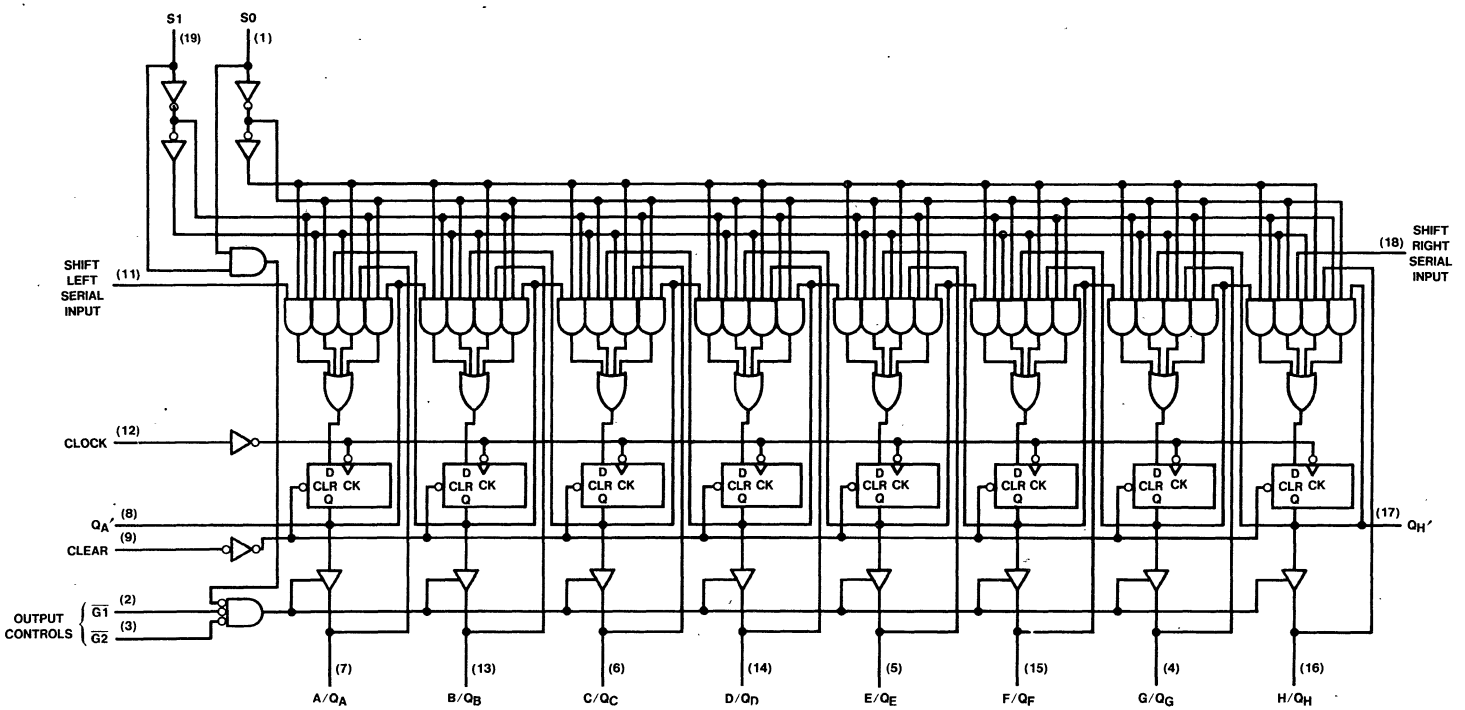
Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G}1$†	$\overline{G}2$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Logic Diagram



TL/F/6217-2

Recommended Operating Conditions

Symbol	Parameter			DM54ALS299			DM74ALS299			Units
				Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
I_{OH}	High Level Output Current	Q_A' or Q_H'				−0.4			−0.4	mA
		Q_A thru Q_H				−1			−2.6	mA
I_{OL}	Low Level Output Current	Q_A' or Q_H'				4			8	mA
		Q_A thru Q_H				12			24	mA
f_{CLOCK}	Clock Frequency			0		25	0		30	MHz
t_W	Pulse Width	Clock High or Low		20			16.5			ns
		$\overline{\text{Clear}}$ Low		10			10			ns
t_{SU}	Data Set-Up Time	Select		25↑			20↑			ns
		Serial or Parallel Data	High	18↑			16↑			ns
			Low	7↑			6↑			ns
		CLR Inactive		15↑			15↑			ns
t_H	Data Hold Time			0↑			0↑			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC} − 2			V
		I_{OH} = Max	Q_A thru Q_H	2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, Q_A' or Q_H'	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
		V_{CC} = 4.5V, Q_A or Q_H	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	S0, S1, SR, SL			−0.2	mA
			All Others			−0.1	mA
I_O	Output Drive Current (V_{CC} = 5.5V)	V_O = 2.25V	Q_A' or Q_H'	−15		−70	mA
			Q_A thru Q_H	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		15	28	mA
			Outputs Low		22	38	mA
			Disabled		23	40	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	DM54ALS299			DM74ALS299			Units
				Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
f_{MAX}	Maximum Clock Frequency (Note 2)			25			30			MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q_A' or Q_H'	5		20	5		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			8		21	8		18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q_A' or Q_H'	6		29	6		22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clock	Q_A thru Q_H	4		15	4		13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			7		25	7		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q_A thru Q_H	6		29	6		22	ns
t_{PZH}	Output Enable Time to High Level	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H	6		21	6		16	ns
t_{PZL}	Output Enable Time to Low Level			8		26	8		22	ns
t_{PHZ}	Output Disable Time from High Level	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H	1		10	1		8	ns
t_{PLZ}	Output Disable Time from Low Level			5		23	5		15	ns
t_{PZH}	Output Enable Time to High Level	S0, S1	Q_A thru Q_H	7		21	7		17	ns
t_{PZL}	Output Enable Time to Low Level			8		26	8		22	ns
t_{PHZ}	Output Disable Time from High Level	S0, S1	Q_A thru Q_H	1		16	1		12	ns
t_{PLZ}	Output Disable Time from Low Level			3		20	3		15	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: For testing f_{MAX}, all outputs are loaded simultaneously.

Note 3: All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

National Semiconductor

DM54ALS352/DM74ALS352 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and an inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with the LS Family counterpart.
- Improved output transient handling capability.

Absolute Maximum Ratings (Note 1)

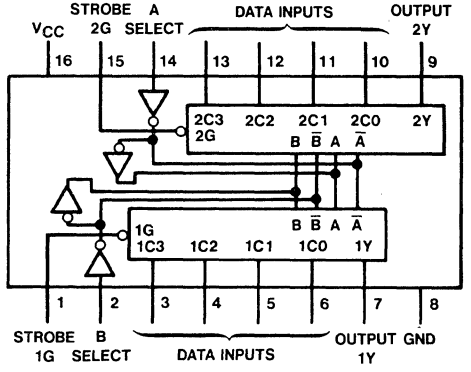
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS352	−55°C to 125°C
DM74ALS352	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature	
(Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6218-1

54ALS352 (J) 74ALS352 (J,N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS352			DM74ALS352			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 2)			6.5	10	mA

Note 1: See Section 1 for test waveforms and output load.

Note 2: I_{CC} is measured with data and select inputs at 4.5V, G inputs grounded and outputs open.

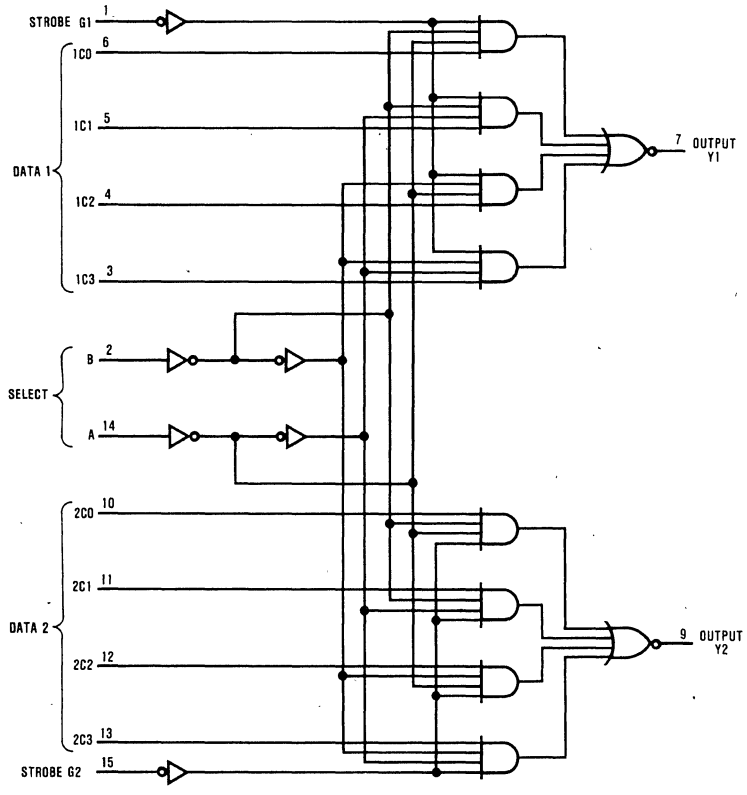
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS352			DM74ALS352			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	5		28	5		24	ns
t_{PHL}, High to low Level Output				5		24	5		21	ns
t_{PLH}, Low to high Level Output	Data			3		21	3		18	ns
t_{PHL}, High to low Level Output				2		15	2		13	ns
t_{PLH}, Low to high Level Output	Strobe			4		22	4		18	ns
t_{PHL}, High to low Level Output				4		24	4		20	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6218-2

National Semiconductor

DM54ALS353/DM74ALS353 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and an inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with LS Family counterpart.
- Improved output transient handling capability.
- Output Control circuitry incorporates power-up TRI-STATE feature.

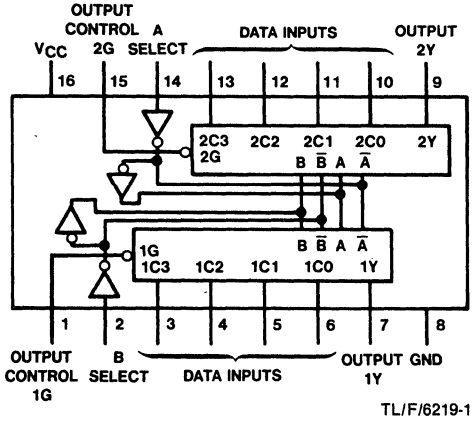
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS353	−55°C to +125°C
DM74ALS353	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6219-1

54ALS353 (J) 74ALS353 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care
Z = High Impedance State

Recommended Operating Conditions

Parameter	DM54ALS353			DM74ALS353			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	All Inputs at 4.5V		8	13	mA
			All Inputs at GND		7	12	

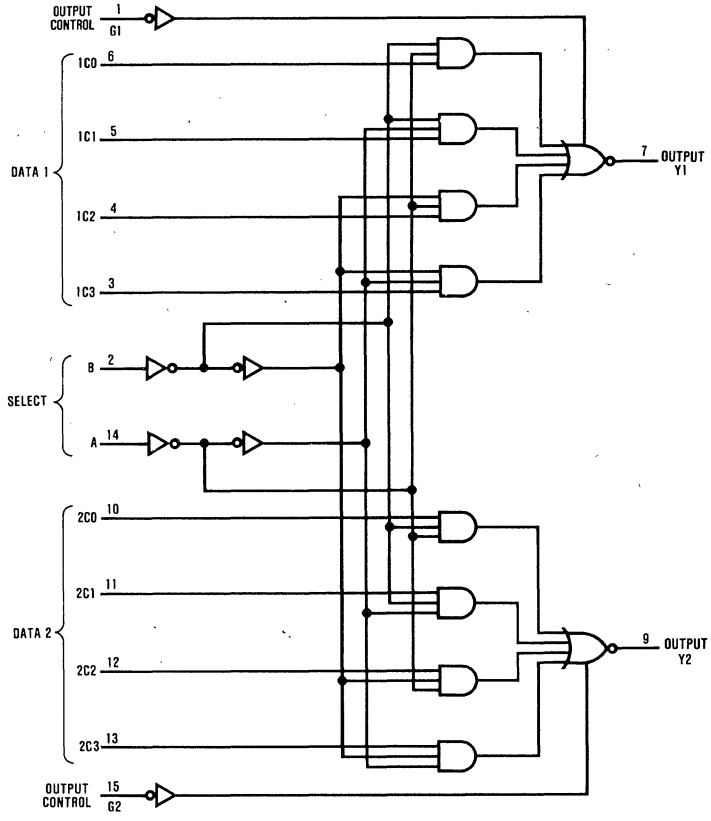
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS353			DM74ALS353			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	5		28	5		24	ns
t_{PHL}, High to low Level Output				5		24	5		21	ns
t_{PLH}, Low to high Level Output	Data			4		21	4		18	ns
t_{PHL}, High to low Level Output				3		15	3		13	ns
t_{ZH}, Output Enable Time to High Level	Output Control			3		15	3		13	ns
t_{ZL}, Output Enable Time to Low Level				3		19	2		16	ns
t_{HZ}, Output Disable Time From High Level				2		12	2		10	ns
t_{LZ}, Output Disable Time From Low Level				2		16	2		14	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6219-2

National Semiconductor

DM54ALS373/DM74ALS373 Octal D-Type Transparent Latches

General Description

These 8-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS373 at Approximately Half the Power.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

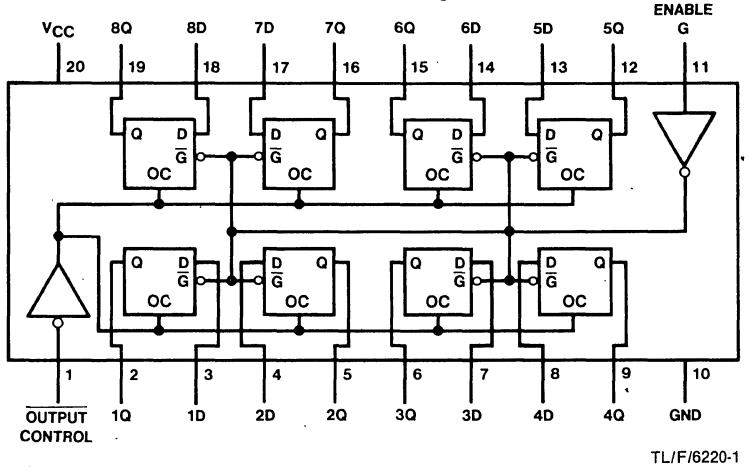
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS373	−55°C to 125°C
DM74ALS373	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6220-1

54ALS373 (J) 74ALS373 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS373			DM74ALS373			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	10			10			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$ $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$ $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$ $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS $V_O = 2.25V$	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$ $V_{IH} = 2V$ $V_O = 2.7V$				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$ $V_{IH} = 2V$ $V_O = 0.4V$				−20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		9	16	mA
			Outputs Low		16	25	mA
			Outputs Disabled		17	27	mA

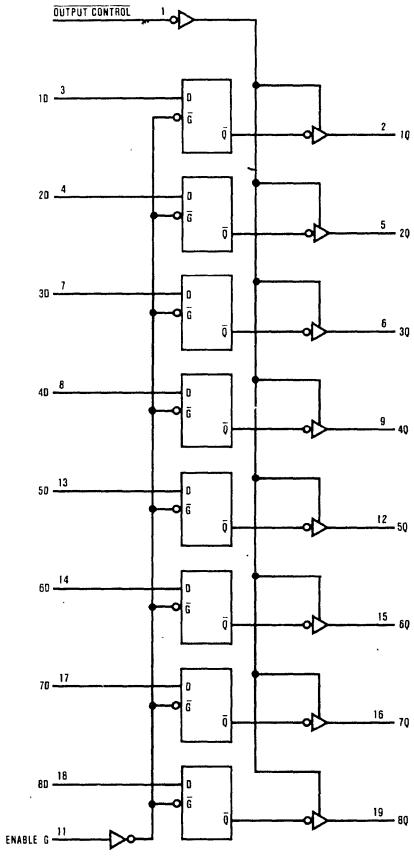
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS373			DM74ALS373			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	2		14	2		12	ns
T_{PHL}				4		19	4		16	ns
T_{PLH}	Enable	Any Q		6		26	6		22	ns
T_{PHL}				7		27	7		23	ns
T_{PZH}	Output Control	Any Q		5		24	5		20	ns
T_{PZL}				6		22	6		18	ns
T_{PHZ}				2		16	2		12	ns
T_{PLZ}				2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6220-2

Function Table

$\overline{\text{Output Control}}$	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

2

National Semiconductor

DM54ALS374/DM74ALS374 Octal D-Type-Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE® output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS374 at Approximately Half the Power.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

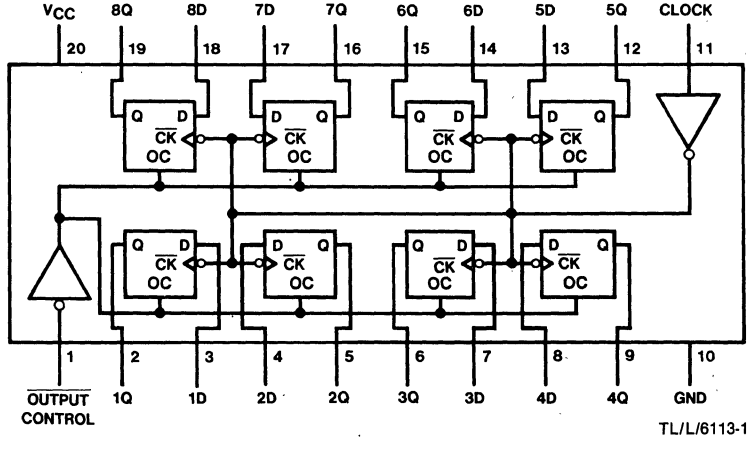
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS374	−55°C to 125°C
DM74ALS374	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/L/6113-1

54ALS374 (J) 74ALS374 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS374			DM74ALS374			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	16.5			14			ns
	Low	16.5			14			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS $V_O = 2.25V$	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 2.7V$				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 0.4V$				−20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		11	19	mA
			Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

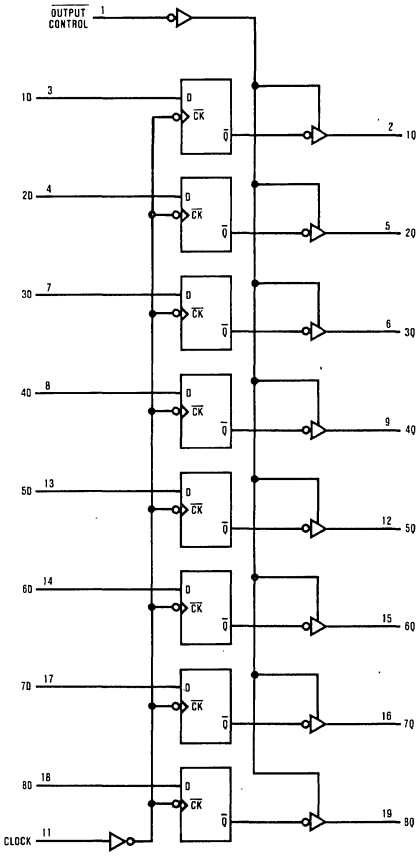
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS374			DM74ALS374			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\ \Omega$ $C_L = 50$ pF	30			35			MHz
T_{PLH}	Clock	Any Q		3		15	3		12	ns
T_{PHL}				5		18	5		16	ns
T_{PZH}	Output Control	Any Q		5		19	5		17	ns
T_{PZL}				7		20	7		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				3		24	3		18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/L/6113-2

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

2

National Semiconductor

DM54/DM74ALS465A, DM54/DM74ALS466A, DM54/DM74ALS467A, DM54/DM74ALS468A Octal TRI-STATE® Bus Drivers

General Description

These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers on the ALS467A and ALS468A, and one common gating control for all eight buffers on the ALS465A and ALS466A. All control inputs are active low enabling. The buffers on the ALS465A and ALS467A are non-inverting and the buffers on the ALS466A and ALS468A are inverting. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart and the DM71/81LS95, 96, 97, 98
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading

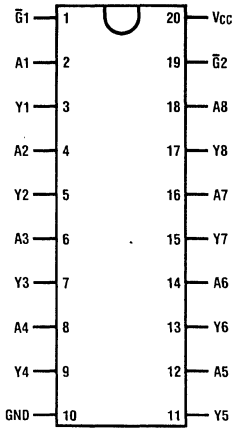
Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Output Voltage (Disabled)	5.5V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package

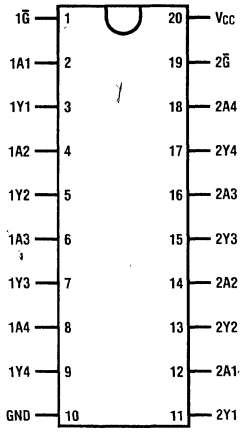


TOP VIEW

TL/F/6221-1

DM54ALS465A (J)
DM54ALS466A (J)
DM74ALS465A (J, N)
DM74ALS466A (J, N)

Dual-In-Line Package



TOP VIEW

TL/F/6221-2

DM54ALS467A (J)
DM54ALS468A (J)
DM74ALS467A (J, N)
DM74ALS468A (J, N)

Recommended Operating Conditions

Symbol	Parameter	DM54ALS465A DM54ALS466A DM54ALS467A DM54ALS468A			DM74ALS465A DM74ALS466A DM74ALS467A DM74ALS468A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS465A DM54ALS466A DM54ALS467A DM54ALS468A			DM74ALS465A DM74ALS466A DM74ALS467A DM74ALS468A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA

Electrical Characteristics (Continued) over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54ALS465A DM54ALS466A DM54ALS467A DM54ALS468A			DM74ALS465A DM74ALS466A DM74ALS467A DM74ALS468A			Units
			Min	Typ	Max	Min	Typ	Max	
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS465A							
		Outputs High		11	21		11	6	mA
		Outputs Low		9	33		9	8	
		Outputs TRI-STATE		23	8		23	33	
		V_{CC} = 5.5V, ALS466A							
		Outputs High		7	5		7	10	mA
		Outputs Low		6	9		6	4	
		Outputs TRI-STATE		9	32		9	7	
		V_{CC} = 5.5V, ALS467A							
		Outputs High		11	21		11	6	mA
		Outputs Low		9	33		9	8	
		Outputs TRI-STATE		23	8		23	33	
		V_{CC} = 5.5V, ALS468A							
		Outputs High		7	5		7	10	mA
		Outputs Low		6	9		6	4	
		Outputs TRI-STATE		9	32		9	7	

'ALS465A and 'ALS467A Switching Characteristics

over recommended operating free air temperature range

Parameter	From (Input)	To (Output)	Conditions	DM54ALS465A DM54ALS467A			DM74ALS465A DM74ALS467A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	2		16	2		13	ns
t_{PHL}				4		15	4		12	ns
t_{PZH}	$\overline{G}$	Any Y		4		27	4		23	ns
t_{PZL}				5		30	5		25	ns
t_{PHZ}	$\overline{G}$	Any Y		2		12	2		10	ns
t_{PLZ}				3		21	3		18	ns

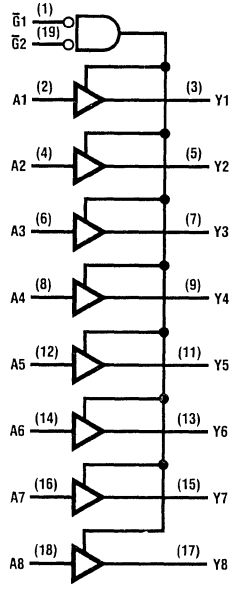
'ALS466A and 'ALS468A Switching Characteristics

over recommended operating free air temperature range

Parameter	From (Input)	To (Output)	Conditions	DM54ALS466A DM54ALS468A			DM74ALS466A DM74ALS468A			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	3		14	3		12	ns
t_{PHL}				2		11	2		9	ns
t_{PZH}	$\overline{G}$	Any Y		4		21	4		16	ns
t_{PZL}				7		25	7		23	ns
t_{PHZ}	$\overline{G}$	Any Y		2		12	2		10	ns
t_{PLZ}				2		20	2		17	ns

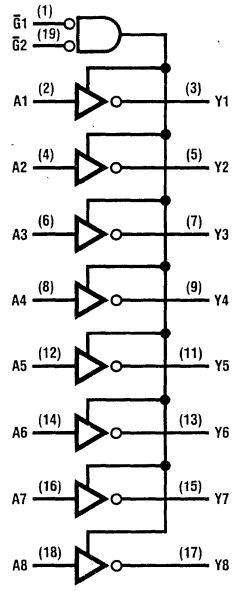
Logic Diagrams

ALS465A



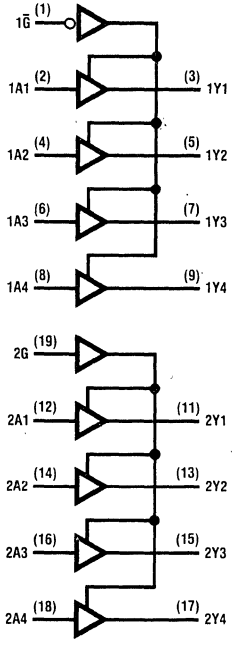
TL/F/6221-3

ALS466A



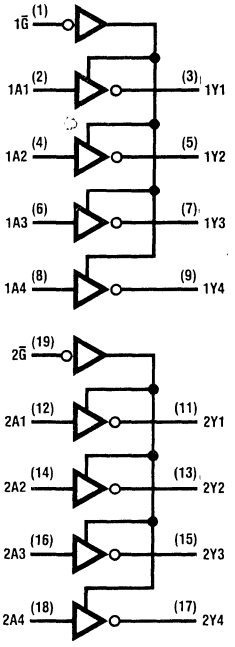
TL/F/6221-4

ALS467A



TL/F/6221-5

ALS468A



TL/F/6221-6

National Semiconductor

DM54ALS/DM74ALS518,519,520,521,522 8-Bit Comparators

General Description

These comparators perform an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the $\overline{EN}$ input produces the output A = B on the ALS518 & 519 and the output $\overline{A = B}$ on the ALS520, 521 & 522. The ALS520 & 521 have totem pole outputs, while the ALS518, 519 & 522 have open collector outputs for wire AND cascading. Additionally, the ALS518, 520 & 522 are provided with B input pull up termination resistors for analog or switch data.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

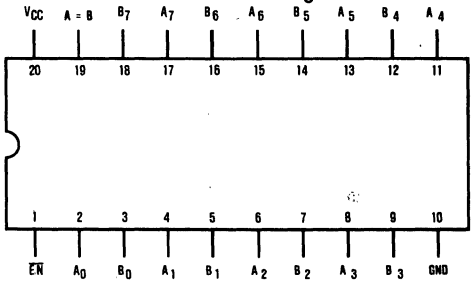
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

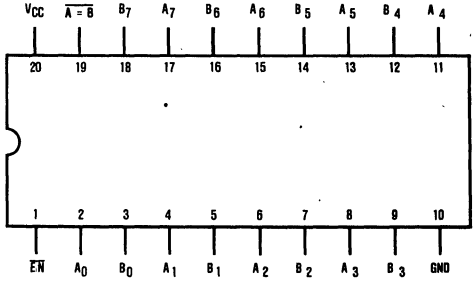
Dual-In-Line Package



TL/F/6114-1

54ALS518 (J) 74ALS518 (J,N)
54ALS519 (J) 74ALS519 (J,N)

Dual-In-Line Package



TL/F/6114-2

54ALS520 (J) 74ALS520 (J,N)
54ALS521 (J) 74ALS521 (J,N)
54ALS522 (J) 74ALS522 (J,N)

Function Tables

ALS518,519

Inputs		Output
$\overline{EN}$	Data	A = B
L	A=B	H
L	A≠B	L
H	X	L

H = High Logic Level; L = Low Logic Level; X = Don't Care

ALS520,521,522

Inputs		Output
$\overline{EN}$	Data	$\overline{A = B}$
L	A=B	L
L	A≠B	H
H	X	H

H = High Logic Level; L = Low Logic Level; X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS 518,519,520,521,522			DM74ALS 518,519,520,521,522			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH} (ALS518,519,522)			5.5			5.5	V
High Level Output Current, I_{OH} (ALS520,521)			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$	ALS520, 521	$V_{CC} - 2$			V
		I_{OH} = Max		2.4	3.2		V
I_{OH}	High Level Output Current	$V_{CC} = 5.5V$, $V_{OH} = 5.5V$	ALS518, 519, 522			0.1	mA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS, $I_{OL} = 12$ mA		0.25	0.4	V
			74ALS, $I_{OL} = 24$ mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$	$V_{IH} = 5.5V$, B Input ALS518, 520, 522			0.1	mA
			$V_{IH} = 7V$, All Others				
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$	All Others			20	μA
			B Input ALS518, 520, 522			−200	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$	B Input ALS518, 520, 522			−0.6	μA
			All Others			−0.1	μA
I_O	Output Drive Current	$V_{CC} = 5.5V$ ALS520 ALS521	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ (Note 1)	ALS518, ALS519, ALS522		11	17	mA
			ALS520, ALS521		12	19	mA

Note 1: I_{CC} is measured with $\overline{G}$ grounded, A and B inputs at 4.5V and outputs open.

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From Input	To Output	Conditions	DM74ALS 518,519			DM54ALS 518,519			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$ or A=B	V_{CC} = 4.5V to 5.5V, C_L = 50pF, R_L = 667Ω	15		37	15		33	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				3		18	3		15	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			15		37	15		33	
T_{PHL}, Propagation Delay Time, High to low Level Output				3		18	3		15	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From Input	To Output	Conditions	DM54ALS 520,521			DM74ALS 520,521			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$	V_{CC} = 4.5V to 5.5V, C_L = 50pF, R_L = 500Ω	3		16	3		12	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				5		25	5		20	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			2		15	2		12	
T_{PHL}, Propagation Delay Time, High to low Level Output				5		23	5		22	

Switching Characteristics over recommended operating free air temperature range (Note 1).

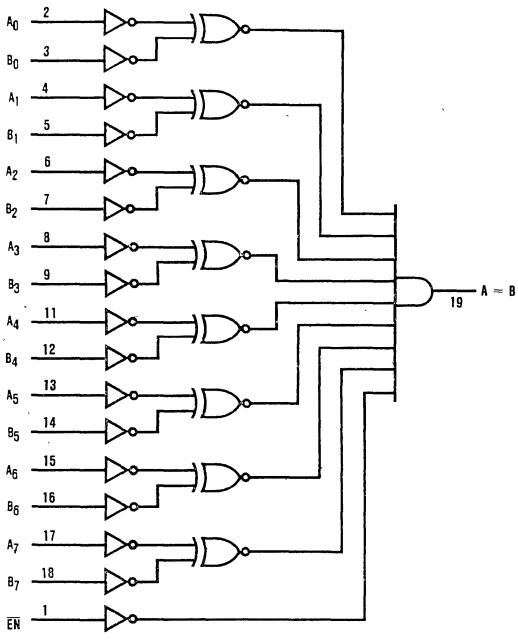
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From Input	To Output	Conditions	DM54ALS 522			DM74ALS 522			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$ or A=B	V_{CC} = 4.5V to 5.5V, C_L = 50pF, R_L = 667Ω	10		30	10		25	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				5		25	5		23	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			8		30	8		25	
T_{PHL}, Propagation Delay Time, High to low Level Output				8		30	8		30	

Note 1: See Section 1 for test waveforms and output load.

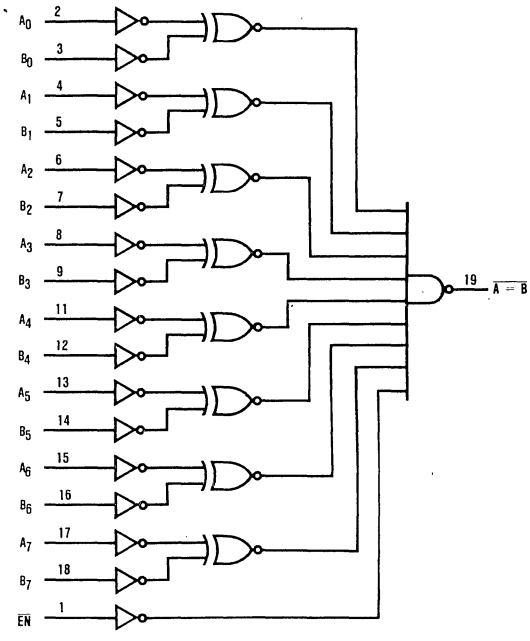
Logic Diagrams

ALS518/519



TL/F/6114-3

ALS520/521/522



TL/F/6114-4

National Semiconductor

DM54ALS533/DM74ALS533
Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS533 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

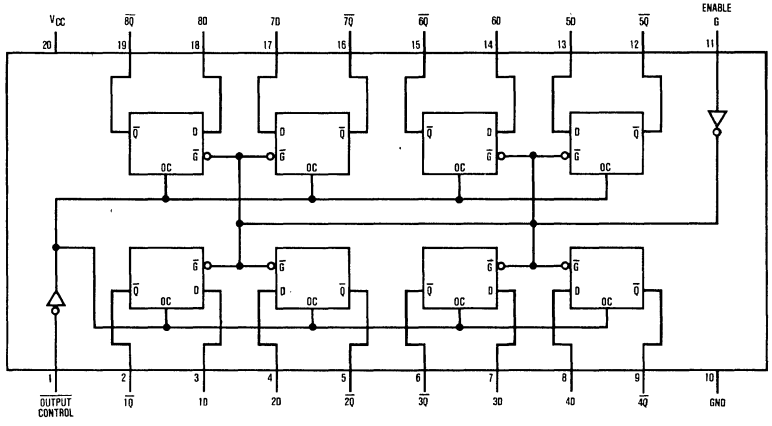
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS533	−55°C to 125°C
DM74ALS533	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6222-1

54ALS533 (J) 74ALS533 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS533			DM74ALS533			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T_{SU}	15↓			15↓			ns
Data Hold Time, T_H	7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	17	mA
			Outputs Low		17	26	mA
			Outputs Disabled		18.5	28	mA

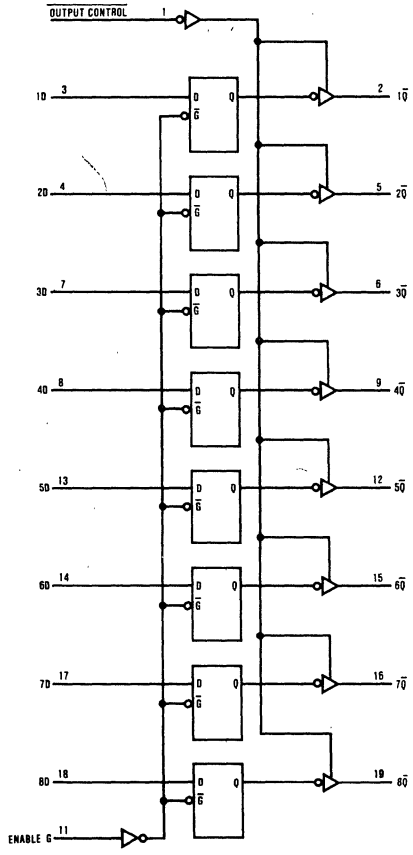
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS533			DM74ALS533			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	4		24	4		19	ns
T_{PHL}				4		14	4		13	ns
T_{PLH}	Enable	Any $\overline{Q}$		5		28	5		23	ns
T_{PHL}				4		21	4		18	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		19	4		17	ns
T_{PZL}				4		20	4		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				3		22	3		16	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6222-2

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low state, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54ALS534/DM74ALS534 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings (Note 1)

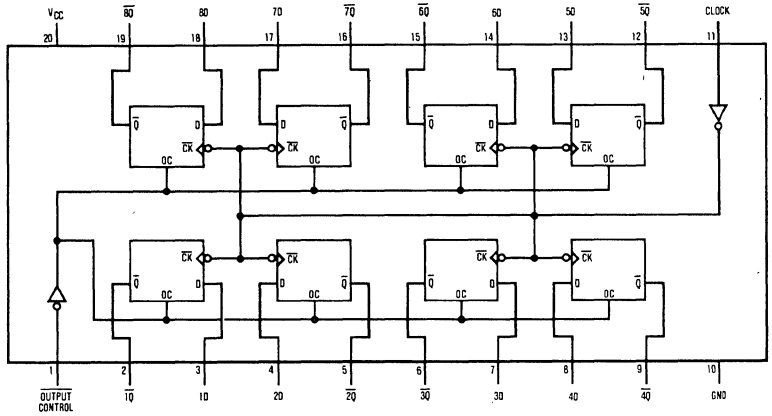
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS534	−55°C to 125°C
DM74ALS534	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/L/6223-1

54ALS534 (J) 74ALS534 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS534			DM74ALS534			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	16.5			14			ns
	Low	16.5			14			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V	All Others			−0.2	mA
			CLK, OC			−0.1	
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	19	mA
			Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

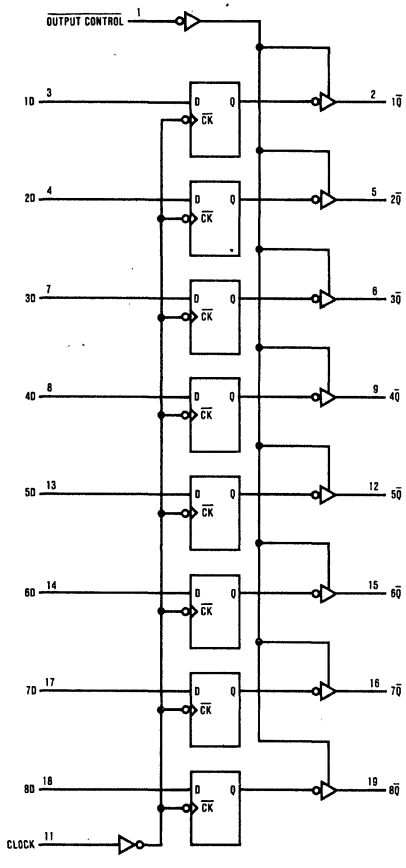
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS534			DM74ALS534			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V $R_L = 500\ \Omega$ C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any $\overline{Q}$		3		15	3		12	ns
T_{PHL}				5		18	5		16	ns
T_{PZH}	Output Control	Any $\overline{Q}$		5		19	5		17	ns
T_{PZL}				7		20	7		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				2		16	2		14	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/L/6223-2

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54ALS563/DM74ALS563 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS563 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings (Note 1)

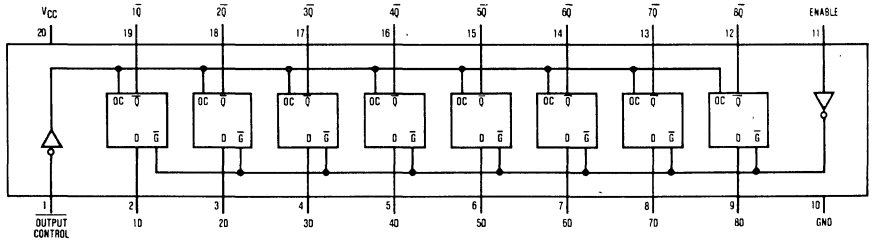
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS563	−55°C to 125°C
DM74ALS563	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6225-1

DM54ALS563 (J) DM74ALS563 (J, N)

Recommended Operating Conditions

Parameter	DM54ALS563			DM74ALS563			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	10↓			10↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		10	17	mA
			Outputs Low		15	24	mA
			Outputs Disabled		15.5	27	mA

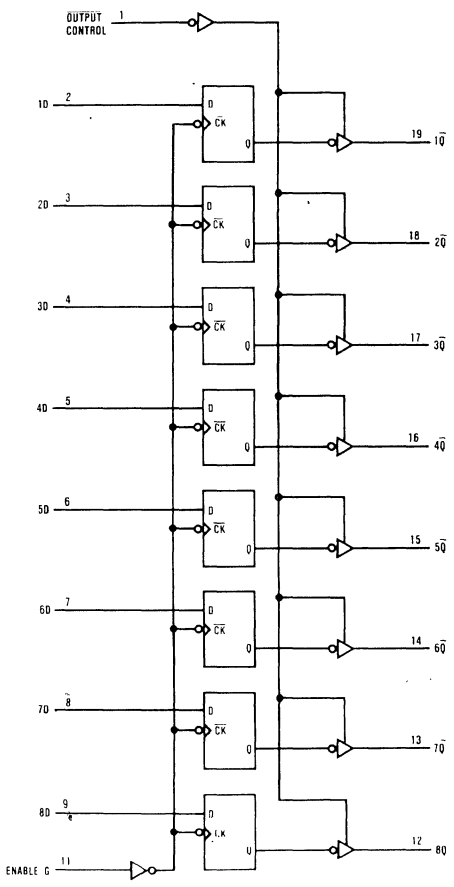
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS563			DM74ALS563			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\bar{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		21	3		18	ns
T_{PHL}				3		15	3		14	ns
T_{PLH}	Enable	Any $\bar{Q}$		8		29	8		22	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any $\bar{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6225-2

Function Table

Output Control	Enable G	D	Output $\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\bar{Q}_0$ = Previous Condition of $\bar{Q}$

National Semiconductor

DM54ALS564/DM74ALS564 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS564 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

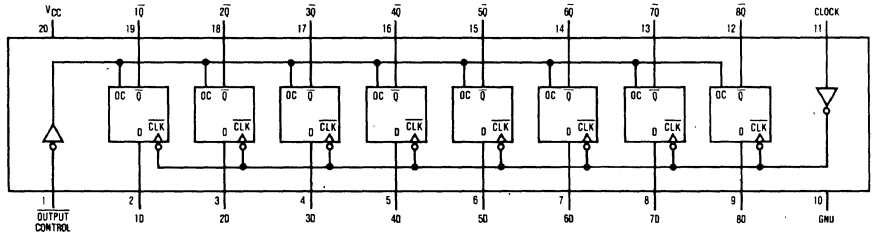
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS564	−55°C to 125°C
DM74ALS564	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6225-1

DM54ALS564 (J) DM74ALS564 (J, N)

Recommended Operating Conditions

Parameter		DM54ALS564			DM74ALS564			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		25	0		30	MHz
Width of Clock Pulse, T_W	High	16.5			14			ns
	Low	16.5			14			ns
Data Setup Time, T_{SU}		15↑			15↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

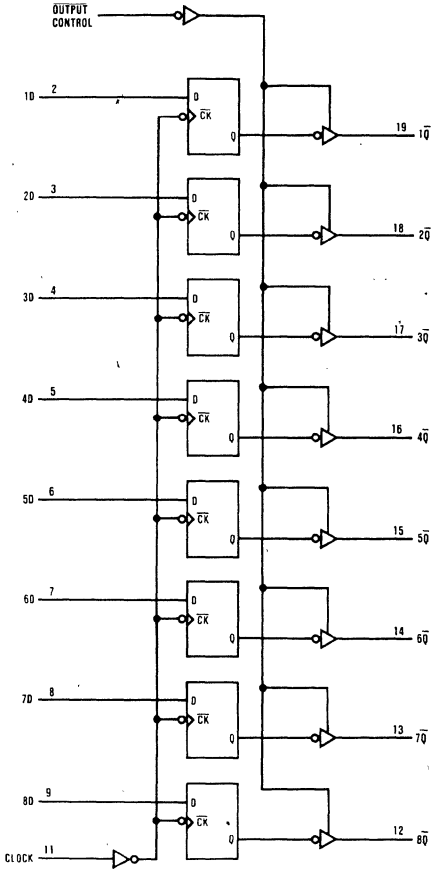
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10.5	17	mA
			Outputs Low		15	24	mA
			Outputs Disabled		16	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS564			DM74ALS564			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Clock	Any $\overline{Q}$		4		15	4		14	ns
T_{PHL}				4		15	4		14	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6225-2

Function Table

Output Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54ALS573/DM74ALS573 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS573 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with LS373.
- Improved AC Performance Over LS373 at Approximately Half the Power.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

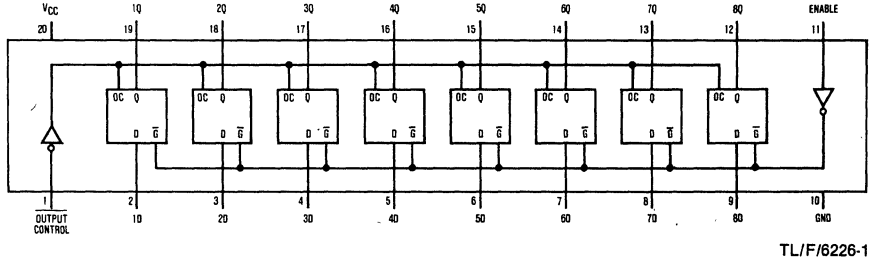
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS573	−55°C to 125°C
DM74ALS573	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6226-1

54ALS573 (J) 74ALS573 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS573			DM74ALS573			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS $V_O = 2.25V$	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 2.7V$				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 0.4V$				−20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		10	17	mA
			Outputs Low		15	24	mA
			Outputs Disabled		15.5	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS573			DM74ALS573			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	2		15	2		14	ns
T_{PHL}				2		15	2		14	ns
T_{PLH}	Enable	Any Q		8		25	8		20	ns
T_{PHL}				8		22	8		19	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				2		15	2		12	ns

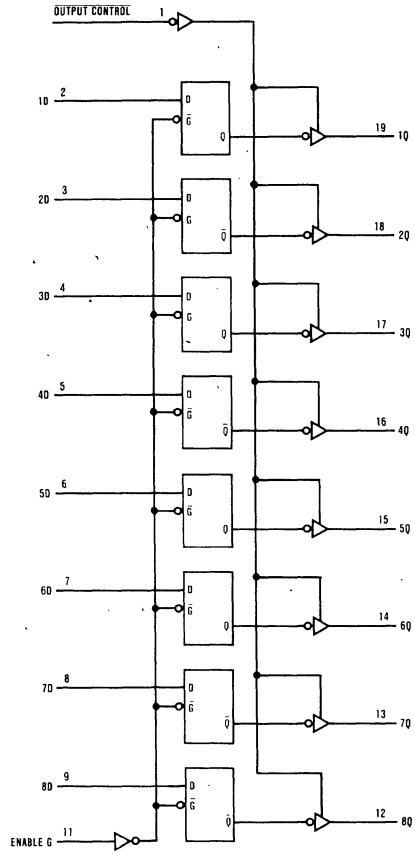
Note 1: See Section 1 for test waveforms and output load.

Function Table

$\overline{\text{Output Control}}$	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6226-2

National Semiconductor

DM54ALS574/DM74ALS574 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with LS374.
- Improved AC Performance Over LS374 at Approximately Half the Power.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

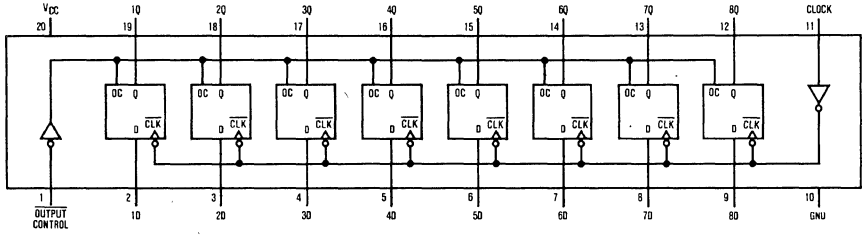
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS574	−55°C to 125°C
DM74ALS574	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/L/6110-1

54ALS574 (J) 74ALS574 (J,N)

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

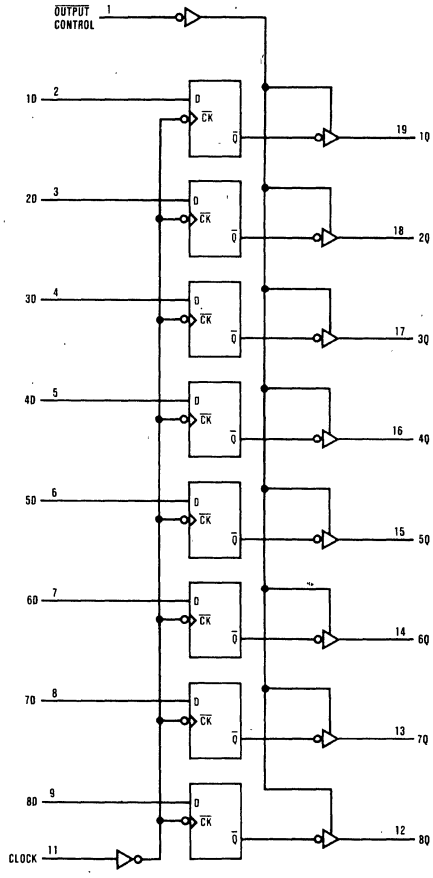
L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54ALS574			DM74ALS574			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	16.5			14			ns
	Low	16.5			14			ns
Data Setup Time, T_{SU}		15↑			15↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Logic Diagram



TL/L/6110-2

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS $V_O = 2.25V$	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 2.7V$				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 0.4V$				−20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		11	18	mA
			Outputs Low		17	27	mA
			Outputs Disabled		17	28	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS574			DM74ALS574			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\ \Omega$ $C_L = 50\ pF$	30			35			MHz
T_{PLH}	Clock	Any Q		4		15	4		14	ns
T_{PHL}				4		15	4		14	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}	Output Control	Any Q		2		12	2		10	ns
T_{PLZ}				2		15	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS576/DM74ALS576 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS576 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

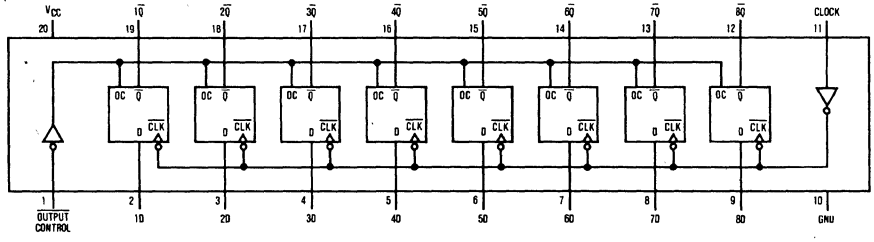
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS576	−55°C to 125°C
DM74ALS576	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6228-1

54ALS576 (J) 74ALS576 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS576			DM74ALS576			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		25	0		30	MHz
Width of Clock Pulse, T_W	High	20			16.5			ns
	Low	20			16.5			ns
Data Setup Time, T_{SU}		15↑			15↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	17	mA
			Outputs Low		15	24	mA
			Outputs Disabled		16	27	mA

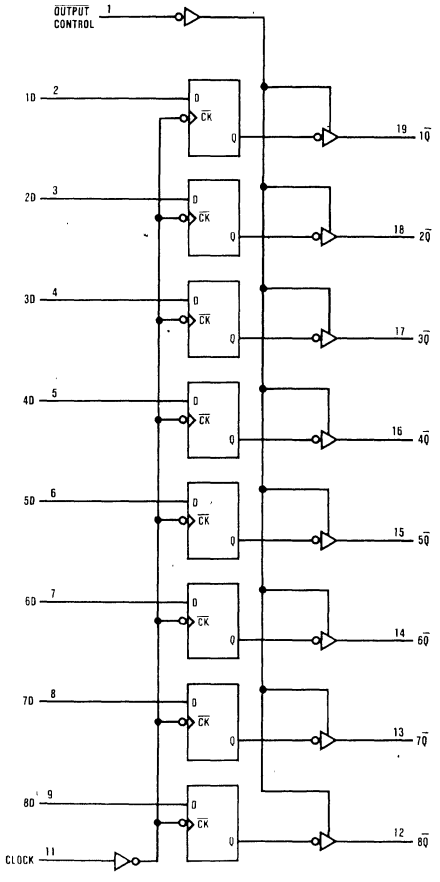
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS576			DM74ALS576			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Clock	Any $\bar{Q}$		4		15	4		14	ns
T_{PHL}				4		15	4		14	ns
T_{PZH}	Output Control	Any $\bar{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6228-2

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of $\bar{Q}$

2

National Semiconductor

DM54ALS580/DM74ALS580 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS580 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

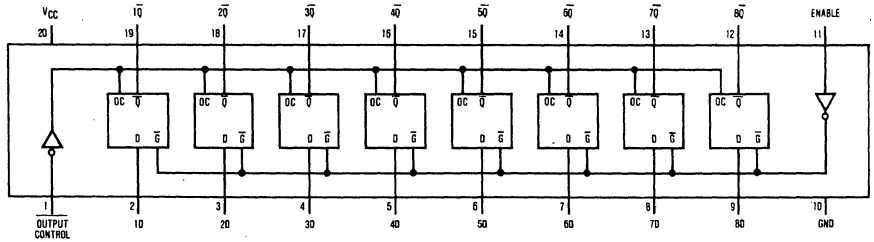
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS580	−55°C to 125°C
DM74ALS580	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6229-1

54ALS580 (J) 74ALS580 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS580			DM74ALS580			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	10↓			10↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, $V_{IL} = V_{IL}$ MAX	54ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	17	mA
			Outputs Low		15	24	mA
			Outputs Disabled		15.5	27	mA

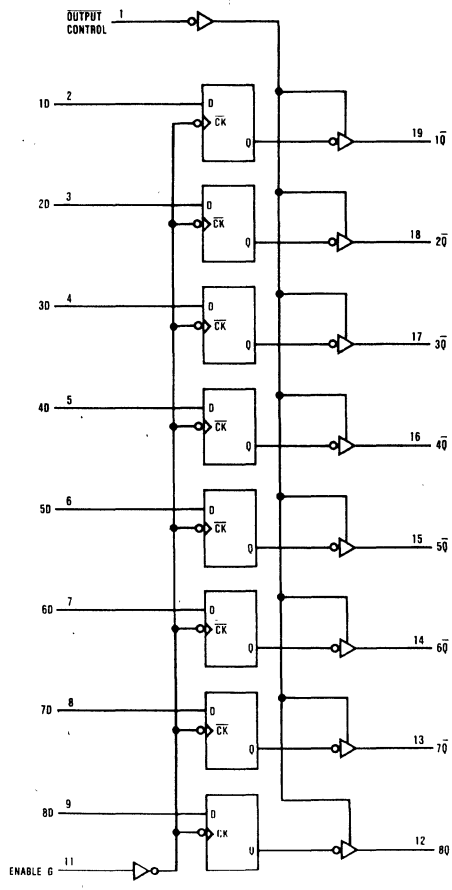
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS580			DM74ALS580			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\bar{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		21	3		18	ns
T_{PHL}				3		15	3		14	ns
T_{PLH}	Enable	Any $\bar{Q}$		8		29	8		22	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any $\bar{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6229-2

Function Table

Output Control	Enable G	D	Output $\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\bar{Q}_0$ = Previous Condition of $\bar{Q}$

National Semiconductor

DM54ALS620A/DM74ALS620A Octal TRI-STATE® Bus Transceiver

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as an octal bus transceiver. It is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives the ALS620A the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Features

- Advanced oxide-isolated, ion implanted Schottky process
- TRI-STATE outputs on A and B buses
- Local bus-latch capability
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

Absolute Maximum Ratings (Note 1)

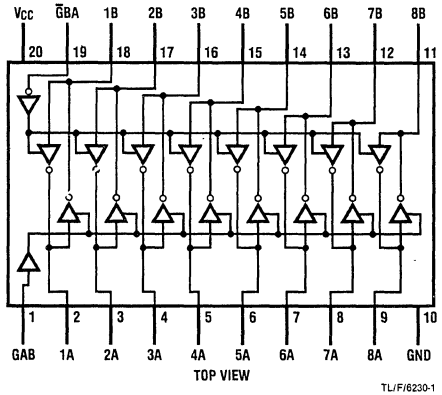
Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagrams

Dual-In-Line Package



54ALS620A (J) **74ALS620A (J, N)**

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ Data to A Bus
H	H	$\overline{A}$ Data to B Bus
H	L	Hi-Z
L	H	$\overline{B}$ Data to A Bus $\overline{A}$ Data to B Bus

Recommended Operating Conditions

Symbol	Parameter	DM54ALS620A			DM74ALS620A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS620A-1 Option Only						48	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

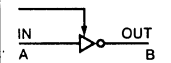
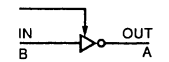
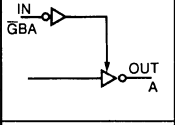
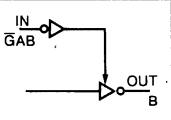
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS620A			DM74ALS620A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3$ mA		2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5V$, I_{OH} = Max		2			2			V
		$I_{OH} = -0.4$ mA, $V_{OL} = 4.5V$ to 5.5V		$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	V
			For 74ALS-1 Option Only $I_{OL} = 48$ mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	A or B Ports			20			20	mA
			Control Inputs			20			20	mA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	A or B Ports			−0.1			−0.1	mA
			Control Inputs			−0.1			−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Output High		24	39		24	34	mA
			Output Low		25	49		31	44	mA
			TRI-STATE		27	52		33	47	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS620A			DM74ALS620A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output		2		12	2		10	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		12	2		10	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		2		12	2		10	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		12	2		10	ns
t_{PZL}	Output Enable Time to Low Level		5		31	5		25	ns
t_{PZH}	Output Enable Time to High Level		3		23	3		17	ns
t_{PLZ}	Output Disable Time from Low Level		3		22	3		18	ns
t_{PHZ}	Output Disable Time from High Level		2		14	2		12	ns
t_{PZL}	Output Enable Time to Low Level		5		31	5		25	ns
t_{PZH}	Output Enable Time to High Level		3		23	3		18	ns
t_{PLZ}	Output Disable Time from Low Level		3		22	3		18	ns
t_{PHZ}	Output Disable Time from High Level		2		14	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

National Semiconductor

DM54ALS621A/DM74ALS621A, DM54ALS622A/DM74ALS622A Octal Open Collector Output Bus Transceivers

General Description

These advanced low power Schottky devices contain 8 pairs of logic elements configured as octal bus transceivers. They are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives the ALS621A and ALS622A the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}(Min) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_3(I_{IL})}$$

Where: $N_1(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Advanced oxide-isolated, ion implanted Schottky process
- Choice of true or inverting logic
- Open collector outputs on A and B buses
- Local bus-latch capability
- Switching response specified into 500Ω/50 pF
- Switching specification guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

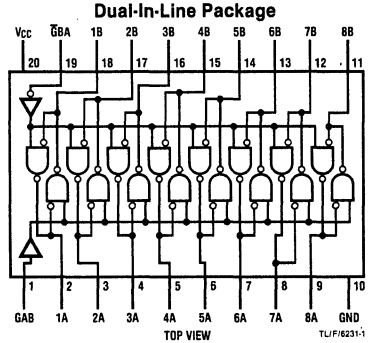
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

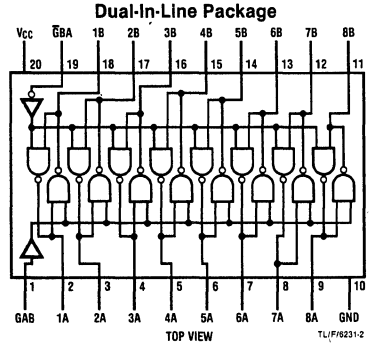
Connection Diagrams

Dual-In-Line Package



54ALS621A (J) 74ALS621A (J, N)

Dual-In-Line Package



54ALS622A (J) 74ALS622A (J, N)

Function Table

Enable Inputs		Operation	
$\overline{G}$BA	GAB	ALS621A	ALS622A
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus
H	H	$\overline{A}$ Data to B Bus	A Data to B Bus
H	L	Hi	Hi
L	H	$\overline{B}$ Data to A Bus $\overline{A}$ Data to B Bus	B Data to A Bus A Data to B Bus

Recommended Operating Conditions

Symbol	Parameter	DM54ALS621A DM54ALS622A			DM74ALS621A DM74ALS622A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS621A-1 and DM74ALS622A-1 Options Only						48	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

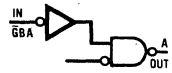
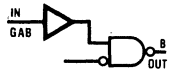
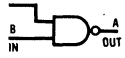
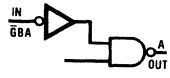
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS621A DM54ALS622A			DM74ALS621A DM74ALS622A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
I_{OH}	High Level Output	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				0.1			0.1	mA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	V
			For 74ALS-1 Option Only $I_{OL} = 48$ mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	A or B Ports			20			20	μA
			Control Inputs			20			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	A or B Ports			−0.1			−0.1	mA
			Control Inputs			−0.1			−0.1	mA
I_{CC}	ALS621A Supply Current	$V_{CC} = 5V$	Outputs High		29	45		29	40	mA
			Outputs Low		35	53		35	48	
	ALS622A Supply Current	$V_{CC} = 5.5V$	Outputs High		11	20		11	15	
			Outputs Low		20	33		20	28	

Switching Characteristics over recommended operating free air temperature (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS621A DM54ALS622A			DM74ALS621A DM74ALS622A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS621A	10		45	10		33	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5		24	5		20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS621A	10		45	10		33	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5		24	5		20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS621A	10		47	10		39	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		12		40	12		35	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS621A	10		47	10		39	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		12		40	12		35	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS622A	18		42	18		35	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5		23	5		19	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS622A	18		42	18		35	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5		23	5		19	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS622A	8		45	8		38	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		10		40	10		35	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS622A	18		45	18		38	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		10		40	10		35	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

National Semiconductor

DM54ALS623A/DM74ALS623A Octal TRI-STATE® Bus Transceiver

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as an octal bus transceiver. It is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives the ALS623A the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Features

- Advanced oxide-isolated, ion implanted Schottky process
- TRI-STATE outputs on A and B buses
- Local bus-latch capability
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

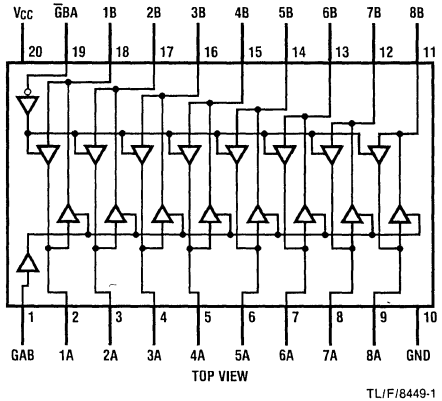
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TL/F/8449-1

54ALS623A (J) 74ALS623A (J, N)

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	ALS623A
L	L	$\overline{B}$ Data to A Bus
H	H	$\overline{A}$ Data to B Bus
H	L	Hi-Z
L	H	$\overline{B}$ Data to A Bus $\overline{A}$ Data to B Bus

Recommended Operating Conditions

Symbol	Parameter	DM54ALS623A			DM74ALS623A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
	DM74ALS623A-1 Option Only						48	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

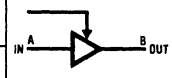
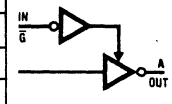
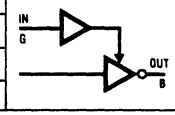
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS623A			DM74ALS623A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3$ mA		2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5V$, I_{OH} = Max		2			2			V
		$I_{OH} = -0.4$ mA, $V_{OL} = 4.5V$ to 5.5V		$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	V
			For 74ALS-1 Option Only $I_{OL} = 48$ mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	A or B Ports			20			20	mA
			Control Inputs			20			20	mA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	A or B Ports			−0.1			−0.1	mA
			Control Inputs			−0.1			−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Output High		32	48		32	43	mA
			Output Low		39	55		39	50	mA
			TRI-STATE		42	60		42	55	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS623A			DM74ALS623A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output		2		15	2		13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		3		13	3		11	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		2		15	2		13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		3		13	3		11	ns
t_{PZL}	Output Enable Time to Low Level		5		25	5		22	ns
t_{PZH}	Output Enable Time to High Level		5		25	5		22	ns
t_{PLZ}	Output Disable Time from Low Level		2		23	2		19	ns
t_{PHZ}	Output Disable Time from High Level		2		19	2		16	ns
t_{PZL}	Output Enable Time to Low Level		5		25	5		22	ns
t_{PZH}	Output Enable Time to High Level		5		25	5		22	ns
t_{PLZ}	Output Disable Time from Low Level		2		23	2		19	ns
t_{PHZ}	Output Disable Time from High Level		2		19	2		16	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

National Semiconductor

PRELIMINARY

DM54ALS677/DM74ALS677, DM54ALS678/DM74ALS678 Address Comparators

General Description

The 'ALS677 and 'ALS678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'ALS677 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high, regardless of the A and P inputs. The 'ALS678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

Features

- 'ALS677 is a 16-bit to 4-bit comparator with enable
- 'ALS678 is a 16-bit to 4-bit comparator with latch
- Switching specifications at 50 pF
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications guaranteed over full temperature and V_{CC} range

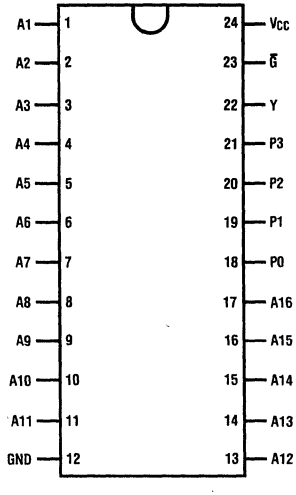
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package

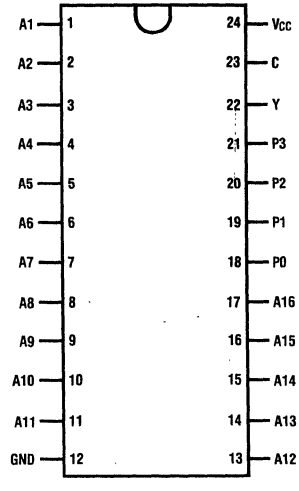


TOP VIEW

TL/F/6236-1

DM54ALS677 (J) **DM74ALS677 (J, N)**

Dual-In-Line Package



TOP VIEW

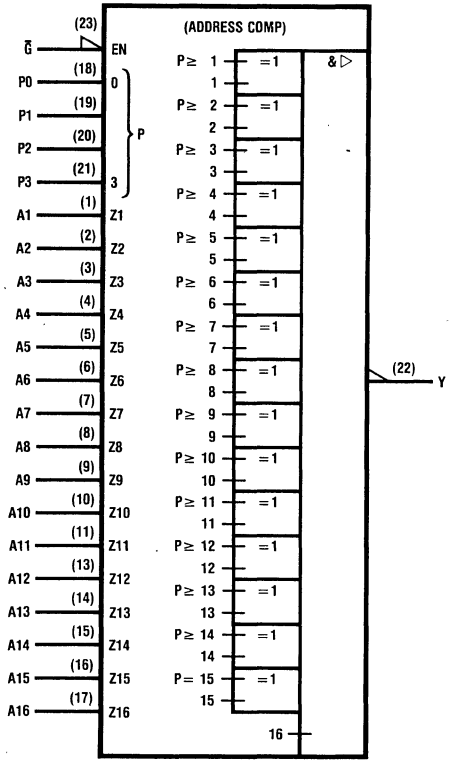
TL/F/6236-2

DM54ALS678 (J) **DM74ALS678 (J, N)**

Function Table

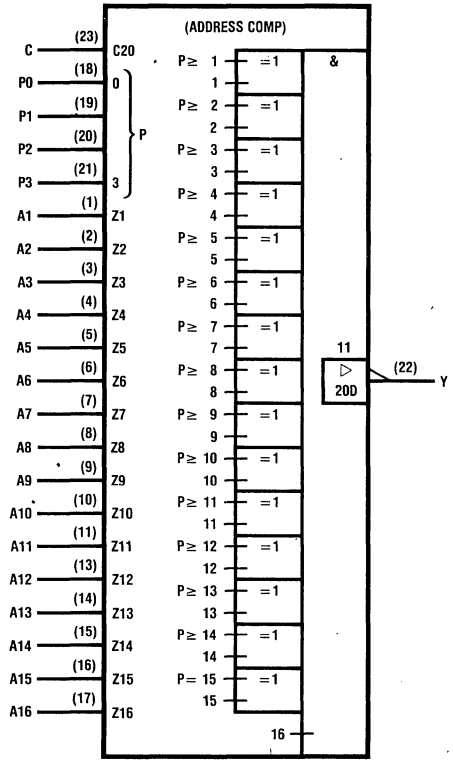
'ALS677 $\overline{G}$	'ALS678 C	Inputs Common to 'ALS677 and 'ALS678																			Output Y
		P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All Other Combinations																				H
H		'ALS677: Any Combination																				H
	L	'ALS678: Any Combination																				Latched

'ALS677



TL/F/6236-3

'ALS678



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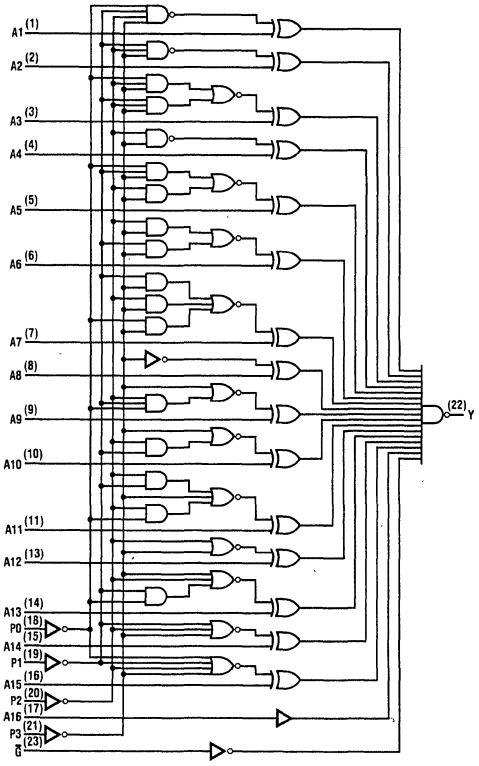
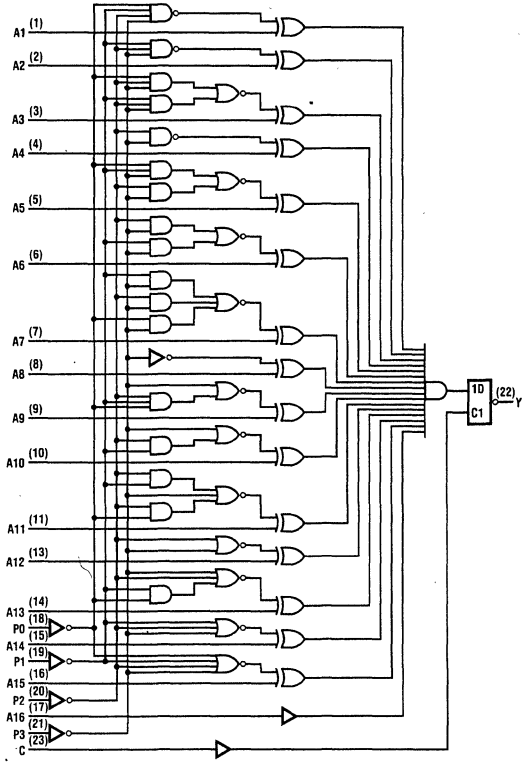
Logic Diagrams (Positive Logic)

'ALS677



TL/F/6236-5

'ALS678



TL/F/6236-6

Pin numbers shown are for JT and NT packages.

Recommended Operating Conditions

Symbol	Parameter	DM54ALS677, 678			DM74ALS677, 678			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	ALS677		18.2	33	mA
			ALS678		17		

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From	To	Conditions	DM54ALS677, 678			DM74ALS677, 678			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any P	Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	4	18	28	4	18	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				8	18	40	8	18	35	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A	Y		5	14	26	5	14	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				5	14	35	5	14	30	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	$\overline{G}$ (ALS667)	Y		3	10	15	3	10	13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				5	10	30	5	10	25	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	C (ALS678)	Y			14			14		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14			14		ns

Note 1: See Section 1 for test waveforms and output load.

Typical Application Information

The 'ALS677 and 'ALS678 can be wired to recognize any one of $2^{16} - 1$ addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8
H	H	L	L	H	H	L	L
A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made:

P3 to 0V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0V.

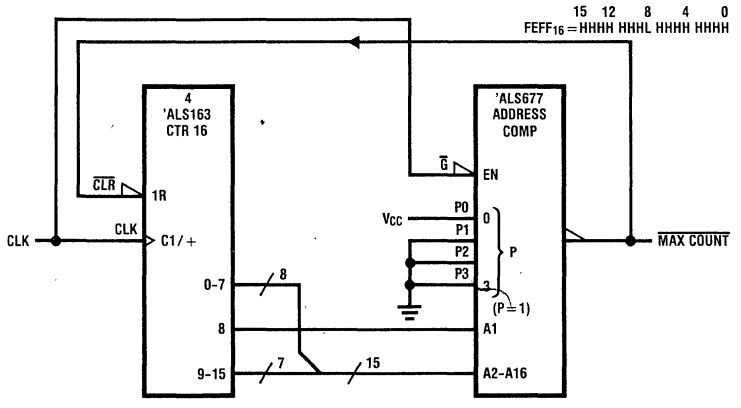
System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when $N = FEFF_{16}$.

Modulo-N Synchronous Counter



TL/F/6236-7

National Semiconductor

PRELIMINARY

DM54ALS679/DM74ALS679, DM54ALS680/DM74ALS680 Address Comparators

General Description

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high, regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

Features

- 'ALS679 is a 12-bit to 4-bit comparator with enable
- 'ALS680 is a 12-bit to 4-bit comparator with latch
- Switching specifications at 50 pF
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications guaranteed over full temperature and V_{CC} range

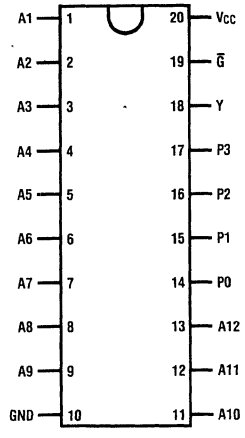
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

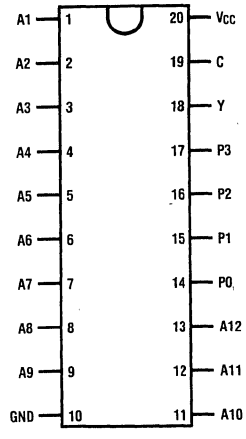
Dual-In-Line Packages



TOP VIEW

TL/F/6237-1

DM54ALS679 (J) **DM74ALS679 (J, N)**



TOP VIEW

TL/F/6237-2

DM54ALS680 (J) **DM74ALS680 (J, N)**

Recommended Operating Conditions

Symbol	Parameter	DM54ALS679, 680			DM74ALS679, 680			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

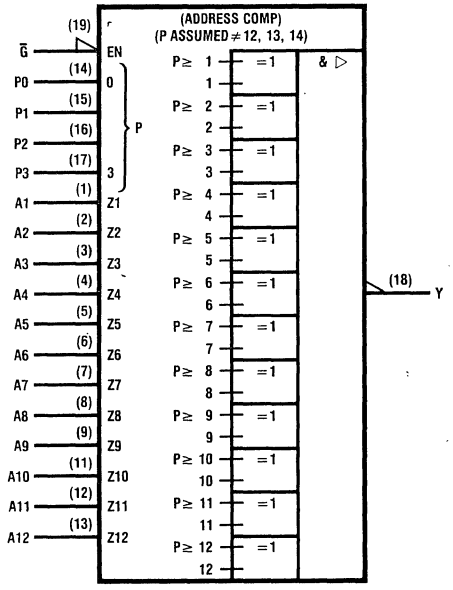
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	ALS679		12.6	28	mA
			ALS680		13.4		

Function Table

'ALS679 $\overline{G}$	'ALS680 C	Inputs Common to 'ALS679 and 'ALS680																Output Y
		P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All Other Combinations																H
H		'ALS679: Any Combination																H
	L	'ALS680: Any Combination																Latched

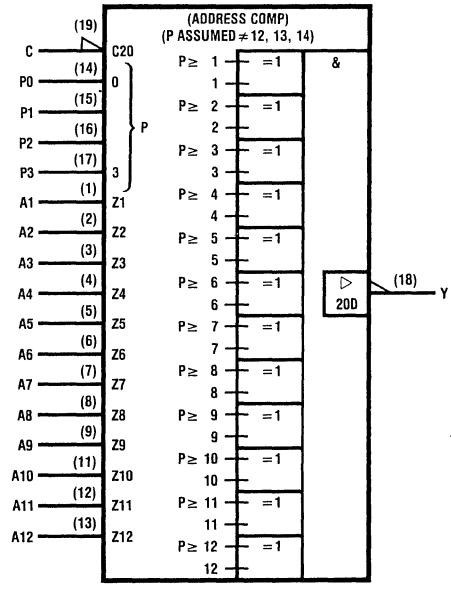
Logic Symbols

'ALS679



TL/F/6237-3

'ALS680



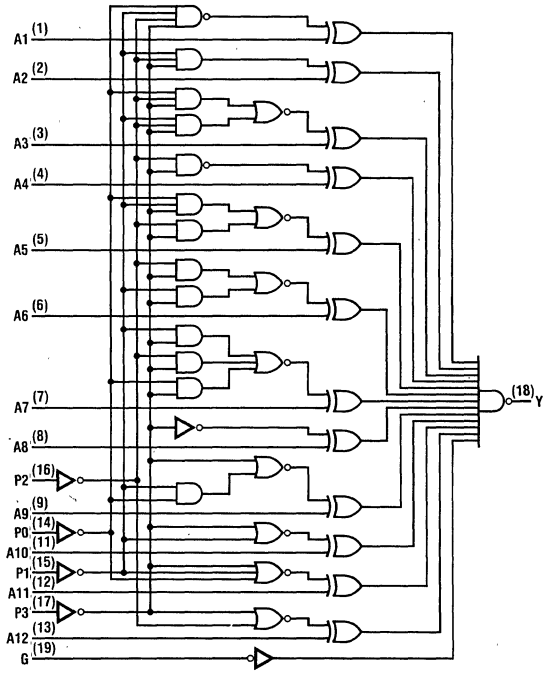
TL/F/6237-4

*The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P = 9...11/13...15, P≥10 to P = 10/11/14/15, and P≥11 to P = 11/15.

Pin numbers shown are for J and N packages.

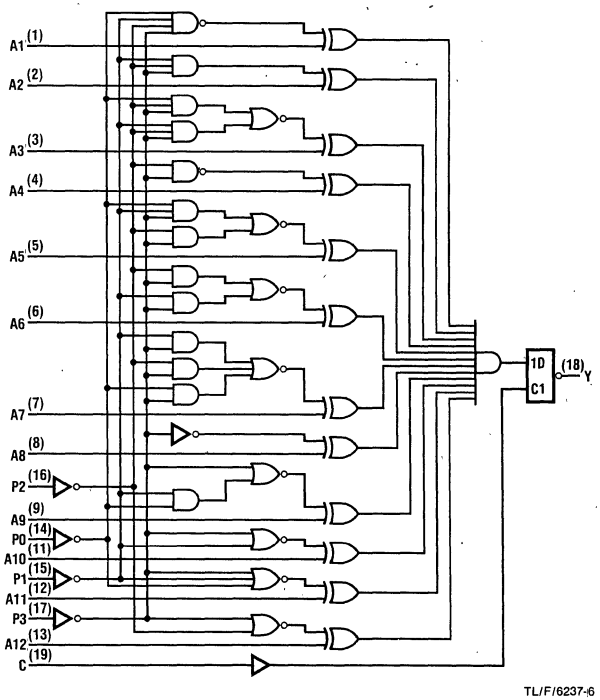
Logic Diagrams (Positive Logic)

'ALS679



TL/F/6237-5

'ALS680



TL/F/6237-6

Pin numbers shown are for J and N packages.

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From	To	Conditions	DM54ALS679, 680			DM74ALS679, 680			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any P	Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	4	18	28	4	18	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				8	18	40	8	18	35	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A	Y		5	14	26	5	14	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				5	14	35	5	14	30	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	$\overline{G}$ (ALS679)	Y		3	10	15	3	10	13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				5	10	30	5	10	25	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	C (ALS680)	Y			14			14		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14			14		ns

Note 1: See Section 1 for test waveforms and output load.

Typical Application Information

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

P3 to 0V, P2 to V_{CC}, P1 to 0V, and P0 to 0V.

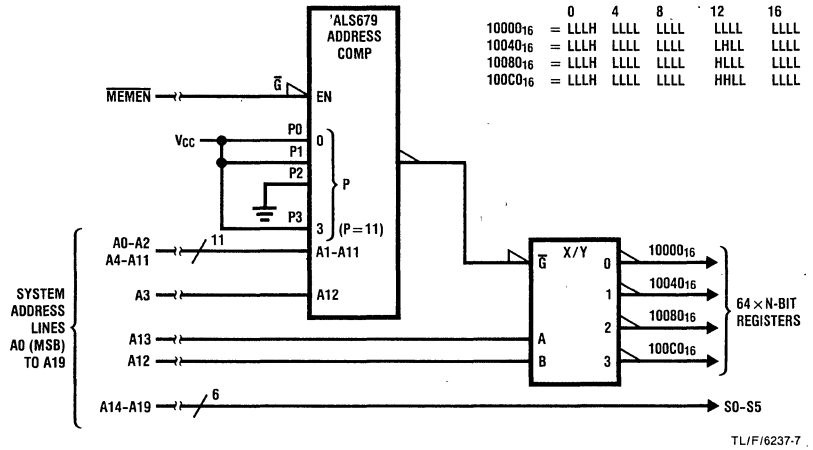
System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.

Register Bank Decoder



TL/F/6237-7

National Semiconductor

DM54ALS689/DM74ALS689 8-Bit Comparator

General Description

This comparator performs an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the $\overline{EN}$ input produces the output $\overline{A = B}$. The ALS 689 has an open collector output for wire AND cascading.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with LS Family TTL Counterpart.
- Improved Output Transient Handling Capability.

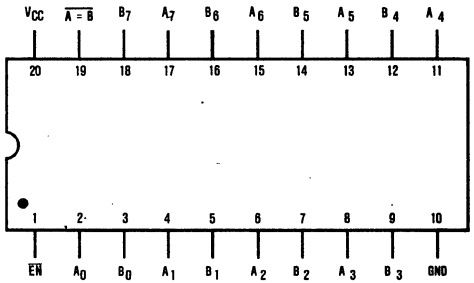
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Offstate Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS689	−55°C to 125°C
DM74ALS689	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6238-1

54ALS689 (J) **74ALS689 (J,N)**

Function Table

Inputs		Output
$\overline{EN}$	Data	$\overline{A=B}$
L	A=B	L
L	A≠B	H
H	X	H

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS689			DM74ALS689			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 5.5V, V_{OH} = 5.5V				0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			12	19	mA

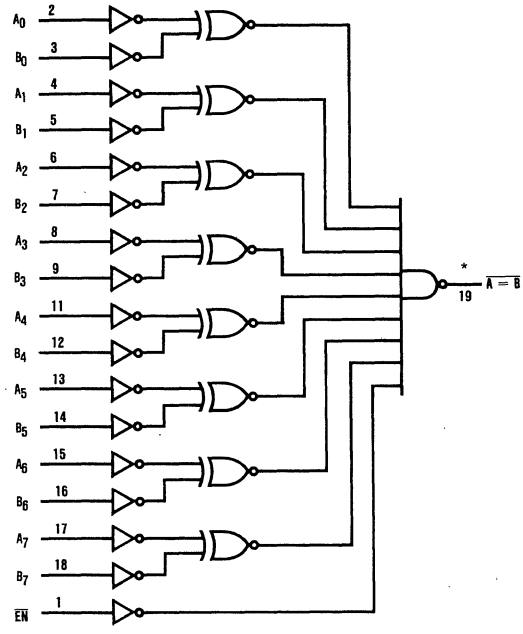
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From Input	To Output	Conditions	DM54ALS689			DM74ALS689			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$	V_{CC}: 4.5V to 5.5V C_L = 50pF R_L = 667Ω	10		30	10		25	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				5		25	5		23	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			8		30	8		25	
T_{PHL}, Propagation Delay Time, High to low Level Output				8		30	8		25	

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



* Output is open collector

TL/F/6238-2

National Semiconductor

DM54ALS804/DM74ALS804 Hex 2-Input NAND Drivers

General Description

These devices contain six independent 2-input drivers, each of which performs the logic NAND function. The -1 option which has an increased I_{OL} maximum to 48 mA is available in the commercial (DM74) part only.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

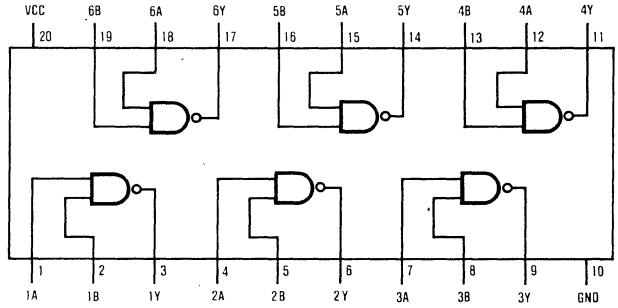
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6239-1

54ALS804 (J) 74ALS804 (J,N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS804			DM74ALS804			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			24	mA
						48*	

*Applies for the DM74ALS804-1 option only.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS (Note 2) I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.9	2.5	mA
			Outputs Low		7	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS804			DM74ALS804			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		8	2		6	ns
T_{PHL}, Propagation delay time. High to low level output		2		9	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: I_{OL} = 48 mA for the -1 option.

National Semiconductor

DM54ALS805/DM74ALS805 Hex 2-Input NOR Drivers

General Description

These devices contain six independent 2-input drivers, each of which performs the logic NOR function. The -1 option which has an increased I_{OL} to 48 mA is available in the commercial (DM74) option only.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

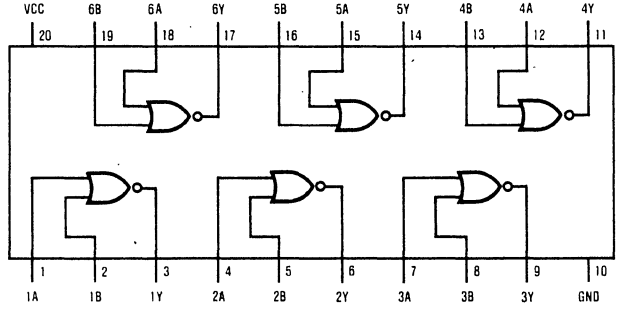
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6240-1

54ALS805 (J) 74ALS805 (J,N)

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS805			DM74ALS805			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			24	mA
						48*	

*Applies for the DM74ALS805-1 option only.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS (Note 2) I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2	4	mA
			Outputs Low		8	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS805			DM74ALS805			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	2		8	2		6	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		9	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: I_{OL} = 48mA for the -1 option.

National Semiconductor

DM54ALS808/DM74ALS808 Hex 2-Input AND Drivers

General Description

These devices contain six independent 2-input drivers, each of which performs the logic AND function. The -1 option which has an increased I_{OL} to 48 mA is available in the commercial (DM74) option only.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings (Note 1)

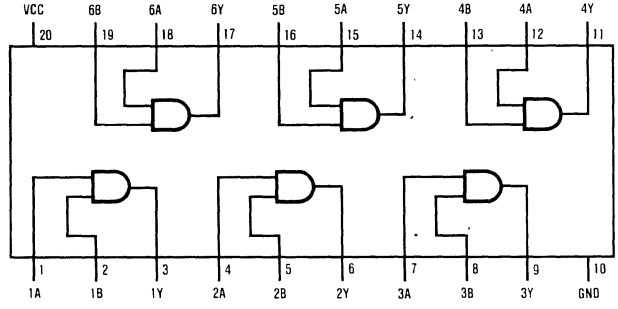
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6241-1

54ALS808 (J) **74ALS808 (J,N)**

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS808			DM74ALS808			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			24	mA
						48*	

*Applies for the DM74ALS808-1 option only.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = 0.4mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = MAX, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS (Note 2) I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	6	mA
			Outputs Low		8	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS808			DM74ALS808			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		10	2		8	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: I_{OL} = 48mA for the -1 option.

National Semiconductor

DM54ALS810/DM74ALS810 Quad 2-Input Exclusive-NOR Gates

General Description

This device contains four independent gates, each of which performs the logic exclusive-NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Absolute Maximum Ratings (Note 1)

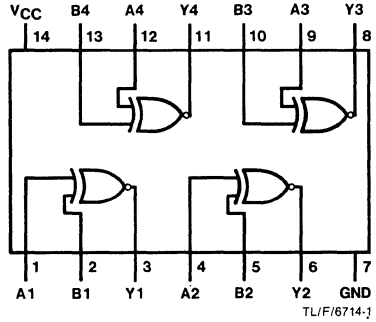
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6714-1

DM54ALS810 (J) DM74ALS810 (J, N)

Function Table

$\overline{Y} = A \oplus B$

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

H = high logic level
L = low logic level

Recommended Operating Conditions

Symbol	Parameter	DM54ALS810			DM74ALS810			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	V_{CC} − 2	3.4		V
			DM74	V_{CC} − 2	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			5	7.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Switching Characteristics over recommended operating free air temperature range

Parameter	Conditions	DM54ALS810			DM74ALS810			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	5		23	5		20	ns
t_{PHL}, Propagation Delay Time High to Low Level Output		3		17	3		14	
t_{PLH}, Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	5		21	5		18	ns
t_{PHL}, Propagation Delay Time High to Low Level Output		3		17	3		14	

National Semiconductor

DM54ALS811/DM74ALS811 Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-NOR function.

The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC\,(Min)} - V_{OH}}{N1\,(I_{OH}) + N2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC\,(Max)} - V_{OL}}{I_{OL} - N3\,(I_{IL})}$$

Where $N1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

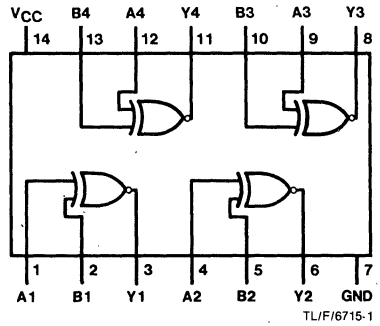
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6715-1

DM54ALS811 (J) DM74ALS811 (J, N)

Function Table

$$\overline{Y} = A \oplus B$$

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

H = high logic level

L = low logic level

Recommended Operating Conditions

Symbol	Parameter	DM54ALS811			DM74ALS811			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{iL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			5	7.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Switching Characteristics over recommended operating free air temperature range

Parameter	Conditions	DM54ALS811			DM74ALS811			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	25		60	25		55	ns
t_{PHL}, Propagation Delay Time High to Low Level Output		5		30	5		28	
t_{PLH}, Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	20		55	20		50	ns
t_{PHL}, Propagation Delay Time High to Low Level Output		5		28	5		23	

National Semiconductor

DM54ALS832/DM74ALS832 Hex 2-Input OR Drivers

General Description

These devices contain six independent drivers, each of which performs the logic OR function. The -1 option which has an increased I_{OL} to 48 mA is available in the commercial option only.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings (Note 1)

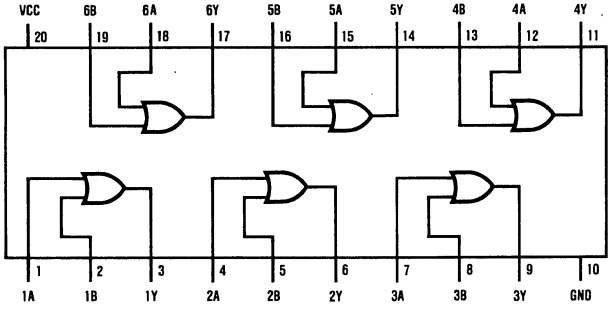
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6242-1

54ALS832 (J) 74ALS832 (J,N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM74ALS832			DM54ALS832			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			24	mA
						48*	

*Applies for the DM74ALS832-1 option only.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = -4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC}-2$			V
		$I_{OH} = -3mA$, $V_{CC} = 4.5V$		2.4			V
		$I_{OH} = MAX$, $V_{CC} = 4.5V$		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS (Note 2) I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		4	8	mA
			Outputs Low		9.5	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS832			DM74ALS832			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, $R_L = 500\ \Omega$, $C_L = 50$ pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		10	2		8	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: $I_{OL} = 48mA$ for the -1 option.

National Semiconductor

DM54ALS873/DM74ALS873 Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS873 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

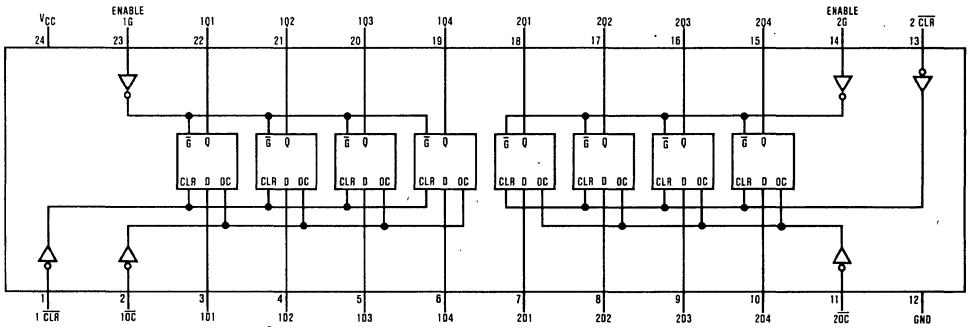
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS873	−55°C to 125°C
DM74ALS873	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6243-1

54ALS873 (J) **74ALS873 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS873			DM74ALS873			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Pulse Width, T_W	Enable High	15			15			ns
	Clear Low	15			15			
Data Setup Time, T_{SU}		10↓			10↓			ns
Data Hold Time, T_H		7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX I_{OH} = Max		2.4	3.2		V
		$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ to 5.5V	54/74ALS	$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 2.7V$				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ $V_O = 0.4V$				−20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		11	21	mA
			Outputs Low		16	29	mA
			Outputs Disabled		20	31	mA

2

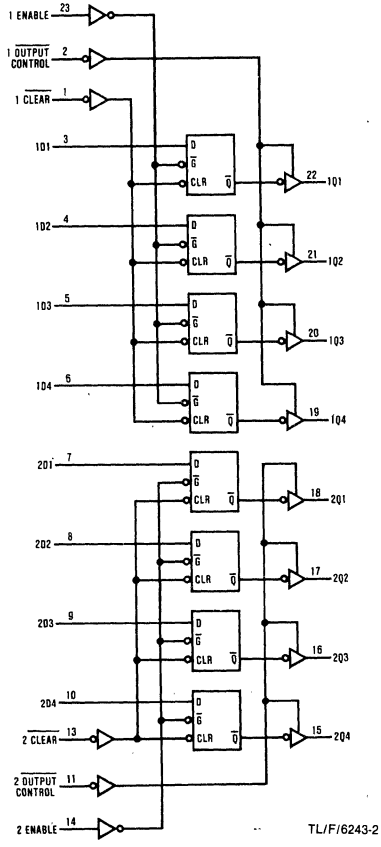
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS873			DM74ALS873			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	2		15	2		14	ns
T_{PHL}				2		15	2		14	ns
T_{PLH}	Enable	Any Q		8		25	8		21	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				2		15	2		12	ns
T_{PHL}	Clear	Any Q		6		23	6		20	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6243-2

Function Table

$\overline{CLR}$	D	EN	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54ALS874/DM74ALS874 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS874 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.
- Asynchronous Clear

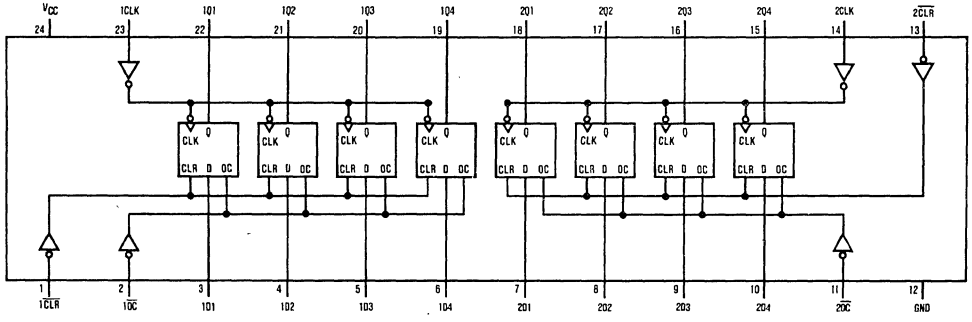
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS874	−55°C to 125°C
DM74ALS874	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6244-1

54ALS874 (J) **74ALS874 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS874			DM74ALS874			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		25	0		30	MHz
Width of Clock Pulse, T_W	High	20			16.5			ns
	Low	20			16.5			ns
Width of Clear Pulse, T_W	Low	10			10			ns
Data Setup Time, T_{SU}		15↑			15↑			ns
Data Hold Time, T_H		4↑			0↑			ns
Clear Inactive, T_{SU}		10			10			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ V_{CC} = 4.5V to 5.5V	54/74ALS	$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$	Data, CLK			−0.2	mA
			All Others			−0.2	
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		19	30	mA
			Outputs Disabled		20	32	mA

2

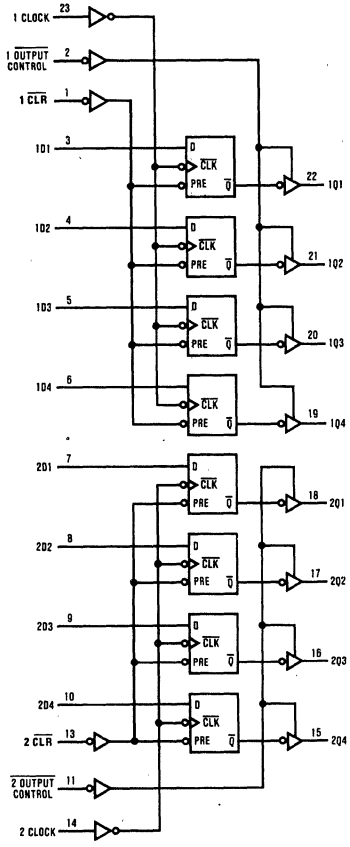
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS874			DM74ALS874			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Clock	Any Q		4		15	4		14	ns
T_{PHL}				4		15	4		14	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				2		15	2		12	ns
T_{PHL}	Clear	Any Q		5		20	5		17	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6244-2

Function Table

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54ALS876/DM74ALS876 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These inverting dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS876 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.
- Asynchronous Preset.

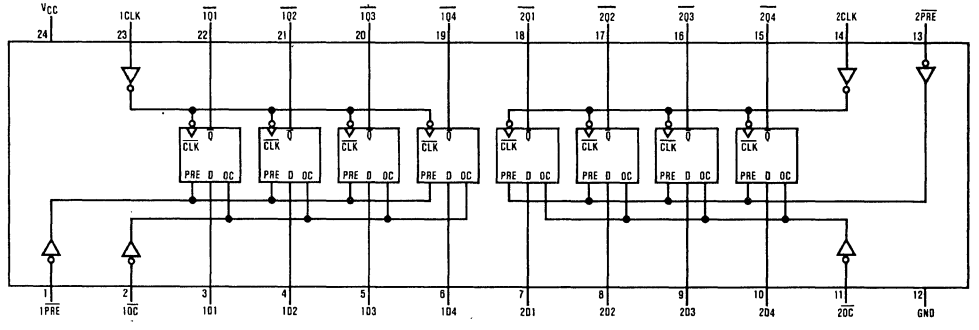
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS876	−55°C to 125°C
DM74ALS876	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6245-1

54ALS876 (J) 74ALS876 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS876			DM74ALS876			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		25	0		30	MHz
Width of Clock Pulse, T_W	High	20			16.5			ns
	Low	20			16.5			ns
Width of Preset Pulse, T_W	Low	10			10			ns
Data Setup Time, T_{SU}		15↑			15↑			ns
Data Hold Time, T_H		4↑			0↑			ns
Preset Inactive, T_{SU}		10↑			10↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$ $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ to $5.5V$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$ $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$ $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$	Data, CLK			−0.2	mA
			All Others			−0.2	
I_O	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS $V_O = 2.25V$	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$ $V_{IH} = 2V$ $V_O = 2.7V$				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$ $V_{IH} = 2V$ $V_O = 0.4V$				−20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		14	21	mA
			Outputs Low		19	30	mA
			Outputs Disabled		20	32	mA

2

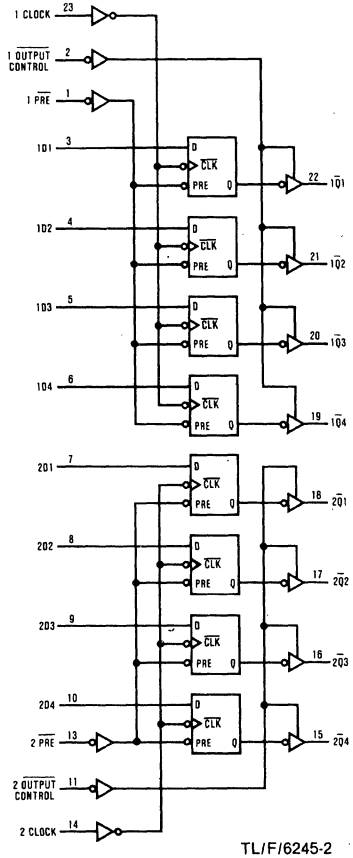
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS876			DM74ALS876			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	25			30			MHz
T_{PLH}	Clock	Any $\overline{Q}$		4		15	4		14	ns
T_{PHL}				4		15	4		14	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				2		15	2		12	ns
T_{PHL}	Preset	Any $\overline{Q}$		5		20	5		17	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6245-2

Function Table

$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54ALS880/DM74ALS880 Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit inverting registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS880 are transparent D-type latches meaning that while the enable (G) is high the $\overline{Q}$ outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

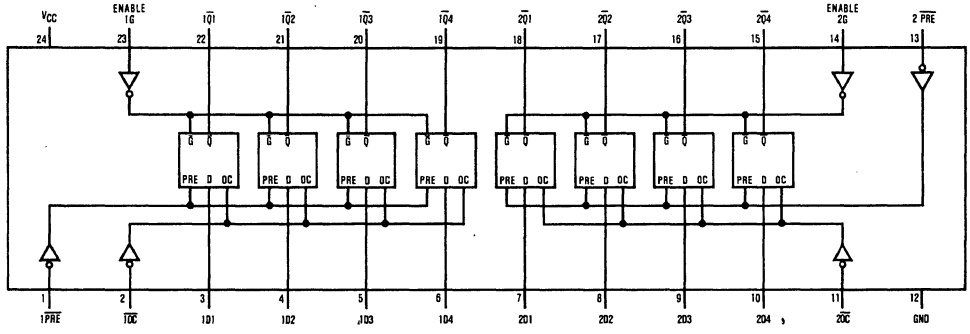
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS880	−55°C to 125°C
DM74ALS880	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6248-1

54ALS880 (J) 74ALS880 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS880			DM74ALS880			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Pulse Width, T_W	Enable High	15			15			ns
	Preset Low	15			15			
Data Setup Time, T_{SU}		10↓			10↓			ns
Data Hold Time, T_H		10↓			10↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ to 5.5V	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		19	29	mA
			Outputs Disabled		20	31	mA

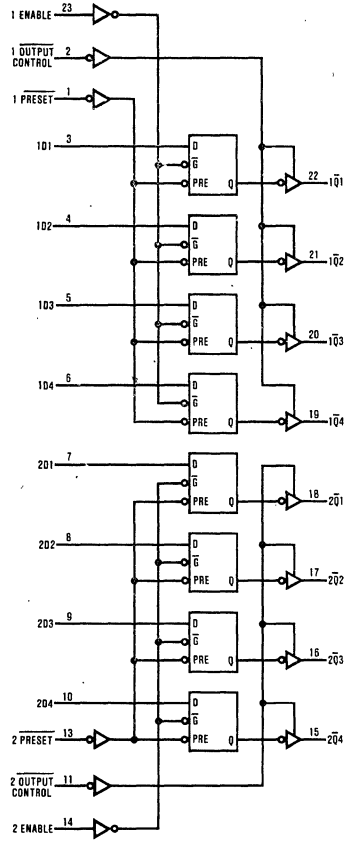
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54ALS880			DM74ALS880			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		23	3		20	ns
T_{PHL}				3		15	3		14	ns
T_{PLH}	Enable	Any $\overline{Q}$		8		31	8		24	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	5		18	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns
T_{PHL}	Preset	Any $\overline{Q}$		6		24	6		21	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6248-2

Function Table

$\overline{PRE}$	D	EN	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54ALS1000A/DM74ALS1000A Quadruple 2-Input NAND Buffers

General Description

These devices contain four independent 2-input buffer/drivers each of which performs the logic NAND function. The 'ALS1000A is a buffer/driver version of the 'ALS00A.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

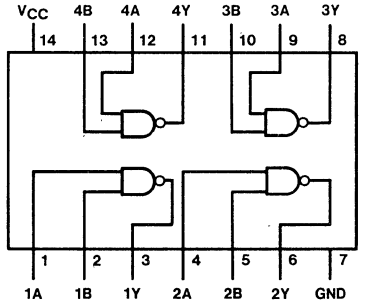
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1000A	−55°C to 125°C
DM74ALS1000A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6249-1

54ALS1000A (J) **74ALS1000A (J, N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS1000A			DM74ALS1000A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ V_{CC} = 4.5V to 5.5V	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			7.8	4.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1000A			DM74ALS1000A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		10	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1002A/DM74ALS1002A Quadruple 2-Input Positive-NOR Buffers

General Description

These devices contain four independent 2-input buffers each of which performs the logic NOR function. The 'ALS1002A is a buffer version of the 'ALS02.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

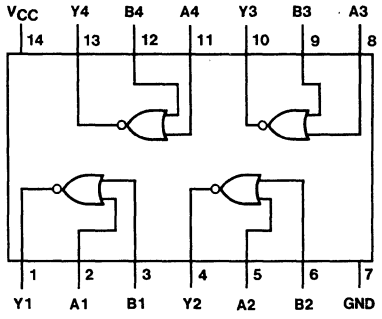
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1002A	−55°C to 125°C
DM74ALS1002A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6250-1

54ALS1002A (J) **74ALS1002A (J,N)**

Function Table

$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

2

Recommended Operating Conditions

Parameter	DM54ALS1002A			DM74ALS1002A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ V_{CC} = 4.5V to 5.5V	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			5.6	9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1002A			DM74ALS1002A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		11	3		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1003A/DM74ALS1003A Quadruple 2-Input NAND Buffers with Open-Collector Outputs

General Description

These devices contain four independent 2-input buffers, each of which performs the logic NAND function. The outputs require an external pull-up resistor for proper logical operation. The 'ALS1003A is a buffer version of the 'ALS03A.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved Line Receiving Characteristics.

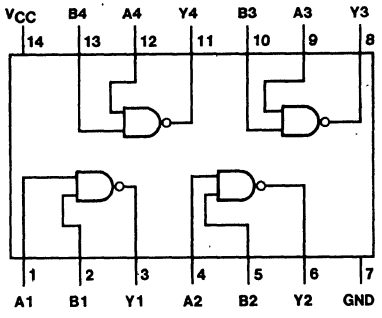
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1003A	−55°C to 125°C
DM74ALS1003A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6251-1

54ALS1003A (J) **74ALS1003A (J,N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS1003A			DM74ALS1003A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$ $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CCH}	Supply Current	Outputs High $V_{CC} = 5.5V$, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low $V_{CC} = 5.5V$, VI = 4.5V			4.8	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1003A			DM74ALS1003A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 667 Ω, C_L = 50 pF.	5		40	5		33	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		18	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1004/DM74ALS1004 Hex Inverting Drivers

General Description

These devices contain six independent 2-input drivers, each of which performs the logic inverter/complement function. The 'ALS1004 is a driver version of the 'ALS04A.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

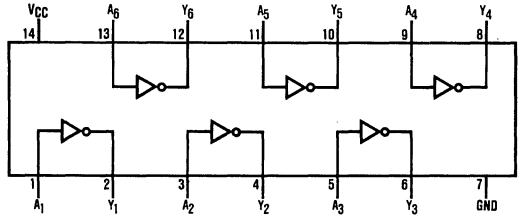
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6252-1

54ALS1004 (J) 74ALS1004 (J,N)

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54ALS1004			DM74ALS1004			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
		I_{OH} = Max, V_{CC} = 4.5V		2			
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.84	3	mA
			Outputs Low		7	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1004			DM74ALS1004			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	1		9	1		7	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		8	1		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1005/DM74ALS1005 Hex Inverting Drivers with Open Collector Outputs

General Description

These devices contain six independent drivers, each of which performs the logic INVERT/Complement function. The outputs require external pull-up resistors for proper logic operation. The 'ALS1005 is a driver version of the 'ALS05A.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

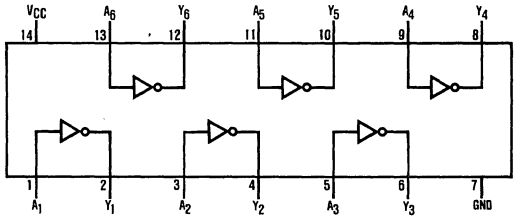
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6253-1

54ALS1005 (J) **74ALS1005 (J,N)**

Function Table

$$Y = \overline{A}$$

Input A	Output Y
H	L
L	H

L = low logic level

H = high logic level

Recommended Operating Conditions

Parameter	DM54ALS1005			DM74ALS1005			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74 ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.9	3	mA
			Outputs Low		7	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1005			DM74ALS1005			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to $5.5V$ $R_L = 667\ \Omega$, $C_L = 50$ pF.	5		35	5		30	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1008A/DM74ALS1008A Quadruple 2-Input AND Buffers

General Description

These devices contain four independent 2-input buffers, each of which performs the logic AND function. The 'ALS1008A is a buffer version of the 'ALS08.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

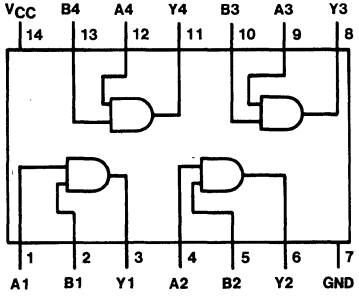
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1008A	−55°C to 125°C
DM74ALS1008A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6254-1

54ALS1008A (J) 74ALS1008A (J,N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

L = low logic level
H = high logic level

2

Recommended Operating Conditions

Parameter	DM54ALS1008A			DM74ALS1008A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA V_{CC} = 4.5V to 5.5V	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IL} = 0.8V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.8	3	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			5.7	9.3	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1008A			DM74ALS1008A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		11	2		9	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		11	3		9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1010A/DM74ALS1010A Triple 3-Input NAND Buffers

General Description

These devices contain three independent 3-input buffers, each of which performs the logic NAND function. The 'ALS1010A is a buffer option of the 'ALS10A.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

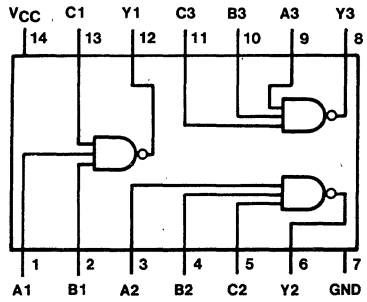
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1010A	−55°C to 125°C
DM74ALS1010A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6255-1

54ALS1010A (J) 74ALS1010A (J,N)

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

L = low logic level
H = high logic level
X = either low or high logic level

2

Recommended Operating Conditions

Parameter	DM54ALS1010A			DM74ALS1010A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ to $5.5V$	54/74ALS	$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CCH}	Supply Current	Outputs High $V_{CC} = 5.5V$, $V_I = 0V$			0.65	1.2	mA
I_{CCL}	Supply Current	Outputs Low $V_{CC} = 5.5V$, $V_I = 4.5V$			3.6	5.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1010A			DM74ALS1010A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to $5.5V$ $R_L = 500\ \Omega$, $C_L = 50$ pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		11	3		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1011A/DM74ALS1011A Triple 3-Input AND Buffers

General Description

These devices contain three independent buffers, each of which performs the logic AND function. The 'ALS1011A is a buffer version of the 'ALS11A.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

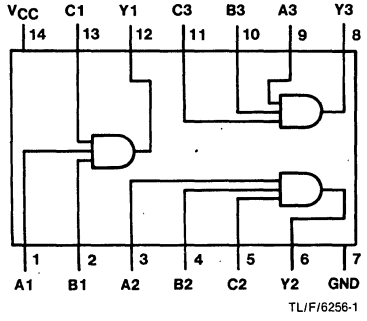
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1011A	−55°C to 125°C
DM74ALS1011A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6256-1

54ALS1011A (J) 74ALS1011A (J,N)

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

L = low logic level
H = high logic level
X = either low or high logic level

Recommended Operating Conditions

Parameter	DM54ALS1011A			DM74ALS1011A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ to $5.5V$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CCH}	Supply Current	Outputs High $V_{CC} = 5.5V$, $V_I = 0V$			1.4	2.3	mA
I_{CCL}	Supply Current	Outputs Low $V_{CC} = 5.5V$, $V_I = 4.5V$			4.3	7	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1011A			DM74ALS1011A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to $5.5V$ $R_L = 500\ \Omega$, $C_L = 50$ pF.	2		12	2		10	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		11	3		9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1020A/DM74ALS1020A Dual 4-Input NAND Buffers

General Description

These devices contain two independent 4-input buffers, each of which performs the logic NAND function. The 'ALS1020A is a buffer version of the 'ALS20A.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

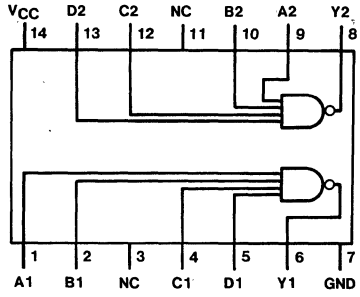
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1020A	−55°C to 125°C
DM74ALS1020A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6257-1

54ALS1020A (J) **74ALS1020A (J,N)**

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = low logic level
H = high logic level
X = either low or high logic level

Recommended Operating Conditions

Parameter	DM54ALS1020A			DM74ALS1020A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	54/74ALS $I_{OH} = -1mA$	2.4	3.2		V
			74ALS $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ to $5.5V$	54/74ALS	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CCH}	Supply Current	Outputs High $V_{CC} = 5.5V$, $V_I = 0V$			0.5	0.8	mA
I_{CCL}	Supply Current	Outputs Low $V_{CC} = 5.5V$, $V_I = 4.5V$			2.4	3.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1020A			DM74ALS1020A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to $5.5V$ $R_L = 500\ \Omega$, $C_L = 50$ pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		10	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1032A/DM74ALS1032A Quadruple 2-Input OR Buffers

General Description

These devices contain four independent buffers, each of which performs the logic OR function. The 'ALS1032A is a buffer version of the 'ALS32.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

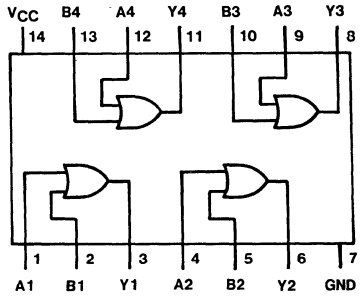
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1032A	−55°C to 125°C
DM74ALS1032A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6258-1

54ALS1032A (J) 74ALS1032A (J,N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
H	X	H
X	H	H

L = low logic level
H = high logic level
X = either low or high logic level

Recommended Operating Conditions

Parameter	DM54ALS1032A			DM74ALS1032A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA V_{CC} = 4.5V to 5.5V	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 0.8V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 4.5V			2.5	5	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 0V			6.6	10.6	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1032A			DM74ALS1032A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		12	2		9	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		15	3		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1034/DM74ALS1034 Hex Non-Inverting Drivers

General Description

These devices contain six independent drivers, each of which performs the logic identity function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

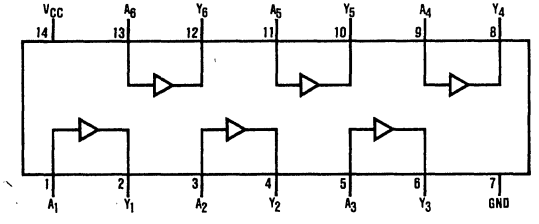
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6259-1

54ALS1034 (J) 74ALS1034 (J,N)

Function Table

$Y = A$

Input A	Output Y
H	H
L	L

L = low logic level

H = high logic level

Recommended Operating Conditions

Parameter	DM54ALS1034			DM74ALS1034			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA, V_{CC} = 4.5 to 5.5V		V_{CC}−2			V
		I_{OH} = Max		2			V
		I_{OH} = −3mA		2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	6	mA
			Outputs Low		8	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1034			DM74ALS1034			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	1		10	1		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		10	1		8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1035/DM74ALS1035 Hex Non-Inverting Drivers with Open Collector Outputs

General Description

These devices contain six independent drivers, each of which performs the logic identity function. The outputs require an external pull-up resistor for proper logical operation.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings (Note 1)

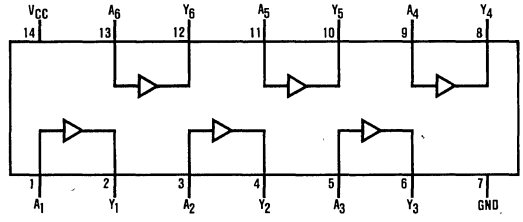
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

Dual-In-Line Package



TL/F/6260-1

54ALS1035 (J) **74ALS1035 (J,N)**

Function Table

$Y = A$

Input A	Output Y
L	L
H	H

L = low logic level
H = high logic level

Recommended Operating Conditions

Parameter	DM54ALS1035			DM74ALS1035			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.5	V
I_{OH}	High Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 12mA$		0.25	0.4	V
			74 ALS $I_{OL} = 24mA$		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.1	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		3	6	mA
			Outputs Low		8	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54ALS1035			DM74ALS1035			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to $5.5V$, $R_L = 667\ \Omega$, $C_L = 50$ pF.	5		35	5		30	ns
T_{PHL}, Propagation delay time. High to low Level Output		2		14	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54ALS1240/DM74ALS1240, DM54ALS1241/DM74ALS1241 Octal TRI-STATE® Bus Drivers

General Description

These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS240 and 'ALS241. The output TRI-STATE gating control is organized into two separate groups of four buffers. The 'ALS1240 control inputs symmetrically enable the respective outputs when set logic low, while the 'ALS1241 has complementary enable gating. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and down.

The -1 versions of the DM74ALS devices are identical to their standard versions except that the recommended maximum I_{OL} is increased to 24 mA. There are no -1 versions of the DM54ALS devices.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS240, 241
- Low level drive current: 54ALS = 8 mA, 74ALS = 16 mA, 74ALS-1 = 24 mA

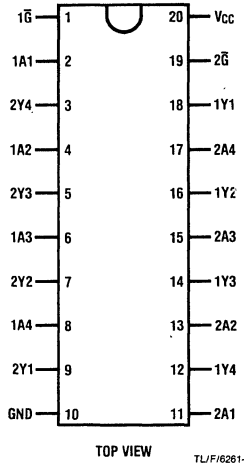
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

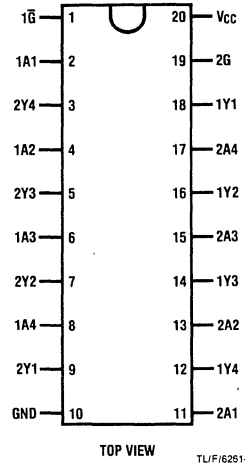
Dual-In-Line Package



TOP VIEW TL/F/6261-1

DM54ALS1240 (J) DM74ALS1240 (J, N)

Dual-In-Line Package



TOP VIEW TL/F/6261-2

DM54ALS1241 (J) DM74ALS1241 (J, N)

Function Table

Enable Input		Data Buffer Output
G	$\overline{G}$	
H	L	Active
L	H	TRI-STATE

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1240 DM54ALS1241			DM74ALS1240 DM74ALS1241			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	DM74ALS1240-1, DM74ALS1241-1			—			24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS1240 DM54ALS1241			DM74ALS1240 DM74ALS1241			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS1240 Outputs High			4	6		4	6	mA
		Outputs Low			8	12		8	12	mA
		Outputs TRI-STATE			9	13		9	13	mA
		V_{CC} = 5.5V, ALS1241 Outputs High			7	11		7	11	mA
		Outputs Low			10	15		10	15	mA
		Outputs TRI-STATE			11	17		11	17	mA

'ALS1240 Switching Characteristics over recommended operating free-air temperature range

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max						Units
			54ALS1240			74ALS1240			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y			9			8	ns
t_{PHL}					7			7	ns
t_{PZH}	$\overline{G}$	Y			19			18	ns
t_{PZL}					20			19	ns
t_{PHZ}	$\overline{G}$	Y			7			6	ns
t_{PLZ}					10			7	ns

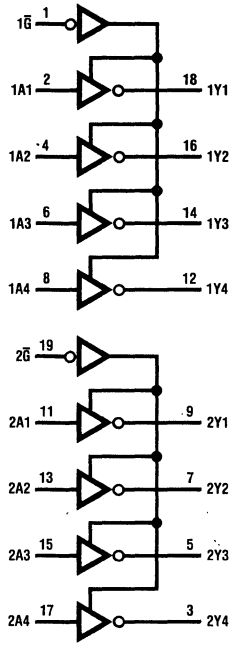
'ALS1241 Switching Characteristics over recommended operating free-air temperature range

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max						Units
			54ALS1241			74ALS1241			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y			12			11	ns
t_{PHL}					13			12	ns
t_{PZH}	$\overline{G}$ or G	Y			23			22	ns
t_{PZL}					22			21	ns
t_{PHZ}	$\overline{G}$ or G	Y			11			11	ns
t_{PLZ}					19			16	ns

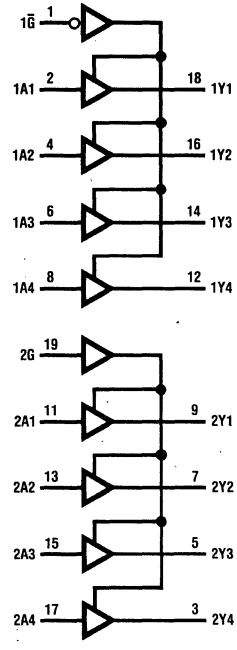
Logic Diagrams

DM54/74ALS1240



TL/F/6261-3

DM54/74ALS1241



TL/F/6261-4

National Semiconductor

DM54ALS1242/DM74ALS1242, DM54ALS1243/DM74ALS1243 Quad Bidirectional Bus Drivers

General Description

These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS242 and 'ALS243. The 'ALS1242 has inverting buffers, while the 'ALS1243 has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power down.

The -1 versions of the DM74ALS devices are identical to their standard versions except that the recommended maximum I_{OL} is increased to 24 mA. There are no -1 versions of the DM54ALS devices.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS242, 243
- Low level drive current: 54ALS = 8 mA, 74ALS = 16 mA, 74ALS-1 = 24 mA

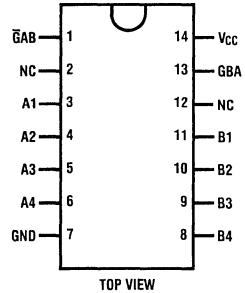
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6262-1

DM54ALS1242, DM54ALS1243 (J)
DM74ALS1242, DM74ALS1243 (J, N)

Function Table

Inputs		ALS1242	ALS1243
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1242 DM54ALS1243			DM74ALS1242 DM74ALS1243			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	DM74ALS1242-1, DM74ALS1243-1			—			24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS1242 DM54ALS1243			DM74ALS1242 DM74ALS1243			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (V_I = 5.5V for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS1242 Active Outputs High			7	10		7	10	mA
		Active Outputs Low			8	13		8	13	mA
		Outputs TRI-STATE			9	14		9	14	mA
		V_{CC} = 5.5V, ALS1243 Active Outputs High			9	14		9	14	mA
		Active Outputs Low			10	16		10	16	mA
		Outputs TRI-STATE			11	17		11	17	mA

'ALS1242 Switching Characteristics over recommended operating free-air temperature range

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max						Units
			54ALS1242			74ALS1242			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A			9			8	ns
t_{PHL}					7			6	ns
t_{PZH}	$\overline{G}$AB	B			23			20	ns
t_{PZL}					20			19	ns
t_{PHZ}	$\overline{G}$AB	B			7			7	ns
t_{PLZ}					12			10	ns
t_{PZL}	GBA	A			22			21	ns
t_{PZL}					22			20	ns
t_{PHZ}	GBA	A			11			10	ns
t_{PLZ}					20			16	ns

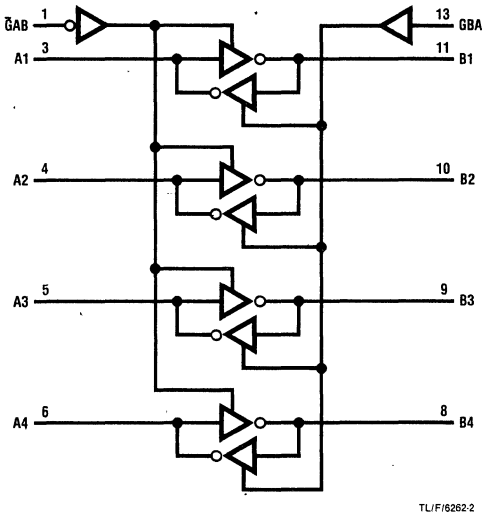
'ALS1243 Switching Characteristics over recommended operating free-air temperature range

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max						Units
			54ALS1243			74ALS1243			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A			12			11	ns
t_{PHL}					13			12	ns
t_{PZH}	$\overline{G}$AB	B			23			22	ns
t_{PZL}					20			20	ns
t_{PHZ}	$\overline{G}$AB	B			7			7	ns
t_{PLZ}					13			12	ns
t_{PZL}	GBA	A			23			22	ns
t_{PZL}					22			21	ns
t_{PHZ}	GBA	A			11			11	ns
t_{PLZ}					19			16	ns

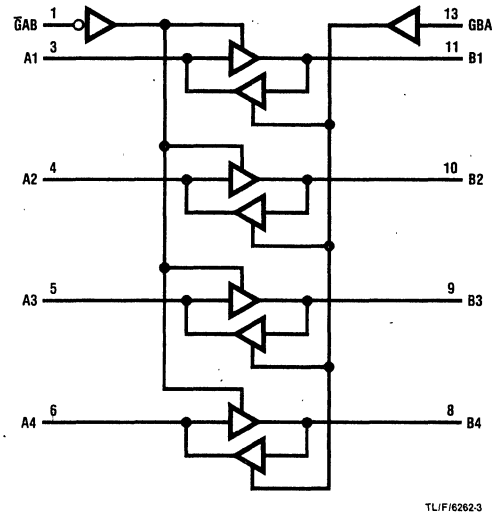
Logic Diagrams

DM54/74ALS1242



TL/F/6262-2

DM54/74ALS1243



TL/F/6262-3

National Semiconductor

DM54ALS1244A/DM74ALS1244A Octal TRI-STATE® Bus Driver

General Description

This octal TRI-STATE bus driver is designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and is a low power dissipation version of the 'ALS244A. The output TRI-STATE gating control is organized into two separate groups of four buffers, and both control inputs enable the respective outputs when set logic low. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

The -1 versions of the DM74ALS devices are identical to their standard versions except that the recommended maximum I_{OL} is increased to 24 mA. There are no -1 versions of the DM54ALS devices.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS244A
- Low level drive current: 54ALS = 8 mA, 74ALS = 16 mA, 74ALS-1 = 24 mA

Absolute Maximum Ratings (Note 1)

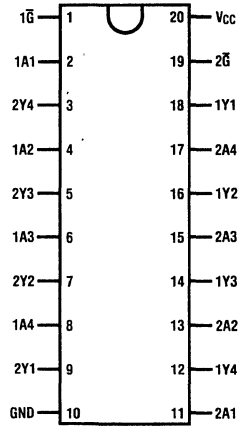
Supply Voltage, V_{CC}	7V
Input Voltage	7V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

2

Connection Diagram

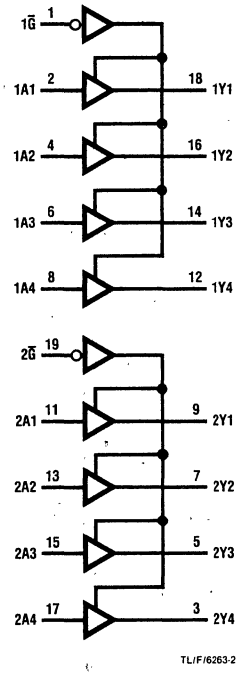
Dual-In-Line Package



TOP VIEW TL/F/6263-1

DM54ALS1244A (J)
DM74ALS1244A (J, N)

Logic Diagram



TL/F/6263-2

Function Table

Enable Input 1G or 2G	Data Buffer Outputs
L	Active
H	TRI-STATE

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1244A			DM74ALS1244A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	DM74ALS1244A-1			—			24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54ALS1244A			DM74ALS1244A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V, I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		I_{OH} = −3 mA	2.4			2.4			V
		I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)		0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)		—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (V_I = 5.5V for A or B Ports)			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V			20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V			−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs High		6	15		6	11	mA
		Outputs Low		10	20		10	17	mA
		Outputs TRI-STATE		11	25		11	20	mA

Switching Characteristics over recommended operating free-air temperature range

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max				Units
			54ALS1244A		74ALS1244A		
			Min	Max	Min	Max	
t_{PLH}	A	Y	3	16	3	14	ns
t_{PHL}			3	16	3	14	ns
t_{PZH}	$\overline{G}$	Y	6	26	6	22	ns
t_{PZL}			6	26	6	22	ns
t_{PHZ}	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}			3	16	3	13	ns

National Semiconductor

DM54ALS1245A/DM74ALS1245A TRI-STATE® Bus Transceivers

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. This circuit is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data either transmits from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode. So that the buses are effectively isolated TTL, the TRI-STATE circuitry also contains a protection feature that prevents the buffer from glitching the bus during power-up or power-down.

Features

- Low power versions of ALS245A
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Choice of true or inverting logic
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

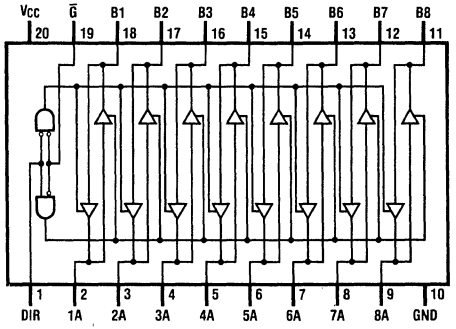
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/8438-1

54ALS1245A (J) **74ALS1245A (J, N)**

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

L = low logic level
H = high logic level
X = either low or high logic level
Hi-Z = high impedance (off) state

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1245A			DM74ALS1245A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	74ALS-1 Option Only						24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

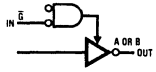
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS1245A			DM74ALS1245A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 45V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3$ mA		2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5V$, I_{OH} = Max		2	2.3		2	2.3		V
		$I_{OH} = -0.4$ mA, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 8$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 16$ mA (Note 3)					0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$				20			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$				−0.1			−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		21	33		21	30	mA
			Outputs Low		23	36		23	33	mA
			TRI-STATE		25	40		25	36	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS1245A			DM74ALS1245A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output		2		15	2		13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		15	2		13	ns
t_{PZL}	Output Enable Time to Low Level		8		28	8		25	ns
t_{PZH}	Output Enable Time to High Level		8		28	8		25	ns
t_{PLZ}	Output Disable Time from Low Level		3		22	3		18	ns
t_{PHZ}	Output Disable Time from High Level		2		14	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

Note 3: $I_{OL} = 24$ mA for -1 option.

National Semiconductor

PRELIMINARY

DM54ALS1620/DM74ALS1620 Octal TRI-STATE® Bus Transceivers

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE log elements configured as an octal bus transceiver. It is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives the ALS1620 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Features

- Low power version of ALS620
- Advanced oxide-isolated, ion implanted Schottky process
- TRI-STATE outputs on A and B buses
- PNP input design reduces input loading
- Local bus-latch capability
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

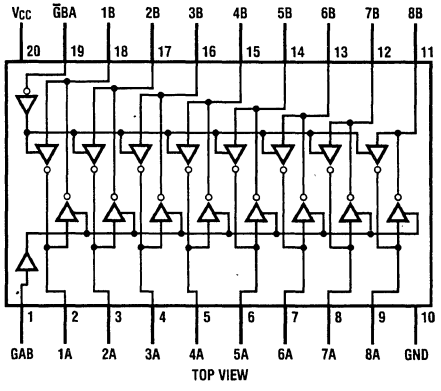
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6264-1

54ALS1620 (J) **74ALS1620 (J, N)**

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ Data to A Bus
H	H	$\overline{A}$ Data to B Bus
H	L	Hi-Z
L	H	$\overline{B}$ Data to A Bus $\overline{A}$ Data to B Bus

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1620			DM74ALS1620			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	DM74ALS1620-1						24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

*Applies to 74ALS-1 options.

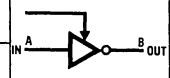
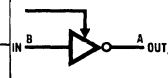
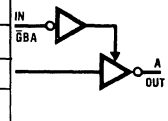
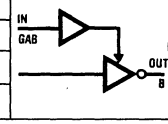
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS1620			DM74ALS1620			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3$ mA		2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5V$, I_{OH} = Max		2			2			
		$I_{OH} = -0.4$ mA, $V_{OL} = 4.5V$ to 5.5V		$V_{CC} - 2$			$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	DM54/74ALS $I_{OL} = 8$ mA		0.25	0.4		0.25	0.4	V
			DM74ALS $I_{OL} = 16$ mA (Note 3)					0.35	0.5	
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$				20			20	mA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$				−0.1			−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		14			14		mA
			Outputs Low		19			19		
			TRI-STATE		21			21		

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS1620			DM74ALS1620			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output			9			9		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			6			6		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output			9			9		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			6			6		ns
t_{PZL}	Output Enable Time to Low Level			17			17		ns
t_{PZH}	Output Enable Time to High Level			14			14		ns
t_{PLZ}	Output Disable Time from Low Level			11			11		ns
t_{PHZ}	Output Disable Time from High Level			7			7		ns
t_{PZL}	Output Enable Time to Low Level			17			17		ns
t_{PZH}	Output Enable Time to High Level			14			14		ns
t_{PLZ}	Output Disable Time from Low Level			11			11		ns
t_{PHZ}	Output Disable Time from High Level			7			7		ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

Note 3: $I_{OL} = 24$ mA for -1 option.

National Semiconductor

PRELIMINARY

DM54ALS1621/DM74ALS1621, DM54ALS1622/DM74ALS1622 Octal Open Collector Output Bus Transceivers

General Description

These advanced low power Schottky devices contain 8 pairs of log elements configured as octal bus transceivers. They are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives the ALS1621 and ALS1622 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Low power versions of 'ALS621, 622
- Advanced oxide-isolated, ion implanted Schottky process
- Choice of true or inverting logic
- Open collector outputs on A and B buses
- PNP input design reduces input loading
- Local bus-latch capability
- Switching response specified into 500Ω/50 pF
- Switching specification guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

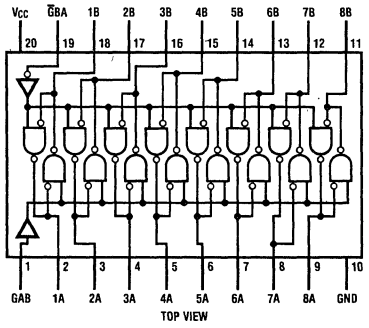
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

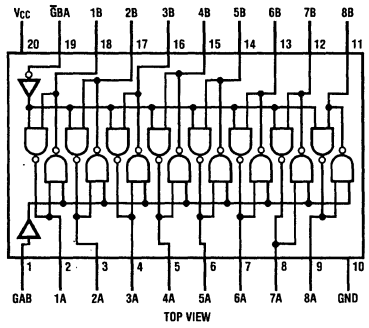
Connection Diagrams

Dual-In-Line Packages



TL/F/6265-1

54ALS1621 (J) 74ALS1621 (J, N)



TL/F/6265-2

54ALS1622 (J) 74ALS1622 (J, N)

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1621 DM74ALS1622			DM74ALS1621 DM74ALS1622			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			8			16	mA
	DM74ALS1621-1 and DM74ALS1622-1 Options Only						24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

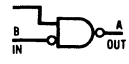
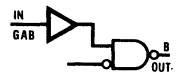
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS1621 DM54ALS1622			DM74ALS1621 DM74ALS1622			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
I_{OH}	High Level Output	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$				0.1			0.1	mA
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 8$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 16$ mA					0.35	0.5	
			For 74ALS-1 Option Only $I_{OL} = 24$ mA					0.35	0.5	
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$				20			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$				−0.1			−0.1	mA
I_{CC}	DM54/74ALS1621 Supply Current	$V_{CC} = 5.5V$	Outputs High		11			11		mA
			Outputs Low		16			16		
I_{CC}	DM54/74ALS1622 Supply Current	$V_{CC} = 5.5V$	Outputs High		13			13		mA
			Outputs Low		18			18		

Switching Characteristics over recommended operating free air temperature (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS1621 DM54ALS1622			DM74ALS1621 DM74ALS1622			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1621		22			22		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			14			14		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1621		22			22		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			14			14		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1621		33			33		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			24			24		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1621		33			33		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			24			24		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1622		25			25		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			13			13		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1622		25			25		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			13			13		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1622		31			31		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			28			28		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1622		31			31		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			28			28		ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

Function Table

Enable Inputs		Operation	
$\overline{G}BA$	GAB	ALS1622	ALS1621
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus
H	H	$\overline{A}$ Data to B Bus	A Data to B Bus
H	L	Hi	Hi
L	H	$\overline{B}$ Data to A Bus $\overline{A}$ Data to B Bus	B Data to A Bus A Data to B Bus

National Semiconductor

PRELIMINARY

DM54ALS1623/DM74ALS1623 Octal TRI-STATE® Bus Transceiver

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE log elements configured as an octal bus transceiver. It is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives the ALS1623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Features

- Low power version of ALS623
- Advanced oxide-isolated, ion implanted Schottky process
- TRI-STATE outputs on A and B buses
- PNP input design reduces input loading
- Local bus-latch capability
- Switching response specified into 500Ω/50 pF load
- Switching specifications guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

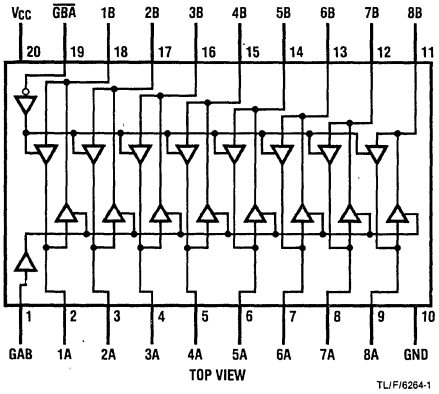
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54ALS1623 (J) **74ALS1623 (J, N)**

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	
L	L	B Data to A Bus
H	H	A Data to B Bus
H	L	Hi-Z
L	H	B Data to A Bus
		A Data to B Bus

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1623			DM74ALS1623			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	DM74ALS1623-1						24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

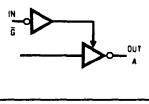
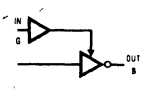
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		DM54ALS1623			DM74ALS1623			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 45V$, $I_{IN} = -18$ mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3$ mA		2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5V$, $I_{OH} = Max$		2			2			V
		$I_{OH} = -0.4$ mA, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 8$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 16$ mA					0.35	0.5	V
			For 74ALS-1 Option Only $I_{OL} = 24$ mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	A or B Ports			20			20	mA
			Control Inputs			20			20	mA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	A or B Ports			−0.1			−0.1	mA
			Control Inputs			−0.1			−0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		11			11		mA
			Outputs Low		18			18		mA
			TRI-STATE		13			13		mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS1623			DM74ALS1623			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output			8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			8			8		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output			8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			8			8		ns
t_{PZL}	Output Enable Time to Low Level			21			21		ns
t_{PZH}	Output Enable Time to High Level			18			18		ns
t_{PLZ}	Output Disable Time from Low Level			13			13		ns
t_{PHZ}	Output Disable Time from High Level			12			12		ns
t_{PZL}	Output Enable Time to Low Level			21			21		ns
t_{PZH}	Output Enable Time to Low Level			18			18		ns
t_{PLZ}	Output Disable Time from Low Level			13			13		ns
t_{PHZ}	Output Disable Time from High Level			12			12		ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

Note 3: $I_{OL} = 24$ mA for -1 option.

National Semiconductor

PRELIMINARY

DM54ALS1638/DM74ALS1638, DM54ALS1639/DM74ALS1639 Octal Bus Transceivers

General Description

These advanced low power Schottky TRI-STATE® octal bus transceivers are designed to provide high speed bidirectional communication between data buses. The output characteristics of the circuits are low enough impedance to drive transmission lines terminated down to 133Ω. The input characteristics of the circuits are high impedance so they will not significantly load the transmission line. These devices allow 8-bit wide bidirectional data transmission controlled by the logic level at the (DIR) input. The TRI-STATE enable input ($\overline{G}$) can be used to isolate both buses. In addition, the TRI-STATE circuitry contains a protection feature that prevents the buffer from glitching the bus during power-up or power-down. To provide design flexibility, the 'ALS1638 and 'ALS1639 have open-collector outputs on the A bus and TRI-STATE outputs on the B bus.

The DM74ALS-1 version of these devices is identical to its standard counterparts except that maximum recommended I_{OL} has been increased to 24 mA. There is no 54ALS-1 version of these parts.

Features

- Low power versions of ALS638, 639
- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74ALS638, 639
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current 74ALS-1 = 24 mA, 74ALS = 16 mA, 54ALS = 8 mA
- Glitch-free bus during power-up/down
- A bus outputs are open-collector, B bus outputs are TRI-STATE

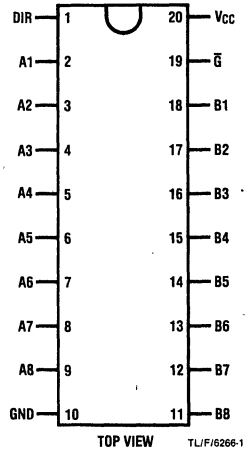
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	
Control Inputs	7V
A Bus I/O Ports	7V
B Bus I/O Ports	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/6266-1

DM54ALS1638, DM54ALS1639 (J)
DM74ALS1638, DM74ALS1639 (N)

Function Table

Control Inputs		Operation	
$\overline{G}$	DIR	'ALS1638	'ALS1639
L	L	B data to A bus	B data to A bus
L	H	A data to B bus	A data to B bus
H	X	Isolation	Isolation

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1638 DM54ALS1639			DM74ALS1638 DM74ALS1639			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current, B Bus Only			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	74ALS-1			—			24	mA
V_{OH}	High Level Output Voltage, A Bus Only			5.5			5.5	V
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS			DM74ALS			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC}=4.5V$, $I_I=-18$ mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage, B Bus Only	$V_{CC}=4.5V$ to 5.5V	$I_{OH}=-0.4$ mA	$V_{CC}-2$			$V_{CC}-2$			V
		$V_{CC}=4.5V$	$I_{OH}=-3$ mA	2.4			2.4			V
			$I_{OH}=$ Max	2			2			V
V_{OL}	Low Level Output Voltage	$V_{CC}=4.5V$ $I_{OL}=8$ mA			0.25	0.4		0.25	0.4	V
		$I_{OL}=16$ mA			—	—		0.35	0.5	V
		$I_{OL}=24$ mA for -1 Options						0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC}=5.5V$, $V_I=7V$ (Control Inputs)				0.1			0.1	mA
		$V_I=5.5V$ (I/O Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC}=5.5V$, $V_I=2.7V$				20			20	μA
I_{IL}	Low Level Input Current	$V_{CC}=5.5V$, $V_{IL}=0.4V$ (Control Inputs)				−0.10			−0.10	mA
		(I/O Port)				−0.10			−0.10	mA
I_O	Output Drive Current	$V_{CC}=5.5V$, $V_O=2.25V$ (B Ports Only)		−30		−112	−30		−112	mA
I_{OH}	High Level Output Current	$V_{CC}=4.5V$, $V_{OH}=5.5V$ (A Bus Only)				0.1			0.1	mA
I_{CC}	Supply Current ALS1638	$V_{CC}=5.5V$, Outputs High			21			21		mA
		Outputs Low			23			23		mA
		Outputs Disabled			25			25		mA
	ALS1639	Outputs High			21			21		mA
		Outputs Low			23			23		mA
		Outputs Disabled			25			25		mA

'ALS1638 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω (A Outputs), T_A = Min to Max						Units
			DM54ALS1638			DM74ALS1638			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	B		6			6		ns
t_{PHL}				21			21		ns
t_{PLH}	B	A		6			6		ns
t_{PHL}				8			8		ns
t_{PLH}	$\overline{G}$	A		23			23		ns
t_{PHL}				17			17		ns
t_{PZH}	$\overline{G}$	B		12			12		ns
t_{PZL}				15			15		ns
t_{PHZ}	$\overline{G}$	B		6			6		ns
t_{PLZ}				7			7		ns

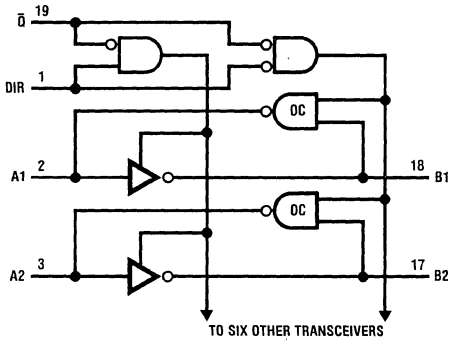
'ALS1639 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1639			DM74ALS1639			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	B		7			7		ns
t_{PHL}				21			21		ns
t_{PLH}	B	A		7			7		ns
t_{PHL}				9			9		ns
t_{PLH}	$\overline{G}$	A		23			23		ns
t_{PHL}				19			19		ns
t_{PZH}	$\overline{G}$	B		14			14		ns
t_{PZL}				17			17		ns
t_{PHZ}	$\overline{G}$	B		7			7		ns
t_{PLZ}				9			9		ns

Note 1: See Section 1 for test waveforms and output load.

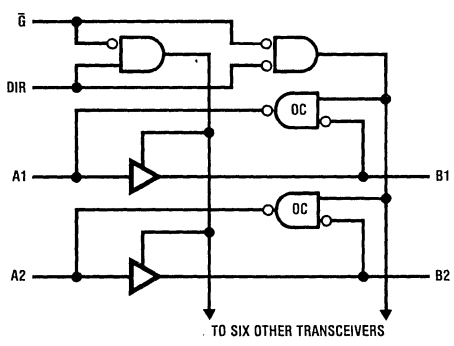
Logic Diagrams

'ALS1638



TL/F/6266-2

'ALS1639



TL/F/6266-3

OC denotes open-collector outputs

National Semiconductor

DM54ALS1640/DM74ALS1640, DM54ALS1643/DM74ALS1643, DM54ALS1645/DM74ALS1645 Octal TRI-STATE® Bus Transceivers

General Description

This family of advanced low power Schottky devices contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data either transmits from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode, so that the buses are effectively isolated. The TRI-STATE circuitry also contains a protection feature that prevents the buffer from glitching the bus during power-up or power-down.

Features

- Low power versions of ALS640A, ALS643A, ALS645A
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Choice of true or inverting logic
- PNP input design reduces input loading
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

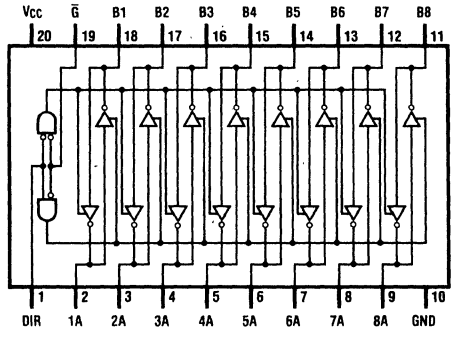
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

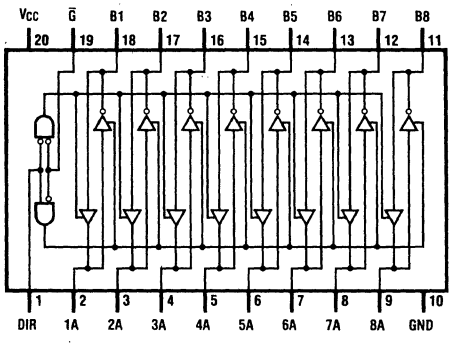
Connection Diagrams

Dual-In-Line Packages



TL/F/6267-1

54ALS1640 (J) 74ALS1640 (J, N)

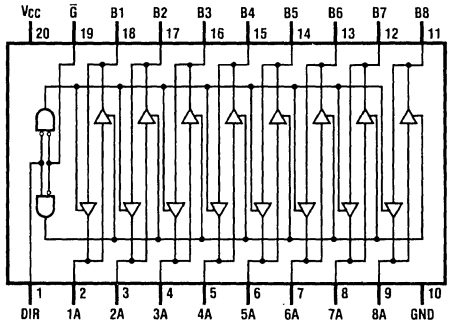


TL/F/6267-2

54ALS1643 (J) 74ALS1643 (J, N)

Connection Diagrams (Continued)

Dual-In-Line Package



TL/F/6267-3

54ALS1645 (J) 74ALS1645 (J, N)

Function Table

Control Inputs		Operation		
$\overline{G}$	DIR	ALS1640	ALS1643	ALS1645
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus	B Data to A Bus
L	H	$\overline{A}$ Data to B Bus	$\overline{A}$ Data to B Bus	A Data to B Bus
H	X	Hi-Z	Hi-Z	Hi-Z

Recommended Operating Conditions

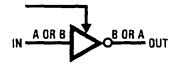
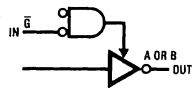
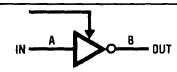
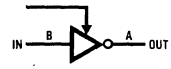
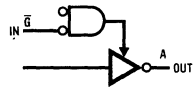
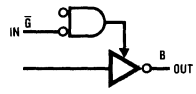
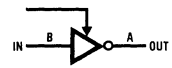
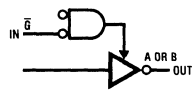
Symbol	Parameter	DM54ALS1640 DM54ALS1643 DM54ALS1645			DM74ALS1640 DM74ALS1643 DM74ALS1645			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
	74ALS-1 Option Only						24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions		DM54ALS1640 DM74ALS1640			DM54ALS1643 DM74ALS1643			DM54ALS1645 DM74ALS1645			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5			−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max		2	2.3		2	2.3		2	2.3		V
		I_{OH} = −0.4 mA		V_{CC} − 2			V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 8 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA (74ALS Only) I_{OL} = 24 mA (-1 Options Only)		0.35	0.5		0.35	0.5		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_{IN} = 7V Control Inputs			0.1			0.1			0.1	mA
			V_{IN} = 5.5V A or B Ports										
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1			−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	DM54		18	35		22			25	40	mA
			DM74		18	32		22			25	36	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54ALS			DM74ALS			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1640	5		17	5		15	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		13	2		10	ns
t_{PZL}	Output Enable Time to Low Level	 ALS1640	5		25	5		22	ns
t_{PZH}	Output Enable Time to High Level		5		23	5		20	ns
t_{PLZ}	Output Disable Time from Low Level		5		16	5		13	ns
t_{PHZ}	Output Disable Time from High Level		2		12	2		10	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1643		7			7		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			7			7		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1643		8			8		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			8			8		ns
t_{PZL}	Output Enable Time to Low Level	 ALS1643		21			21		ns
t_{PZH}	Output Enable Time to High Level			18			18		ns
t_{PLZ}	Output Disable Time from Low Level			13			13		ns
t_{PHZ}	Output Disable Time from High Level			12			12		ns
t_{PZL}	Output Enable Time to Low Level	 ALS1643		21			21		ns
t_{PZH}	Output Enable Time to High Level			18			18		ns
t_{PLZ}	Output Disable Time from Low Level			13			13		ns
t_{PHZ}	Output Disable Time from High Level			12			12		ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 ALS1645	2		15	2		13	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2		15	2		13	ns
t_{PZL}	Output Enable Time to Low Level	 ALS1645	8		28	8		25	ns
t_{PZH}	Output Enable Time to High Level		8		28	8		25	ns
t_{PLZ}	Output Disable Time from Low Level		3		22	3		18	ns
t_{PHZ}	Output Disable Time from High Level		2		14	2		12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

National Semiconductor

PRELIMINARY

DM54ALS1641/DM74ALS1641, DM54ALS1642/DM74ALS1642, DM54ALS1644/DM74ALS1644 Octal Bus Transceivers

General Description

These advanced low power Schottky TRI-STATE® octal bus transceivers are designed to provide high speed bidirectional communication between data buses. The output characteristics of the circuits are low enough impedance to drive transmission lines terminated down to 133Ω. The input characteristics of the circuits are high impedance so they will not significantly load the transmission line. These devices allow 8-bit wide bidirectional data transmission controlled by the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to isolate both buses. The 'ALS1641, 'ALS1642 and 'ALS1644 have open-collector outputs on both the A bus and the B bus.

Features

- PNP input design reduces input loading
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Switching response specified into 500Ω and 50 pF
- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Improved switching performance with less power dissipation compared with 54/74LS counterpart
- Functional and pin compatible with 54/74LS counterpart
- Low power versions of 'ALS641, 642, 644
- Glitch-free bus during power-up/down

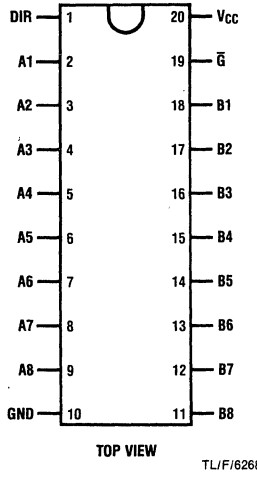
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6268-1

54ALS1641, 1642, 1644 (J)
74ALS1641, 1642, 1644 (N)

Function Table

Control Inputs		Operation		
$\overline{G}$	DIR	'ALS1642	'ALS1641	'ALS1644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

Circuit Configurations

Device	Output	Logic
'ALS1641	Open-Collector	True
'ALS1642	Open-Collector	Inverting
'ALS1644	Open-Collector	True and Inverting

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1641 DM54ALS1642 DM54ALS1644			DM74ALS1641 DM74ALS1642 DM74ALS1644			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			8			16	mA
	74ALS-1						24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54ALS			DM74ALS			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = − 18 mA			−1.5			−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V							
		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 24 mA					0.35	0.5	V
	DM74ALS-1	I_{OL} = 48 mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
		V_I = 5.5V (I/O Port)			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20			20	µA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1			−0.1	mA
		(I/O Port)			−0.1			−0.1	mA
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V			0.1			0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V							
	ALS1641			23			23		mA
	ALS1642			20			20		mA
	ALS1644			22			22		mA

'ALS1641 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1641			DM74ALS1641			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A		22			22		ns
t_{PHL}				14			14		ns
t_{PLH}	$\overline{G}$ or DIR	A or B		26			26		ns
t_{PHL}				26			26		ns

'ALS1642 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1642			DM74ALS1642			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A		25			25		ns
t_{PHL}				13			13		ns
t_{PLH}	$\overline{G}$ or DIR	A or B		29			29		ns
t_{PHL}				29			29		ns

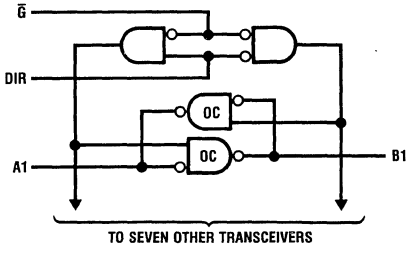
'ALS1644 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1644			DM74ALS1644			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	B		27			27		ns
t_{PHL}				19			19		ns
t_{PLH}	B	A		24			24		ns
t_{PHL}				17			17		ns
t_{PLH}	$\overline{G}$	A		30			30		ns
t_{PHL}				27			27		ns
t_{PLH}	$\overline{G}$	B		24			24		ns
t_{PHL}				30			30		ns
t_{PLH}	DIR	A		30			30		ns
t_{PHL}				27			27		ns
t_{PLH}	DIR	B		24			24		ns
t_{PHL}				30			30		ns

Note 1: See Section 1 for test waveforms and output load.

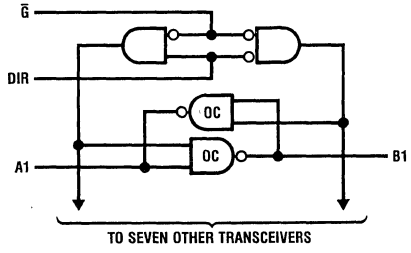
Logic Diagrams

'ALS1641



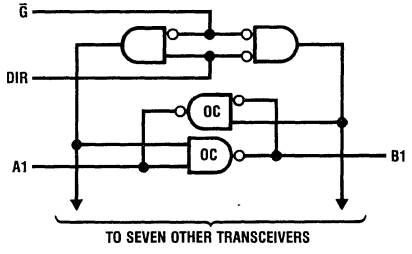
TL/F/6268-2

'ALS1642



TL/F/6268-3

'ALS1644



TL/F/6268-4

OC denotes open-collector outputs

Section 3

Advanced Schottky

3

Section Contents

Section Contents (Continued)

Section Contents (Continued)

National Semiconductor

DM54AS00/DM74AS00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterpart.

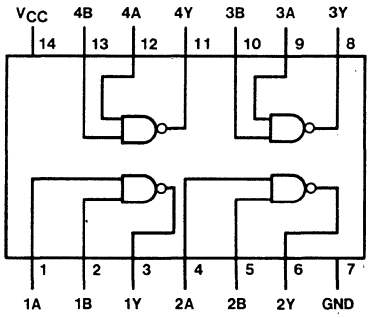
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/L/6105-1

54AS00 (J) **74AS00 (J,N)**

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS00			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.2	3.2	mA
			Outputs Low		10.8	17.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS00			DM74AS00			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		5	1		4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		5	1		4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS02/DM74AS02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings (Note 1)

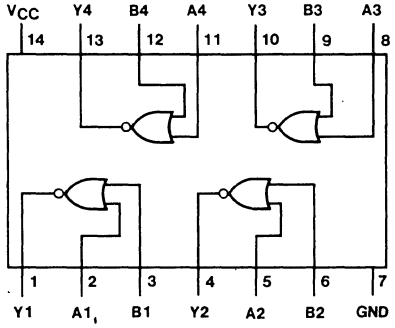
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6272-1

54AS02 (J) 74AS02 (J,N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54/74AS02			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3.7	5.9	mA
			Outputs Low		12.5	20.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS02			DM74AS02			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		5	1		4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		5	1		4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS04/DM74AS04 Hex Inverters

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

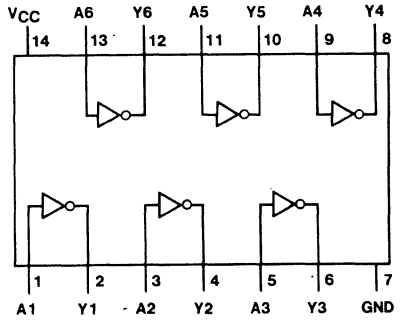
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6273-1

54AS04 (J) 74AS04 (J,N)

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

3

Recommended Operating Conditions

Parameter	DM54AS04			DM74AS04			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−2			−2	mA
Low Level Output Current, I_{OL}			20			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	4.8	mA
			Outputs Low		14	26.3	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS04			DM74AS04			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6	1		5	ns
T_{PHL}, Propagation delay time. High to low level output		1		4.5	1		4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS08/DM74AS08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

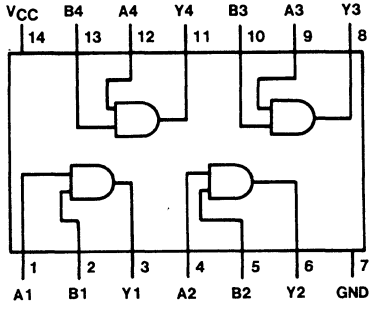
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/L/6106-1

54AS08 (J) 74AS08 (J,N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS08			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		5.8	9.3	mA
			Outputs Low		14.9	24	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS08			DM74AS08			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		5.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		6.5	1		5.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS10/DM74AS10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

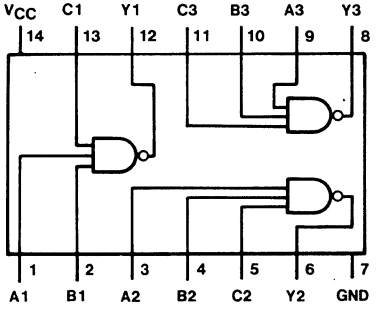
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6274-1

54AS10 (J) 74AS10 (J,N)

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS10			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.5	2.4	mA
			Outputs Low		8.1	13	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS10			DM74AS10			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		5	1		4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		5	1		4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS11/DM74AS11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

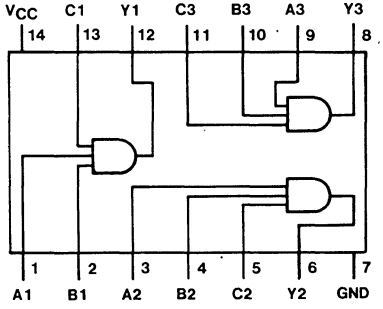
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6275-1

54AS11 (J) 74AS11 (J,N)

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54/74AS11			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.3	7	mA
			Outputs Low		11.2	18	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS11			DM74AS11			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		6	ns
T_{PHL}, Propagation delay time. High to low level output		1		6.5	1		5.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS20/DM74AS20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

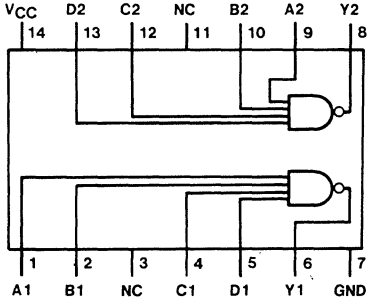
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6276-1

54AS20 (J) 74AS20 (J,N)

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS20			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.1	1.6	mA
			Outputs Low		6	8.7	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS20			DM74AS20			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		5.5	1		5	ns
T_{PHL}, Propagation delay time. High to low level output		1		5	1		4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS21/DM74AS21 Dual 4-Input AND Gates

General Description

This device contains two independent 4-input gates, each of which performs the logic AND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

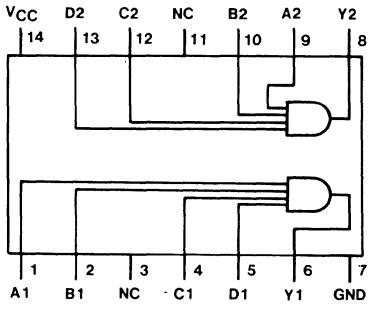
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6277-1

54AS21 (J) 74AS21 (J,N)

Function Table

Inputs				Output
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS21			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.9	4.6	mA
			Outputs Low		7.4	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS21			DM74AS21			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		6	ns
T_{PHL}, Propagation delay time. High to low level output		1		6.5	1		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS27/DM74AS27 Triple 3-Input NOR Gates

General Description

This device contains three independent 3-input gates, each of which performs the logic NOR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

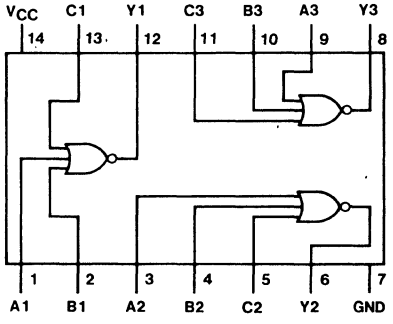
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6278-1

54AS27 (J) 74AS27 (J,N)

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	B	C	Y
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS27			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4	6.4	mA
			Outputs Low		10.6	17.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS27			DM74AS27			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		5.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		5	1		4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS30/DM74AS30 8 Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

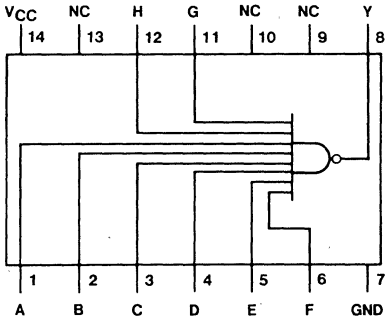
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6279-1

54AS30 (J) 74AS30 (J,N)

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS30			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1	1.5	mA
			Outputs Low		3.4	4.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS30			DM74AS30			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		5.5	1		5	ns
T_{PHL}, Propagation delay time. High to low level output		1		5	1		4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS32/DM74AS32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

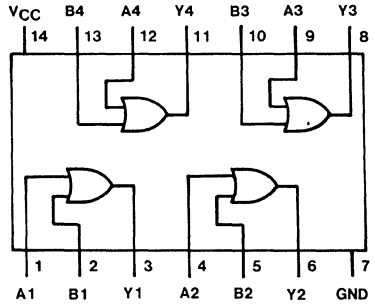
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6280-1

54AS32 (J) 74AS32 (J,N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

3

Recommended Operating Conditions

Parameter	DM54/74AS32			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		7.3	12	mA
			Outputs Low		16.5	26.6	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS32			DM74AS32			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	1		7.5	1		5.8	ns
T_{PHL}, Propagation delay time. High to low level output		1		6.5	2		5.8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS34/DM74AS34 Hex Non-Inverter

General Description

These devices contain six independent gates, each of which performs the logic identity function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

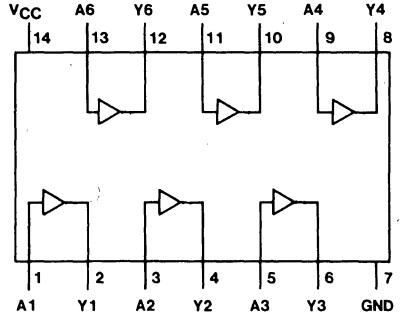
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6281-1

54AS34 (J) 74AS34 (J, N)

Function Table

$Y = \overline{A}$

Input A	Output Y
H	H
L	L

3

Recommended Operating Conditions

Parameter	DM54/74AS34			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		7.4	12	mA
			Outputs Low		21.3	34.6	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54/74AS34			DM54/74AS34			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		5.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		7	1		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS74/DM74AS74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54AS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\bar{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-For-Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S74 at Approximately Half the Power.

Absolute Maximum Ratings (Note 1)

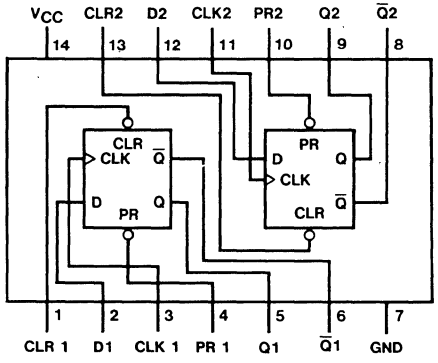
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6282-1

54AS74 (J) 74AS74 (J,N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Q_0 = Previous Condition of Q
* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54AS74			DM74AS74			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock frequency, f_{CLOCK}		0		90	0		105	MHz
Width of Clock Pulse, T_W	High	4			4			ns
	Low	5.5			5.5			ns
Pulse Width T_W, Preset & Clear	Low	4			4			ns
Data Setup Time, T_{SU}	High	4.5↑			4.5↑			ns
	Low	4.5↑			4.5↑			ns
PRE or CLR Setup Time		2↑			2↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18mA$			−1.2	V
V_{OH}	High Level Output Voltage		$V_{CC} = 4.5V$ to $5.5V$ $I_{OH} = -2mA$	$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = Max$ $I_{OL} = 20mA$		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$ $V_{IH} = 7V$			0.1	mA
I_{IH}	High Level Input Current	Clock, D	$V_{CC} = 5.5V$ $V_{IH} = 2.7V$			20	μA
		Preset, Clear				40	μA
I_{IL}	Low Level Input Current	Clock, D	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$			−0.5	mA
		Preset, Clear				−1.8	mA
I_O	Output Drive Current		$V_{CC} = 5.5V$ $V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$		10.5	16	mA

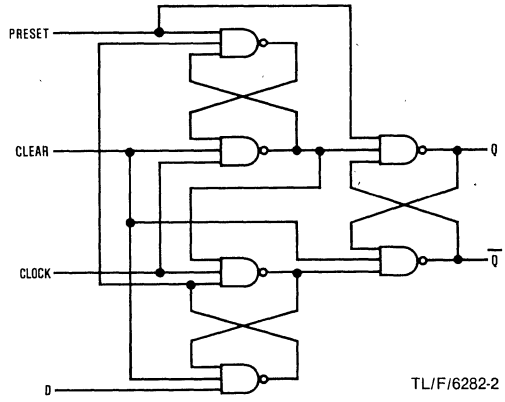
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS74			DM74AS74			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	90			105			MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3		8.5	3.3		7.5	ns
T_{PHL}				3.5		11.5	3.5		10.5	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3.5		9	3.5		8	ns
T_{PHL}				4.5		10.5	4.5		9	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6282-2

National Semiconductor

PRELIMINARY

DM54AS86/DM74AS86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

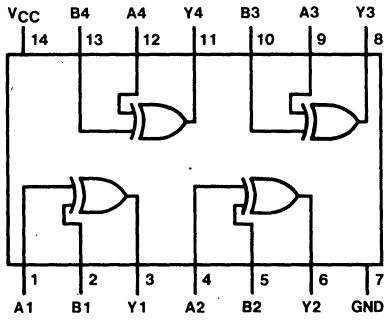
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6283-1

54AS86 (J) **74AS86 (J, N)**

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Outputs
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54AS86/DM74AS86			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V I_{OH} = −2 mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High				mA
			Outputs Low				mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS86			DM74AS86			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.							ns
T_{PHL}, Propagation delay time. High to low level output								ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS95/DM74AS95 4-Bit Parallel Access Shift Register

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction of Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the 4 bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock 2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

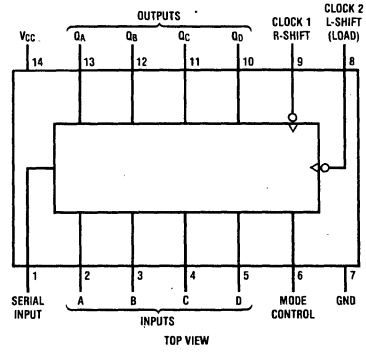
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

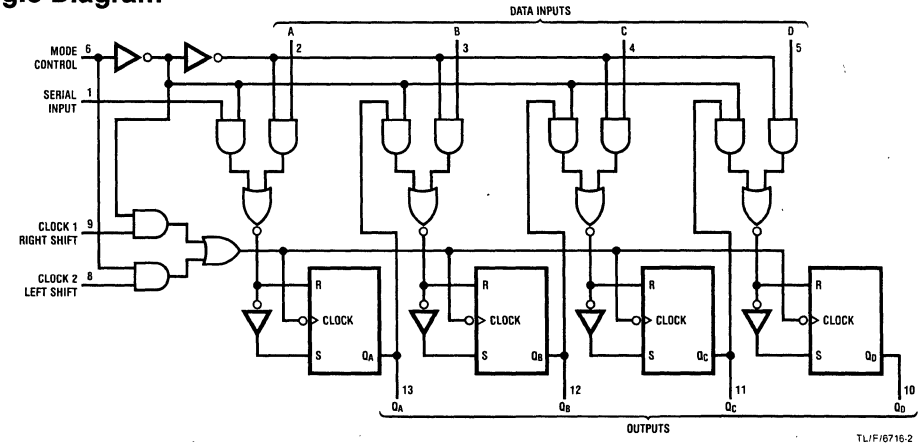
Dual-In-Line Package



TL/F/6716-1

DM54AS95 (J) DM74AS95 (J, N)

Logic Diagram



TL/F/6716-2

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = high level (steady-state), L = low level (steady-state), X = don't care (any input, including transitions).

↓ = transition from high-to-low level, ↑ = transition from low-to-high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Recommended Operating Conditions

Symbol	Parameter		DM54AS95			DM74AS95			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−2	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency		0		80	0		100	MHz
$t_{W(CLK)}$	Clock Pulse Width		6.5			5			ns
t_{SU}	Data Set-Up Time		2.5↓			2↓			ns
t_H	Hold Time	Data	2.5↓			2.5↓			ns
		CLK1 to Mode	3.5↓			3↓			ns
		CLK2 to Mode	1↓			0↓			ns
t_{EN}	Clock Enable Time	Clock 1	13			12			ns
		Clock 2	13			12			ns
t_{IN}	Clock Inhibit Time	Clock 1	3			2.5			ns
		Clock 2	1			0			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

Parameter	Conditions		DM54AS95			DM74AS95			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = Min, I_{OL} = 20 mA			0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	V_{CC} = 5.5V, V_{IL} = 0.4V	Mode			−1			−1	mA
		Others			−0.5			−0.5	mA
I_O	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5V			21	34		21	34	mA
I_{CCL}	V_{CC} = 5.5V			26.1	39		26.1	39	mA

Switching Characteristics over recommended operating free-air temperature range

Parameter	Input	Output	Conditions	DM54AS95			DM74AS95			Units
				Min	Typ	Max	Min	Typ	Max	
f_{MAX}, Maximum Clock Frequency				100			100			MHz
t_{PLH}, Propagation Delay Time, Low to High Level Output	Clock	Q	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2		11			10	ns
t_{PLH}, Propagation Delay Time, High to Low Level Output	Clock	Q		2		10.5			9.5	ns

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54AS109/DM74AS109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54AS109 is a dual edge-triggered flip-flop. Each flip-flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or $\overline{K}$ is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The J$\overline{K}$ design allows operation as a D flip flop by tying the J and $\overline{K}$ inputs together.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S109 at Approximately Half the Power.

Absolute Maximum Ratings (Note 1)

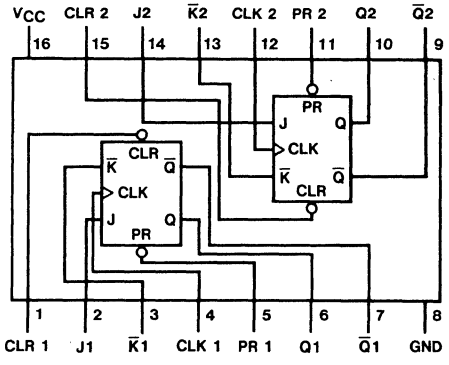
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6284-1

54AS109 (J) 74AS109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54AS109			DM74AS109			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, fCLOCK		0		90	0		105	MHz
Pulse Width T_W	Clock High	4			4			ns
	Clock Low	5.5			5.5			ns
Pulse Width T_W, Preset & Clear		4			4			ns
Data Setup Time, T_{SU}	J or $\overline{K}$	5.5↑			5.5↑			ns
	PRE or CLR inactive	2↑			2↑			
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V, I_I = −18mA			−1.2	V
V_{OH}	High Level Output Voltage		I_{OH} = −2mA V_{CC} = 4.5V to 5.5V	V_{CC} −2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V V_{IH} = 2V I_{OL} = 20mA		0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V, V_{IH} = 7V			0.1	mA
I_{IH}	High Level Input Current	Clock, J, $\overline{K}$	V_{CC} = 5.5V, V_{IH} = 2.7V			20	μA
		Preset, Clear				40	
I_{IL}	Low Level Input Current	Clock, J, $\overline{K}$	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.5	mA
		Preset, Clear				−1.8	
I_O	Output Drive Current		V_O = 2.25V, V_{CC} = 5.5V	−30		−112	mA
I_{CC}	Supply Current		V_{CC} = 5.5V		11.5	17	mA

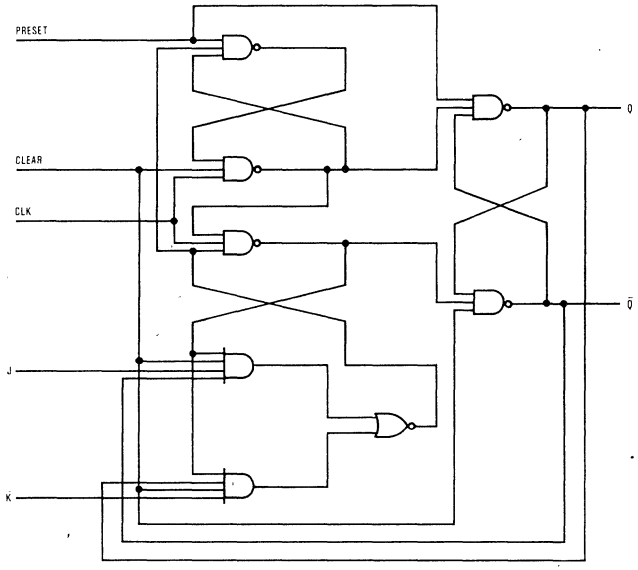
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS109			DM74AS109			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	90			105			MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3		9	3		8	ns
T_{PHL}				3.5		11.5	3.5		10.5	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3.5		10	3.5		9	ns
T_{PHL}				4.5		10.5	4.5		9	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6284-2

National Semiconductor

PRELIMINARY

DM54AS112/DM74AS112 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54AS112 is a dual edge-triggered flip-flop. Each flip-flop has individual J, K, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

By tying the J K inputs high, these devices can operate as toggle flip-flops.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S112 at Approximately Half the Power.

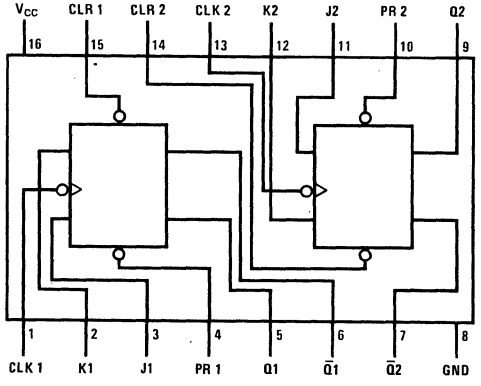
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6285-1

54AS112 (J) **74AS112 (J, N)**

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q0	$\overline{Q}$0

L = Low State, H = High State, X = Don't Care

↓ = Negative Edge Transition, Q0 = Previous Condition of Q

*This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54AS112			DM74AS112			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, fCLOCK		0			0			MHz
Pulse Width T_W	Clock High							ns
	Clock Low							ns
Pulse Width T_W, Preset & Clear								ns
Data Setup Time, T_{SU}	J or K							ns
	PRE inactive							
Data Hold Time, T_H ↓								ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics *over recommended operating free air temperature range.*

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18mA$			−1.2	V
V_{OH}	High Level Output Voltage		$I_{OH} = -2mA$ $V_{CC} = 4.5V$ to $5.5V$	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$ $I_{OL} = 20mA$		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$				mA
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				μA
		Preset, Clear					
I_{IL}	Low Level Input Current	Clock	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		−5		mA
		J, K			−1		
		Preset, Clear			−5.5		
I_O	Output Drive Current		$V_O = 2.25V$, $V_{CC} = 5.5V$	−30		−112	mA
I_{CC}	Supply Current (Note 1)		$V_{CC} = 5.5V$		38		mA

Note 1: I_{CC} is measured with outputs open and J, K, CLK, PRE grounded, then with J, K, CLK, and CLR grounded.

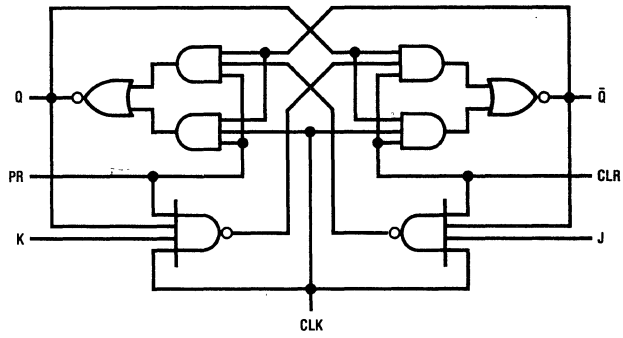
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS112			DM74AS112			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		175			175		MHz
T_{PLH}	Preset	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns
T_{PLH}	Clock	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6285-2

National Semiconductor

PRELIMINARY

DM54AS113/DM74AS113 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

General Description

The DM54AS113 is a dual-edge-triggered flip-flops. Each flip-flop has individual J, K, clock, and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset inputs will set Q output upon the application of low level signal.

The JK design allows operation as a toggle flip-flop by tying the J and K inputs high.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S113 at Approximately Half the Power.

Absolute Maximum Ratings (Note 1)

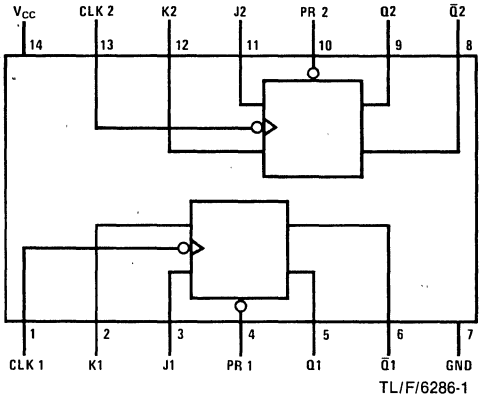
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6286-1

54AS113 (J) **74AS113 (J, N)**

Function Table

Inputs				Outputs	
PR	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	H	X	X	Q0	$\overline{Q}$0

L = Low State, H = High State, X = Don't Care
↓ = Negative Edge Transition, Q0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54AS113			DM74AS113			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, fCLOCK		0			0			MHz
Pulse Width T_W	Clock High							ns
	Clock Low							ns
Pulse Width T_W, Preset								ns
Data Setup Time, T_{SU}	J or K							ns
	PRE inactive							
Data Hold Time, T_H								ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18mA$			−1.2	V
V_{OH}	High Level Output Voltage		$I_{OH} = -2mA$ $V_{CC} = 4.5V$ to $5.5V$	V_{CC} −2			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$ $I_{OL} = 20mA$		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA
I_{IH}	High Level Input Current	Clock, J, K	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA
		Preset				40	
I_{IL}	Low Level Input Current	Clock	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		−5		mA
		J, K			−1		
		Preset			−5.5		
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$		38		mA

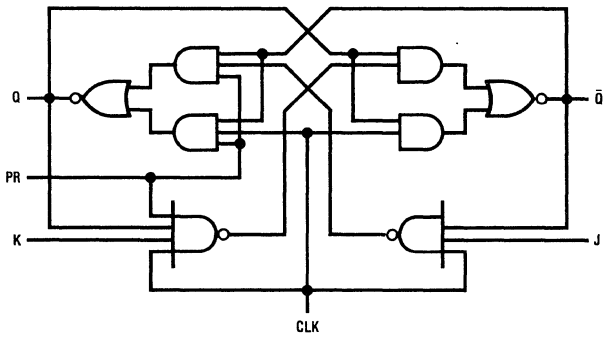
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS113			DM74AS113			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		175			175		MHz
T_{PLH}	Preset	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns
T_{PLH}	Clock	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6286-2

National Semiconductor

PRELIMINARY

DM54AS114/DM74AS114 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear and Common Clock

General Description

The DM54AS114 is a dual edge-triggered flip-flop. Each flip-flop has individual J, K, and preset inputs, and also complementary Q and Q outputs. The clear and clock inputs are common to both flip-flops.

Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, K input signal has no effect.

Asynchronous preset and common clear inputs will set or clear Q outputs respectively upon the application of low level signal.

The JK design allows operation as a toggle flip-flop by tying the J and K inputs high.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S114 at Approximately Half the Power.

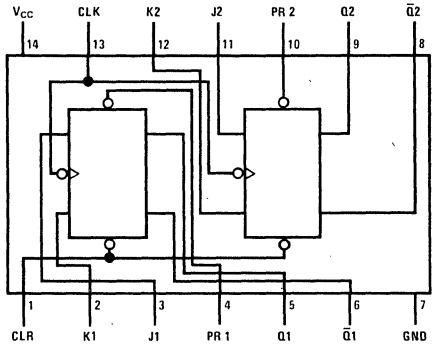
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6287-1

54AS114 (J) **74AS114 (J, N)**

Function Table

Inputs					Outputs	
PR	CLR	CK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	H	X	X	Q_0	$\bar{Q}_0$

L = Low State, H = High State, X = Don't Care
↓ = Negative Edge Transition, Q_0 = Previous Condition of Q
* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54AS114			DM74AS114			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, fCLOCK		0			0			MHz
Pulse Width T_W	Clock High							ns
	Clock Low							ns
Pulse Width T_W, Preset & Clear								ns
Data Setup Time, T_{SU}	J or K							ns
	PRE or CLR inactive							
Data Hold Time, T_H		↓			↓			ns

The (↓) arrow indicates the negative edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18mA$			−1.2	V
V_{OH}	High Level Output Voltage		$I_{OH} = -2mA$ $V_{CC} = 4.5V$ to $5.5V$	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$ $I_{OL} = 20mA$		0.35	0.5	V
I_I	Max High Input Current		$V_{CC} = 5.5V$, $V_{IH} = 7V$				mA
I_{IH}	High Level Input Current	Clock, J, $\overline{K}$	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				μA
		Preset					
I_{IL}	Low Level Input Current	Clock,	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		−10.5		mA
		J, $\overline{K}$			−1		
		Preset			−5.5		
		Clear			−11.5		
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$		38		mA

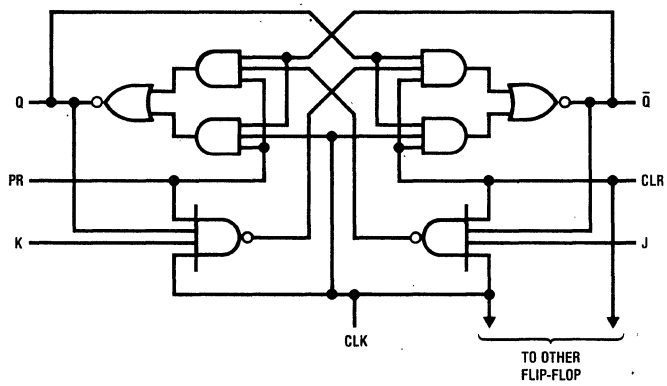
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS114			DM74AS114			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		175			175		MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns
T_{PLH}	Clock	Q or $\overline{Q}$			3			3		ns
T_{PHL}					4			4		ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6287-2

National Semiconductor

DM54AS131/DM74AS131 3-to-8 Line Decoders/Demultiplexers with Address Registers

General Description

The DM54/74AS131 is a 3-to-8 line decoder/demultiplexer with registers on the three address inputs. When the clock input (CLK) goes from low to high, the DM54/74AS131 acts as a decoder/demultiplexer, and the address present at the select inputs (A, B, and C) is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The DM54/74AS131 is ideally suited for implementing glitch-free decoders in strobed (stored address) applications in bus-oriented systems.

Features

- Combines decoder and 3-bit address register
- Incorporates 2 enable inputs to simplify cascading

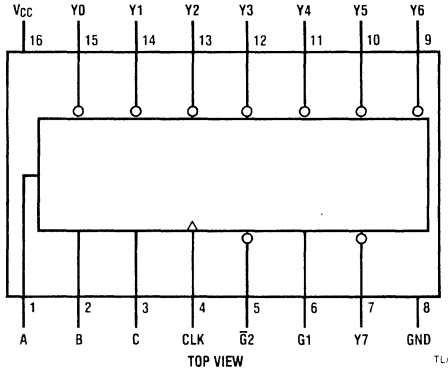
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



DM54AS131 (J) DM74AS131 (J, N)

Function Table

Inputs						Outputs							
CLK	Enable		Select										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L or H	H	L	X	X	X	Outputs Corresponding to Stored Address L. All Others H.							

Recommended Operating Conditions

Symbol	Parameter		DM54AS131			DM74AS131			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−2	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLOCK}	Clock Frequency		0		90	0		100	MHz
t_W	Clock Pulse Width	CLK High	5.5			5			ns
		CLK Low	5.5			5			
t_{SU}	Select Set-Up Time		3.5			3.5↑			ns
t_H	Select Hold Time		1			0↑			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

The arrow (↑) indicates that the positive going edge of the clock is used as reference.

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

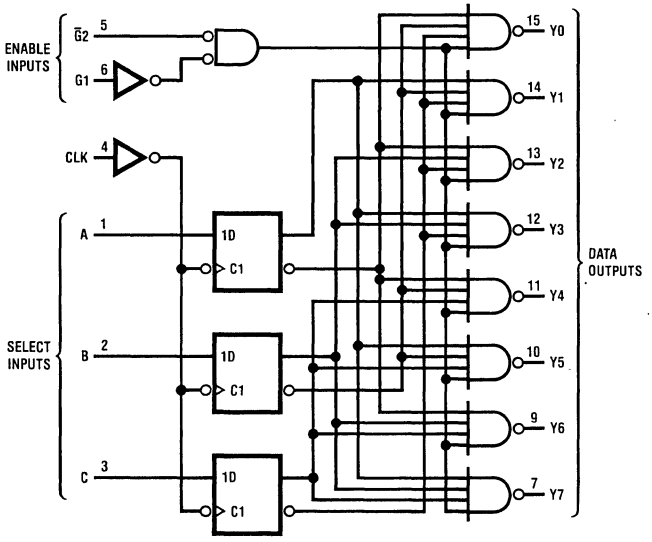
Parameter	Conditions	DM54AS131			DM74AS131			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5V, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = 5.5V, V_I = 0.4V			−1			−1	mA
I_O	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CCL}	V_{CC} = 5.5V		16	30		16	30	mA
I_{CCH}	V_{CC} = 5.5V		15	29		15	29	mA

Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS131			DM74AS131			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	Clock	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	2		10	2		9	ns
t_{PHL}	Clock	Y		2		10	2		9	ns
t_{PLH}	G1	Y		2		10.5	2		9.5	ns
t_{PHL}	G1	Y		2		9	2		8.5	ns
t_{PLH}	$\overline{G}2$	Y		2		7.5	2		7	ns
t_{PHL}	$\overline{G}2$	Y		2		8.5	2		8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Logic Diagram



TL/F/6717-2

National Semiconductor

PRELIMINARY

DM54AS136/DM74AS136 Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxidé-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterparts
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

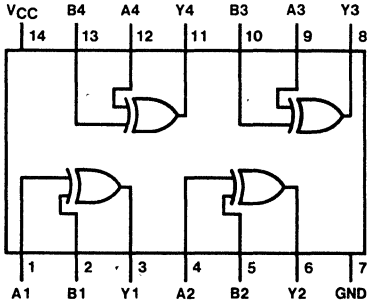
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6718-1

DM54AS136 (J) **DM74AS136 (N)**

Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54AS136			DM74AS136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.35	0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−0.5	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)				mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Parameter	Conditions	DM54AS136			DM74AS136			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF							ns
t_{PHL} Propagation Delay Time High to Low Level Output								ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF							ns
t_{PHL} Propagation Delay Time High to Low Level Output								ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

National Semiconductor

PRELIMINARY

DM54AS137/DM74AS137 3-to-8 Line Decoder/Demultiplexer with Address Latches

General Description

The DM54/74AS137 is a 3-to-8 line decoder/demultiplexer with latches on the three address inputs. When the latch enable input ($\overline{GL}$) is low, the DM54/74AS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The DM54/74AS137 is ideally suited for implementing glitch-free decoders in strobed (stored address) applications in bus-oriented systems.

Features

- Combines decoder and 3-bit address latch
- Incorporates 2 output enables to simplify cascading

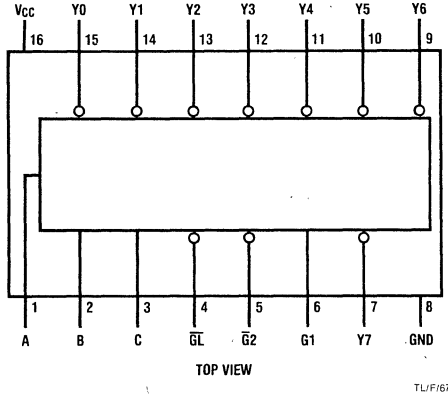
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



DM54AS137 (J) **DM74AS137 (J, N)**

Function Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output Corresponding to Stored Address, L, All Others, H							

Recommended Operating Conditions

Symbol	Parameter	DM54AS137			DM74AS137			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
t_W	Latch Enable Low Pulse Width							ns
t_{SU}	Select Set-Up Time with Respect to Latch Enable	4.5		4				ns
t_H	Select Hold Time with Respect to Latch Enable	1		1				ns
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

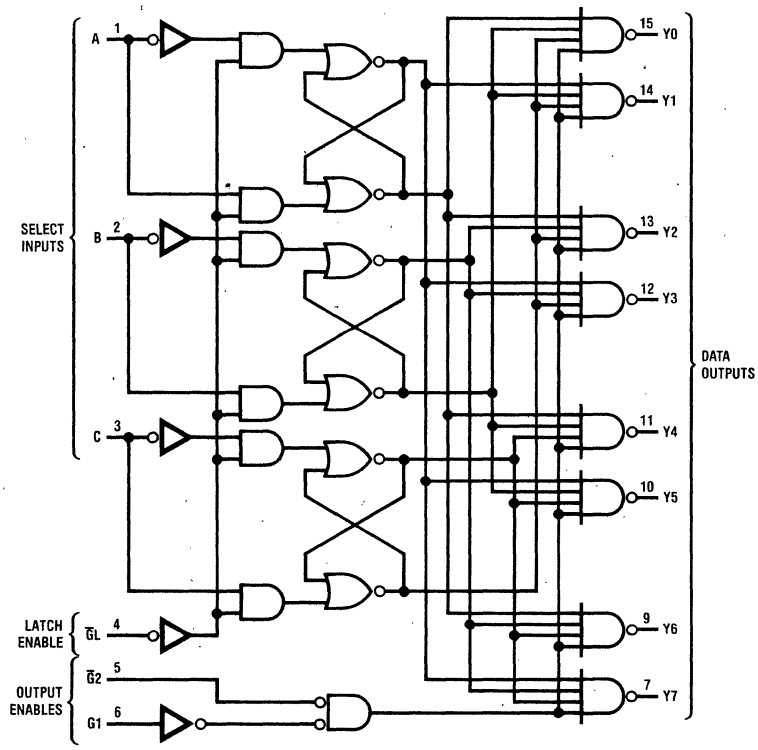
Parameter		Conditions	DM54AS137			DM74AS137			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5V to 5.5V, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	V_{CC} − 2			V_{CC} − 2			V
V_{OL}		V_{CC} = 4.5V, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5		0.35	0.5	V
I_I	Enable	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
	A, B, C				0.1			0.1	
I_{IH}	Enable	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
	A, B, C				20			20	
I_{IL}	Enable	V_{CC} = 5.5V, V_I = 0.4V			−1			−1	mA
	A, B, C				−1			−1	
I_O		V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5V		16	24		16	24	mA

Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS137			DM74AS137			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	A, B, C	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	2		14	2		12.5	ns
t_{PHL}	A, B, C	Y		2		14	2		12.5	ns
t_{PLH}	$\overline{G2}$	Y		2		8	2		7	ns
t_{PHL}	$\overline{G2}$	Y		2		8.5	2		8	ns
t_{PLH}	G1	Y		2		10.5	2		9.5	ns
t_{PHL}	G1	Y		2		9	2		8.5	ns
t_{PLH}	$\overline{GL}$	Y		2		14.5	2		13	ns
t_{PHL}	$\overline{GL}$	Y		2		14.5	2		13	ns

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Logic Diagram



TL/F/6719-2

National Semiconductor

PRELIMINARY

DM54AS138/DM74AS138 3-to-8 Line Decoder/Demultiplexer

General Description

The DM54/74AS138 circuit is designed to be used in high performance memory decoding or data routing applications requiring very short propagation delay times. In high performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Features

- Designed specifically for high speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception

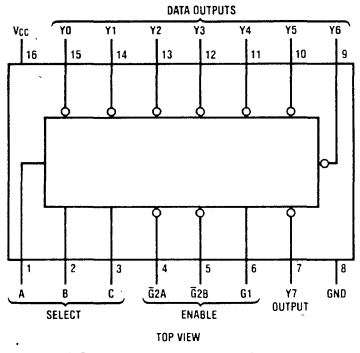
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6720-1

DM54AS138 (J) **DM74AS138 (J, N)**

Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

Recommended Operating Conditions

Symbol	Parameter	DM54AS138			DM74AS138			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

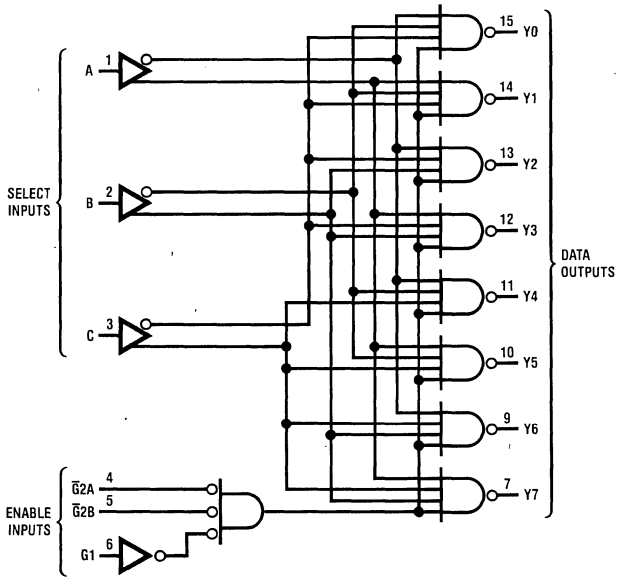
Parameter	Conditions	DM54AS138			DM74AS138			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5V, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5V, V_I = 7V							mA
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V							μA
I_{IL}	V_{CC} = 5.5V, V_{IL} = 0.4V							mA
I_O	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CCL}	V_{CC} = 5.5V		14	20		14	20	mA
I_{CCH}	V_{CC} = 5.5V		13	19		13	19	mA

Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS138			DM74AS138			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PHL}	A, B, C	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	2		9	2	5.6	8	ns
t_{PHL}	A, B, C	Y		2		11	2	6.4	9	ns
t_{PLH}	$\overline{G}2$	Y		2		8	2	5.8	7.5	ns
t_{PHL}	$\overline{G}2$	Y		2		9	2	5.5	7.5	ns
t_{PLH}	G1	Y		2	11.5		2		9	ns
t_{PHL}	G1	Y		2	10		2		8.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6720 2

National Semiconductor

PRELIMINARY

DM54AS151/DM74AS151 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. A Strobe input is provided which, when at the high level, disables all data inputs and forces the Y output to the low state and the W output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.

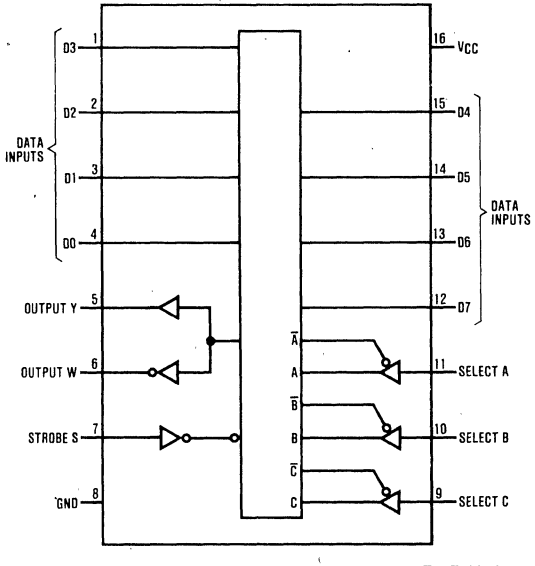
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS151	−55°C to 125°C
DM74AS151	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54AS151 (J) **74AS151(J,N)** TL/F/6288-1

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0 thru D7 = the level of the respective D input

Recommended Operating Conditions

Parameter	DM54AS151			DM74AS151			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		IOH = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V	A, B, C			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	A, B, C			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A,B,C			−1	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			18.6	30	mA

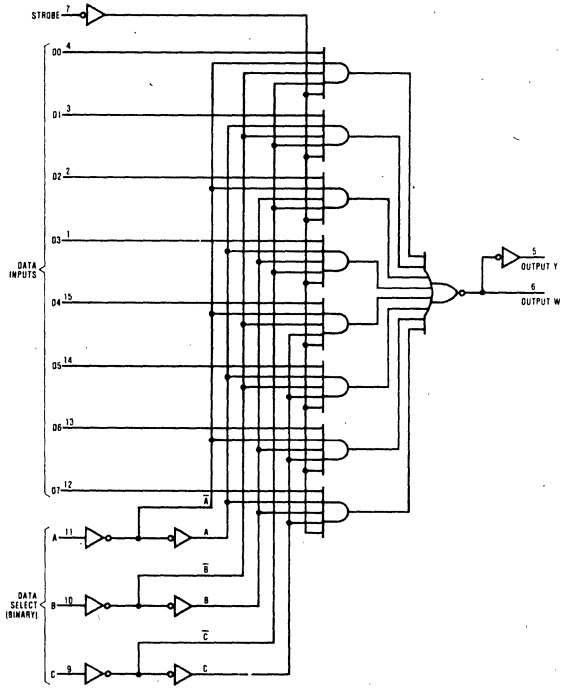
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS151			DM74AS151			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	4.5		16	4.5		14.5	ns
t_{PHL}, High to low Level Output				4.5		16	4.5		15	ns
t_{PLH}, Low to high Level Output		W		4		14.5	4		12	ns
t_{PHL}, High to low Level Output				4		14.5	4		12	ns
t_{PLH}, Low to high Level Output	Data	Y		3		11.5	3		10.5	ns
t_{PHL}, High to low Level Output				3		12	3		11	ns
t_{PLH}, Low to high Level Output		W		2		8	2		6.5	ns
t_{PHL}, High to low Level Output				1		5:5	1		4.5	ns
t_{PLH}, Low to high Level Output	Strobe	Y		4.5		16	4.5		14	ns
t_{PHL}, High to low Level Output				3		12.5	3		11	ns
t_{PLH}, Low to high Level Output		W		1.5		7	1.5		6.5	ns
t_{PHL}, High to low Level Output				3		11	3		10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6288-2

National Semiconductor

DM54AS153/DM74AS153 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and a non-inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the low state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.

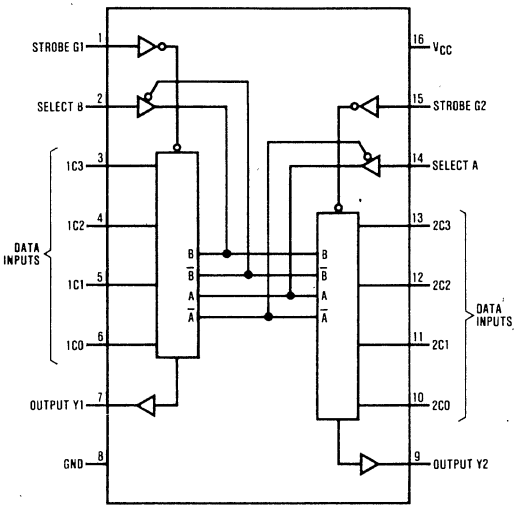
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS153	−55°C to 125°C
DM74AS153	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6289-1

54AS153 (J) 74AS153 (J,N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections
H = High Level L = Low Level X = Don't Care

Recommended Operating Conditions

Parameter	DM54AS153			DM74AS153			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V	A, B			0.2	mA
			G			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	A, B			40	μA
			G			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IN} = 0.4V	A, B			−1	mA
			G			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		16	26	mA
			Outputs low		21	33	

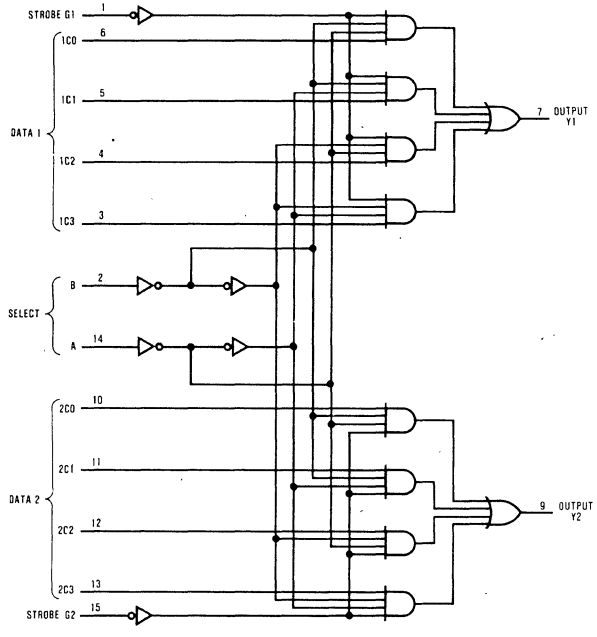
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS153			DM74AS153			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	3		14	3		12.5	ns
t_{PHL}, High to low Level Output				3		12.5	3		11	ns
t_{PLH}, Low to high Level Output	Data	Y		2		8	2		7	ns
t_{PHL}, High to low Level Output				2		8.5	2		8	ns
t_{PLH}, Low to high Level Output	Strobe	Y		3		13	3		11.5	ns
t_{PHL}, High to low Level Output				2		10	2		9	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6289-2

National Semiconductor

DM54AS/DM74AS157,158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The AS157 presents true data whereas the AS158 presents inverted data to minimize propagation delay time.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

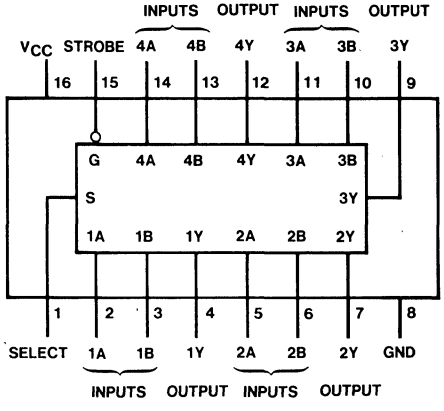
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6290-1

54AS157 (J) **74AS157 (J, N)**
54AS158 (J) **74AS158 (J, N)**

Function Table

Inputs				Output Y	
Strobe	Select	A	B	AS157	AS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54/74AS157,158			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V	Select			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Select			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Select			−1	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	54/74AS157		17.5	28	mA
			54/74AS158		15.6	22.5	mA

'AS157 Switching Characteristics over recommended operating free air temperature range (Note 1)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54AS157			DM74AS157			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	1		7.5	1		6	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Data	Y		1		6.5	1		5.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Strobe	Y		2		12.5	2		10.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Strobe	Y		2		8.5	2		7.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Y		2		12	2		11	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Select	Y		2		12	2		10	ns

'AS158 Switching Characteristics over recommended operating free air temperature range (Note 1)

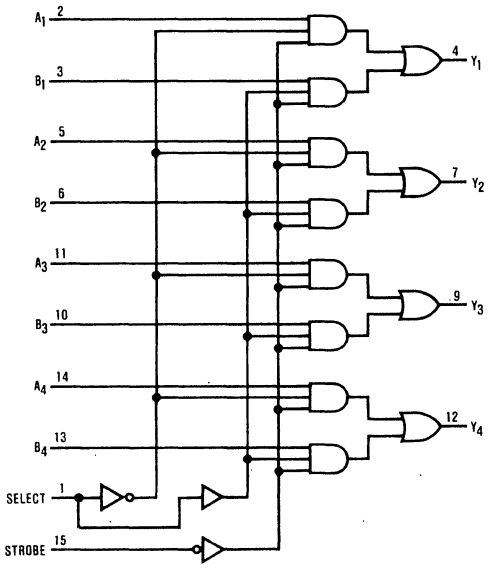
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54AS158			DM74AS158			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	1		6	1		5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Data	Y		1		5.5	1		4.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Strobe	Y		2		8	2		6.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Strobe	Y		2		11.5	2		10	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Y		2		11	2		9.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Select	Y		2		11.5	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

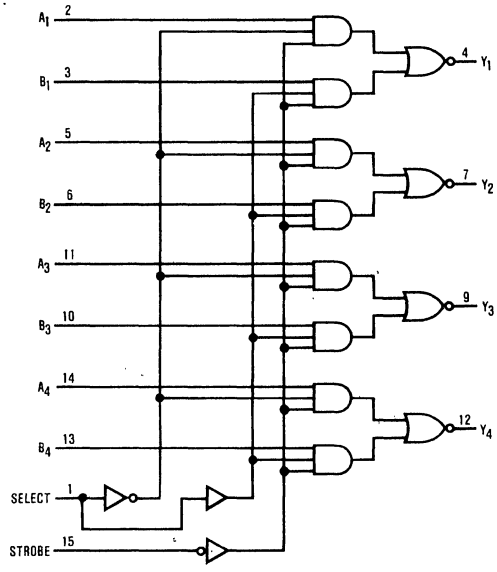
Logic Diagrams

AS157



TL/F/6290-2

AS158



TL/F/6290-3

3

National Semiconductor

DM54AS/DM74AS160,161,162,163 Synchronous Four-Bit Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The AS160 and AS162 are four-bit decade counters, while the AS161 and AS163 are four-bit binary counters. The AS160 and AS161 clear asynchronously, while the AS162 and AS163 clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. (Continued)

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Shottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously programmable.
- Internal look ahead for fast counting.
- Carry output for n-bit cascading.
- Synchronous counting.
- Load control line.
- ESD inputs.

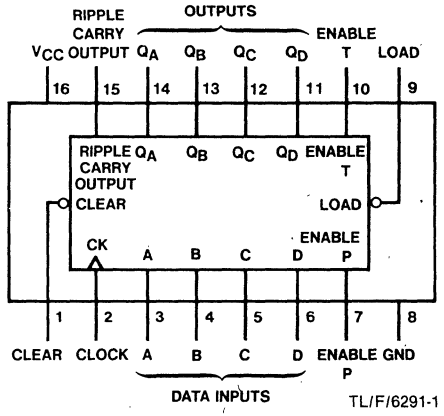
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6291-1

54AS160 (J) 74AS160 (J,N) 54AS162 (J) 74AS162 (J,N)
54AS161 (J) 74AS161 (J,N) 54AS163 (J) 74AS163 (J,N)

General Description (Continued)

The AS160 and AS161 clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The AS162 and AS163 clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the AS162 and AS163 are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) and a ripple carry output. Both count-enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the AS160 through AS163, may occur regardless of the logic level on the clock.

The AS160 through AS163 feature a fully independent clock circuit. Changes made to control-inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Recommended Operating Conditions

Parameter			DM54AS 160,161,162,163			DM74AS 160,161,162,163			Unit
			Min	Nom	Max	Min	Nom	Max	
Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}			2			2			V
Low Level Input Voltage, V_{IL}					0.8			0.8	V
High Level Output Current, I_{OH}					−2			−2	mA
Low Level Output Current, I_{OL}					20			20	mA
Clock Frequency, f_{CLOCK}			0		65	0		75	MHz
tsetup, Set-up time	Data; A, B, C, D		10			8			ns
	En P, En T		10			8			ns
	Load		10			8			ns
	Clear (Only for 162 & 163)	Low	14			12			ns
		High	10			9			
Set-up 1 (Only for 160 & 161)	Clear		10			8			ns
thold, Hold time	Data; A, B, C, D		2			0			ns
	En P, En T		2			0			ns
	Load		2			0			ns
	Clear (Only for 162 & 163)		2			0			ns
Hold 0 (Only for 160 & 161)	Clear		2			0			ns
Width of Clock Pulse, T_W			7.7			6.7			ns
Width of Clear Pulse, T_W ('AS160, 'AS161 Low)			10			8			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$I_{OH} = -2mA$ $V_{CC} = 4.5V$ to $5.5V$		$V_{CC}-2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = 20mA$			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$	Load			0.3	mA
			ENT			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$ $V_{IH} = 2.7V$	Load			60	μA
			ENT			40	
			Others			20	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$	Load			−1.5	mA
			ENT			−1	
			Others			−0.5	
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$			35	53	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

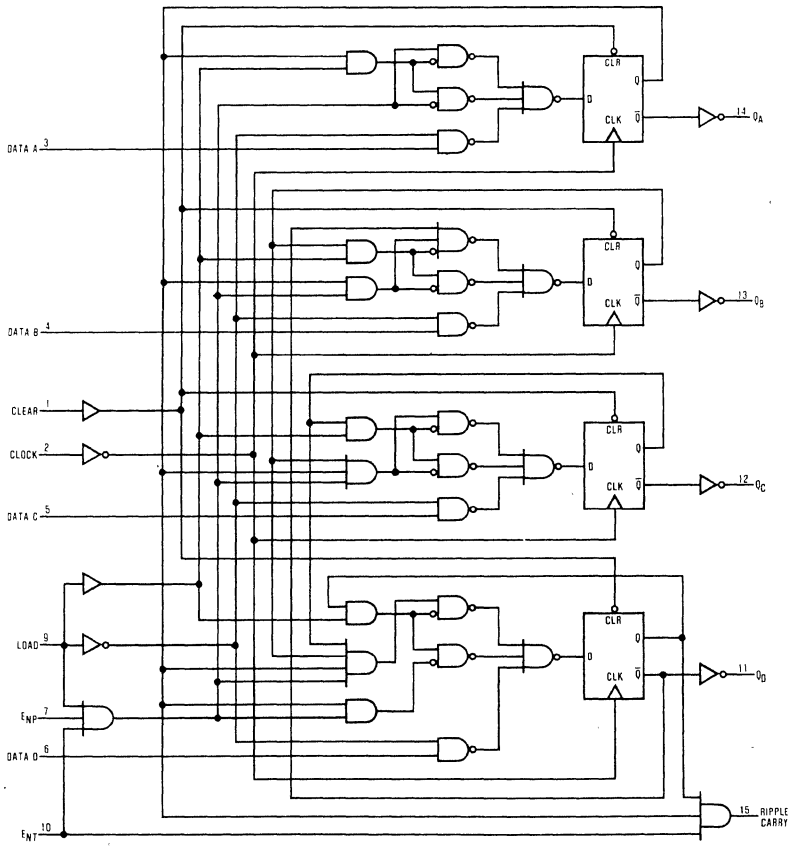
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS 160, 161, 162, 163			DM74AS 160, 161, 162, 163			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			$V_{CC} = 4.5$ to $5.5V$ $R_L = 500\ \Omega$ $C_L = 50$ pF	65			75			MHZ
T_{PHL}, Propagation delay time. High to low level output.	Clock	Ripple Carry		2		14	2		12.5	ns
T_{PLH}, Propagation delay time. Low to high level output. With Load High				2		14	2		12.5	ns
With Load Low				2		15	2		14.5	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		1		7.5	1		7	ns
T_{PHL}, Propagation delay time. High to low level output.				2		14	2		13	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	Ripple Carry		1.5		10	1.5		9	ns
T_{PHL}, Propagation delay time. Low to high level output.				1		9.5	1		8.5	ns
T_{PHL}, Propagation delay time. High to low level output.	Clear (AS160, AS161)	Any Q		2		14	2		13	ns
T_{PHL}, Propagation delay time. High to low level output.	Clear (AS160, AS161)	Ripple Carry		2		15	2		13.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

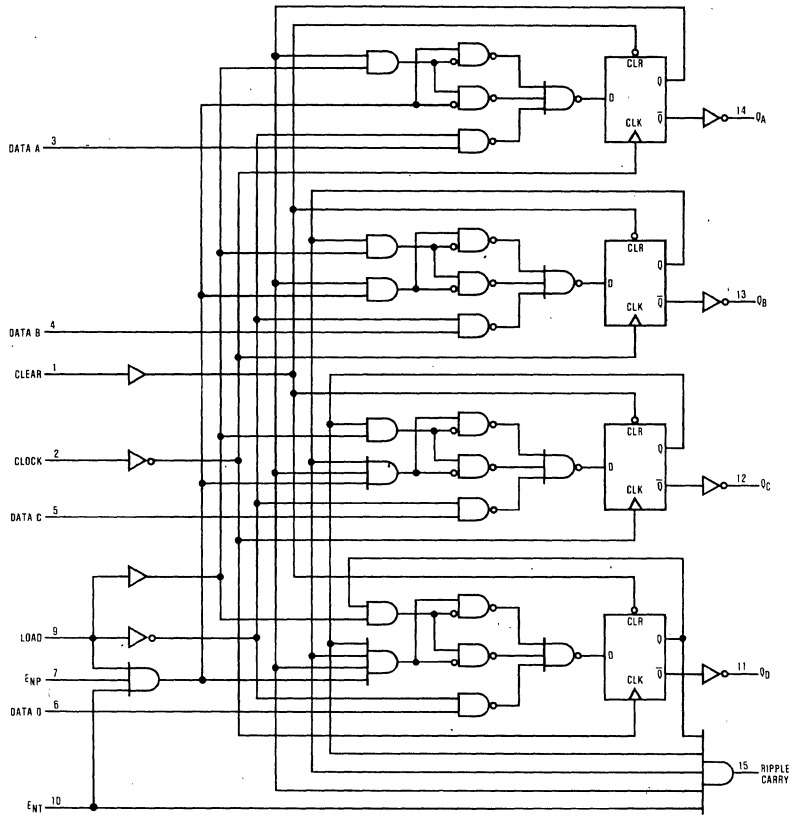
AS160



TL/F/6291-2

Logic Diagrams (Continued)

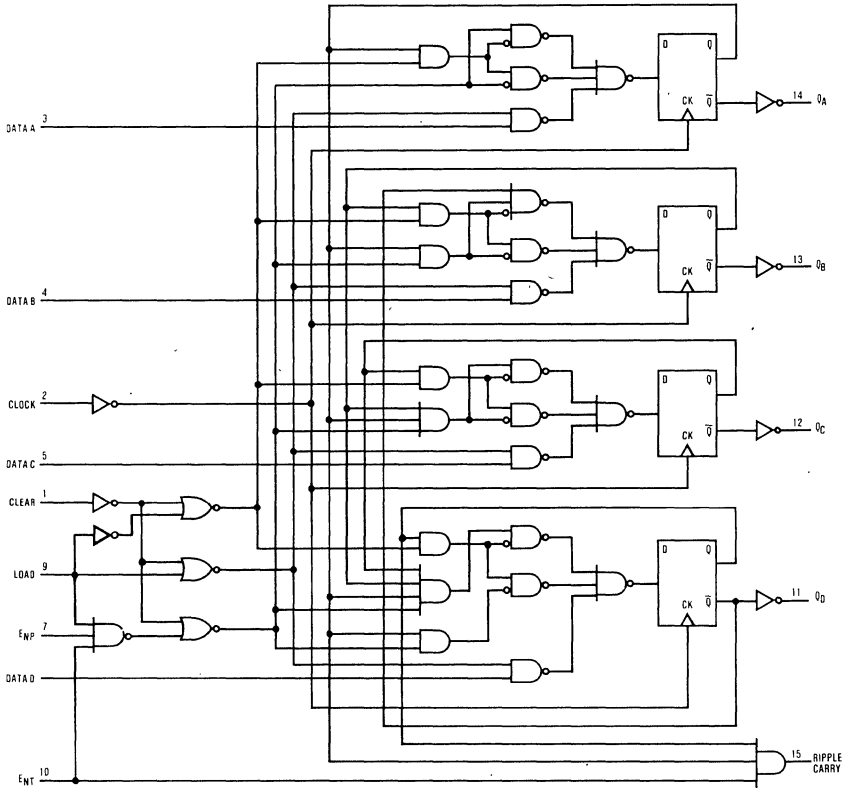
AS161



TL/F/6291-3

Logic Diagrams (Continued)

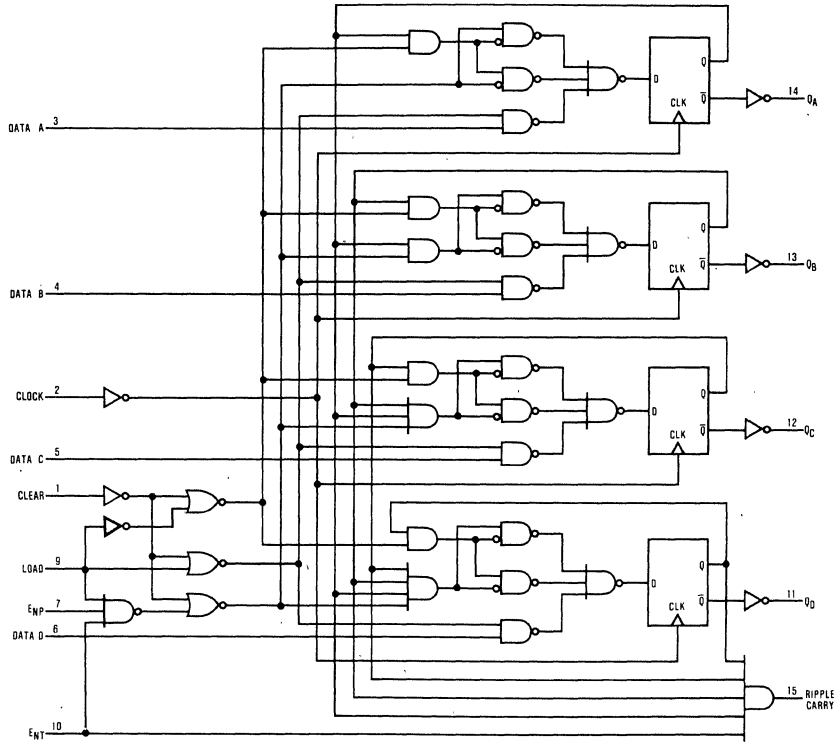
AS162



TL/F/6291-4

Logic Diagrams (Continued)

AS163



TL/F/6291-5

National Semiconductor

DM54AS/DM74AS168,169 Synchronous Four Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The AS168 is a four-bit decade up/down counter and the AS169 is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the QA output when counting up, and approximately equal to the low portion of the QA output when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

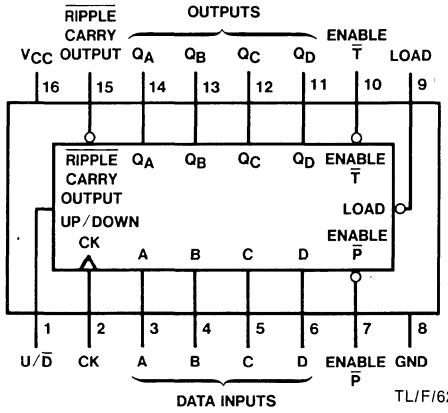
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously Programmable.
- Internal Look Ahead for Fast Counting.
- Carry Output for N-bit Cascading.
- Synchronous Counting.
- Load Control Line.
- ESD Inputs.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



TL/F/6292-1

Dual-In-Line Package

54AS168 (J)	**74AS168 (J,N)**
54AS169 (J)	**74AS169 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS168,168			DM74AS168,169			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, f_{CLOCK}		0		65	0		75	MHz
tsetup, Set-up time	Data; A, B, C, D	10			8			ns
	En $\overline{P}$, En $\overline{T}$	10			8			ns
	Load	10			8			ns
	U/$\overline{D}$	10			8			ns
thold, Hold time	Data; A, B, C, D	2			0			ns
	En $\overline{P}$, En $\overline{T}$	2			0			ns
	Load	2			0			ns
	U/$\overline{D}$	2			0			ns
Width of Clock Pulse, T_W		7.7			6.7			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V	Load, ENT, U/$\overline{D}$			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 4.5V V_{IH} = 2.7V	Load, ENT, U/$\overline{D}$			40	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V	CLK, DATA, EN$\overline{P}$			−0.5	mA
			LOAD, EN $\overline{T}$ U/$\overline{D}$			−1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			46	63	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

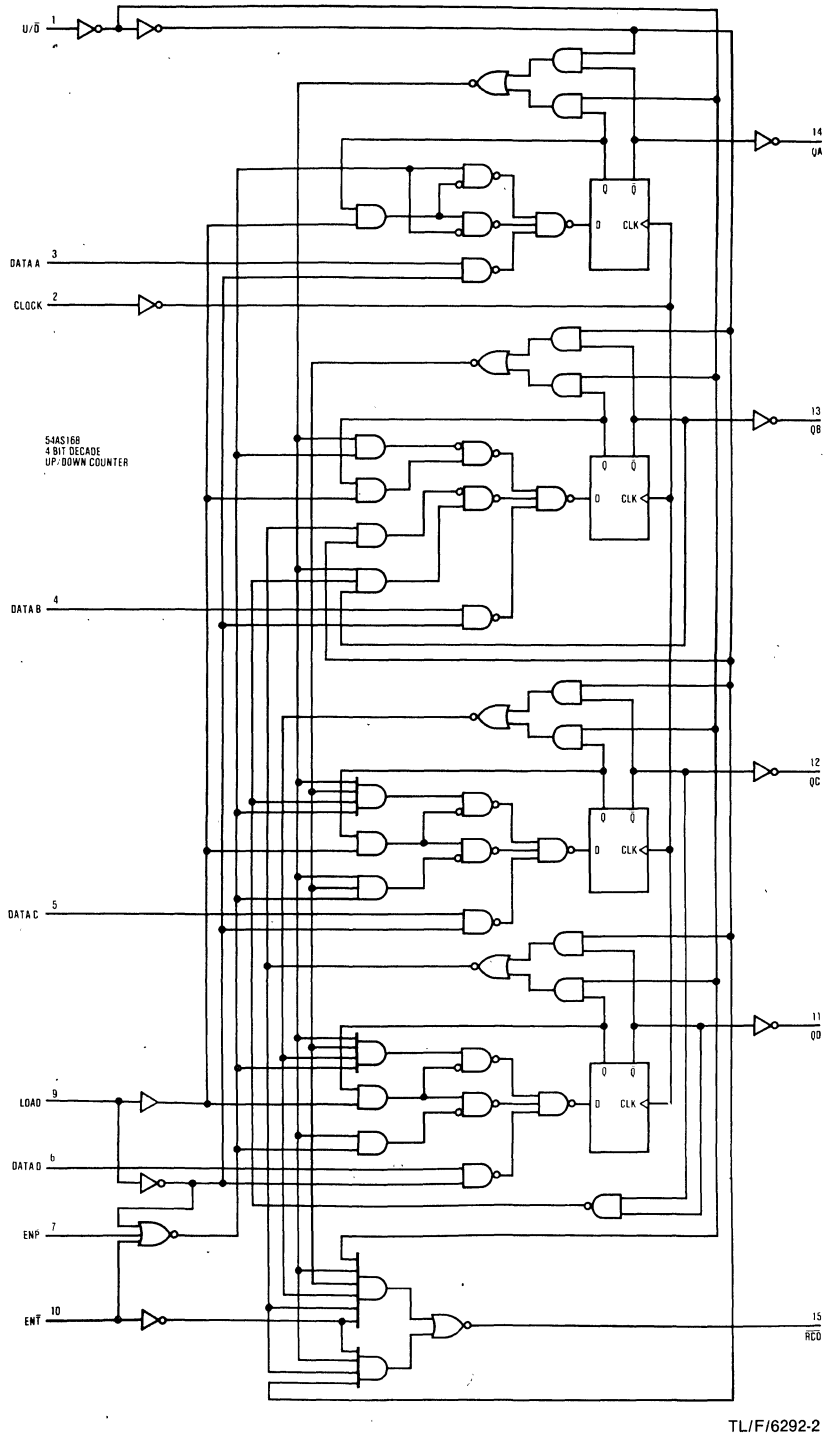
Parameter	From	To	Conditions	DM54AS168,169			DM74AS168,169			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	65			75			MHz
T_{PLH}, Propagation delay time. Low to high level output. With Load Low	Clock	$\overline{\text{Ripple}}$ Carry		3		17.5	3		16.5	ns
T_{PHL}, Propagation delay time. High to low level output.				2		14	2		13	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		1		7.5	1		7	ns
T_{PHL}, Propagation delay time. High to low level output.				2		14	2		13	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	$\overline{\text{Ripple}}$ Carry		1.5		10	1.5		9	ns
T_{PHL}, Propagation delay time. High to low level output.				1.5		10	1.5		9	ns
T_{PLH}, Propagation delay time. Low to high level output.	U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry		2		14	2		12	ns
T_{PHL}, Propagation delay time. High to low level output.				2		14.5	2		13	ns

NOTE 1: See Section 1 for test waveforms and output load.

NOTE 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for AS168 or 15 for AS169), the ripple carry output will be out of phase.

Logic Diagrams

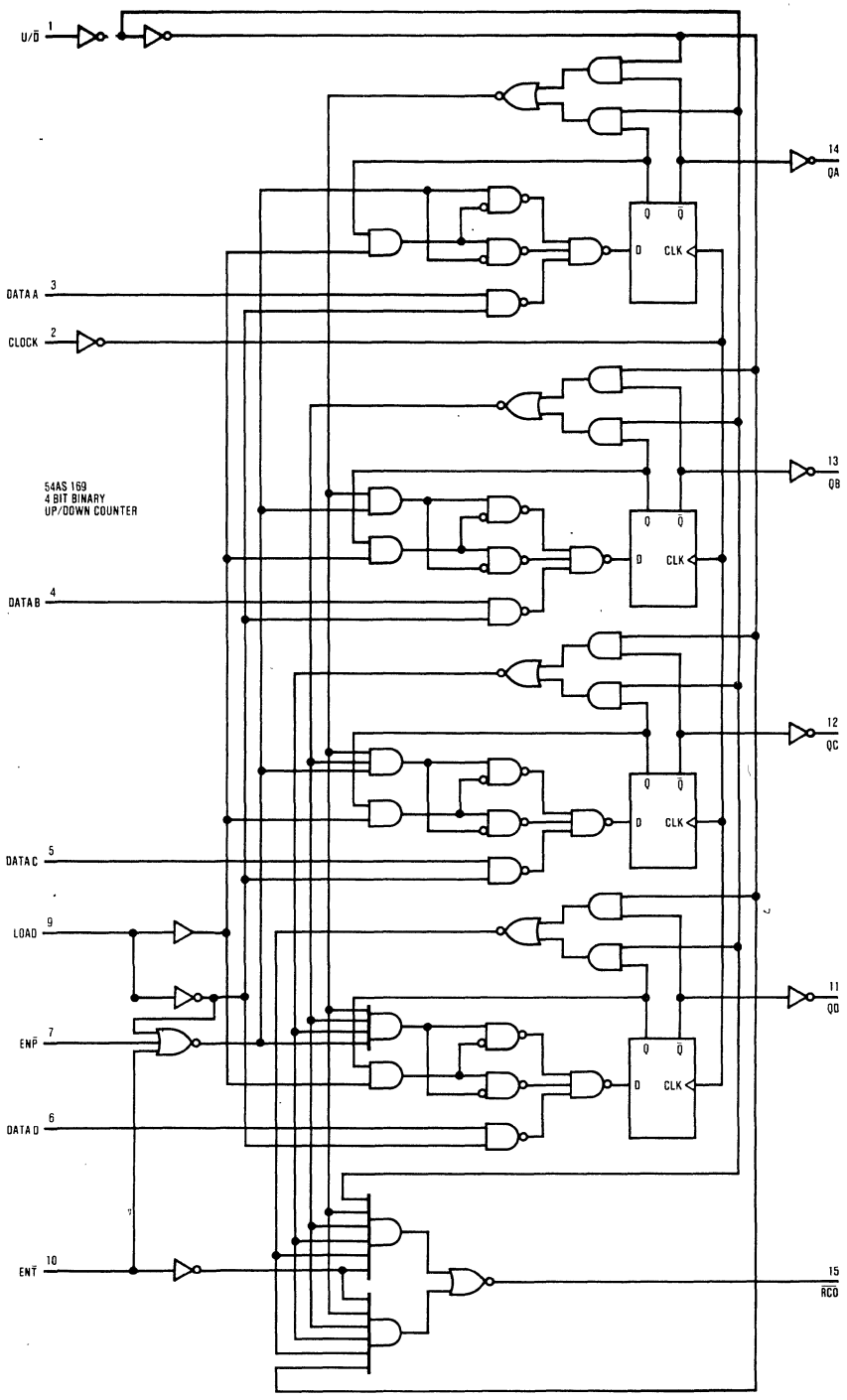
DM54AS/DM74AS168



TL/F/6292-2

Logic Diagrams (Continued)

DM54AS/DM74AS169



TL/F/6292-3

National Semiconductor

PRELIMINARY

DM54AS/DM74AS174,175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Pin and Functional compatible with LS and Schottky family counterpart.
- Switching performance guaranteed over full temperature and V_{CC} supply range.
- 54AS174 contains six flip-flops with separate D inputs and Q outputs.
- 54AS175 contains four flip-flops with separate D inputs and both Q and $\overline{Q}$ outputs.

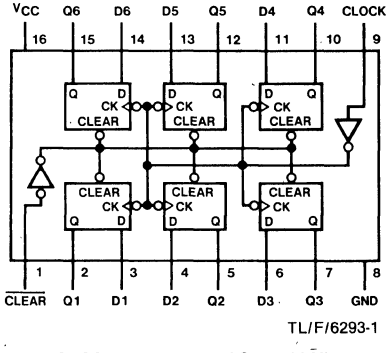
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS174/175	−55°C to 125°C
DM74AS174/175	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

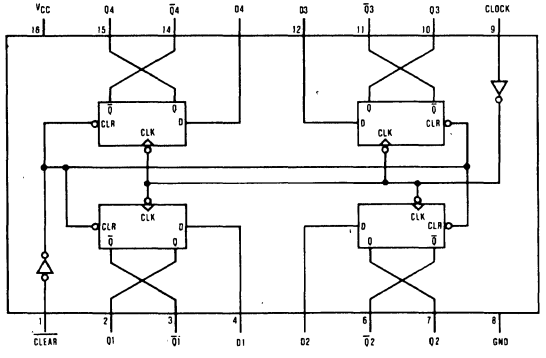
Dual-In-Line Package



TL/F/6293-1

54AS174 (J) 74AS174 (J,N)

Dual-In-Line Package



TL/F/6293-2

54AS175 (J) 74AS175 (J,N)

Function Table

Inputs			Outputs	
$\overline{Clear}$	Clock	D	Q	$\overline{Q}$*
L	X	X	L	L
H	↑	H	H	H
H	↑	L	L	L
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
* applies to 54AS175/74AS175 only

Recommended Operating Conditions

Parameter		DM54AS174,175			DM74AS174,175			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Pulse Width, t_W	Clock High	4			4			ns
	Clock Low-AS174	6			6			
	Clock Low-AS175	5			3			
	Clear	5.5			5			
Setup Time, t_{SETUP} Data Input	Data-AS174	4			4			ns
	Data-AS175	3			3			
	$\overline{\text{Clear}}$ Inactive State	6			6			
Hold Time, t_{HOLD} Data Input		1			1			ns
Clock frequency, f_{CLOCK}		0		100	0		100	MHZ

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ to 5.5V, $I_{OH} = -2mA$		$V_{CC}-2$	$V_{CC}-1.6$		V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = 20mA$			0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V = 2.25V$		−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	AS174		30	45	mA
			AS175		22.5	34	

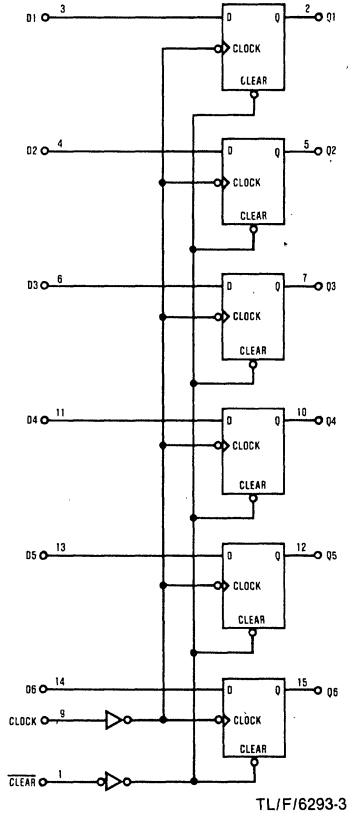
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	54AS174,175			74AS174,175			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}, Maximum Clock Frequency	$R_L = 500\,\Omega$, $C_L = 50pF$, $V_{CC} = 4.5$ to $5.5V$	100			105			MHz
t_{PLH}, Propagation Delay Time, Low to high Level Output From $\overline{Clear}$ (175 Only)		5		15	5		14	ns
t_{PHL}, Propagation Delay Time, High to low Level Output From $\overline{Clear}$		5		15	5		14	ns
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clock		3.5		9.5	3.5		8	ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clock		4.5		11.5	4.5		10	ns

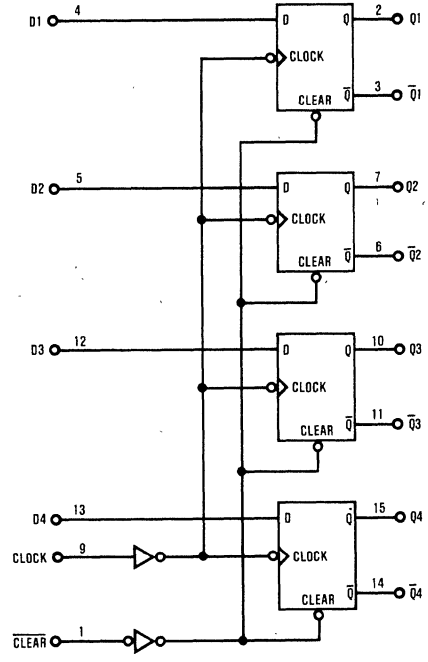
Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams



TL/F/6293-3

54AS174/74AS174



TL/F/6293-4

54AS175/74AS175

National Semiconductor

DM54AS181B/DM74AS181B Arithmetic Logic Unit/Function Generators

General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54AS182/DM74AS182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words when full carry look-ahead is employed. The method of cascading AS182 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54AS182/DM74AS182.

(Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words
- Switching specifications guaranteed over full temperature and V_{CC} range
- Switching specifications at 500Ω/50 pF
- Advanced oxide-isolated ion-implanted Schottky TTL process

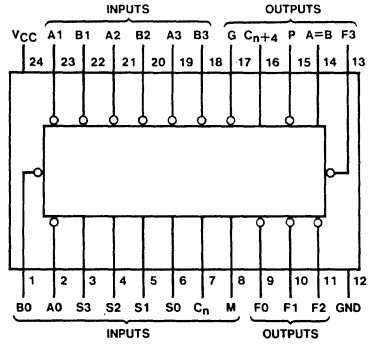
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to +125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6295-1

54AS181B (J) **74AS181B (J, N)**

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
$\overline{P}$	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Number of Bits	Typical Addition Times Using AS181B & AS882	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	5 ns	1	0	None
5 to 8	10 ns	2	0	Ripple
9 to 16	14 ns	3 or 4	1	Full Look-Ahead
17 to 64	101 ns	5 to 16	2 to 5	Full Look-Ahead

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The AS181B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables I and II and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

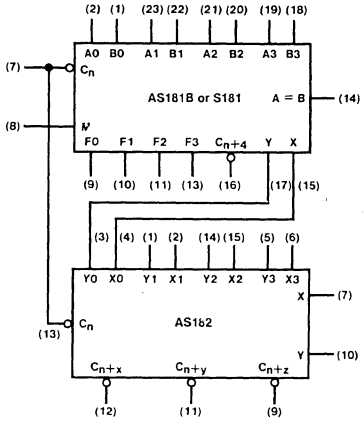
The TTL S181 and AS181B can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table II)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_{n+4}	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

General Description (Continued)



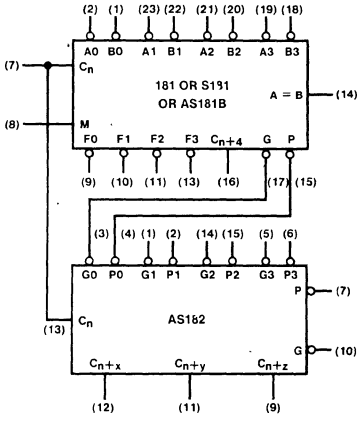
TL/F/6295-2

Figure 1

Table I

Selection				Active High Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $A\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A $\oplus$ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.



TL/F/6295-3

Figure 2

Table II

Selection				Active Low Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{AB}$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Recommended Operating Conditions

Parameter		54AS181B			74AS181B			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}	All Outputs except A = B and $\overline{G}$			−2			−2	mA
	$\overline{G}$			−3			−3	
Low Level Output Current, I_{OL}	All Outputs except $\overline{G}$			20			20	mA
	$\overline{G}$			48			48	
High Level Output Voltage, V_{OH} (A = B Only)				5.5			5.5	

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA	Any Output except A = B	V_{CC}−2			V
		I_{OH} = −3mA	$\overline{G}$	2.4	3.4		
I_{OH}	High Level Output Current (A = B)	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA	Any Output except $\overline{G}$		0.3	0.5	V
		I_{OL} = 48mA	$\overline{G}$		0.4	0.5	
I_I	Max High Input Current	V_{CC} = Max, V_{IH} = 7V	Mode			0.1	mA
			Any A or B			0.3	
			S			0.4	
			Carry			0.6	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7V	Mode Input			20	μA
			Any S Input			80	
			Any A or B Input			60	
			Carry Input			120	

Electrical Characteristics (Continued) over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Mode Input			−0.5	mA
			Any S Input			−2	
			Any A or B Input			−1.5	
			Carry Input			−2.5	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			70	104	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Sym	Parameter	From (Input)	To (Output)	Conditions (Note 2)	DM54AS181B			DM74AS181B			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+4}		2	7	11	2	7	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	11	2	7	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)	2	8	14	2	8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	14	2	8	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	2	8	20	2	8	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	20	2	8	16	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	3	6	11	3	6	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	6	11	3	6	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)	2	5	9	2	5	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	5	9	2	5	7	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	2	6	12	2	6	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	12	2	6	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)	2	6	11	2	6	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	11	2	6	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	2	6	13	2	6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	13	2	6	10	

Switching Characteristics (Continued) over recommended operating free air temperature range (Note 1).

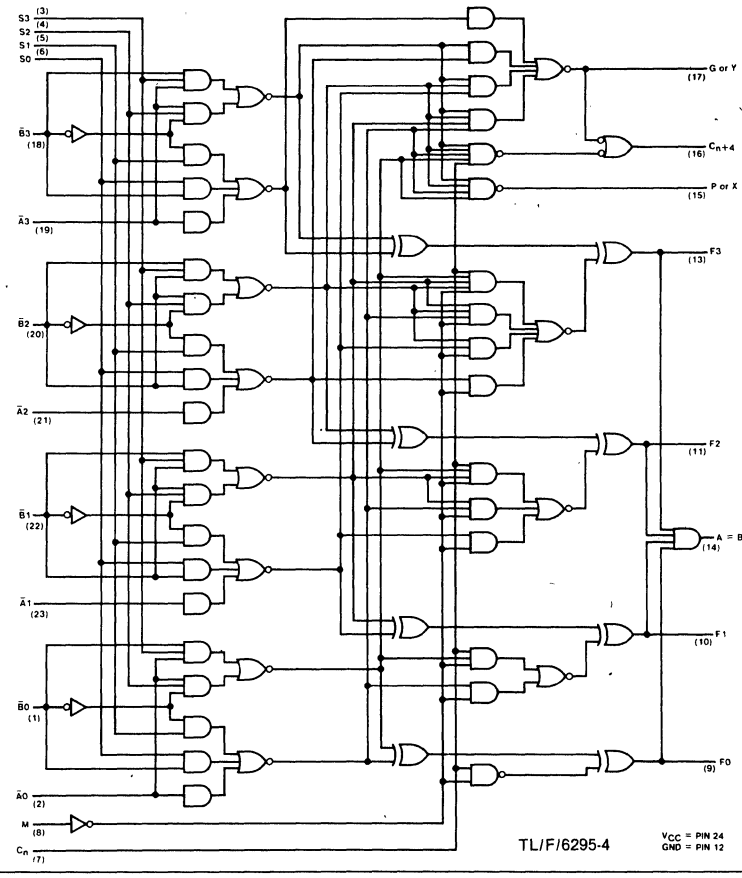
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Sym	Parameter	From (Input)	To (Output)	Conditions (Note 2)	DM54AS181B			DM74AS181B			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)	2	5	11	2	5	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	5	11	2	5	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	2	6	12	2	6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	12	2	6	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5 V (logic mode)	2	6	16	2	6	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	16	2	6	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)	4	14	26	4	14	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				4	14	26	4	16	21	

Note 1: See Section 1 for test waveforms and output load.

Note 2: $V_{CC} = 4.5V$ to 5.5V, $C_L = 50$ pF (15 pF for A = B), $R_L = 500\Omega$ (280Ω for A = B).

Logic Diagram



Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}							
t_{PLH}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All A	All B	Any F or C_{n+4}	In-Phase
t_{PHL}							
t_{PLH}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase

National Semiconductor

PRELIMINARY

DM54AS182/DM74AS182 Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the AS181B arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each AS182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the AS182 are:

$C_{n+x} = \overline{G}0 + \overline{P}0\ C_n$

$C_{n+y} = \overline{G}1 + \overline{P}1\ \overline{G}0 + \overline{P}1\ \overline{P}0\ C_n$

$C_{n+z} = \overline{G}2 + \overline{P}2\ \overline{G}1 + \overline{P}2\ \overline{P}1\ \overline{G}0 + \overline{P}2\ \overline{P}1\ \overline{P}0\ C_n$

$\overline{G} = \overline{G}3\ (\overline{P}3 + \overline{G}2)\ (\overline{P}3 + \overline{P}2 + \overline{G}1)\ (\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$

$\overline{P} = \overline{P}3\ \overline{P}2\ \overline{P}1\ \overline{P}0$

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Offers carry functions in a compatible form for direct connection to the ALU
- Cascadable to perform look-ahead across n-bit adders
- PNP inputs reduce input loading
- Improved AC performance over Schottky at reduced power consumption

Absolute Maximum Ratings (Note 1)

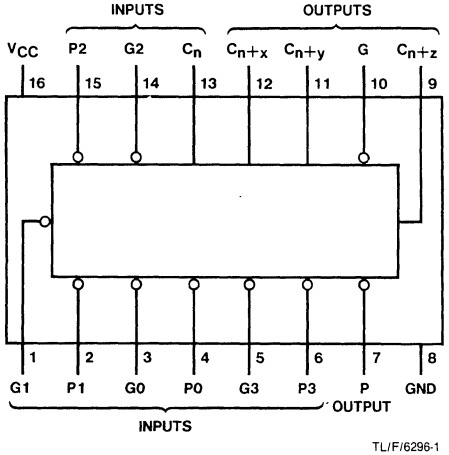
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6296-1

54AS182 (J) **74AS182 (J, N)**

Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

Recommended Operating Conditions

Symbol	Parameter	DM54AS182			DM74AS182			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage		$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.2	V
V_{OH}	High Level Output Voltage		$I_{OH} = -2$mA		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage		$V_{CC} = 4.5V$, $I_{OL} = 20$ mA			0.35	0.5	V
I_I	Max High Input Current	P3	$V_{CC} = 5.5V$, $V_{IH} = 7V$				200	μA
		C_n, P2					300	
		P0, P1, G3					400	
		G0, G2					700	
		G1					800	
I_{IH}	High Level Input Current	C_n Input	$V_{CC} = Max$, $V_I = 2.7V$				60	μA
		P3 Input					40	
		P2 Input					60	
		P0, P1, or G3 Input					80	
		G0 or G2 Input					140	
		G1 Input					160	
I_{IL}	Low Level Input Current	C_n Input	$V_{CC} = Max$, $V_I = 0.5V$				−1.5	mA
		P3 Input					−1	
		P2 Input					−1.5	
		P0, P1, or G3 Input					−2	
		G0 or G2 Input					−3.5	
		G1 Input					−4	
I_O	Output Drive Current		$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{CC}	Supply Current		$V_{CC} = 5.5V$	Outputs High (1)		16	25	mA
				Outputs Low (2)		21	33	

Note 1: I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

Note 2: I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54AS182			DM74AS182			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$		5			5		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low to High Level Output	G0, G1, G2, G3, P1, P2, or P3	G			6			6		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low to High Level Output	P0, P1, P2, or P3	P			5			5		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low to High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			5			5		ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					5			5		

Note 1: See Section 1 for test waveforms and output load.

Function Tables

Inputs							Output
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All Other Combinations							H

Inputs				Output
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All Other Combinations				H

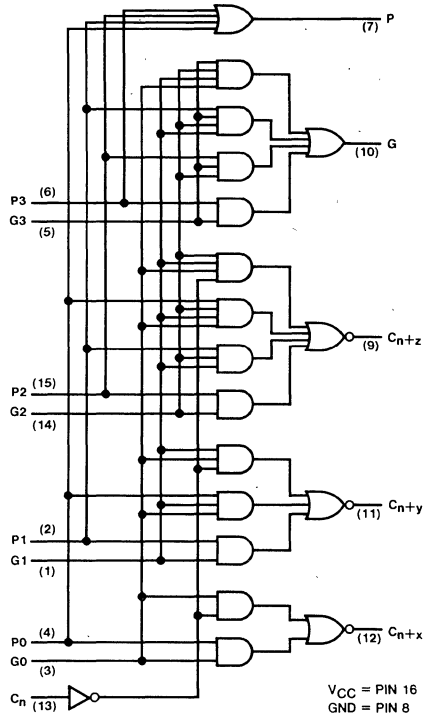
Inputs			Output
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All Other Combinations			L

Inputs							Output
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All Other Combinations							L

Inputs					Output
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All Other Combinations					L

H = High level, L = Low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output

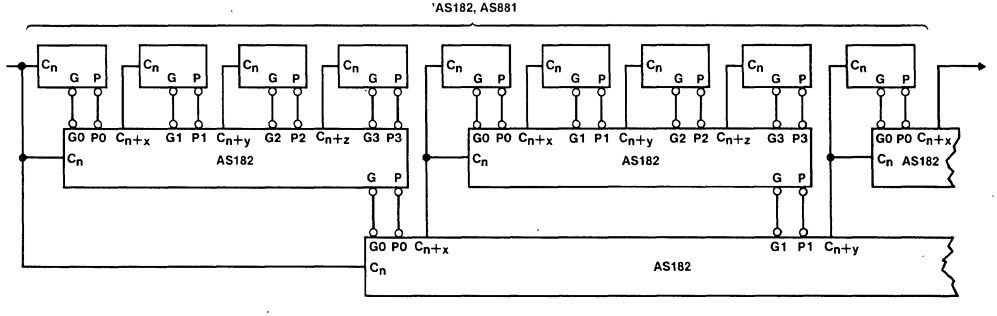
Logic Diagram



TL/F/6296-2

Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs and F outputs of AS181B are not shown.

TL/F/6296-3

National Semiconductor

PRELIMINARY

DM54AS194/DM74AS194 4-Bit Bidirectional Universal Shift Register

General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. They feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift-right (in the direction Q_A toward Q_D)
Shift-left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low.

Features

- Parallel-to-serial, serial-to-parallel conversions
- Temporary data latching capability
- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right-shift
  - Left-shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

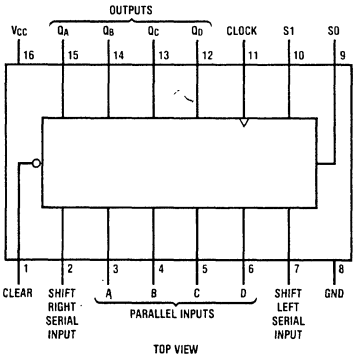
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram



TL/F/6721-1

Dual-In-Line Package

DM54AS194 (J)
DM74AS194 (J, N)

Function Table

Inputs									Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady-state),
L = low level (steady-state),
X = don't care (any input, including transitions).

↑ = transition from low-to-high level.

a, b, c, d = the level of steady-state input at input A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Recommended Operating Conditions

Symbol	Parameter			DM54AS194			DM74AS194			Units
				Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.8	V
I_{OH}	High Level Output Current					−2			−2	mA
I_{OL}	Low Level Output Current					20			20	mA
f_{CLOCK}	Clock Frequency			0	110		0	110		MHz
t_W	Pulse Width	Clear Low		4			4			ns
		CLK	High	2			2			
			Low	6			6			
t_{SU}	Set-Up Time	Select		6.5			6.5			ns
		Data		2.5			2.5			
t_{REC}	Clear Recovery Time			4			4			
t_H	Hold Time			0			0			ns
T_A	Operating Free-Air Temperature			−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

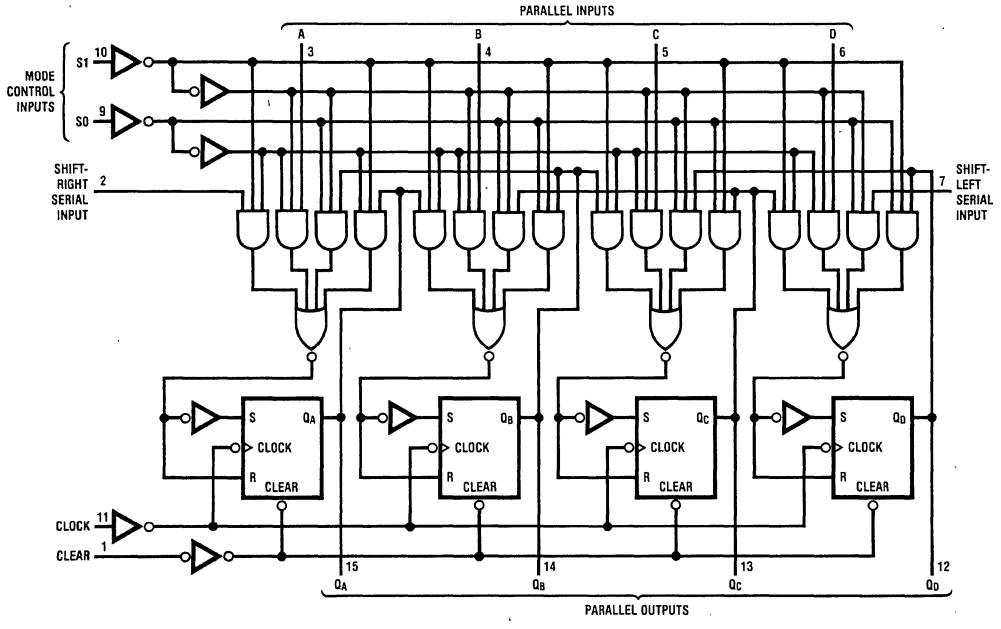
Parameter	Conditions		DM54AS194			DM74AS194			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5V, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min			0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5V, V_I = 7V	Data, Clear, CLK			100			100	μA
		Mode, SL, SR			200			200	
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V	Data, Clear, CLK			20			20	μA
		Mode, SL, SR			40			40	
I_{IL}	V_{CC} = 5.5V, V_I = 0.4V	Data, Clear, CLK			−0.5			−0.5	mA
		Mode, SL, SR			−1			−1	
I_O	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5V	Outputs High		28	44		28	44	mA
		Outputs Low		35	56		35	56	

Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS194			DM74AS194			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
f_{MAX}			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = R2 = 500Ω		110			110		MHz
t_{PLH}	Clock	Any Q		2		9	2		8	ns
t_{PHL}	Clock	Any Q		2		9	2		8	ns
t_{PHL}	Clear	Any Q		3		12.5	3		11.5	ns

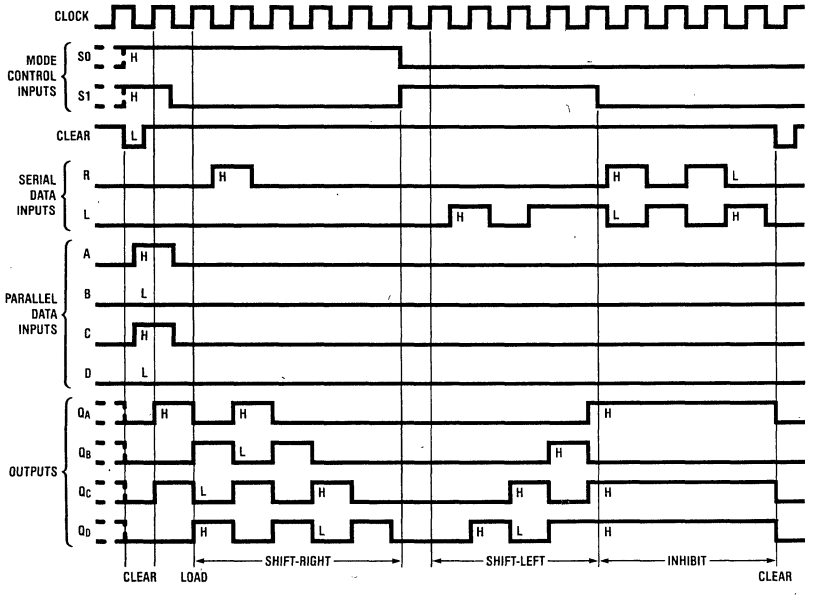
Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Logic Diagram



TL/F/6721-2

Timing Diagram



TL/F/6721-3

National Semiconductor

PRELIMINARY

DM54AS195/DM74AS195
4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

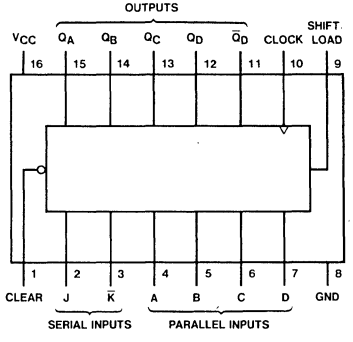
The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  - accumulators/processors
  - serial-to-parallel, parallel-to-serial converters
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterpart

Connection Diagram

Dual-In-Line Package



TL/F/6476-1

54AS195 (J) **74AS195 (N)**

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial J	Serial $\overline{K}$	Parallel A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

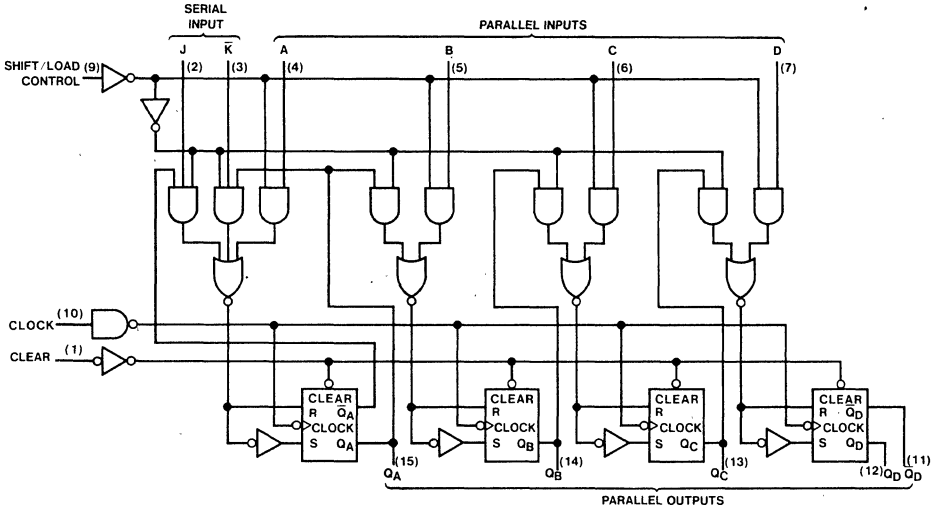
↑ = Transition from low to high level

a,b,c,d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

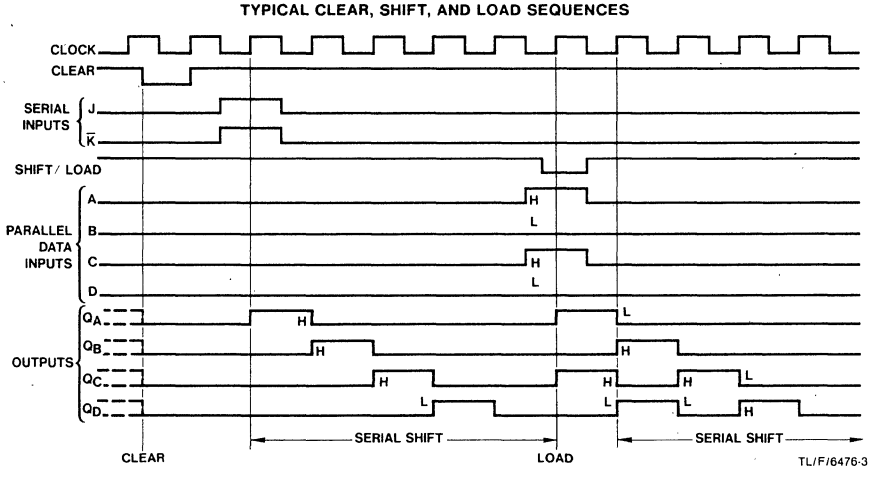
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

Logic Diagram



TL/F/6476-2

Timing Diagram



TL/F/6476-3

National Semiconductor

DM54AS/DM74AS230,231 TRI-STATE® Bus Drivers/Receivers

General Description

This family of Advanced Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The AS230 is organized as 4 bit buffers inverting & 4 bit buffers non inverting. The AS231 is organized as two 4 bit wide inverting buffers with separate complementary output control buffers.

The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (V_{CC}) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or down.

Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance over Low Power Schottky Counterpart.
- Functional and Pin Compatible with Low Power Schottky Counterpart.
- Switching Response Specified into 500 ohm and 50pF.
- Low Level Drive Current 74AS = 48mA, 54AS = 40mA
- Glitch Free Bus During Power Up/Down
- Specified to Interface with CMOS at $V_{OH} = V_{CC} - 2V$.

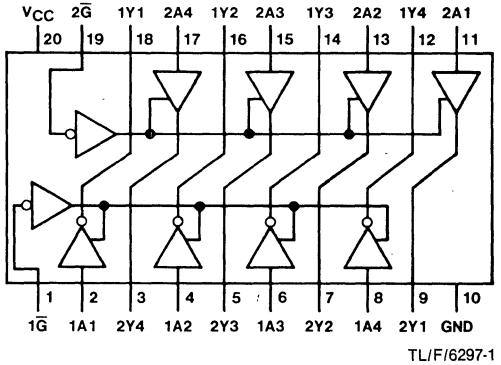
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

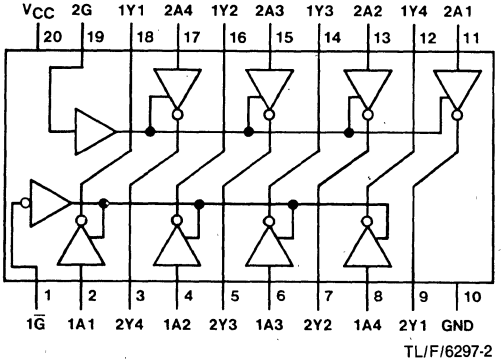
Dual-In-Line Package



TL/F/6297-1

54AS230 (J) 74AS230 (J,N)

Dual-In-Line Package



TL/F/6297-2

54AS231 (J) 74AS231 (J,N)

Function Table

G (AS231)	$\overline{G}$	A	AS231 Y (Invert)	AS230 Y (Non-Invert)
H	L	L	H	L
H	L	H	L	H
L	H	X	Z (Isolation)	

H = high logic level
L = low logic level
X = either low or high logic level
Z = high impedance (off)

Recommended Operating Conditions

Parameter	DM54AS 230,231			DM74AS 230,231			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			−48			−64	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V		2.4			V
		I_{OH} = −2.0mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	Others			−0.5	mA
			AS230 2A Inputs			−1	
I_{OZH}	High Level TRI-STATE® Output Current	V_{CC} = 5.5V, V = 2.7V				50	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−50		−150	mA
I_{CC}	54/74AS230 Supply Current	V_{CC} = 5.5V	Outputs High		16	25	mA
			Outputs Low		55	87	
			TRI-STATE		29	46	
I_{CC}	54/74AS231 Supply Current	V_{CC} = 5.5V	Outputs High		12	18	mA
			Outputs Low		52	82	
			TRI-STATE		25	39	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	To (Output)	Conditions	DM54AS230			DM74AS230			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	1A	1Y	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	2.5		7	2.5		6.5	ns
t_{PHL}				2		6	2		5.7	
t_{PLH}	2A	2Y		2.5		9	2.5		6.2	ns
t_{PHL}				2		7	2		6.2	
t_{PZH}	$1\overline{G}$	1Y		2		7	2		6.4	ns
t_{PZL}				2		9	2		8.5	
t_{PHZ}				2		5.5	2		5	
t_{PLZ}				2		12.5	2		9.5	
t_{PZH}	$2\overline{G}$	2Y		2		10	2		9	ns
t_{PZL}				2		8	2		7.5	
t_{PHZ}				2		6.5	2		6	
t_{PLZ}				2		10.5	2		9	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	To (Output)	Conditions	DM54AS231			DM74AS231			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	2		7	2		6.5	ns
t_{PHL}				2		6	2		5.7	
t_{PZH}	$\overline{G}$	Y		2		7	2		6.4	ns
t_{PZL}				2		9	2		8.5	
t_{PHZ}				2		5.5	2		5	
t_{PLZ}				2		12.5	2		9.5	
t_{PZH}	G	Y		3		7	3		6	ns
t_{PZL}				3		10	3		9	
t_{PHZ}				3		6.5	3		6	
t_{PLZ}				3		13.5	3		7	

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS/DM74AS240,241,242,243,244 TRI-STATE® Bus Drivers/Receivers

General Description

This family of Advance Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The AS240, 241 and 244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The AS242 and 243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control.

Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance with Less Power Dissipation compared with Schottky Counterpart.
- Functional and Pin Compatible with 54/74LS and Schottky Counterpart.
- Switching Response Specified Into 500 ohm and 50pF.
- Glitch Free Bus During Power Up/Down.
- Specified to Interface with CMOS at $V_{OH} = V_{CC} - 2V$.

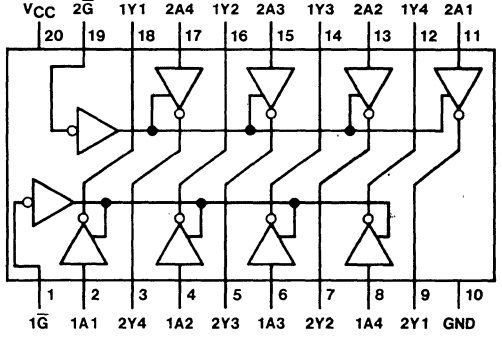
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

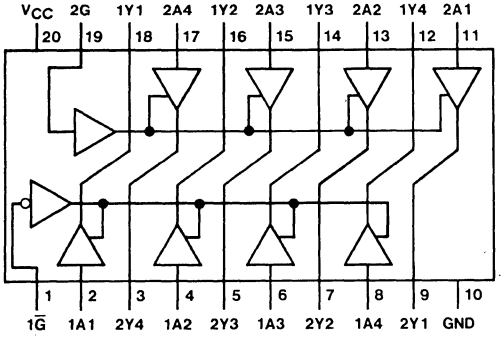
Dual-In-Line Package



TL/F/6298-1

54AS240 (J) 74AS240 (J,N)

Dual-In-Line Package

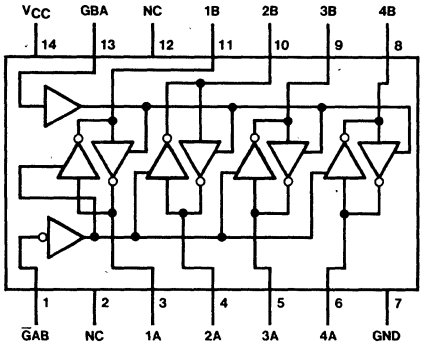


TL/F/6298-2

54AS241 (J) 74AS241 (J,N)

Connection Diagrams (Continued)

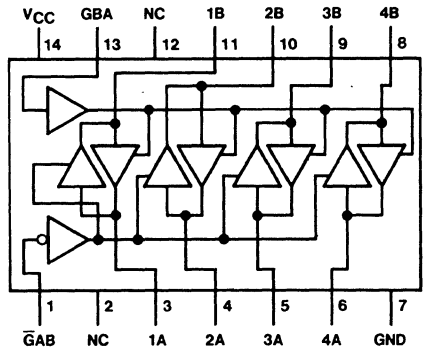
Dual-In-Line Package



TL/F/6298-3

54AS242 (J) 74AS242 (J,N)

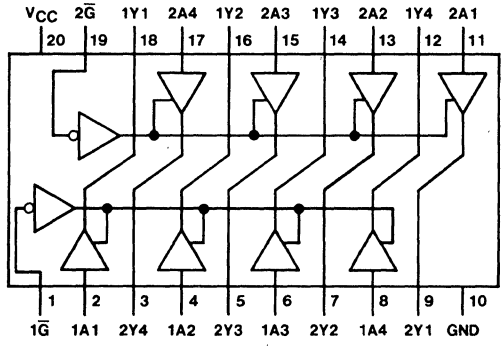
Dual-In-Line Package



TL/F/6298-4

54AS243 (J) 74AS243 (J,N)

Dual-In-Line Package



TL/F/6298-5

54AS244 (J) 74AS244 (J,N)

Function Tables

LS240

$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

LS241

2G	$1\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = Logic Low Level
H = Logic High Level
X = Either Logic Low or Logic High Level
Z = High Impedance

LS244

$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

LS242, LS243

INPUTS		'AS242	'AS243
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

Recommended Operating Conditions

Parameter	DM54AS 240,241,242,243,244			DM74AS 240,241,242,243,244			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			48			64	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18mA$					−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = -3mA$			2.4	3.2		V
		$V_{CC} = 4.5V$, $I_{OH} = Max$			2.4			
		$I_{OH} = -2mA$			$V_{CC}-2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = Max$				0.35	0.55	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$	$V_{IN} = 7V$	Others			100	μA
			$V_{IN} = 5.5V$	For AS242, 243 (A or B)				
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$		AS242, 243 (A or B)			70	μA
				Others			20	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$		AS240, 241 (G, $\overline{G}$), 242, 243 (Control Inputs), 244 ($\overline{G}$)			−500	μA
				AS241 (A), 243 (A or B), 244 (A)			−1000	
I_{OZH}	High Level TRI-STATE® Output Current	$V_{CC} = 5.5V$, $V_O = 2.7V$					50	μA
I_{OZL}	Low Level TRI-STATE Output Current	$V_{CC} = 5.5V$, $V = 0.4V$		AS242			−500	μA
				AS240, 241, 244			−50	
				AS243			−1000	
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$			−50	−115	−150	mA
I_{CC}	54/74AS240 Supply Current	$V_{CC} = 5.5V$	Outputs High			11	17	mA
			Outputs Low			51	75	
			TRI-STATE			24	38	
I_{CC}	54/74AS241 Supply Current	$V_{CC} = 5.5V$	Outputs High			22	35	mA
			Outputs Low			61	90	
			TRI-STATE			35	56	
I_{CC}	54/74AS242 Supply Current	$V_{CC} = 5.5V$	A Port Outputs High			18	28	mA
			A Port Outputs Low			38	60	
			TRI-STATE			25	39	

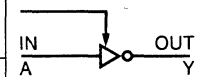
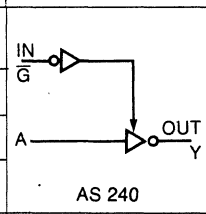
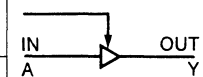
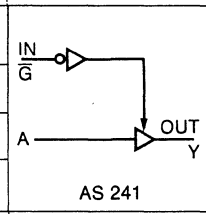
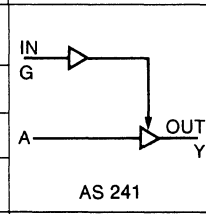
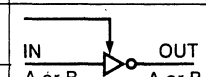
Electrical Characteristics (Continued) over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	54/74AS243 Supply Current	V_{CC} = 5.5V	A Port Outputs High		28	44	mA
			A Port Outputs Low		47	74	
			TRI-STATE		35	56	
I_{CC}	54/74AS244 Supply Current	V_{CC} = 5.5V	Outputs High		22	34	mA
			Outputs Low		60	90	
			TRI-STATE		34	54	

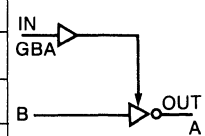
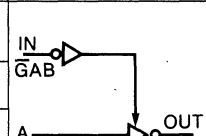
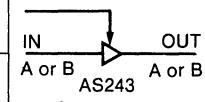
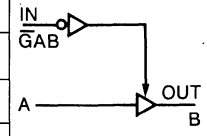
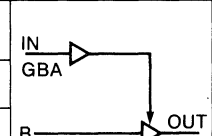
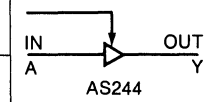
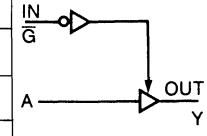
Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter (Propagation Delay Time)	Circuit Configuration	74AS			54AS			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Low-to-High Level Output	 AS 240	2		7	2		6.5	ns
T_{PHL}, High-to-Low Level Output		2		6	2		5.7	ns
T_{PZL}, Output Enable to Low Level	 AS 240	2		9.5	2		9	ns
T_{PZH}, Output Enable to High Level		2		7	2		6.4	ns
T_{PLZ}, Output Disable From Low Level		2		12.5	2		9.5	ns
T_{PHZ}, Output Disable From High Level		2		5.5	2		5	ns
T_{PLH}, Low-to-High Level Output	 AS 241	2		9	2		6.2	ns
T_{PHL}, High-to-Low Level Output		2		7	2		6.2	ns
T_{PZL}, Output Enable to Low Level	 AS 241	2		8	2		7.5	ns
T_{PZH}, Output Enable to High Level		2		10	2		9	ns
T_{PLZ}, Output Disable From Low Level		2		10.5	2		9	ns
T_{PHZ}, Output Disable From High Level		2		6.5	2		6	ns
T_{PZL}, Output Enable to Low Level	 AS 241	3		9.5	3		8.5	ns
T_{PZH}, Output Enable to High Level		3		11	3		10.5	ns
T_{PLZ}, Output Disable From Low Level		3		12	3		12	ns
T_{PHZ}, Output Disable From High Level		3		7	3		7	ns
T_{PLH}, Low-to-High Level Output	 AS 242	2		7	2		6.5	ns
T_{PHL}, High-to-Low Level Output		2		6	2		5.7	ns

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter (Propagation Delay Time)	Circuit Configuration	54AS			74AS			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PZL}, Output Enable to Low Level	 AS 242	3		9	3		8	ns
T_{PZH}, Output Enable to High Level		3		7	3		6	ns
T_{PLZ}, Output Disable From Low Level		3		13.5	3		10.5	ns
T_{PHZ}, Output Disable From High Level		3		8.5	3		6	ns
T_{PZL}, Output Enable to Low Level	 AS242	2		8.5	2		7.5	ns
T_{PZH}, Output Enable to High Level		2		9	2		5.5	ns
T_{PLZ}, Output Disable From Low Level		2		12.5	2		9.5	ns
T_{PHZ}, Output Disable From High Level		2		7	2		6.5	ns
T_{PLH}, Low-to-High Level Output	 AS243	3		9	3		7.5	ns
T_{PHL}, High-to-Low Level Output		3		8	3		6.5	ns
T_{PZL}, Output Enable to Low Level	 AS243	2		9	2		7.5	ns
T_{PZH}, Output Enable to High Level		2		10	2		9	ns
T_{PLZ}, Output Disable From Low Level		2		11	2		9	ns
T_{PHZ}, Output Disable From High Level		2		7	2		6.5	ns
T_{PZL}, Output Enable to Low Level	 AS243	3		9.5	3		8.5	ns
T_{PZH}, Output Enable to High Level		3		11	3		10.5	ns
T_{PLZ}, Output Disable From Low Level		3		14	3		11	ns
T_{PHZ}, Output Disable From High Level		3		7.5	3		7	ns
T_{PLH}, Low-to-High Level Output	 AS244	2		9	2		6.2	ns
T_{PHL}, High-to-Low Level Output		2		7	2		6.2	ns
T_{PZL}, Output Enable to Low Level	 AS244	2		8	2		7.5	ns
T_{PZH}, Output Enable to High Level		2		10	2		9	ns
T_{PLZ}, Output Disable From Low Level		2		10.5	2		9	ns
T_{PHZ}, Output Disable From High Level		2		6.5	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

National Semiconductor

PRELIMINARY

DM74AS245A Octal TRI-STATE® Bus Transceivers

General Description

This advanced Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data transmits either from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode so that the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Non-inverting logic output
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- PNP inputs reduce input loading
- Switching specifications guaranteed over full temperature and V_{CC} range

Absolute Maximum Ratings

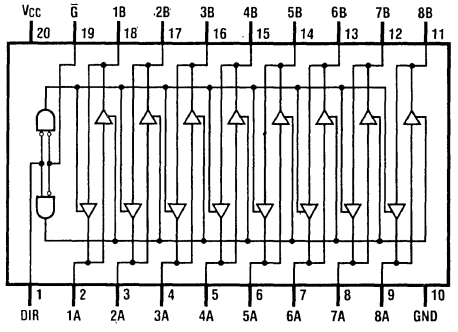
Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6299-1

DM74AS245A (J, N)

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

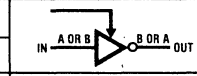
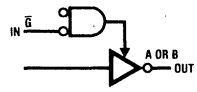
Recommended Operating Conditions

Symbol	Parameter	DM74AS245A			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC}=4.5V$, $I_{IN}=-18$ mA				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC}=4.5V$, $I_{OH}=-3$ mA		2.4	3.2		V
		$V_{CC}=4.5V$, $I_{OH}=-15$ mA		2.0	2.3		
		$I_{OH}=-2$ mA, $V_{CC}=4.5V$ to 5.5V		$V_{CC}-2$			
V_{OL}	Low Level Output Voltage	$V_{CC}=4.5V$, $I_{OL}=$ Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC}=5.5V$, $V_{IN}=7V$ ($V_{IN}=5.5V$ for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	$V_{CC}=5.5V$, $V_{IN}=2.7V$	Control Inputs			20	μA
			A or B Ports			50	
I_{IL}	Low Level Input Current	$V_{CC}=5.5V$, $V_{IN}=0.4V$	Control Inputs			−0.1	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	$V_{CC}=5.5V$, $V_{OUT}=2.25V$		−30		−112	mA
I_{CC}	Supply Current	$V_{CC}=5.5V$	Outputs High		62		mA
			Outputs Low		75		
			TRI-STATE		79		

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

Parameter (Propagation Delay Time)	Circuit Configuration	DM74AS245A			Units
		Min	Typ	Max	
t_{PLH}, High-to-Low Level Output			6		ns
t_{PHL}, High-to-Low Level Output			5		ns
t_{PZL}, Output Enable to Low Level			8		ns
t_{PZH}, Output Enable to High Level			8		ns
t_{PLZ}, Output Disable from Low Level			5		ns
t_{PHZ}, Output Disable from High Level			4.5		ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC}=4.5V$ to 5.5V, $R_L=500\Omega$, $C_L=50$ pF.

National Semiconductor

PRELIMINARY

DM54AS251/DM74AS251 TRI-STATE® 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. An Output Control input is provided which, when at the high level, places both outputs in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

Absolute Maximum Ratings (Note 1)

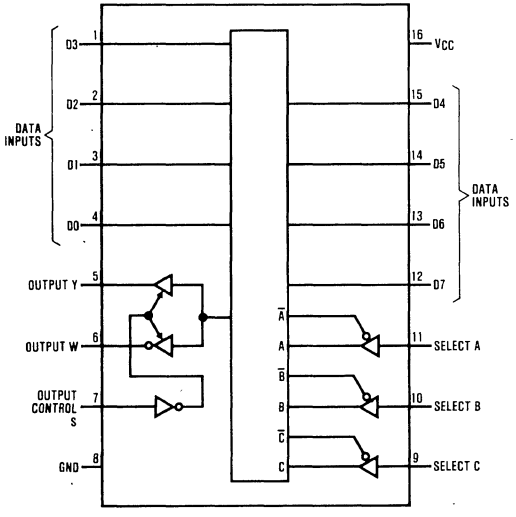
Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS251	−55°C to 125°C
DM74AS251	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6300-1

54AS251 (J) **74AS251 (J,N)**

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level, X = Don't Care
Z = High Impedance (Off)
D0 thru D7 = The Level of the Respective D Input

Recommended Operating Conditions

Parameter	DM54AS251			DM74AS251			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V	A, B, C			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	A, B, C			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IN} = 0.4V	A, B, C		−0.6	−1	mA
			All others		−0.3	−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Data Inputs = 3.0V Select Inputs = 3.0V Control Inputs = 3.0V			28	48	mA

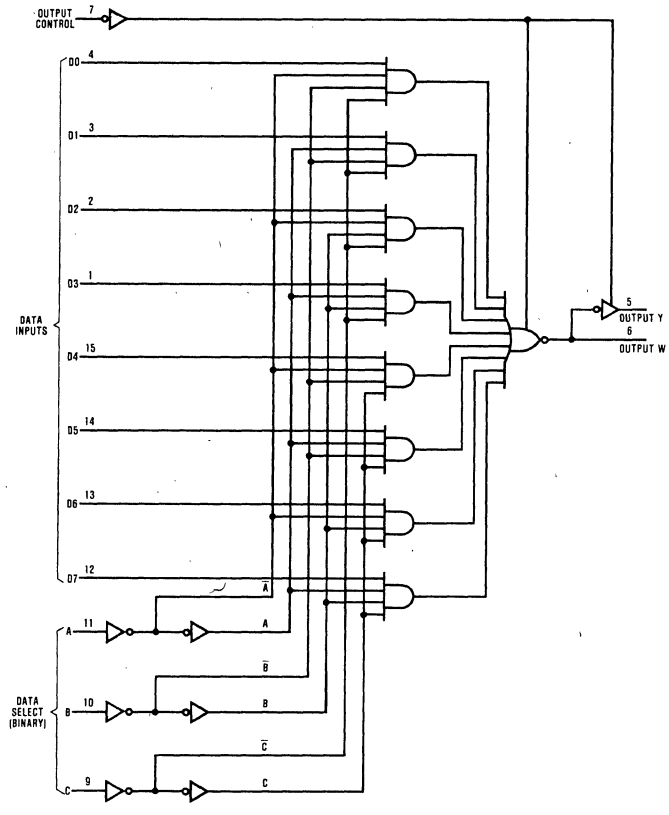
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS251			DM74AS251			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω		5			5		ns
t_{PHL}, High to low Level Output					5			5		ns
t_{PLH}, Low to high Level Output		W			4.5			4.5		ns
t_{PHL}, High to low Level Output					4.5			4.5		ns
t_{PLH}, Low to high Level Output	Data	Y			3			3		ns
t_{PHL}, High to low Level Output					4			4		ns
t_{PLH}, Low to high Level Output		W			3			3		ns
t_{PHL}, High to low Level Output					2.5			2.5		ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y			5			5		ns
t_{ZL}, Output Enable Time to Low Level					6			6		ns
t_{ZH}, Output Enable Time to High Level		W			5			5		ns
t_{ZL}, Output Enable Time to Low Level					6			6		ns
t_{HZ}, Output Disable Time From High Level		Y			3			3		ns
t_{LZ}, Output Disable Time From Low Level					4			4		ns
t_{HZ}, Output Disable Time From High Level		W			3			3		ns
t_{LZ}, Output Disable Time From Low Level					4			4		ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6300-2

National Semiconductor

PRELIMINARY

DM54AS253/DM74AS253 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and a non-inverting Tri-state output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

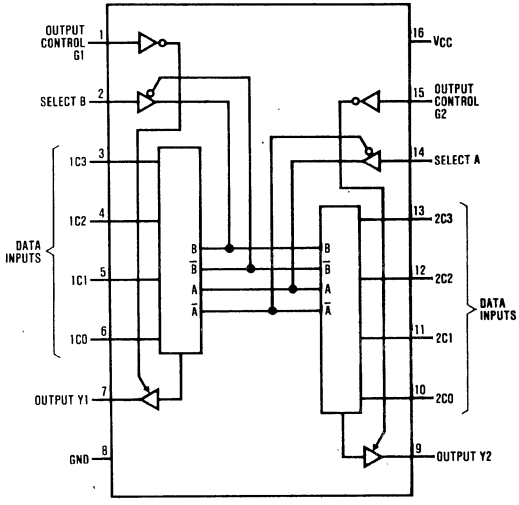
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS253	−55°C to 125°C
DM74AS253	0° to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6301-1

54AS253 (J) 74AS253 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Recommended Operating Conditions

Parameter	DM54AS253			DM74AS253			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2mA, V_{OC} = 4.5V to 5.5V		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V	A, B			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	A, B			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B		−0.6	−1	mA
			All others		−0.3	−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		17	29	mA
			Outputs low		20	32	
			Outputs disabled		21	33	

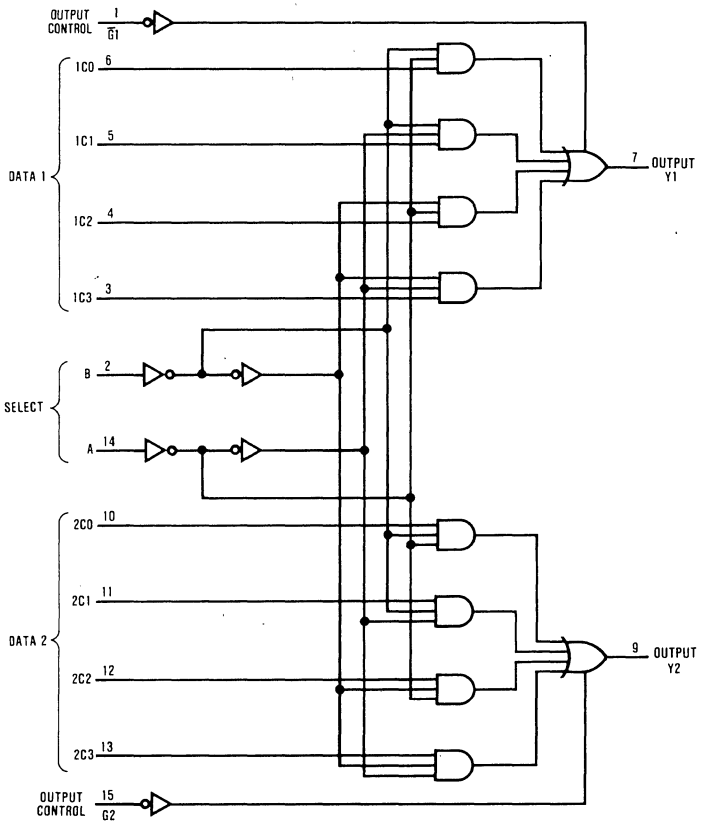
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS253			DM74AS253			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	4		14.5	4		13.5	ns
t_{PHL}, High to low Level Output				4		12	4		11.5	ns
t_{PLH}, Low to high Level Output	Data			3		8.5	3		7.5	ns
t_{PHL}, High to low Level Output				3		8.5	3		7.5	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y		4		13	4		12.5	ns
t_{ZL}, Output Enable Time to Low Level				4		12	4		11.5	ns
t_{HZ}, Output Disable Time From High Level				2		6.5	2		6	ns
t_{LZ}, Output Disable Time From Low Level				2		8	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6301-2

National Semiconductor

DM54AS/DM74AS257, 258 TRI-STATE® Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The AS257 presents true data whereas the AS258 presents inverted data to minimize propagation delay time.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 300 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

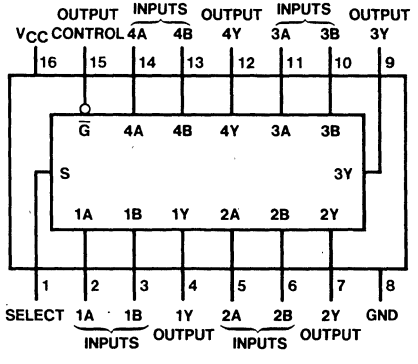
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6107-1

54AS257 (J) 74AS257 (J,N)
54AS258 (J) 74AS258 (J,N)

Function Table

Inputs				Output Y	
Output Control	Select	A	B	AS257	AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

Recommended Operating Conditions

Parameter	DM54AS257,258			DM74AS257,258			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage		V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
			I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC} −2V			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V	A, B, $\overline{G}$			0.1	mA
				Select			0.2	
I_{IH}	High Level Input Current		V_{CC} = 5.5V V_{IH} = 2.7V	A, B, $\overline{G}$			20	μA
				Select			40	
I_{IL}	Low Level Input Current		V_{CC} = 5.5V V_{IL} = 0.4V	Select			−1	mA
				All others			−0.5	
I_O	Output Drive Current		V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = 5.5V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CCH}	Supply Current	AS257	V_{CC} = 5.5V Outputs Open	Outputs High		12.9	19.7	mA
		AS258				8.8	13.5	mA
I_{CCL}	Supply Current	AS257		Outputs Low		19	30.6	mA
		AS258				15.8	24.6	mA
I_{CCZ}	Supply Current	AS257		Outputs Disabled		19.7	31.9	mA
		AS258				15.5	25.2	mA

'AS257 Switching Characteristics over recommended operating free air temperature range (Note 1)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From	To	Conditions	DM54AS257			DM74AS257			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Any Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	1		6.5	1		5.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				1		7	1		6	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Any Y		2		12	2		11	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2		10.5	2		10	ns
t_{ZH}	Output Enable Time to High Level	Output Control	Any Y		2		8.5	2		7.5	ns
t_{ZL}	Output Enable Time to Low Level				2		10.5	2		9.5	ns
t_{HZ}	Output Disable Time, from High Level	Output Control	Any Y		1.5		8	1.5		6.5	ns
t_{LZ}	Output Disable Time, from Low Level				2		8	2		7	ns

'AS258 Switching Characteristics over recommended operating free air temperature range (Note 1)

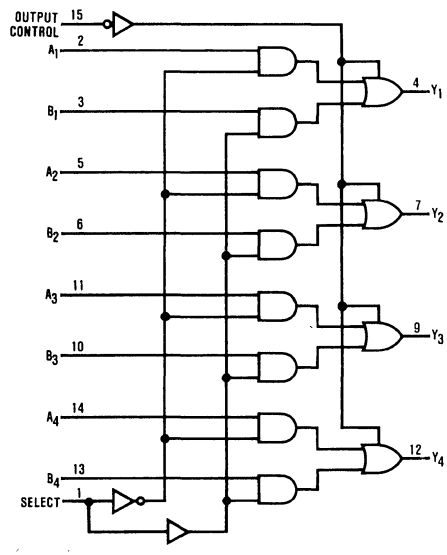
All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From	To	Conditions	DM54AS258			DM74AS258			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Any Y	$V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_L = 500\Omega$	1		5.5	1		5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				1		5	1		4	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Any Y		2		11	2		9.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2		11	2		10	ns
t_{ZH}	Output Enable Time to High Level	Output Control	Any Y		2		8.5	2		8	ns
t_{ZL}	Output Enable Time to Low Level				2		11	2		10	ns
t_{HZ}	Output Disable Time, from High Level	Output Control	Any Y		1.5		7	1.5		6	ns
t_{LZ}	Output Disable Time, from Low Level				2		8.5	2		6.5	ns

Note 1: See Section 1 for test waveforms and output load.

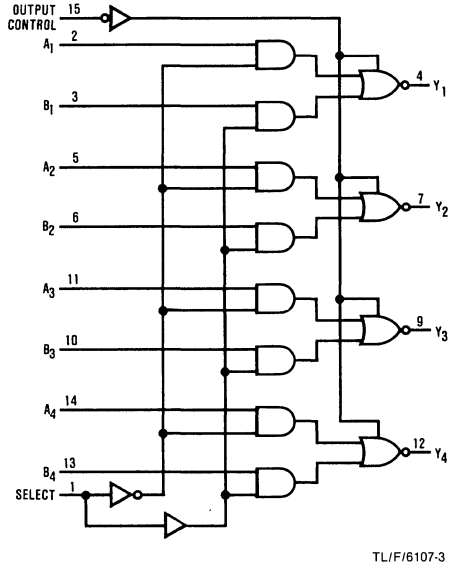
Logic Diagrams

54/74AS257



TL/F/6107-2

54/74AS258



TL/F/6107-3

National Semiconductor

PRELIMINARY

DM54AS264/DM74AS264 Look-Ahead Carry Generator

General Description

This circuit is a high speed, look-ahead carry generator capable of anticipating a carry across four counters. It is cascadable to perform look-ahead across N-bit counters. Carry, generate-carry and propagate-carry output functions are provided as shown in the connection diagram.

This circuit can accommodate counters which have either low level carry pulse or high level carry pulse outputs, and can provide high speed carry look-ahead capability for any word length. Each AS264 generates the look-ahead (anticipated carry) across a group of four counters, and in addition, other carry look-ahead circuits may be employed to anticipate a carry across sections of four look-ahead packages up to N bits. This method of cascading circuits to perform multi-level look-ahead is illustrated under Typical Applications.

Features

- Advanced oxide-isolated ion implanted Schottky TTL process
- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature range and V_{CC} range
- PNP inputs reduce input loading

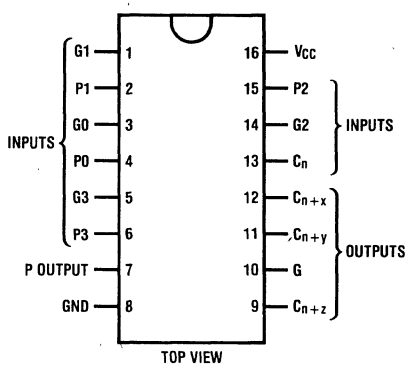
Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free-Air Temperature Range	
DM54AS264	−55°C to +125°C
DM74AS264	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



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DM54AS264 (J) DM74AS264 (N)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Recommended Operating Conditions

Symbol	Parameter	DM54AS264			DM74AS264			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54AS264			DM74AS264			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n	V_{CC} = 5.5V, V_I = 7V			500			500	μA
	G0, G7				700			700	
	G1				800			800	
	G3, P0, P1				400			400	
	P2				300			300	
	P3				200			200	
I_{IH}	C_n	V_{CC} = 5.5V, V_I = 2.7V			100			100	μA
	G0, G2				140			140	
	G1				160			160	
	G3, P0, P1				80			80	
	P2				60			60	
	P3				40			40	
I_{IL}	C_n	V_{CC} = 5.5V, V_I = 0.4V			−2.5			−2.5	mA
	G0				−3.5			−3.5	
	G1, G2				−4			−4	
	G3, P0, P1				−2			−2	
	P2				−1			−1	
	P3				−1.5			−1.5	
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		26			26		mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		28			28		mA

Switching Characteristics over recommended supply and temperature range (Note 1)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter		From (Input)	To (Output)	Conditions	DM54AS264			DM74AS264			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	$C_L = 50$ pF, $R_L = 500\Omega$		5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P1, P2, or P3	G			5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P0, P1, P2, or P3	P			5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6			6		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		

Note 1: See Section 1 for test waveforms and output load.

Function Tables

Logic Equations for the 'AS264 are:

Active High Carry Counters (C_n = H)

$C_{n+x} = \overline{G0}$
$C_{n+y} = \overline{G0} \cdot \overline{G1}$
$C_{n+z} = \overline{G0} \cdot \overline{G1} \cdot \overline{G2}$
$\overline{G} = \overline{G0} \cdot \overline{G1} \cdot \overline{G2} \cdot \overline{G3}$
$\overline{P} = 0$

Active Low Carry Counters (C_n = L)

$C_{n+x} = \overline{P0}$
$C_{n+y} = \overline{P0} \cdot \overline{P1}$
$C_{n+z} = \overline{P0} \cdot \overline{P1} \cdot \overline{P2}$
$\overline{P} = \overline{P0} + \overline{P1} + \overline{P2} + \overline{P3}$
$G = \overline{P1}\,\overline{G3}\,\overline{G2}\,\overline{G1} + \overline{P2}\,\overline{G3}\,\overline{G2}\,\overline{G1} + \overline{P3}\,\overline{G3}$

Inputs								Output
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{G}$
L	X	X	X	X	X	X	X	L
X	L	X	X	L	X	X	X	L
X	X	L	X	L	L	X	X	L
X	X	X	L	L	L	L	X	L
X	X	X	X	L	L	L	L	L
All Other Combinations								H

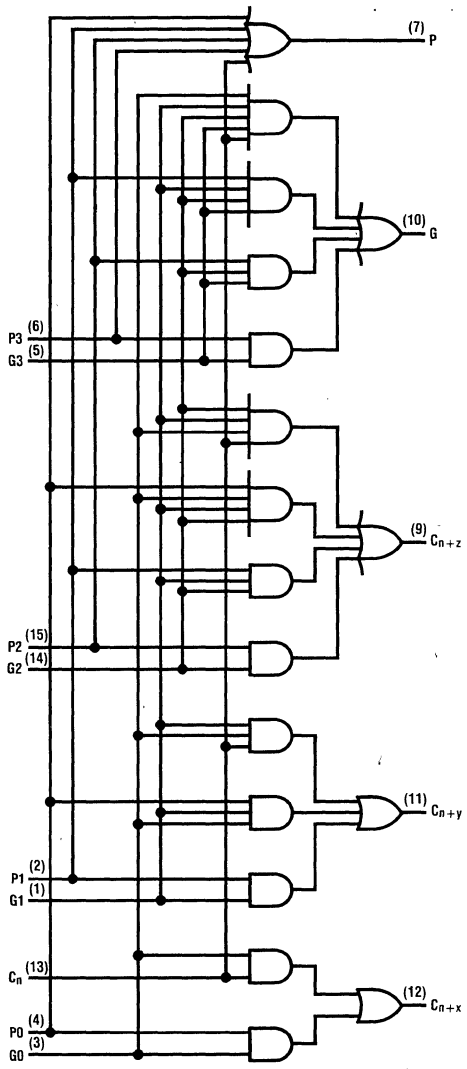
Inputs					Output
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	$\overline{P}$
L	L	L	L	L	L
All Other Combinations					H

Inputs			Output
G0	P0	C_n	C_{n+x}
H	H	X	H
H	X	H	H
All Other Combinations			L

Inputs					Output
G1	G0	P1	P0	C_n	C_{n+y}
H	X	H	X	X	H
H	H	X	H	X	H
H	H	X	X	H	H
All Other Combinations					L

Inputs							Output
G2	G1	G0	P2	P1	P0	C_n	C_{n+z}
H	X	X	H	X	X	X	H
H	H	X	X	H	X	X	H
H	H	H	X	X	H	X	H
H	H	H	X	X	X	H	H
All Other Combinations							L

Logic Diagram



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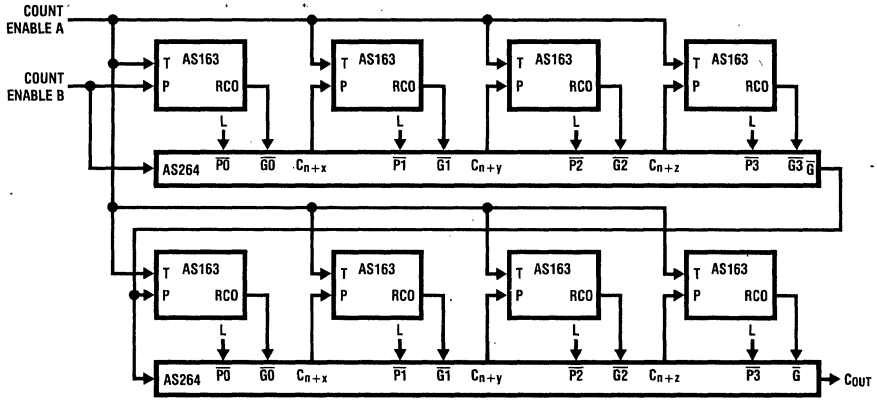
V_{CC} = pin 16
GND = pin 8

Typical Applications

Active High Carry Scheme



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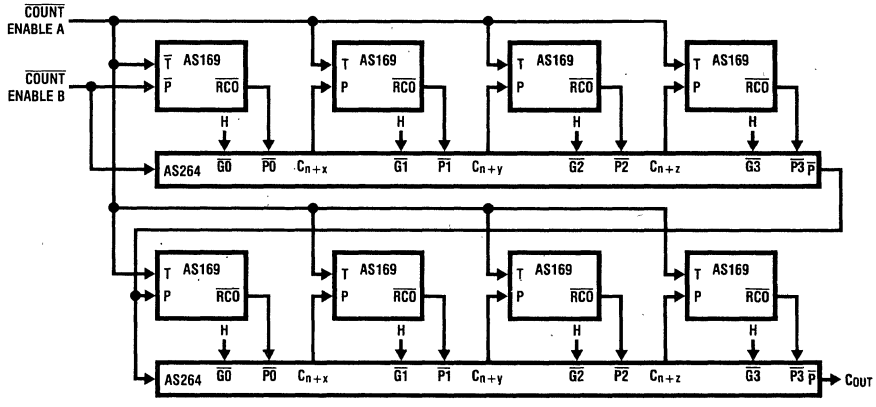
Active Low Carry Scheme



TL/F/6302-4

National Semiconductor

PRELIMINARY

DM54AS280/DM74AS280 9-Bit Parity Generator/Checker

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

The AS280 can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the AS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and no internal connection at pin 3. This permits the AS280 to be substituted for the '180 in existing designs to produce identical function even if 'AS280s are mixed with existing '180s.

Features

- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for N-bits
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

Absolute Maximum Ratings (Note 1)

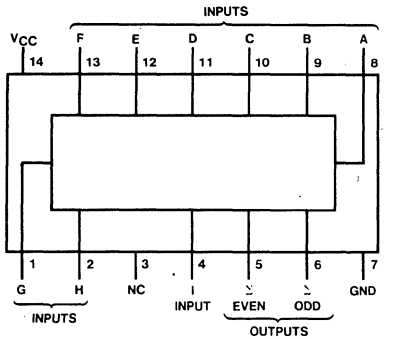
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



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54AS280 (J) **74AS280 (J, N)**

Function Table

Number of Inputs (A Thru I) that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

L = Low State
H = High State

Recommended Operating Conditions

Parameter	DM54AS280			DM74AS280			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−2			−2	mA
Low Level Output Current, I_{OL}			20			20	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = Max			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	DM54AS		25	40	mA
			DM74AS		25	35	

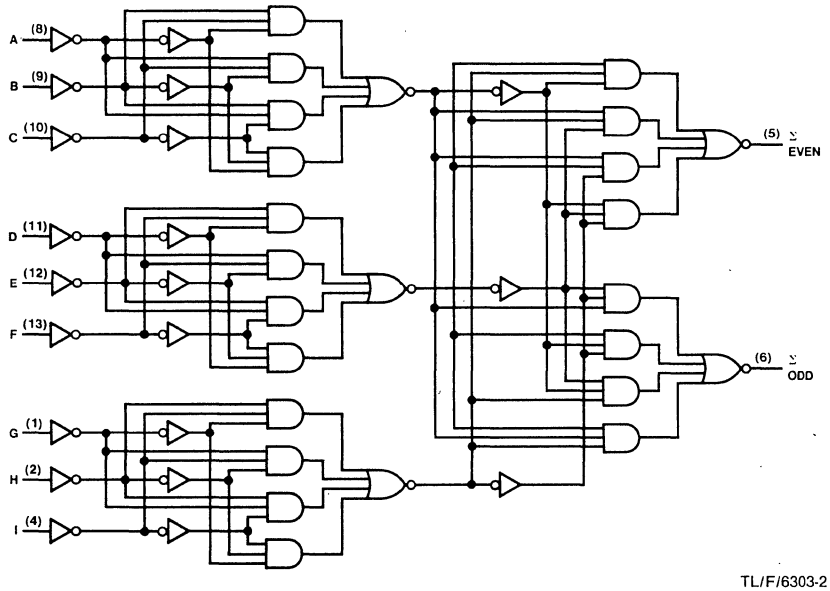
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	From	To	Conditions	DM54AS280			DM74AS280			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Σ Even	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	2		15	2		14	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2		15	2		14	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Σ Odd		2		15	2		14	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2		15	2		14	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



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Typical Applications

Three AS280s can be used to implement a 25-line parity generator/checker.

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (AS86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading AS280s. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits.

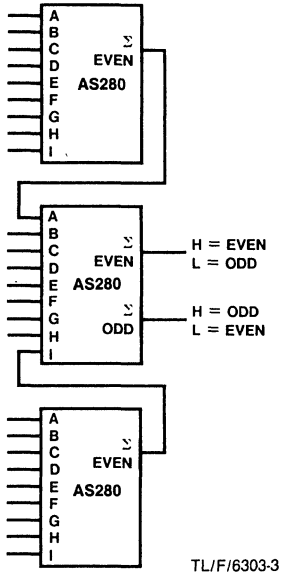

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FIGURE 1. 25-Line Parity/Generator Checker

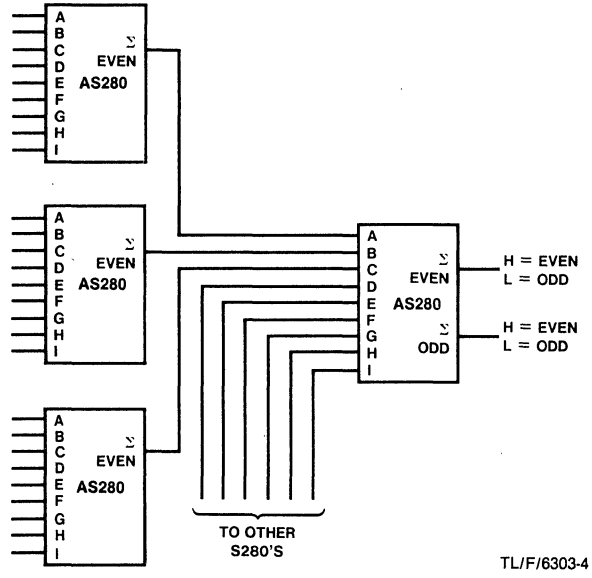

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FIGURE 2. 81-Line Parity/Generator Checker

National Semiconductor

PRELIMINARY

DM54AS282/DM74AS282 Look-Ahead Carry Generator with Selectable Carry Inputs

General Description

This circuit is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. It is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided.

When used in conjunction with the 'AS881 arithmetic logic unit, this generator provides high-speed carry look-ahead capability for any word length. Each 'AS282 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under Typical Applications.

The carry functions (inputs, outputs, generate and propagate) of the look-ahead generator are implemented in compatible forms for direct connection to the 'AS881 ALU. The carry inputs are selectable in either active high or active low.

Features

- Selectable input version of 'AS182 allows double precision carry
- Advanced oxide-isolated ion-implanted Schottky TTL process
- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- PNP inputs reduce input loading

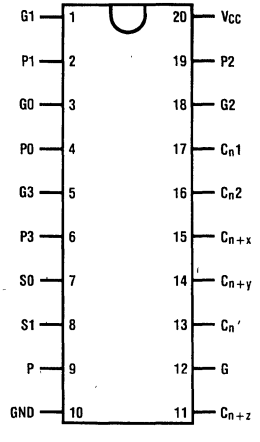
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free-Air Temperature Range	
DM54AS282	−55°C to 125°C
DM74AS282	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

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DM54AS282 (J) **DM74AS282 (N)**

Recommended Operating Conditions

Symbol	Parameter	DM54AS282			DM74AS282			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54AS282			DM74AS282			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	C_n1, C_n2	V_{CC} = 5.5V, V_I = 7V			200			200	μA
	S0, S1, P3				200			200	
	P2				300			300	
	P0, P1, G3				400			400	
	G0, G2				700			700	
	G1				800			800	
I_{IH}	C_n1, C_n2	V_{CC} = 5.5V, V_I = 2.7V			40			40	μA
	S0, S1, P3				40			40	
	P2				60			60	
	P0, P1, G3				80			80	
	G0, G2				140			140	
	G1				160			160	
I_{IL}	C_n1, C_n2	V_{CC} = 5.5V, V_I = 0.4V			−1			−1	mA
	S0, S1, P3				−1			−1	
	P2				−1.5			−1.5	
	P0, P1, G3				−2			−2	
	G0, G2				−3.5			−3.5	
	G1				−4			−4	
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−117	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		22			22		mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		26			26		mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current I_{OS}.

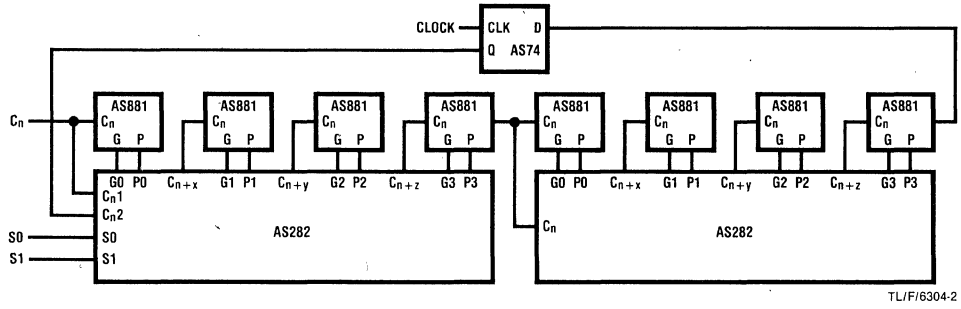
Switching Characteristics over recommended supply and temperature range (Note 1)

Sym	Parameter	From (Input)	To (Output)	Conditions	DM54AS282			DM74AS282			Units
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	$C_L = 50$ pF, $R_L = 500\Omega$		5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P1, P2, or P3	G			6			6		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P0, P1, P2, or P3	P			5			5		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					5			5		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6			6		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					6			6		
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n1, C_n2, S1, S2	C_n'			6			6		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					6			6		

Note 1: See Section 1 for test waveforms and output load.

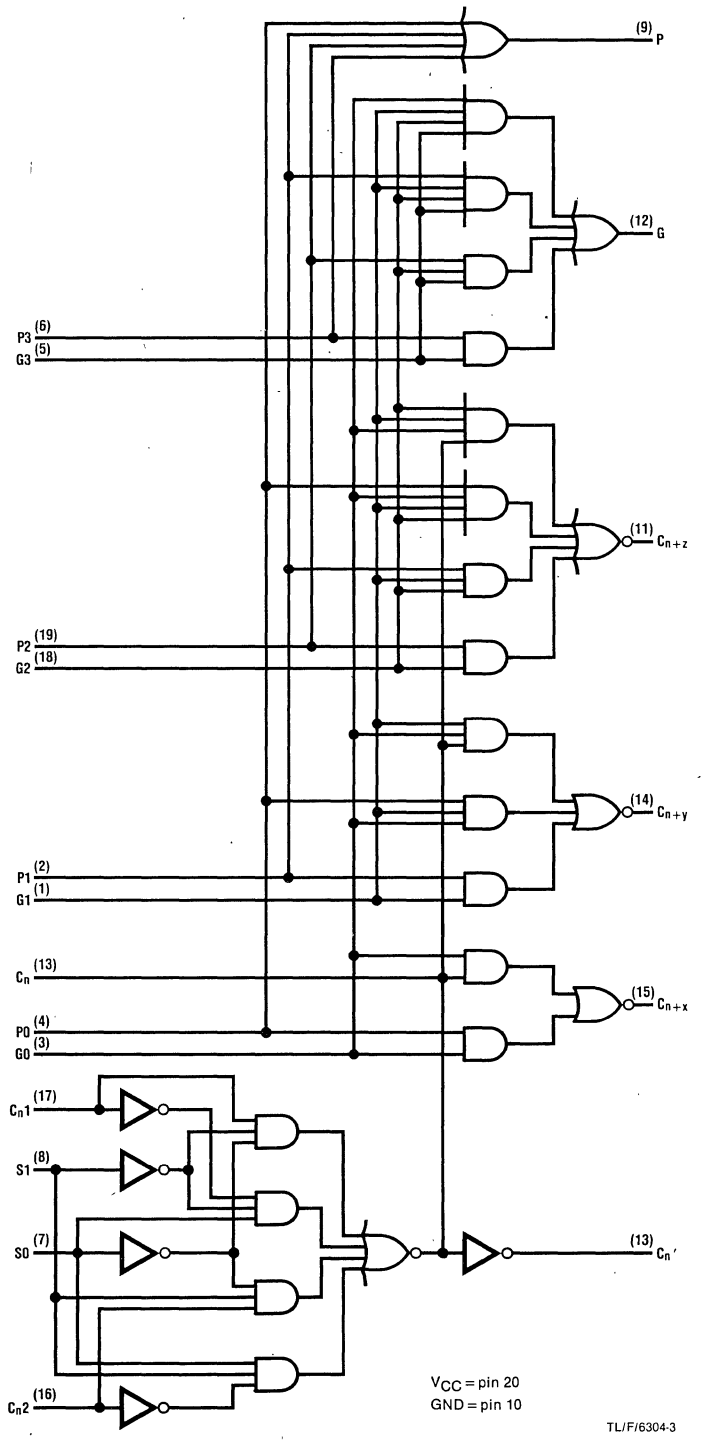
Typical Application

32 Bit Look-Ahead Carry with Double Precision Carry



TL/F/6304-2

Logic Diagram



National Semiconductor

PRELIMINARY

DM54AS286/DM74AS286 9-Bit Parity Generator/Checker with Bus-Driver Parity I/O Port

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

The 'AS286 can be usd to upgrade the performance of most systems utilizing the 'AS180, 'AS280 parity generator/ checker. Although the 'AS286 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4. Pin 4 ($\overline{XMIT}$) is a control line which makes parity error output active and parity an input port when "high"; when "low", parity error output is inactive and parity becomes an output port. In addition, parity I/O control circuitry contains a feature to keep the I/O port in the TRI-STATE® during power up or down to prevent bus glitches.

Features

- PNP inputs to reduce bus loading
- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for n-bits
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- A parity I/O portable to drive bus

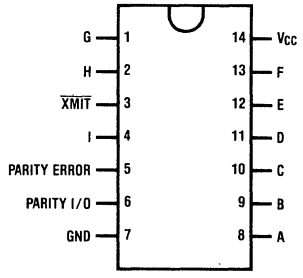
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6305-1

DM54AS286 (J) DM74AS286 (J, N)

Function Table

Number of Inputs (A thru I) that are High	Parity I/O		$\overline{XMIT}$	Parity Error	Mode of Operation
	Input	Output			
0, 2, 4, 6, 8	N/A	H	L	H	Parity Generator
1, 3, 5, 7, 9	N/A	L	L	H	
0, 2, 4, 6, 8	H	N/A	H	H	Parity Checker
0, 2, 4, 6, 8	L	N/A	H	L	
1, 3, 5, 7, 9	H	N/A	H	L	Parity Checker
1, 3, 5, 7, 9	L	N/A	H	H	

Recommended Operating Conditions

Symbol	Parameter		DM54AS286			DM74AS286			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current	Parity I/O			−12			−15	mA
		Parity Error			−2			−2	mA
I_{OL}	Low Level Output Current	Parity I/O			32			48	mA
		Parity Error			20			20	mA
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended free-air temperature range (Note 1)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Sym	Parameter	Conditions		DM54AS286			DM74AS286			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.2			−1.2	V
V_{OH}	High Level Output Voltage	$I_{OH} = Max$, $V_{CC} = 4.5V$		2.4	3.2		2.4	3.2		V
		$I_{OH} = -2$ mA		$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5V$ to $5.5V$								
V_{OL}	Parity Error	$V_{CC} = 4.5V$, $I_{OL} = 20$ mA			0.35	0.5		0.35	0.5	V
	Parity I/O	$V_{CC} = 4.5V$, $I_{OL} = 32$ mA				0.5				V
		$V_{CC} = 4.5V$, $I_{OL} = 48$ mA							0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$ ($V_I = 5.5V$ for Parity I/O)				0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$	Others			20			20	μA
			Parity I/O			50			50	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5			−0.5	mA
I_{OZH}	High Level TRI-STATE Output Current	$V_{CC} = 5.5V$, $V = 2.7V$ I/O Port Pin 6				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	$V_{CC} = 5.5V$, $V = 0.4V$ I/O Port Pin 6				−0.5			−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	−30		−112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Transmit Mode Input of Pin 3 Low				42			42	mA
		Receive Mode Input of Pin 3 High				49			49	mA

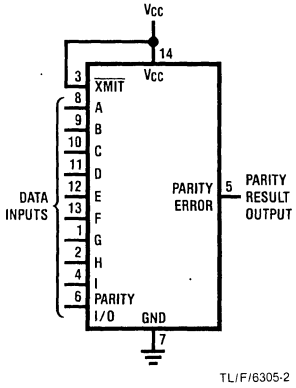
Note 1: See Section 1 for test waveforms and output load.

Switching Characteristics over recommended supply and temperature range (Note 1)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

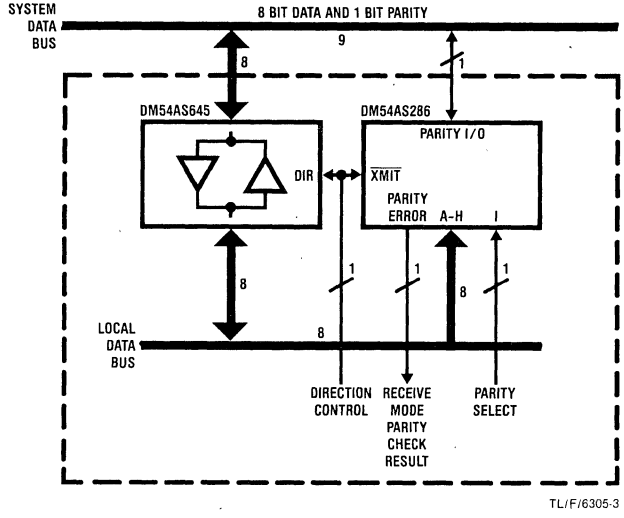
Sym	Parameter	From	To	DM54AS286			DM74AS286			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time from Low to High Level Output	Any Data Input	Parity I/O Pin 6		8			8		ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Any Data Input	Parity I/O Pin 6		8.5			8.5		ns
t_{PLH}	Propagation Delay Time from Low to High Level Output	Any Data Input	Parity Error Pin 5		9			9		ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Any Data Input	Parity Error Pin 5		9.5			9.5		ns
t_{PLH}	Propagation Delay Time from Low to High Level Output	Parity I/O Pin 6	Parity Error Pin 5		5.0			5.0		ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Parity I/O Pin 6	Parity Error Pin 5		6.0			6.0		ns
t_{PZL}	Output Enable to Low Level	Control Pin 3	Parity I/O Pin 6		6			6		ns
t_{PZL}	Output Disable from Low Level	Control Pin 3	Parity I/O Pin 6		9.5			9.5		ns
t_{PZH}	Output Disable from High Level	Control Pin 3	Parity I/O Pin 6		5			5		ns
t_{PHZ}	Output Enable to High Level	Control Pin 3	Parity I/O Pin 6		10			10		ns

Note 1: See Section 1 for test waveforms and output load.



Number of Inputs that are Logic '1'		Parity Result Output
0, 2, 4, 6, 8, 10	Even	L
1, 3, 5, 7, 9	Odd	H

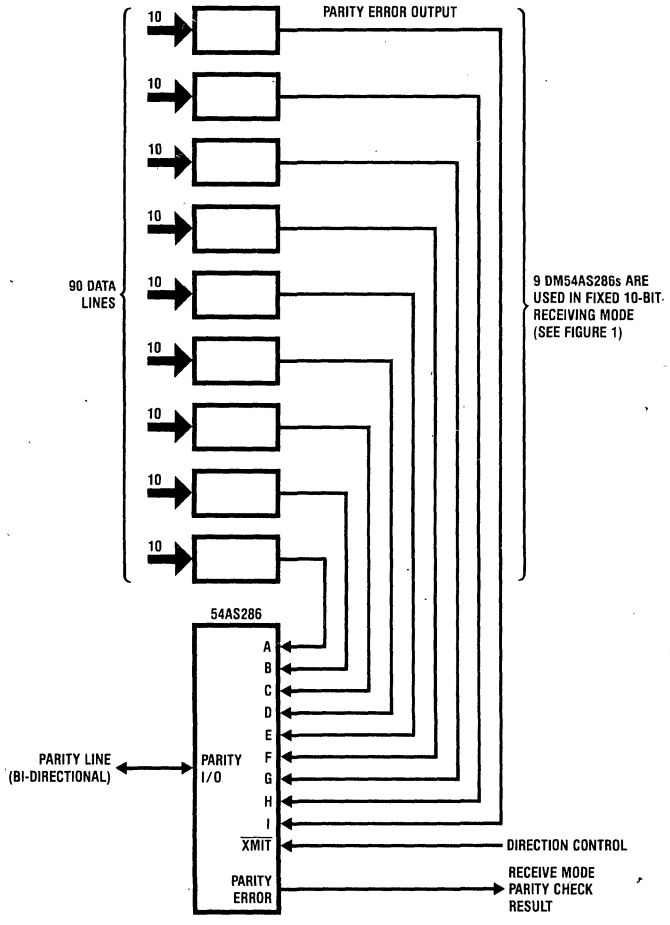
FIGURE 1. Dedicated 10-Bit Parity Sensing Configuration



Direction Control (XMIT)	I/O Direction (Parity I/O)	Parity Check Result (Parity Error) Level	Σ Result
H	Input (Receive)	H	True
		L	False
L	Output (Transmit)	H	N/A

Parity Select (Input I) Level	Format
H	Even
L	Odd

FIGURE 2. Bus I/O Parity Implementation



Note: Parity format in this configuration is "odd parity"

FIGURE 3. 90-Bit Parity Generator/Checker Implementation Using Device Expansion Techniques

National Semiconductor

PRELIMINARY

DM54AS352/DM74AS352 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and an inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with the LS and Schottky Family counterpart.
- Improved output transient handling capability.

Absolute Maximum Ratings (Note 1)

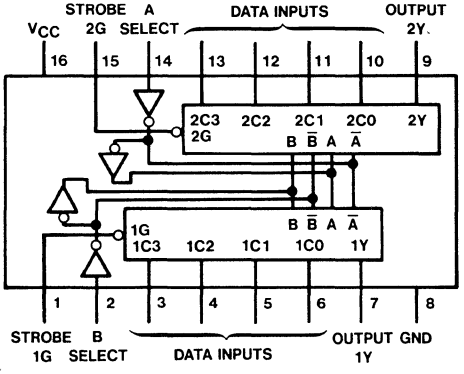
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS352	−55°C to 125°C
DM74AS352	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6307-1

54AS352 (J) **74AS352 (J,N)**

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54AS352			DM74AS352			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V	A, B			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	A, B			40	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B		−0.3	−1	mA
			All others		−0.3	−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		15.5	25	mA
			Outputs low		17.5	28	

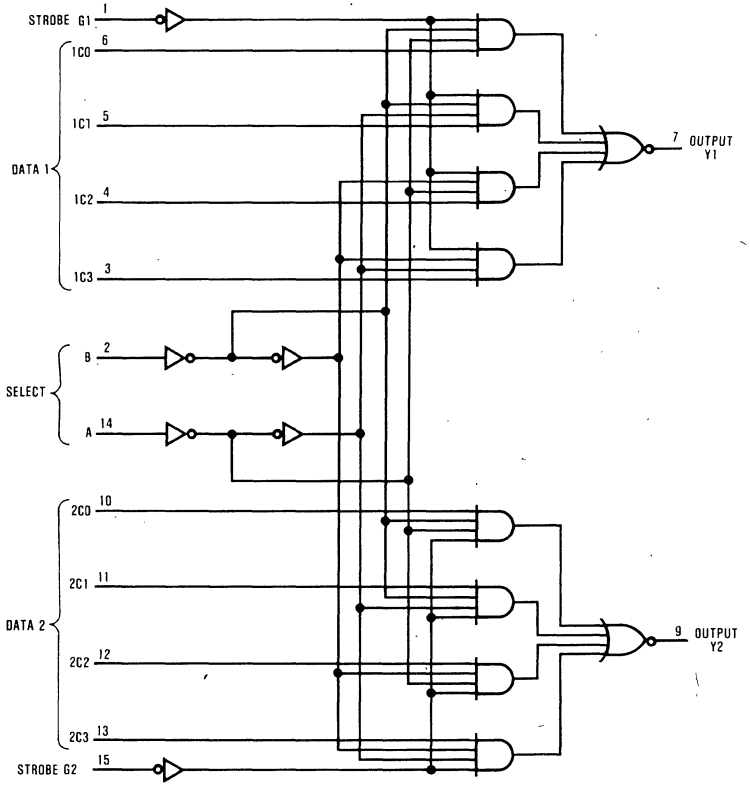
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS352			DM74AS352			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	4		12.5	4		11	ns
t_{PHL}, High to low Level Output				4		14	4		13	ns
t_{PLH}, Low to high Level Output	Data			2		7.5			6.5	ns
t_{PHL}, High to low Level Output				2		7			6	ns
t_{PLH}, Low to high Level Output	Strobe			3		8			7	ns
t_{PHL}, High to low Level Output				4		13.5			12	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6307-2

National Semiconductor

PRELIMINARY

DM54AS353/DM74AS353 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and an inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with LS and Schottky Family counterpart.
- Improved output transient handling capability.
- Output Control circuitry incorporates power-up TRI-STATE feature.

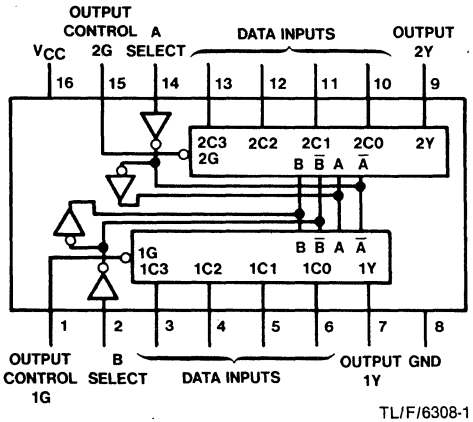
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS353	−55°C to +125°C
DM74AS353	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6308-1

54AS353 (J) 74AS353 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs A and B are common to both sections
H = High Level. L = Low Level. X = Don't Care.
Z = High Impedance State

Recommended Operating Conditions

Parameter	DM54AS353			DM74AS353			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			12			15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V	A, B			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	A, B			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B			−1	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		15	24	mA
			Outputs low		19	31	
			Outputs disabled		18	30	

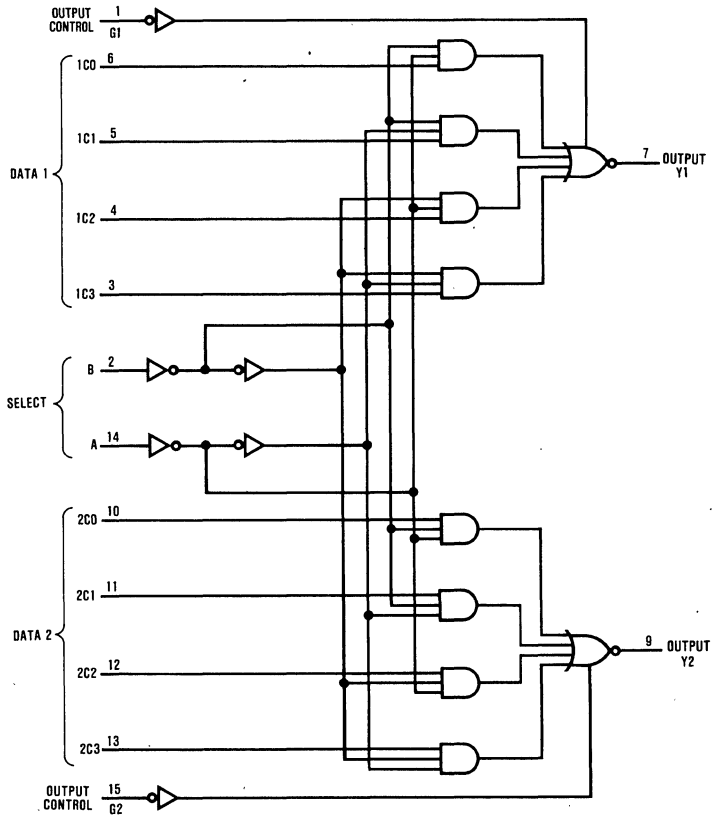
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS353			DM74AS353			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V C_L = 50 pF R_L = 500 Ω	3		10	3		9	ns
t_{PHL}, High to low Level Output				4		14	4		12	ns
t_{PLH}, Low to high Level Output	Data			3		8.5	3		7.5	ns
t_{PHL}, High to low Level Output				2		6.5	2		6	ns
t_{ZH}, Output Enable Time to High Level	Output Control			3		8.5	3		7.5	ns
t_{ZL}, Output Enable Time to Low Level				4		12	4		11	ns
t_{HZ}, Output Disable Time From High Level				2		6.5	2		5.5	ns
t_{LZ}, Output Disable Time From Low Level				3		9	3		7.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6308-2

National Semiconductor

DM54AS373/DM74AS373 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS and ALS TTL Counterparts.
- Improved AC Performance Over LS and ALS TTL Counterparts.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

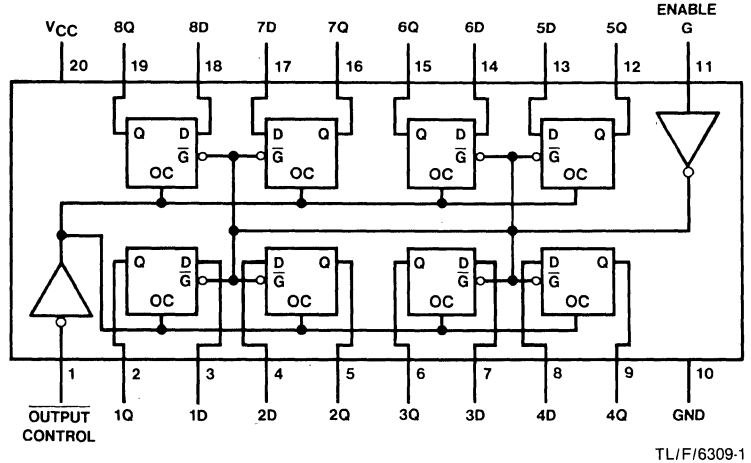
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS373	−55°C to 125°C
DM74AS373	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6309-1

54AS373 (J) 74AS373 (J,N)

Recommended Operating Conditions

Parameter	DM54AS373			DM74AS373			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High	5.5			4.5			ns
Data Setup Time, T_{SU}	2↓			2↓			ns
Data Hold Time, T_H	3↓			3↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ I_{OH} = MAX		2.4	3.2		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC}-2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 2.7V$				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 0.4V$				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		55	90	mA
			Outputs Low		55	85	
			Outputs Disabled		65	100	

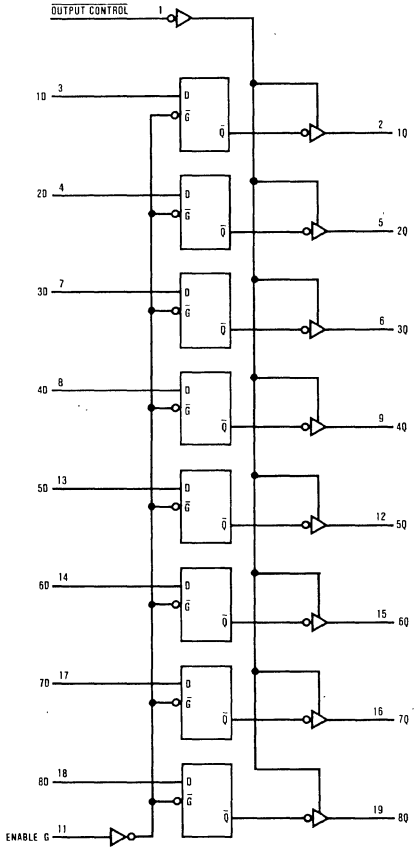
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS373			DM74AS373			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3.5		8	3.5		6	ns
T_{PHL}				3.5		7	3.5		6	ns
T_{PLH}	Enable	Any Q		6.5		14	6.5		11.5	ns
T_{PHL}				5		8	5		7.5	ns
T_{PZH}	Output Control	Any Q		2		7.5	2		6.5	ns
T_{PZL}				4.5		10.5	4.5		9.5	ns
T_{PHZ}				3		7.5	3		6.5	ns
T_{PLZ}				3		8	3		7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6309-2

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

3

National Semiconductor

DM54AS374/DM74AS374 Octal D-Type-Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS and ALS TTL Counterparts.
- Improved AC Performance Over LS and ALS TTL Counterparts.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

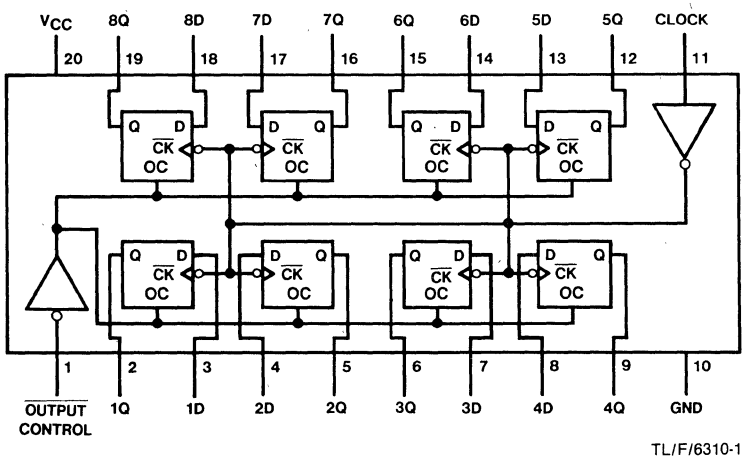
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS374	−55°C to 125°C
DM74AS374	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6310-1

54AS374 (J) 74AS374 (J,N)

Recommended Operating Conditions

Parameter		DM54AS374			DM74AS374			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5.5			4			ns
	Low	5			3			
Data Setup Time, T_{SU}		3↑	0		2↑	0		ns
Data Hold Time, T_H		3↑	0		2↑	0		ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$ $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $I_{OH} = MAX$		2.4	3.2		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to $5.5V$		$V_{CC}-2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = MAX$			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$ $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$ $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$ $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$ $V_O = 2.7V$				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$ $V_O = 0.4V$				−50	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		77	120	mA
			Outputs Low		84	128	
			Outputs Disabled		84	128	

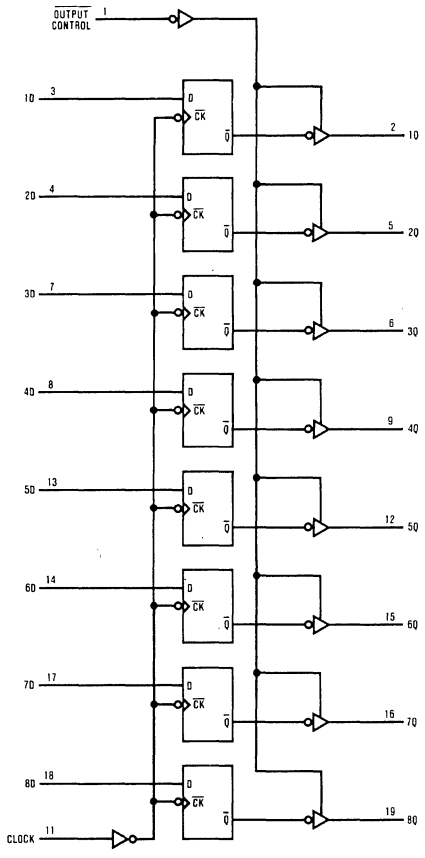
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS374			DM74AS374			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\,\Omega$ $C_L = 50$ pF	100			125			MHz
T_{PLH}	Clock	Any Q		3		11	3		8	ns
T_{PHL}				4		11.5	4		9	ns
T_{PZH}	Output Control	Any Q		2		7	2		6	ns
T_{PZL}				3		11	3		10	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6310-2

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

3

National Semiconductor

DM54AS533/DM74AS533 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS533 are transparent D-type latches meaning that while the enable (G) is high the $\overline{Q}$ outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

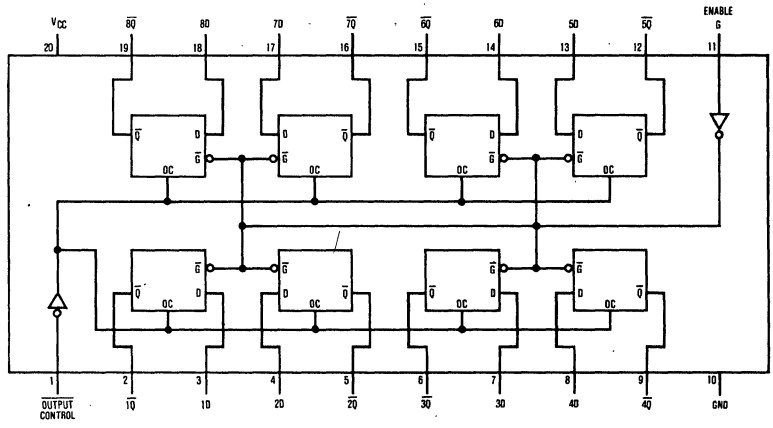
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS533	−55°C to 125°C
DM74AS533	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6311-1

54AS533 (J) **74AS533 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS533			DM74AS533			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High or Low	5.5			4.5			ns
Data Setup Time, T_{SU}	2↑			2↑			ns
Data Hold Time, T_H	3↑			3↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{VO} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		62	100	mA
			Outputs Low		64	100	
			Outputs Disabled		71	110	

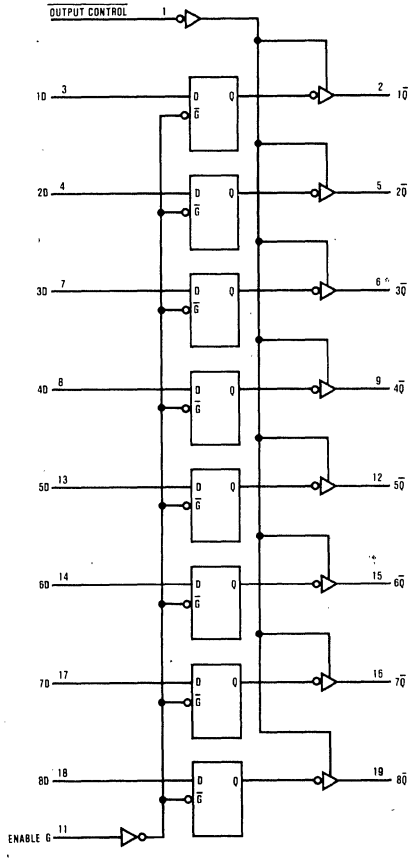
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS533			DM74AS533			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF .	4		10	4		7.5	ns
T_{PHL}				4		8	4		7	ns
T_{PLH}	Enable	Any $\overline{Q}$		5		11	5		9	ns
T_{PHL}				4.5		8.5	4.5		8	ns
T_{PZH}	Output Control	Any $\overline{Q}$		2		7.5	2		6.5	ns
T_{PZL}				4.5		10.5	4.5		9.5	ns
T_{PHZ}				3		7.5	3		6.5	ns
T_{PLZ}				3		8	3		7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6311-2

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low state, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54AS534/DM74AS534 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Llnes Directly.

Absolute Maximum Ratings (Note 1)

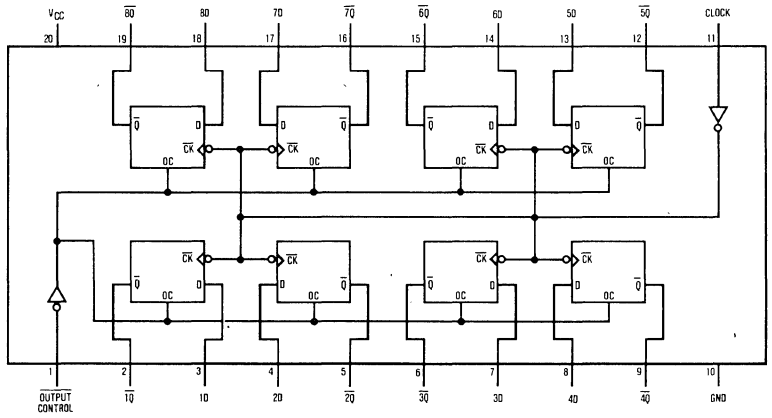
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS534	−55°C to 125°C
DM74AS534	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6312-1

54AS534 (J) **74AS534 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS534			DM74AS534			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5.5			4			ns
	Low	5			3			
Data Setup Time, T_{SU}		3↑			2↑			ns
Data Hold Time, T_H		3↑			2↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $I_{OH} = MAX$		2.4	3.2		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to $5.5V$		$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = MAX$			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 2.7V$				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 0.4V$				−50	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs High		77	120	mA
			Outputs Low		84	128	
			Outputs Disabled		84	128	

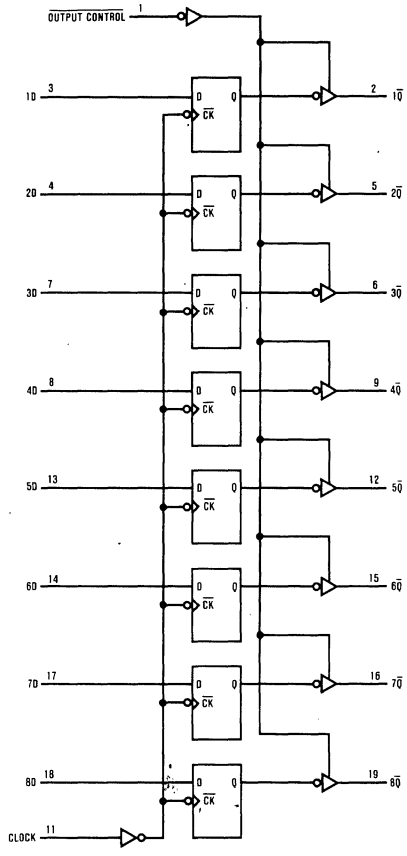
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS534			DM74AS534			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\ \Omega$ $C_L = 50\ pF$	100			125			MHz
T_{PLH}	Clock	Any $\bar{Q}$		3		11	3		8	ns
T_{PHL}				4		11.5	4		9	ns
T_{PZH}	Output Control	Any $\bar{Q}$		2		7	2		6	ns
T_{PZL}				3		11	3		10	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6312-2

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\bar{Q}_0$ = Previous Condition of $\bar{Q}$

National Semiconductor

DM54AS573/DM74AS573 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS573 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with S373.
- Improved AC Performance Over S373 at Approximately Half the Power.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings (Note 1)

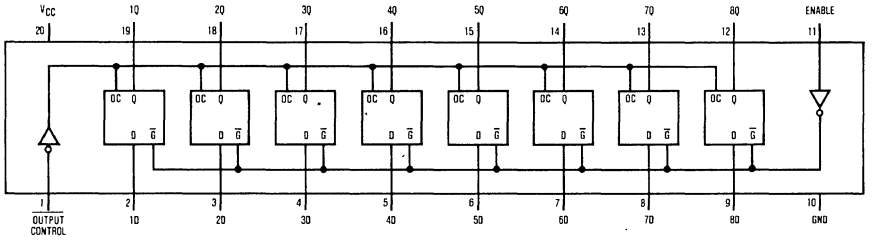
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS573	−55°C to 125°C
DM74AS573	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6313-1

54AS573 (J) **74AS573 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS573			DM74AS573			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High or Low	5.5			4.5			ns
Data Setup Time, T_{SU}	2↑			2↑			ns
Data Hold Time, T_H	3↑			3↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$		$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		56	93	mA
			Outputs Low		55	90	
			Outputs Disabled		65	106	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS573			DM74AS573			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		9	3		6	ns
T_{PHL}				3		7	3		6	ns
T_{PLH}	Enable	Any Q		6		14	6		11.5	ns
T_{PHL}				4		9	4		7.5	ns
T_{PZH}	Output Control	Any Q		2		8	2		6.5	ns
T_{PZL}				4		11	4		9.5	ns
T_{PHZ}				2		8	2		6.5	ns
T_{PLZ}				2		8	2		7	ns

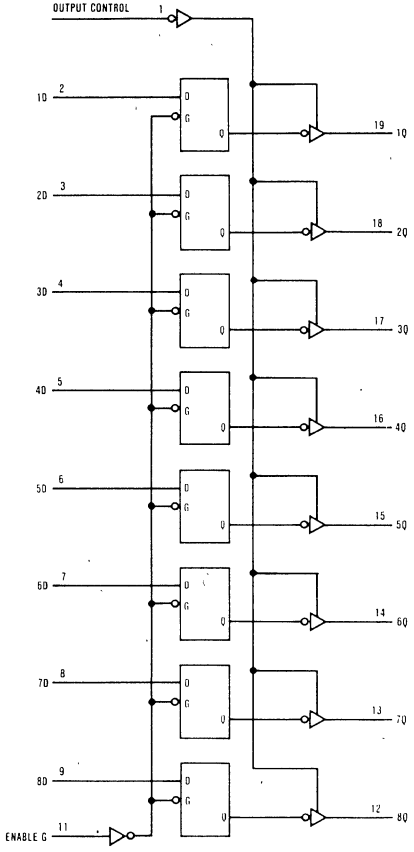
Note 1: See Section 1 for test waveforms and output load.

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6313-2

National Semiconductor

DM54AS574/DM74AS574 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with S374.
- Improved AC Performance Over S374 at Approximately Half the Power.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

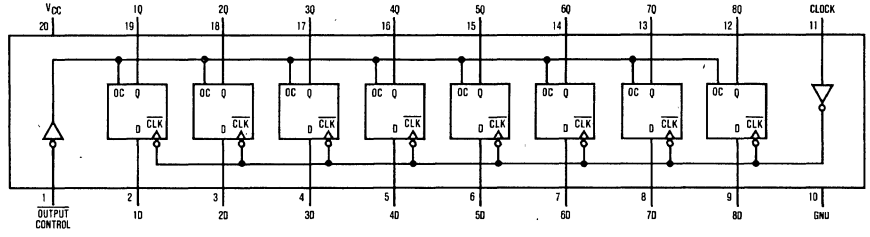
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS574	−55°C to 125°C
DM74AS574	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6314-1

54AS574 (J) 74AS574 (J,N)

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

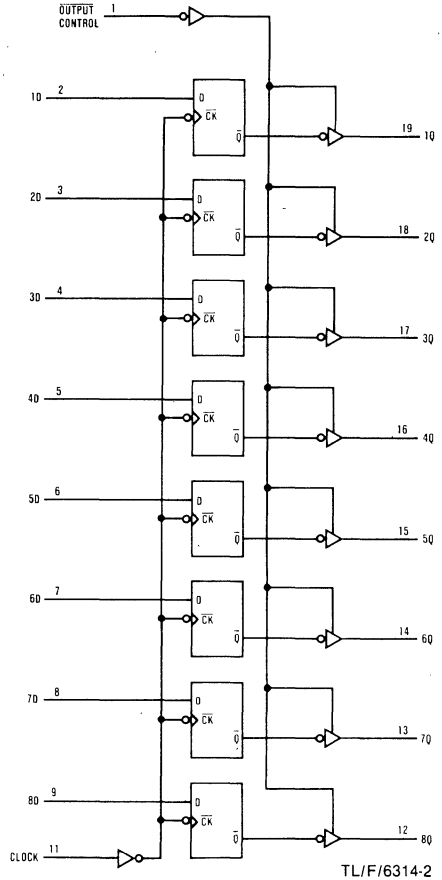
L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54AS574			DM74AS574			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5			4			ns
	Low	3			2			
Data Setup Time, T_{SU}		3↑			2↑			ns
Data Hold Time, T_H		3↑			2↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Logic Diagram



TL/F/6314-2

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		73	116	mA
			Outputs Low		85	134	
			Outputs Disabled		84	134	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS574			DM74AS574			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V $R_L = 500\ \Omega$ C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any Q		3		11	3		8	ns
T_{PHL}				4		11	4		9	ns
T_{PZH}	Output Control	Any Q		2		7	2		6	ns
T_{PZL}				3		11	3		10	ns
T_{PHZ}	Output Control	Any Q		2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS575/DM74AS575 Octal D-Type Edge-Triggered Flip-Flops with Synchronous Clear

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS575 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Synchronous Clear

Absolute Maximum Ratings (Note 1)

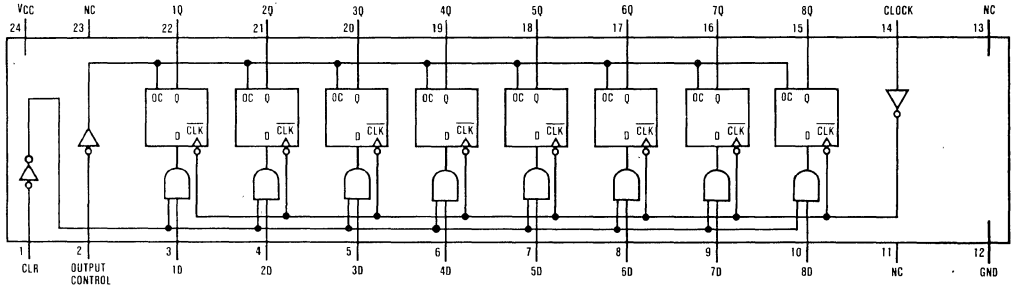
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS575	−55°C to 125°C
DM74AS575	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram

Dual-In-Line Package



TL/F/6315-1

54AS575 (J) 74AS575 (J,N)

Function Table

Output Control	$\overline{CLR}$	Clock	D	Output Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

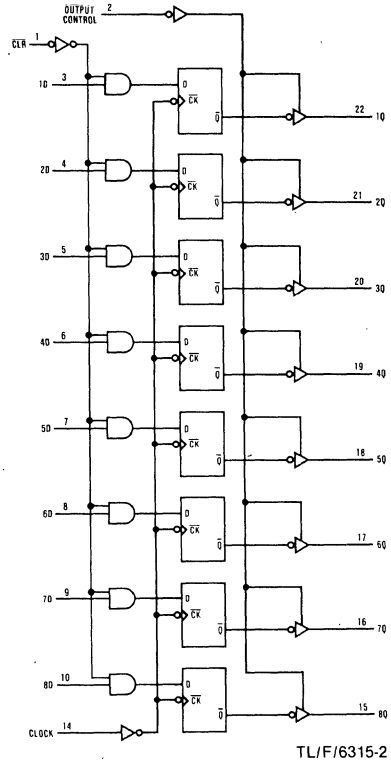
L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q
NC = No Internal Connection

Recommended Operating Conditions

Parameter		DM54AS575			DM74AS575			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5			4			ns
	Low	3			2			
Data Setup Time, T_{SU}	DATA	3↑			2↑			ns
	$\overline{CLR}$ High or Low	6.5↑			5.5↑			
Data Hold Time, T_H	DATA	3↑			2↑			ns
	$\overline{CLR}$	0↑			0↑			

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Logic Diagram



TL/F/6315-2

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$		$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		78	126	mA
			Outputs Low		88	142	
			Outputs Disabled		88	142	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS575			DM74AS575			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V $R_L = 500\ \Omega$ C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any Q		3		11	3		8	ns
T_{PHL}				4		11	4		9	ns
T_{PZH}	Output Control	Any Q		2		7	2		6	ns
T_{PZL}				3		11	3		10	ns
T_{PHZ}	Output Control	Any Q		2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS576/DM74AS576 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS576 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

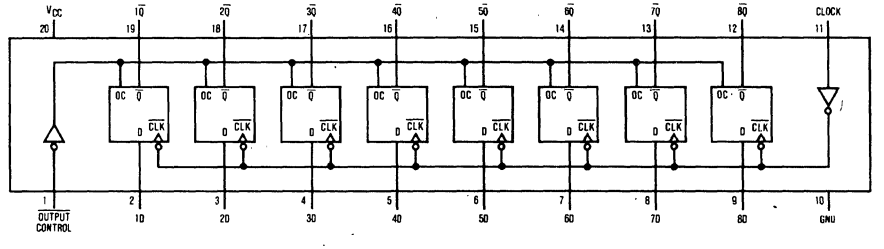
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS576	−55°C to 125°C
DM74AS576	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6316-1

54AS576 (J) 74AS576 (J,N)

Recommended Operating Conditions

Parameter		DM54AS576			DM74AS576			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5			4			ns
	Low	3			2			
Data Setup Time, T_{SU}		3↑			2↑			ns
Data Hold Time, T_H		3↑			2↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

3

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to $5.5V$		$V_{CC} -2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		77	125	mA
			Outputs Low		84	135	
			Outputs Disabled		84	135	

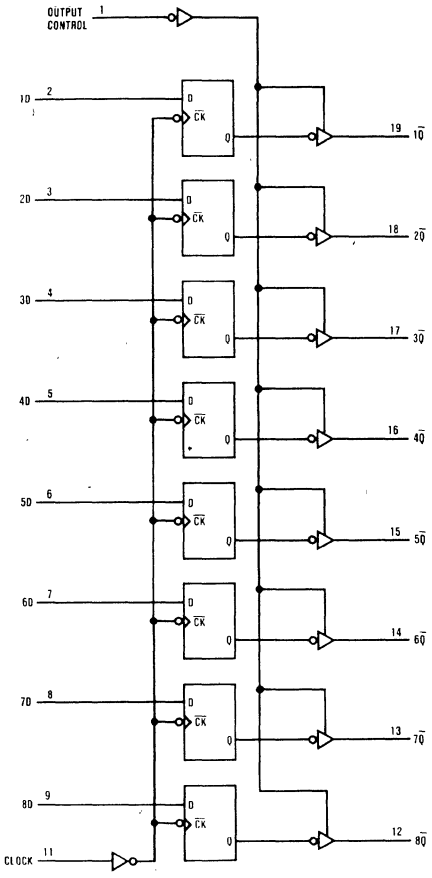
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS576			DM74AS576			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any $\overline{Q}$		3		11	3		8	ns
T_{PHL}				4		11	4		9	ns
T_{PZH}	Output Control	Any $\overline{Q}$		2		7	2		6	ns
T_{PZL}				3		11	3		10	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6316-2

Function Table

Output Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54AS577/DM74AS577 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs and Synchronous Preset

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS577 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the $\overline{D}$ inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

When the $\overline{CLR}$ is held on during a positive transition of the clock the $\overline{Q}$ outputs of the flip-flops with go high.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Synchronous Preset

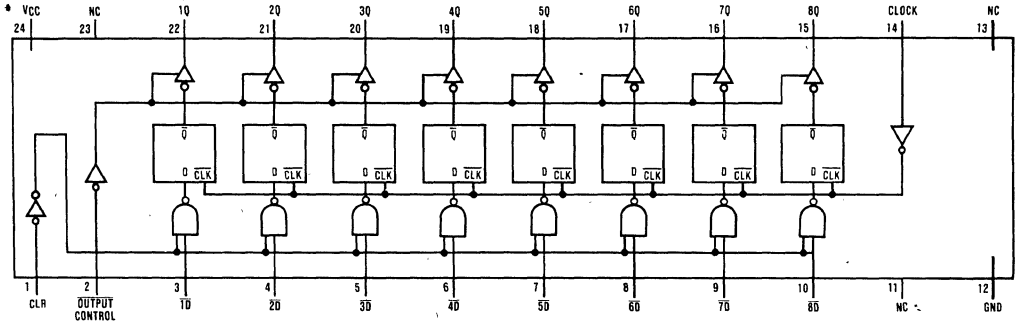
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS577	−55°C to 125°C
DM74AS577	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6317-1

54AS576 (J) 74AS576 (J,N)

Recommended Operating Conditions

Parameter		DM54AS577			DM74AS577			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5			4			ns
	Low	3			2			ns
Data Setup Time, T_{SU}	Data	3↑			2↑			ns
	$\overline{CLR}$	6.5↑			5.5↑			ns
Data Hold Time, T_H	Data	3↑			2↑			ns
	$\overline{CLR}$	0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

3

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		V_{CC} −2			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		78	126	mA
			Outputs Low		76	123	
			Outputs Disabled		88	142	

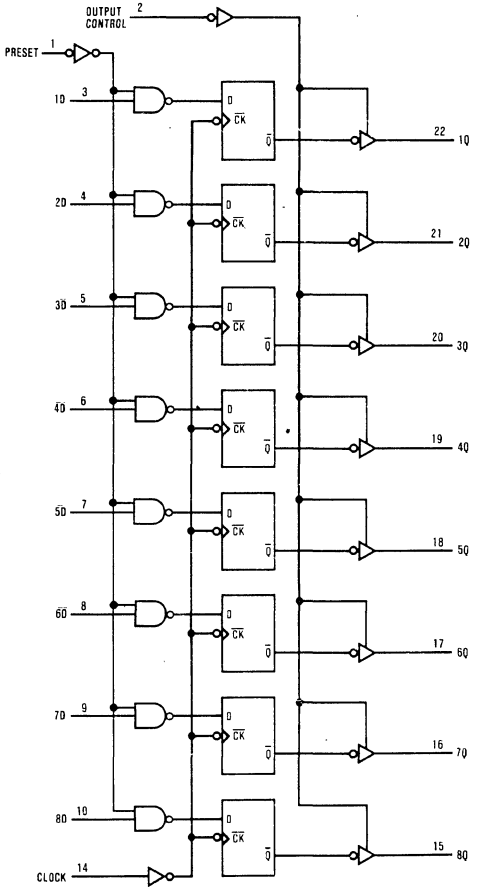
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS577			DM74AS577			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any $\overline{Q}$		3		11	3		8	ns
T_{PHL}				4		11	4		9	ns
T_{PZH}	Output Control	Any $\overline{Q}$		2		7	2		6	ns
T_{PZL}				3		11	3		10	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6317-2

Function Table

$\overline{\text{Output}}$ Control	CLR	Clock	$\overline{D}$	Output $\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

3

National Semiconductor

DM54AS580/DM74AS580 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS580 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.

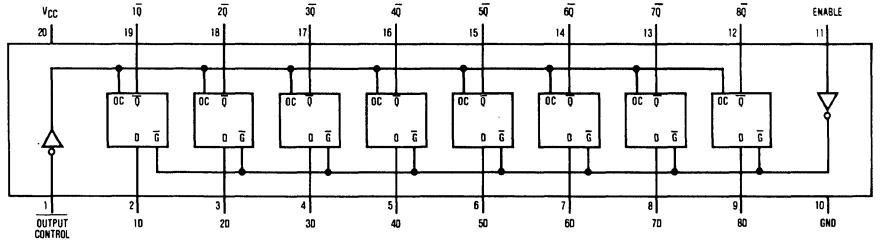
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS580	−55°C to 125°C
DM74AS580	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6318-1

54AS580 (J) 74AS580 (J,N)

Recommended Operating Conditions

Parameter	DM54AS580			DM74AS580			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High or Low	3			2			ns
Data Setup Time, T_{SU}	2			2			ns
Data Hold Time, T_H	3			3			ns

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} -2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		62	100	mA
			Outputs Low		65	106	
			Outputs Disabled		71	115	

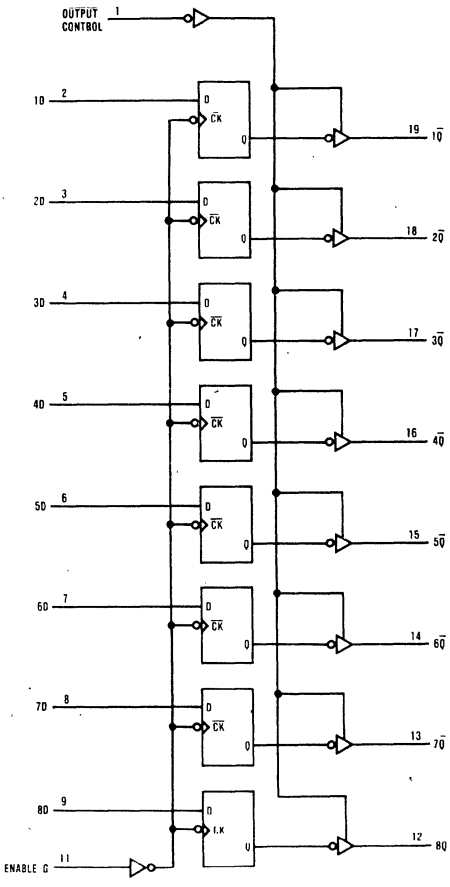
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS580			DM74AS580			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\bar{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		10	3		7.5	ns
T_{PHL}				3		7.5	3		7	ns
T_{PLH}	Enable	Any $\bar{Q}$		5		12	5		9	ns
T_{PHL}				4		8.5	4		8	ns
T_{PZH}	Output Control	Any $\bar{Q}$		2		7.5	2		6.5	ns
T_{PZL}				4		10.5	4		9.5	ns
T_{PHZ}				2		7.5	2		6.5	ns
T_{PLZ}				2		8	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6318-2

Function Table

Output Control	Enable G	D	Output $\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\bar{Q}_0$ = Previous Condition of $\bar{Q}$

National Semiconductor

DM54AS620/DM74AS620, DM54AS621/DM74AS621, DM54AS622/DM74AS622, DM54AS623/DM74AS623 Octal Bus Transceivers

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the octal bus transceivers the capability of storing data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the AS621 and AS623, or complementary for the AS620 and AS622.

Features

- Local bus-latch capability
- Choice of true or inverting logic
- Choice of TRI-STATE® or open-collector outputs

Device	Output	Logic
AS620	TRI-STATE	Inverting
AS621	Open-Collector	True
AS622	Open-Collector	Inverting
AS623	TRI-STATE	True

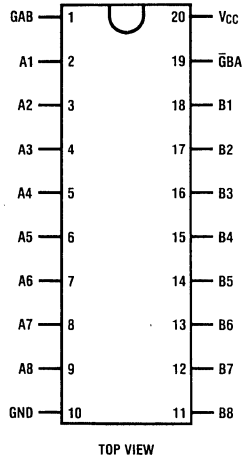
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage (I/O ports for AS620, AS623)	5.5V
Input Voltage (all other inputs)	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



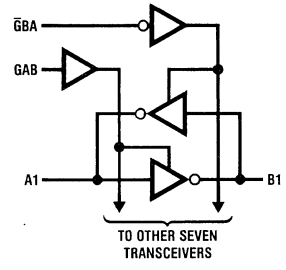
TOP VIEW

TL/F/6319-1

DM54AS620 (J) DM74AS620 (J, N)
DM54AS621 (J) DM74AS621 (J, N)
DM54AS622 (J) DM74AS622 (J, N)
DM54AS623 (J) DM74AS623 (J, N)

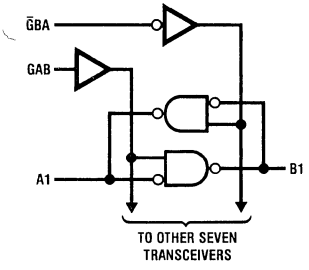
Logic Diagrams

AS620



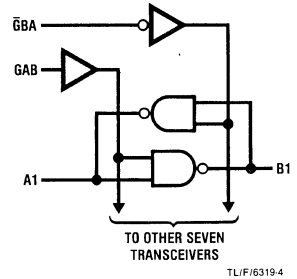
TL/F/6319-2

AS621



TL/F/6319-3

AS622



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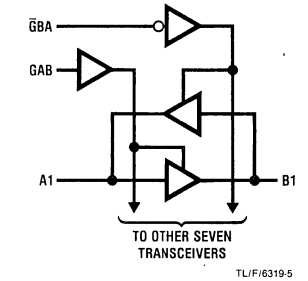
AS623



TL/F/6319-5

Function Table

Enable Inputs		Operation	
$\overline{G}BA$	GAB	AS620, AS622	AS621, AS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

Recommended Operating Conditions

Symbol	Parameter	DM54AS620 DM54AS623			DM74AS620 DM74AS623			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	DM54AS620 DM54AS623			DM74AS620 DM74AS623			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Output High Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V, I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5V, I_{OH} = −12 mA	2						
		V_{CC} = 4.5V, I_{OH} = −15 mA				2			
V_{OL}	Output Low Voltage	V_{CC} = 4.5V, I_{OL} = Max		0.3	0.55		0.35	0.55	V
I_I	Control Inputs	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
	A or B Ports	V_{CC} = 5.5V, V_I = 5.5V			0.1			0.1	
I_{IH}	Control Inputs	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
	A or B Ports (Note 3)				70			70	
I_{IL}	Control Inputs	V_{CC} = 5.5V, V_I = 0.4V			−0.5			−0.5	mA
	A or B Ports (Note 3)				−0.75			−0.75	

Electrical Characteristics (Continued) over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM54AS620 DM54AS623			DM74AS620 DM74AS623			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
I_O (Note 2)		V_{CC} = 5.5V, V_O = 2.25V		−50		−150	−50		−150	mA
I_{CC}	AS620	V_{CC} = 5.5V	Outputs High		35	57		35	57	mA
			Outputs Low		74	122		74	122	
			Outputs Disabled		48	77		48	77	
	AS623	V_{CC} = 5.5V	Outputs High		58	93		58	93	
			Outputs Low		116	189		116	189	
			Outputs Disabled		72	116		72	116	

AS620 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS620			DM74AS620			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	1		8	1		7	ns
t_{PHL}				2		7	2		6	ns
t_{PLH}	B	A		1		8	1		7	ns
t_{PHL}				2		7	2		6	ns
t_{PZH}	$\overline{G}$BA	A		2		8.5	2		8	ns
t_{PZL}				2		10	2		9	ns
t_{PHZ}	$\overline{G}$BA	A		1		7.5	1		6	ns
t_{PLZ}				2		15	2		12	ns
t_{PZH}	GAB	B		2		9	2		8	ns
t_{PZL}				2		10.5	2		9	ns
t_{PHZ}	GAB	B		1		6.5	1		6	ns
t_{PLZ}				2		16	2		13	ns

AS623 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS623			DM74AS623			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	1		10	1		9	ns
t_{PHL}				1		9	1		8	ns
t_{PLH}	B	A		1		10	1		9	ns
t_{PHL}				1		9.5	1		8.5	ns
t_{PZH}	$\overline{G}$BA	A		2		11.5	2		11	ns
t_{PZL}				2		11	2		10	ns
t_{PHZ}	$\overline{G}$BA	A		1		8.5	1		7.5	ns
t_{PLZ}				1		13.5	1		11.5	ns
t_{PZH}	GAB	B		2		13	2		11.5	ns
t_{PZL}				2		12	2		11	ns
t_{PHZ}	GAB	B		1		8	1		7	ns
t_{PLZ}				1		10.5	1		9	ns

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

Recommended Operating Conditions

Symbol	Parameter	DM54AS621 DM54AS622			DM74AS621 DM74AS622			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			48			64	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM54AS621 DM54AS622			DM74AS621 DM74AS622			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
I_{OH}	Output High Voltage	V_{CC} = 4.5V, V_{OH} = 5.5V				0.1			0.1	mA
V_{OL}	Output Low Voltage	V_{CC} = 4.5V, I_{OL} = Max				0.5			0.5	V
I_I	Control Inputs	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
	A or B Ports	V_{CC} = 5.5V, V_I = 5.5V				0.1			0.1	
I_{IH}	Control Inputs	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
	A or B Ports (Note 2)					70			70	
I_{IL}	Control Inputs	V_{CC} = 5.5V, V_I = 0.4V				−0.5			−0.5	mA
	A or B Ports (Note 2)					−0.75			−0.75	
I_{CC}	AS621	V_{CC} = 5.5V	Outputs High		48	79		48	79	mA
			Outputs Low		100	189		100	189	
	AS622	V_{CC} = 5.5V	Outputs High		25	39		25	39	mA
			Outputs Low		62	103		62	103	

AS621 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS621			DM74AS621			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 680Ω, T_A = Min to Max	5		28.5	5		24	ns
t_{PHL}				1		8.5	1		7.5	ns
t_{PLH}	B	A		5		23	5		21	ns
t_{PHL}				1		8.5	1		7.5	ns
t_{PLH}	$\overline{G}$BA	A		5		24	5		21	ns
t_{PHL}				1		10	1		9	ns
t_{PLH}	GAB	B		5		26	5		22	ns
t_{PHL}				1		11	1		10	ns

AS622 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS622			DM74AS622			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 680Ω, T_A = Min to Max	5		28.5	5		24.5	ns
t_{PHL}				1		8.5	1		8	ns
t_{PLH}	B	A		5		30	5		25	ns
t_{PHL}				1		8.5	1		8	ns
t_{PLH}	$\overline{G}$BA	A		5		26	5		22	ns
t_{PHL}				1		11.5	1		10	ns
t_{PLH}	GAB	B		5		26	5		23	ns
t_{PHL}				1		11.5	1		10.5	ns

Note 1: All typicals are at V_{CC} = 5.0V, T_A = 25°C.

Note 2: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

National Semiconductor

DM54AS638/DM74AS638, DM54AS639/DM74AS639 Octal Bus Transceivers

General Description

These octal bus transceivers are designed for asynchronous two-way communications between open-collector and TRI-STATE® buses. The devices transmit data from the A bus (open-collector) to the B bus (TRI-STATE) or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

Device	A Output	B Output	Logic
DM54/74ALS638	Open-Collector	TRI-STATE	Inverting
DM54/74ALS639	Open-Collector	TRI-STATE	True

Features

- Bidirectional bus transceivers in high-density 20-pin packages
- Choice of true or inverting logic
- A bus outputs are open-collector; B bus outputs are TRI-STATE

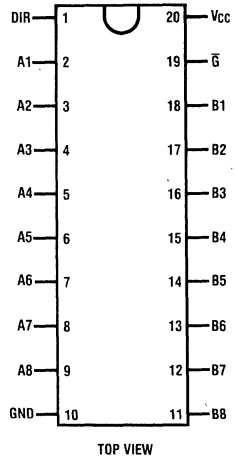
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
A Bus I/O Ports	7V
B Bus I/O Ports	5.5V
Other Inputs	7V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

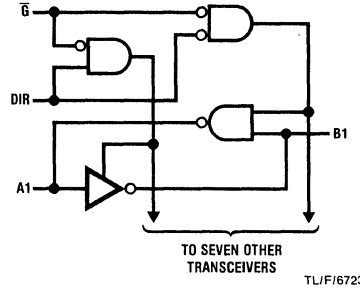
TL/F/6723-1

Function Table

Control Inputs		Operation	
$\overline{G}$	DIR	DM54/74ALS638	DM54/74ALS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

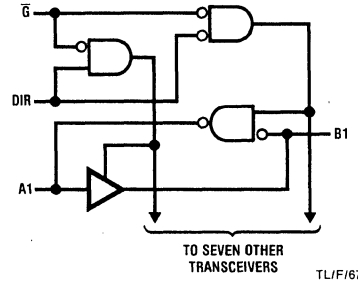
Logic Diagrams

DM54/74AS638



TL/F/6723-2

DM54/74AS639



TL/F/6723-3

Recommended Operating Conditions

Symbol	Parameter		DM54AS638 DM54AS639			DM74AS638 DM74AS639			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
V_{OH}	High Level Output Voltage	A Ports			5.5			5.5	V
I_{OH}	High Level Output Current	B Ports			−12			−15	mA
I_{OL}	Low Level Output Current	A or B Ports			48			64	mA
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

Symbol	Parameter	Conditions		DM54AS638 DM54AS639			DM74AS638 DM74AS639			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
I_{OH}	A Ports	V_{CC} = 4.5V, V_{OH} = 5.5V				0.1			0.1	mA
V_{OH}	B Ports	V_{CC} = 4.5V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max		2			2			
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V_{CC} − 2			
V_{OL}	A or B Ports	V_{CC} = 4.5V, I_{OL} = Max			0.25	55		0.35	55	V
I_I	Control Inputs	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
	A or B Ports	V_{CC} = 5.5V, V_I = 5.5V				0.1			0.1	
I_{IH}	Control Inputs	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
	A or B Ports					70			70	
I_{IL}	Control Inputs	V_{CC} = 5.5V, V_I = 0.4V				−0.5			−0.5	mA
	A or B Ports					−0.75			−0.75	
I_O (Note 2)	B Ports	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	−50		−150	mA
I_{CC}	DM54/74ALS638	V_{CC} = 5.5V	Outputs High		24	40		24	40	mA
			Outputs Low		75	122		75	122	
			Outputs Disabled		37	61		37	61	
	DM54/74ALS639		Outputs High		56	92		56	92	mA
			Outputs Low		95	154		95	154	
			Outputs Disabled		62	100		62	100	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

DM54/74AS638 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS638		DM74AS638		Units
				Min	Max	Min	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω (A Outputs), R1 = R2 = 500Ω (B Outputs), T_A = Min to Max	2	8	2	7	ns
t_{PHL}				2	7.5	2	6.5	ns
t_{PLH}	B	A		5	23	5	20	ns
t_{PHL}				2	8	2	7	ns
t_{PLH}	$\overline{G}$	A		5	20	5	19	ns
t_{PHL}				2	10	2	9	ns
t_{PZH}	$\overline{G}$	B		2	10	2	8	ns
t_{PZL}				2	12	2	10	ns
t_{PHZ}	$\overline{G}$	B		2	8	2	7	ns
t_{PLZ}				2	12	2	10	ns

DM54/74AS639 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS639		DM74AS639		Units
				Min	Max	Min	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω (A Outputs), R1 = R2 = 500Ω (B Outputs), T_A = Min to Max	2	11	2	9.5	ns
t_{PHL}				2	10.5	2	9	ns
t_{PLH}	B	A		5	25	5	22	ns
t_{PHL}				2	10	2	9	ns
t_{PLH}	$\overline{G}$	A		5	23	5	21.5	ns
t_{PHL}				2	12.5	2	11.5	ns
t_{PZH}	$\overline{G}$	B		2	12	2	10.5	ns
t_{PZL}				2	12	2	10.5	ns
t_{PHZ}	$\overline{G}$	B		2	7.5	2	7	ns
t_{PLZ}				2	12	2	10.5	ns

National Semiconductor

DM54/74AS640, DM54/74AS641, DM54/74AS642, DM54/74AS643, DM54/74AS644, DM54/74AS645 TRI-STATE® Octal Bus Transceiver

General Description

This family of advanced Schottky devices contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bi-directional data buses. These devices transmit data from the A bus to the B bus, or vice versa, depending upon the logic level of the direction control input (DIR). The enable input ($\overline{G}$) can be used to disable the devices, effecting isolation of buses A and B.

The TRI-STATE circuitry also contains a protection feature that prevents these transceivers from glitching the bus during power-up or power-down.

The DM54/74AS640, 643 and 645 have TRI-STATE outputs, while the DM54/74AS641, 642 and 644 feature open-collector outputs.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance drive to drive terminated transmission lines to 133Ω
- Choice of true or inverting logic
- Choice of TRI-STATE or open-collector outputs
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- Extended drive current for DM74ALS

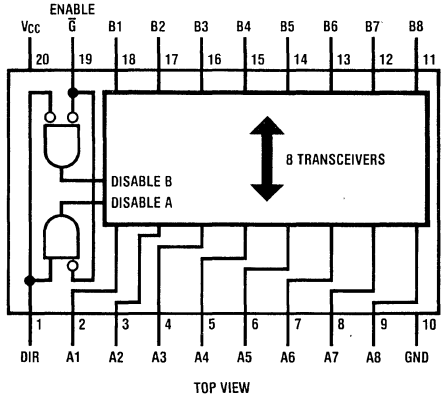
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free-Air Temperature Range	
DM54AS	−55°C to +125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6708-1

DM54AS640 thru 645 (J) DM745AS640 thru 645 (J, N)

Function Table

Control Inputs		Operation		
$\overline{G}$	DIR	'AS640 'AS642	'AS641 'AS645	'AS643 'AS644
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus	B Data to A Bus
L	H	$\overline{A}$ Data to B Bus	A Data to B Bus	$\overline{A}$ Data to B Bus
H	X	Isolation	Isolation	Isolation

Circuit Configurations

Device	Output Type	Logic
DM54/74AS640	TRI-STATE	Inverting
DM54/74AS641	Open-Collector	True
DM54/74AS642	Open-Collector	Inverting
DM54/74AS643	TRI-STATE	True from B to A Inverting from A to B
DM54/74AS644	Open-Collector	True from B to A Inverting from A to B
DM54/74AS645	TRI-STATE	True

Recommended Operating Conditions

Symbol	Parameter	DM54AS			DM74AS			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current (AS640, 643, 645 Only)			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA
T_A	Free-Air Operating Temperature	−55		125	0		70	°C

DM54/74AS640, 643 and 645 Electrical Characteristics

over recommended operating free-air temperature unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = Max			2.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V, (V_I = 5.5V for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max (Note 2)				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max (Note 2)				−50	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V	DM54	−50		−150	mA
			DM74	−50		−150	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	'AS640		37	58	mA
I_{CCL}	Supply Current with Outputs Low				78	123	mA
I_{CCZ}	Supply Current with Outputs in TRI-STATE				51	80	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	'AS643		48	79	mA
I_{CCL}	Supply Current with Outputs Low				88	143	mA
I_{CCZ}	Supply Current with Outputs in TRI-STATE				61	100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	'AS645		62	97	mA
I_{CCL}	Supply Current with Outputs Low				95	149	mA
I_{CC}	Supply Current with Outputs in TRI-STATE				79	123	mA

Note 1: All typicals are at V_{CC} = 5.0V, T_A = 25°C.
Note 2: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

DM54/74AS641, 642 and 644 Electrical Characteristics

over recommended operating free-air temperature unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	'AS641		50	82	mA
I_{CCL}	Supply Current with Outputs Low				84	36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	'AS642		25	42	mA
I_{CCL}	Supply Currents with Outputs Low				64	104	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	'AS644		38	62	mA
I_{CCL}	Supply Current with Outputs Low				76	124	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics over recommended operating free-air temperature unless otherwise noted

Symbol	Parameter	From (Input) To (Output)	V_{CC} = Min to Max, C_L = 50 pF, R_L = 500Ω						Units
			DM54AS			DM74AS			
			Min	Typ	Max	Min	Typ	Max	
DM54/74AS640									
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	2		8	2		7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	2		7	2		6	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$ to A or B	2		10	2		8	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$ to A or B	2		12	2		10	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$ to A or B	2		9	2		8	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$ to A or B	2		16	2		13	ns
DM54/74AS641									
t_{PLH}	Propagation Delay Time Low to High Level Output	DIR to A or B	5		26	5		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	DIR to A or B	1		11	1		10	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	5		23	5		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	1		8.5	1		7.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{G}$ or DIR to A or B	5		26	5		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{G}$ or DIR to A or B	1		11	1		10	ns

Switching Characteristics (Continued)

over recommended operating free-air temperature unless otherwise noted

Symbol	Parameter	From (Input) To (Output)	V_{CC} = Min to Max, C_L = 50 pF, R_L = 500Ω						Units
			DM54AS			DM74AS			
			Min	Typ	Max	Min	Typ	Max	
DM54/74AS642									
t_{PLH}	Propagation Delay Time Low to High Level Output	DIR to A or B	5		26.5	5		23.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	DIR to A or B	1		12.5	1		11.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	5		28.5	5		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	1		8.5	1		7.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{G}$ or DIR to A or B	5		25	5		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{G}$ or DIR to A or B	1		11	1		10	ns
DM54/74AS643									
t_{PLH}	Propagation Delay Time Low to High Level Output	A to B	2		10	2		8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to B	2		7.5	2		7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to A	2		11.5	2		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to A	2		10	2		9	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$ to A	2		13	2		11	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$ to A	2		13	2		11	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$ to A	2		8.5	2		7.5	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$ to A	2		12	2		10.5	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$ to A	2		11.5	2		10	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$ to A	2		12	2		10	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$ to B	2		8	2		7	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$ to B	2		12	2		10	ns
DM54/74AS644									
t_{PLH}	Propagation Delay Time Low to High Level Output	A to B	5		28.5	5		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to B	1		8.5	1		7.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to A	5		23	5		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to A	1		8.5	1		7.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{G}$ to A	5		24	5		21	ns

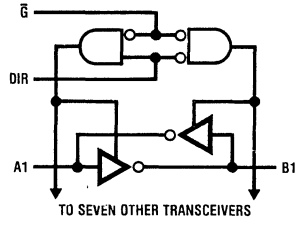
Switching Characteristics (Continued)

over recommended operating free-air temperature unless otherwise noted

Symbol	Parameter	From (Input) To (Output)	V_{CC} = Min to Max, C_L = 50 pF, R_L = 500Ω						Units
			DM54AS			DM74AS			
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{G}$ to A	1		10	1		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	DIR to A or B	5		26	5		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	DIR to A or B	1		11	1		10	ns
DM54/74AS645									
t_{PLH}	Propagation Delay Time Low to High Level Output	B to A	2		11	2		9.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to A	2		10.5	2		9	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$ to A or B	2		12	2		11	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$ to A or B	2		12	2		11	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$ to A or B	2		8	2		7	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$ to A or B	2		13	2		12	ns

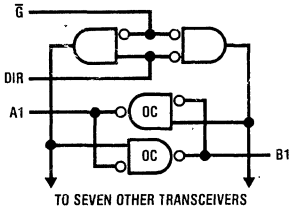
Logic Diagrams

DM54/74AS640



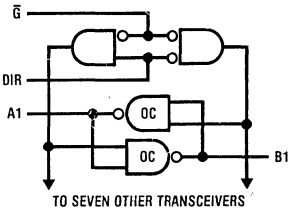
TL/F/6708-2

DM54/74AS641



TL/F/6708-3

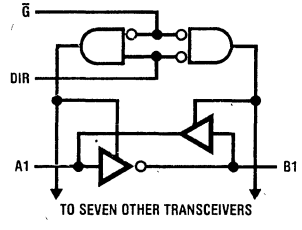
DM54/74AS642



TL/F/6708-4

OC denotes open-collector outputs

DM54/74AS643



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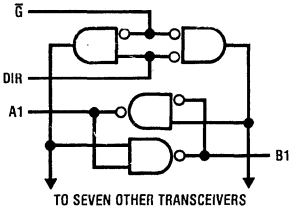
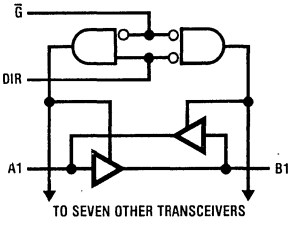
DM54/74AS644



TL/F/6708-6

DM54/74AS645



TL/F/6708-7

National Semiconductor

PRELIMINARY

DM54AS646,648/DM74AS646,648 Octal Bus Transceivers and Registers

General Description

These devices incorporate an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

These bus transceivers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS646,648 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data, and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable $\overline{G}$ and direction control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal store data transfer to bus A or B.

When the enable $\overline{G}$ pin is low, the direction pin selects which bus receives data. When the enable $\overline{G}$ pin is high, both buses become disabled yet their input function is still enabled.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

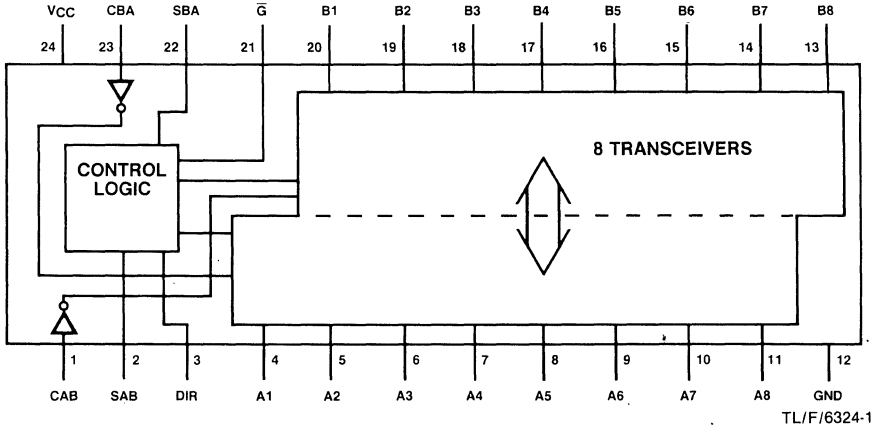
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS646,648	−55°C to 125°C
DM74AS646,648	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package

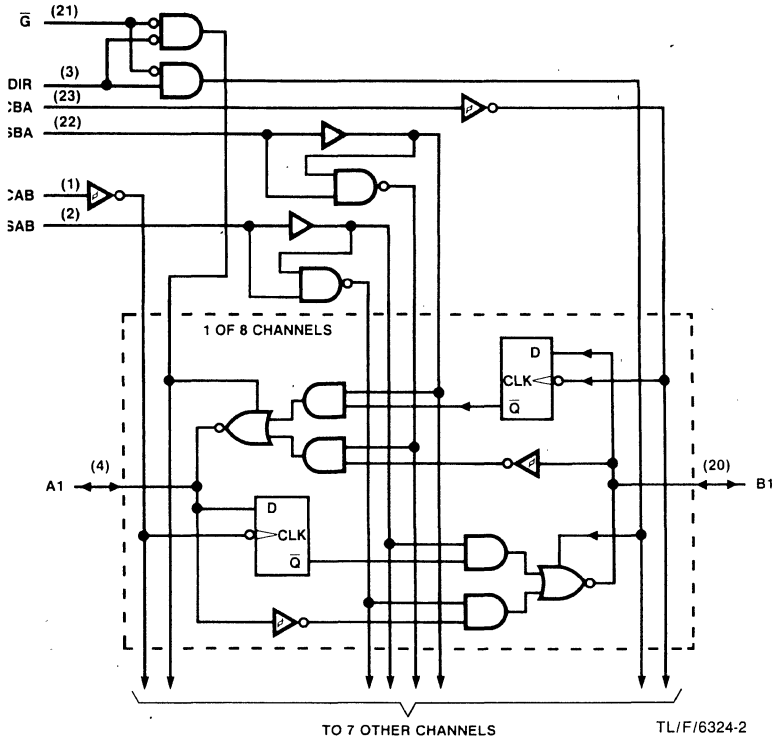


TL/F/6324-1

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

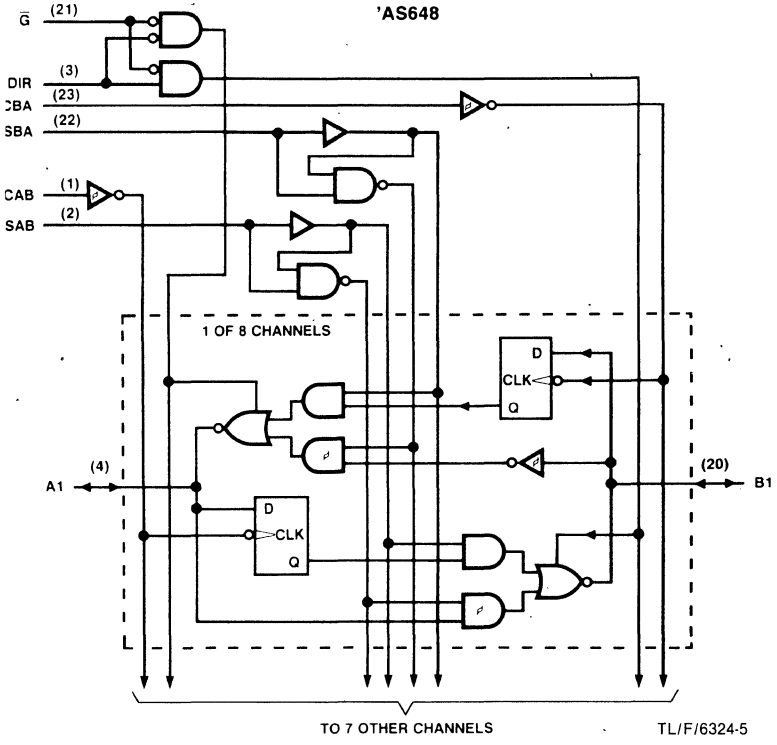
Block Diagram (positive logic)

'AS646



TL/F/6324-2

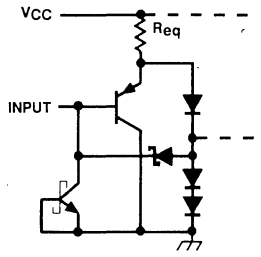
'AS648



TL/F/6324-5

Schematics of Inputs and Outputs

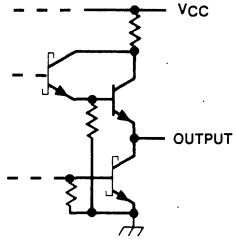
EQUIVALENT OF ALL OTHER INPUTS



A and B: R_{eq} - 10 kΩ NOM
CAB and CBA: R_{eq} - 10 k NOM
ALL OTHER: 5 kΩNOM

TL/F/6324-3

TYPICAL OF ALL 'AS646, 'AS648 OUTPUTS



TL/F/6324-4

Recommended Operating Conditions

Parameter		DM54AS646,648			DM74AS646,648			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		75	0		90	MHz
Width of Clock Pulse, T_W	High	6			5			ns
	Low	7			6			ns
Data Setup Time, T_{SU}		7↑			6↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$					−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX, V_{IH} = V_{IH} MIN		I_{OH} = MAX	2			V
				$I_{OH} = -3mA$	2.4	3.2		
				$I_{OH} = -2mA$	V_{CC} −2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, V_{IL} = V_{IL} MIN		I_{OL} = MAX		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V	$V_I = 7V$	Control Inputs			0.1	mA
			$V_I = 5.5V$	A or B Ports			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, $V_{IH} = 2.7V$		Control Inputs			20	μA
				A or B Ports			70	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		Control Inputs			−0.5	mA
				A or B Ports			−0.75	
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$			−30		−112	mA

Electrical Characteristics (Continued) over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{CC}	Supply Current	V_{CC} = 5.5V	'AS646	Outputs High		120	195	mA
				Outputs Low		130	211	
				Outputs Disabled		130	211	
			'AS648	Outputs Low		120	195	
				Outputs High		110	185	
				Outputs Disabled		120	195	

AS646 Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	To (Output)	Conditions	DM54AS646			DM74AS646			Unit
				Min	Typ	Max	Min	Typ	Max	
f_{MAX}				75			90			MHz
t_{PLH}	Clock	Bus	R_L = 500 Ω, C_L = 50pF. See Note 1	2		9.5	2		8.5	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Bus	Bus		2		11	2		9	ns
t_{PHL}				1		8	1		7	ns
t_{PLH}	Select, with bus input high	Bus		2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Select, with bus input low			2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PZH}	Enable $\overline{G}$	Bus		2		10	2		9	ns
t_{PZL}				3		15	3		14	ns
t_{PHZ}				2		11	2		9	ns
t_{PLZ}				2		11	2		9	ns
t_{PZH}	Direction DIR	Bus		3		20	3		18	ns
t_{PZL}				3		22	3		20	ns
t_{PHZ}				2		12	2		10	ns
t_{PLZ}				2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

'AS648 Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	To (Output)	Conditions	DM54AS648			DM74AS648			Unit
				Min	Typ	Max	Min	Typ	Max	
f_{MAX}				75			90			MHz
t_{PLH}	Clock	Bus	$R_L = 500\ \Omega$, $C_L = 50pF$. See Note 1	2		9.5	2		8.5	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Bus	Bus		2		9	2		8	ns
t_{PHL}				1		8	1		7	ns
t_{PLH}	Select, with bus input high	Bus		2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Select, with bus input low			2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PZH}	Enable $\overline{G}$	Bus		2		10	2		9	ns
t_{PZL}				3		18	3		15	ns
t_{PHZ}				2		11	2		9	ns
t_{PLZ}				2		11	2		9	ns
t_{PZH}	Direction DIR	Bus		3		20	3		18	ns
t_{PZL}				3		22	3		20	ns
t_{PHZ}				2		12	2		10	ns
t_{PLZ}				2		12	2		10	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS646	'AS648
H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data B Bus

H — high level; L — low level; X — irrelevant; ↑ — low-to-high level transition

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

National Semiconductor

DM54AS651,652/DM74AS651,652 Octal Bus Transceivers and Registers

General Description

These devices incorporate an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

These bus transceivers feature totem-pole TRI-STATE output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS651,652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The Enable (GAB and $\overline{GBA}$) control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

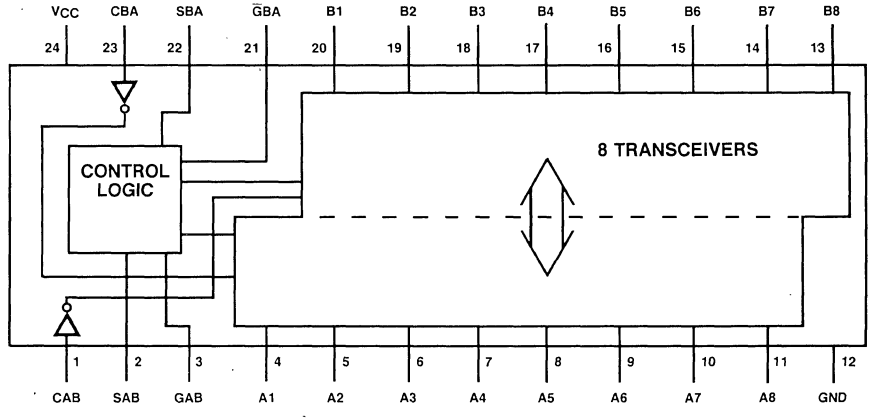
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS651,652	−55°C to 125°C
DM74AS651,652	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

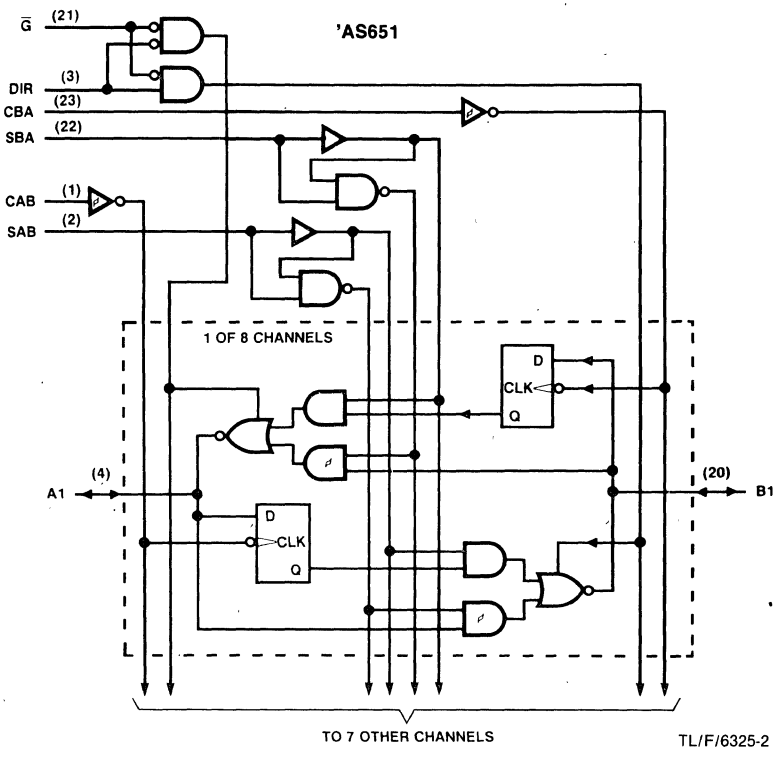
Connection Diagram

Dual-In-Line Package

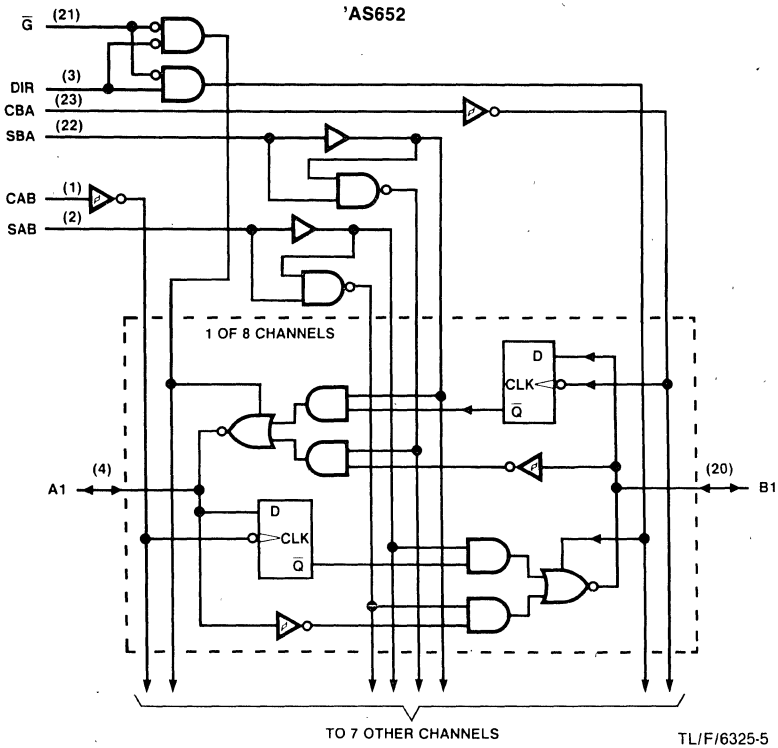


TL/F/6325-1

Block Diagram (positive logic)



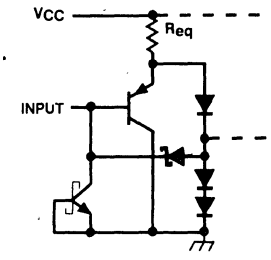
TL/F/6325-2



TL/F/6325-5

Schematics of Inputs and Outputs

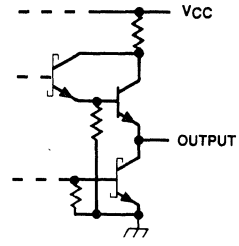
EQUIVALENT OF ALL OTHER INPUTS



A and B: R_{eq} - 10 kΩ NOM
CAB and CBA: R_{eq} - 10 k NOM
ALL OTHER: 5 kΩNOM

TL/F/6325-3

TYPICAL OF ALL 'AS651, 'AS652 OUTPUTS



TL/F/6325-4

Recommended Operating Conditions

Parameter		DM54AS651,652			DM74AS651,652			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		75	0		90	MHz
Width of Clock Pulse, T_W	High	6			5			ns
	Low	7			6			ns
Data Setup Time, T_{SU}		7			6			ns
Data Hold Time, T_H		0			0			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$					−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX $V_{IH} = V_{IH}$ MIN		I_{OH} = MAX	2			V
				$I_{OH} = -3mA$	2.4	3.2		
				$I_{OH} = -2mA$	$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$ $V_{IL} = V_{IL}$ MIN		I_{OL} = MAX		0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$	$V_I = 7V$	Control Inputs			0.1	mA
			$V_I = 5.5V$	A or B Ports			0.1	
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$		Control Inputs			20	μA
				A or B Ports			70	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		Control Inputs			−0.5	mA
				A or B Ports			−0.75	
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$			−30		−112	mA

Electrical Characteristics (Continued) over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{CC}	Supply Current	V_{CC} = 5.5V	'AS651	Outputs High		110	185	mA
				Outputs Low		120	195	
				Outputs Disabled		130	195	
			'AS652	Outputs Low		120	195	
				Outputs High		130	211	
				Outputs Disabled		130	211	

'AS651 Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	To (Output)	Conditions	DM54AS651			DM74AS651			Unit
				Min	Typ	Max	Min	Typ	Max	
f_{MAX}			R_L = 500 Ω, C_L = 50pF. See Note 1	75			90			MHz
t_{PLH}	Clock	Bus		2		9.5	2		8.5	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Bus	Bus		2		9	2		8	ns
t_{PHL}				1		8	1		7	ns
t_{PLH}	Select, with bus input high	Bus		2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Select, with bus input low			2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PZH}	Enable $\overline{G}$BA	A Bus		2		11	2		10	ns
t_{PZL}				3		18	3		16	ns
t_{PHZ}				2		10	2		9	ns
t_{PLZ}				2		10	2		9	ns
t_{PZH}	Enable GAB	B Bus		3		12	3		11	ns
t_{PZL}				3		20	3		16	ns
t_{PHZ}				2		11	2		10	ns
t_{PLZ}				2		12	2		11	ns

'AS652 Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From (Input)	To (Output)	Conditions	DM54AS652			DM74AS652			Unit
				Min	Typ	Max	Min	Typ	Max	
f_{MAX}				75			90			MHz
t_{PLH}	Clock	Bus	$R_L = 500\ \Omega$, $C_L = 50pF$. See Note 1	2		9.5	2		8.5	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Bus	Bus		2		11	2		9	ns
t_{PHL}				1		8	1		7	ns
t_{PLH}	Select, with bus input high	Bus		2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PLH}	Select, with bus input low			2		12	2		11	ns
t_{PHL}				2		10	2		9	ns
t_{PZH}	Enable $\overline{G}BA$	A Bus		2		11	2		10	ns
t_{PZL}				3		18	3		16	ns
t_{PHZ}				2		10	2		9	ns
t_{PLZ}				2		10	2		9	ns
t_{PZH}	Enable GAB	B Bus		3		12	3		11	ns
t_{PZL}				3		20	3		16	ns
t_{PHZ}				2		11	2		10	ns
t_{PLZ}				2		12	2		11	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{G}BA$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS651	'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus & Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus & Stored B Data to A Bus

H — high level L — low level X — irrevelant ↑ — low-to-high-level transition

*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

National Semiconductor

DM54AS804B/DM74AS804B Hex 2-Input NAND Drivers

General Description

These devices contain six independent drivers, each of which performs the logic NAND function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power Schottky TTL Counterpart.

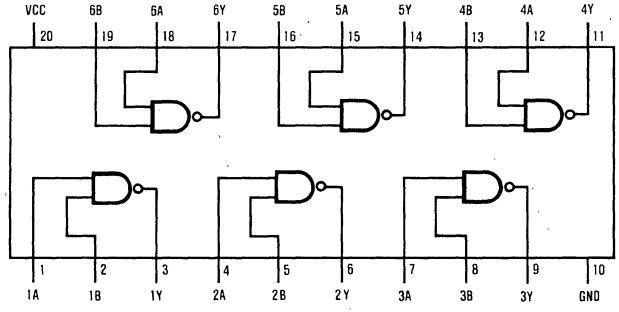
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6326-1

54AS804B (J) **74AS804B (J, N)**

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54AS804B			DM74AS804B			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			
		I_{OH} = MAX, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX V_{IH} = 2V			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.5	4	mA
			Outputs Low		16	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS804B			DM74AS804B			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		4.5	1		3.5	ns
T_{PHL}, Propagation delay time. High to low level output		1		4.5	1		3.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS805B/DM74AS805B Hex 2-Input NOR Drivers

General Description

These devices contain six independent drivers, each of which performs the logic NOR function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power Schottky TTL Counterpart.

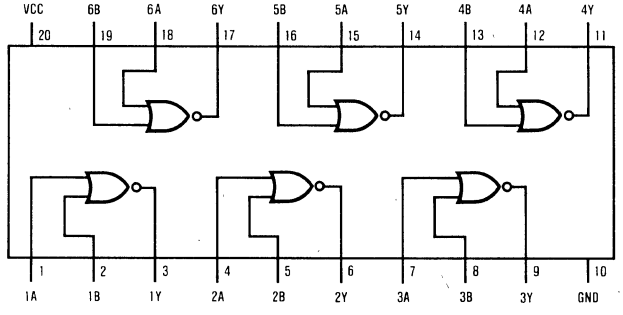
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6327-1

54AS805B (J) **74AS805B (J, N)**

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54AS805B			DM74AS805B			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			
		I_{OH} = MAX, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		5	9	mA
			Outputs Low		18	32	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS805B			DM74AS805B			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		4.5	1		4	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		4.5	1		4	ns

Note 1: See Section 1 for test waveforms and output load.

3

National Semiconductor

DM54AS808B/DM74AS808B Hex 2-Input AND Drivers

General Description

These devices contain six independent drivers, each of which performs the logic AND function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power Schottky TTL Counterpart.

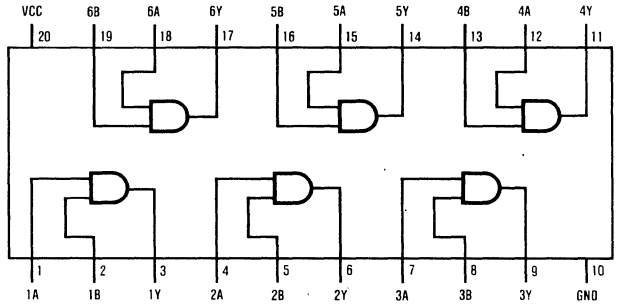
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6328-1

54AS808B (J) **74AS808B (J, N)**

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54AS808B			DM74AS808B			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			
		I_{OH} = MAX, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		6.5	11	mA
			Outputs Low		19	32	

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS808B			DM74AS808B			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		6	1		5	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		6	1		5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

PRELIMINARY

DM54AS810/DM74AS810 Quad 2-Input Exclusive-NOR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

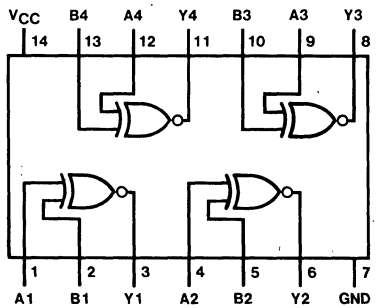
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6724-1

DM54AS810 (J) DM74AS810 (J, N)

Function Table

$\overline{Y} = A \oplus B$

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54AS810			DM74AS810			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = Max, V_{IH} = Min, V_{IL} = Max	DM54	V_{CC} − 2V	3.4		V
			DM74	V_{CC} − 2V	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.35	0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−0.5	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)					mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 2)					mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CCL} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 3: I_{CCH} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics over recommended operating free air temperature range

Parameter	Conditions	DM54AS810			DM74AS810			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF							ns
t_{PHL} Propagation Delay Time High to Low Level Output								ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF							ns
t_{PHL} Propagation Delay Time High to Low Level Output								ns

National Semiconductor

PRELIMINARY

DM54AS811/DM74AS811 Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic exclusive-NOR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{max} = \frac{V_{CC\,(min)} - V_{OH}}{N1\,(I_{OH}) + N2\,(I_{IH})}$$

$$R_{min} = \frac{V_{CC\,(max)} - V_{OL}}{I_{OL} - N3\,(I_{IL})}$$

Where $N1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

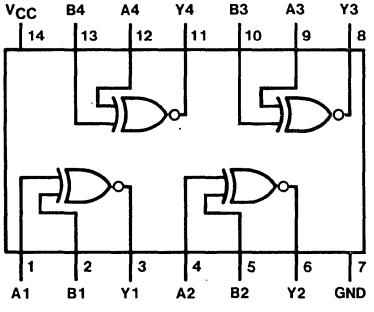
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6725-1

DM54AS811 (J) DM74AS811 (J, N)

Function Table

$$\overline{Y} = A \oplus B$$

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54AS811			DM74AS811			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.35	0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)				mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 2)				mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CCL} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 3: I_{CCH} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics over recommended operating free air temperature range

Parameter	Conditions	DM54AS811			DM74AS811			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF							ns
t_{PHL} Propagation Delay Time High to Low Level Output								ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF							ns
t_{PHL} Propagation Delay Time High to Low Level Output								ns

National Semiconductor

DM54AS832B/DM74AS832B Hex 2-Input OR Drivers

General Description

These devices contain six independent drivers, each of which performs the logic OR function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

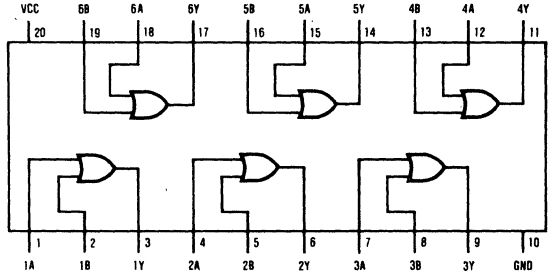
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6329-1

54AS832B (J) **74AS832B (J, N)**

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54AS832B			DM74AS832B			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA, V_{CC} = 4.5V		2.4			
		I_{OH} = MAX, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		9	17	mA
			Outputs Low		22	36	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS832B			DM74AS832B			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		7	1		5.5	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		6.5	1		5.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

PRELIMINARY

DM54AS841/DM74AS841, DM54AS842/DM74AS842 10-Bit Bus Interface D-Type Latches with TRI-STATE® Outputs

General Description

These 10-bit latches feature TRI-STATE outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 10 latches are transparent D-type latches. While the enable (C) is high, the 'AS841 Q outputs will follow the data inputs and the 'AS842 Q outputs will complement the data inputs. When the enable (C) is taken low, the 'AS841 Q outputs will be latched at the levels that were set up at the D inputs, while the 'AS842 Q outputs will be latched at the complement of the $\overline{D}$ input levels.

A buffered output control ($\overline{OC}$) input can be used to place the latch output in either a low impedance (high or low logic level) or a high impedance state (TRI-STATE). In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance TRI-STATE and increased drive in the low impedance states provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data entered while the outputs are in TRI-STATE.

Features

- 10-bit versions of 'AS573/588 with improved I_{OH} specifications
- Provides extra bus driving latches necessary for wider address/data paths or busses with parity
- Buffered control inputs to reduce DC loading
- Power-up in TRI-STATE

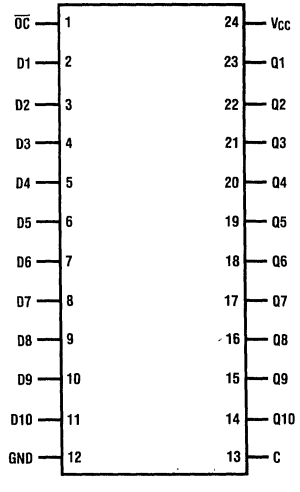
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−55°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package

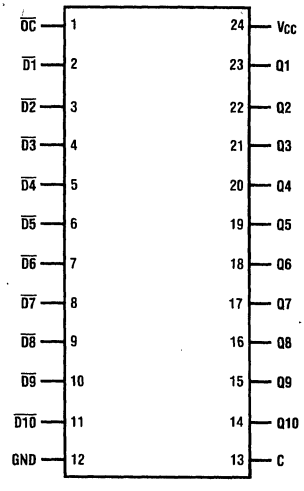


TOP VIEW

TL/F/6726-1

DM54AS841 (J) DM74AS841 (N)

Dual-In-Line Package



TOP VIEW

TL/F/6726-2

DM54AS842 (J) DM74AS842 (N)

Recommended Operating Conditions

Symbol	Parameter	DM54AS841			DM74AS841			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage	2			2			V
V_{IL}	Low-Level Input Voltage			0.8			0.8	V
I_{OH}	High-Level Output Current			−24			−24	mA
I_{OL}	Low-Level Output Current			32			48	mA
t_W	Pulse Width, Enable (C) High	5			4			ns
t_{SU}	Set-Up Time, Data to Enable (C)	3.5			2.5			ns
t_H	Hold Time, Enable (C) to Data	3.5			2.5			ns
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended free-air operating temperature range

Parameter	Conditions	DM54AS841			DM74AS841			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_I	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = Min, I_{OH} = −15 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = Min, I_{OH} = −24 mA	2			2			V
V_{OL}	V_{CC} = Min, I_{OL} = Max		0.25	0.5		0.25	0.5	V
I_{OZH}	V_{CC} = Max, V_O = 2.7V			50			50	μA
I_{OZL}	V_{CC} = Max, V_O = 0.4V			−50			−50	μA
I_I	V_{CC} = Max, V_I = 7V			0.1			0.1	μA
I_{IH}	V_{CC} = Max, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = Max, V_I = 0.4V			−0.5			−0.5	mA
I_{OS}	V_{CC} = Max, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = Max, Outputs High		36	60		36	60	mA
	V_{CC} = Max, Outputs Low		58	94		58	94	mA
	V_{CC} = Max, Outputs Off		56	92		56	92	mA

Switching Characteristics over recommended free-air operating temperature

Parameter	Input	Output	Conditions	DM54AS841			DM74AS841			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	D	Q	V_{CC} = 4.5V to 5.5V, $R1 = 500\Omega$, $R2 = 500\Omega$, C_L = 50 pF	1		8.5	1		6.5	ns
t_{PHL}				1		10	1		9	ns
t_{PLH}	C	Q		2		13	2		12	ns
t_{PHL}				2		13	2		12	ns
t_{PZH}	$\overline{OC}$	Q		2		13.5	2		10.5	ns
t_{PZL}				2		14.5	2		11.5	ns
t_{PHZ}				1		10	1		8	ns
t_{PLZ}				1		10	1		8	ns

Note 1: All typicals are measured at V_{CC} = 5V and T_A = 25°C.

Recommended Operating Conditions

Symbol	Parameter	DM54AS842			DM74AS842			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage	2			2			V
V_{IL}	Low-Level Input Voltage			0.8			0.8	V
I_{OH}	High-Level Output Current			−24			−24	mA
I_{OL}	Low-Level Output Current			32			48	mA
t_W	Pulse Width, Enable (C) High	5			4			ns
t_{SU}	Set-Up Time, Data to Enable (C)	3.5			2.5			ns
t_H	Hold Time, Enable (C) to Data	3.5			2.5			ns
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended free-air operating temperature range

Parameter	Conditions	DM54AS842			DM74AS842			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_I	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = Min, I_{OH} = −15 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = Min, I_{OH} = −24 mA	2			2			V
V_{OL}	V_{CC} = Min, I_{OL} = Max		0.25	0.5		0.25	0.5	V
I_{OZH}	V_{CC} = Max, V_O = 2.7V			50			50	μA
I_{OZL}	V_{CC} = Max, V_O = 0.4V			−50			−50	μA
I_I	V_{CC} = Max, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = Max, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = Max, V_I = 0.4V			−0.5			−0.5	mA
I_{OS}	V_{CC} = Max, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = Max, Outputs High		38	62		38	62	mA
	V_{CC} = Max, Outputs Low		60	97		60	97	mA
	V_{CC} = Max, Outputs Off		58	95		58	95	mA

Switching Characteristics over recommended free-air operating temperature

Parameter	Input	Output	Conditions	DM54AS842			DM74AS842			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	D	Q	V_{CC} = 4.5V to 5.5V R1 = 500Ω R2 = 500Ω C_L = 50 pF	1		11	1		8.5	ns
t_{PHL}				1		10	1		9	ns
t_{PLH}	C	Q		2		13	2		12	ns
t_{PHL}				2		13	2		12	ns
t_{PZH}	OC	Q		2		14.5	2		12	ns
t_{PZL}				2		15	2		12.5	ns
t_{PHZ}				1		10	1		8	ns
t_{PLZ}				1		10	1		8	ns

Note 1: All typicals are measured at V_{CC} = 5V and T_A = 25°C.

Function Tables

'AS841

Inputs			Output
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Hi-Z

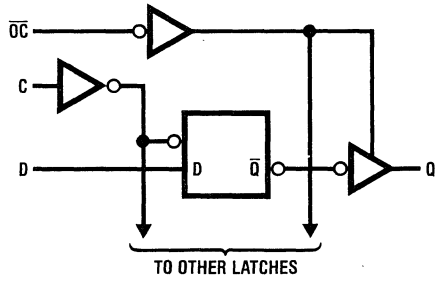
'AS842

Inputs			Output
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q0
H	X	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level
Q0 = the level of Q before the indicated steady-state input conditions were set up
Hi-Z = TRI-STATE

Logic Diagrams

'AS841



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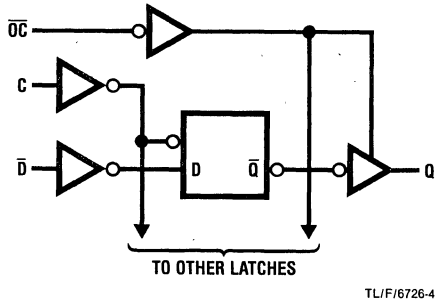
'AS842



TL/F/6726-4

National Semiconductor

PRELIMINARY

DM54AS843/DM74AS843, DM54AS844/DM74AS844 9-Bit Bus Interface D-Type Latches with TRI-STATE® Outputs

General Description

These 9-bit latches feature TRI-STATE outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 9 latches are transparent D-type latches. While the enable (C) is high, the 'AS843 Q outputs will follow the data inputs and the 'AS844 Q outputs will complement the data inputs. When the enable (C) is taken low, the 'AS843 Q outputs will be latched at the levels that were set up at the D inputs, while the 'AS844 Q outputs will be latched at the complement of the $\overline{D}$ input levels.

Taking the $\overline{CLEAR}$ input low will cause the 9 Q outputs to go low, and taking the $\overline{PRESET}$ input low will cause the 9 Q outputs to go high. When both $\overline{PR}$ and $\overline{CLR}$ are taken low, the outputs will follow the $\overline{PRESET}$ condition.

A buffered output control ($\overline{OC}$) input can be used to place the 9 outputs in either a low impedance (high or low logic level) or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance TRI-STATE and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data entered while the outputs are off.

Features

- 9-bit versions of 'AS573/580 with Clear, Preset and improved I_{OH} specifications
- Provides extra bus driving latches necessary for wider address/data paths or busses with parity
- Buffered control inputs to reduce DC loading
- Power-up in TRI-STATE

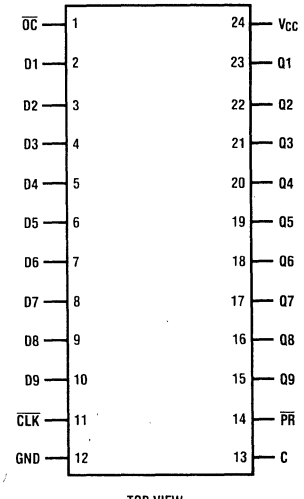
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−55°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package

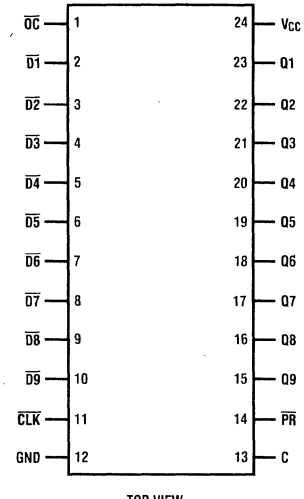


TOP VIEW

TL/F/6727-1

DM54AS843 (J) DM74AS843 (N)

Dual-In-Line Package



TOP VIEW

TL/F/6727-2

DM54AS844 (J) DM74AS844 (N)

Recommended Operating Conditions

Symbol	Parameter		DM54AS843			DM74AS843			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0.8			0.8	V
I_{OH}	High-Level Output Current				−24			−24	mA
I_{OL}	Low-Level Output Current				32			48	mA
t_W	Pulse Width	$\overline{CLR}$, $\overline{PR}$ Low	5			4			ns
		C High	5			4			ns
t_{SU}	Set-Up Time, Data to Enable (C)		3.5			2.5			ns
t_H	Hold Time, Enable (C) to Data		3.5			2.5			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended free-air operating temperature range

Parameter	Conditions	DM54AS843			DM74AS843			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_I	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = Min, I_{OH} = −15 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = Min, I_{OH} = −24 mA	2			2			V
V_{OL}	V_{CC} = Min, I_{OL} = Max		0.25	0.5		0.25	0.5	V
I_{OZH}	V_{CC} = Max, V_O = 2.7V			50			50	μA
I_{OZL}	V_{CC} = Max, V_O = 0.4V			−50			−50	μA
I_I	V_{CC} = Max, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = Max, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = Max, V_I = 0.4V			−0.5			−0.5	mA
I_{OS}	V_{CC} = Max, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = Max, Outputs High		38	62		38	62	mA
	V_{CC} = Max, Outputs Low		57	92		57	92	mA
	V_{CC} = Max, Outputs Off		56	92		56	92	mA

Note 1: All typical values are at V_{CC} = 5V and T_A = 25°C.

Switching Characteristics over recommended free-air operating temperature

Parameter	Input	Output	Conditions	DM54AS843			DM74AS843			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	D	Q	V_{CC} = 4.5V to 5.5V R1 = 500Ω R2 = 500Ω C_L = 50 pF	1		8.5	1		6.5	ns
t_{PHL}				1		10	1		9	ns
t_{PLH}	C	Q		2		13	2		12	ns
t_{PHL}				2		13	2		12	ns
t_{PLH}	$\overline{PR}$	Q		2		12	2		10	ns
t_{PHL}	$\overline{CLR}$	Q		2		14	2		13	ns
t_{PZH}	$\overline{OC}$	Q		2		13.5	2		10.5	ns
t_{PZL}				2		14.5	2		11.5	ns
t_{PHZ}				1		10	1		8	ns
t_{PLZ}				1		10	1		8	ns

Note 1: All typicals are measured at V_{CC} = 5V and T_A = 25°C.

Recommended Operating Conditions

Symbol	Parameter		DM54AS844			DM74AS844			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0.8			0.8	V
I_{OH}	High-Level Output Current				−15			−15	mA
					−24			−24	mA
I_{OL}	Low-Level Output Current				32			48	mA
t_W	Pulse Width	$\overline{CLR}$, $\overline{PR}$ Low	5			4			ns
		C High	5			4			ns
t_{SU}	Set-Up Time, Data to Enable (C)		3.5			2.5			ns
t_H	Hold Time, Enable (C) to Data		3.5			2.5			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended free-air operating temperature range

Parameter	Conditions	DM54AS844			DM74AS844			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_I	V_{CC} = Min, I_I = − 18 mA			− 1.2			− 1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = − 2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = Min, I_{OH} = − 15 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = Min, I_{OH} = − 24 mA	2			2			V
V_{OL}	V_{CC} = Min, I_{OL} = Max		0.25	0.5		0.25	0.5	V
I_{OZH}	V_{CC} = Max, V_O = 2.7V			50			50	μA
I_{OZL}	V_{CC} = Max, V_O = 0.4V			− 50			− 50	μA
I_I	V_{CC} = Max, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = Max, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = Max, V_I = 0.4V			− 0.5			− 0.5	mA
I_{OS}	V_{CC} = Max, V_O = 2.25V	− 30		− 112	− 30		− 112	mA
I_{CC}	V_{CC} = Max, Outputs High		39	64		39	64	mA
	V_{CC} = Max, Outputs Low		58	95		58	95	mA
	V_{CC} = Max, Outputs Off		58	95		58	95	mA

Switching Characteristics over recommended free-air operating temperature

Parameter	Input	Output	Conditions	DM54AS844			DM74AS844			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	D	Q	V_{CC} = 4.5V to 5.5V R1 = 500Ω R2 = 500Ω C_L = 50 pF	1		11	1		8.5	ns
t_{PHL}				1		11	1		10	ns
t_{PLH}	C	Q		2		14	2		12.5	ns
t_{PHL}				2		14	2		13	ns
t_{PLH}	$\overline{PR}$	Q		2		12	2		10	ns
t_{PHL}	$\overline{CLR}$	Q		2		14.5	2		13.5	ns
t_{PZH}	$\overline{OC}$	Q		2		14.5	2		12	ns
t_{PZL}				2		15	2		13.5	ns
t_{PHZ}				1		10	1		8	ns
t_{PLZ}				1		10	1		8	ns

Note 1: All typicals are measured at V_{CC} = 5V and T_A = 25°C.

Function Tables

'AS843

Inputs					Output
$\overline{OC}$	$\overline{CLR}$	$\overline{PR}$	C	D	Q
L	L	H	H	X	L
L	H	L	H	X	H
L	L	L	H	X	H
L	H	H	H	H	H
L	H	H	H	L	L
L	X	X	L	X	Q0
H	X	X	X	X	Hi-Z

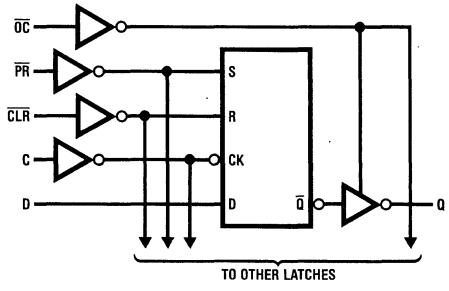
'AS844

Inputs					Output
$\overline{OC}$	$\overline{CLR}$	$\overline{PR}$	C	$\overline{D}$	Q
L	L	H	H	X	L
L	H	L	H	X	H
L	L	L	H	X	H
L	H	H	H	H	L
L	H	H	H	L	H
L	X	X	L	X	Q0
H	X	X	X	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level
Q0 = the level of Q before the indicated steady-state input conditions were set up
Hi-Z = TRI-STATE

Logic Diagrams

'AS843



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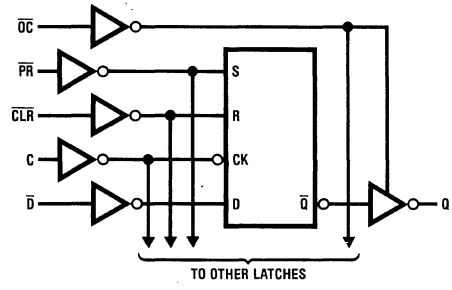
'AS844



TL/F/6727-4

National Semiconductor

PRELIMINARY

DM54AS845/DM74AS845, DM54AS846/DM74AS846 8-Bit Bus Interface D-Type Latches with TRI-STATE® Outputs

General Description

These 8-bit latches feature TRI-STATE outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 8 latches are transparent D-type latches. While the enable (C) is high, the 'AS845 Q outputs will follow the data inputs and the 'AS846 Q outputs will complement the data inputs. When the enable (C) is taken low, the 'AS845 Q outputs will be latched at the levels that were set up at the D inputs, while the 'AS846 Q outputs will be latched at the complement of the D input levels.

Taking the $\overline{\text{CLEAR}}$ input low will cause the 8 Q outputs to go low, and taking the $\overline{\text{PRESET}}$ input low will cause the 8 Q outputs to go high. When both $\overline{\text{PR}}$ and $\overline{\text{CLR}}$ are taken low, the outputs will follow the $\overline{\text{PRESET}}$ condition.

A multiuser buffered output control ($\overline{\text{OC}}$) input can be used to place the 8 outputs in either a low impedance (high or low logic level) or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance TRI-STATE and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

The output control ($\overline{\text{OC}}$) does not affect the internal operation of the latches. Old data can be retained or new data entered while the outputs are off.

Features

- Similar to 'AS573/580 with Clear, Preset, and multiple output controls
- Improved I_{OH} specifications
- Multiple output control inputs allow multiuser control of the interface
- Buffered control inputs to reduce DC loading
- Power-up in TRI-STATE

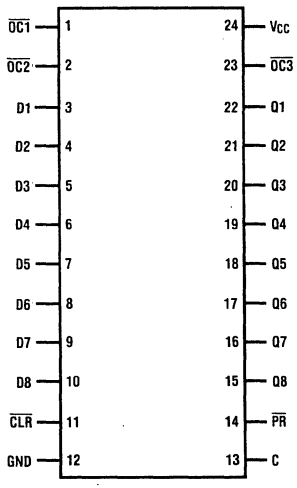
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−55°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package

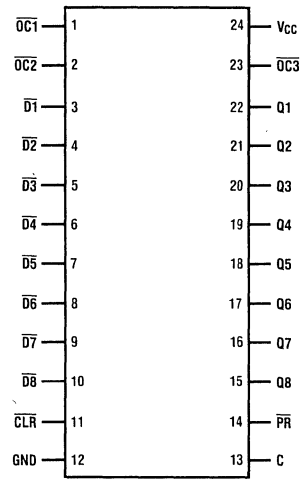


TOP VIEW

TL/F/6728-1

DM54AS845 (J) DM74AS845 (N)

Dual-In-Line Package



TOP VIEW

TL/F/6728-2

DM54AS846 (J) DM74AS846 (N)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Recommended Operating Conditions

Symbol	Parameter		DM54AS845			DM74AS845			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0.8			0.8	V
I_{OH}	High-Level Output Current				−24			−24	mA
I_{OL}	Low-Level Output Current				32			48	mA
t_W	Pulse Width	$\overline{CLR}$, $\overline{PR}$ Low	5			4			ns
		C High	5			4			ns
t_{SU}	Set-Up Time, Data to Enable (C)		3.5			2.5			ns
t_H	Hold Time, Enable (C) to Data		3.5			2.5			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended free-air operating temperature range

Parameter	Conditions	DM54AS845			DM74AS845			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_I	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = Min, I_{OH} = −15 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = Min, I_{OH} = −24 mA	2			2			V
V_{OL}	V_{CC} = Min, I_{OL} = Max		0.25	0.5		0.25	0.5	V
I_{OZH}	V_{CC} = Max, V_O = 2.7V			50			50	μA
I_{OZL}	V_{CC} = Max, V_O = 0.4V			−50			−50	μA
I_I	V_{CC} = Max, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = Max, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = Max, V_I = 0.4V			−0.5			−0.5	mA
I_{OS}	V_{CC} = Max, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = Max, Outputs High		35	58		35	58	mA
	V_{CC} = Max, Outputs Low		52	85		52	85	mA
	V_{CC} = Max, Outputs Off		52	85		52	85	mA

Note 1: All typical values are at V_{CC} = 5V and T_A = 25°C.

Switching Characteristics over recommended free-air operating temperature

(See Section 1 for Test Waveforms and Output Load)

Parameter	Input	Output	Conditions	DM54AS845			DM74AS845			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	D	Q	V_{CC} = 4.5V to 5.5V R1 = 500Ω R2 = 500Ω C_L = 50 pF	1		8.5	1		6.5	ns
t_{PHL}				1		10	1		9	ns
t_{PLH}	C	Q		2		13	2		12	ns
t_{PHL}				2		13	2		12	ns
t_{PLH}	$\overline{PR}$	Q		2		12	2		10	ns
t_{PHL}	$\overline{CLR}$	Q		2		14	2		13	ns
t_{PZH}	$\overline{OC}$	Q		2		13.5	2		10.5	ns
t_{PZL}				2		14.5	2		11.5	ns
t_{PHZ}				1		10	1		8	ns
t_{PLZ}				1		10	1		8	ns

Recommended Operating Conditions

Symbol	Parameter		DM54AS846			DM74AS846			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0.8			0.8	V
I_{OH}	High-Level Output Current				−24			−24	mA
I_{OL}	Low-Level Output Current				32			48	mA
t_W	Pulse Width	$\overline{CLR}$, $\overline{PR}$ Low	5			4			ns
		C High	5			4			ns
t_{SU}	Set-Up Time, Data to Enable (C)		3.5			2.5			ns
t_H	Hold Time, Enable (C) to Data		3.5			2.5			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Note 1: All typicals are measured at V_{CC} = 5V and T_A = 25°C.

Electrical Characteristics over recommended free-air operating temperature range

Parameter	Conditions	DM54AS846			DM74AS846			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_I	V_{CC} = Min, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	V_{CC} = Min, I_{OH} = −15 mA	2.4	3.2		2.4	3.2		V
	V_{CC} = Min, I_{OH} = −24 mA	2			2			V
V_{OL}	V_{CC} = Min, I_{OL} = Max		0.25	0.5		0.25	0.5	V
I_{OZH}	V_{CC} = Max, V_O = 2.7V			50			50	μA
I_{OZL}	V_{CC} = Max, V_O = 0.4V			−50			−50	μA
I_I	V_{CC} = Max, V_I = 7V			0.1			0.1	mA
I_{IH}	V_{CC} = Max, V_I = 2.7V			20			20	μA
I_{IL}	V_{CC} = Max, V_I = 0.4V			−0.5			−0.5	mA
I_{OS}	V_{CC} = Max, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = Max, Outputs High		36			36		mA
	V_{CC} = Max, Outputs Low		53			53		mA
	V_{CC} = Max, Outputs Off		53			53		mA

Switching Characteristics over recommended free-air operating temperature

(See Section 1 for Test Waveforms and Output Load)

Parameter	Input	Output	Conditions	DM54AS846			DM74AS846			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	D	Q	V_{CC} = 4.5V to 5.5V R1 = 500Ω R2 = 500Ω C_L = 50 pF		4.5			4.5		ns
t_{PHL}					5			5		ns
t_{PLH}	C	Q								ns
t_{PHL}										ns
t_{PLH}	$\overline{PR}$	Q			5			5		ns
t_{PHL}	$\overline{CLR}$	Q			5.5			5.5		ns
t_{PZH}	$\overline{OC}$	Q			6			6		ns
t_{PZL}					6			6		ns
t_{PHZ}					4			4		ns
t_{PLZ}					5			5		ns

Note 1: All typicals are measured at V_{CC} = 5V and T_A = 25°C.

Function Tables

'AS845

Inputs					Output
$\overline{OC}$*	$\overline{CLR}$	$\overline{PR}$	C	D	Q
L	L	H	H	X	L
L	H	L	H	X	H
L	L	L	H	X	H
L	H	H	H	H	H
L	H	H	H	L	L
L	X	X	L	X	Q0
H	X	X	X	X	Hi-Z

'AS846

Inputs					Output
$\overline{OC}$*	$\overline{CLR}$	$\overline{PR}$	C	$\overline{D}$	Q
L	L	H	H	X	L
L	H	L	H	X	H
L	L	L	H	X	H
L	H	H	H	H	L
L	H	H	H	L	H
L	X	X	L	X	Q0
H	X	X	X	X	Hi-Z

*$\overline{OC} = \overline{OC1} \bullet \overline{OC2} \bullet \overline{OC3}$

H = High Logic Level

L = Low Logic Level

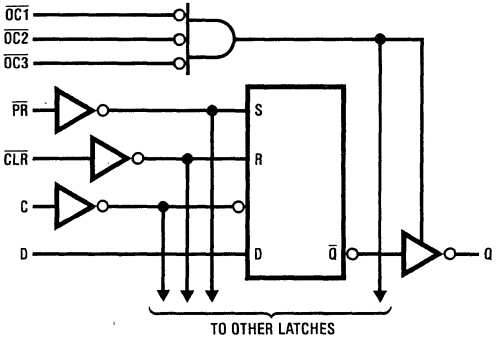
X = Either High or Low Logic Level

Q0 = the level of Q before the indicated steady-state input conditions were set up

Hi-Z = TRI-STATE

Logic Diagrams

'AS845



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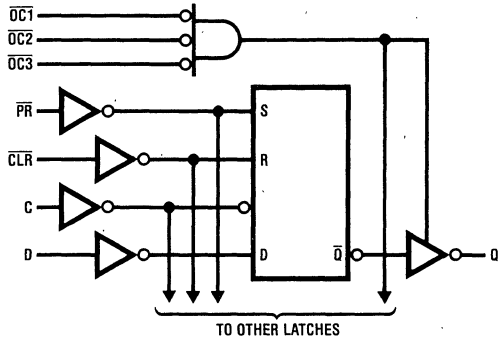
'AS846



TL/F/6728-4

National Semiconductor

DM54AS873/DM74AS873 Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS873 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output conrol does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

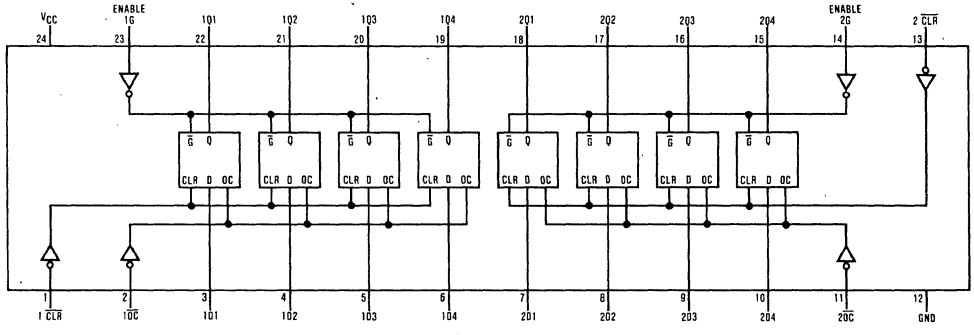
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS873	−55°C to 125°C
DM74AS873	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6630-1

54AS873 (J) **74AS873 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS873			DM74AS873			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Pulse Width, T_W	Enable High	5.5			4.5			ns
	Clear Low	4.5			3.5			
Data Setup Time, T_{SU}		2↓			2↓			ns
Data Hold Time, T_H		3↓			3↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		68	110	mA
			Outputs Low		67	109	mA
			Outputs Disabled		80	129	mA

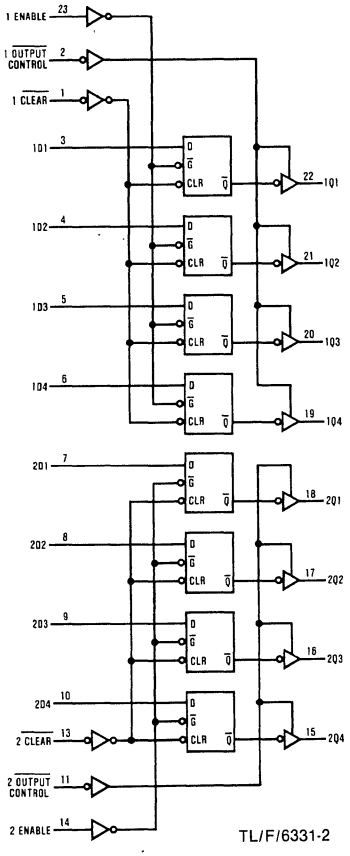
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS873			DM74AS873			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		9	3		6	ns
T_{PHL}				3		7	3		6	ns
T_{PLH}	Enable	Any Q		6		14	6		11.5	ns
T_{PHL}				4		9	4		7.5	ns
T_{PZH}	Output Control	Any Q		2		8	2		6.5	ns
T_{PZL}				4		11	4		9.5	ns
T_{PHZ}				2		8	2		6.5	ns
T_{PLZ}				2		8.5	2		7.5	ns
T_{PHL}	Clear	Any Q		3		8.5	3		7.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6331-2

Function Table

$\overline{CLR}$	D	EN	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54AS874/DM74AS874
Dual 4-Bit D-Type Edge-Triggered Flip-Flops

General Description

These dual 4-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS874 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

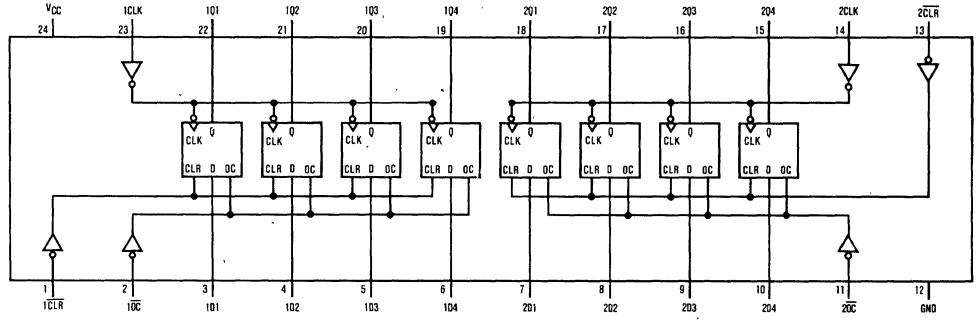
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS874	−55°C to 125°C
DM74AS874	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6331-1

54AS874 (J) 74AS874 (J,N)

Recommended Operating Conditions

Parameter		DM54AS874			DM74AS874			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	4			3			ns
	Low	5			4			ns
Width of Clear Pulse, T_W	Low	3			2			ns
Setup Time, T_{SU}	Data	2.5↑			2↑			ns
	Clear Inactive	5↑			4↑			
Data Hold Time, T_H		1↑			1↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

3

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		82	133	mA
			Outputs Low		92	149	mA
			Outputs Disabled		100	160	mA

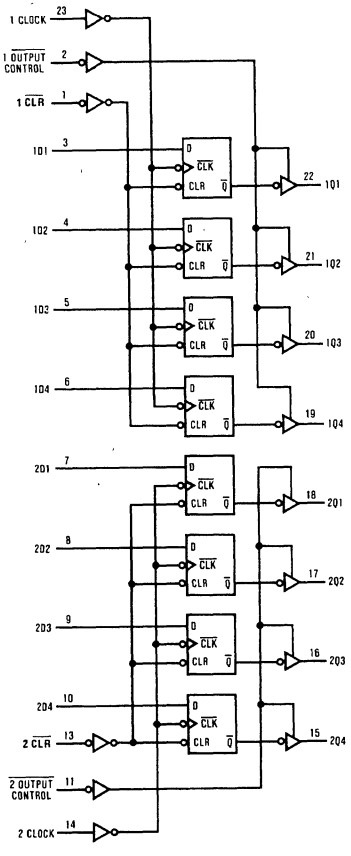
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS874			DM74AS874			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any Q		3		11.5	3		8.5	ns
T_{PHL}				4		12.5	4		10.5	ns
T_{PZH}	Output Control	Any Q		2		8	2		7	ns
T_{PZL}				3		11.5	3		10.5	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		8.5	2		7.5	ns
T_{PHL}	Clear	Any Q		4		11	4		9.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6331-2

Function Table

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54AS876/DM74AS876 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These inverting dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS876 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

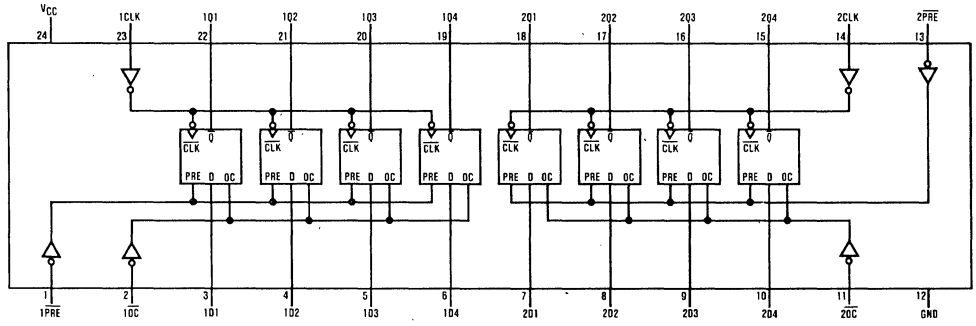
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS876	−55°C to 125°C
DM74AS876	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6332-1

54AS876 (J) **74AS876 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS876			DM74AS876			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	4			3			ns
	Low	5			4			
Width of Preset Pulse, T_W	Low	3			2			ns
Data Setup Time, T_{SU}	Data	2.5↑			2↑			ns
	Clear Inactive	5			4			
Data Hold Time, T_H		1↑			1↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

3

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		88	142	mA
			Outputs Low		94	150	
			Outputs Disabled		100	160	

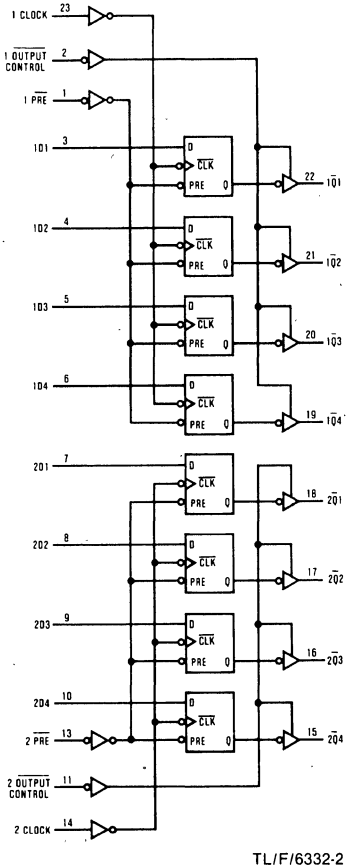
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS876			DM74AS876			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any $\overline{Q}$		3		11.5	3		8.5	ns
T_{PHL}				4		12.5	4		10.5	ns
T_{PZH}	Output Control	Any $\overline{Q}$		2		8	2		7	ns
T_{PZL}				3		11.5	3		10.5	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns
T_{PHL}	Preset	Any $\overline{Q}$		4		11	4		9.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6332-2

Function Table

$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

3

National Semiconductor

DM54AS878/DM74AS878 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with Synchronous Clear

General Description

These dual 4-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS878 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.
- Synchronous clear.

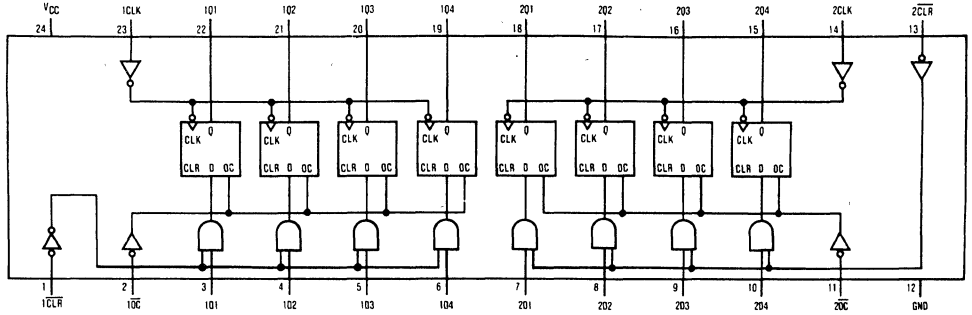
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS878	−55°C to 125°C
DM74AS878	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6333-1

54AS878 (J) 74AS878 (J,N)

Recommended Operating Conditions

Parameter		DM54AS878			DM74AS878			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5			4			ns
	Low	3			2			
Data Setup Time, T_{SU}	Data	3↑			2↑			ns
	$\overline{CLR}$	6.5↑			5.5↑			
Data Hold Time, T_H	Data	3↑			2↑			ns
	$\overline{CLR}$	0↑			0↑			

The (↑) arrow indicates the positive edge of the Clock is used for reference.

3

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				-1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to $5.5V$		$V_{CC} -2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				-0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		-30		-112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				-50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		82	132	mA
			Outputs Low		96	155	
			Outputs Disabled		100	160	

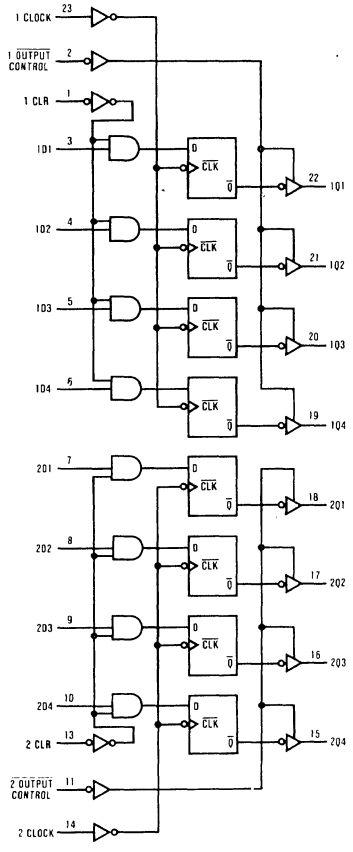
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS878			DM74AS878			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any Q		3		11.5	3		8.5	ns
T_{PHL}				4		12.5	4		10.5	ns
T_{PZH}	Output Control	Any Q		2		8	2		7	ns
T_{PZL}				3		11.5	3		10.5	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6333-2

Function Table

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	↑	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

3

National Semiconductor

DM54AS879/DM74AS879 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs and Synchronous Clear

General Description

These inverting dual 4-bit registers feature totem-pole TRI-STATE®outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS879 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.
- Synchronous Preset.

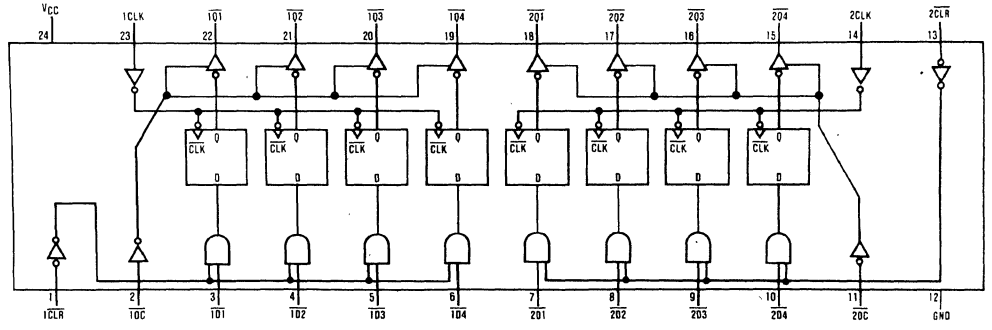
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS879	−55°C to 125°C
DM74AS879	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6334-1

54AS879 (J) **74AS879 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS879			DM74AS879			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		125	MHz
Width of Clock Pulse, T_W	High	5			4			ns
	Low	3			2			ns
Data Setup Time, T_{SU}	Data	3↑			2↑			ns
	CLR	6.5↑			5.5↑			
Data Hold Time, T_H	Data	3↑			2↑			ns
	CLR	0↑			0↑			

The (↑) arrow indicates the positive edge of the Clock is used for reference.

3

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} - 2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$ I_{OH} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		88	142	mA
			Outputs Low		94	150	
			Outputs Disabled		100	160	

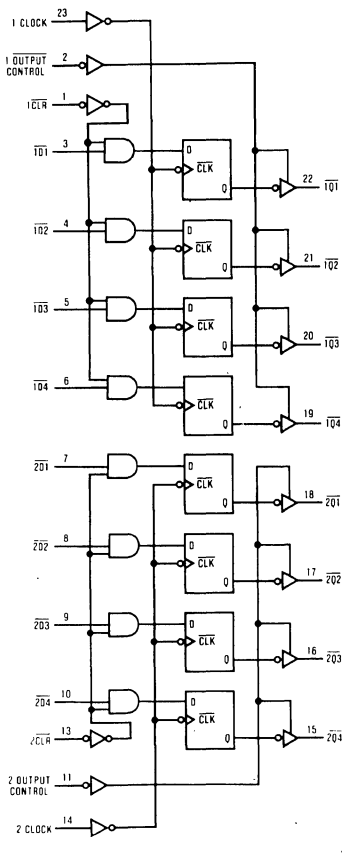
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS879			DM74AS879			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100			125			MHz
T_{PLH}	Clock	Any $\overline{Q}$		3		11.5	3		8.5	ns
T_{PHL}				4		12.5	4		10.5	ns
T_{PZH}	Output Control	Any $\overline{Q}$		2		8	2		7	ns
T_{PZL}				3		11.5	3		10.5	ns
T_{PHZ}				2		7	2		6	ns
T_{PLZ}				2		7	2		6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6334-2

Function Table

CLR	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	↑	L	H
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54AS880/DM74AS880 Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit inverting registers feature totem-pole TRI-STATE®outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS880 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- TRI-STATE Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

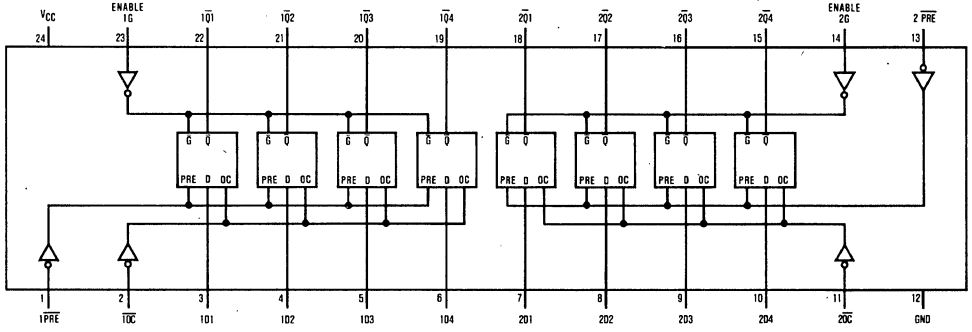
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS880	−55°C to 125°C
DM74AS880	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6335-1

54AS880 (J) 74AS880 (J,N)

Recommended Operating Conditions

Parameter		DM54AS880			DM74AS880			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Pulse Width, T_W	Enable	3.5			2.5			ns
	Preset Low	4.5			3.5			ns
Data Setup Time, T_{SU}		2↓			2↓			ns
Data Hold Time, T_H		1↓			1↓			ns

The (↓) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX I_{OH} = MAX		2.4	3.3		V
		$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC} -2$			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V$, $V_{IH} = 2V$ V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		73	118	mA
			Outputs Low		76	122	
			Outputs Disabled		86	137	

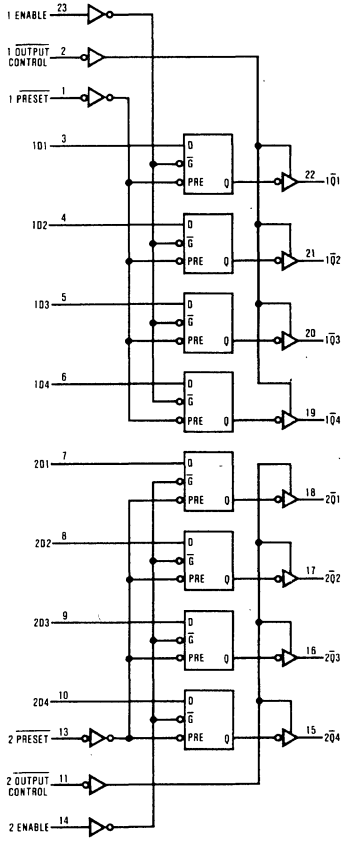
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS880			DM74AS880			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	4		11	4		9.5	ns
T_{PHL}				4		9	4		8.5	ns
T_{PLH}	Enable	Any $\overline{Q}$		6		14	6		11.5	ns
T_{PHL}				4		10	4		8	ns
T_{PZH}	Output Control	Any $\overline{Q}$		2		8	2		7.5	ns
T_{PZL}				4		11	4		10	ns
T_{PHZ}				2		8	2		6.5	ns
T_{PLZ}				2		9	2		8	ns
T_{PHL}	Preset	Any $\overline{Q}$		4		11.5	4		10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6335-2

Function Table

$\overline{PRE}$	D	EN	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

3

National Semiconductor

DM54AS881B/DM74AS881B 4-Bit Arithmetic Logic Unit/Function Generator

General Description

The DM54/DM74AS881B are arithmetic logic units (ALU)/function generators that have a complexity of 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the DM54AS882 or DM74AS882 full carry look-ahead circuits, high speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under "signal designations".

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterpart
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high speed operations on long words

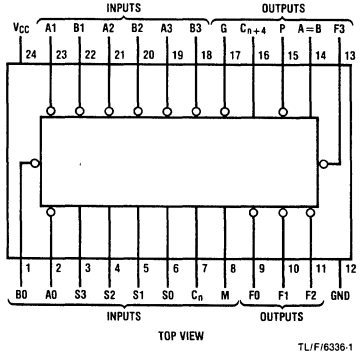
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free-Air Temperature Range	
DM54AS	−55°C to +125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6336-1

54AS881B (J) 74AS881B (J, N)

Pin Designations

Designation	Pin Number	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Recommended Operating Conditions

Symbol	Parameter	DM54AS881B			DM74AS881B			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{OH}	High Level Output Voltage A = B Output Only			5.5			5.5	V
I_{OH}	High Level Output Current All Outputs Except A = B and $\overline{G}$			−2			−2	mA
	$\overline{G}$			−3			−3	
I_{OL}	Low Level Output Current All Outputs Except $\overline{G}$			20			20	mA
	$\overline{G}$			48			48	
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

Symbol	Parameter	Conditions	DM54AS881A			DM74AS881A			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any Output Except A = B	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
	$\overline{G}$	V_{CC} = 4.5V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
I_{OH}	A = B	V_{CC} = 4.5V, V_{OH} = 5.5V			0.1			0.1	mA
V_{OL}	Any Output Except $\overline{G}$	V_{CC} = 4.5V, I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	$\overline{G}$	V_{CC} = 4.5V, I_{OL} = 48 mA		0.4	0.5		0.4	0.5	
I_I	M Input	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
	Any A or B Input				0.3			0.3	
	Any S Input				0.4			0.4	
	Carry Input				0.6			0.6	
I_{IH}	M Input	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
	Any A or B Input				60			60	
	Any S Input				80			80	
	Carry Input				120			120	
I_{IL}	M Input	V_{CC} = 5.5V, V_I = 0.4V			−0.5			−0.5	mA
	Any A or B Input				−1.5			−1.5	
	Any S Input				−2			−2	
	Carry Input				−3			−3	
I_O (Note 2)	All Outputs Except A = B and $\overline{G}$	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
	$\overline{G}$			−165			−165		
I_{CC}		V_{CC} = 5.5V		70	104		70	104	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit current, I_{OS}.

Switching Characteristics

Symbol	Parameter	From (Input)	To (Output)	Conditions	$C_L = 50$ pF (15 pF for A = B), $R_L = 500\Omega$ (280Ω for A = B)						Units
					DM54AS881B			DM74AS881B			
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+4}		2		11	2		9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		11	2		9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ Mode)	2		14	2		12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		14	2		12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	2		20	2		16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		20	2		16	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ Mode)	3		11	3		9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3		11	3		9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ Mode)	2		9	2		7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		9	2		7	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	2		12	2		9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		12	2		9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ Mode)	2		11	2		8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		11	2		8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	2		13	2		10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		13	2		10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ Mode)	2		11	2		8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		11	2		8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	2		12	2		10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		12	2		10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5V (Logic Mode)	2		16	2		11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2		16	2		11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	4		26	4		21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				4		26	4		21	

Switching Characteristics (Continued)

Symbol	Parameter	From (Input)	To (Output)	Conditions	$C_L = 50$ pF (15 pF for A = B), $R_L = 500\Omega$ (280Ω for A = B)						Units
					DM54AS881B			DM74AS881B			
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A or B	P	C_n = M = S0 = S3 = 4.5V, S1 = S2 = 0V, Equality ($A_i = B_i$ or $A_i \neq B_i$)	2		19	2		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2		19	2		15	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A or B	C_{n+4}	C_n = M = S3 = 4.5V, S1 = S2 = 0V, Equality ($A_i = B_i$ or $A_i \neq B_i$)	2		24	2		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2		24	2		18	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A or B	P	C_n = m = S2 = 4.5V, S0 = S1 = S3 = 0V, ($A_i = B_i$ = H or A_i or B_i = L	2		19	2		15	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2		19	2		15	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Any A or B	C_{n+4}	C_n = M = S2 = 4.5V, S0 = S1 = S3 = 0V, ($A_i = B_i$ = H or A_i or B_i = L)	2		25	2		19	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2		25	2		19	ns

Number of Bits	Typical Addition Times Using AS881 and AS882	Package Count		Carry Method Between ALUs
		Arithmetic/ Logic Units	Look-Ahead Carry Generators	
1 to 4	5	1	0	None
5 to 8	10	2	0	Ripple
9 to 16	14	3 or 4	1	Full Look-Ahead
17 to 64	19	5 to 16	2 to 5	Full Look-Ahead

Functional Description

The DM54/74AS881B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table I)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-High Data (Table II)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B.

The DM54/DM74AS881B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	Active-Low Data *(Figure 1)*	Active-High Data *(Figure 2)*
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables I and II and include exclusive-OR, NAND, AND, NOR, and OR functions.

Functional Description (Continued)

TABLE I

Selection				Active-Low Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = L (No Carry)	C_n = H (With Carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus $(A + \overline{B})$	F = A Plus $(A + \overline{B})$ Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus $(A + \overline{B})$	F = AB Plus $(A + \overline{B})$ Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	F = $(A + \overline{B})$ Plus 1
H	L	L	L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $A\overline{B}$ Plus (A + B)	F = $A\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = $A\overline{B}$ Plus A	F = $A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

TABLE II

Selection				Active-High Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		$\overline{C}_n$ = H (No Carry)	$\overline{C}_n$ = L (With Carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	F = $(A + \overline{B})$ Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Comp)	F = Zero
L	H	L	L	$F = \overline{AB}$	F = A Plus $A\overline{B}$	F = A Plus $A\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	F = (A + B) Plus $A\overline{B}$	F = (A + B) Plus $A\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $(A + \overline{B})$ Plus AB	F = $(A + \overline{B})$ Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = $(A + \overline{B})$ Plus A	F = $(A + \overline{B})$ Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

Functional Description (Continued)

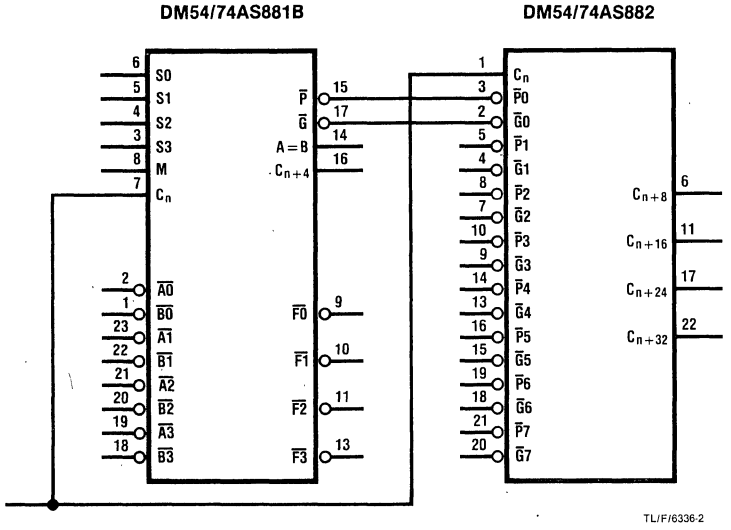


FIGURE 1 (Use with Table I)

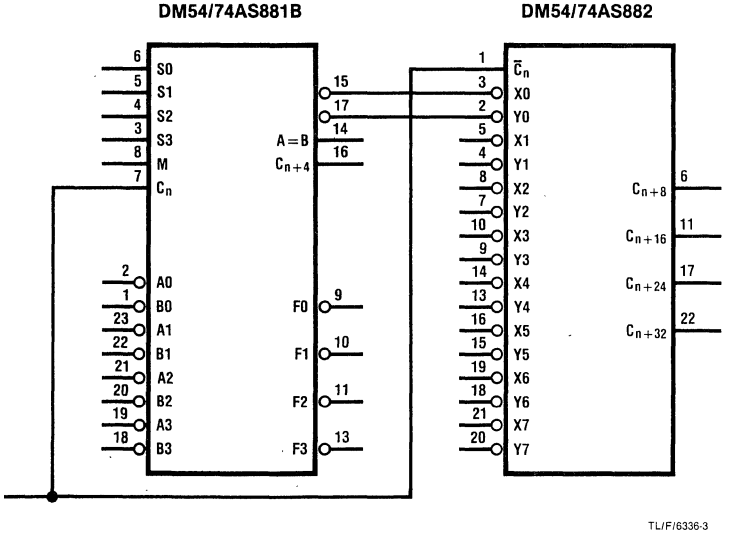


FIGURE 2 (Use with Table II)

Functional Description (Continued)

The DM54/74AS881B has the same pinout and same functionality as the DM54/74AS181B, except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode, the DM54/74AS881B provides the user with a status check on the input words, A and B, and the output word, F. While in the logic mode, the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$\overline{P} = F0 + F1 + F2 + F3$
$\overline{G} = H$
$C_{n+4} = PC_n$.

The combination of signals on the S3 through S0 control lines determines the operation performed on the data words to generate the output bits, F_i. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see Function Table for Input Bits Equal/Not Equal) or if any pair of inputs is high (see Function Table for Input Pairs High/Not High). The DM54/74AS881B has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H, a status check is generated to determine whether all pairs (A_i, B_i) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words, which is available on the totem pole $\overline{P}$ output, is particularly useful when cascading the DM54/74AS881B. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus, the A = B status is transmitted to the second state more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P}$ =
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	$(A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$

SIGNAL DESIGNATIONS

In both *Figures 1 and 2*, the polarity indicators (o—) indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and that the symbols are the same in both figures. The signal designations in *Figure 1* agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table I. The signal designations have been changed in *Figure 2* to accommodate the logic functions and arithmetic operations for the active-high data given in Table II. The DM54/74AS181 and DM54/74AS881B, together with the DM54/74AS882 and DM54/74S182, can be used with the signal designation of either *Figure 1* or *Figure 2*.

Function Table for Input Pairs High/Not High
S0 = S1 = S3 = L, S2 = H, and M = H

C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	H
L	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	L
X	A0 ≠ B0	X	X	X	H	H	L
X	X	A1 ≠ B1	X	X	H	H	L
X	X	X	A2 ≠ B2	X	H	H	L
X	X	X	X	A3 ≠ B3	H	H	L

Function Table for Input Bits Equal/Not Equal
S0 = S3 = H, S1 = S2 = L, and M = H

C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

Parameter Measurement Information

$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In-Phase

Parameter Measurement Information (Continued)

Input Bits Equal/Not Equal Test Table
Function Inputs: S0 = S3 = M = 4.5V, S1 = S2 = 0V

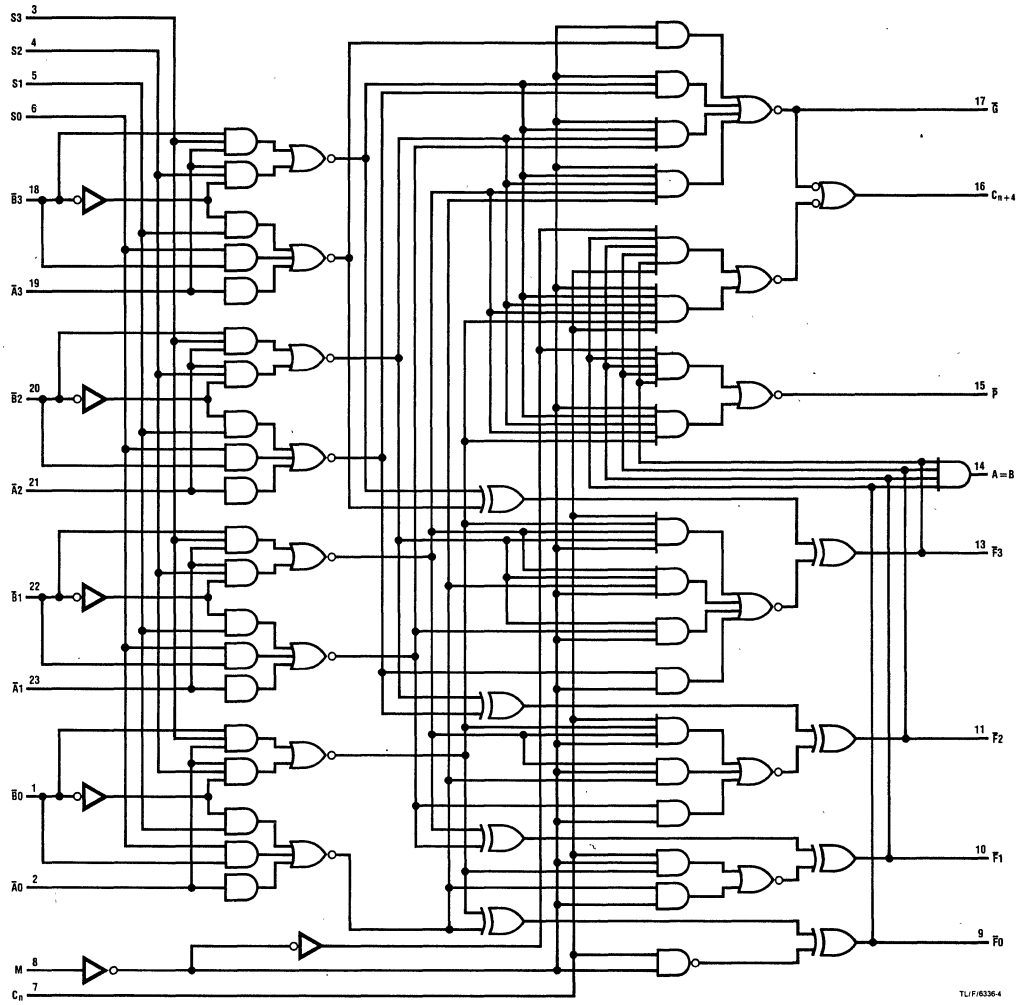
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase

Input Pairs High/Not High Test Table
Function Inputs: S2 = M = 4.5V, S0 = S1 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase

Logic Diagram (Positive Logic)

DM54/74AS881



National Semiconductor

DM54AS1000A/DM74AS1000A Quadruple 2-Input NAND Drivers

General Description

These devices contain four independent 2-input drivers, each of which performs the logic NAND function. The 'AS1000A is a driver version of the 'AS00. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

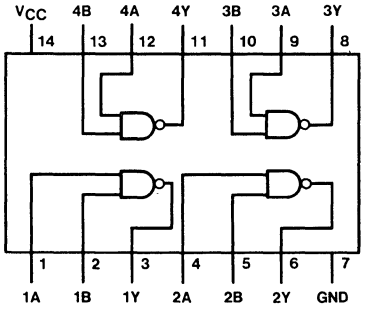
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74AS1000A	−55°C to 125°C
DM54AS1000A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6337-1

54AS1000A (J) 74AS1000A (J, N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Parameter	DM54AS1000A			DM74AS1000A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL}$ MAX	$I_{OH} = -3mA$	2.4	3.2		V
			I_{OH} = MAX	2			V
		$I_{OH} = -2mA$	$V_{CC} = 4.5V$ to 5.5V	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$ I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$		−135		mA
I_{CCH}	Supply Current	Outputs High $V_{CC} = 5.5V$, VI = 0V			2.3	3.5	mA
I_{CCL}	Supply Current	Outputs Low $V_{CC} = 5.5V$, VI = 4.5V			11.5	19	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS1000A			DM74AS1000A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1		5	1		4	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		5	1		4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS1004A/DM74AS1004A Hex Inverting Drivers

General Description

These devices contain six independent 2-input drivers, each of which performs the logic invert/complement function. The 'AS1004A is a driver version of the 'AS04. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

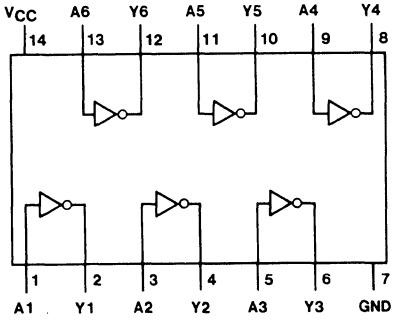
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6338-1

54AS1004A (J) 74AS1004A (J, N)

Function Table

$A = \overline{Y}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

3

Recommended Operating Conditions

Parameter	DM54AS1004A			DM74AS1004A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$I_{OH} = -2mA$, $V_{CC} = 4.5V$ to 5.5V		$V_{CC}-2$			V
		$I_{OH} = -3mA$, $V_{CC} = 4.5V$		2.4	3.2		
		$I_{OH} = MAX$, $V_{CC} = 4.5V$		2			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = MAX$			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$		−135		mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High		3.2	5	mA
			Outputs Low		17.2	28	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS1004A			DM74AS1004A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to 5.5V $R_L = 500\ \Omega$, $C_L = 50$ pF.	1		5	1		4	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		5	1		4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS1008A/DM74AS1008A Quadruple 2-Input AND Drivers

General Description

These devices contain four independent 2-input drivers, each of which performs the logic AND function. The 'AS1008A is a driver version of the 'AS08. Each driver has increased output drive to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

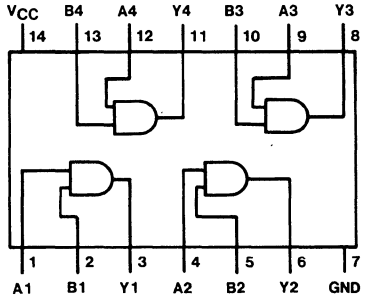
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS1008A	−55°C to 125°C
DM74AS1008A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6339-1

54AS1008A (J) 74AS1008A (J, N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

L = low logic level
H = high logic level

3

Recommended Operating Conditions

Parameter	DM54AS1008A			DM74AS1008A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	$I_{OH} = -3mA$	2.4	3.2		V
			I_{OH} = MAX	2			V
		$I_{OH} = -2mA$	$V_{CC} = 4.5V$ to 5.5V	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, $V_{IL} = 0.8V$, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 4.5V			5.6	9.5	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 0V			18.5	22	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS1008A			DM74AS1008A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		6	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		6.5	1		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS1032A/DM74AS1032A Quadruple 2-Input OR Driver

General Description

These devices contain four independent 2-input drivers, each of which performs the logic OR function. The 'AS1032A is a driver version of the 'AS32. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

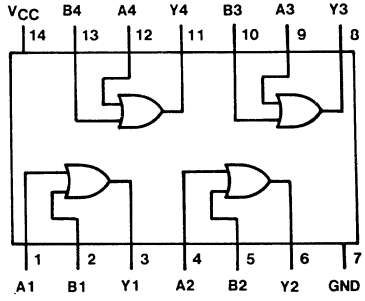
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS1032A	−55°C to 125°C
DM74AS1032A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6340-1

54AS1032A (J) 74AS1032A (J, N)

Function Table

Y = A + B

Inputs		Output
A	B	Y
L	L	L
H	X	H
X	H	H

L = low logic level
H = high logic level
X = either low or high logic level

3

Recommended Operating Conditions

Parameter	DM54AS1032A			DM74AS1032A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18mA$				1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$	$I_{OH} = -3mA$	2.4	3.2		V
			$I_{OH} = MAX$	2			V
		$I_{OH} = -2mA$	$V_{CC} = 4.5V$ to $5.5V$	$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $V_{IH} = 0.8V$, $I_{OL} = MAX$			0.35	0.5	V
I_I	Max High Input Current	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$		−135		mA
I_{CCH}	Supply Current	Outputs High $V_{CC} = 5.5V$, $V_I = 4.5V$			7.7	11.5	mA
I_{CCL}	Supply Current	Outputs Low $V_{CC} = 5.5V$, $V_I = 0V$			14.7	24	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS1032A			DM74AS1032A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5$ to $5.5V$, $R_L = 500\,\Omega$, $C_L = 50$ pF.	1		7	1		6.3	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		7	1		6.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS1034A/DM74AS1034A Hex Non-Inverting Drivers

General Description

These devices contain six independent drivers, each of which performs the logic identity function. The 'AS1034A is a driver version of the 'AS34. Each driver has increased output drive capability, allowing the drivng of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

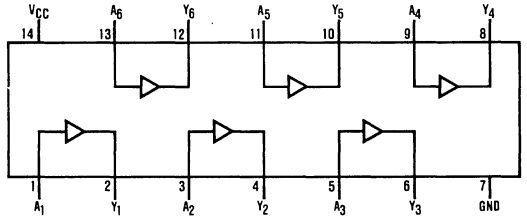
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6341-1

54AS1034A (J) 74AS1034A (J, N)

Function Table

A = Y

Input A	Output Y
L	L
H	H

L = low logic level

H = high logic level

Recommended Operating Conditions

Parameter	DM54AS1034A			DM74AS1034A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		I_{OH} = −3mA		2.4	3.2		V
		I_{OH} = Max		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = MAX		0.35		0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		9.3	14	mA
			Outputs Low		22	33	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS1034A			DM74AS1034A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	1		6.5	1		6	ns
T_{PHL}, Propagation delay time. High to low Level Output		1		6.5	1		6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS1036A/DM74AS1036A Quad 2-Input NOR Drivers

General Description

These devices contain four independent drivers, each of which performs the logic NOR function. Each driver has increased output drive capability, allowing the driving of high capacitive loads.

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power.
- Improved AC Performance Over TTL Counterparts.

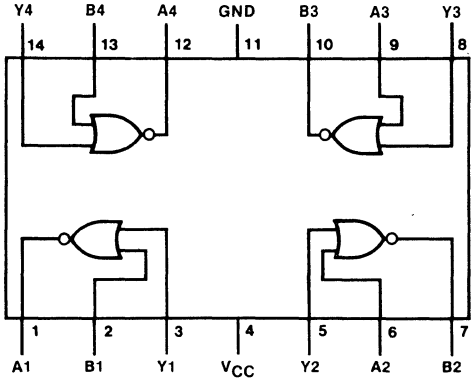
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

3

Connection Diagram



TL/F/6342-1

54AS1036A (J) 74AS1036A (J, N)

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
X	H	L
H	X	L
L	L	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Parameter	DM54AS1036A			DM74AS1036A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
		V_{CC} = 4.5V	I_{OH} = −3mA	2.4			
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−135		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.7	7	mA
			Outputs Low		15.3	23	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	Conditions	DM54AS1036A			DM74AS1036A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	1		4.8	1		4.3	ns
T_{PHL}, Propagation delay time. High to low level output		1		4.8	1		4.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor

DM54AS2620/DM74AS2620, DM54AS2623/DM74AS2623 Octal Bus Transceivers/MOS Drivers

General Description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of the $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

Features

- Bidirectional octal bus transceivers for driving MOS devices
- I/O ports have 25Ω series resistors so no external resistors are required
- Local bus-latch capability
- Choice of true or inverting logic

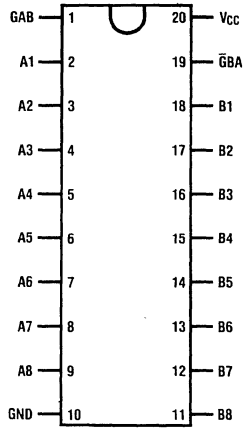
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
I/O Ports	5.5V
Other Ports	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TOP VIEW

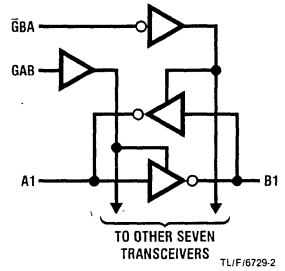
TL/F/6729-1

Function Table

Enable Inputs		Operation	
$\overline{G}$BA	GAB	'AS2620	'AS2623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

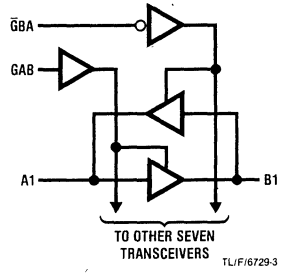
Logic Diagrams

'AS2620



TL/F/6729-2

'AS2623



TL/F/6729-3

Recommended Operating Conditions

Symbol	Parameter	DM54AS2620 DM54AS2623			DM74AS2620 DM74AS2623			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM54AS2620 DM54AS2623			DM74AS2620 DM74AS2623			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 1 mA			0.15	0.4		0.15	0.4	V
		V_{CC} = 4.5V, I_{OL} = 12 mA			0.35	0.7		0.35	0.7	V
I_I	Control Inputs	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
	A or B Ports	V_{CC} = 5.5V, V_I = 5.5V				0.1			0.1	mA
I_{IH}	Control Inputs	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
	A or B Ports (Note 3)					70			70	μA
I_{IL}	Control Inputs	V_{CC} = 5.5V, V_I = 0.4V				−0.5			−0.5	mA
	A or B Ports (Note 3)					−0.75			−0.75	mA
I_O (Note 2)	Output Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	−50		−150	mA
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_O = 2V		−35			−35			mA
I_{OL}	Low Level Output Current	V_{CC} = 4.5V, V_O = 2V		35			35			mA
I_{CC}	AS2620	V_{CC} = 5.5V	Outputs High		62	100		62	100	mA
			Outputs Low		74	121		74	121	mA
			Outputs Disabled		48	77		48	77	mA
	AS2623	V_{CC} = 5.5V	Outputs High		58	93		58	93	mA
			Outputs Low		116	189		116	189	mA
			Outputs Disabled		72	116		72	116	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

AS2620 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS2620			DM74AS2620			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	1		9.5	1		8	ns
t_{PHL}				1		7.5	1		6.5	ns
t_{PLH}	B	A		1		9.5	1		8	ns
t_{PHL}				1		7.5	1		6.5	ns
t_{PZH}	$\overline{G}$BA	A		1		11	1		10	ns
t_{PZL}				1		12	1		11	ns
t_{PHZ}	$\overline{G}$BA	A		1		7.5	1		6	ns
t_{PLZ}				1		15	1		12	ns
t_{PZH}	GAB	B		1		9	1		8	ns
t_{PZL}				1		9	1		8	ns
t_{PHZ}	GAB	B		1		12	1		11	ns
t_{PLZ}				1		12	1		11	ns

AS2623 Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS2623			DM74AS2623			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PLH}	A	B	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	1		9.5	1		8.5	ns
t_{PHL}				1		8.5	1		7.5	ns
t_{PLH}	B	A		1		10	1		9	ns
t_{PHL}				1		9	1		7.5	ns
t_{PZH}	$\overline{G}$BA	A		1		12.5	1		11	ns
t_{PZL}				1		12	1		11	ns
t_{PHZ}	$\overline{G}$BA	A		1		8.5	1		7.5	ns
t_{PLZ}				1		13	1		12	ns
t_{PZH}	GAB	B		1		13	1		12	ns
t_{PZL}				1		13.5	1		12	ns
t_{PHZ}	GAB	B		1		7.5	1		7	ns
t_{PLZ}				1		14.5	1		12.5	ns

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54AS2640/DM74AS2640, DM54AS2645/DM74AS2645 TRI-STATE® Bus Transceivers/MOS Drivers

General Description

This family of advanced low power Schottky devices contains 8 pairs of logic elements configured as octal bus transceivers. They are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous bidirectional communications between data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus are selectively controlled by (DIR and $\overline{G}$) the direction and enable inputs. This enable input is also used to disable the device so that the buses are effectively isolated.

Features

- Bidirectional octal bus transceivers for driving MOS devices
- I/O ports have 25Ω series resistors so no external resistors are required
- Choice of true or inverting logic
- Advanced oxide isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω/50 pF load
- Switching specifications guaranteed over full temperature and V_{CC} range

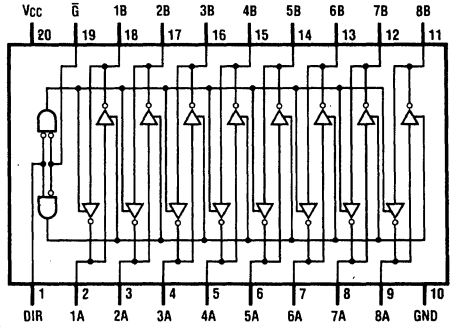
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package

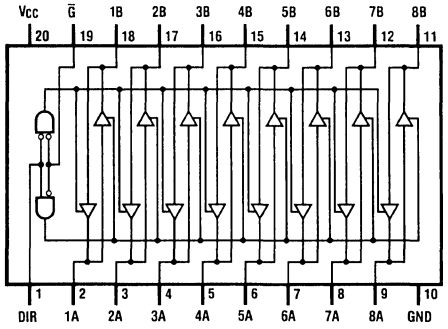


TL/F/6343-1

DM54AS2640 (J) **DM74AS2640 (J, N)**

Connection Diagrams (Continued)

Dual-In-Line Package



TL/F/6343-3

DM54AS2645 (J) **DM74AS2645 (J, N)**

Function Table

Control Inputs		Operation	
$\overline{G}$	DIR	AS2640	AS2645
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus
L	H	$\overline{A}$ Data to B Bus	A Data to B Bus
H	X	Hi-Z	Hi-Z

Recommended Operating Conditions

Symbol	Parameter	DM54AS			DM74AS			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
T_A	Operating Free Air Temperature	−55		125	0		70	°C

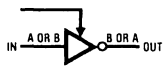
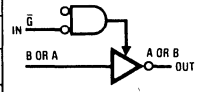
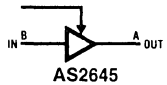
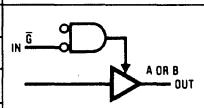
Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18$ mA				−1.2	V
V_{OH}	High Level Output Voltage	$I_{OH} = -2$ mA		$V_{CC} - 2$			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = -1$ mA		0.25	0.4	V
			$I_{OL} = 12$ mA		0.35	0.7	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$ ($V_{IN} = 5.5V$ for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−50		−150	mA
I_{CC}	DM54/74AS2640 Supply Current	$V_{CC} = 5.5V$	Outputs High		37	58	mA
			Outputs Low		78	123	mA
			TRI-STATE		51	80	mA
I_{CC}	DM54/74AS2645 Supply Current	$V_{CC} = 5.5V$	Outputs High		58	95	mA
			Outputs Low		95	155	mA
			TRI-STATE		73	119	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Circuit Configuration	DM54AS			DM74AS			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	 AS2640	1		9.5	1		7.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		1		7	1		6.5	ns
t_{PZL}	Output Enable Time to Low Level	 AS2640	2		11	2		9	ns
t_{PZH}	Output Enable Time to High Level		2		12	2		10	ns
t_{PLZ}	Output Disable Time from Low Level		1		8	1		7	ns
t_{PHZ}	Output Disable Time from High Level		2		15	2		13	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	 AS2645	1		12	1		10	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		1		11	1		9.5	ns
t_{PZL}	Output Enable Time to Low Level	 AS2645	1		13	1		11.5	ns
t_{PZH}	Output Enable Time to High Level		1		13	1		10.5	ns
t_{PLZ}	Output Disable Time from Low Level		1		9	1		8	ns
t_{PHZ}	Output Disable Time from High Level		1		13	1		12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are $V_{CC} = 4.5V$ to $5.5V$, $R_L = 500\Omega$, $C_L = 50$ pF.

Section 4

Low Power Schottky

4

Section Contents

Section Contents (Continued)

Section Contents (Continued)

National Semiconductor

DM54LS00/DM74LS00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

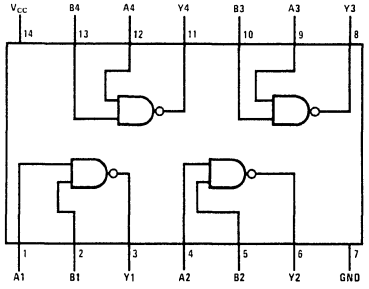
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6439-1

DM54LS00 (J) DM74LS00 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS00			DM74LS00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	5	10	4	8	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	5	10	4	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS01/DM74LS01 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

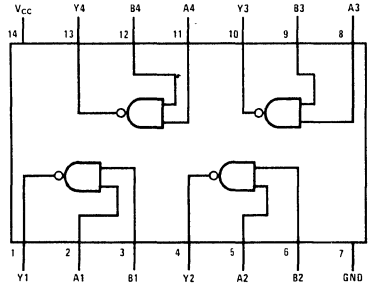
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6440-1

DM54LS01 (J) DM74LS01 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS01			DM74LS01			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	6	12	20	20	32	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	15	4	10	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS02/DM74LS02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

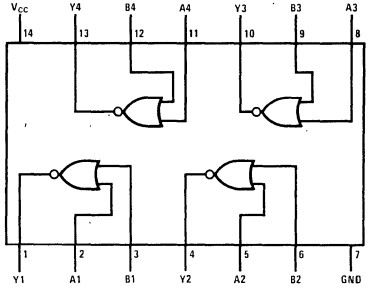
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6441-1

DM54LS02 (J) DM74LS02 (N)

Function Table

$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS02			DM74LS02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.6	3.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.8	5.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	9	13	4	12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	5	10	4	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS03/DM74LS03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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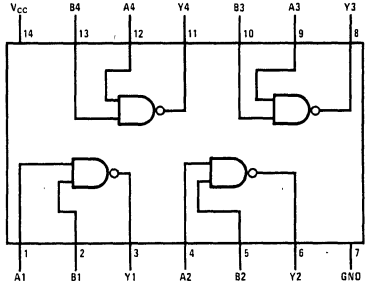
Connection Diagram

Dual-In-Line Package



TL/F/6344-1

DM54LS03 (J) DM74LS03 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS03			DM74LS03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	6	12	20	20	32	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	15	4	10	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS04/DM74LS04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

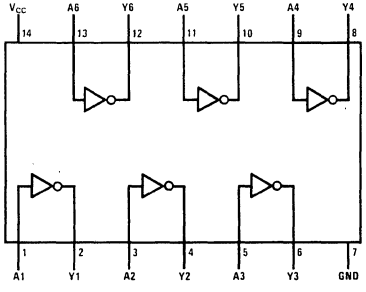
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6345-1

DM54LS04 (J) DM74LS04 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS04			DM74LS04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	5	10	4	8	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	5	10	4	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

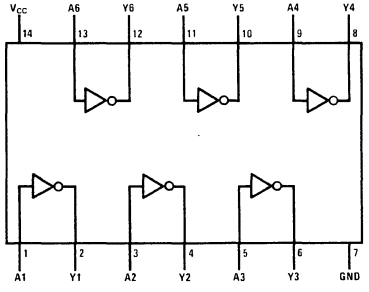
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6346-1

DM54LS05 (J) DM74LS05 (N)

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS05			DM74LS05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	6	12	20	20	32	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	15	4	10	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS08/DM74LS08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

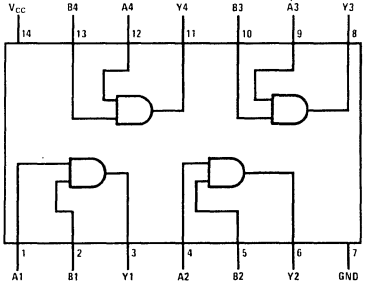
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6347-1

DM54LS08 (J) DM74LS08 (N)

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	4	8	13	6	11	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7.5	11	5	11	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS09/DM74LS09 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

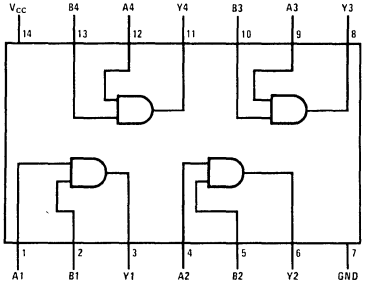
Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



TL/F/6348-1

DM54LS09 (J) DM74LS09 (N)

Function Table

$$Y = AB$$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS09			DM74LS09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	5	13	20	8	20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	4	10	15	6	18	27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS10/DM74LS10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

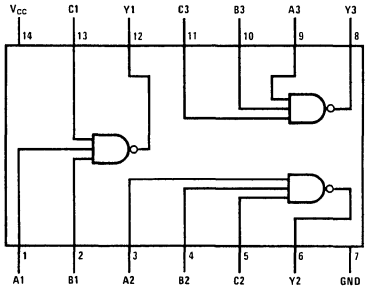
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6349-1

DM54LS10 (J) DM74LS10 (N)

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS10			DM74LS10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.6	1.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	5	10	4	8	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	5	10	4	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS11/DM74LS11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

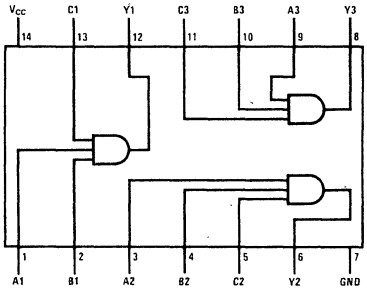
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6350-1

DM54LS11 (J) DM74LS11 (N)

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS11			DM74LS11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.8	3.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3.3	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	4	8	13	6	11	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7.5	11	5	11	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS12/DM74LS12 Triple 3-Input NAND Gates with Open-Collector Outputs

General Description

This device contains three independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

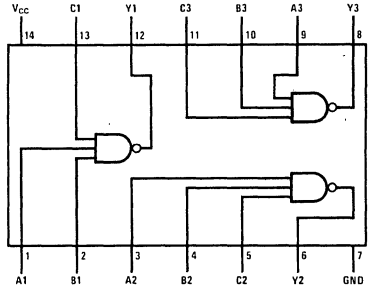
Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



TL/F/6351-1

DM54LS12 (J) DM74LS12 (N)

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS12			DM74LS12			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.7	1.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	6	12	20	20	32	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	15	4	10	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS13/DM74LS13 Dual 4-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains two independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

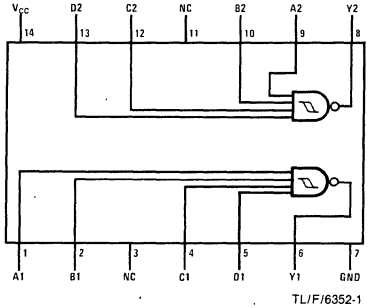
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6352-1

DM54LS13 (J) **DM74LS13 (N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS13			DM74LS13			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-} Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+} Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.18		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.9	6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.1	7	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 2\ k\Omega$						Units
	$C_L = 15\ pF$			$C_L = 50\ pF$			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	5	15	22	8	18	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	5	15	22	10	21	33	ns

National Semiconductor

DM54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

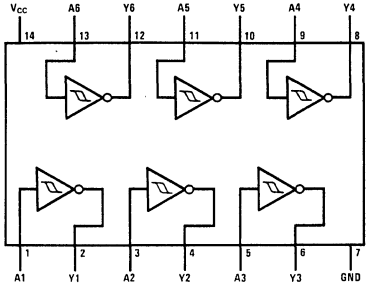
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6353-1

DM54LS14 (J) **DM74LS14 (N)**

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.18		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 2\ k\Omega$						Units
	$C_L = 15\ pF$			$C_L = 50\ pF$			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	5	15	22	8	18	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	5	15	22	10	21	33	ns

National Semiconductor

DM54LS15/DM74LS15 Triple 3-Input AND Gates with Open-Collector Outputs

General Description

This device contains three independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

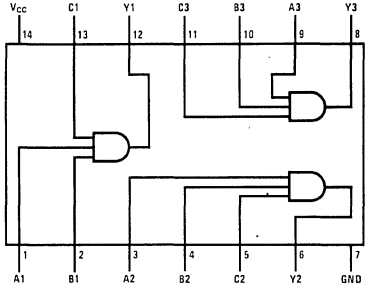
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6354-1

DM54LS15 (J) **DM74LS15 (N)**

Function Table

$$Y = ABC$$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS15			DM74LS15			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.8	3.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3.3	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	5	13	20	8	20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	4	10	15	6	18	27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS20/DM74LS20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

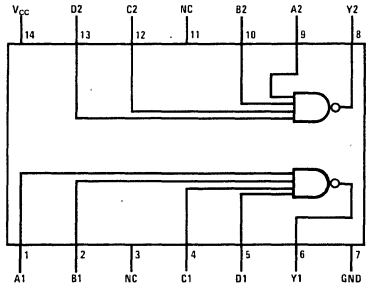
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6355-1

DM54LS20 (J) **DM74LS20 (N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS20			DM74LS20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.4	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.2	2.2	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	5	10	4	8	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	5	10	4	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS21/DM74LS21 Dual 4-Input AND Gates

General Description

This device contains two independent gates each of which performs the logic AND function.

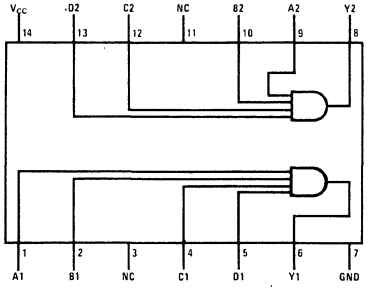
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6356-1

DM54LS21 (J) **DM74LS21 (N)**

Function Table

Y = ABCD

Inputs				Output
A	B	C	D	Y
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS21			DM74LS21			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.2	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	4	8	13	6	11	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7.5	11	5	11	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS22/DM74LS22 Dual 4-Input NAND Gates with Open-Collector Outputs

General Description

This device contains two independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

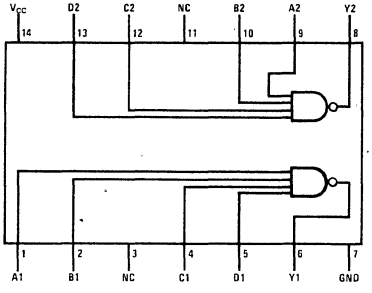
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6357-1

DM54LS22 (J) **DM74LS22 (N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS22			DM74LS22			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.4	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.2	2.2	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	6	12	20	20	32	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	15	4	10	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS26/DM74LS26 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

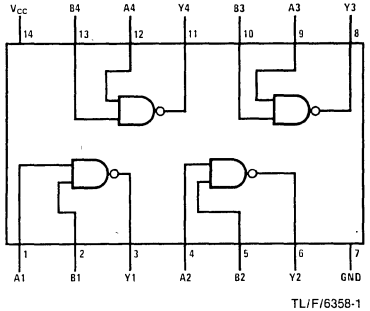
Supply Voltage	7V
Input Voltage	7V
Output Voltage	15V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



TL/F/6358-1

DM54LS26 (J) **DM74LS26 (N)**

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS26			DM74LS26			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{IL} = Max	V_O = 15V			1000	μA
			V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 2 kΩ, C_L = 15 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			17	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output			15	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS27/DM74LS27 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

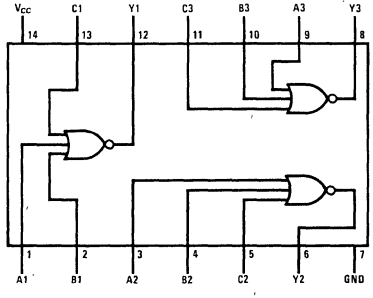
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6359-1

DM54LS27 (J) **DM74LS27 (N)**

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS27			DM74LS27			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3.4	6.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	9	13	5	12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	5	10	4	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS30/DM74LS30 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

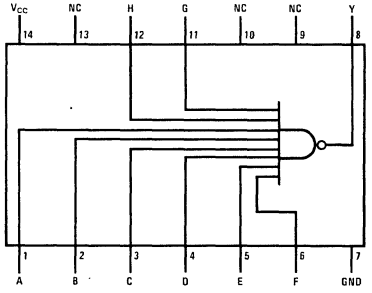
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6360-1

DM54LS30 (J) **DM74LS30 (N)**

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs A thru H	Output Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS30			DM74LS30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.35	0.5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.6	1.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	4	7	12	5	9	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	4	7	15	5	11	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS32/DM74LS32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

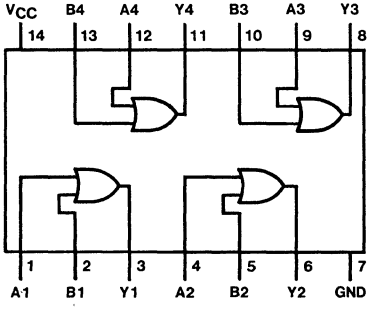
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6361-1

DM54LS32 (J) DM74LS32 (N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	7	11	4	10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	11	4	10	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS37/DM74LS37 Quad 2-Input NAND Buffers

General Description

This device contains four independent gates each of which performs the logic NAND function.

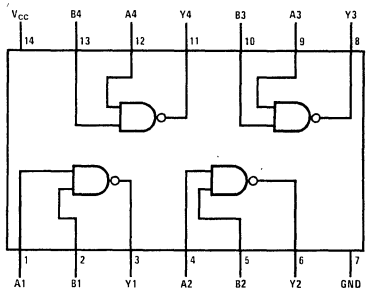
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6362-1

DM54LS37 (J) **DM74LS37 (N)**

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS37			DM74LS37			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			6	12	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 667Ω						Units
	C_L = 45 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	10	15	4	13	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	10	15	4	16	21	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS38/DM74LS38 Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

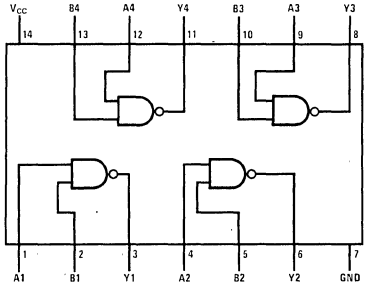
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6363-1

DM54LS38 (J) **DM74LS38 (N)**

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS38			DM74LS38			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			6	12	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 667Ω						Units
	C_L = 45 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		14	22		37	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output		12	22		22	29	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54LS40/DM74LS40 Dual 4-Input NAND Buffers

General Description

This device contains two independent gates each of which performs the logic NAND function.

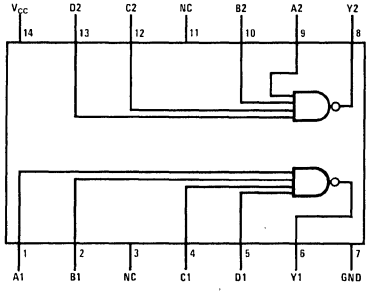
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6364-1

DM54LS40 (J) **DM74LS40 (N)**

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS40			DM74LS40			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.45	1	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 667Ω						Units
	C_L = 45 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	10	15	4	13	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	10	15	4	16	21	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS42/DM74LS42 BCD/Decimal Decoders

General Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 35 mW
- Typical propagation delay 17 ns

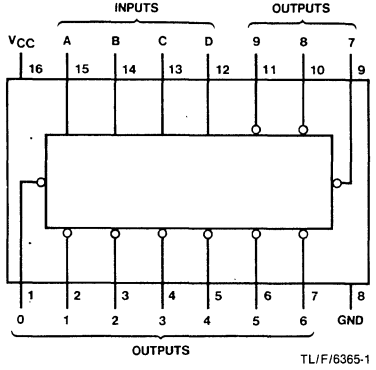
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6365-1

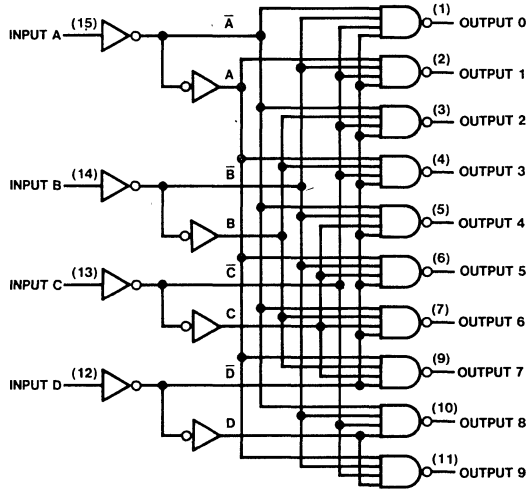
DM54LS42A (J) **DM74LS42A (N)**

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

Logic Diagram



TL/F/6365-2

Recommended Operating Conditions

Symbol	Parameter	DM54LS42			DM74LS42			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			7	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C, or D (2 Levels of Logic) to Output		14	25		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C, or D (3 Levels of Logic) to Output		17	30		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C, or D (2 Levels of Logic) to Output		10	25		15	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C, or D (3 Levels of Logic) to Output		17	30		23	35	ns

National Semiconductor

DM54LS47/DM74LS47, DM54LS48/DM74LS48, DM54LS49/DM74LS49 BCD/7-Segment Decoders/Drivers

General Description

The LS47 features active-low outputs designed for driving common-anode LEDs or incandescent indicators directly; and the LS48 and LS49 feature active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits except the LS49 have full ripple-blanking input/output controls and a lamp test input. The LS49 features a direct blanking input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

All of the circuits except the LS49 incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types (including LS49) contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing), or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability

54LS47/74LS47

- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

54LS48/74LS48

- Internal pull-ups eliminate need for external resistors
- Lamp-test provision
- Leading/trailing zero suppression

54LS49/74LS49

- Open-collector outputs
- Blanking input

Absolute Maximum Ratings (Note 1)

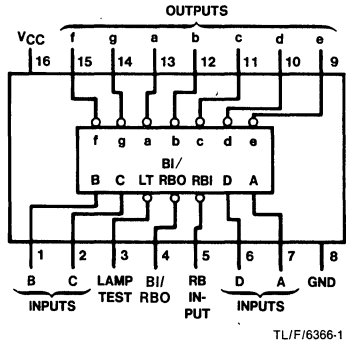
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Type	Driver Outputs				Typical Power Dissipation	Packages
	Active Level	Output Configuration	Sink Current	Max Voltage		
DM54LS47	low	open-collector	12 mA	15 V	35 mW	J
DM54LS48	high	2 kΩ pull-up	2 mA	5.5 V	125 mW	J
DM54LS49	high	open-collector	4 mA	5.5 V	40 mW	J
DM74LS47	low	open-collector	24 mA	15 V	35 mW	N
DM74LS48	high	2 kΩ pull-up	6 mA	5.5 V	125 mW	N
DM74LS49	high	open-collector	8 mA	5.5 V	40 mW	N

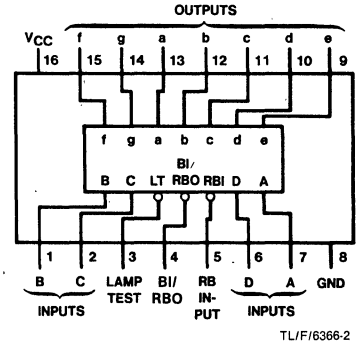
Connection Diagrams

Dual-In-Line Packages



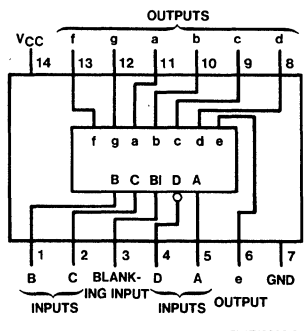
TL/F/6366-1

54LS47 (J) 74LS47 (N)



TL/F/6366-2

54LS48 (J) 74LS48 (N)



TL/F/6366-3

54LS49 (J) 74LS49 (N)

Recommended Operating Conditions

Symbol	Parameter	DM54LS47			DM74LS47			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−50			−50	μA
I_{OL}	Low Level Output Current (a thru g)			12			24	mA
	Low Level Output Current (BI/RBO)			1.6			3.2	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS47 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	4.2		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Min, V_O = 15V V_{IL} = Max				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = Max/2 V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−1	mA
			Others			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)		−0.3		−2	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			7	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'LS47 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 665\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Output			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Output			100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	RBI to Output			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	RBI to Output			100	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS48			DM74LS48			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			5.5			5.5	V
I_{OH}	High Level Output Current (BI/RBO)			−50			−50	μA
	High Level Output Current (a thru g)			−100			−100	
I_{OL}	Low Level Output Current (a thru g)			2			6	mA
	Low Level Output Current (BI/RBO)			1.6			3.2	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS48 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	4.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.24	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 2 mA V_{CC} = Min	DM74		0.25	0.4	
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_{IH} = Min V_{IL} = Max, V_O = 0.85V		−1.3	−2		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V (Any Input except BI/RBO)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Any Input except BI/RBO)				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−1	mA
			Others			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−0.3		−2	mA
			DM74	−0.3		−2	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			25	38	mA

'LS48 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	C_L = 15 pF						Units
		R_L = 4 kΩ			R_L = 6 kΩ			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Output			100				ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Output			100				ns
t_{PLH} Propagation Delay Time Low to High Level Output	RBI to Output						100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	RBI to Output						100	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs at 4.5V.

Recommended Operating Conditions

Symbol	Parameter	DM54LS49			DM74LS49			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS49 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			8	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

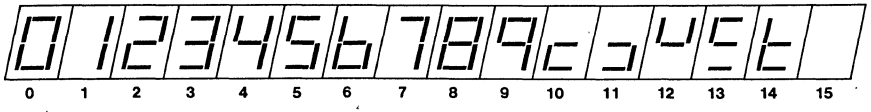
'LS49 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$C_L = 15$ pF						Units
		$R_L = 2\ k\Omega$			$R_L = 6\ k\Omega$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Output			100				ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Output			100				ns
t_{PLH} Propagation Delay Time Low to High Level Output	BI to Output						100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	BI to Output						100	ns

Output Display

Numerical Designations and Resultant Displays



Segment Identification

TL/F/6366-4

Function Tables

LS47

Decimal or Function	Inputs						BI/RBO(1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	(2)
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	L	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(3)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(4)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(5)

Function Tables (Continued)

LS48

Decimal or Function	Inputs						BI/RBO(1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	(2)
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	(3)
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	(4)
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	(5)

LS49

Decimal or Function	Inputs					Outputs							Note
	D	C	B	A	BI	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	(6)
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	(7)

H = High level, L = Low level, X = Don't Care

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 2: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

Note 3: When a low logic level is applied directly to the blanking input (BI), all segment outputs are H (46, 47); L (48) regardless of the level of any other input.

Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

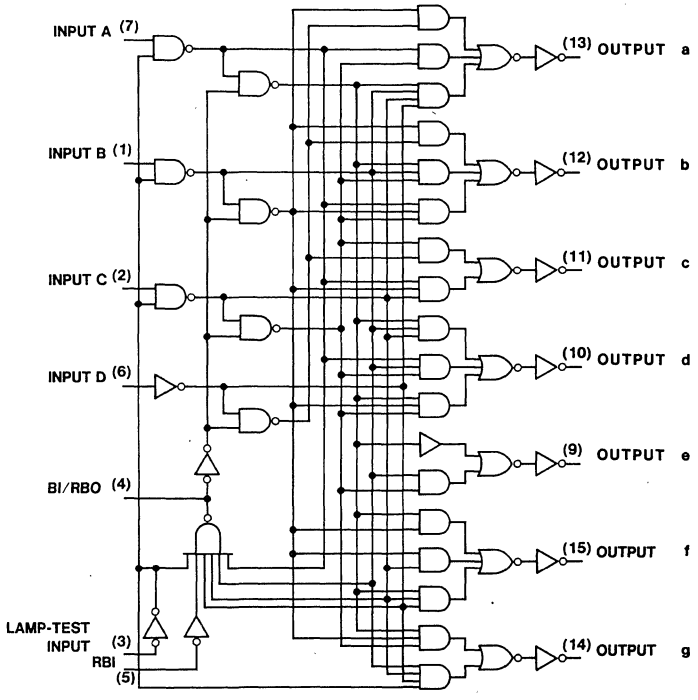
Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

Note 6: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.

Note 7: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

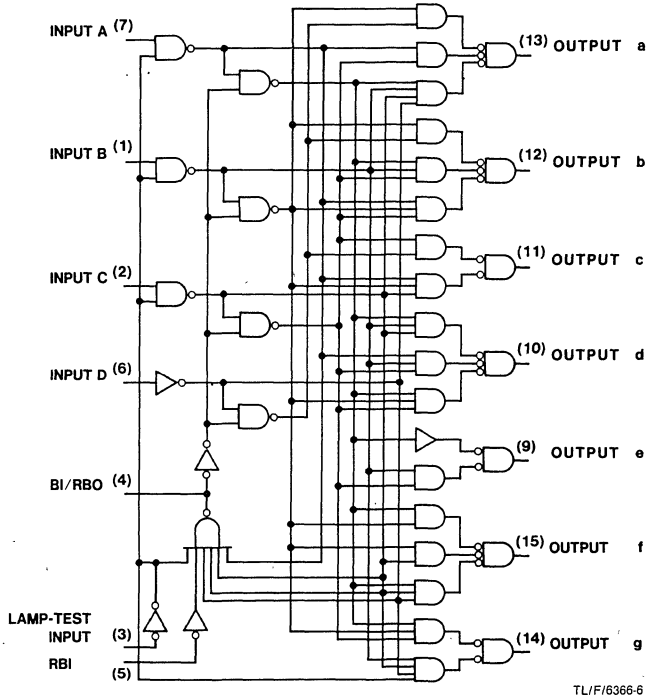
Logic Diagrams

LS47



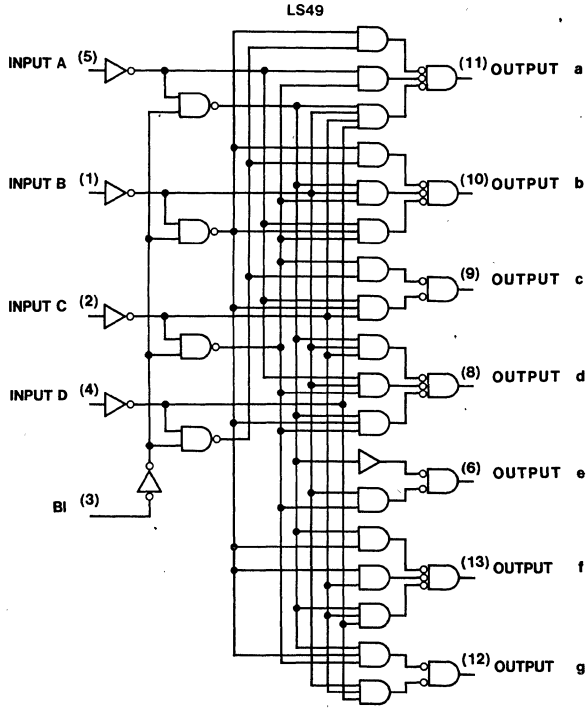
TL/F/6366-5

LS48



TL/F/6366-6

Logic Diagrams (Continued)



TL/F/6366-7

National Semiconductor

DM54LS51/DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

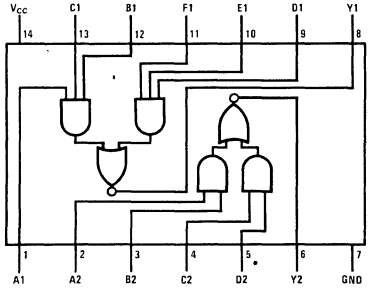
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6369-1

DM54LS51 (J) **DM74LS51 (N)**

Function Table

$$Y1 = \overline{(A1)\,(B1)\,(C1) + (D1)\,(E1)\,(F1)}$$

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Other Combinations						H

$$Y2 = \overline{((A2)\,(B2) + (C2)\,(D2))}$$

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	L
X	X	H	H	L
Other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS51			DM74LS51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.4	2.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	9	13	4	12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	6	12	3	8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS54/DM74LS54 4-Wide AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

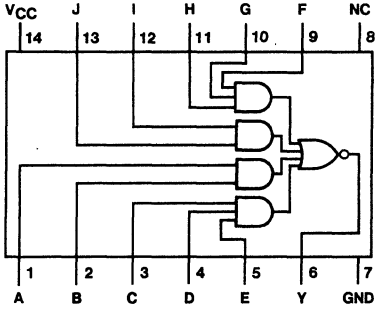
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6370-1

DM54LS54 (J) **DM74LS54 (N)**

Function Table

$$Y = \overline{AB = CDE + FGH + IJ}$$

Inputs										Output
A	B	C	D	E	F	G	H	I	J	Y
H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	X	X	L
X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	H	H	L
All other combinations										H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS54			DM74LS54			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1	2	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	5	15	20	6	18	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	7	13	4	10	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS55/DM74LS55 2-Wide 4-Input AND-OR-INVERT Gates

General Description

This device contains a combination of gates which perform the logic AND-OR-INVERT function.

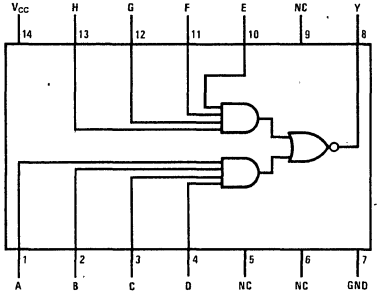
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6371-1

DM54LS55 (J) **DM74LS55 (N)**

Function Table

$$Y = \overline{ABCD + EFGH}$$

Inputs								Output
A	B	C	D	E	F	G	H	Y
H	H	H	H	X	X	X	X	L
X	X	X	X	H	H	H	H	L
All other combinations								H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54LS55			DM74LS55			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.4	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.7	1.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 2 kΩ						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	9	13	4	12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	6	12	3	10	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS73A/DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

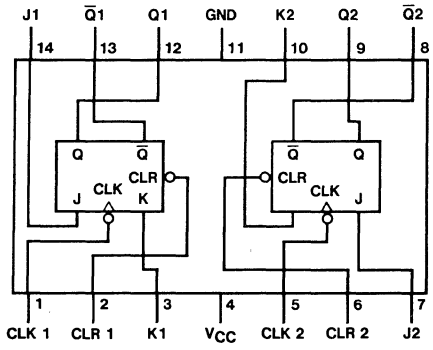
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6372-1

DM54LS73A (J) **DM74LS73A (N)**

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_O	$\overline{Q}_O$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative going edge of pulse

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM54LS73A			DM74LS73A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

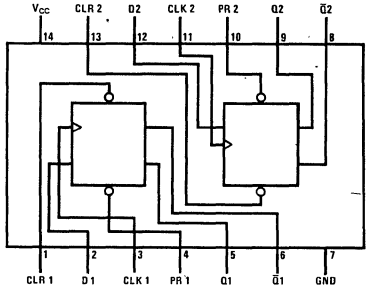
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6373-1

DM54LS74A (J) **DM74LS74A (N)**

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

Recommended Operating Conditions

Sym	Parameter		DM54LS74A			DM74LS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 and 2)		20↑			20↑			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↑			25↑			ns
t_H	Hold Time		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 7V	Data			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Data			20	μA
			Clock			20	
			Clear			40	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Data			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	33		20	28		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		22	30		26	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		22	30		26	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		22	30		26	35	ns

National Semiconductor

DM54LS75/DM74LS75 Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

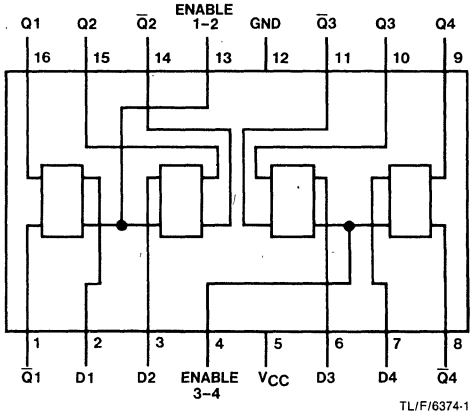
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6374-1

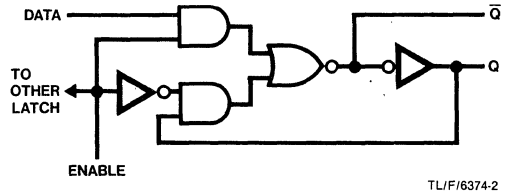
DM54LS75 (J) **DM74LS75 (N)**

Function Table (Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care
Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)



TL/F/6374-2

Recommended Operating Conditions

Sym	Parameter	DM54LS75			DM74LS75			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
t_W	Enable Pulse Width	20			20			ns
t_{SU}	Setup Time	20			20			ns
t_H	Hold Time	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.5		V
			DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D			0.1	mA
			G			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			20	μA
			G			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D			−0.4	mA
			G			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	D to Q		15	27		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to Q		9	17		14	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		10	20		13	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		8	15		10	20	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to Q		15	27		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to Q		14	25		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to $\overline{Q}$		16	30		18	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to $\overline{Q}$		7	15		10	20	ns

National Semiconductor

DM54LS76A/DM74LS76A Dual Negative-Edge-Triggered J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is accepted by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock. Data on the J and K inputs may be changed while the clock is low or high without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

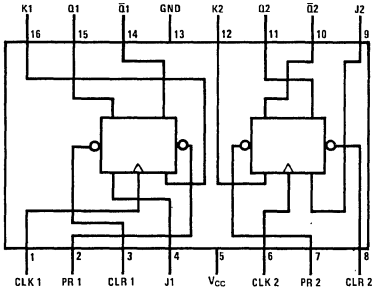
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6375-1

DM54LS76A (J) **DM74LS76A (N)**

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

L = Low Logic Level

↓ = Negative Going Transition

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active (↓) of the clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM54LS76A			DM74LS76A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			20	μA
			Clear			60	
			Preset			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−0.4	mA
			Preset			−0.8	
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

National Semiconductor

DM54LS77/DM74LS77 Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

For higher component density applications, the DM54LS77/DM74LS77 4-bit latches are available in 14-pin flat packages (only).

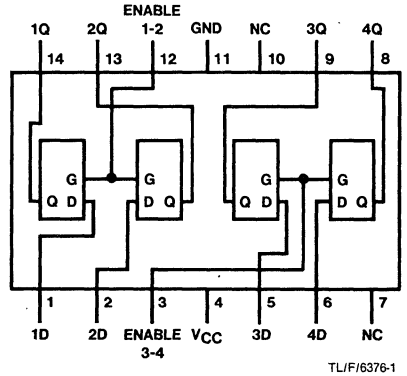
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Flat Package



TL/F/6376-1

54LS77 (W) 74LS77 (W)

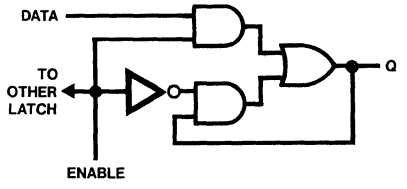
Function Table

(Each Latch)

Inputs		Outputs
D	G	Q
L	H	L
H	H	H
X	L	Q_0

H = High Level, L = Low Level, X = Don't Care
Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)



TL/F/6376-2

Recommended Operating Conditions

Sym	Parameter	DM54LS77			DM74LS77			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
t_W	Enable Pulse Width	20			20			ns
t_{SU}	Setup Time	20			20			ns
t_H	Hold Time	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	D Input			0.1	mA
			G Input			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D Input			20	μA
			G Input			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D Input			−0.4	mA
			G Input			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.9	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	D to Q		15	27		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to Q		9	17		14	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to Q		15	27		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to Q		17	25		20	30	ns

National Semiconductor

DM54LS78A/DM74LS78A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Common Clear, Common Clock and Complementary Outputs

General Description

This device contains two negative-edge triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

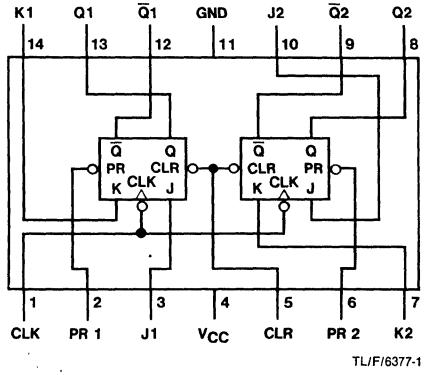
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6377-1

DM54LS78A (J) DM74LS78A (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\bar{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\bar{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM54LS78A			DM74LS78A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.2	
			Preset			0.2	
			Clock			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			120	
			Preset			60	
			Clock			160	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 4)	J, K			−0.4	mA
			Clear			−1.6	
			Preset			−0.8	
			Clock			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

National Semiconductor

DM54LS83A/DM74LS83A 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 25 ns
  Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

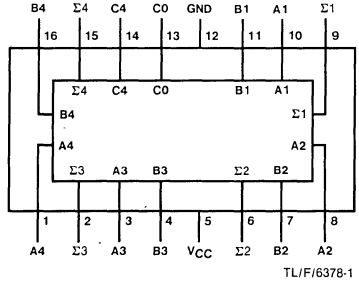
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams and Truth Table

Dual-In-Line Package



TL/F/6378-1

54LS83A (J) 74LS83A (N)

Input				Output					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs Σ3, Σ4, and C4.

Recommended Operating Conditions

Sym	Parameter	DM54LS83A			DM74LS83A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	A or B			0.2	mA
			C0			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A or B			40	μA
			C0			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A or B			−0.8	mA
			C0			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

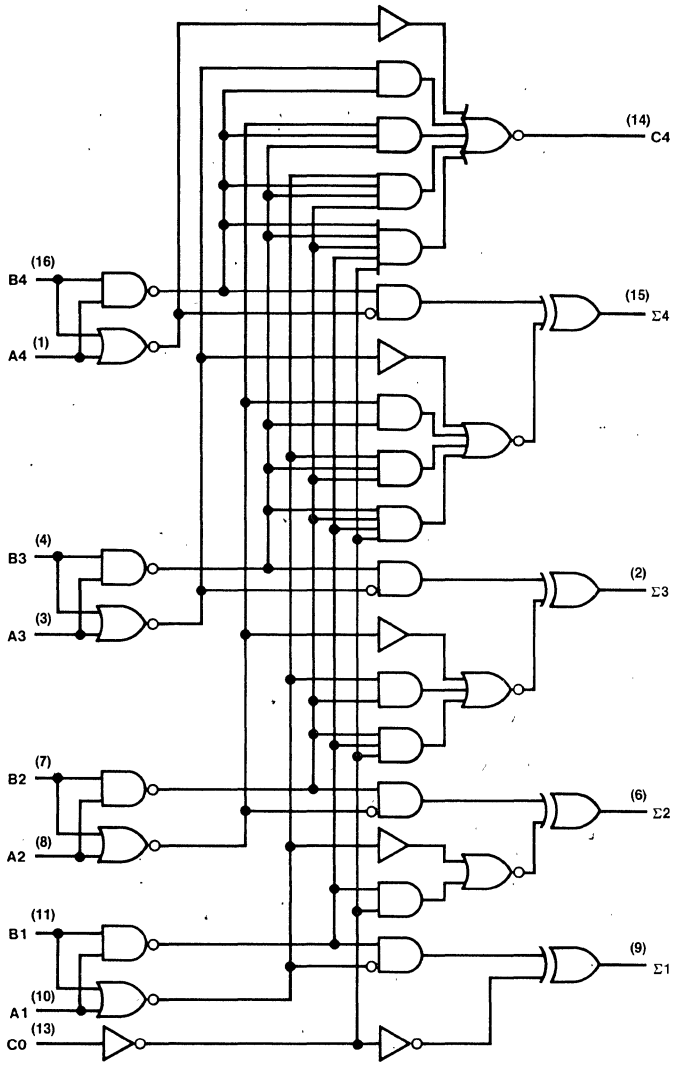
Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ1 or Σ2		16	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ1 or Σ2		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ3		16	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ3		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ4		16	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ4		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Ai or Bi to Σi		15	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Ai or Bi to Σi		15	24		19	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to C4		11	17		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to C4		11	17		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Ai or Bi to C4		11	17		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Ai or Bi to C4		12	17		17	26	ns

Logic Diagram



TL/F/6378-2

National Semiconductor

DM54LS85/DM74LS85 4-Bit Magnitude Comparators

General Description

These four-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns

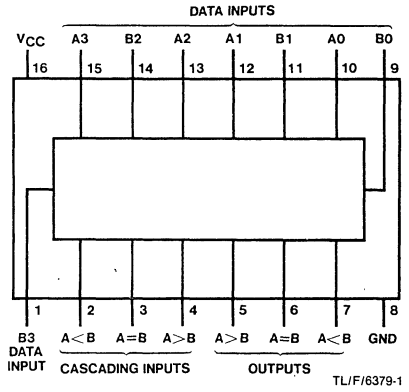
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6379-1

54LS85 (J) **74LS85 (N)**

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Sym	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	A < B			0.1	mA
			A > B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A < B			20	μA
			A > B			20	
			Others			60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A < B			−0.4	mA
			A > B			−0.4	
			Others			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			10	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

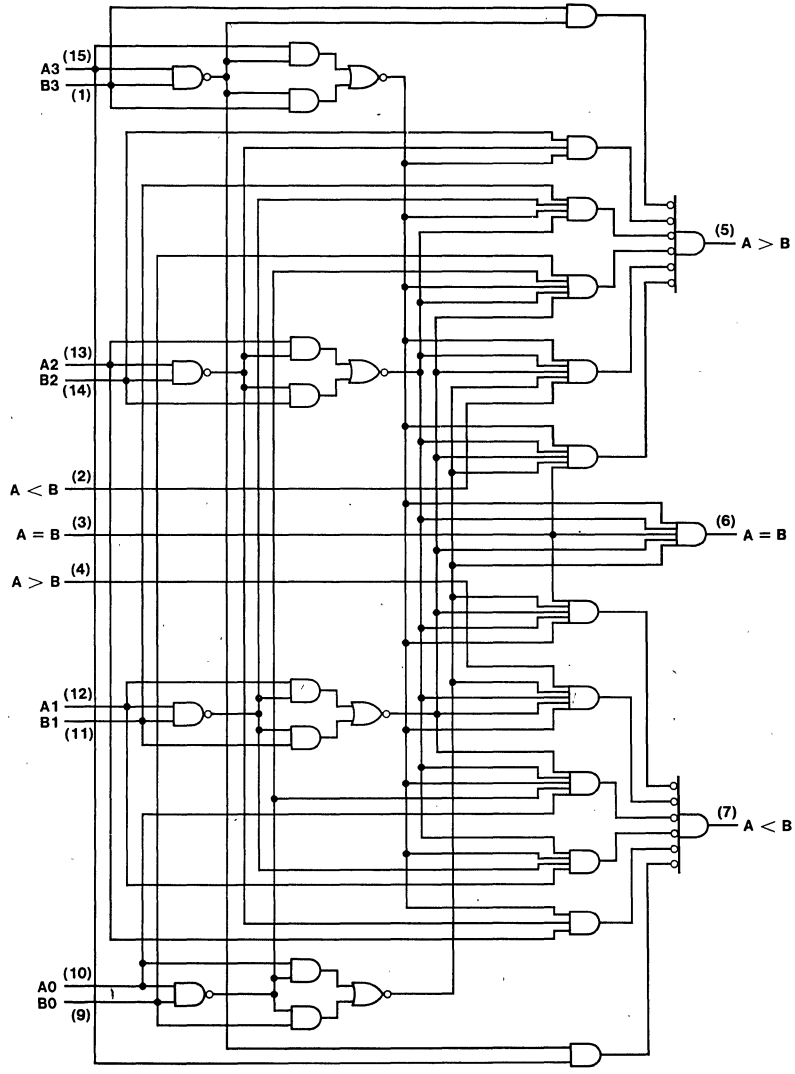
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From Input	To Output	Number of Gate Levels	$R_L = 2\ k\Omega$						Units
				$C_L = 15\ pF$			$C_L = 50\ pF$			
				Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	1		14			17		ns
			2		19			22		
			3		24	36		27	42	
		A = B	4		23	40		26	40	
t_{PHL} Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	1		11			17		ns
			2		15			21		
			3		20	30		26	40	
		A = B	4		20	30		26	40	
t_{PLH} Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		14	22		17	26	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		11	17		17	26	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		13	20		16	25	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		11	17		17	26	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		14	22		17	26	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		11	17		17	26	ns

Logic Diagram



TL/F/6379-2

National Semiconductor

DM54LS86/DM74LS86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

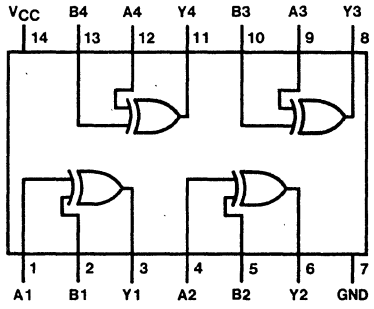
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6380-1

DM54LS86 (J) **DM74LS86 (N)**

Function Table

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS86			DM74LS86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low		12	18		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output			10	17		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High		7	10		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output			6	12		10	15	ns

National Semiconductor

DM54LS90/DM74LS90, DM54LS92/DM74LS92, DM54LS93/DM74LS93 Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the LS90, divide-by-six for the LS92, and divide-by-eight for the LS93.

All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

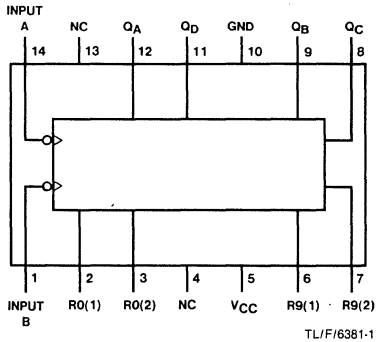
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Storage Temperature Range	−65°C to 150°C

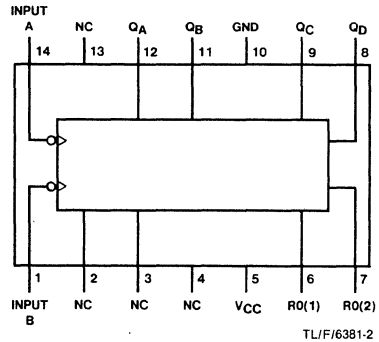
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams (Dual-In-Line Packages)



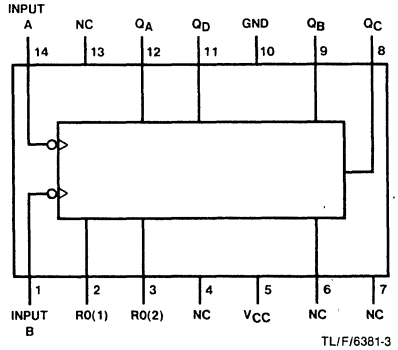
TL/F/6381-1

54LS90 (J) 74LS90 (N)



TL/F/6381-2

54LS92 (J) 74LS92 (N)



TL/F/6381-3

54LS93 (J) 74LS93 (N)

Function Tables

LS90
BCD COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
BI-QUINARY (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS92
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

LS93
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LS90
RESET/COUNT TRUTH TABLE

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS92,LS93
RESET/COUNT TRUTH TABLE

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.
Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

Recommended Operating Conditions

Sym	Parameter		DM54LS90			DM74LS90			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 1)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_W	Pulse Width (Note 2)	A	25			25			ns
		B	50			50			
		Reset	25			25			
t_{REL}	Reset Release Time (Note 1)		25			25			ns
t_{REL}	Reset Release Time (Note 2)		35			35			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

'LS90 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'LS90 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		20	30		MHz
	B to Q_B	16			10			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18		18	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48		35	52	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50		40	60	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32		25	37	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35		25	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35		29	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		20	30		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		26	40		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40		35	52	ns

Recommended Operating Conditions

Sym	Parameter		DM54LS92			DM74LS92			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 1)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_W	Pulse Width (Note 2)	A	25			25			ns
		B	50			50			
		Reset	25			25			
t_{REL}	Reset Release Time (Note 1)		25			25			ns
t_{REL}	Reset Release Time (Note 2)		35			35			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

'LS92 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current With	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'LS92 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		20	30		MHz
	B to Q_B	16			10			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18		18	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48		35	52	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50		40	60	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		10	16		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35		29	44	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40		35	52	ns

Recommended Operating Conditions

Sym	Parameter		DM54LS93			DM74LS93			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 1)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_W	Pulse Width (Note 2)	A	25			25			ns
		B	50			50			
		Reset	25			25			
t_{REL}	Reset Release Time (Note 1)		25			25			ns
t_{REL}	Reset Release Time (Note 2)		35			35			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

'LS93 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current With	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

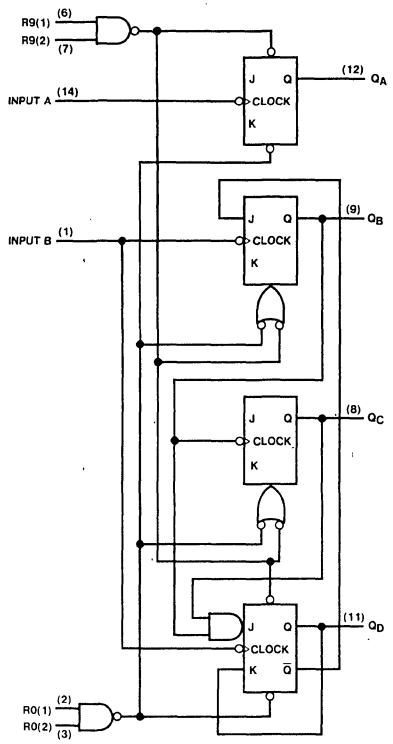
'LS93 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		20	30		MHz
	B to Q_B	16			10			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18		18	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		46	70		55	85	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		46	70		60	90	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32		25	37	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35		29	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		34	51		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		34	51		46	70	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40		35	52	ns

Logic Diagrams

LS90



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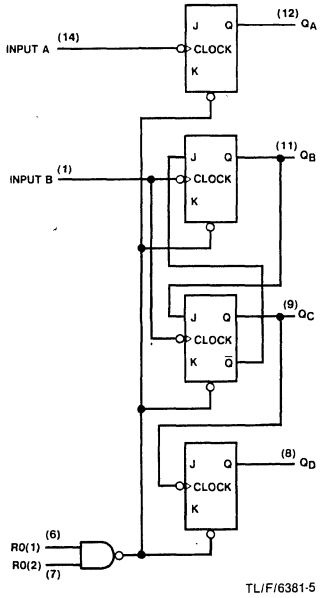
LS92



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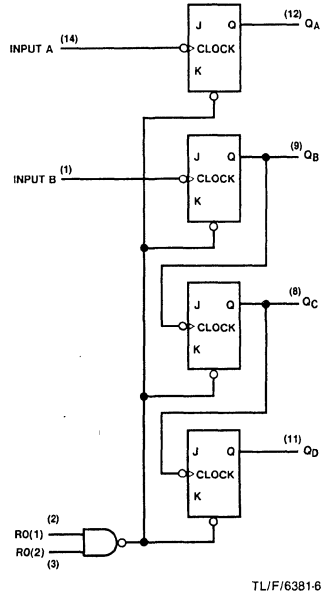
LS93



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The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor

DM54LS107A/DM74LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

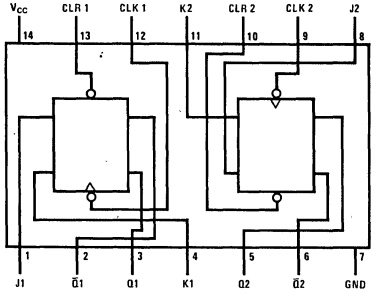
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6369-1

DM54LS107A (J) DM74LS107A (N)

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_O	$\overline{Q}_O$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Symbol	Parameter		DM54LS107A			DM74LS107A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current With	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

DM54LS109A/DM74LS109A Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

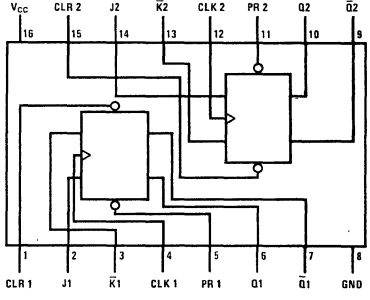
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6368-1

DM54LS109A (J) DM74LS109A (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_O	$\overline{Q}_O$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↑ = Rising Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Recommended Operating Conditions

Symbol	Parameter		DM54LS109A			DM74LS109A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 and 2)	Data High	30↑			30↑			ns
		Data Low	20↑			20↑			
t_{SU}	Setup Time (Notes 1 and 3)	Data High	35↑			35↑			ns
		Data Low	25↑			25↑			
t_H	Hold Time		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	J, $\overline{K}$			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, $\overline{K}$			20	μA
			Clock			20	
			Preset			40	
			Clear			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, $\overline{K}$			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	33		20	28		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		22	30		26	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		22	30		26	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		22	30		26	35	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: I_{CC} is measured with all outputs open, with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

National Semiconductor

DM54LS112A/DM74LS112A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

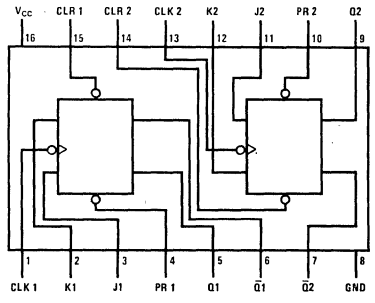
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6382-1

DM54LS112A (J) DM74LS112A (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\bar{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\bar{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Symbol	Parameter		DM54LS112A			DM74LS112A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

Electrical Characteristics (Continued)

over recommended operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Preset			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Preset			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current With	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

DM54LS113A/DM74LS113A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset input will set the outputs regardless of the other inputs.

Absolute Maximum Ratings (Note 1)

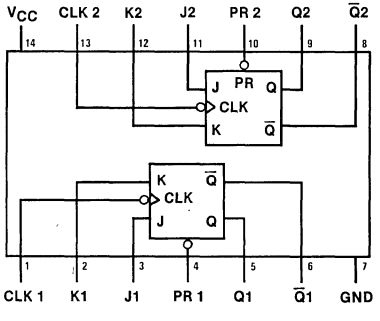
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



TL/F/6383-1

DM54LS113A (J) **DM74LS113A (N)**

Function Table

Inputs				Outputs	
PR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_O	$\bar{Q}_O$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_O	$\bar{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Symbol	Parameter		DM54LS113A			DM74LS113A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Preset			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Preset			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Preset			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current With	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

DM54LS114A/DM74LS114A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Common Clear, Common Clock and Complementary Outputs

General Description

This device contains two negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

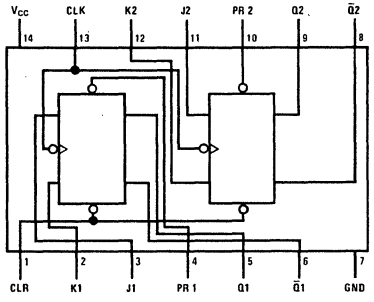
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6384-1

DM54LS114A (J) DM74LS114A (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions

Symbol	Parameter		DM54LS114A			DM74LS114A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.6	
			Preset			0.3	
			Clock			0.8	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			120	
			Preset			60	
			Clock			160	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−1.6	
			Preset			−0.8	
			Clock			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current With	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		25	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		11	20		21	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		15	20		18	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		11	20		21	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

DM54LS122/DM74LS122 Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74LS122 is a retriggerable monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 10 kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. The 'LS122 has two active-low transition triggering inputs (A), two active-high transition triggering inputs (B), and a CLEAR input that terminates the output pulse width at a predetermined time independent of the timing components. The (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⊓⊔). To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Over-Riding clear terminates output pulse
- Internal 10 kΩ timing resistor
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

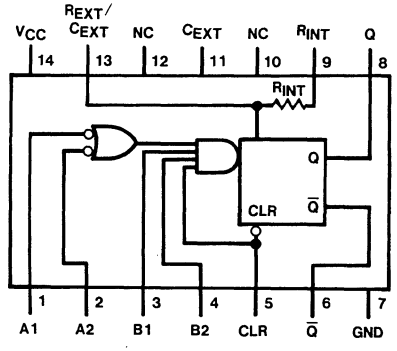
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Functional Description

The basic output pulse width is determined by selection of the internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered the output pulse width may be extended by retgriggering the gated active-low (A) transition inputs or the active-high transition (B) inputs or the CLEAR input. The output pulse width can be reduced or terminated by overriding it with the active-low CLEAR input.

Connection Diagram

Dual-In-Line Package



TL/F/6385-1

DM54LS122 (J) DM74LS122 (N)

Function Table

Inputs					Outputs	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⊓⊔	⊔⊓
H	L	X	H	↑	⊓⊔	⊔⊓
H	X	L	↑	H	⊓⊔	⊔⊓
H	X	L	H	↑	⊓⊔	⊔⊓
H	H	↓	H	H	⊓⊔	⊔⊓
H	↓	↓	H	H	⊓⊔	⊔⊓
H	↓	H	H	H	⊓⊔	⊔⊓
↑	L	X	H	H	⊓⊔	⊔⊓
↑	X	L	H	H	⊓⊔	⊔⊓

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High Level
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓⊔ = A Positive Pulse
⊔⊓ = A Negative Pulse

4

Recommended Operating Conditions

Symbol	Parameter		DM54LS122			DM74LS122			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	A or B High	40			40			ns
		A or B Low	40			40			
		Clear Low	40			40			
R_{EXT}	External Timing Resistor		5		180	5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50			50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3, 4 and 5)			6	11	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) to (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$, $C_{EXT} = 0\ pF$, $R_{EXT} = 5\ k\Omega$			$C_L = 15\ pF$, $C_{EXT} = 1000\ pF$, $R_{EXT} = 10\ k\Omega$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q		22	33				ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q		29	44				ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		30	45				ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		37	56				ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		30	45				ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		18	27				ns
$t_{WQ(Min)}$ Minimum Width of Pulse at Output Q	A or B to Q		116	200				ns
$t_{W(out)}$ Output Pulse Width	A or B to Q				4	4.5	5	μs

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

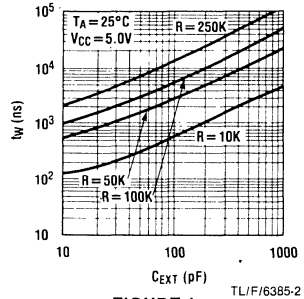
Operating Rules

1. To use the internal 10 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (10 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.

Operating Rules (Continued)

3. The pulse width is essentially determined by external timing components R_X and C_X. For $C_X < 1000$ pF see *Figure 1*; design curves on T_W as function of timing components value. For $C_X >> 1000$ pF the output is defined as:

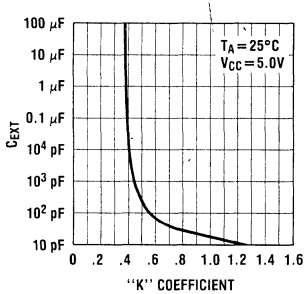
$T_W = KR_XC_X$
where $[R_X$ is in kΩ$]$
$[C_X$ is in pF$]$
$[T_W$ is in ns$]$
$K \approx 0.37$



TL/F/6385-2

FIGURE 1

The K factor is not a constant, but, varies with C_X. See *Figure 2*.

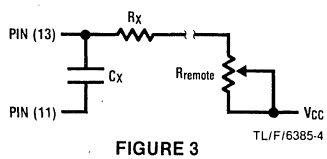


TL/F/6385-3

FIGURE 2

4. The switching diode required for most TTL one-shots when using an electrolytic timing capacitor is not needed for the 'LS122 and should not be used.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6385-4

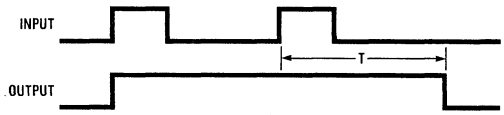
FIGURE 3

Note: "R_{remote}" should be as close to the device pins as possible.

6. The retriggerable pulse width is calculated as shown below:

$T = T_W + t_{PLH} = 0.50 \times R_X \times C_X + t_{PLH}$

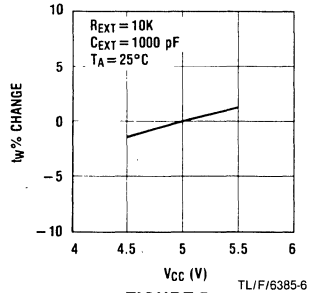
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 4)*.



TL/F/6385-5

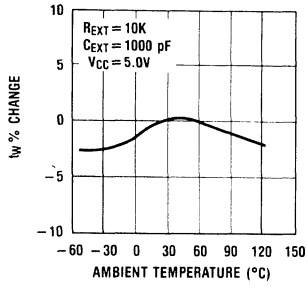
FIGURE 4

7. Output pulse width variation versus V_{CC} and operation temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}; and *Figure 6* depicts pulse width variation versus temperatures.



TL/F/6385-6

FIGURE 5



TL/F/6385-7

FIGURE 6

8. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (13) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation such that the output pulse width will be accurate.

9. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

*For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-366.

National Semiconductor

DM54LS123/DM74LS123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⊓⊔). To obtain the best trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Compensated for V_{CC} and temperature variations
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

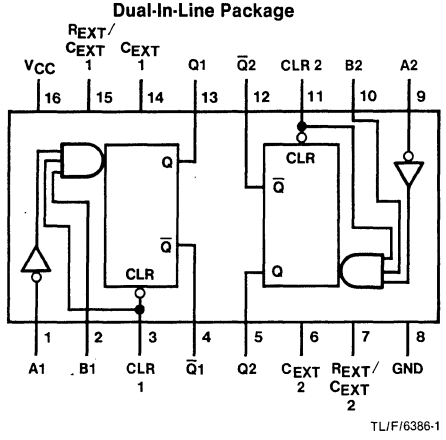
Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low or CLEAR input. Retriggering to 100% duty cyle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

4

Connection Diagram

Dual-In-Line Package



TL/F/6386-1

DM54LS123 (J) DM74LS123 (N)

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓⊔	⊔⊓
H	↓	H	⊓⊔	⊔⊓
↑	L	H	⊓⊔	⊔⊓

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓⊔ = A Positive Pulse
⊔⊓ = A Negative Pulse

Recommended Operating Conditions

Symbol	Parameter		DM54LS123			DM74LS123			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	A or B High	40			40			ns
		A or B Low	40			40			
		Clear Low	40			40			
R_{EXT}	External Timing Resistor		5		180	5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50			50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3, 4 and 5)			12	20	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

Parameter	From (Input) to (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$, $C_{EXT} = 0\ pF$, $R_{EXT} = 5\ k\Omega$			$C_L = 15\ pF$, $C_{EXT} = 1000\ pF$, $R_{EXT} = 10\ k\Omega$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q		22	33				ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q		29	44				ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		30	45				ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		37	56				ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		30	45				ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		18	27				ns
$t_{WQ(Min)}$ Minimum Width of Pulse at Output Q	A or B to Q		116	200				ns
$t_{W(out)}$ Output Pulse Width	A or B to Q				4	4.5	5	μs

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.

2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation.

3. For $C_X >> 1000$ pF the output pulse width (T_W) is defined as follows:

$$T_W = KR_XC_X$$

where $[R_X$ is in kΩ$]$
$[C_X$ is in pF$]$
$[T_W$ is in ns$]$
$K \approx 0.37$

4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

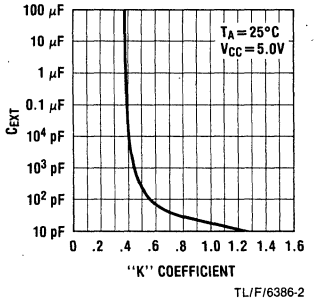


FIGURE 1

5. For $C_X < 1000$ pF see *Figure 2* for T_W vs C_X family curves with R_X as a parameter:

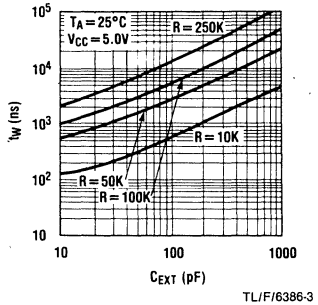


FIGURE 2

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:

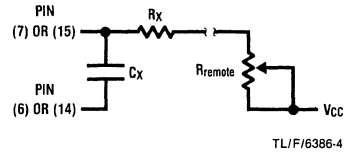


FIGURE 3

Note: "R_{remote}" should be as close to the one-shot as possible.

7. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$$

The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 4)*.

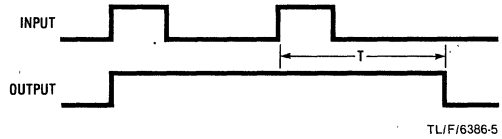


FIGURE 4

8. Output pulse width variation versus V_{CC} and temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}, and *Figure 6* depicts pulse width variation versus temperatures.

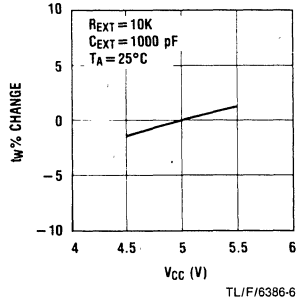


FIGURE 5

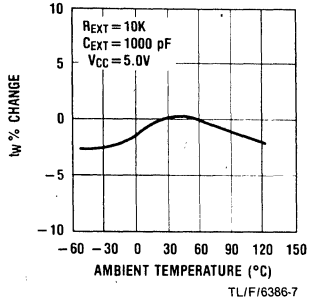


FIGURE 6

Operating Rules (Continued)

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation such that the output pulse width will be accurate.

10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.

*However, it should be noted that although the 'LS221 series one-shot is pin-for-pin compatible with the 'LS123 device, its C_{EXT} pin is not an internal connection to ground. Hence, if substitution of an 'LS221 on to an 'LS123 design layout whose C_{EXT} pin is wired to the ground is attempted, the 'LS221 device will not function!

11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01μF to 0.10μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

*For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-366.

National Semiconductor

DM54LS125A/DM74LS125A Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

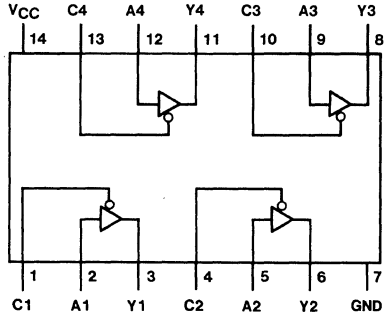
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6387-1

DM54LS125A (J) DM74LS125A (N)

Function Table

Y = A

Input		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Symbol	Parameter	DM54LS125A			DM74LS125A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the data control (C) inputs at 4.5V and the data inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	15		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output		10	18		15	22	ns
t_{PZH} Output Enable Time to High Level Output		19	25		23	35	ns
t_{PZL} Output Enable Time to Low Level Output		16	25		26	40	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)		10	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)		12	20				ns

Note 1: $C_L = 5$ pF.

National Semiconductor

DM54LS126A/DM74LS126A Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

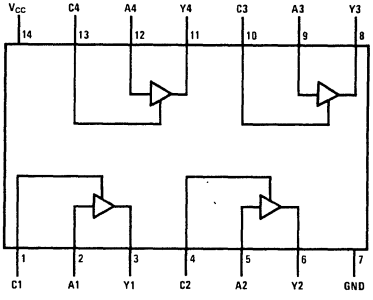
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6388-1

DM54LS126A (J) DM74LS126A (N)

Function Table

Y = A

Input		Output
A	C	Y
L	H	L
H	H	H
X	L	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS126A			DM74LS126A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	22	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with both the output control and data inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	15		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output		10	18		15	22	ns
t_{PZH} Output Enable Time to High Level Output		22	30		24	36	ns
t_{PZL} Output Enable Time to Low Level Output		19	30		28	42	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)		10	25				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)		14	25				ns

Note 1: $C_L = 5$ pF

4

National Semiconductor

DM54LS132/DM74LS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

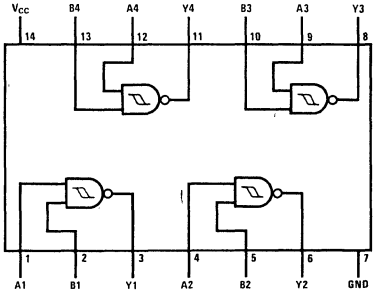
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6389-1

DM54LS132 (J) **DM74LS132 (N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS132			DM74LS132			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-} Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+} Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.18		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			5.9	11	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			8.2	14	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 2\ k\Omega$						Units
	$C_L = 15\ pF$			$C_L = 50\ pF$			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	5	15	22	8	18	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	5	15	22	10	21	33	ns

National Semiconductor

DM54LS136/DM74LS136 Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

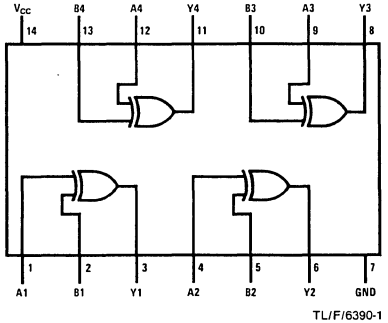
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6390-1

DM54LS136 (J) **DM74LS136 (N)**

Function Table

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS136			DM74LS136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			6.1	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low		18	30		21	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output			18	30		24	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High		18	30		21	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output			18	30		24	40	ns

National Semiconductor

DM54LS138/DM74LS138, DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high-speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW

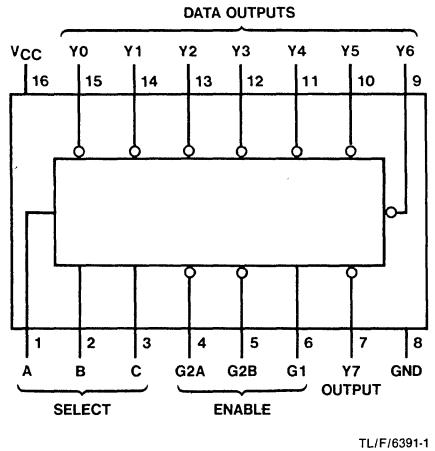
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

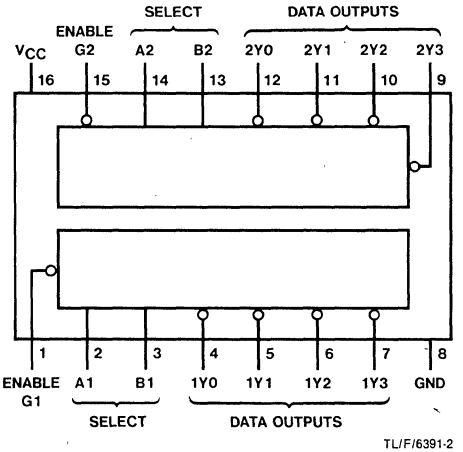
Dual-In-Line Package



TL/F/6391-1

54LS138 (J) 74LS138 (N)

Dual-In-Line Package



TL/F/6391-2

54LS139 (J) 74LS139 (N)

Recommended Operating Conditions

Symbol	Parameter	DM54LS138			DM74LS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS138 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS138 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Levels of Delay	$R_L = 2\ k\Omega$						Units
			$C_L = 15$ pF			$C_L = 50$ pF			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	2		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	2		17	27		23	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	3		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	3		17	27		23	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output	2		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output	2		16	24		22	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output	3		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output	3		19	28		25	40	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS139			DM74LS139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS139 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.8	11	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS139 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		17	27		23	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output		16	24		22	40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = High level, L = low level, X = don't care

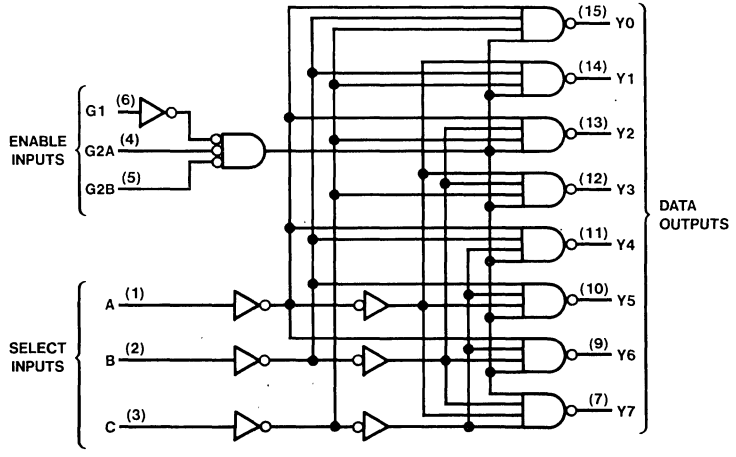
LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

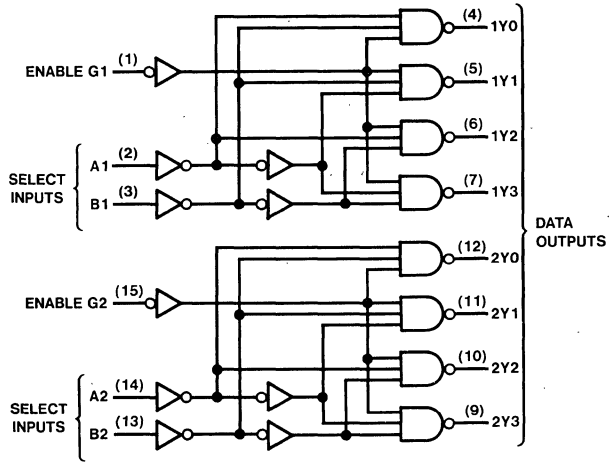
Logic Diagrams

LS138



TL/F/6391-3

LS139



TL/F/6391-4

National Semiconductor

DM54LS151/DM74LS151 Data Selector/Multiplexer

General Description

This data selector/multiplexer contains full on-chip decoding to select the desired data source. The LS151 selects one-of-eight data sources. The LS151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output low.

The LS151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time data input to W output 12.5 ns
- Typical power dissipation 30 mW

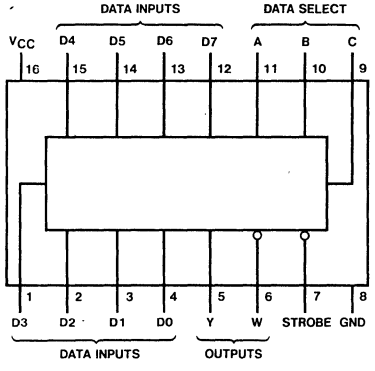
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6392-1

54LS151 (J) **74LS151 (N)**

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1...D7 = the level of the respective D input

Recommended Operating Conditions

Symbol	Parameter	DM54LS151			DM74LS151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

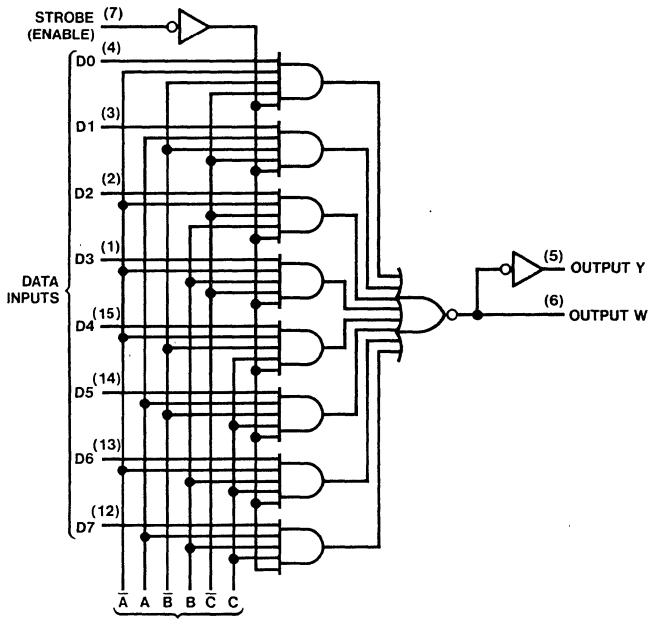
Note 3: I_{CC} is measured with all outputs open, strobe and data select inputs at 4.5V, and all other inputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		27	43		30	46	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		18	30		24	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		14	23		17	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		20	32		26	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		26	42		29	44	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		20	32		26	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to W		15	24		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to W		18	30		24	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		20	32		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		16	26		22	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D0 thru D7 to W		13	21		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D0 thru D7 to W		12	20		18	27	ns

Logic Diagram

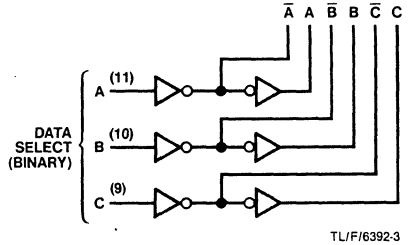
LS151



See Address Buffers Below

TL/F/6392-2

Address Buffers for 54LS151/74LS151



TL/F/6392-3

National Semiconductor

DM54LS153/DM74LS153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  From data 14 ns
  From strobe 19 ns
  From select 22 ns
- Typical power dissipation 31 mW

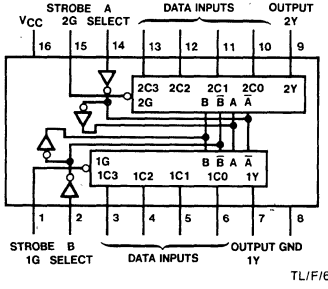
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6393-1

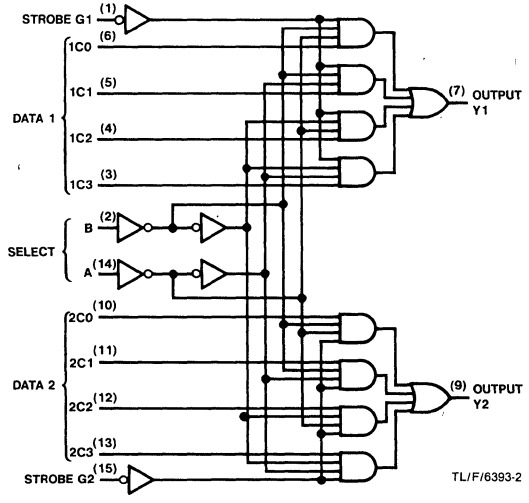
54LS153 (J) **74LS153 (N)**

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

Logic Diagram



TL/F/6393-2

Recommended Operating Conditions

Symbol	Parameter	DM54LS153			DM74LS153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		10	15		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		17	26		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		19	29		22	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		25	38		31	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		16	24		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		21	32		27	40	ns

National Semiconductor

DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 23 ns
  Strobe 19 ns
- Typical power dissipation 45 mW

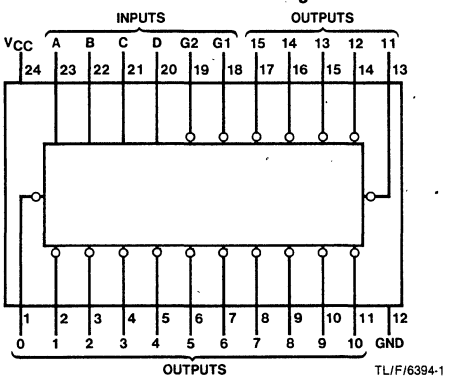
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection and Logic Diagrams

Dual-In-Line Package



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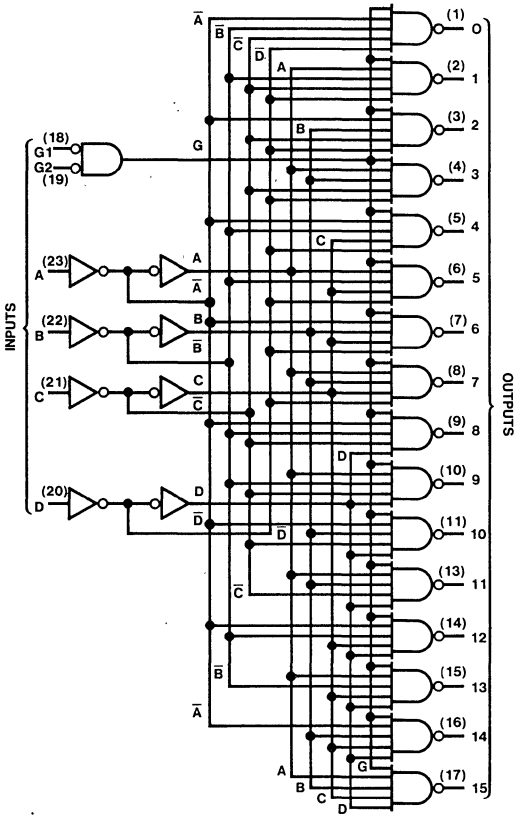
54LS154 (J) **74LS154 (N)**



TL/F/6394-2

Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		18	30		22	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		18	30		24	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		12	20		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		16	25		23	35	ns

Function Table

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
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L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

National Semiconductor

DM54LS155/DM74LS155, DM54LS156/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demuliplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  - Totem-pole (LS155)
  - Open-collector (LS156)

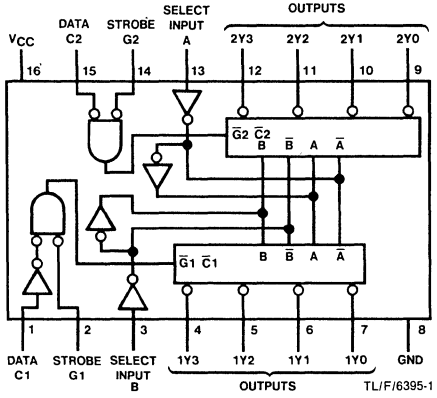
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS155 (J) **74LS155 (N)**
54LS156 (J) **74LS156 (N)**

Function Tables

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

Recommended Operating Conditions

Symbol	Parameter	DM54LS155			DM74LS155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS155 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.1	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

'LS155 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		12	18		15	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		17	27		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y		12	18		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y		17	27		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C1 to Y		13	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C1 to Y		17	27		23	35	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS156			DM74LS156			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Current			5.5			5.5	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS156 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			6.1	10	mA

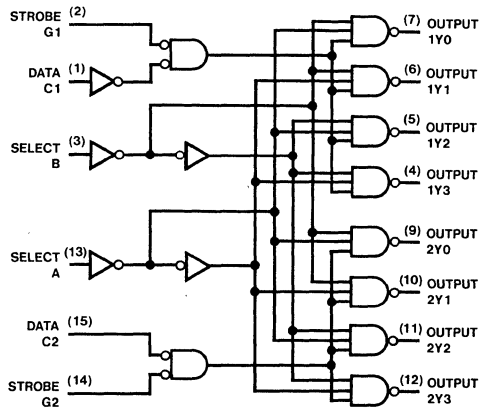
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		17	28			53	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		18	33			43	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y		17	28			53	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y		19	33			43	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C1 to Y		18	28			53	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C1 to Y		19	34			43	ns

Logic Diagram



TL/F/6395-2

National Semiconductor

DM54LS157/DM74LS157, DM54LS158/DM74LS158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS157 presents true data whereas the LS158 presents inverted data to minimize propagation delay time.

Features

- Buffered inputs and outputs
- Typical Propagation Time
  - LS157 9 ns
  - LS158 7 ns
- Typical Power Dissipation
  - LS157 49 mW
  - LS158 24 mW

Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

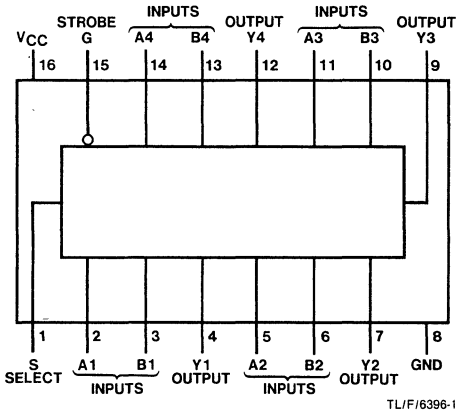
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



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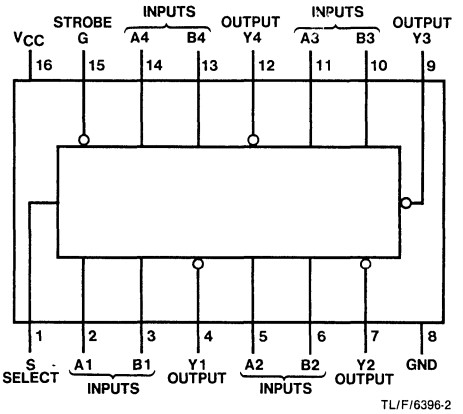
Low level at S selects A inputs
High level at S selects B inputs

54LS157 (J) **74LS157 (N)**

Dual-In-Line Package



TL/F/6396-2

Low level at S selects A inputs
High level at S selects B inputs

54LS158 (J) **74LS158 (N)**

Function Table

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Symbol	Parameter	DM54LS157			DM74LS157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS157 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			40	μA
			A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9.7	16	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

'LS157 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		9	14		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		9	14		15	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		13	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		16	23		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		15	27		21	32	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS158			DM74LS158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS158 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			40	μA
			A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4.8	8	mA

'LS158 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		9	12		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		8	12		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		12	17		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		13	18		19	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		13	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		18	24		24	36	ns

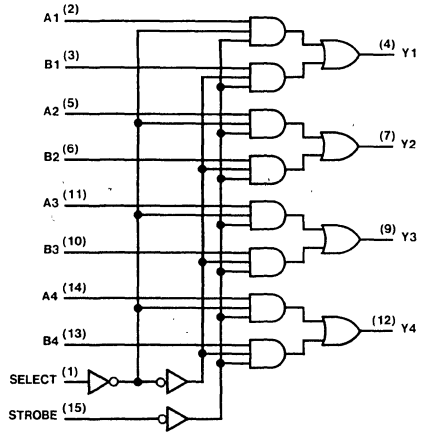
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs at 4.5V and all outputs open.

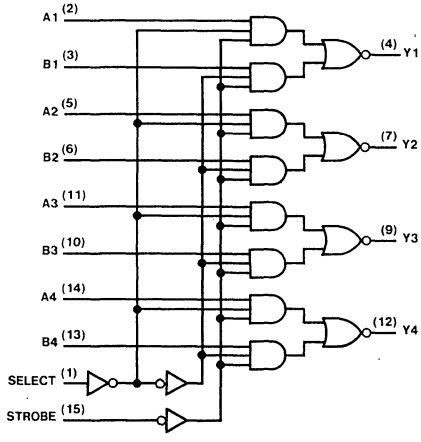
Logic Diagrams

LS157



TL/F/6396-3

LS158



TL/F/6396-4

National Semiconductor

DM54LS160A/DM74LS160A, DM54LS161A/DM74LS161A, DM54LS162A/DM74LS162A, DM54LS163A/DM74LS163A Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS160A and LS162A are decade counters and the LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the set-up data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input of the LS160A through LS163A are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the LS160A and LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS162A and LS163A is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs of the LS160A through LS163A may occur, regardless of the logic level of the clock.

LS160A through LS163A feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

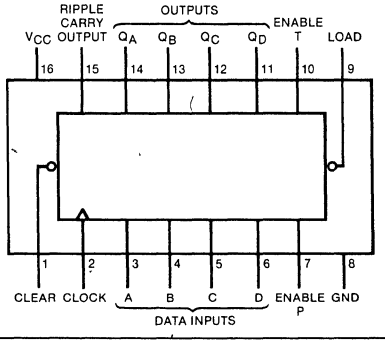
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6397-1

54LS160A (J) 74LS160A (N)
54LS161A (J) 74LS161A (N)
54LS162A (J) 74LS162A (N)
54LS163A (J) 74LS163A (N)

Recommended Operating Conditions

Symbol	Parameter		DM54LS160A, LS161A			DM74LS160A, LS161A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 1)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 2)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 1)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 2)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 1)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 2)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 1)		20			20			ns
	Clear Release Time (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

'LS160 and 'LS161 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	μA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			18	31	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			19	32	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS160 and 'LS161 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	32		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		16	24		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		19	30		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		15	22		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		19	27		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		16	24		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		21	29		26	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		10	15		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		25	35		31	45	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS162A, LS163A			DM74LS162A, LS163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 1)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 2)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 1)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 2)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 1)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 2)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 1)		20			20			ns
	Clear Release Time (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

'LS162 and 'LS163 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	μA
			Load			40	
			Clock			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			18	31	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			18	32	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS162 and 'LS163 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

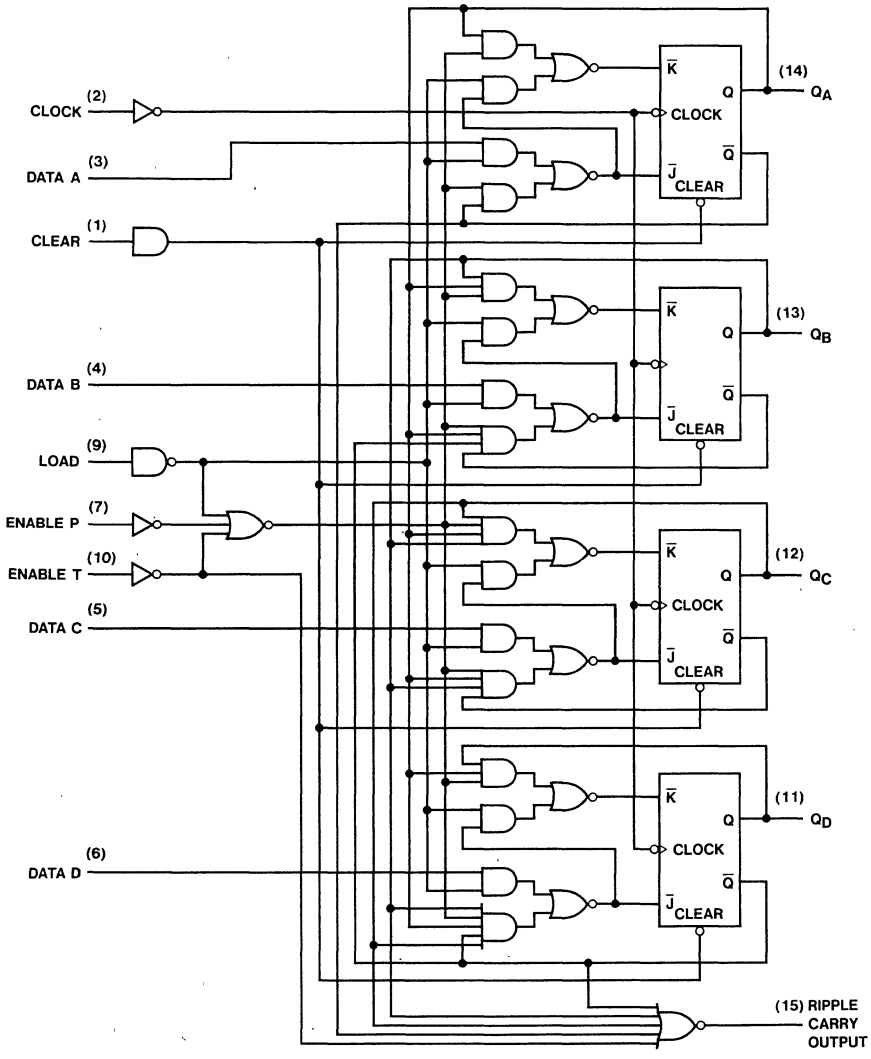
(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	32		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		16	24		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		19	30		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		15	22		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		19	27		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		16	24		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		21	29		26	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		13	18		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		10	15		16	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q (Note 1)		25	35		31	45	ns

Note 1: The propagation delay clear to output is measured from the clock input transition.

Logic Diagrams

LS160A



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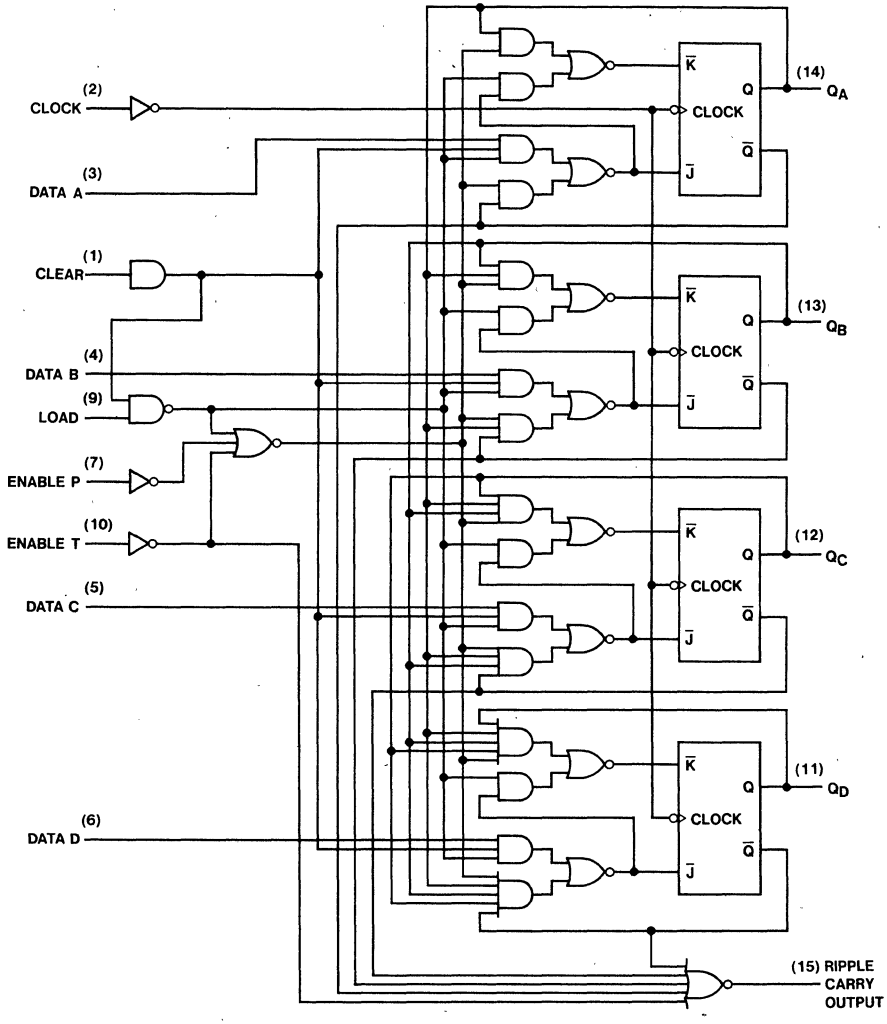
LS161A is similar; however, the clear is asynchronous as shown for LS160A decade counters.

Logic Diagrams (Continued)

LS163A



LS162A is similar; however, the clear is synchronous as shown for the LS163A binary counters.

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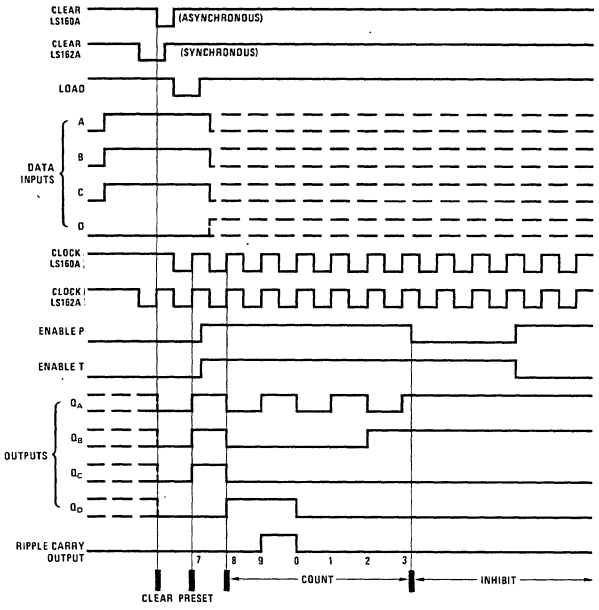
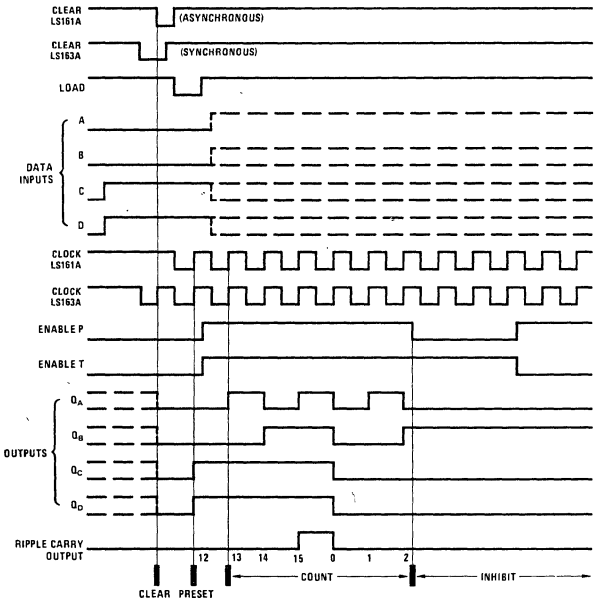
Timing Diagrams

LS160A, LS162A SYNCHRONOUS DECADE COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

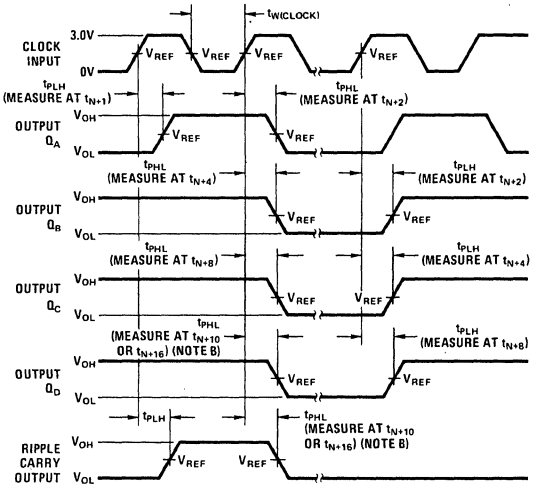
LS161A, LS163A SYNCHRONOUS BINARY COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

SWITCHING TIME WAVEFORMS

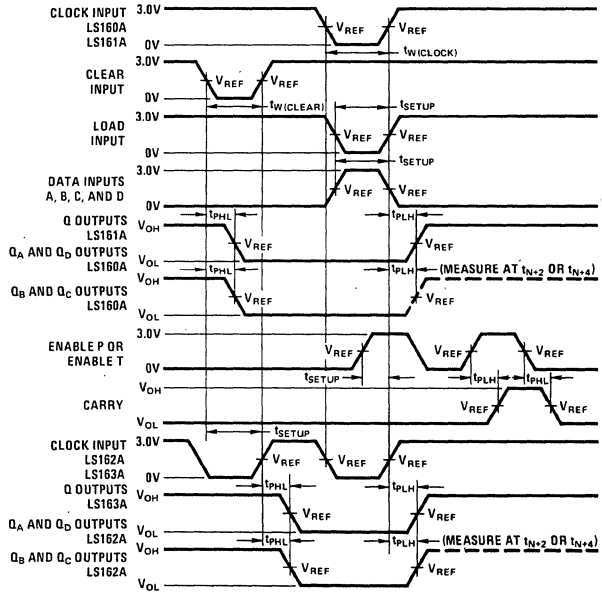


Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For LS160A through LS163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for LS160A, LS162A and at t_{n+16} for LS161A, LS163A where t_n is the bit time when all outputs are low.

Note C. For LS160A through LS163A, $V_{REF} = 1.5V$.

SWITCHING TIME WAVEFORMS



Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For LS160A through LS163A, $t_r \leq 6$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: For LS160A through LS163A, $V_{REF} = 1.3V$.

National Semiconductor

DM54LS164/DM74LS164 8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW

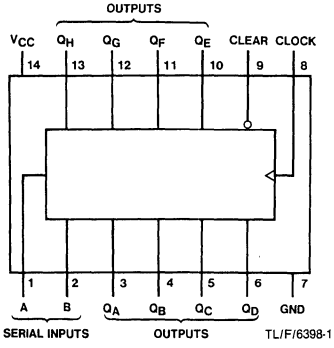
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS164 (J) **74LS164 (N)**

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

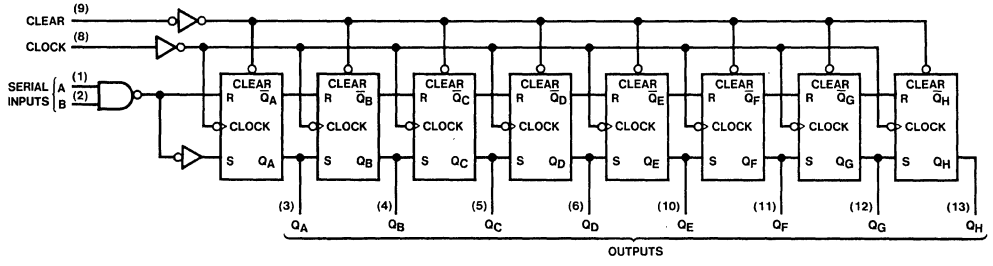
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



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Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time		15			15			ns
t_H	Data Hold Time		5			5			ns
t_{REL}	Clear Release Time		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

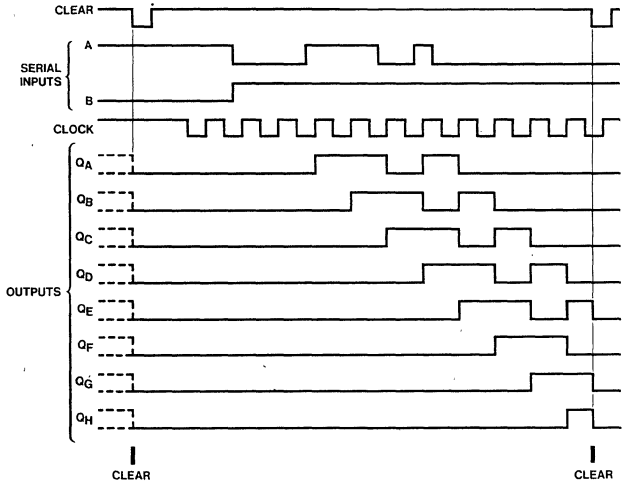
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	36					MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		17	27		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		21	32		28	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		24	36		30	45	ns

Timing Diagram



TL/F/6398-3

4

National Semiconductor

DM54LS165/DM74LS165 8-Bit Parallel In/Serial Output Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

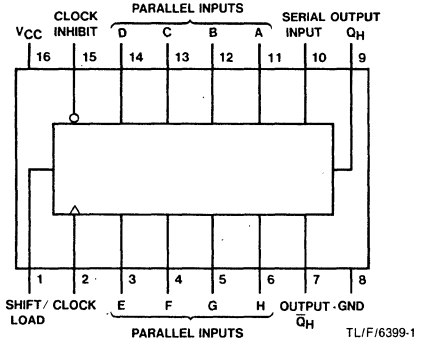
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS165 (J) **74LS165 (N)**

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low-to-high level
a...h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Recommended Operating Conditions

Symbol	Parameter		DM54LS165			DM74LS165			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width	Clock	25			25			ns
		Load	15			15			
t_{SU}	Setup Time	Parallel	10			10			ns
		Serial	20			20			
		Enable	30			30			
		Shift	45			45			
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Shift/Load			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Shift/Load			60	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Shift/Load			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			21	36	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ.

Note 2: C_L = 50 pF, R_L = 2 kΩ.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

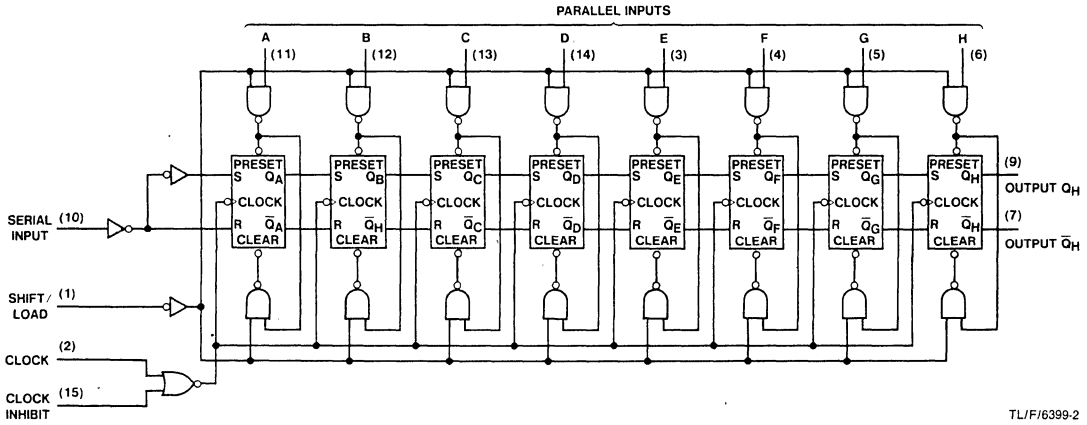
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		22	35		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		22	35		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		27	40		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		28	40		35	52	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to Q_H		14	25		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to Q_H		21	30		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		21	30		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		16	25		22	33	ns

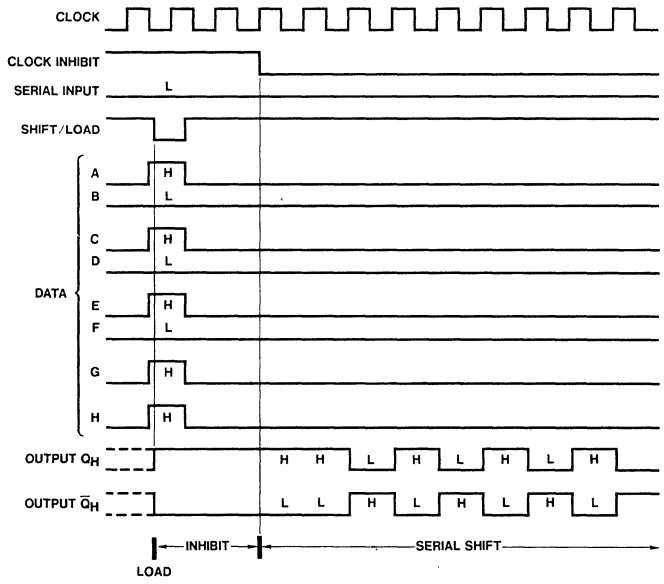
Logic Diagram



TL/F/6399-2

Timing Diagram

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES



TL/F/6399-3

National Semiconductor

DM54LS166/DM74LS166 8-Bit Parallel In/Serial Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

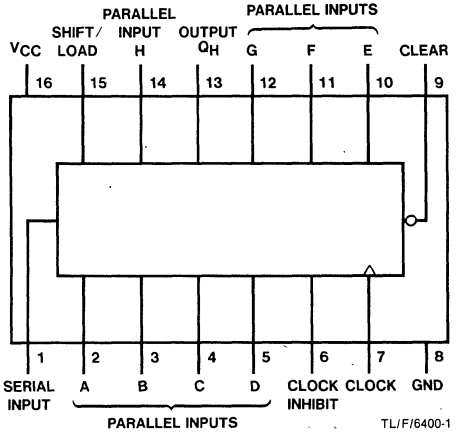
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS166 (J) **74LS166 (N)**

Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a...h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Recommended Operating Conditions

Symbol	Parameter		DM54LS166			DM74LS166			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			22	38	mA

Note 1: C_L = 15 pF and R_L = 2 kΩ.

Note 2: C_L = 50 pF and R_L = 2 kΩ.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

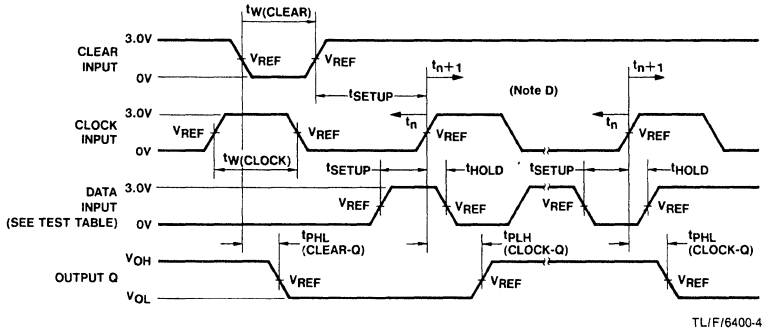
Note 5: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output	8	24	35		27	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output	8	23	35		29	41	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output	6	19	30		25	36	ns

Parameter Measurement Information

Voltage Waveforms



TL/F/6400-4

Test Table For Synchronous Inputs

Data Input For Test	Shift/Load	Output Tested (See Note C)
H	0 V	Q_H at T_{N+1}
Serial Input	4.5 V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns. When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

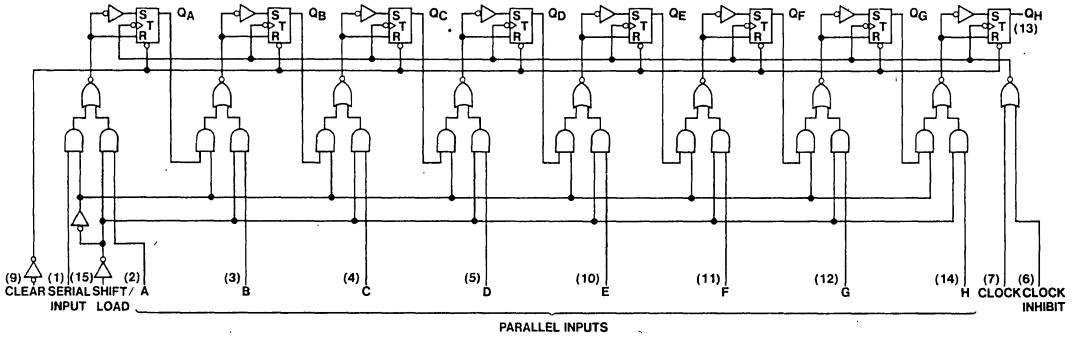
Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

Note E: $V_{REF} = 1.3V$.

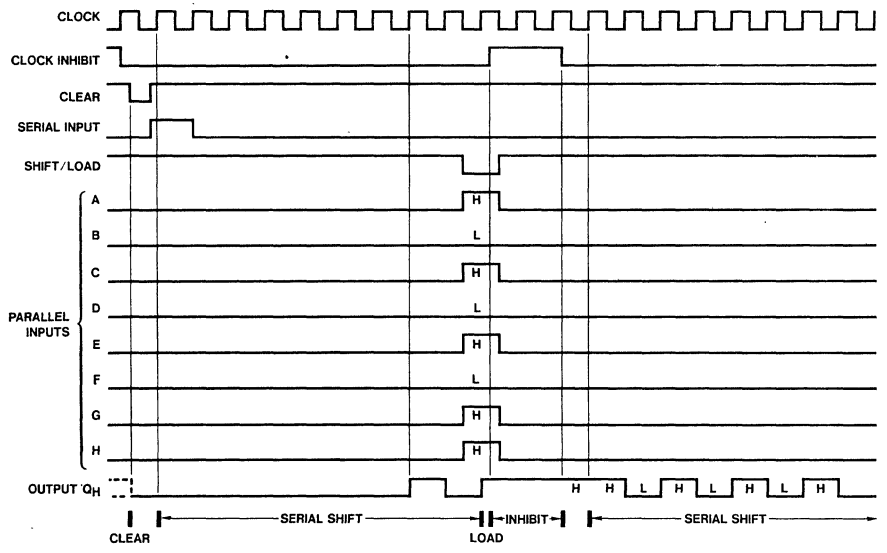
Logic Diagram



TL/F/6400-2

Timing Diagram

Typical Clear, Shift, Load, Inhibit, and Shift Sequences



TL/F/6400-3

National Semiconductor

DM54LS168A/DM74LS168A, DM54LS169A/DM74LS169A Synchronous 4-Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit
- 'LS168A—decade counter
- 'LS169A—binary counter

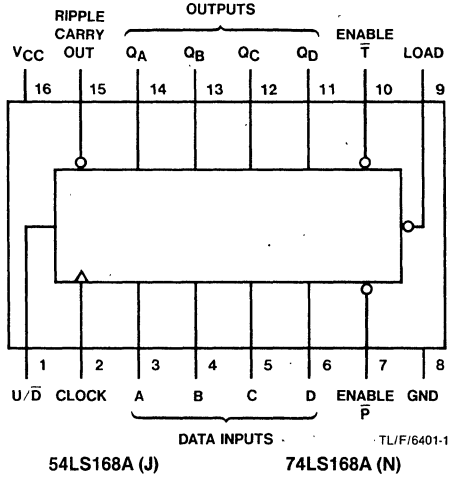
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS168A (J) **74LS168A (N)**
54LS169A (J) **74LS169A (N)**

Recommended Operating Conditions

Symbol	Parameter		DM54LS168A, LS169A			DM74LS168A, LS169A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Clock Pulse Width		25			25			ns
t_{SU}	Setup Time	Data	20			20			ns
		Enable $\overline{T}$ or $\overline{P}$	20			20			
		Load	25			25			
		U/D	30			30			
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

'LS168A and 'LS169A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable $\overline{T}$			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable $\overline{T}$			40	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable $\overline{T}$			−0.8	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			20	34	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured after a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and all the outputs open.

'LS168A and 'LS169A Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

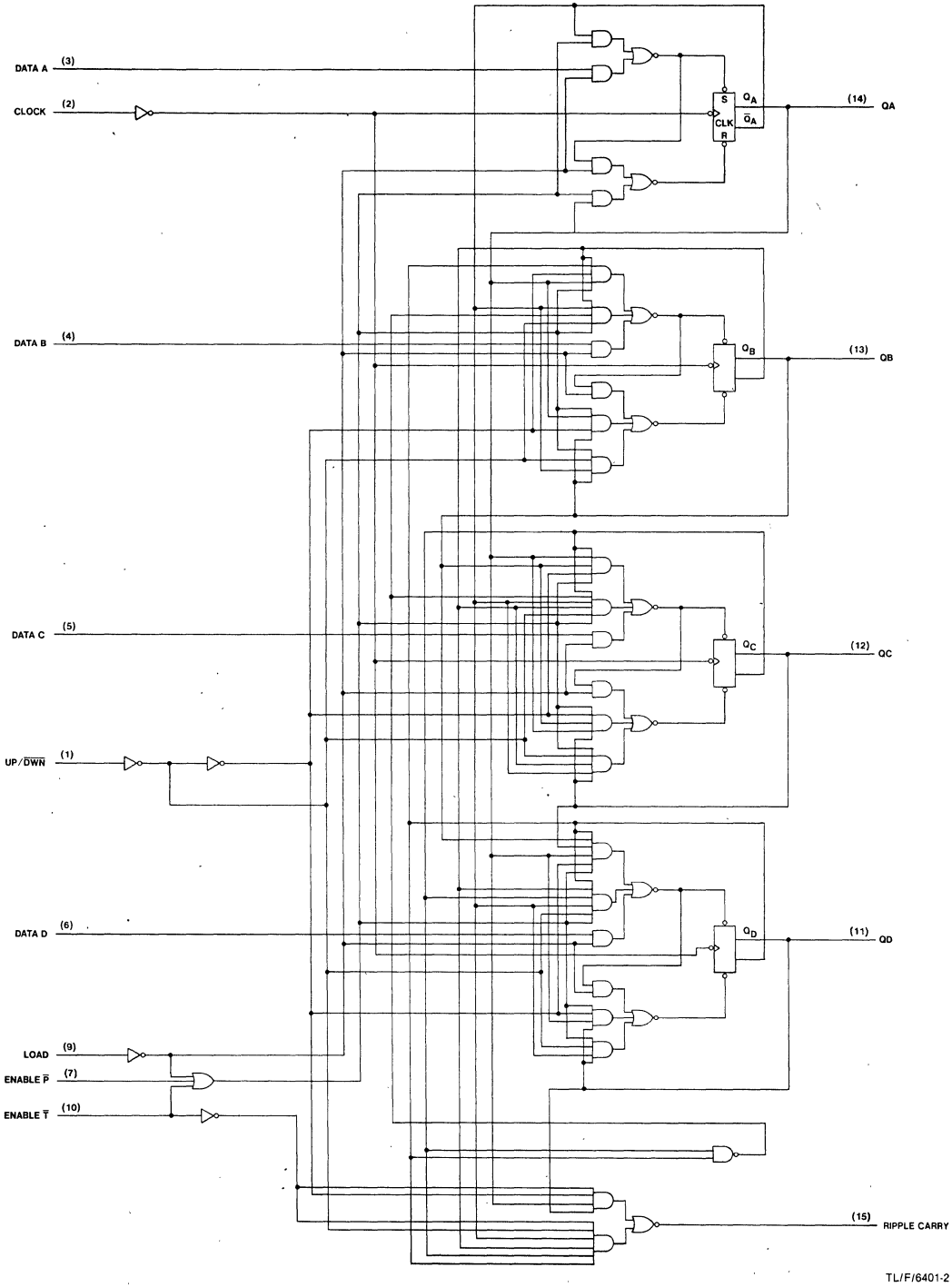
(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	32		20	28		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		23	35		26	39	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		23	35		29	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		13	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		15	23		21	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable $\overline{T}$ to Ripple Carry		12	18		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable $\overline{T}$ to Ripple Carry		12	18		18	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Up/Down to Ripple Carry (Note 1)		17	25		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Up/Down to Ripple Carry (Note 1)		19	29		20	38	ns

Note 1: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

Logic Diagram

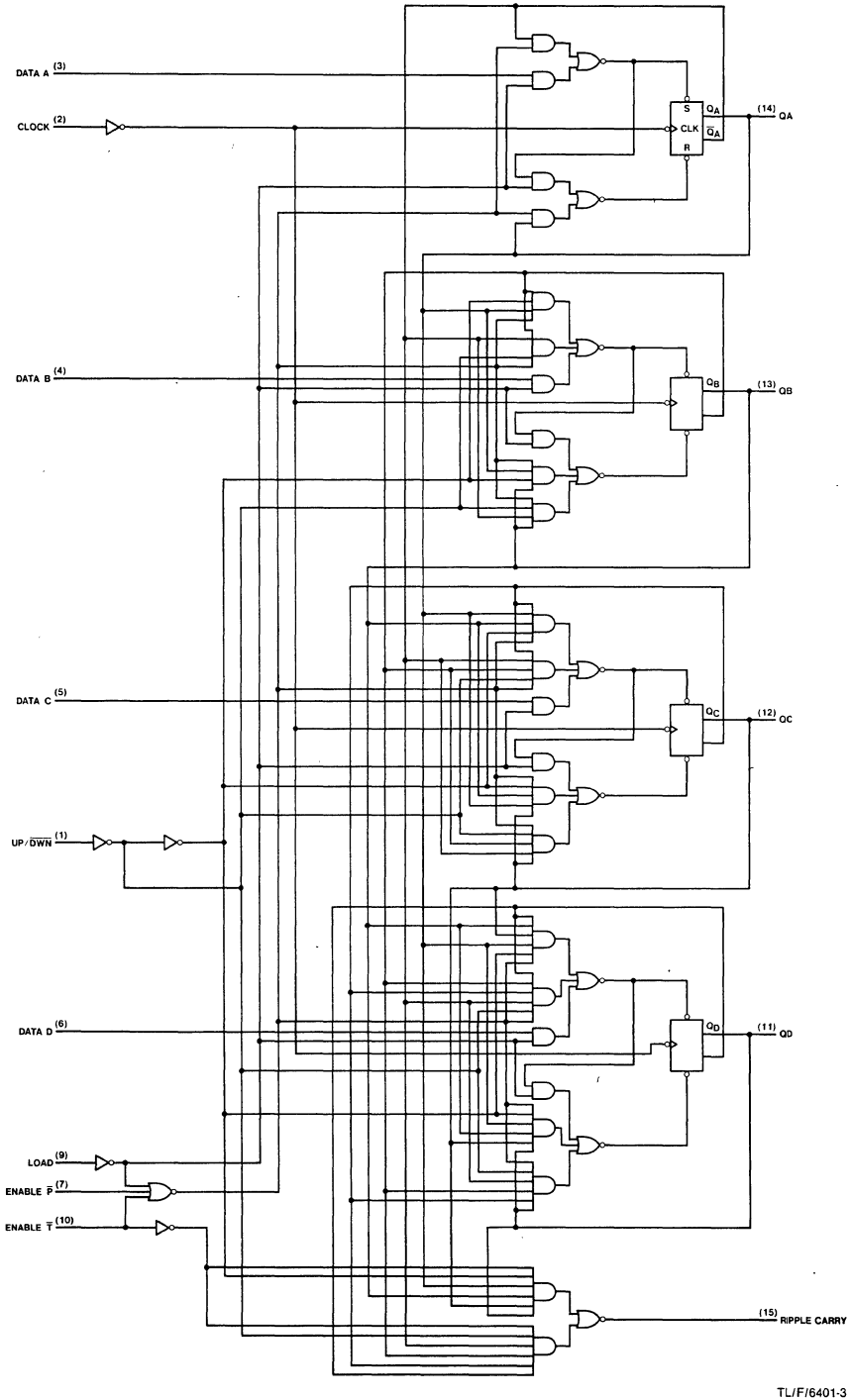
LS168A Decade Counter



TL/F/6401-2

Logic Diagram

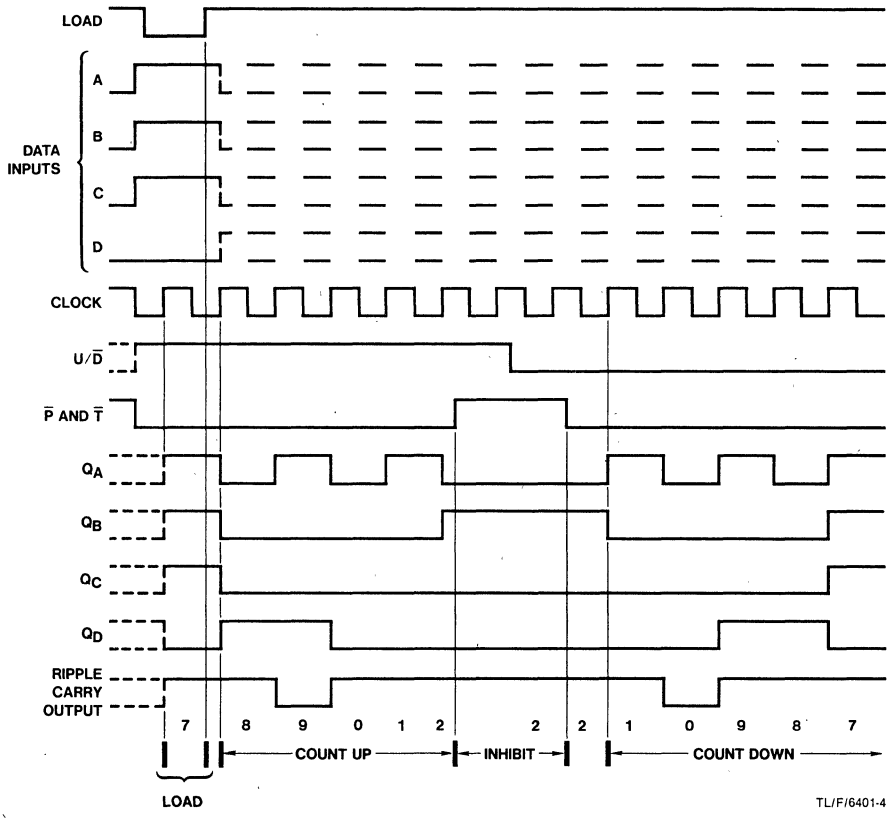
LS169A Binary Counter



TL/F/6401-3

Timing Diagrams

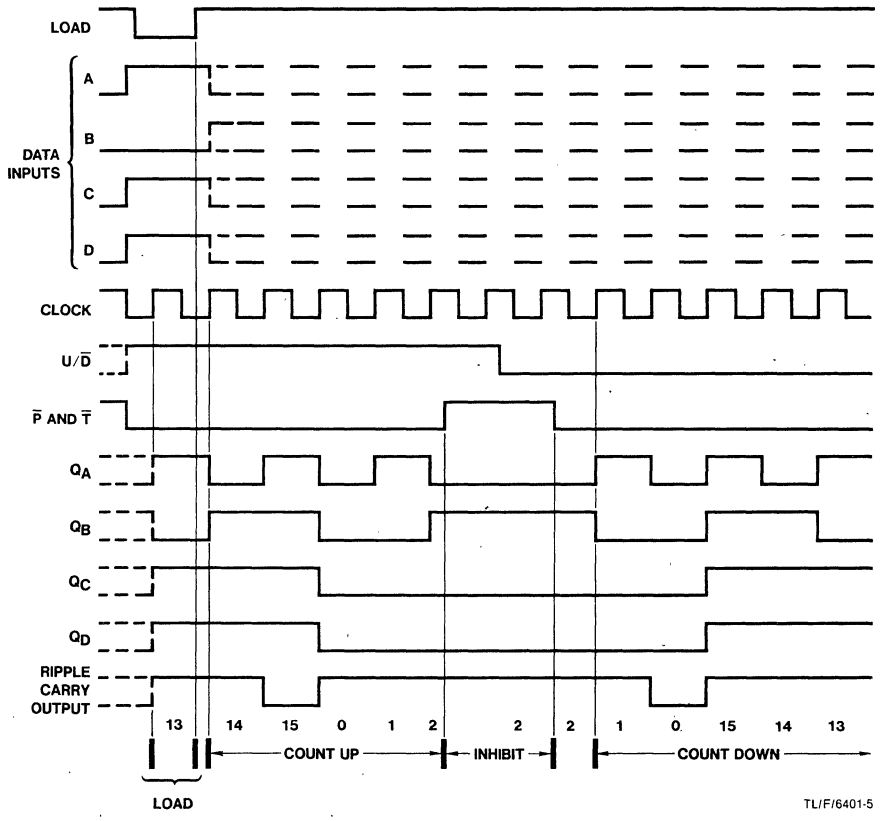
LS168A Decade Counters
Typical Load, Count, and Inhibit Sequences



Sequence 1: Load (preset) to BCD seven
Sequence 2: Count up to eight, nine, zero, one and two
Sequence 3: Inhibit
Sequence 4: Count down to one, zero, nine, eight and seven

Timing Diagrams (Continued)

LS169A Binary Counters
Typical Load, Count, and Inhibit Sequences



Sequence 1: Load (preset) to binary thirteen
Sequence 2: Count up to fourteen, fifteen, zero, one and two
Sequence 3: Inhibit
Sequence 4: Count down to one, zero, fifteen, fourteen and thirteen

National Semiconductor

DM54LS170/DM74LS170 4 by 4 Register Files

General Description

These 16-bit TTL register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location and reading from another word location, simultaneously.

Four data inputs are available to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct reading of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 ns typical) and the read time (25 ns typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable are buffered to lower the drive requirements to one standard load. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- Separate addressing permits simultaneous reading and writing
- Fast access times typically 20 ns
- Organized as 4 words of 4 bits
- Expandable to 1024 words of n-bits
- For use as:
  - Scratch-pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Open-collector outputs with low maximum off-state current: 20 μA
- DM54LS670 and DM74LS670 are similar but have TRI-STATE® outputs

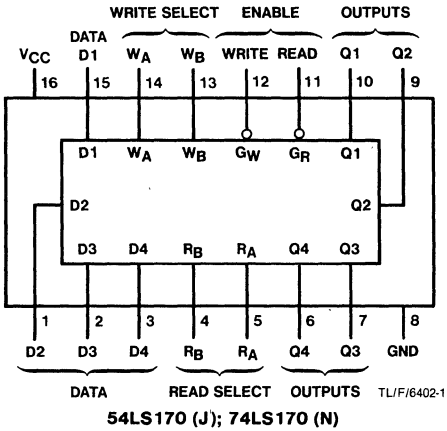
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6402-1

54LS170 (J); 74LS170 (N)

Function Table

WRITE TABLE (SEE NOTES A, B, AND C)

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (SEE NOTES A AND D)

Read Inputs			Outputs			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

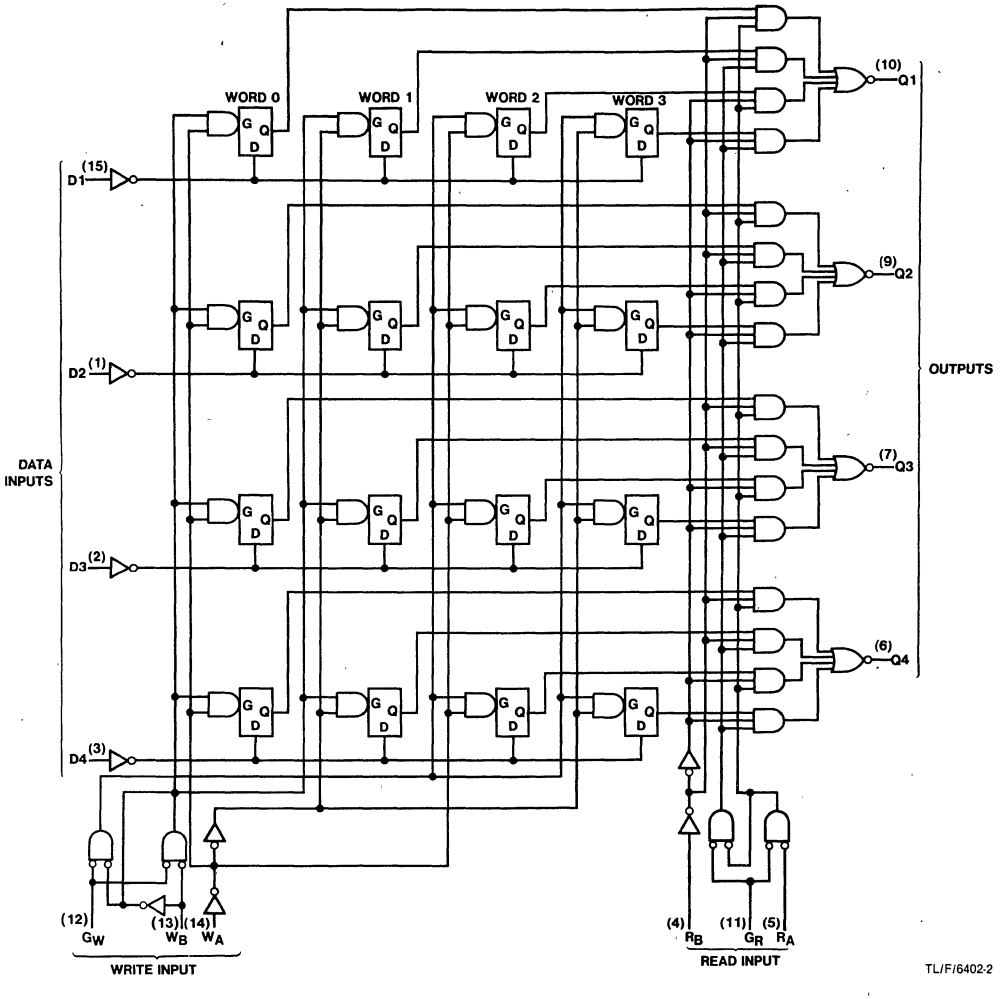
Note A: H = High Level, L = Low Level, X = Don't Care

Note B: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Note C: Q_0 = The level of Q before the indicated input conditions were established.

Note D: W0B1 = The first bit of word 0, etc.

Logic Diagram



Recommended Operating Conditions

Symbol	Parameter		DM54LS170			DM74LS170			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
V_{OH}	High Level Output Voltage				5.5			5.5	V
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	Write-Enable	25			25			ns
		Read-Enable	25			25			
t_{SU}	Setup Time (Note 1)	Data	10			10			ns
		Write Select	15			15			
t_H	Hold Time (Note 1)	Data	15			15			ns
		Write Select	5			5			
t_{LAT}	Latch Time for New Data		25			25			nS
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				20	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 7V	D, R, W			0.1	mA
			G_R, G_W			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	D, R, W			20	μA
			G_R, G_W			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	D, R, W			−0.4	mA
			G_R, G_W			−0.8	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			25	40	mA

Note 1: Times are with respect to the Write-Enable input.

Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: I_{CC} is measured with all data and enable inputs at 4.5V, all address inputs grounded and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Read Enable to Any Q		20	30		45	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Read Enable to Any Q		20	30		33	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Read Select to Any Q		25	40		45	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Read Select to Any Q		25	40		33	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Write Enable to Any Q		30	45		53	65	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Write Enable to Any Q		26	40		34	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		30	45		55	65	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		22	35		25	40	ns

National Semiconductor

DM54LS173A/DM74LS173A TRI-STATE® Quad D Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the the bus line. Detailed operation is given in the truth table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 18 ns
- Typical frequency 45 MHz
- Typical power dissipation 85 mW

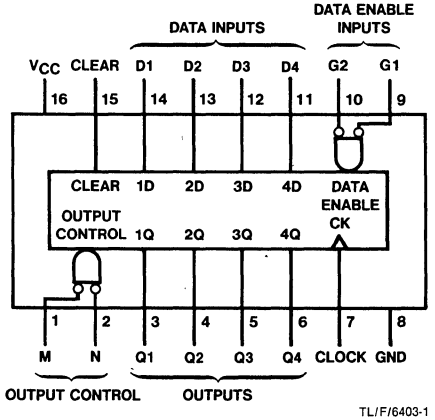
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6403-1

54LS173A (J) **74LS173A (N)**

Function Table

Inputs					Output Q
Clear	Clock	Data Enable G1	Data Enable G2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Recommended Operating Conditions

Sym	Parameter		DM54LS173A			DM74LS173A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width	Clock	17			17			ns
		Clear	17			17			
t_{SU}	Setup Time	Enable	17			17			ns
		Data	10			10			
t_H	Hold Time	Enable	0			0			ns
		Data	0			0			
t_{REL}	Clear Release Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 45$ pF and $R_L = 667\Omega$.
Note 2: $C_L = 150$ pF and $R_L = 667\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			17	30	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 667Ω						Units
		C_L = 45 pF			C_L = 150 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	45		20	30		ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		16	25		21	34	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		20	30		26	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		20	30		26	40	ns
t_{PZH} Output Enable Time to High Level Output	Output Control (M or N) to Any Q	7	18	21	9	27	34	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control (M or N) to Any Q	7	18	27	9	30	45	ns
t_{PHZ} Output Disable Time from High Level Output (Note 4)	Output Control (M or N) to Any Q	3	11	17				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 4)	Output Control (M or N) to Any Q	3	10	20				ns

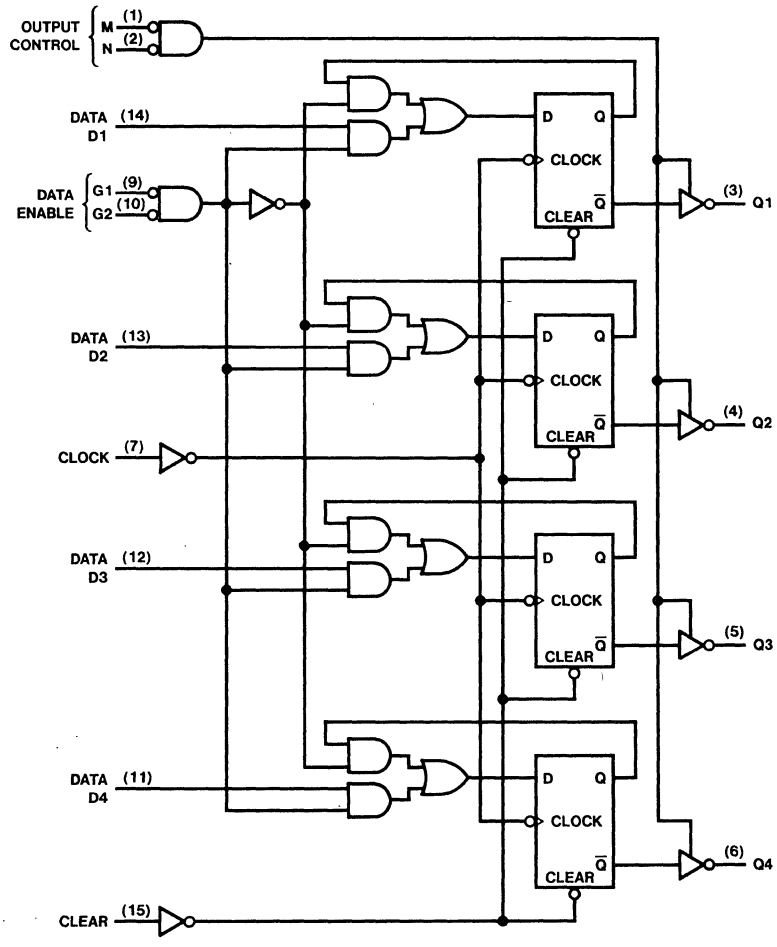
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open: Clear grounded after a momentary 4.5V; N, G1, G2 and all data inputs grounded: and the CLOCK and M input at 4.5V.

Note 4: C_L = 5 pF.

Logic Diagram



TL/F/6403-2

National Semiconductor

DM54LS174/DM74LS174, DM54LS175/DM74LS175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- LS174 contains six flip-flops with single-rail outputs
- LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  Buffer/storage registers
  Shift registers
  Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW

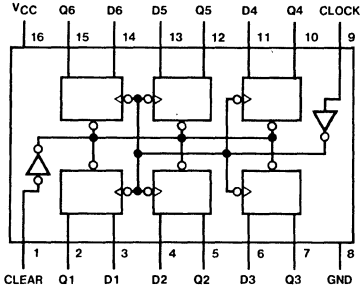
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

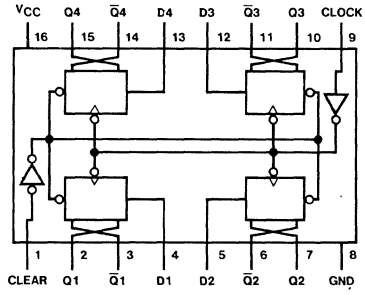
Dual-In-Line Package



TL/F/6404-1

54LS174 (J) **74LS174 (N)**

Dual-In-Line Package



TL/F/6404-2

54LS175 (J) **74LS175 (N)**

Recommended Operating Conditions

Sym	Parameter		DM54LS174			DM74LS174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Data Hold Time		0			0			ns
t_{REL}	Clear Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS174 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			16	26	mA

Note 1: C_L = 15 pF and R_L = 2 kΩ.

Note 2: C_L = 50 pF and R_L = 2 kΩ.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

'LS174 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	40		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		20	30		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		21	30		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		23	35		28	42	ns

Recommended Operating Conditions

Sym	Parameter		DM54LS175			DM74LS175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Data Hold Time		0			0			ns
t_{REL}	Clear Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2\ k\Omega$.
Note 2: $C_L = 50$ pF and $R_L = 2\ k\Omega$.

'LS175 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Parameter		Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	18	mA

'LS175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	40		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20	30		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		21	30		24	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		16	25		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		23	35		28	42	ns

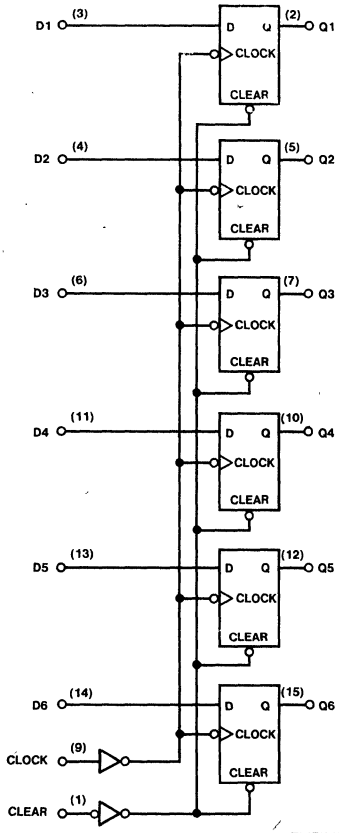
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V, applied to the clock input.

Logic Diagrams

LS174



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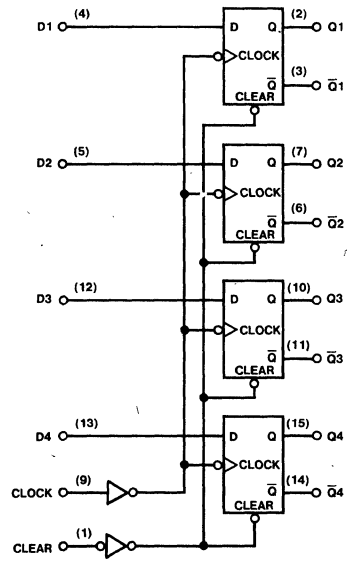
LS175



TL/F/6404-4

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = LS175 only

National Semiconductor

DM54LS190/DM74LS190, DM54LS191/DM74LS191 Synchronous 4-Bit Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

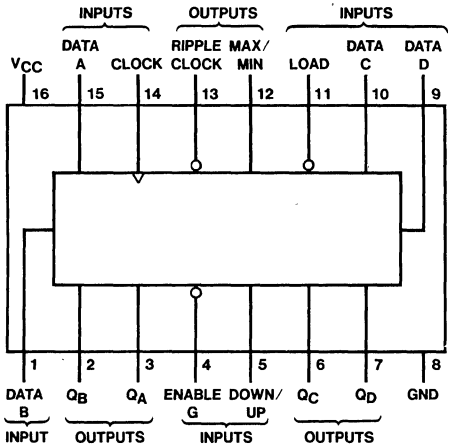
- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



TL/F/6405-1

Dual-In-Line Package

54LS190 (J) **74LS190 (N)**
54LS191 (J) **74LS191 (N)**

Recommended Operating Conditions

Sym	Parameter		DM54LS190, LS191			DM74LS190, LS191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time		20			20			ns
t_H	Data Hold Time		0			0			ns
t_{EN}	Enable Time to Clock		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS190 and 'LS191 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable			60	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable			−1.08	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			20	35	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

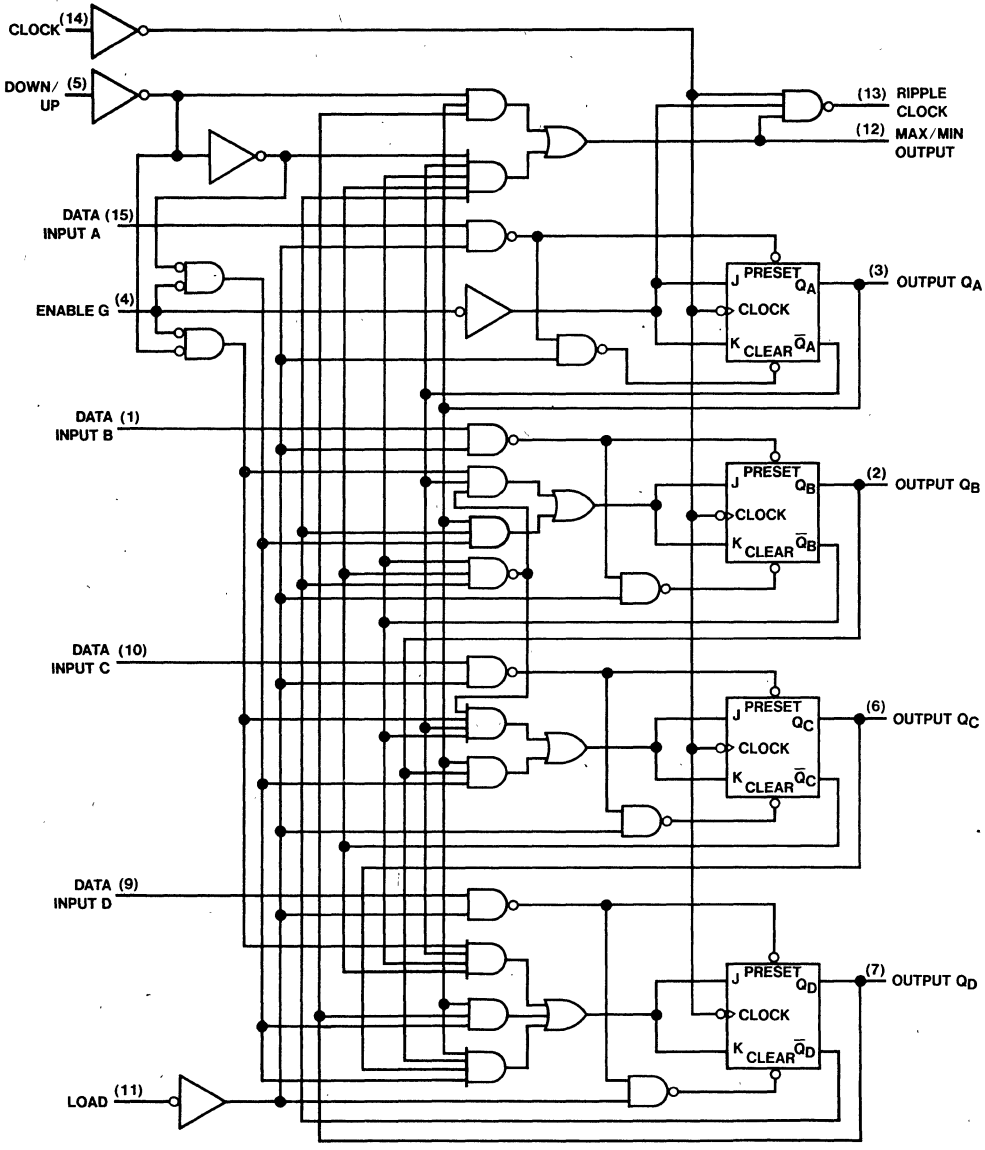
'LS190 and 'LS191 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		22	33		25	43	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		33	50		39	59	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		14	22		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		35	50		41	62	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Clock		13	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Clock		16	24		22	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		16	24		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		24	36		30	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Max/Min		28	42		31	47	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Max/Min		37	52		43	65	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Up/Down to Ripple Clock		30	45		33	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Up/Down to Ripple Clock		30	45		36	54	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		21	33		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		22	33		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Ripple Clock		21	33		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Ripple Clock		22	33		28	42	ns

Logic Diagrams

LS190 Decade Counters

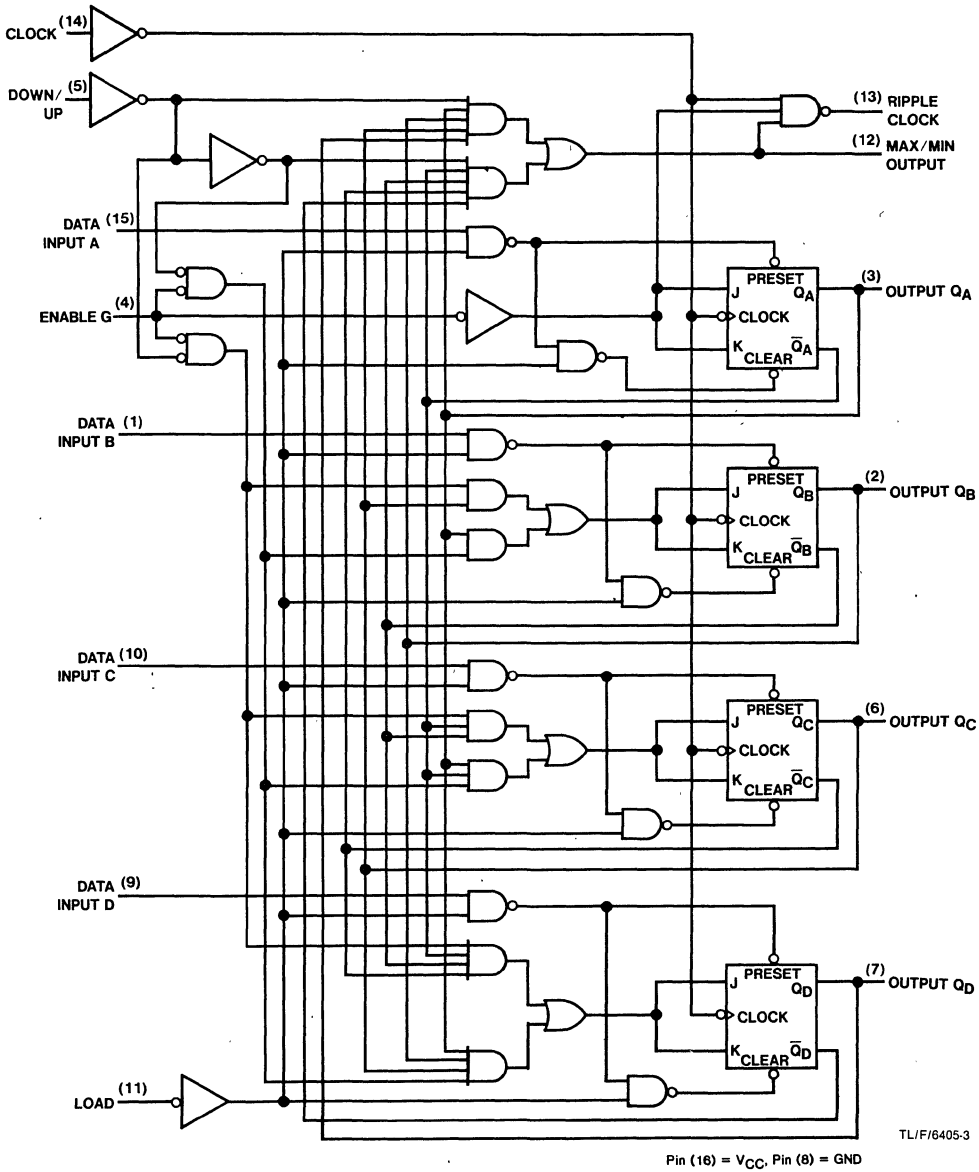


TL/F/6405-2

Pin (16) = V_{CC}, Pin (8) = GND

Logic Diagrams (Continued)

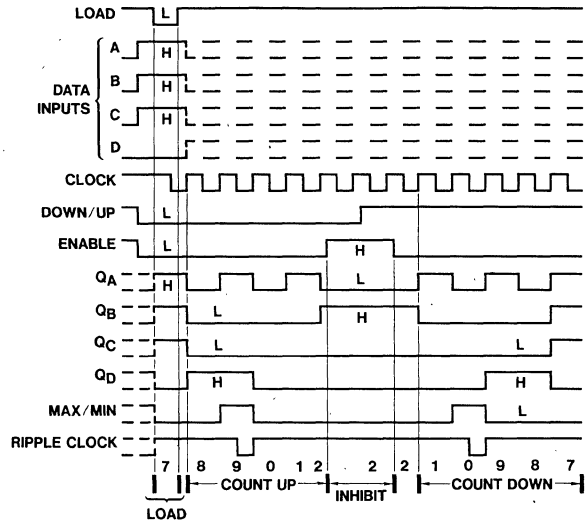
LS191 Binary Counters



Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

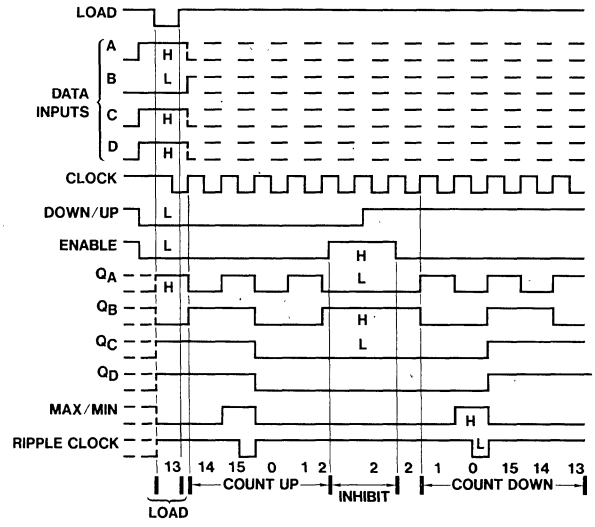
LS190 Decade Counters
Typical Load, Count, and Inhibit Sequences



TL/F/6405-4

Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

LS191 Binary Counters
Typical Load, Count, and Inhibit Sequences



TL/F/6405-5

Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

National Semiconductor

DM54LS192/DM74LS192, DM54LS193/DM74LS193 Synchronous 4-Bit Up/Down Counters with Dual Clock

General Description

These circuits are synchronous up/down counters; the LS192 circuit is a BCD counter and the LS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

The counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows.

Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop
- Typical count frequency 32 MHz
- Typical power dissipation 95 mW

Absolute Maximum Ratings (Note 1)

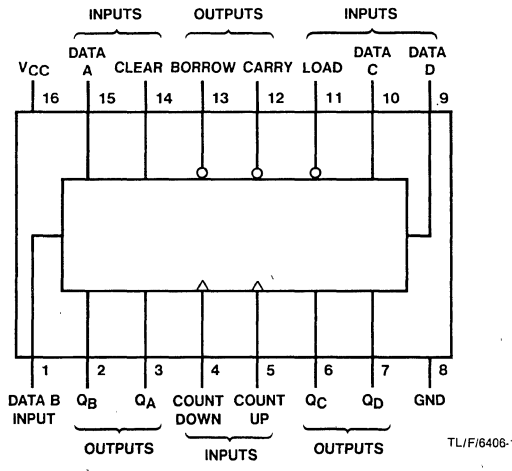
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



Note: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D.

54LS192 (J) **74LS192 (N)**
54LS193 (J) **74LS193 (N)**

Recommended Operating Conditions

Sym	Parameter	DM54LS192, LS193			DM74LS192, LS193			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
f_{CLK}	Clock Frequency (Note 1)	0		25	0		25	MHz
	Clock Frequency (Note 2)	0		20	0		20	MHz
t_W	Pulse Width of Any Input	20			20			ns
t_{SU}	Data Setup Time	20			20			ns
t_H	Data Hold Time	0			0			ns
t_{REL}	Release Time	40			40			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS192 and 'LS193 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			19	34	mA

Note 1: C_L = 15 pF and R_L = 2 kΩ.

Note 2: C_L = 50 pF and R_L = 2 kΩ.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

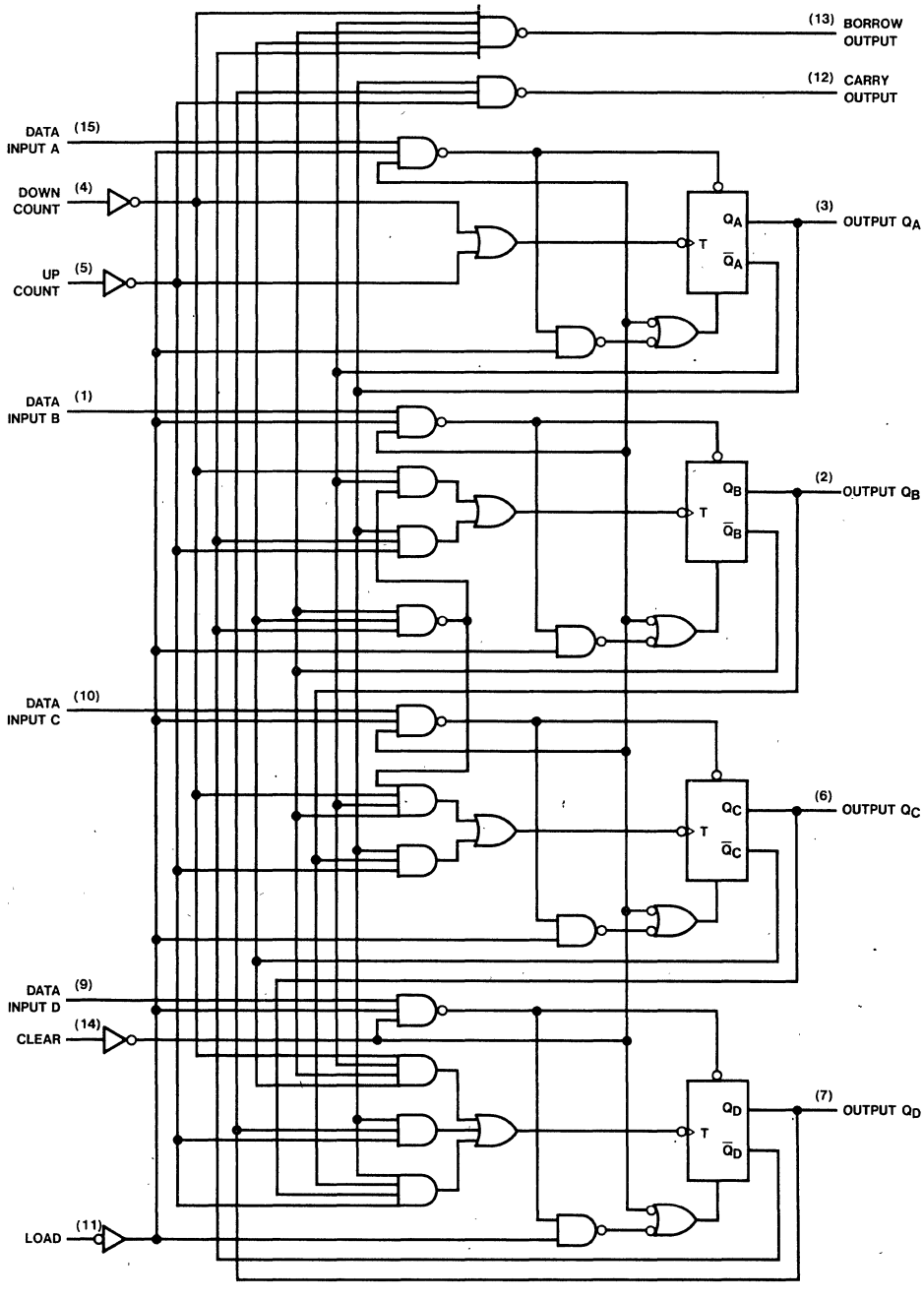
'LS192 and 'LS193 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	32		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		17	26		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		18	24		24	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		16	24		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		15	24		21	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Either Count to Any Q		27	38		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Either Count to Any Q		30	47		36	54	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		24	40		27	41	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		25	40		31	47	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		23	35		29	44	ns

Logic Diagrams

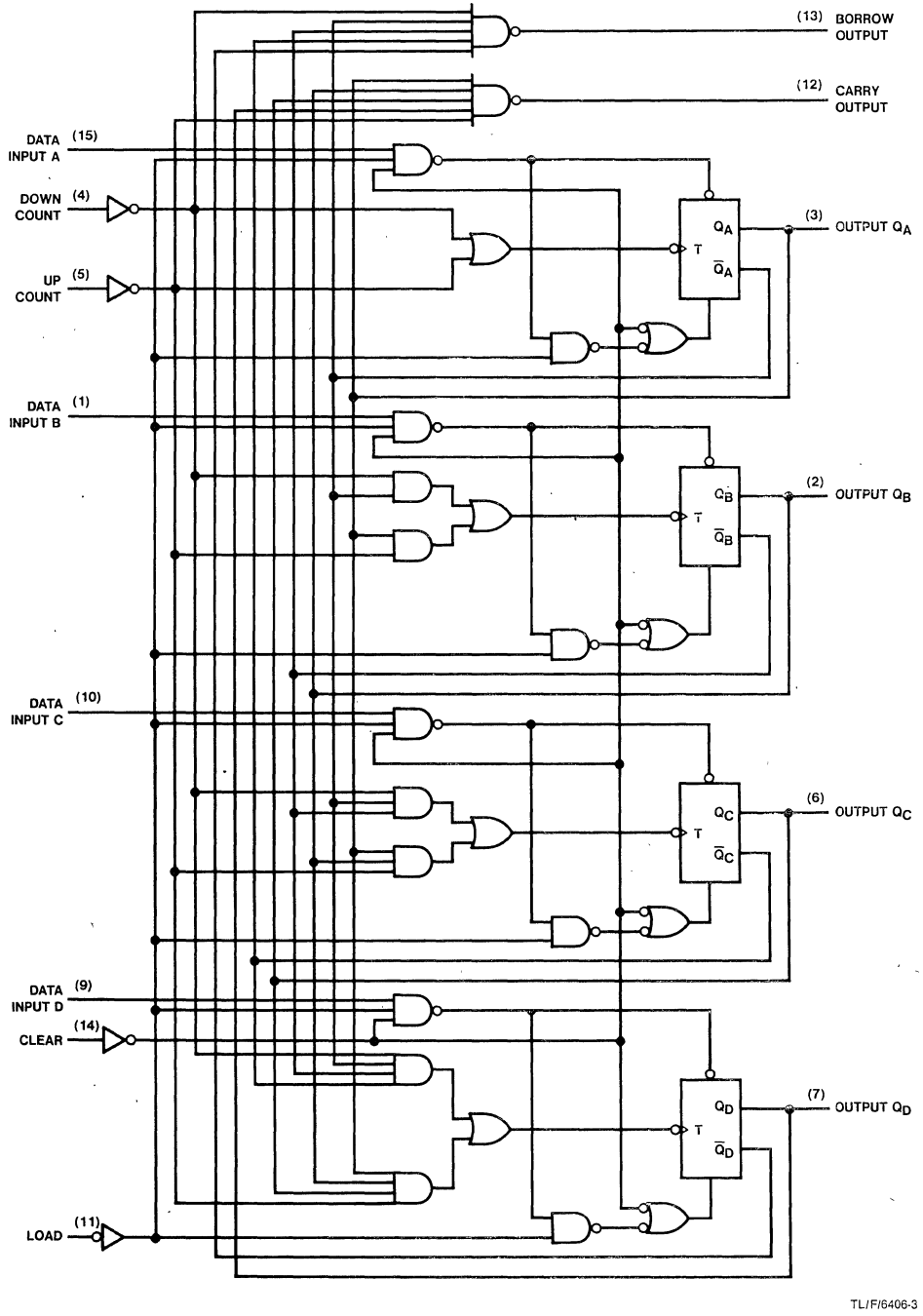
LS192



TL/F/6406-2

Logic Diagrams (Continued)

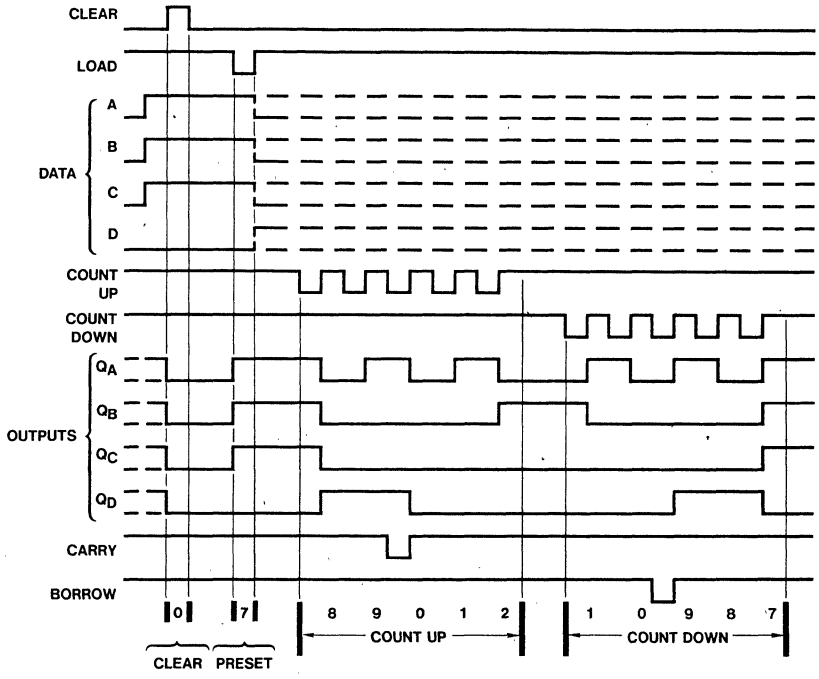
LS193



TL/F/6406-3

Timing Diagrams

LS192 DECADE COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



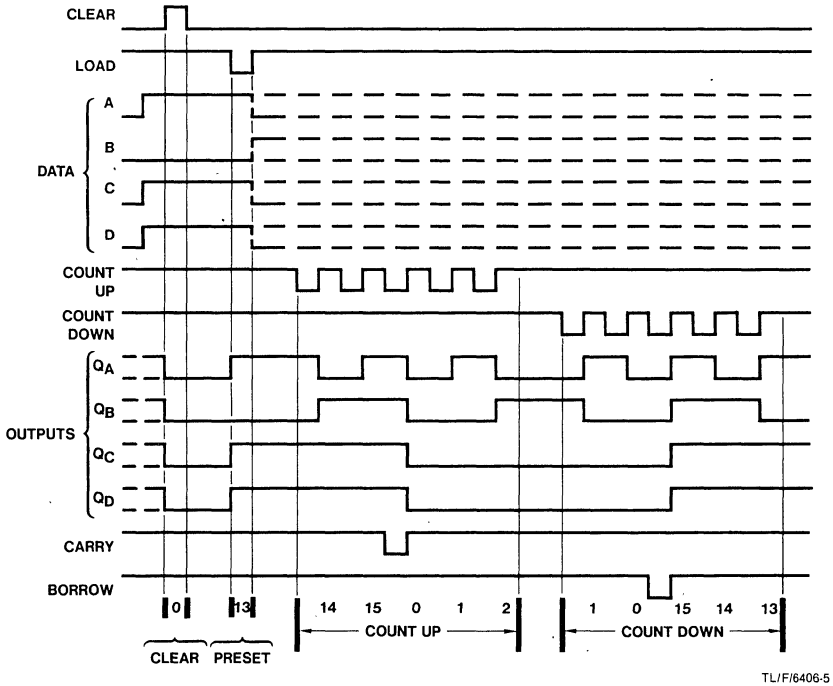
TL/F/6406-4

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

LS193 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



TL/F/6406-5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

DM54LS194A/DM74LS194A 4-Bit Bidirectional Universal Shift Registers

General Description

This bidirectional shift registers is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 36 MHz
- Typical power dissipation 75 mW

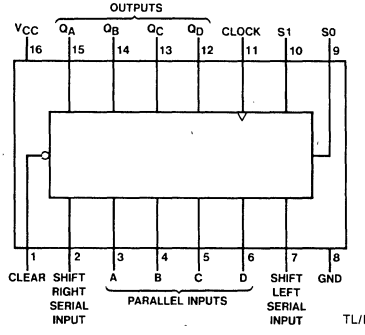
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS194A (J)
74LS194A (N)

TL/F/6407-1

Function Table

Inputs									Outputs			
Clear	Mode S1	Mode S0	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Recommended Operating Conditions

Sym	Parameter		DM54LS194A			DM74LS194A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time		0			0			ns
t_{REL}	Clear Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			15	23	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	36		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		14	22		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		17	22		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		19	30		25	38	ns

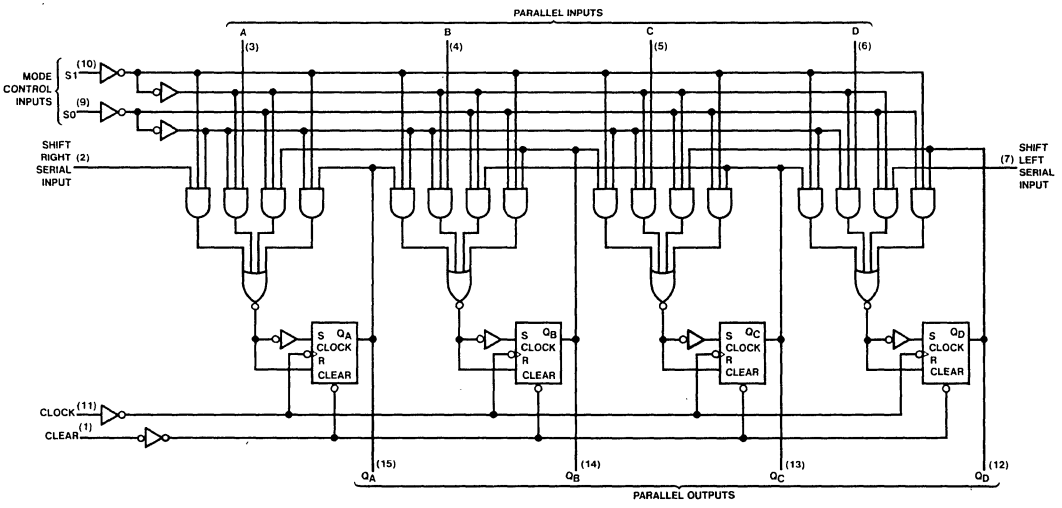
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Logic Diagram

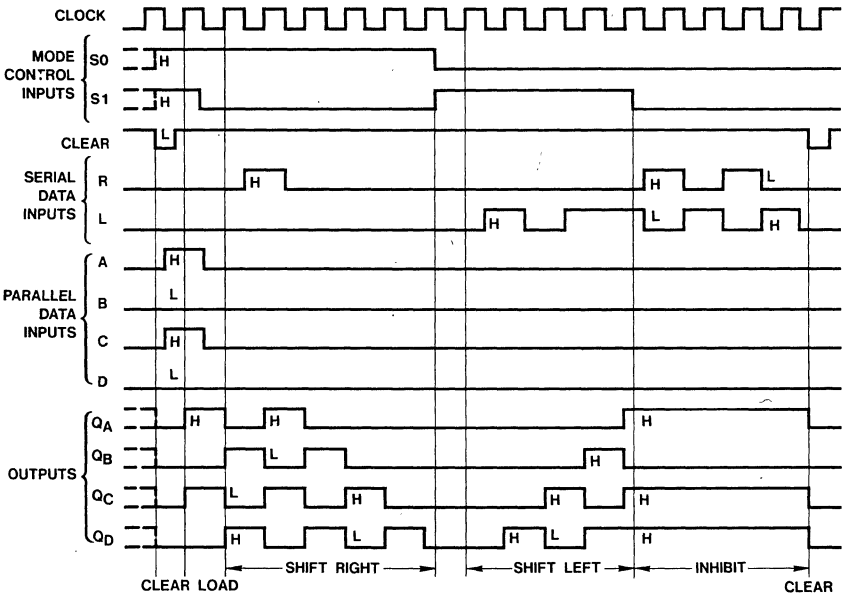
LS194A



TL/F/6407-2

Timing Diagram

TYPICAL CLEAR, LOAD , RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



TL/F/6407-3

National Semiconductor

DM54LS195A/DM74LS195A 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 39 MHz
- Typical power dissipation 70 mW

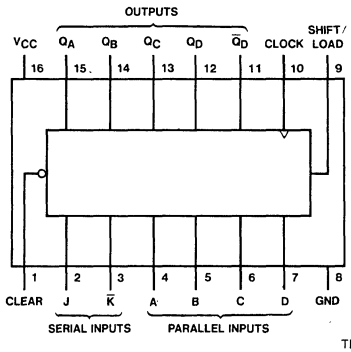
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6408-1

54LS195A (J)
74LS195A (N)

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a,b,c,d = The level of steady state input at A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

Recommended Operating Conditions

Sym	Parameter		DM54LS195A			DM74LS195A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width	Clock	16			16			ns
		Clear	12			12			
t_{SU}	Setup Time	Shift/Load	25			25			ns
		Data	15			15			
t_H	Hold Time		0			0			ns
t_{REL}	Shift/Load Release Time		10			10			ns
	Clear Release Time		25			25			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.
Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

4

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	21	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

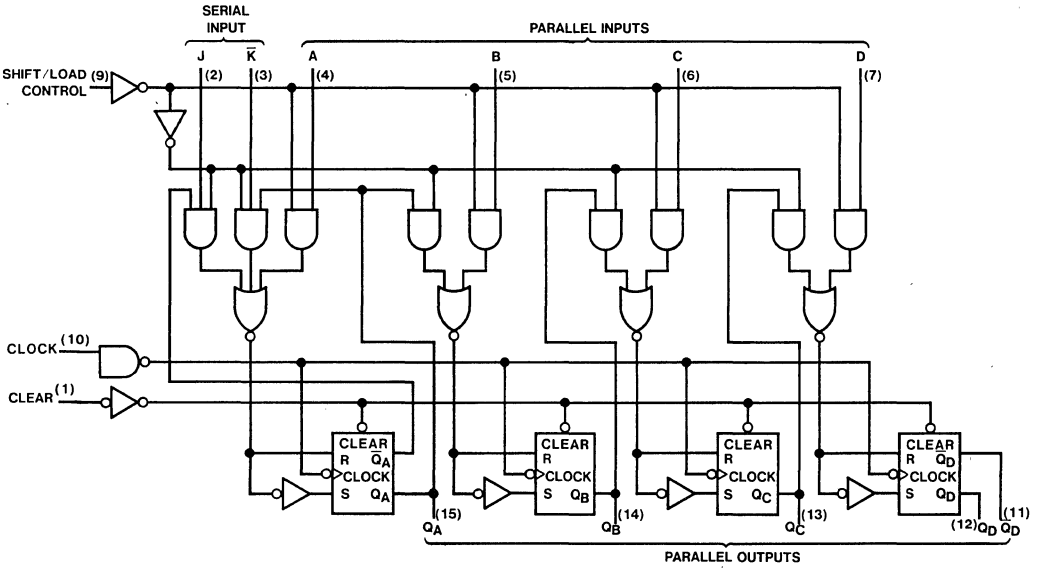
Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	39		25	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		14	22		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		17	26		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		19	30		25	38	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

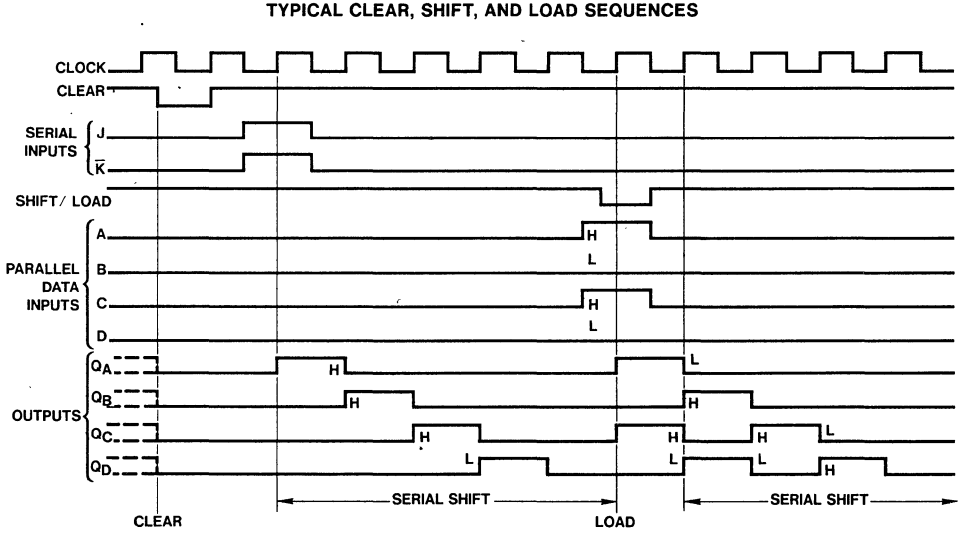
Note 3: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V, to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Logic Diagram



TL/F/6408-2

Timing Diagram



TL/F/6408-3

National Semiconductor

DM54LS196/DM74LS196, DM54LS197/DM74LS197 Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (196) or a divide-by-two and a divide-by-eight counter (197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

TYPICAL COUNT CONFIGURATIONS LS196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

LS197

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input
- Typical count frequency
  - Clock 1 40 MHz
  - Clock 2 20 MHz
- Typical power dissipation 80 mW

Absolute Maximum Ratings (Note 1)

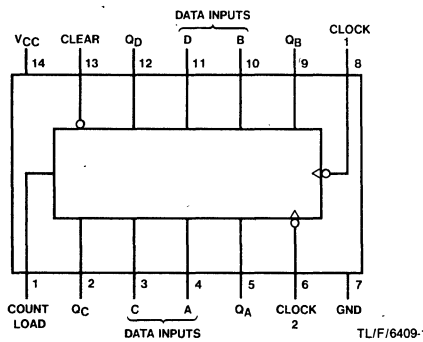
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram (Dual-In-Line Package)

54LS196 (J) **74LS196 (N)**
54LS197 (J) **74LS197 (N)**

Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.



TL/F/6409-1

Recommended Operating Conditions

Symbol	Parameter		DM54LS196			DM74LS196			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width	Clock 1	20			20			ns
		Clock 2	30			30			
		Clear	15			15			
		Load	20			20			
t_{SU}	Setup Time (Note 1)	Data High	8↑			8↑			ns
		Data Low	12↑			12↑			
t_H	Hold Time (Note 1)	Data High	0↑			0↑			ns
		Data Low	6↑			6↑			
t_{EN}	Count Enable Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Note 4: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

'LS196 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V	Clock 1			0.2	mA
			Clock 2			0.4	
			Clear			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clock 1			40	μA
			Clock 2			80	
			Clear			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock 1			−2.4	mA
			Clock 2			−2.8	
			Clear			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the CLOCK 2 input. This permits driving the CLOCK 2 input while maintaining full fan-out capability.

'LS196 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock 1 to Q_A	30	40		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		8	15		11	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		13	20		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		10	24		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		22	33		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		22	57		45	68	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		22	62		48	72	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		12	18		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		12	45		36	54	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		11	30		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		29	44		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		27	41		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		30	45		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		29	51		40	60	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS197			DM74LS197			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width	Clock 1	20			20			ns
		Clock 2	30			30			
		Clear	15			15			
		Load	20			20			
t_{SU}	Setup Time (Note 1)	Data High	8↑			8↑			ns
		Data Low	12↑			12↑			
t_H	Hold Time (Note 1)	Data High	0↑			0↑			ns
		Data Low	6↑			6↑			
t_{EN}	Count Enable Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 3: $C_L = 50$ pF and $R_L = 2$ kΩ.

Note 4: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

'LS197 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Clock 1			0.2	mA
			Clock 2			0.2	
			Clear			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clock 1			40	μA
			Clock 2			40	
			Clear			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock 1			−2.4	mA
			Clock 2			−1.3	
			Clear			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the CLOCK 2 input. This permits driving the CLOCK 2 input while maintaining full fan-out capability.

'LS197 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock 1 to Q_A	30	40		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		8	15		11	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		14	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		12	19		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		15	35		29	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		22	51		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		25	63		50	75	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		30	78		65	98	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		35	95		71	106	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		15	27		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		29	44		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		20	39		29	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		30	45		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		29	51		40	60	ns

Function Tables

LS196
Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS196
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS197
(See Note A)

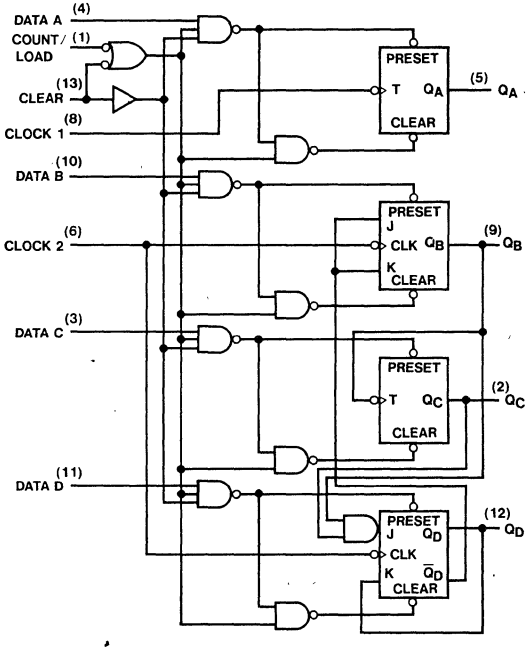
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Level, L = Low Level

Note A: Output Q_A connected to clock-2 input.
Note B: Output Q_D connected to clock-1 input.

Logic Diagrams

LS196



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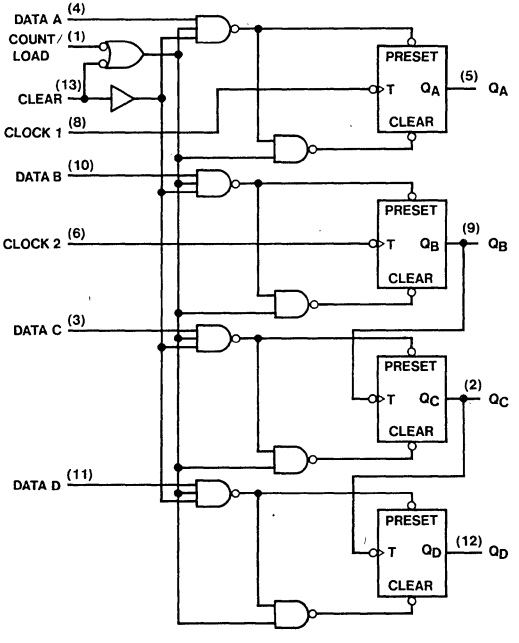
LS197



TL/F/6409-3

4

National Semiconductor

DM54LS221/DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-low trigger transition input and pin (B) is an active-high transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to V_{CC} noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⌐⌙). To obtain the best and trouble free operation from this device please read operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- A dual, highly stable one-shot
- Compensated for V_{CC} and temperature variations
- Pin-out identical to 'LS123 (Note 1)
- Output pulse width range from 30 ns to 70 seconds
- Hysteresis provided at (B) input for added noise immunity

Note 1: The pin-out is identical to 'LS123 but, functionally it is not; refer to Operating Rules #10 in this datasheet.

- Direct reset terminates output pulse
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

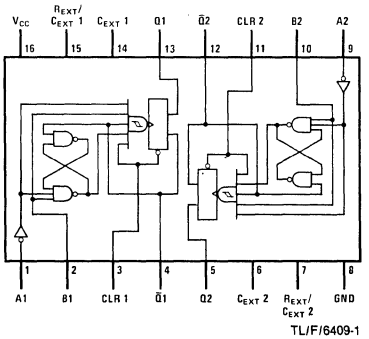
Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

Connection Diagram

Dual-In-Line Package



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DM54LS221 (J) **DM74LS221 (N)**

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌐⌙	⌐⌙
H	↓	H	⌐⌙	⌐⌙
* ↑	L	H	⌐⌙	⌐⌙

H = High Logic Level

L = Low Logic Level

X = Can Be Either Low or High

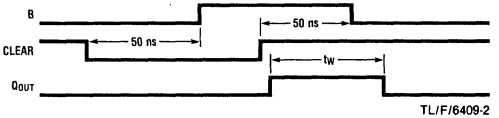
↑ = Positive Going Transition

↓ = Negative Going Transition

⌐⌙ = A Positive Pulse

⌐⌙ = A Negative Pulse

*This mode of triggering requires first the B input be set from a low to high level while the CLEAR input is maintained at logic low level. Then with the B input at logic high level, the CLEAR input whose positive transition from low to high will trigger an output pulse.



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Recommended Operating Conditions

Symbol	Parameter		DM54LS221			DM74LS221			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)			1	2		1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1		0.8	1		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1	2		1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		0.8	0.9		0.8	0.9		V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	Data	40			40			ns
		Clear	40			40			
t_{REL}	Clear Release Time		15			15			ns
$\frac{dV}{dt}$	Rate of Rise or Fall of Schmitt Input (B)				1			1	$\frac{V}{s}$
$\frac{dV}{dt}$	Rate of Rise or Fall of Logic Input (A)				1			1	$\frac{V}{\mu s}$
R_{EXT}	External Timing Resistor		1.4		70	1.4		100	kΩ
C_{EXT}	External Timing Capacitance		0		1000	0		1000	μF
DC	Duty Cycle	R_T = 2 kΩ			67			67	%
		$R_T = R_{EXT}$ (Max)			90			90	
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A1, A2			−0.4	mA
			B			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		4.7	11	mA
			Triggered		19	27	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) to (Output)	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output	A1, A2 to Q	$C_{EXT} = 80$ pF, $R_{EXT} = 2$ kΩ, $C_L = 15$ pF, $R_L = 2$ kΩ		45	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q			35	55	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A1, A2 to $\overline{Q}$			50	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			40	65	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			45	65	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q			40	55	ns
$t_{W(out)}$ Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	$C_{EXT} = 0$, $R_{EXT} = 2$ kΩ, $R_L = 2$ kΩ, $C_L = 15$ pF	20	47	70	ns
$t_{W(out)}$ Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	$C_{EXT} = 100$ pF, $R_{EXT} = 10$ kΩ, $R_L = 2$ kΩ, $C_L = 15$ pF	600	670	750	ns
		$C_{EXT} = 1$ μF, $R_{EXT} = 10$ kΩ, $R_L = 2$ kΩ, $C_L = 15$ pF	6	6.7	7.5	ns
		$C_{EXT} = 80$ pF, $R_{EXT} = 2$ kΩ, $R_L = 2$ kΩ, $C_L = 15$ pF	70	120	150	ns

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to approximately 1000 μF. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitor may be used. For large time constants use tantalum or special aluminum capacitors. If timing capacitor has leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS221 one-shot and should not be used.
3. For $C_X >> 1000$ pF, the output pulse width (T_W) is defined as follows:

$$T_W = KR_XC_X$$

where [R_X is in kΩ]
[C_X is in pF]
[T_W is in ns]

$K \approx Ln2 = 0.70$

4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

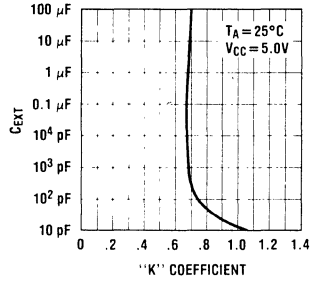


FIGURE 1

5. For $C_X < 1000$ pF see *Figure 2* for T_W vs C_X family curves with R_X as a parameter.

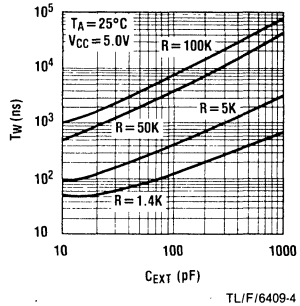
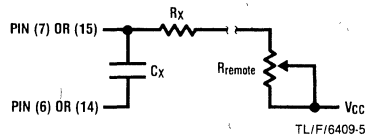


FIGURE 2

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:



Note: "R_{remote}" should be as close to the one-shot as possible.

FIGURE 3

7. Output pulse width versus V_{CC} and temperatures: *Figure 4* depicts the relationship between pulse width variation versus V_{CC}. *Figure 5* depicts pulse width variation versus temperatures.

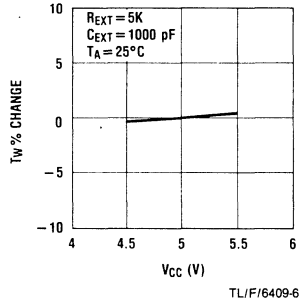


FIGURE 4

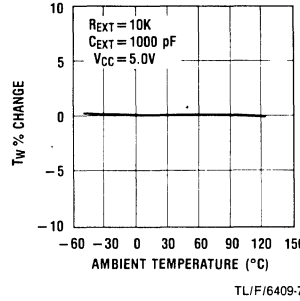


FIGURE 5

8. Duty cycle is defined as $T_W/T \times 100$ in percentage, if it goes above 50% the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes output pulse width to vary, or jitter (a function of the R_{EXT} only). To reduce jitter, R_{EXT} should be as large as possible, for example, with $R_{EXT} = 100k$ jitter is not appreciable until the duty cycle approaches 90%.

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation such that the output pulse width will be accurate.

10. Although the 'LS221's pin-out is identical to the 'LS123 it should be remembered that they are not functionally identical. The 'LS123 is a retriggerable device such that the output is dependent upon the input transitions when its output "Q" is at the "High" state. Furthermore, it is recommended for the 'LS123 to externally ground the C_{EXT} pin for improved system performance. However, this pin on the 'LS221 is not an internal connection to the device ground. Hence, if substitution of an 'LS221 onto an 'LS123 design layout where the C_{EXT} pin is wired to the ground, the device will not function.

11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

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* For further detailed device characteristics and output performance, please refer to the NSC one-shot application note AN-366.

National Semiconductor

DM54LS240/DM74LS240, DM54LS241/DM74LS241 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS − 12 mA
  - 74LS − 15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

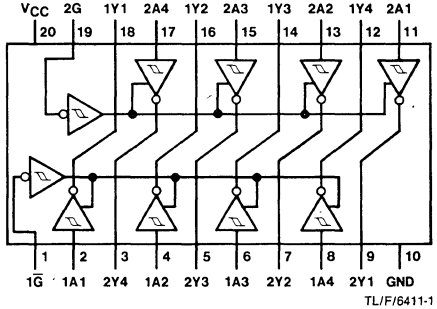
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

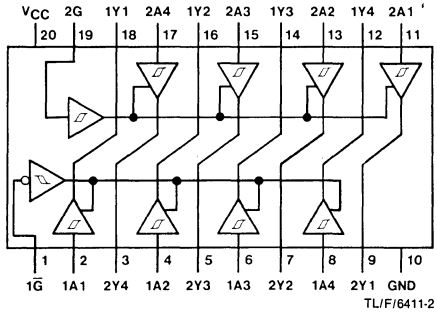
Dual-In-Line Package



TL/F/6411-1

54LS240 (J) 74LS240 (N)

Dual-In-Line Package



TL/F/6411-2

54LS241 (J) 74LS241 (N)

Function Tables

LS240

$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

LS241

G	$\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = Logic Low Level
H = Logic High Level
X = Either Logic Low or Logic High Level
Z = High Impedance

Recommended Operating Conditions

Symbol	Parameter	DM74LS240, 241			DM54LS240, 241			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High	LS240, LS241		13	23	mA
			Outputs Low	LS240		26	44	
				LS241		27	46	
			Outputs Disabled	LS240		29	50	
				LS241		32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF, $R_L = 667\Omega$	LS240	3	9	14	ns
			LS241	5	12	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF, $R_L = 667\Omega$	LS240	5	12	18	ns
			LS241	7	12	18	
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF, $R_L = 667\Omega$	LS240	10	20	30	ns
			LS241	10	20	30	
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF, $R_L = 667\Omega$	LS240	5	15	23	ns
			LS241	10	15	23	
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, $R_L = 667\Omega$	LS240	7	15	25	ns
			LS241	8	15	25	
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, $R_L = 667\Omega$	LS240	5	10	18	ns
			LS241	5	10	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF, $R_L = 667\Omega$	LS240	5	11	18	ns
			LS241	6	14	21	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF, $R_L = 667\Omega$	LS240	6	15	22	ns
			LS241	6	15	22	
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF, $R_L = 667\Omega$	LS240	12	22	33	ns
			LS241	12	22	33	
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF, $R_L = 667\Omega$	LS240	6	18	26	ns
			LS241	11	18	26	

National Semiconductor

DM54LS242/DM74LS242, DM54LS243/DM74LS243 Quadruple Bus Transceivers

General Description

These four data line transceivers are designed for asynchronous two-way communications between data buses. They can be used to drive terminated lines down to 133 ohms.

Features

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

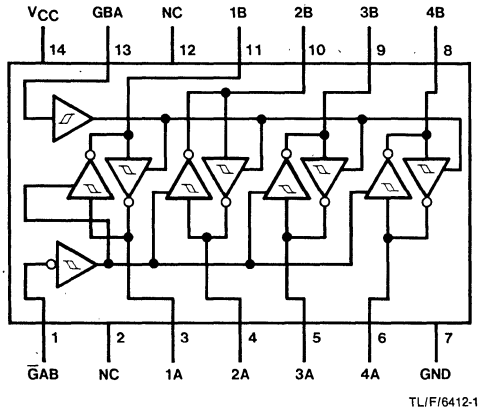
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
Any G	7V
A or B	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

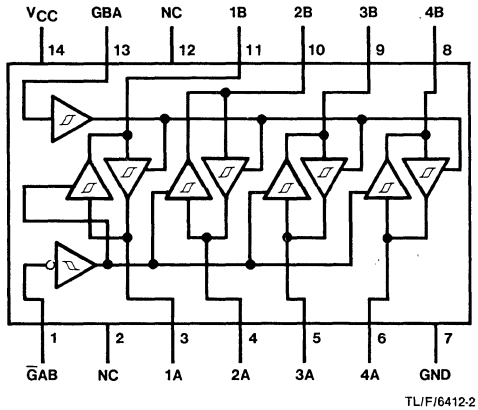
Dual-In-Line Package



TL/F/6412-1

54LS242 (J) 74LS242 (N)

Dual-In-Line Package



TL/F/6412-2

54LS243 (J) 74LS243 (N)

Function Table

Control Inputs		LS242 Data Port Status		LS243 Data Port Status	
$\overline{G}AB$	GBA	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	•	•	•	•
H	L	ISOLATED		ISOLATED	
L	L	I	$\overline{O}$	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

I = Input, O = Output, $\overline{O}$ = Inverting Output.

H = High Logic Level, L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS242, 243			DM74LS242, 243			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				40	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V	A or B			0.1	mA
			V_I = 7V	Any G			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High	LS242, LS243		22	38	mA
			Outputs Low	LS242		29	50	
				LS243				
			Outputs Disabled	LS242		29	50	
				LS243		32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF, $R_L = 667\Omega$	LS242	3	9	14	ns
			LS243	5	12	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF, $R_L = 667\Omega$	LS242	5	12	18	ns
			LS243	7	12	18	
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF, $R_L = 667\Omega$	LS242	10	20	30	ns
			LS243	10	20	30	
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF, $R_L = 667\Omega$	LS242	5	15	23	ns
			LS243	10	15	23	
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, $R_L = 667\Omega$	LS242	7	15	25	ns
			LS243	8	15	25	
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, $R_L = 667\Omega$	LS242	5	10	18	ns
			LS243	5	10	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF, $R_L = 667\Omega$	LS242	5	11	18	ns
			LS243	6	14	21	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF, $R_L = 667\Omega$	LS242	6	15	22	ns
			LS243	6	15	22	
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF, $R_L = 667\Omega$	LS242	12	22	33	ns
			LS243	12	22	33	
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF, $R_L = 667\Omega$	LS242	6	18	26	ns
			LS243	11	18	26	

National Semiconductor

DM54LS244/DM74LS244
Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS − 12 mA
  - 74LS − 15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

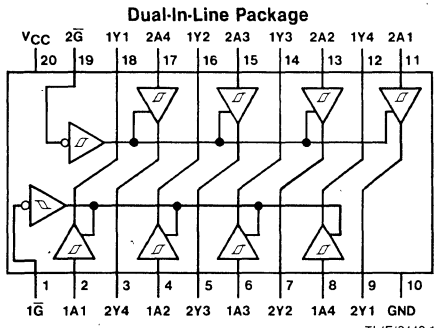
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram



54S244 (J) **74S244 (N)**

Function Table

$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Recommended Operating Conditions

Symbol	Parameter	DM54LS244			DM74LS244			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			13	23	mA
			Outputs Low			27	46	
			Outputs Disabled			32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF $R_L = 667\Omega$	5	12	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF $R_L = 667\Omega$	7	12	18	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF $R_L = 667\Omega$	10	20	30	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF $R_L = 667\Omega$	10	15	23	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF $R_L = 667\Omega$	8	15	25	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF $R_L = 667\Omega$	5	10	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF $R_L = 667\Omega$	6	14	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF $R_L = 667\Omega$	6	15	22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF $R_L = 667\Omega$	12	22	33	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF $R_L = 667\Omega$	11	18	26	ns

National Semiconductor

DM54LS245/DM74LS245 TRI-STATE® Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-directional bus transceiver in a high-density 20-pin package
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  54LS 12 mA
  74LS 24 mA
- I_{OH} (source current)
  54LS −12 mA
  74LS −15 mA

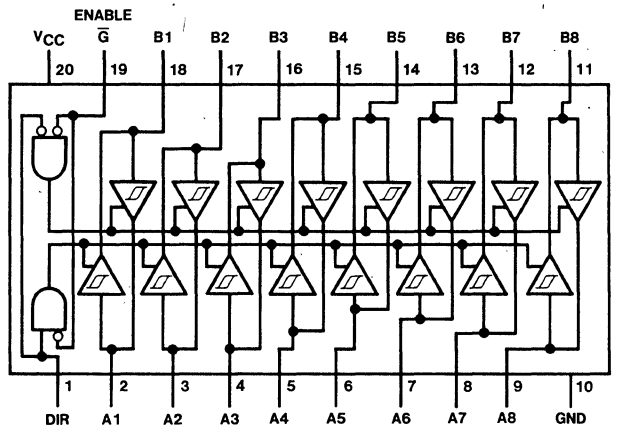
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6413-1

54LS245 (J) 74LS245 (N)

Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

Recommended Operating Conditions

Symbol	Parameter	DM54LS245			DM74LS245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				10	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or $\overline{G}$	V_I = 7V			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs High		V_{CC} = Max		48	70	mA
		Outputs Low				62	90	
		Outputs at Hi-Z				64	95	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output shorted at a time, not to exceed one second duration.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	DM54/74 LS245			Units
			Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 45 pF, R_L = 667 Ω		8	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			8	12	ns
t_{PZL}	Output Enable Time to Low Level			27	40	ns
t_{PZH}	Output Enable Time to High Level			25	40	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 667 Ω		15	25	ns
t_{PHZ}	Output Disable Time from High Level			15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 150 pF, R_L = 667 Ω		10	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			11	17	ns
t_{PZL}	Output Enable Time to Low Level			30	45	ns
t_{PZH}	Output Enable Time to High Level			30	45	ns

National Semiconductor

DM54LS247/DM74LS247, DM54LS248/DM74LS248, DM54LS249/DM74LS249 BCD-to-Seven Segment Decoders/Drivers

General Description

The DM54LS247/DM74LS247 and DM54LS248/DM74LS248 are electrically and functionally identical to the DM54LS47/DM74LS47 and DM54LS48/DM74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The DM54LS249/DM74LS249 is a 16-pin version of the 14-pin DM54LS49/DM74LS49. Included in the DM54LS249/DM74LS249 circuit is the full functional capability for lamp test and ripple blanking, which is not available in the DM54LS49/DM74LS49 circuit. The DM54LS247/DM74LS247, DM54LS248/DM74LS248, and DM54LS249/DM74LS249 compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The DM54LS247/DM74LS247 features active-low outputs designed for driving indicators directly, and the DM54LS248/DM74LS248 and DM54LS249/DM74LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Features

- All circuit types feature lamp intensity modulation capability

54LS247/74LS247

- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

54LS248/74LS248

- Internal pull-ups eliminate need for external resistors
- Lamp-test provision
- Leading/trailing zero suppression

54LS249/74LS249

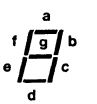
- Open-collector outputs
- Lamp-test provision
- Leading/trailing zero suppression

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Segment Identification



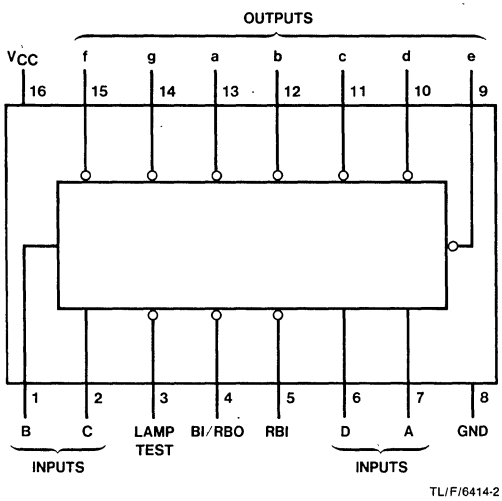
Numerical Designations and Resultant Displays

TL/F/6414-1

Type	Driver Outputs				Typical Power Dissipation	Packages
	Active Level	Output Configuration	Sink Current	Max Voltage		
DM54LS247	low	open-collector	12 mA	15 V	35 mW	J
DM54LS248	high	2 kΩ pull-up	2 mA	5.5 V	125 mW	J
DM54LS249	high	open-collector	4 mA	5.5 V	40 mW	J
DM74LS247	low	open-collector	24 mA	15 V	35 mW	N
DM74LS248	high	2 kΩ pull-up	6 mA	5.5 V	125 mW	N
DM74LS249	high	open-collector	8 mA	5.5 V	40 mW	N

Connection Diagrams

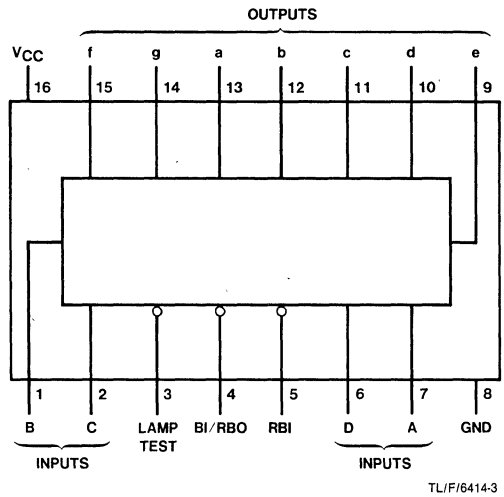
Dual-In-Line Package



TL/F/6414-2

54LS247 (J) 74LS247 (N)

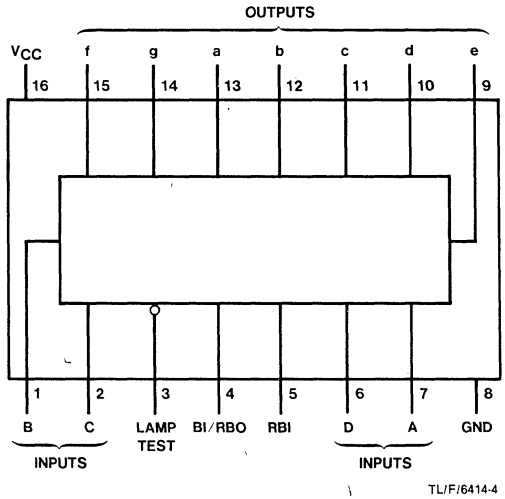
Dual-In-Line Package



TL/F/6414-3

54LS248 (J) 74LS248 (N)

Dual-In-Line Package



TL/F/6414-4

54LS249 (J) 74LS249 (N)

Function Tables

DM54LS247/DM74LS247

Decimal or Function	Inputs						BI/RBO†	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	1
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

DM54LS248/DM74LS248, DM54LS249/DM74LS249

Decimal or Function	Inputs						BI/RBO†	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	1
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

† BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Recommended Operating Conditions

Symbol	Parameter	DM54LS247			DM74LS247			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−50			−50	μA
I_{OL}	Low Level Output Current (a thru g)			12			24	mA
I_{OL}	Low Level Output Current (BI/RBO)			1.6			3.2	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS247 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min, V_{IL} = Max I_{OH} = Max V_{IH} = Min		2.4	4.2		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Min, V_O = 15V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = Max/2 V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current (BI/RBO)	V_{CC} = Max		−0.3		−2	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			7	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'LS247 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) to (Output)	$R_L = 665\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A or RBI to Any Output			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or RBI to Any Output			100	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS248			DM74LS248			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			5.5			5.5	V
I_{OH}	High Level Output Current (BI/RBO)			−50			−50	μA
	High Level Output Current (a thru g)			−100			−100	
I_{OL}	Low Level Output Current (a thru g)			2			6	mA
I_{OL}	Low Level Output Current (BI/RBO)			1.6			3.2	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS248 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	4.2		V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 0.85V V_{IH} = Min, V_{IL} = Max		−1.3	−2		mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.24	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 2 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)		−0.3		−2	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			25	38	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ(A), 6 kΩ(RBI)						Units
		C_L = 15pF			C_L = 50pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Output			100			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Output			100			100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	RBI to Output			100			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	RBI to Output			100			100	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS249			DM74LS249			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			5.5			5.5	V
I_{OH}	High Level Output Current (BI/RBO)			−50			−50	μA
I_{OL}	Low Level Output Current (a thru g)			4			8	mA
I_{OL}	Low Level Output Current (BI/RBO)			1.6			3.2	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS249 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min, V_{IL} = Max I_{OH} = Max V_{IH} = Min		2.4	4.2		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = Max/2 V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current (BI/RBO)	V_{CC} = Max		−0.3		−2	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			8	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

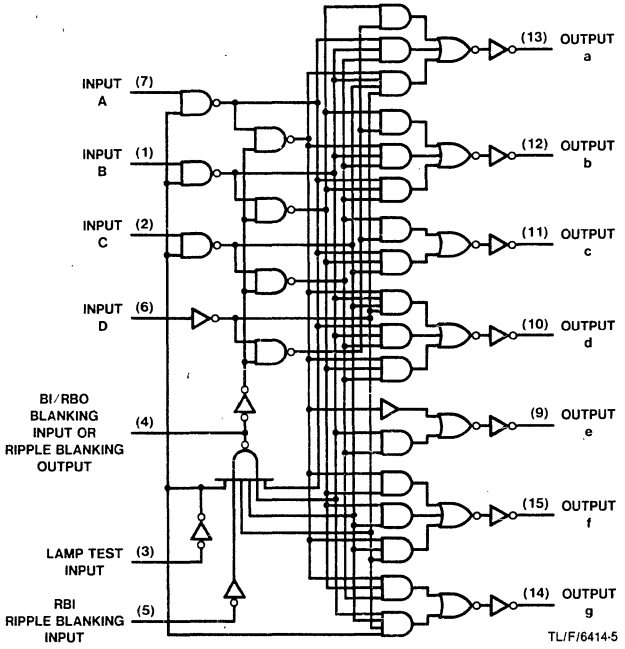
Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

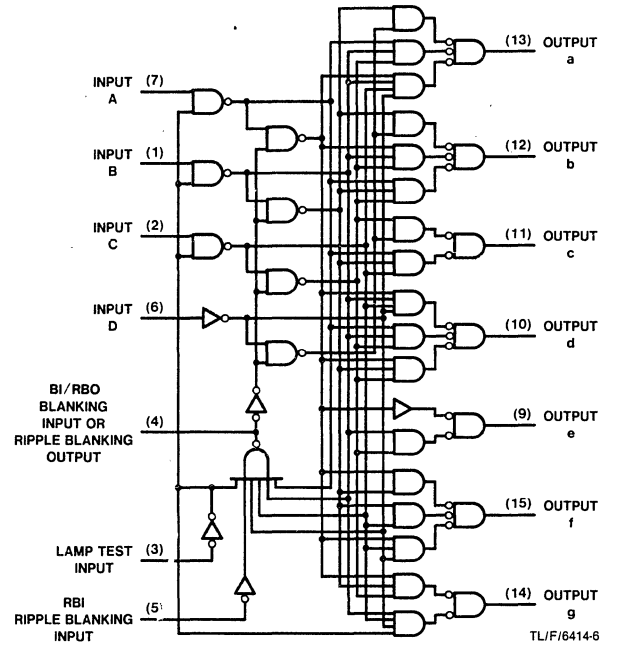
Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$(A), 6 kΩ(RBI)						Units
		$C_L = 15pF$			$C_L = 50pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Output			100			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Output			100			100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	RBI to Output			100			100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	RBI to Output			100			100	ns

Logic Diagrams

DM54LS247/DM74LS247



DM54LS248/DM74LS248, DM54LS249/DM74LS249



National Semiconductor

DM54LS251/DM74LS251 TRI-STATE® Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of LS151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Maximum number of common outputs
  - 54LS 49
  - 74 LS 129
- Typical propagation delay time (D to Y)
  - 54LS 17 ns
  - 74LS 17 ns
- Typical power dissipation
  - 54LS 35 mW
  - 74LS 35 mW

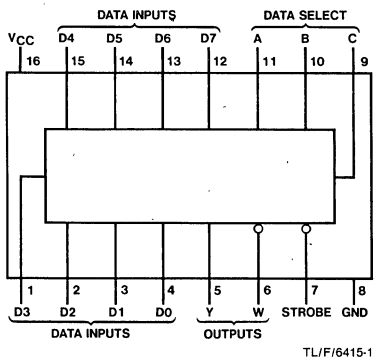
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6415-1

54LS251 (J) **74LS251 (N)**

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1...D7 = The Level of the respective D input.

Recommended Operating Conditions

Symbol	Parameter	DM54LS251			DM74LS251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			7.1	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with the outputs open, STROBE grounded, and all other inputs at 4.5V.

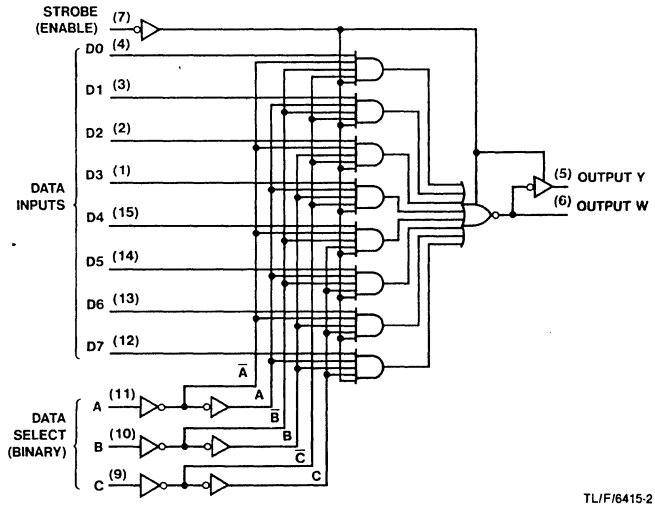
Note 4: I_{CC2} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 667\Omega$						Units
		$C_L = 45$ pF			$C_L = 150$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C (4 Levels) to Y		29	45		35	53	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C (4 Levels) to Y		28	45		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C (3 Levels) to W		20	33		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C (3 Levels) to W		21	33		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to Y		17	28		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to Y		18	28		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to W		10	15		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to W		9	15		16	25	ns
t_{PZH} Output Enable Time to High Level Output	Strobe to Y		30	45		40	60	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to Y		26	40		34	51	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)	Strobe to Y		30	45				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)	Strobe to Y		15	25				ns
t_{PZH} Output Enable Time to High Level Output	Strobe to W		17	27		26	40	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to W		24	40		31	47	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)	Strobe to W		37	55				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)	Strobe to W		15	25				ns

Note 1: $C_L = 5$ pF.

Logic Diagram



National Semiconductor

DM54LS253/DM74LS253 TRI-STATE® Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of LS153 with same pinout
- Schottky-diode-clamped transistors
- Permit multiplexing from N-lines to one line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fanout totem-pole outputs
- Typical propagation delay
  - Data to output 12 ns
  - Select to output 21 ns
- Typical power dissipation 35 mW

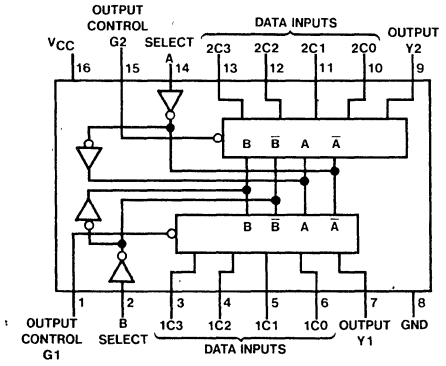
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6416-1

54LS253 (J) 74LS253 (N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (off).

Recommended Operating Conditions

Symbol	Parameter	DM54LS253			DM74LS253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			7	12	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			8.5	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, and all the inputs grounded.

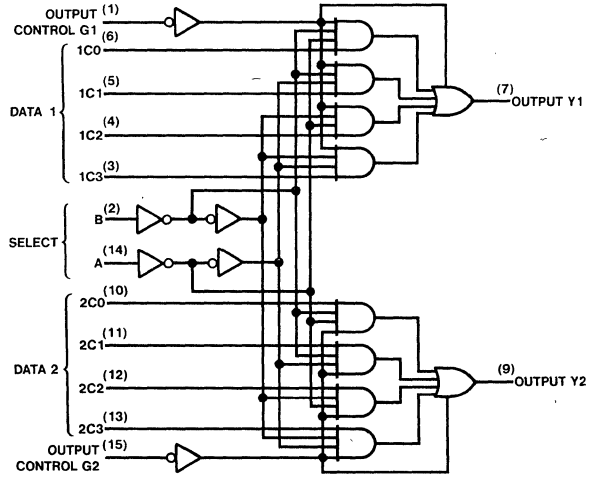
Note 4: I_{CC2} is measured with the outputs open, OUTPUT CONTROL at 4.5V and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 667\Omega$						Units
		$C_L = 45$ pF			$C_L = 150$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		13	20		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		30	45		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		21	32		29	44	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y		10	18		20	32	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y		15	23		23	35	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)	Output Control to Y		27	41				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)	Output Control to Y		18	27				ns

Note 1: $C_L = 5$ pF.

Logic Diagram



TL/F/6416-2

National Semiconductor

DM54LS257B/DM74LS257B, DM54LS258B/DM74LS258B TRI-STATE® Quad 2-Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions LS157 and LS158 with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input 12 ns
- Typical power dissipation
  LS257B 50 mW
  LS258B 35 mW

Absolute Maximum Ratings (Note 1)

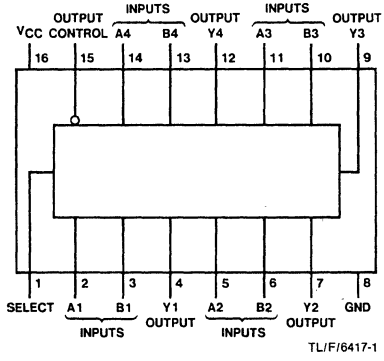
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

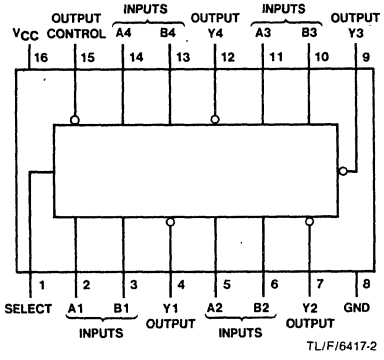
Connection Diagrams

Dual-In-Line Package



54LS257B (J) 74LS257B (N)

Dual-In-Line Package



54LS258B (J) 74LS258B (N)

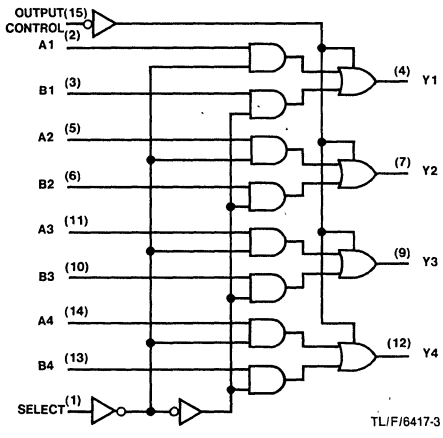
Function Table

Inputs				Output Y	
Output Control	Select	A	B	LS257	LS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

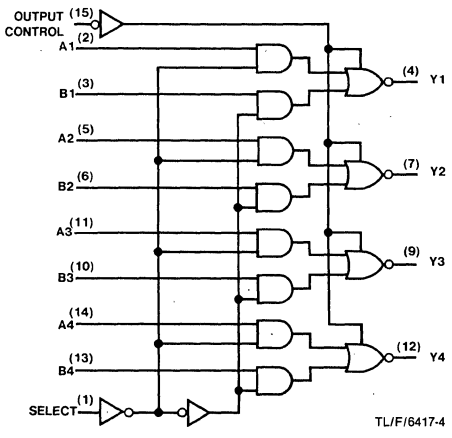
Logic Diagrams

LS257B



TL/F/6417-3

LS258B



TL/F/6417-4

Recommended Operating Conditions

Symbol	Parameter	DM54LS257B			DM74LS257B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS257B Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	μA
			Other			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			5.9	10	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 3)			9.2	16	mA
I_{CCZ}	Supply Current With Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS257B Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 667\Omega$						Units
		$C_L = 45$ pF			$C_L = 150$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		12	18		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		12	18		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		18	28		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		22	35		28	42	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y		8	15		18	27	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y		17	28		25	38	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)	Output Control to Y		17	26				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)	Output Control to Y		14	25				ns

Note 1: $C_L = 5$ pF.

Recommended Operating Conditions

Symbol	Parameter	DM54LS258B			DM74LS258B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS258B Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	μA
			Other			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			4.1	7	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 3)			9	14	mA
I_{CCZ}	Supply Current With Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS258B Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 667\Omega$						Units
		$C_L = 45$ pF			$C_L = 150$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		12	18		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		12	18		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		18	28		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		22	35		28	42	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y		8	15		18	27	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y		17	28		25	38	ns
t_{PHZ} Output Disable Time from High Level Output (Note 4)	Output Control to Y		17	26				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 4)	Output Control to Y		14	25				ns

Note 4: $C_L = 5$ pF.

National Semiconductor

DM54LS259/DM74LS259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possiblity of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Direct Replacement for Fairchild 9334
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Typical Propagation Delay Times:
  - Enable-to-Output 18 ns
  - Data-to-Output 16 ns
  - Address-to-Output 21 ns
  - Clear-to-Output 17 ns
- Fan-Out
  - I_{OL} (Sink Current)
    - 54LS259 4 mA
    - 74LS259 8 mA
  - I_{OH} (Source Current) −0.4 mA
- Typical I_{CC} 22 mA

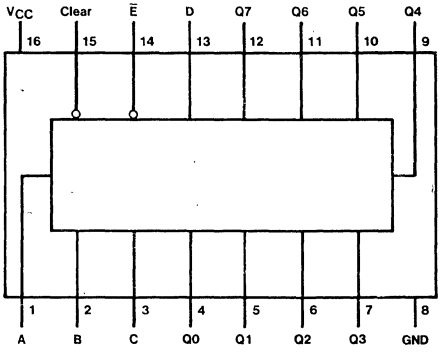
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6418-1

54LS259 (J) 74LS259 (N)

Function Table

Inputs		Output Of Addressed Latch	Each Other Output	Function
Clear	$\overline{E}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

D = the level of the data input

Q_{i0} = the level of Q_i (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

Recommended Operating Conditions

Symbol	Parameter		DM54LS259			DM74LS259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	Enable	15			15			ns
		Clear	15			15			
t_{SU}	Setup Time (Notes 1, 2 and 3)	Data	15↑			15↑			ns
		Select	15↓			15↓			
t_H	Hold Time (Notes 1 and 2)	Data	0↑			0↑			ns
		Select	0↑			0↑			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			22	36	mA

Note 1: The symbols (↓, ↑) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: Setup and hold times are with reference to the enable input.

Note 3: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all inputs at 4.5V, and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output		22	35		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output		15	24		21	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		20	32		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		13	21		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		24	38		27	41	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		18	29		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		17	27		24	36	ns

National Semiconductor

DM54LS266/DM74LS266 Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic exclusive-NOR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

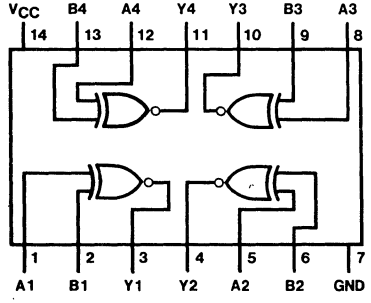
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6419-1

54LS266 (J) 74LS266 (N)

Function Table

$$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS266			DM74LS266			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			8	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low		18	30		21	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output			18	30		24	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High		18	30		21	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output			18	30		24	40	ns

National Semiconductor

DM54LS279/DM74LS279 Quad $\overline{S}$-$\overline{R}$ Latches

General Description

This device consists of four individual and independent Set-Reset Latches with active low inputs. Two of the four latches have an additional $\overline{S}$ input ANDed with the primary $\overline{S}$ input. A low on any $\overline{S}$ input while the $\overline{R}$ input is high will be stored in the latch and appear on the corresponding Q output as a high. A low on the $\overline{R}$ input while the $\overline{S}$ input is high will clear the Q output to a low. Simultaneous transition of the $\overline{R}$ and $\overline{S}$ inputs from low to high will cause the Q output to be indeterminate. Both inputs are voltage level triggered and are not affected by transition time of the input data.

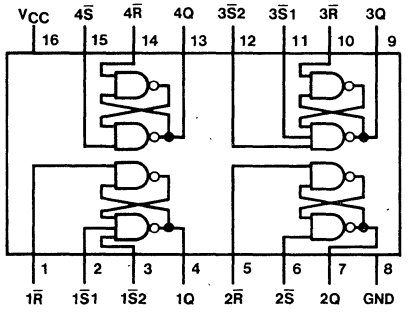
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6420-1

54LS279 (J) 74LS279 (N)

Function Table

Inputs		Output
$\overline{S}$(1)	$\overline{R}$	Q
L	L	H*
L	H	H
H	L	L
H	H	Q_O

H = high level

L = low level

Q_O = the level of Q before the indicated input conditions were established.

*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.

Note 1: For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

4

Recommended Operating Conditions

Symbol	Parameter	DM54LS279			DM74LS279			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.5		V
			DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			3.8	7	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5V, and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	$\overline{S}$ to Q		12	22		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	$\overline{S}$ to Q		9	15		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	$\overline{R}$ to Q		15	27		21	33	ns

National Semiconductor

DM54LS283/DM74LS283 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 25 ns
  Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

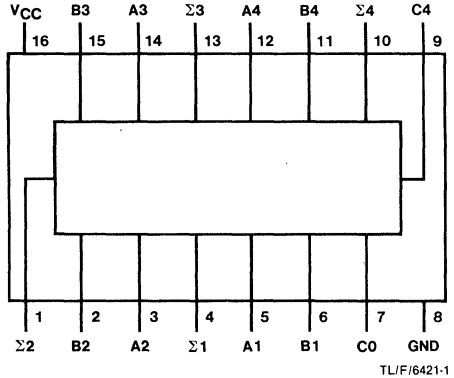
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6421-1

54LS283 (J) 74LS283 (N)

Recommended Operating Conditions

Symbol	Parameter	DM54LS283			DM74LS283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	A, B			0.2	mA
			C0			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A, B			40	μA
			C0			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A, B			−0.8	mA
			C0			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

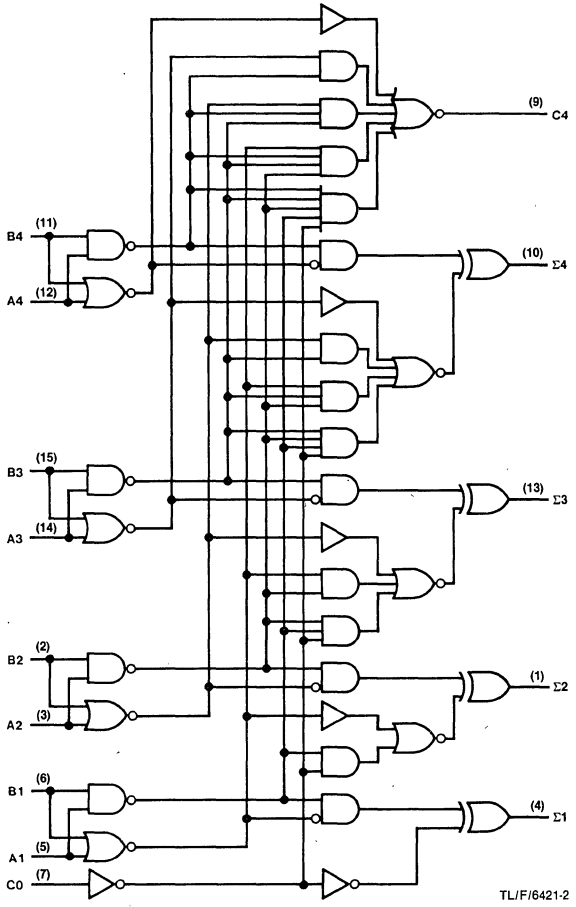
Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ1, Σ2		16	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ1, Σ2		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ3		16	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ3		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ4		16	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ4		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Ai or Bi to Σi		15	24		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Ai or Bi to Σi		15	24		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to C4		11	17		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to C4		11	17		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Ai or Bi to C4		11	17		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Ai or Bi to C4		12	17		18	26	ns

Logic Diagram

LS283



TL/F/6421-2

Function Table

Input				Output					
				When C0 = L			When C0 = H		
						When C2 = L			When C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

National Semiconductor

DM54LS290/DM74LS290 4-Bit Decade Counter

General Description

The DM54LS290/DM74LS290 counters are electrically and functionally identical to the DM54LS90/DM74LS90. Only the arrangement of the terminals has been changed for the 'LS290.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

These counters have a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS290 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

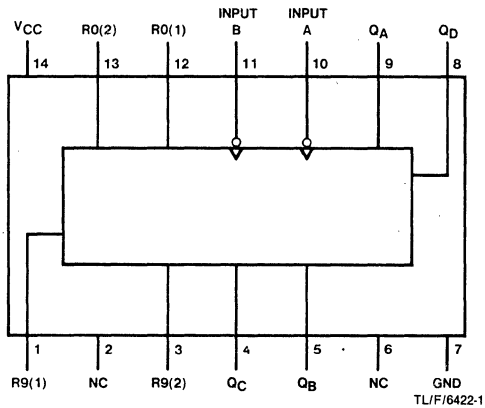
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6422-1

54LS290 (J) **74LS290 (N)**

Function Tables

BCD COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Note A: Output Q_A is connected to input B for BCD count.
H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

BI-QUINARY (5-2)
(See Note B)

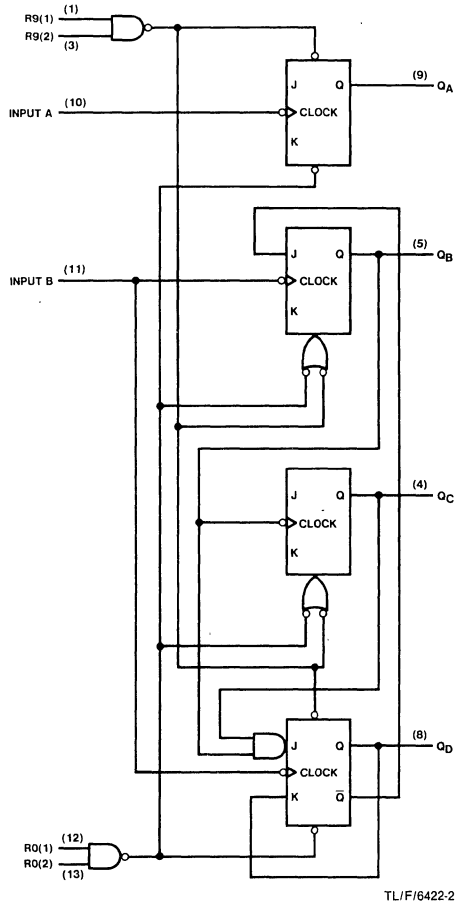
Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note B: Output Q_D is connected to input A for bi-quinary count.

RESET/COUNT TRUTH TABLE

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Logic Diagram



TL/F/6422-2

The J and K inputs shown without connection are for reference only and are functionally at a high level.

Recommended Operating Conditions

Symbol	Parameter		DM54LS290			DM74LS290			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Freq. (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Freq. (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		10	0		10	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		20	30		MHz
	B to Q_B	16			10			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50		45	68	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		20	30		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		26	40		35	53	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40		35	53	ns

Note 1: $C_L = 15$ pF and $R_L = 2\ k\Omega$.

Note 2: $C_L = 50$ pF and $R_L = 2\ k\Omega$.

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

National Semiconductor

DM54LS293/DM74LS293 4-Bit Binary Counters

General Description

The DM54LS293/DM74LS293 counters are electrically and functionally identical to the DM54LS93/DM74LS93. Only the arrangement of the terminals has been changed for the 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

All of these counters have a gated zero reset.

To use the maximum count length (four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

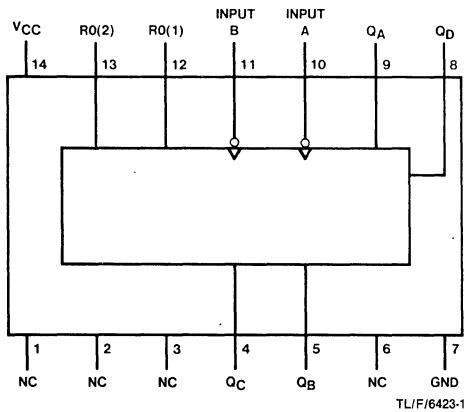
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6423-1

54LS293 (J) **74LS293 (N)**

Function Tables

COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

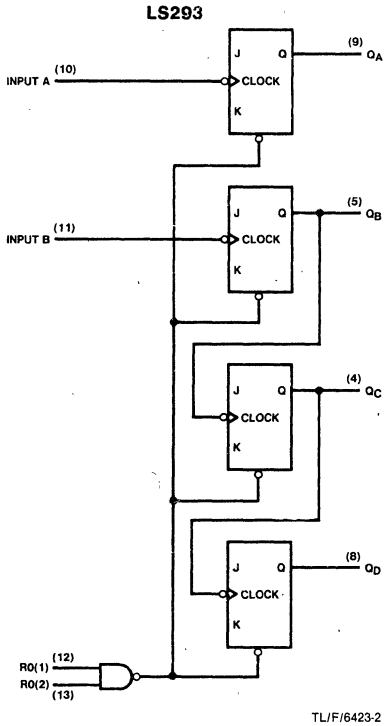
Note C: Output Q_A is connected to input B.

RESET/COUNT TRUTH TABLE

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

H = High Level, L = Low Level, X = Don't Care.

Logic Diagram



TL/F/6423-2

Note: The J and K inputs shown without connection are for reference only and are functionally at a high level.

Recommended Operating Conditions

Symbol	Parameter		DM54LS293			DM74LS293			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Freq. (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Freq. (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		10	0		10	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		20	30		MHz
	B to Q_B	16			10			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		46	70		58	87	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		46	70		62	93	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35		35	53	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		34	51		47	71	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		34	51		47	71	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40		35	53	ns

Note 1: $C_L = 15$ pF and $R_L = 2\ k\Omega$.

Note 2: $C_L = 50$ pF and $R_L = 2\ k\Omega$.

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

National Semiconductor

DM54LS298/DM74LS298 Quad 2-Multiplexers with Storage

General Description

These integrated circuits provide essentially the equivalent functional capabilities of two separate MSI functions (DM54157/DM74157 or DM54LS157/DM74LS157 and DM54175/DM74175 or DM54LS175/DM74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is entered into the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is then clocked to the output terminals on the negative-going edge of the clock pulse.

Features

- Selects one of two 4-bit data sources and stores data synchronously with system clock
- Applications:

  Dual source for operands and constants in arithmetic processor; can release processor register files for acquiring new data

  Implement separate registers capable of parallel exchange of contents, yet retain external load capability

  Universal type register for implementing various shift patterns; even has compound left-right capabilities

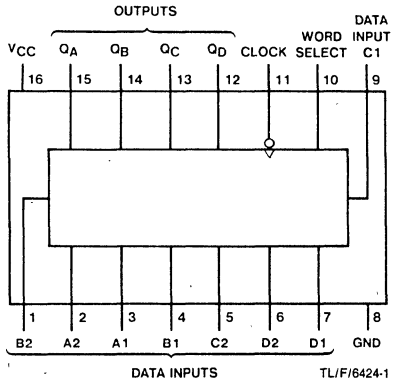
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS298 (J) 74LS298 (N)

Function Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)

L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↓ = Transition from high to low level

a1,a2, etc = The level of steady-state input at A1, A2, etc

Q_{A0}, Q_{B0}, etc = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

Recommended Operating Conditions

Symbol	Parameter		DM54LS298			DM74LS298			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Clock Pulse Width		20			20			ns
t_{SU}	Setup Time	Data	15			15			ns
		Word Select	25			25			
t_H	Hold Time	Data	5			5			ns
		Word Select	0			0			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

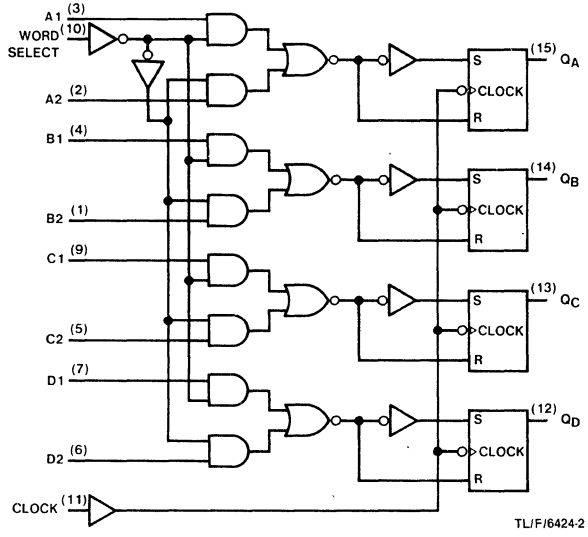
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and all inputs except CLOCK low, I_{CC} is measured after applying a momentary 4.5V, followed by ground, to the CLOCK input.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 2\ k\Omega$						Units
	$C_L = 15\ pF$			$C_L = 50\ pF$			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		18	27		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output		21	32		27	41	ns

Logic Diagram



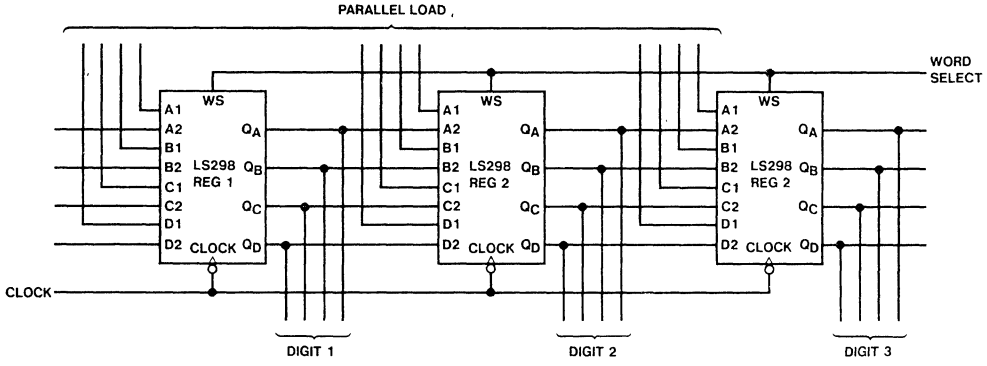
Typical Applications

Figure 1 illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

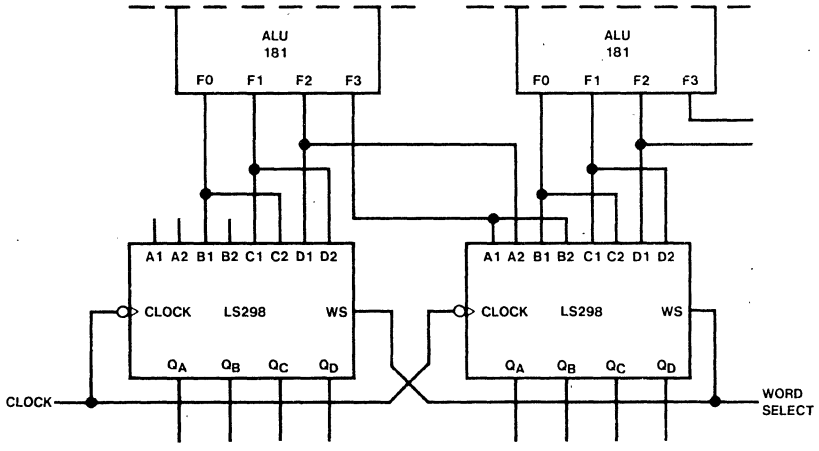
Another function that can be implemented with the LS298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.



TL/F/6424-3

FIGURE 1



TL/F/6424-4

FIGURE 2

National Semiconductor

DM54LS352/DM74LS352 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Inverting version of DM54/74LS153
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  - From data 15 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW

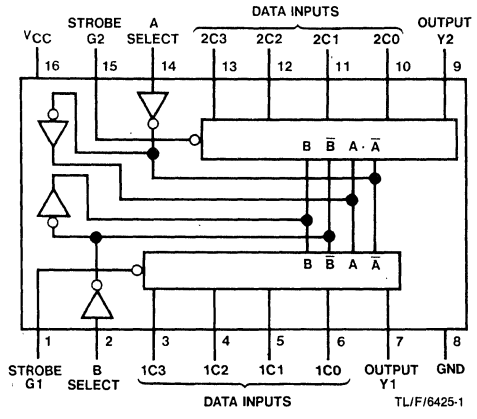
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54LS352 (J, N) **74LS352 (J, N)**

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Symbol	Parameter	DM54LS352			DM74LS352			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

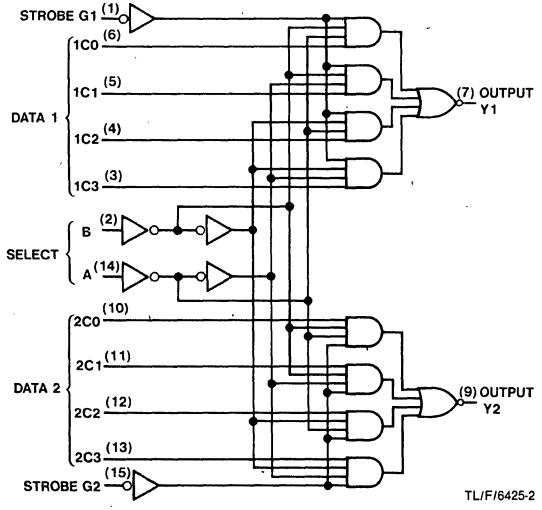
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs at ground.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		13	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		17	26		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		19	29		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		25	38		31	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		16	24		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		21	32		27	41	ns

Logic Diagram



TL/F/6425-2

National Semiconductor

DM54LS353/DM74LS353 TRI-STATE® Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply full complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- Inverting version of DM54/74LS253
- Schottky-diode clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs
- Typical propagation delay
  Data to output 12 ns
  Select to output 21 ns
- Typical power dissipation 35 mW

Absolute Maximum Ratings (Note 1)

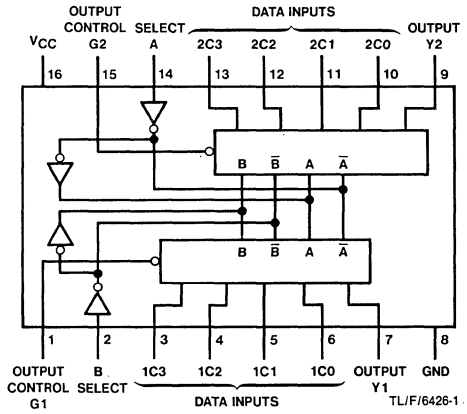
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



54LS353 (J, N) **74LS353 (J, N)**

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Recommended Operating Conditions

Symbol	Parameter	DM54LS353			DM74LS353			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			7	12	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			8.5	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, and all the inputs grounded.

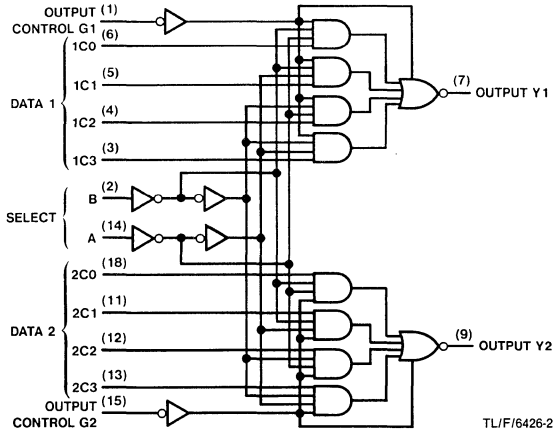
Note 4: I_{CC2} is measured with the outputs open, OUTPUT CONTROL at 4.5V and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 667\Omega$						Units
		$C_L = 45$ pF			$C_L = 150$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		17	25		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		13	20		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		30	45		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		21	32		29	44	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y		15	23		25	38	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y		15	23		23	35	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)	Output Control to Y		27	41				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)	Output Control to Y		18	27				ns

Note 1: $C_L = 5$ pF.

Logic Diagram



National Semiconductor

DM54LS365A/DM74LS365A Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

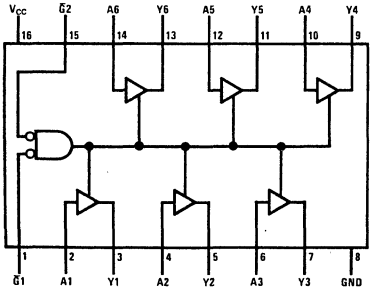
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6427-1

DM54LS365A (J) DM74LS365A (N)

Function Table

Y = A

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Sym	Parameter	DM54LS365A			DM74LS365A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	24	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	16		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output		10	16		16	25	ns
t_{PZH} Output Enable Time to High Level Output		16	30		25	40	ns
t_{PZL} Output Enable Time to Low Level Output		14	30		25	40	ns
t_{PHZ} Output Disable Time from High Level Output (Note 6)		10	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 6)		11	20				ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Note 6: $C_L = 5$ pF.

National Semiconductor

DM54LS366A/DM74LS366A Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

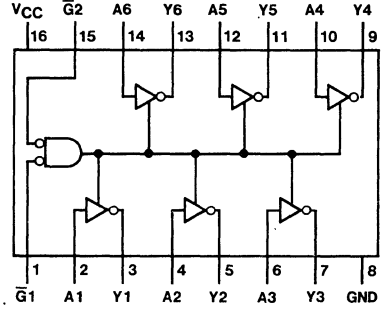
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6428-1

DM54LS366A (J) DM74LS366A (N)

Function Table

$Y = \overline{A}$

Input			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	H
L	L	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

4

Recommended Operating Conditions

Sym	Parameter	DM54LS366A			DM74LS366A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	15		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output		10	16		16	25	ns
t_{PZH} Output Enable Time to High Level Output		11	30		20	35	ns
t_{PZL} Output Enable Time to Low Level Output		18	30		30	40	ns
t_{PHZ} Output Disable Time from High Level Output (Note 6)		10	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 6)		10	20				ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Note 6: $C_L = 5$ pF.

National Semiconductor

DM54LS367A/DM74LS367A Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

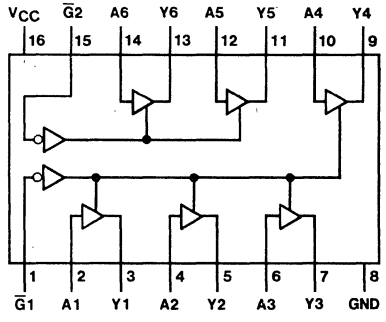
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6429-1

DM54LS367A (J) DM74LS367A (N)

Function Table

$Y = A$

Input		Output
A	$\overline{G}$	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Sym	Parameter	DM54LS367A			DM74LS367A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	24	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	16		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output		10	16		16	25	ns
t_{PZH} Output Enable Time to High Level Output		16	30		25	40	ns
t_{PZL} Output Enable Time to Low Level Output		14	30		25	40	ns
t_{PHZ} Output Disable Time from High Level Output (Note 6)		10	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 6)		11	20				ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Note 6: $C_L = 5$ pF.

National Semiconductor

DM54LS368A/DM74LS368A Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

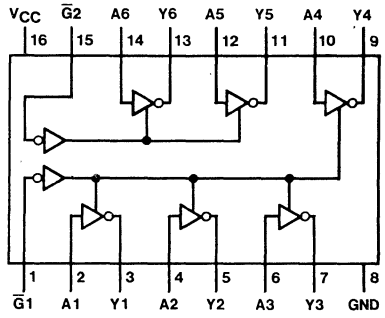
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6430-1

DM54LS368A (J) DM74LS368A (N)

Function Table

$Y = \overline{A}$

Input		Output
A	$\overline{G}$	Y
L	L	H
H	L	L
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Symbol	Parameter	DM54LS368A			DM74LS368A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max V_I = 0.4V	$\overline{G}$ Input			−0.4	

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 667Ω						Units
	C_L = 50 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	15		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output		10	18		16	25	ns
t_{PZH} Output Enable Time to High Level Output		11	30		20	35	ns
t_{PZL} Output Enable Time to Low Level Output		18	30		30	40	ns
t_{PHZ} Output Disable Time from High Level Output (Note 6)		10	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 6)		10	20				ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Note 6: C_L = 5 pF.

National Semiconductor

DM54LS373/DM74LS373, DM54LS374/DM74LS374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

(Continued next page)

Features

- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- TRI-STATE Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

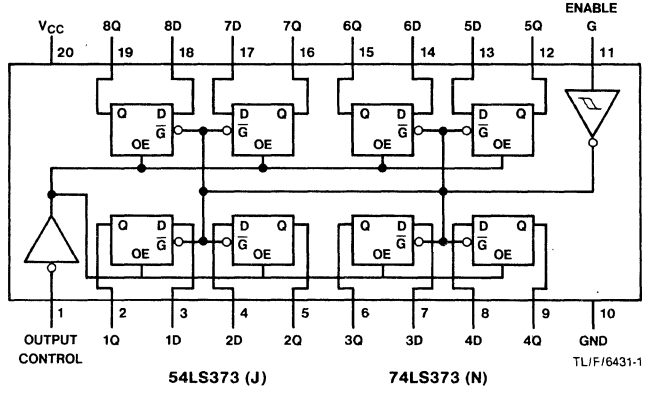
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

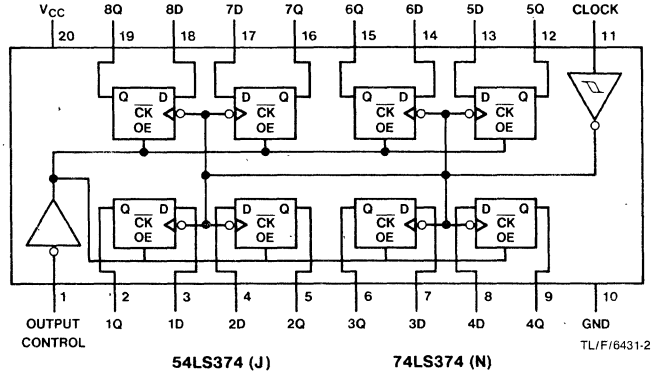
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



54LS373 (J) **74LS373 (N)**



54LS374 (J) **74LS374 (N)**

General Description (continued)

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

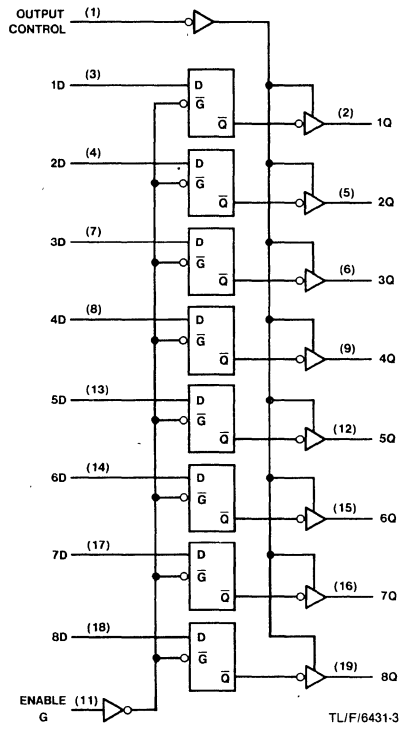
DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

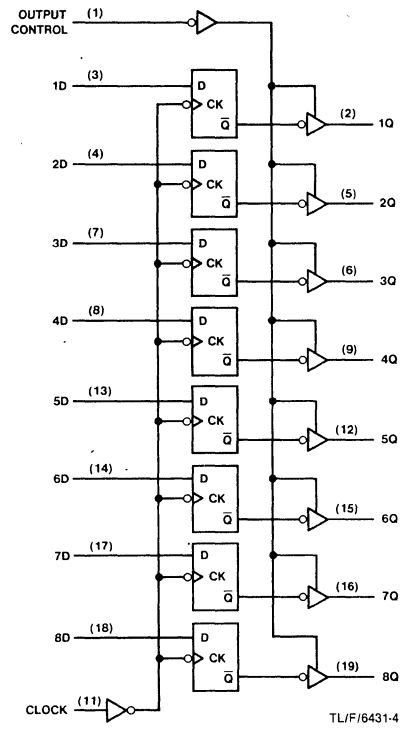
Logic Diagram

DM54/74LS373
Transparent Latches



TL/F/6431-3

DM54/74LS374
Positive-Edge-Triggered Flip-Flops



TL/F/6431-4

Recommended Operating Conditions

Symbol	Parameter		DM54LS373			DM74LS373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width	Enable High	15			15			ns
		Enable Low	15			15			
t_{SU}	Data Setup Time (Note 1)		5↓			5↓			ns
t_H	Data Hold Time (Note 1)		20↓			20↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

'LS373 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA

'LS373 Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			24	40	mA

'LS373 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 667Ω						Units
		C_L = 45 pF			C_L = 150 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Q		12	18		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Q		12	18		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Q		20	30		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Q		18	30		24	36	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Any Q		15	28		24	36	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Any Q		25	36		33	50	ns
t_{PHZ} Output Disable Time from High Level Output (Note 3)	Output Control to Any Q		12	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 3)	Output Control to Any Q		15	25				ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter		DM54LS374			DM74LS374			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 2)		0		35	0		35	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width	Clock High	15			15			ns
		Clock Low	15			15			
t_{SU}	Data Setup Time (Note 1)		20↑			20↑			ns
t_H	Data Hold Time (Note 1)		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 45$ pF and $R_L = 667\Omega$.

Note 3: $C_L = 150$ pF and $R_L = 667\Omega$.

'LS374 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA

'LS374 Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			27	45	mA

'LS374 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 667Ω						Units
	C_L = 45 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	35	50		20	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output		15	28		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output		19	28		25	38	ns
t_{PZH} Output Enable Time to High Level Output		20	28		29	44	ns
t_{PZL} Output Enable Time to Low Level Output		21	28		29	44	ns
t_{PHZ} Output Disable Time from High Level Output (Note 3)		12	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 3)		14	25				ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: C_L = 5 pF.

National Semiconductor

DM54LS386/DM74LS386 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

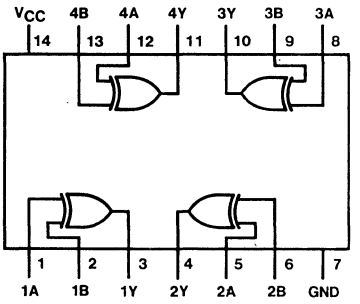
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6432-1

54LS386 (J) 74LS386 (N)

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54LS386			DM74LS386			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			8.5	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low		12	18		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output			10	17		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High		7	10		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output			6	12		10	15	ns

National Semiconductor

DM54LS390/DM74LS390 Dual 4-Bit Decade and Binary Counters

General Description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'LS390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Features

- Dual Versions of the Popular 'LS90
- 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters
- Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Version Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

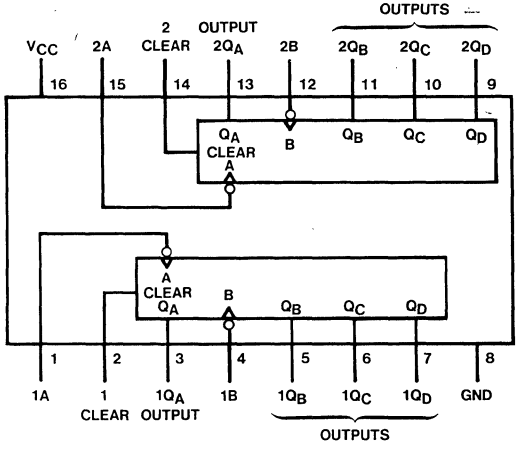
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
Clear	7V
A or B	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6433-1

54LS390 (J) 74LS390 (N)

Function Tables

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

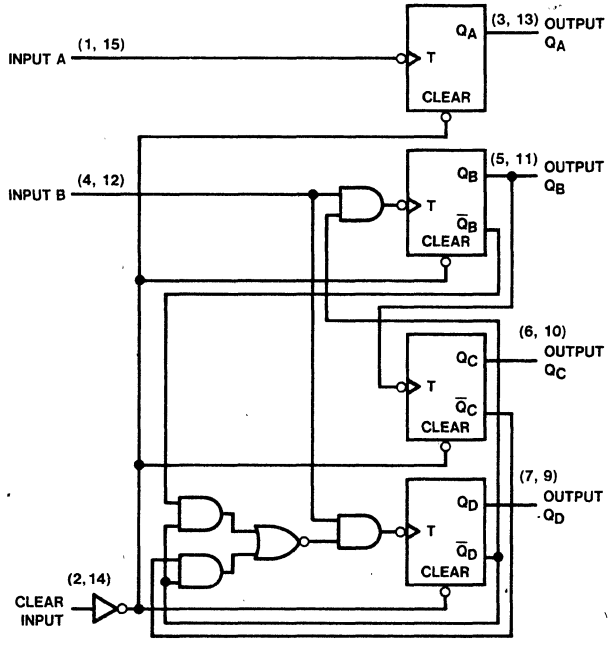
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (EACH COUNTER) (See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

A Output Q_A is connected to Input B for BCD count.
B. Output Q_D is connected to Input A for Bi-quinary count.
C H = high level, L = low level.

Logic Diagram



'LS390

TL/F/6433-2

Recommended Operating Conditions

Sym	Parameter		DM54LS390			DM74LS390			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Freq. (Note 1)	A to Q_A	0		25	0		25	MHz
		B to Q_B	0		20	0		20	
f_{CLK}	Clock Freq. (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		15	0		15	
t_W	Pulse Width (Note 1)	A	20			20			ns
		B	25			25			
		Clear High	20			20			
t_{REL}	Clear Release Time (Note 3)		25↓			25↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 2$ kΩ.

Note 2: $C_L = 50$ pF and $R_L = 2$ kΩ.

Note 3: The symbol (↓) indicates the falling edge of the clear pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
			B			−2.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			15	26	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5 and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	25	35		20	30		MHz
	B to Q_B	20	30		15	20		
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		12	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		13	20		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_C		37	60		54	81	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_C		39	60		54	81	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		13	21		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21		22	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		24	39		34	51	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		26	39		36	54	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		13	21		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		14	21		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		24	39		30	45	ns

National Semiconductor

DM54LS393/DM74LS393 Dual 4-Bit Decade and Binary Counters

General Description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The LS393 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Features

- Dual Versions of the Popular 'LS93
- 'LS393 Dual 4-Bit Binary Counter with Individual Clocks
- Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

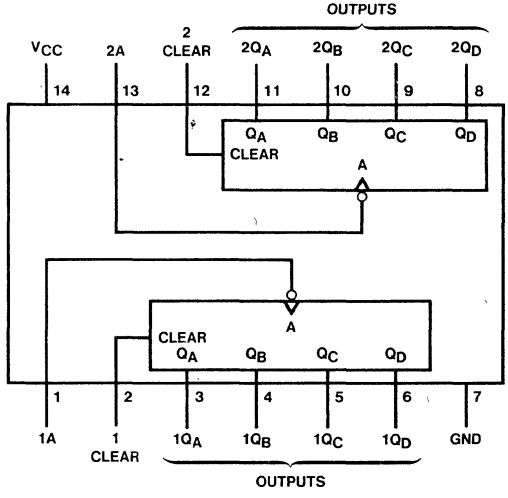
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
Clear	7V
A	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TL/F/6434-1

54LS393 (J) 74LS393 (N)

Function Table

COUNT SEQUENCE (EACH COUNTER)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter		DM54LS393			DM74LS393			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width	A	20			20			ns
		Clear High	20			20			
t_{REL}	Clear Release Time (Note 3)		25↓			25↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	μA
			A			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			15	26	mA

Note 1: C_L = 15 pF and R_L = 2 kΩ.

Note 2: C_L = 50 pF and R_L = 2 kΩ.

Note 3: The symbol (↓) indicates that the falling edge of the clear pulse is used for reference.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

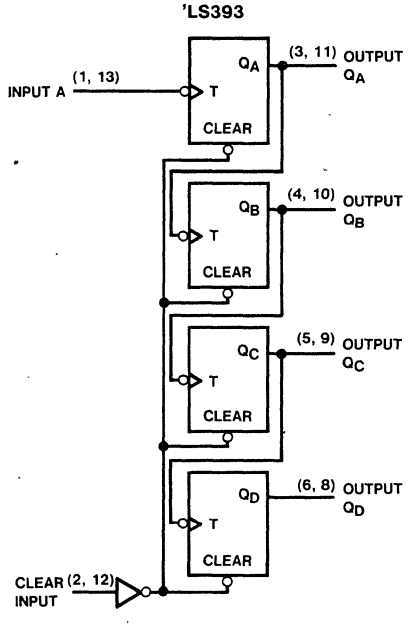
Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	25	35		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		12	20		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		13	20		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		40	60		58	87	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		40	60		58	87	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		24	39		30	45	ns

Logic Diagram



TL/F/6434-2

National Semiconductor

DM54LS465/DM74LS465, DM54LS466/DM74LS466, DM54LS467/DM74LS467, DM54LS468/DM74LS468 (DM71LS95A/DM81LS95A, DM71LS96A/DM81LS96A, DM71LS97A/DM81LS97A, DM71LS98A/DM81LS98A) TRI-STATE® Octal Buffers

General Description

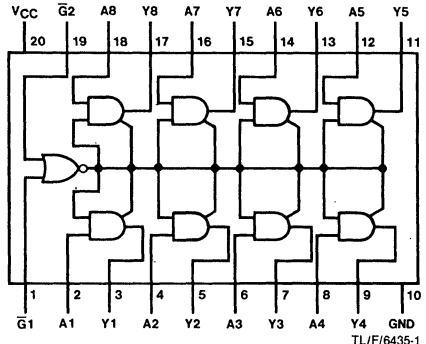
These devices provide eight, two-input buffers in each package. All employ the newest low-power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The LS465 and LS467 present true data at the outputs, while the LS466 and LS468 are inverting. On the LS465 and LS466 versions, all eight TRI-STATE enable lines are common, wth access through a 2-input NOR gate. On the LS467 and LS468 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM54/74365, 366, 367, and 368 (DM70/8095, 96, 97, and 98) TRI-STATE hex buffers.

Features

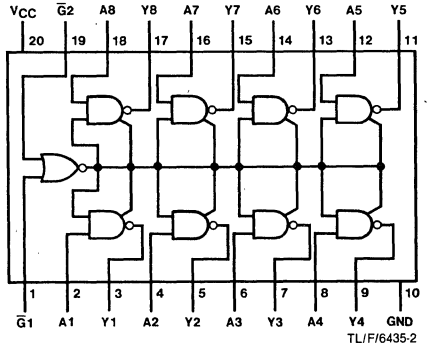
- Octal versions of popular DM54/74365, 366, 367, and 368 (DM70/8095, 96, 97 and 98)
- Typical power dissipation
  - DM54/74LS465, 467 80 mW
  - DM54/74LS466, 468 65 mW
- Typical propagation delay
  - DM54/74LS465, 467 15 ns
  - DM54/74LS466, 468 10 ns
- Low power-Schottky, TRI-STATE technology

Connection Diagrams

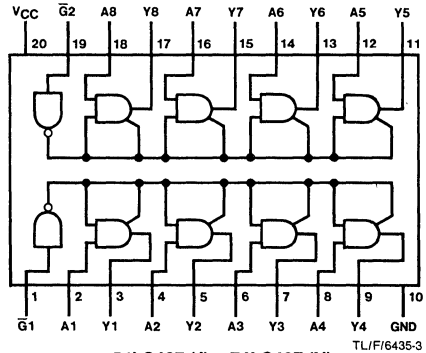
Dual-In-Line Packages



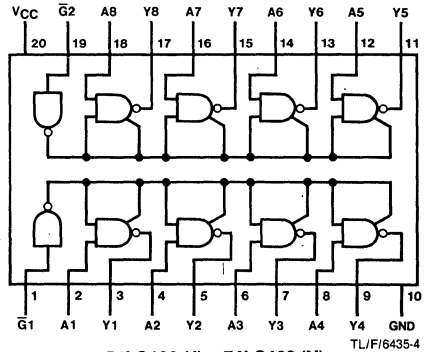
54LS465 (J) 74LS465 (N)



54LS466 (J) 74LS466 (N)



54LS467 (J) 74LS467 (N)



54LS468 (J) 74LS468 (N)

Function Tables

LS465

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

LS466

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

LS467

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

LS468

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Recommended Operating Conditions

Symbol	Parameter	DM54LS465, 466, 467, 468			DM74LS465, 466, 467, 468			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−2.6			−5.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS465 and 'LS467 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		DM54	2.5			V
				DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		DM54			0.4	V
				DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min		DM74			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.5V	A (Note 3)			−20	μA
			V_I = 0.4V	A (Note 4)			−50	
				$\overline{G}$			−50	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max					20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max					−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		DM54	−20		−100	mA
				DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				16	26.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Both $\overline{G}$ inputs are at 2V.

Note 4: Both $\overline{G}$ inputs at 0.4V.

'LS465 and 'LS467 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		10	16		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output		19	28		25	40	ns
t_{PZH} Output Enable Time to High Level Output		11	25		20	30	ns
t_{PZL} Output Enable Time to Low Level Output		20	30		28	42	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)		13	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)		19	27				ns

Note 1: $C_L = 5$ pF.

'LS466 and 'LS468 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		DM54	2.5			V
				DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		DM54			0.4	V
				DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min		DM74			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.5V	A (Note 3)			−20	μA
			V_I = 0.4V	A (Note 4)			−50	
				$\overline{G}$			−50	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max					20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max					−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		DM54	−20		−100	mA
				DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				13	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Both $\overline{G}$ inputs are at 2V.

Note 4: Both $\overline{G}$ inputs at 0.4V.

'LS466 and 'LS468 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	$C_L = 50$ pF			$C_L = 150$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		6	10		11	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output		13	17		19	30	ns
t_{PZH} Output Enable Time to High Level Output		10	15		20	30	ns
t_{PZL} Output Enable Time to Low Level Output		23	35		30	45	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)		13	20				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)		18	27				ns

Note 1: $C_L = 5$ pF.

National Semiconductor

DM54LS645/DM74LS645 Octal Bus Transceivers

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

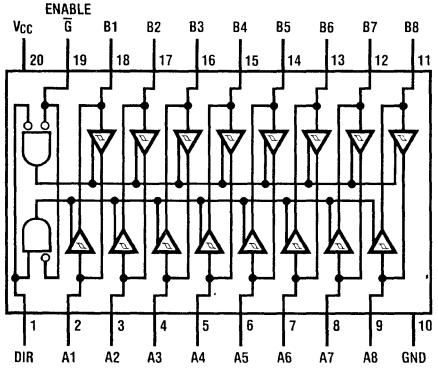
- Bi-directional bus transceivers in high-density 20-pin packages
- Hysteresis at bus inputs improves noise margins
- TRI-STATE® outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−55°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



DM54LS645 (J) DM74LS645 (N)

Function Table

Control Inputs		'LS645
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level
L = Low Level
X = Irrelevant

Recommended Operating Conditions

Symbol	Parameter	DM54LS645			DM74LS645			DM74LS645-1			Units
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage (Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
I_{OH}	High Level Output Current			−12			−15			−15	mA
I_{OL}	Low Level Output Current			12			24			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions (Note 2)		DM54LS645			DM74LS645			DM74LS645-1			Units
					Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage						0.5			0.6			0.6	V
V_{IK}	Input Clamp Voltage		V_{CC} = Min, I_I = 18 mA				−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{-}$) A or B Input		V_{CC} = Min		0.1	0.4		0.2	0.4		0.2	0.4		V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		2.4	3.4		V
				I_{OH} = Max	2			2			2			
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
				I_{OL} = 48 mA								0.4	0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = Max, G at 2V, V_O = 2.7V				20			20			20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_{CC} = Max, G at 2V, V_O = 0.4V				−400			−400			−400	μA
I_I	Input Current at Maximum Input Voltage	A or B	V_{CC} = Max	V_I = 5.5V			0.1			0.1			0.1	mA
		DIR or G		V_I = 7V			0.1			0.1			0.1	
I_{IH}	High Level Input Current		V_{CC} = Max, V_{IH} = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current		V_{CC} = Max, V_{IL} = 0.4V				−0.4			−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current (Note 4)		V_{CC} = Max		−40		−225	−40		−225	−40		−225	mA
I_{CC}	Total Supply Current	Outputs High	V_{CC} = Max, Outputs Open			48	70		48	70		48	70	mA
		Outputs Low				62	90		62	90		62	90	
		Outputs at Hi-Z				64	95		64	95		64	95	

Note 1: Voltage values are with respect to the network ground terminal.

Note 2: For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

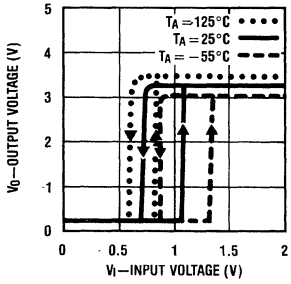
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

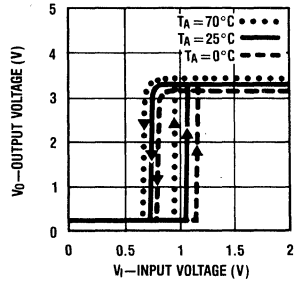
Parameter	From (Input) To (Output)	$R_L = 667\Omega$ (Note 2)						Units
		$C_L = 45$ pF			$C_L = 5$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to B		8	15				ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to B		11	15				ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to A		8	15				ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to A		11	15				ns
t_{PZL} Output Enable Time to Low Level	$\overline{G}$, DIR to A		31	40				ns
t_{PZH} Output Enable Time to High Level	$\overline{G}$, DIR to A		26	40				ns
t_{PZL} Output Enable Time to Low Level	$\overline{G}$, DIR to B		31	40				ns
t_{PZH} Output Enable Time to High Level	$\overline{G}$, DIR to B		26	40				ns
t_{PLZ} Output Disable Time to Low Level	$\overline{G}$, DIR to A					15	25	ns
t_{PHZ} Output Disable Time to High Level	$\overline{G}$, DIR to A					15	25	ns
t_{PLZ} Output Disable Time to Low Level	$\overline{G}$, DIR to B					15	25	ns
t_{PHZ} Output Disable Time to High Level	$\overline{G}$, DIR to B					15	25	ns

Typical Characteristics

DM54LS Noninverting Output Voltage vs Input Voltage



DM74LS Noninverting Output Voltage vs Input Voltage



National Semiconductor

DM54LS670/DM74LS670 TRI-STATE®4-by-4 Register Files

General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, TRI-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- TRI-STATE versions of DM54LS170/DM74LS170
- Fast access times 20 ns typ

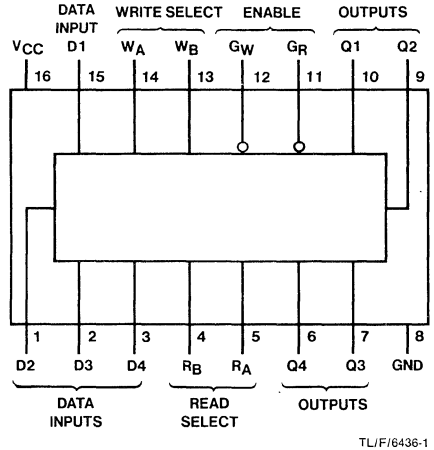
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6436-1

54LS670 (J, N) **74LS670 (J, N)**

Function Tables

WRITE TABLE (SEE NOTES A, B, AND C)

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (SEE NOTES A AND D)

Read Inputs			Outputs			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

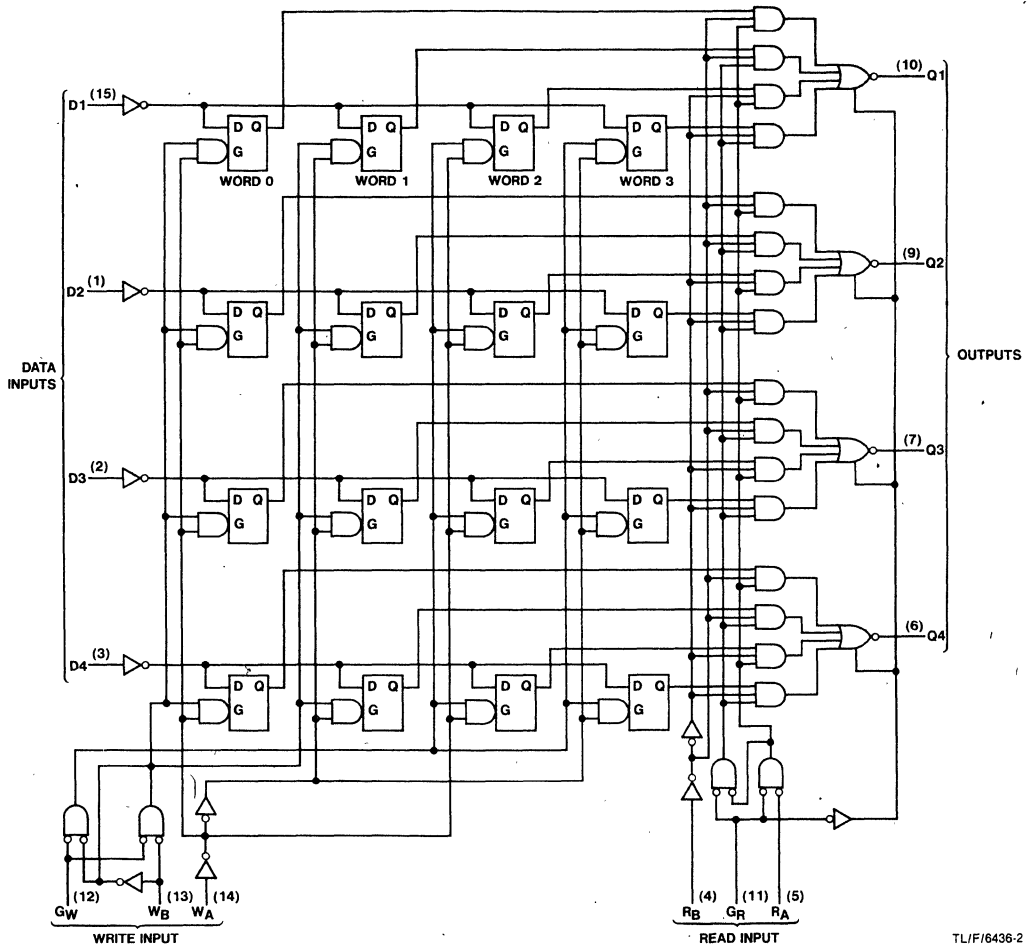
Note A: H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (Off)

Note B: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Note C: Q_0 = The level of Q before the indicated input conditions were established.

Note D: W0B1 = The first bit of word 0, etc.

Logic Diagram



Recommended Operating Conditions

Symbol	Parameter		DM54LS670			DM74LS670			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Write Enable Pulse Width		25			25			ns
t_{SU}	Setup Time (Note 1)	Data	10			10			ns
		W_A, W_B	15			15			
t_H	Hold Time (Note 1)	Data	15			15			ns
		W_A, W_B	5			5			
t_{LATCH}	Latch Time for New Data (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address, t_{SETUP} (W_A, W_B) can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during t_H (W_A, W_B) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.34	0.5	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V	D, R or W			0.1	mA
			G_W			0.2	
			G_R			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D, R or W			20	μA
			G_W			40	
			G_R			60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D, R or W			−0.4	mA
			G_W			−0.8	
			G_R			−1.2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 667Ω						Units
		C_L = 45 pF			C_L = 150 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Read Select to Q		23	40		28	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Read Select to Q		25	45		31	55	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Write Enable to Q		26	45		31	55	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Write Enable to Q		28	50		34	60	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Q		25	45		30	55	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Q		23	40		29	50	ns
t_{PZH} Output Enable Time to High Level Output	Read Enable to Any Q		15	35		25	45	ns
t_{PZL} Output Enable Time to Low Level Output	Read Enable to Any Q		22	40		30	50	ns
t_{PHZ} Output Disable Time from High Level Output (Note 4)	Read Enable to Any Q		30	50				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 4)	Read Enable to Any Q		16	35				ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all DATA inputs and both ENABLE inputs, all ADDRESS inputs are grounded and all outputs are open.

Note 4; C_L = 5 pF.

National Semiconductor

DM54LS952/DM74LS952 Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", synchronously clear. Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Absolute Maximum Ratings (Note 1)

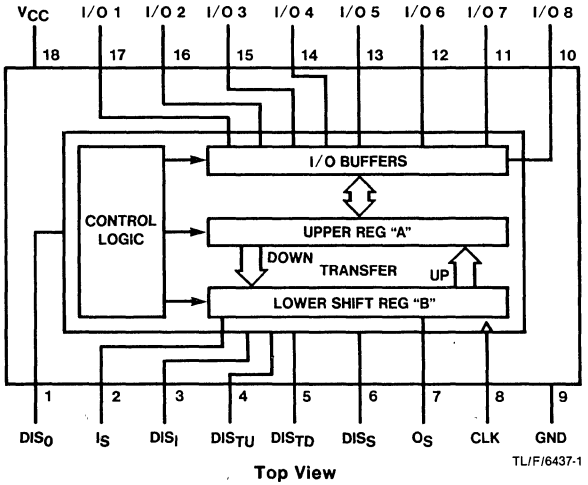
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



TL/F/6437-1

Top View

54LS952 (J) **74LS952 (N)**

Pin Description

DIS_O—Output disable
I_S—Serial input
DIS_I—Input disable
DIS_{TU}—Transfer up disable
DIS_{TD}—Transfer down disable
DIS_S—Shift disable
O_S—Serial output
CLK—Clock
GND—Ground
I/O 1...I/O 8—8-bit I/O pins
V_{CC}—Supply Voltage

Recommended Operating Conditions

Symbol	Parameter	DM54LS952			DM74LS952			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			2			V
V_{IL}	Low-Level Input Voltage			0.7			0.8	V
I_{OH}	High-Level Output Current			−2.6			−5.2	mA
I_{OL}	Low-Level Output Current			8			16	mA
f_{CLOCK}	Clock Frequency	0		25	0		25	MHz
Clock Pulse	High Pulse Width	25	17		25	17		ns
	Low Pulse Width	15	7		15	7		ns
t_{SET-UP}	Data Set-Up Time	10						ns
t_{HOLD}	Data Hold Time	0						ns
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		DM54LS952			DM74LS952			Units
				Min	Typ (2)	Max	Min	Typ (2)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V,	I_{OH} = −2.6 mA	2.4						V
		V_{IL} = V_{IL} max	I_{OH} = −5.2 mA				2.4			
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL} max	I_{OL} = 16 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7 V				20			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4 V				−50			−50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99		61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2 V	V_O = 2.4 V			20			20	μA
			V_O = 0.4 V			−20			−20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5 V, T_A = 25°C.

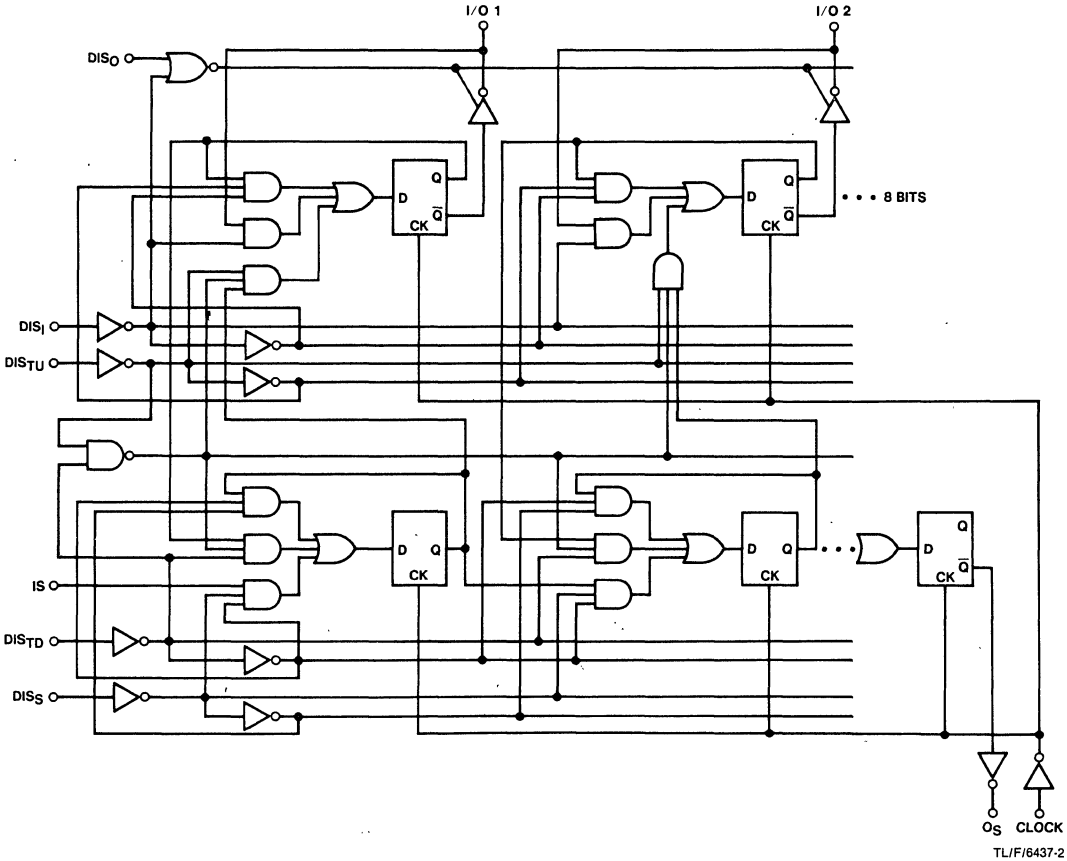
Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4 V. All other control inputs and I/O pins grounded.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	25	36		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Output		7	22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Output		10	32	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	16	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	18	27	ns
t_{ZH}	Output Enable Time to High Level		5	15	23	ns
t_{ZL}	Output Enable to Low Level		4	12	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 1 kΩ	5	15	23	ns
t_{LZ}	Output Disable Time from Low Level		6	18	27	ns

Logic Diagram



Function Table

Table I

DIS_O	DIS_I	DIS_{TU}	DIS_{TD}	DIS_S	CLK	I_S	8-BIT I/O PINS	CONTENT OF UPPER REG. "A"								CONTENT OF LOWER SERIAL SHIFT REG. "B"								O_S	COMMENTS
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	← DOR →								b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O and reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(1) Synchronously clear both registers to
L	H	L	L	X	↑	X	Output	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(2) logic "L" level
X	L	L	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	L	L	L	L	L	L	L	L	L	(3) Enter data to reg. "A" clear reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	← DOR →								d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

a1...a8/b1...b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

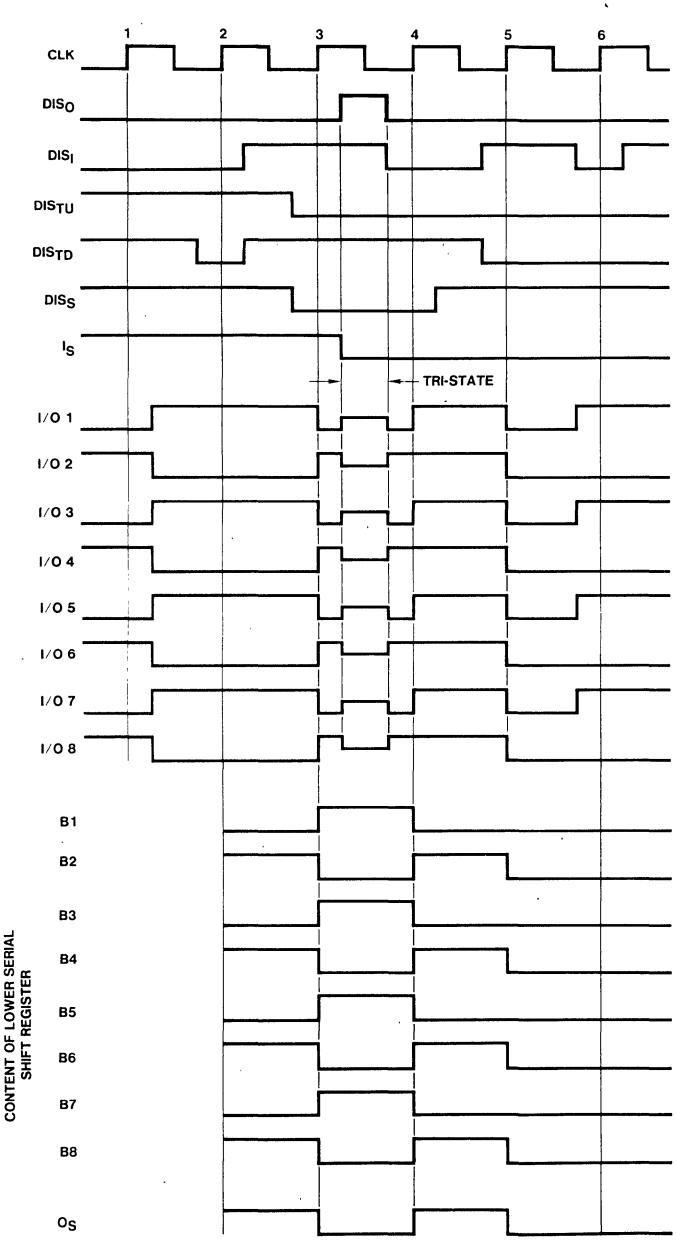
$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

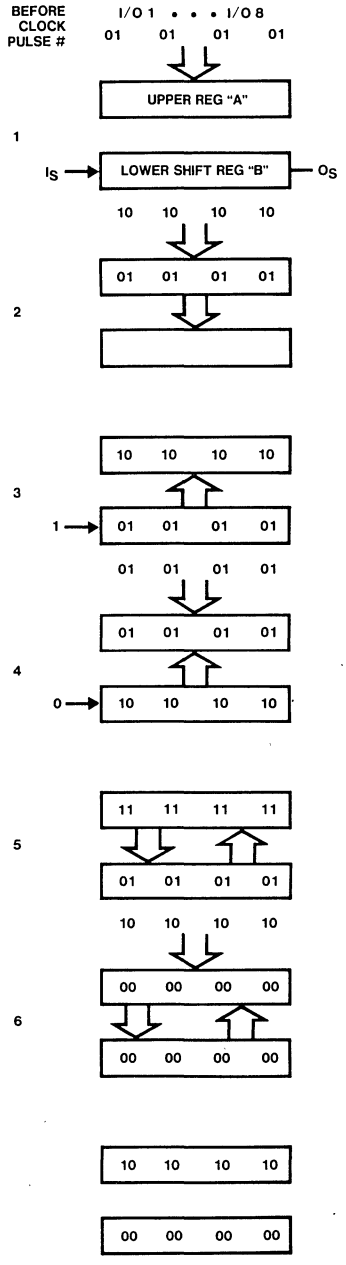
DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., $I_1 + b1$, $I_2 + b2$, $I_3 + b3 \ldots I_8 + b8$

d ≡ Data of the serial input

Timing Diagram

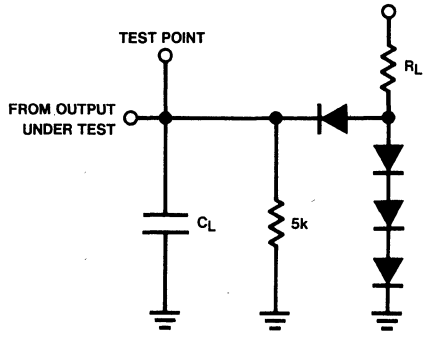
DM54/74LS952





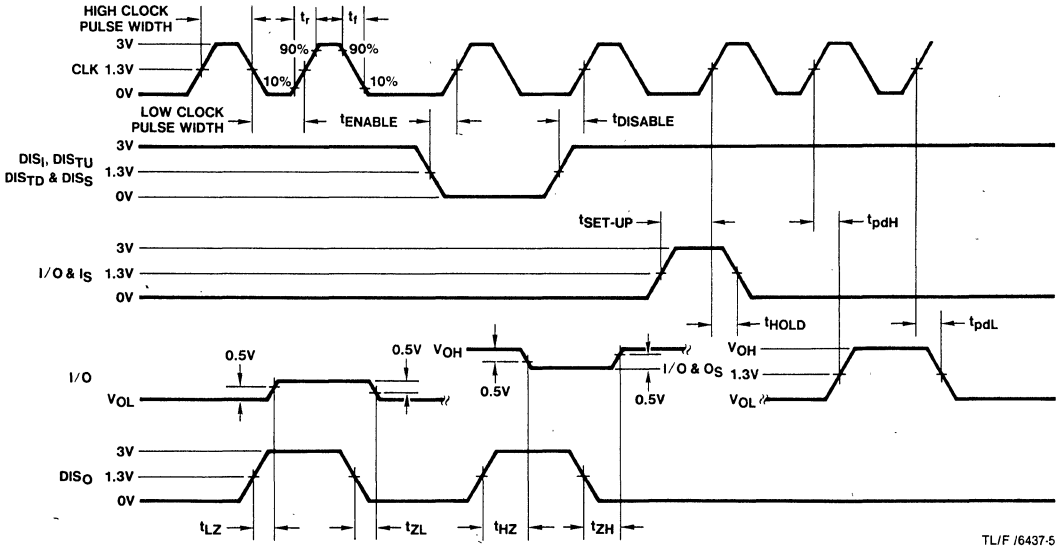
TL/F/6437-3

AC Test Circuit and Switching Time Waveforms



All diodes are 1N916 or 1N3064.
C_L includes probe and jig capacitance.

TL/F/6437-4

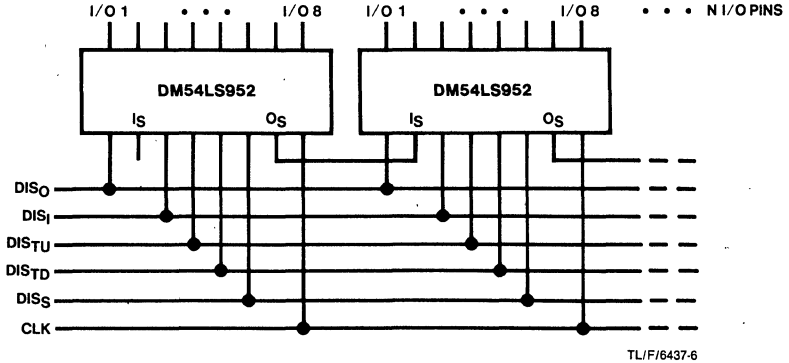


TL/F /6437-5

All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{OUT} \approx 50\ \Omega$.

Cascading Packages

Cascading Packages for N-Bit Word



TL/F/6437-6

National Semiconductor

DM54LS962/DM74LS962 Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", or exchange data between register "A" and shift register "B". Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Absolute Maximum Ratings (Note 1)

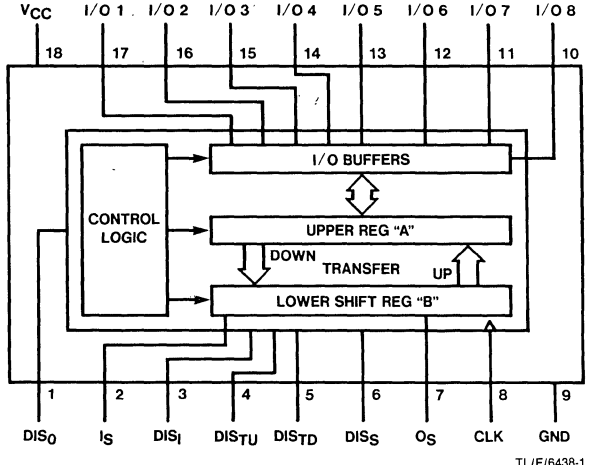
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

4

Connection Diagram

Dual-In-Line Package



Top View

TL/F/6438-1

54LS962 (J) **74LS962 (N)**

Pin Description

DIS_O—Output disable
I_S—Serial input
DIS_I—Input disable
DIS_{TU}—Transfer up disable
DIS_{TD}—Transfer down disable
DIS_S—Shift disable
O_S—Serial output
CLK—Clock
GND—Ground
I/O 1...I/O 8—8-bit I/O pins
V_{CC}—Supply Voltage

Recommended Operating Conditions

Symbol	Parameter	DM54LS962			DM74LS962			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			2			V
V_{IL}	Low-Level Input Voltage			0.8			0.8	V
I_{OH}	High-Level Output Current			−2.6			−5.2	mA
I_{OL}	Low-Level Output Current			8			16	mA
f_{CLOCK}	Clock Frequency	0		25	0		25	MHz
Clock Pulse	High Pulse Width	25	17		25	17		ns
	Low Pulse Width	15	7		15	7		ns
t_{SET-UP}	Data Set-Up Time	10						ns
t_{HOLD}	Data Hold Time	0						ns
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		DM54LS962			DM74LS962			Units
				Min	Typ (2)	Max	Min	Typ (2)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V,	I_{OH} = −2.6 mA	2.4						V
		V_{IL} = V_{IL} max	I_{OH} = −5.2 mA				2.4			
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL} max	I_{OL} = 16 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7 V				20			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4 V				−50			−50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99		61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2 V	V_O = 2.4 V			20			20	μA
			V_O = 0.4 V			−20			−20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5 V, T_A = 25°C.

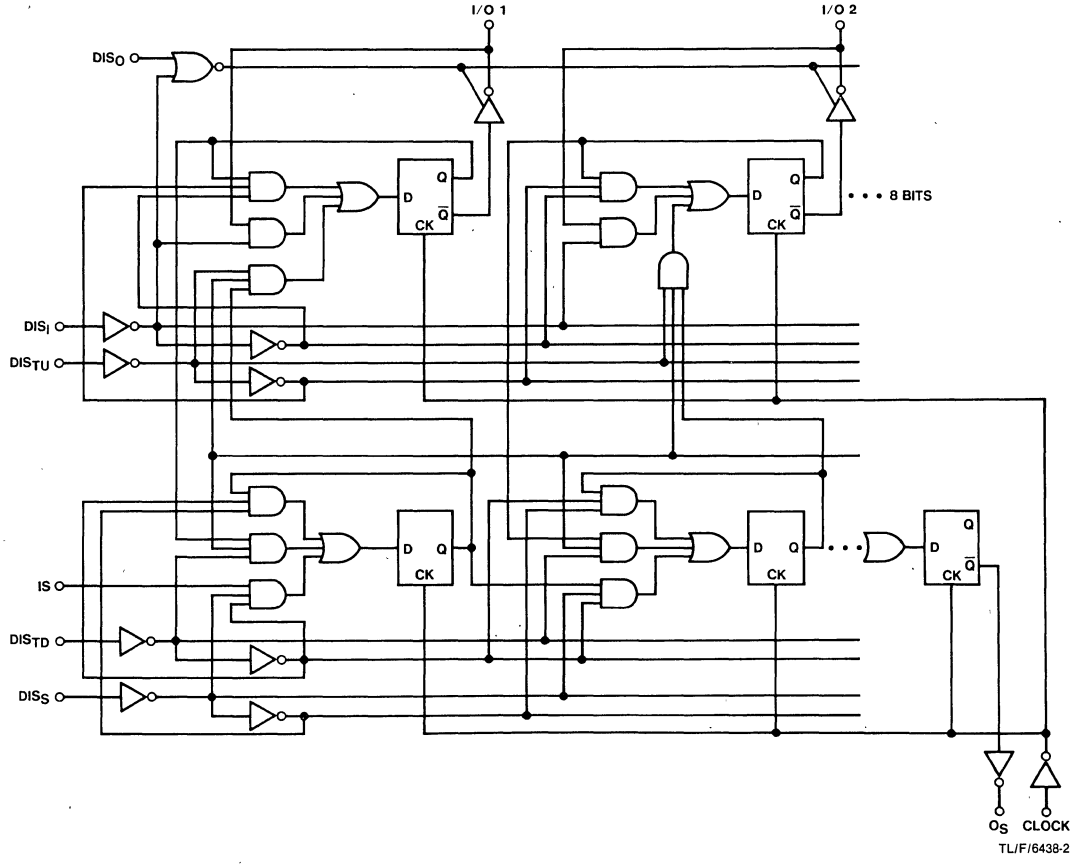
Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4 V. All other control inputs and I/O pins grounded.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	25	36		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	22	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Outputs		10	32	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	16	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	18	27	ns
t_{ZH}	Output Enable Time to High Level		5	15	23	ns
t_{ZL}	Output Enable to Low Level		4	12	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 1 kΩ	5	15	23	ns
t_{LZ}	Output Disable Time from Low Level		6	18	27	ns

Logic Diagram



TL/F/6438-2

Function Table

Table I

DIS_O	DIS_I	DIS_{TU}	DIS_{TD}	DIS_S	CLK	I_S	8-BIT I/O PINS	CONTENT OF UPPER REG. "A"								CONTENT OF LOWER SERIAL SHIFT REG. "B"								O_S	COMMENTS
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	← DOR →								b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O and reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(1) Exchange data between registers
L	H	L	L	X	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(2) Beside data exchanging, reg. "A"
X	L	L	L	X	↑	X	Input	← DOR →								a1	a2	a3	a4	a5	a6	a7	a8	a8	(3) will "OR" data from I/O and reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	← DOR →								d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

a1...a8/b1...b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

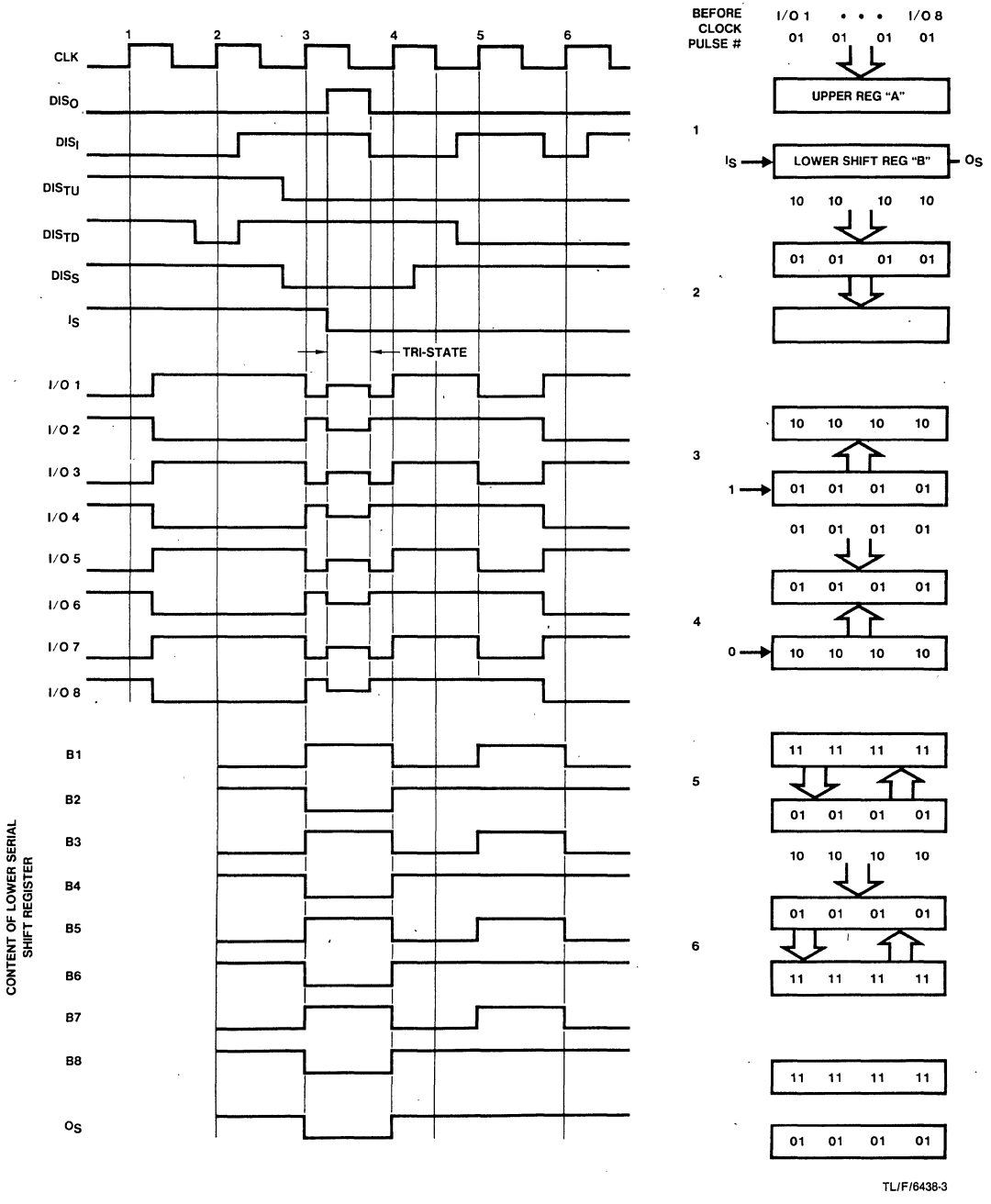
$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., I_1 + b1, I_2 + b2, I_3 + b3 ... I_8 + b8

d ≡ Data of the serial input

Timing Diagram

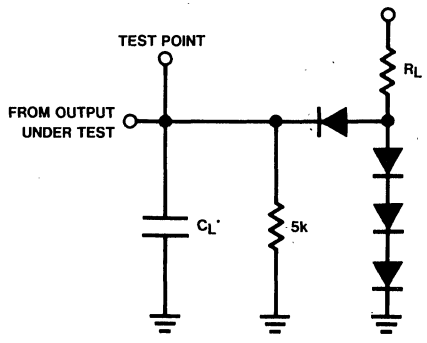
DM54/74LS962



TL/F/6438-3

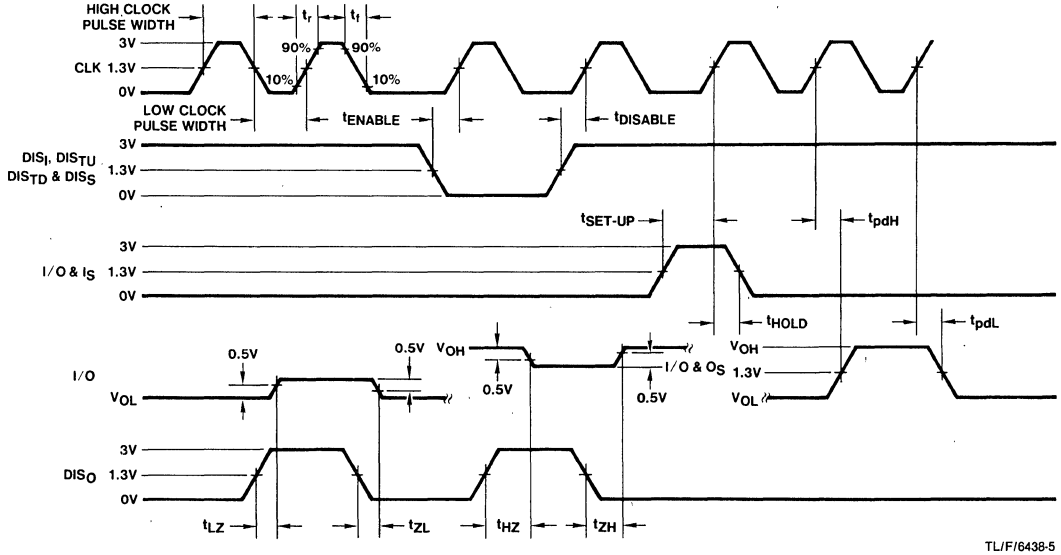
4

AC Test Circuit and Switching Time Waveforms



All diodes are 1N916 or 1N3064.
C_L includes probe and jig capacitance.

TL/F/6438-4

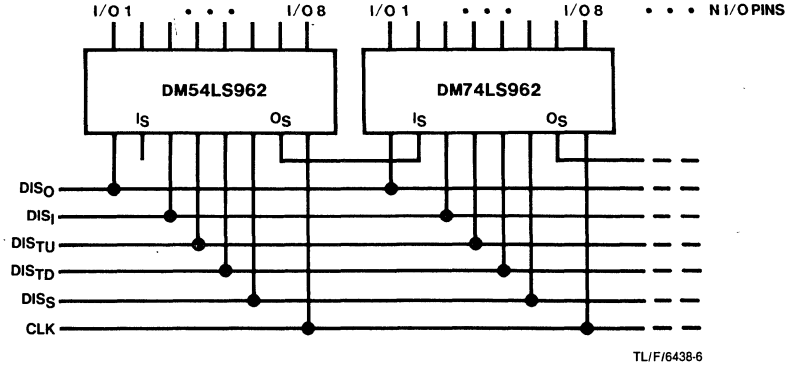


TL/F/6438-5

All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{OUT} \approx 50\ \Omega$.

Cascading Packages

Cascading Packages for N-Bit Word



TL/F/6438-6

Section 5

Schottky

5

Section Contents

Section Contents (Continued)

National Semiconductor

DM54S00/DM74S00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

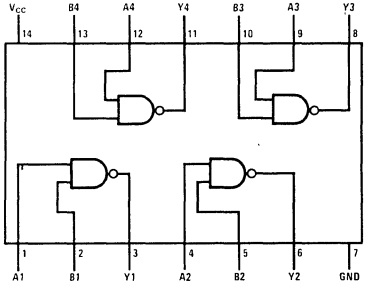
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6489-1

DM54S00 (J) DM74S00 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S00			DM74S00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			10	16	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			20	36	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	3	4.5	2	4.5	7	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	3	5	2	5	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S02/DM74S02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

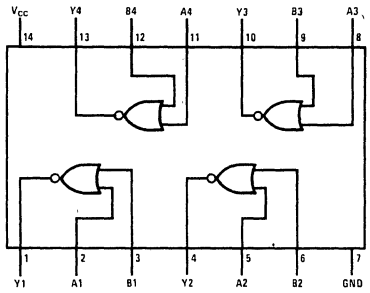
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6490-1

DM54S02 (J) DM74S02 (N)

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S02			DM74S02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			17	29	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			26	45	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	1.5	3.5	5.5	2	5	7.5	ns
t_{PHL} Propagation Delay Time High to Low Level Output	1.5	3.5	5.5	2	5	7.5	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S03/DM74S03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

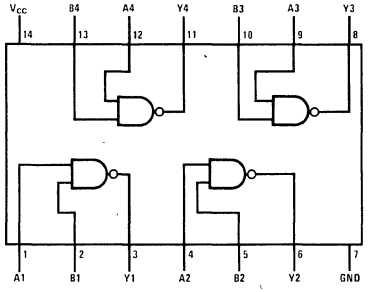
Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

5

Connection Diagram

Dual-In-Line Package



TL/F/6491-1

DM54S03 (J) DM74S03 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S03			DM74S03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		6.0	13.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		20	36	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	5	7.5	3	7.5	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4.5	7	3	7	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54S04/DM74S04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

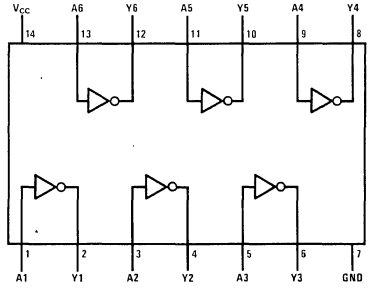
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6442-1

DM54S04 (J) DM74S04 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S04			DM74S04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			15	24	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			30	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	3	4.5	2	4.5	7	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	3	5	2	5	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S05/DM74S05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

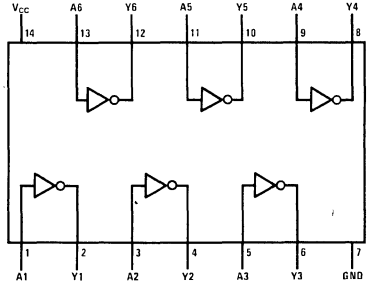
Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

5

Connection Diagram

Dual-In-Line Package



TL/F/6443-1

DM54S05 (J) DM74S05 (N)

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S05			DM74S05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		9.0	19.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		30	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output ut	2	5	7.5	3	7.5	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output ut	2	4.5	7	3	7	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54S08/DM74S08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

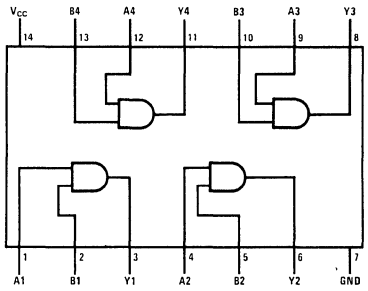
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6444-1

DM54S08 (J) DM74S08 (N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S08			DM74S08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			18	32	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			32	57	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2.5	4.5	7	3	6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2.5	5	7.5	3	7.5	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S09/DM74S09 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require an external pull-up resistor for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

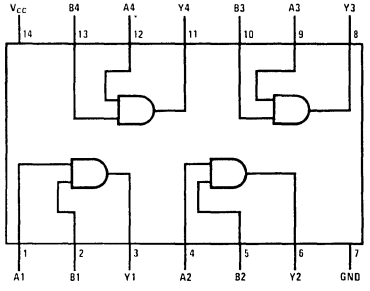
Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

5

Connection Diagram

Dual-In-Line Package



TL/F/6465-1

DM54S09 (J) DM74S09 (N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S09			DM74S09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		18	32	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		32	57	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	3	6.5	10	4	9	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	3	6.5	10	4	9	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54S10/DM74S10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

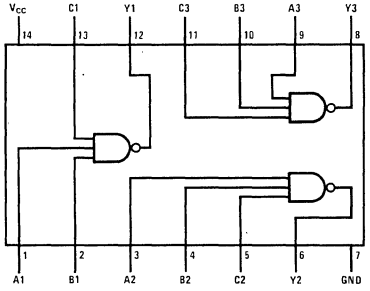
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6446-1

DM54S10 (J) DM74S10 (N)

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S10			DM74S10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			7.5	12	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			15	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	3	4.5	2	4.5	7	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	3	5	2	5	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S11/DM74S11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

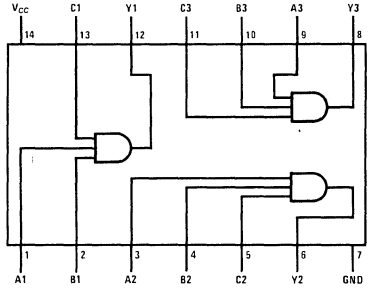
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6447-1

DM54S11 (J) DM74S11 (N)

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S11			DM74S11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			13.5	24	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			24	42	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2.5	4.5	7	3	6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2.5	5.0	7.5	3	7.5	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S15/DM74S15 Triple 3-Input AND Gates with Open-Collector Outputs

General Description

This device contains three independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

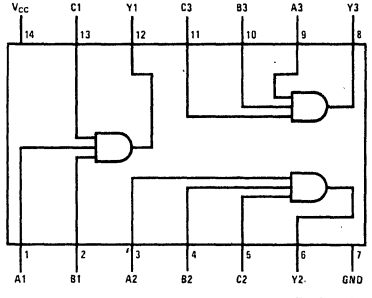
Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

5

Connection Diagram

Dual-In-Line Package



TL/F/6448-1

DM54S15 (J) DM74S15 (N)

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S15			DM74S15			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		11	19.5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		24	42	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	5.5	8.5	3	8.5	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	6	9	3	8	12	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54S20/DM74S20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

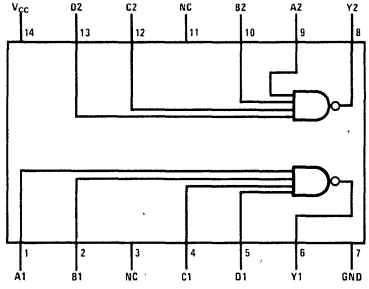
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6449-1

DM54S20 (J) DM74S20 (N)

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S20			DM74S20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			5	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			10	18	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	3	4.5	2	4.5	7	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	3	5	2	5	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S22/DM74S22 Dual 4-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

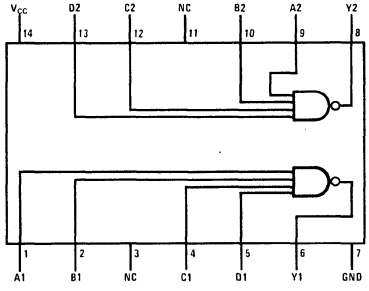
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6450-1

DM54S22 (J) DM74S22 (N)

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S22			DM74S22			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		3	6.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		10	18	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	5	7.5	3	7.5	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4.5	7	3	7	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54S30/DM74S30 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

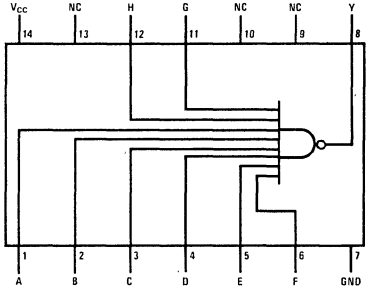
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6451-1

DM54S30 (J) DM74S30 (N)

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	**Y**
All inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S30			DM74S30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			3	5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			5.5	10	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	4	6	2	5.5	8	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4.5	7	3	6.5	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S32/DM74S32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

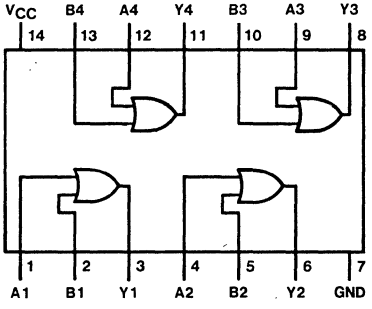
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6452-1

DM54S32 (J) DM74S32 (N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S32			DM74S32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			18	32	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			38	68	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	4	7	2	5	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4	7	2	5	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S40/DM74S40 Dual 4-Input NAND Buffers

General Description

This device contains two independent gates each of which performs the logic NAND function.

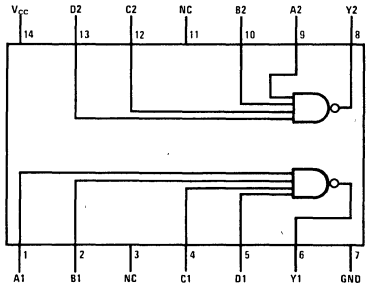
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6453-1

DM54S40 (J) DM74S40 (N)

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S40			DM74S40			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−3			−3	mA
I_{OL}	Low Level Output Current			60			60	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			10	18	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			25	44	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 93Ω						Units
	C_L = 50 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	4	6.5	3	6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4	6.5	3	6	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S51/DM74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

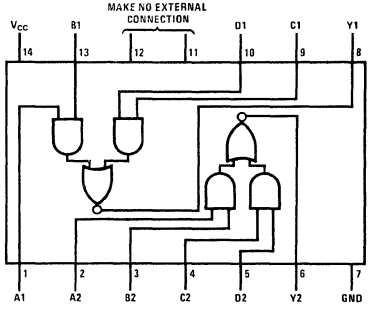
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6454-1

DM54S51 (J) DM74S51 (N)

Function Table

$$Y = \overline{AB + CD}$$

Inputs				Output
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S51			DM74S51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			8.2	17.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			14	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	3.5	5.5	3	5	8	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	3.5	5.5	3	5.5	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S64/DM74S64 4-Wide AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

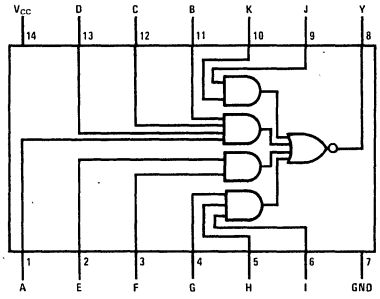
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6455-1

DM54S64 (J) DM74S64 (N)

Function Table

$$Y = \overline{ABCD + EF + GHI + JK}$$

Inputs											Output
A	B	C	D	E	F	G	H	I	J	K	Y
H	H	H	H	X	X	X	X	X	X	X	L
X	X	X	X	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S64			DM74S64			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			7	12.5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			8.5	16	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	3.5	5.5	3	5	8	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	3.5	5.5	3	5.5	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S65/DM74S65 4-Wide AND-OR-INVERT Gates with Open-Collector Outputs

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function. The open-collector output requires an external pull-up resistor for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Absolute Maximum Ratings (Note 1)

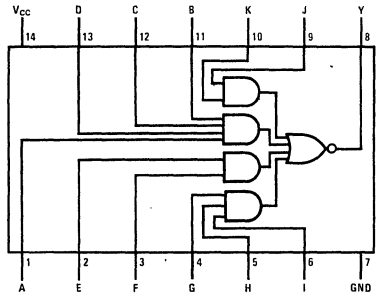
Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

5

Connection Diagram

Dual-In-Line Package



TL/F/6456-1

DM54S65 (J) DM74S65 (N)

Function Table

$$Y = \overline{ABCD + EF + GHI + JK}$$

Inputs											Output
A	B	C	D	E	F	G	H	I	J	K	Y
H	H	H	H	X	X	X	X	X	X	X	L
X	X	X	X	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S65			DM74S65			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		6	11	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		8.5	16	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	5	7.5	3	8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	5.5	8.5	3	6.5	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54S74/DM74S74 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

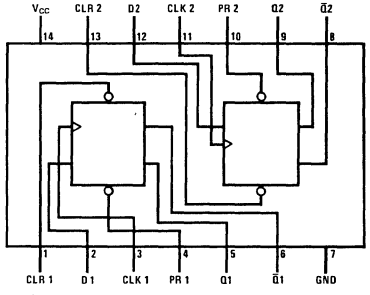
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6457-1

DM54S74 (J) DM74S74 (N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

5

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S74			DM74S74			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	95	65	0	95	65	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
		Clear Low	7			7			
		Preset Low	7			7			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	9			9			
		Clear Low	9			9			
		Preset Low	9			9			
t_{SU}	Setup Time (Notes 1 and 2)		3↑			3↑			ns
t_{SU}	Setup Time (Notes 1 and 3)		3↑			3↑			ns
t_H	Input Hold Time (Notes 1 and 2)		2↑			2↑			ns
t_H	Input Hold Time (Notes 1 and 3)		2↑			2↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge at the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			50	μA
			Clear			150	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 4)	D			−2	μA
			Clear			−6	
			Preset			−4	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		75	110		65	95		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		4	6		6	9	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		4	6		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Clock High)	Preset to $\overline{Q}$		9	13.5		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Clock Low)	Preset to $\overline{Q}$		5	8		8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Clock High)	Clear to Q		9	13.5		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Clock Low)	Clear to Q		5	8		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		6	9		8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		6	9		9	13	ns

National Semiconductor

DM54S86/DM74S86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic Exclusive-OR function.

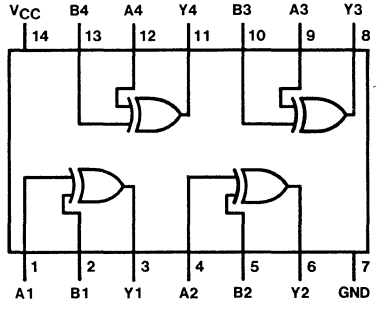
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6458-1

DM54S86 (J) DM74S86 (N)

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S86			DM74S86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			35	50	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) to (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y		7	10.5		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output			6.5	10		9	13	ns

National Semiconductor

DM54S112/DM74S112 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

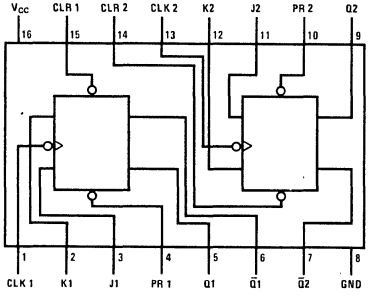
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6459-1

DM54S112 (J) DM74S112 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_O = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S112			DM74S112			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Clear Low	8			8			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	CLock High	8			8			ns
		Clock Low	8			8			
		Clear Low	10			10			
		Preset Low	10			10			
t_{SU}	Setup Time (Note 1)		3↓			3↓			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			50	μA
			Clear			100	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	J, K			−1.6	mA
			Clear			−7	
			Preset			−7	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		80	125		60	80		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		4	7		6	9	ns
t_{PHL} Proagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		5	7		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		5	7		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		5	7		8	12	ns

National Semiconductor

DM54S113/DM74S113 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset input will set or reset the outputs regardless of the logic levels of the other inputs.

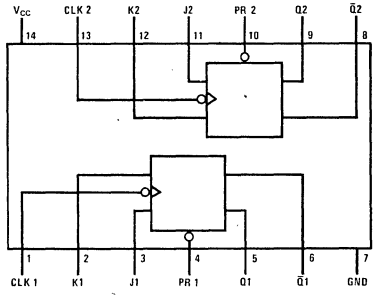
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6460-1

DM54S113 (J) DM74S113 (N)

Function Table

Inputs				Outputs	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_O	$\overline{Q}_O$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S113			DM74S113			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Preset Low	10			10			
t_{SU}	Setup Time (Note 1)		3↓			3↓			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.

Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			50	μA
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	J, K			−1.6	μA
			Preset			−7	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		80	125		60	80		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		5	7		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		5	7		8	12	ns

National Semiconductor

DM54S114/DM74S114 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Common Clear, Common Clock and Complementary Outputs

General Description

This device contains two negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

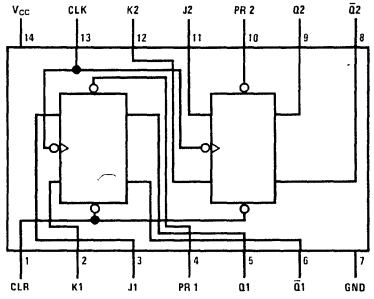
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6461-1

DM54S114 (J) DM74S114 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_O = The output logic level before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to its inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

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Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S114			DM74S114			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Clear Low	8			8			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Clear Low	10			10			
		Preset Low	10			10			
t_{SU}	Setup Time (Note 1)		3↓			3↓			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Parameter		Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			50	μA
			Clear			200	
			Preset			100	
			Clock			200	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	J, K			−1.6	μA
			Clear			−14	
			Preset			−7	
			Clock			−8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		80	125		60	80		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		5	7		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		5	7		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		4	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		5	7		8	12	ns

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National Semiconductor

DM54S133/DM74S133 13-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

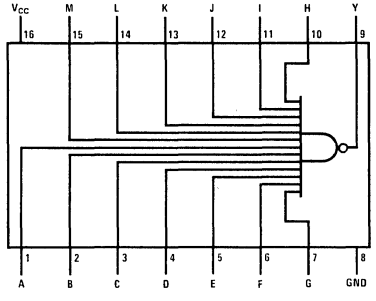
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6462–1

DM54S133 (J) DM74S133 (N)

Function Table

$$Y = \overline{ABCDEFGHIJKLM}$$

Inputs	Output
A thru M	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S133			DM74S133			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			3	5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			5.5	10	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 280Ω						Units
	C_L = 15 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	4	6	2	5.5	8	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4.5	7	3	6.5	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S134/DM74S134 TRI-STATE® 12-Input NAND Gate

General Description

This device contains a gate which performs the logic NAND function. The output has the TRI-STATE feature. When enabled, the output exhibits the low impedance of a standard S output with additional drive at the high logic level to permit the driving of the bus lines without external pull-up resistors. When disabled, both the output transistors are turned off, presenting a high impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver.

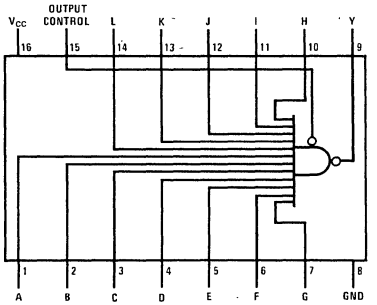
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6463-1

DM54S134 (J) **DM74S134 (N)**

Function Table

$Y = ABCDEFGHIJKL$

Output Control	Inputs A	B	C	D	E	F	G	H	I	J	K	L	Outputs Y
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	Any One or More Inputs Low												H
H	X	X	X	X	X	X	X	X	X	X	X	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = High Impedance (off) State

Recommended Operating Conditions

Sym	Parameter	DM54S134			DM74S134			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−6.5			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4 V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5 V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			7	13	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			9	16	mA
I_{CCZ}	Supply Current With Outputs Disabled	V_{CC} = Max			14	25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 280\Omega$						Units
	$C_L = 15$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		4	6		5.5	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output		5	7.5		7	11	ns
t_{PZH} Output Enable Time to High Level Output					13	19.5	ns
t_{PZL} Output Enable Time to Low Level Output					14	21	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)					5.5	8.5	ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)					9	14	ns

Note 1: $C_L = 5$ pF.

National Semiconductor

DM54S135/DM74S135 Quad Exclusive-OR/NOR Gates

General Description

This device contains two combinations of gates which performs the logic Exclusive-OR/NOR function.

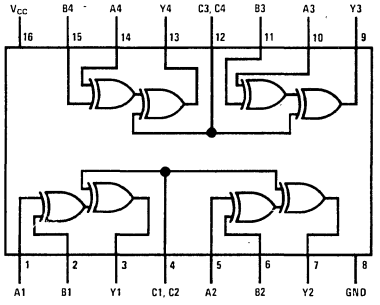
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6464-1

DM54S135 (J) **DM74S135 (N)**

Function Table

$Y = (A \oplus B) \oplus C = A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$

Inputs			Output
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = High Logic Level
L = Low Logic Level

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Recommended Operating Conditions

Sym	Parameter	DM54S135			DM74S135			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			65	99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the inputs grounded and the outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y (A or B = H, C = H)		8.5	13		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y (A or B = H, C = H)		11	15		14	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y (A or B = L, C = H)		8.0	12		11	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y (A or B = L, C = H)		9.0	13.5		12	16.5	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y (A or B = H, C = L)		10	15		13	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y (A or B = H, C = L)		6.5	10		9.5	13	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y (A or B = L, C = L)		8.5	12		12	15	ns
t_{PLH} Propagation Delay Time High to Low Level Output	A or B to Y (A or B = L, C = L)		7.0	11		10	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C to Y (A ≠ B)		8.0	12		11	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C to Y (A ≠ B)		9.5	14.5		13	17.5	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C to Y (A = B)		7.5	11.5		11	14.5	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C to Y (A = B)		8.0	12		11	15	ns

5

National Semiconductor

DM54S136/DM74S136 Quad 2-Input EXCLUSIVE-OR Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic EXCLUSIVE-OR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor.

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

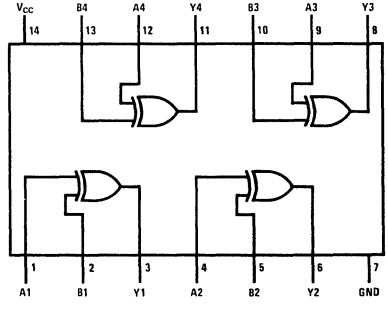
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6465-1

DM54S136 (J) DM74S136 (N)

Function Table

$$Y = A \oplus B = A\bar{B} + \bar{A}B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54S136			DM74S136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Parameter	From (Input) to (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y		8	12.5		10	14.5	ns
t_{PHL} Propagation Delay Time High to Low Level Output			7.5	12		9.5	14	ns

National Semiconductor

DM54S138/DM74S138, DM54S139/DM74S139 Decoders/Demultipexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The S138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The S139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- S138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- S139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay time (3 levels of logic)
  - S138 8 ns
  - S139 7.5 ns
- Typical power dissipation
  - S138 245 mW
  - S139 300 mW

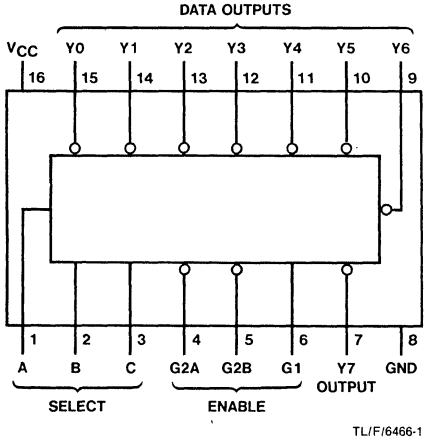
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

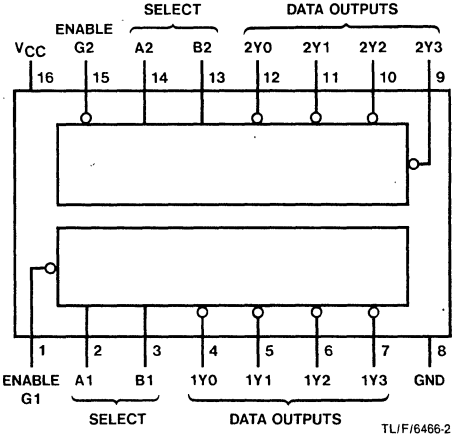
Dual-In-Line Package



TL/F/6466-1

54S138 (J) 74S138 (N)

Dual-In-Line Package



TL/F/6466-2

54S139 (J) 74S139 (N)

Recommended Operating Conditions

Sym	Parameter	DM54S138, S139			DM74S138, S139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min; I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current (S138)	V_{CC} = Max (Note 3)			49	74	mA
I_{CC}	Supply Current (S139)	V_{CC} = Max (Note 3)			60	90	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'S138 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Levels of Delay	$R_L = 280\Omega$						Units
			$C_L = 15$ pF			$C_L = 50$ pF			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	2		4.5	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	2		7	10.5		9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	3		7.5	12		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	3		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output	2		5	8		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output	2		7	11		9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output	3		7	11		8.5	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output	3		7	11		9	14	ns

'S139 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Levels of Delay	$R_L = 280\Omega$						Units
			$C_L = 15$ pF			$C_L = 50$ pF			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	2		5	7.5		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	2		6.5	10		8.5	13	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	3		7	12		8.5	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	3		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output	2		5	8		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output	2		6.5	10		8.5	13	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

Function Tables

S138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = don't care (either low or high logic level)

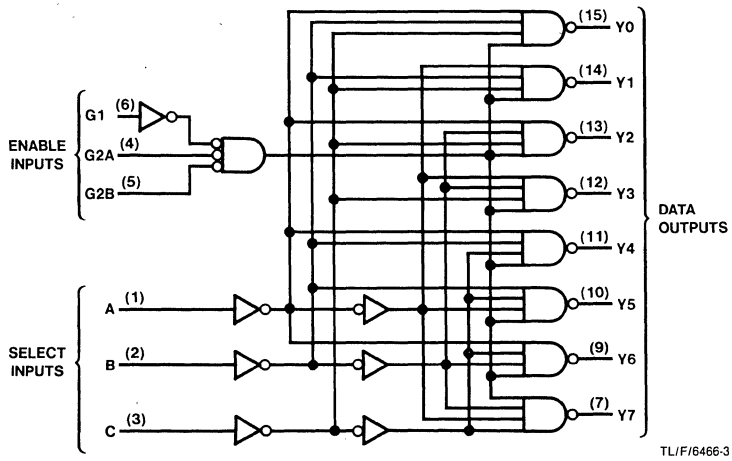
S139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care (either low or high logic level)

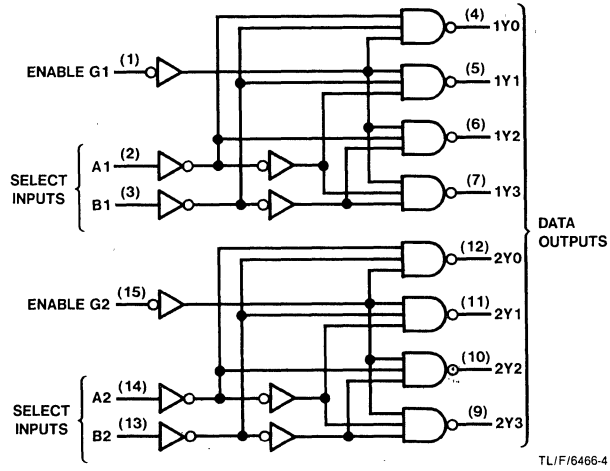
Logic Diagrams

S138



TL/F/6466-3

S139



TL/F/6466-4

National Semiconductor

DM54S140/DM74S140
Dual 4-Input NAND 50Ω Line Driver

General Description

This device contains two independent line driver gates each of which performs the logic NAND function.

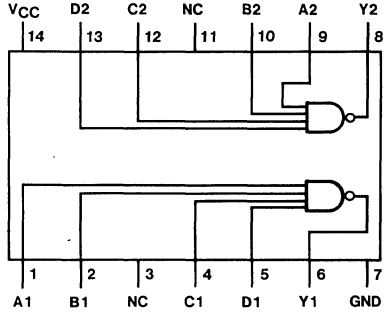
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6467-1

DM54S140 (J) DM74S140 (N)

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Sym	Parameter	DM54S140			DM74S140			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−40			−40	mA
I_{OL}	Low Level Output Current			60			60	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
		V_{IL} = 0.5V, R_O = 50Ω to GND		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			10	18	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			25	44	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 93Ω						Units
	C_L = 50 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	2	4	6.5	3	6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	2	4	6.5	3	6	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S151/DM74S151 1 of 8 Data Selector/Multiplexer with Complementary Outputs

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The S151 selects one-of-eight data sources. The S151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output low.

The S151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output 4.5 ns
- Typical power dissipation 225 mW

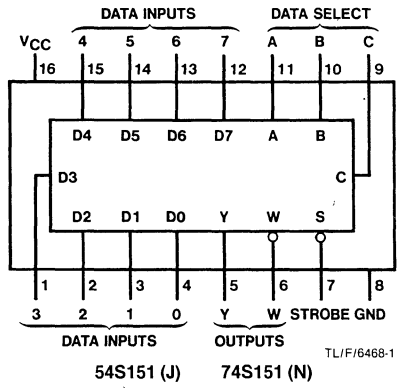
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54S151 (J) 74S151 (N)

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = don't care

D0, D1...D7 = the level of the respective D input

Recommended Operating Conditions

Sym	Parameter	DM54S151			DM74S151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

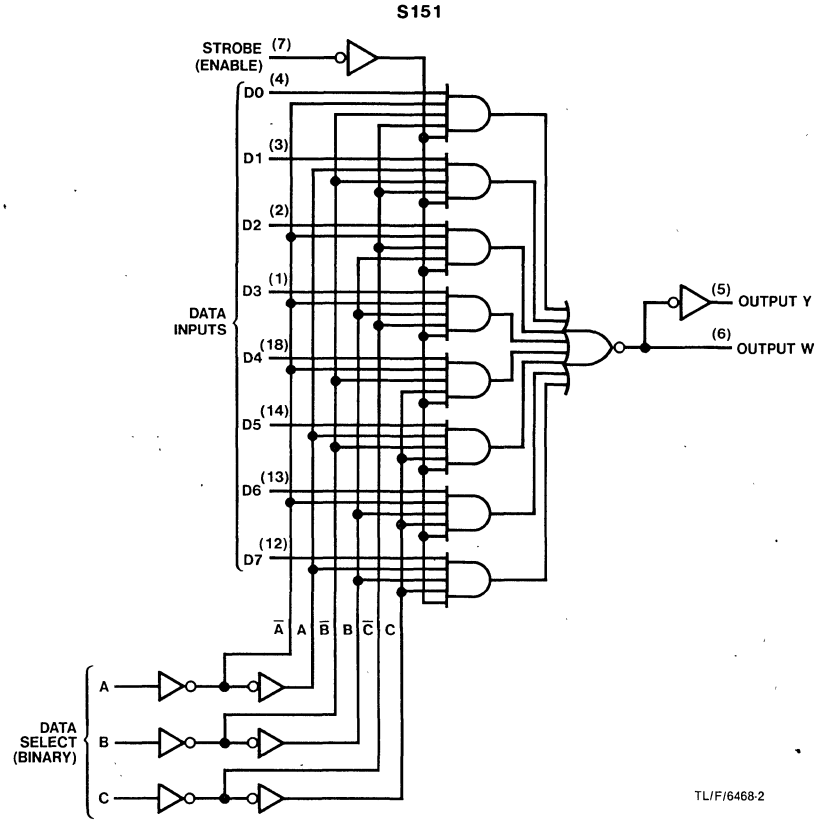
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y (4 Levels)		12	18		13	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y (4 Levels)		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to W (3 Levels)		10	15		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to W (3 Levels)		9	13.5		11	17	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		11	16.5		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to W		9	13		11	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to W		8.5	12		11	16	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		8	12		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D0 thru D7 to W		4.5	7		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D0 thru D7 to W		4.5	7		6.5	10	ns

Logic Diagram



National Semiconductor

DM54S153/DM74S153 Dual 1 of 4 Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

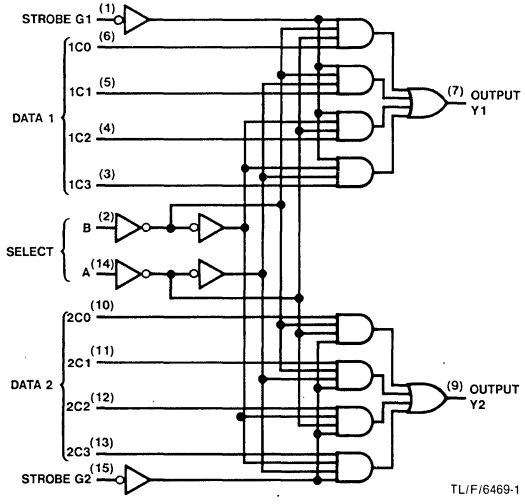
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  From data 6 ns
  From strobe 9.5 ns
  From select 12 ns
- Typical power dissipation 225 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

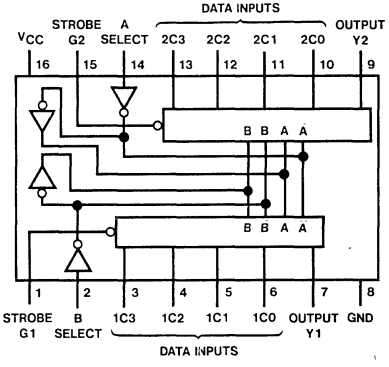
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Logic and Connection Diagrams



TL/F/6469-1

Dual-In-Line Package



54S153 (J) 74S153 (N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Sym	Parameter	DM54S153			DM74S153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs gounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		6	9		7.5	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		6	9		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		12	18		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		10	15		15	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		9	13.5		11	17	ns

5

National Semiconductor

DM54S157/DM74S157, DM54S158/DM74S158 Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The S157 presents true data whereas the S158 presents inverted data to minimize propagation delay time.

Features

- Buffered inputs and outputs
- Typical propagation time
  - S157 5 ns
  - S158 4 ns
- Typical power dissipation
  - S157 250 mW
  - S158 195 mW

Applications

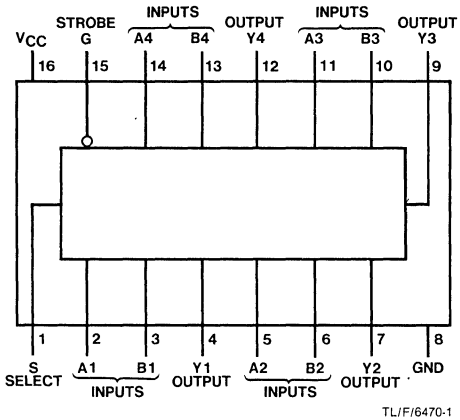
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

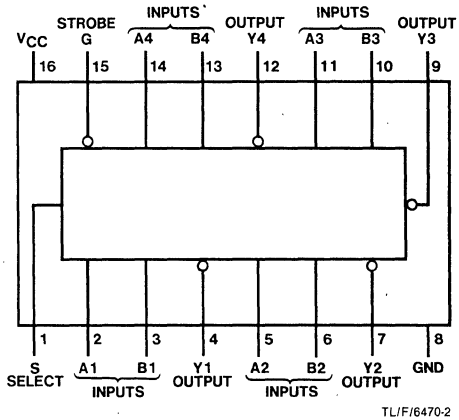
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams (Dual-In-Line Packages)



TL/F/6470-1

54S157 (J) 74S157 (N)



TL/F/6470-2

54S158 (J) 74S158 (N)

Function Table

Inputs				Output Y	
Strobe	Select	A	B	S157	S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Sym	Parameter	DM54S157			DM74S157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S157 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			100	μA
			A or B			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	S or G			−4	mA
			A or B			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	78	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured 4.5V applied to all inputs and all outputs open.

'S157 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		5	7.5		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		4.5	6.5		6.5	10	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		8.5	12.5		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		7.5	12		9.5	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		9.5	15		11	17	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		9.5	15		12	17	ns

Recommended Operating Conditions

Sym	Parameter	DM54S158			DM74S158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S158 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			100	μA
			A or B			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	S or G			−4	mA
			A or B			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			39	61	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)				81	mA

'S158 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		4	6		5.5	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		4	6		6	9	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		6.5	11.5		8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		7	12		9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		8	12		9.5	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		8	12		10	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

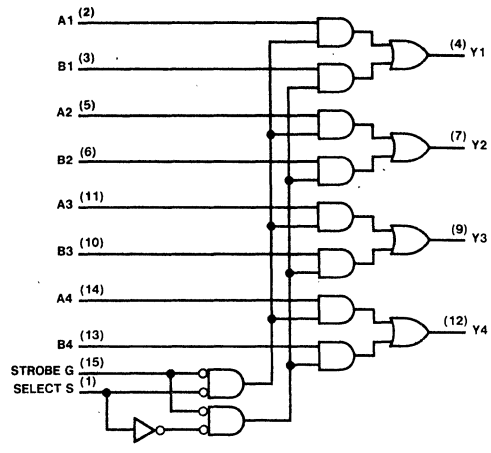
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open and all inputs at 4.5V.

Note 4: I_{CC2} is measured with B, G, and S inputs grounded, A inputs at 4.5V, and all outputs open.

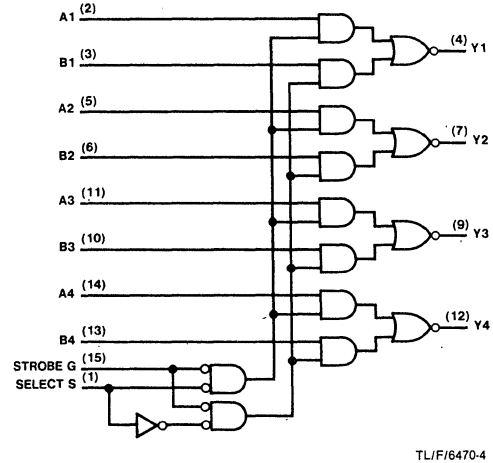
Logic Diagrams

S157



TL/F/6470-3

S158



TL/F/6470-4

National Semiconductor

DM54S160/DM74S160, DM54S161/DM74S161, DM54S162/DM74S162, DM54S163/DM74S163 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The S160 and S162 are 4-bit decade counters and the S161 and S163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 9 ns
- Typical clock frequency 70 MHz
- Typical power dissipation 475 mW

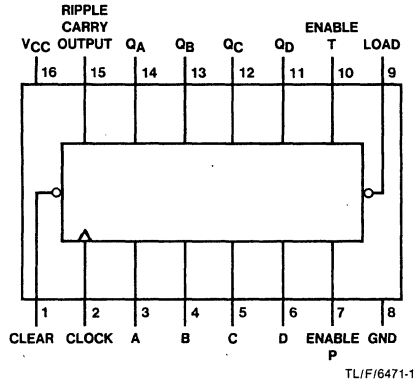
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6471-1

DM54S160 (J) DM74S160 (N)
DM54S161 (J) DM74S161 (N)
DM54S162 (J) DM74S162 (N)
DM54S163 (J) DM74S163 (N)

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S161 thru 163			DM74S161 thru 163			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0		40	0		40	MHz
	Clock Frequency (Note 2)		0		35	0		35	
t_W	Pulse Width (Note 1)	Clock	10			10			ns
		Clear	10			10			
	Pulse Width (Note 2)	Clock	12			12			
		Clear	12			12			
t_{SU}	Setup Time (Note 1)	Data	4			4			ns
		Enable P	12			12			
		Load	14			14			
		Clear (Note 3)	14			14			
	Setup Time (Note 2)	Data	5			5			
		Enable P	14			14			
		Load	16			16			
		Clear (Note 3)	16			16			
t_H	Hold Time (Note 1)	Data	3			3			ns
		Others	0			0			
	Hold Time (Note 2)	Data	5			5			
		Others	2			2			
t_{REL}	Clear Release Time (Note 1)		12			12			ns
	Clear Release Time (Note 2)		14			14			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 2: $C_L = 50$ pF and $R_L = 280\Omega$.
Note 3: Applies only to 'S162 and 'S163 which have synchronous clear inputs.

'S160 thru 'S163 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			100	μA
			Others			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Enable T			−4	mA
			Others			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			95	160	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		40	70		35	60		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		14	25		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		17	25		19	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		8	15		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		10	15		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		10	15		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		10	15		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output (Note 3)	Clear to Any Q		14	20		16	24	ns

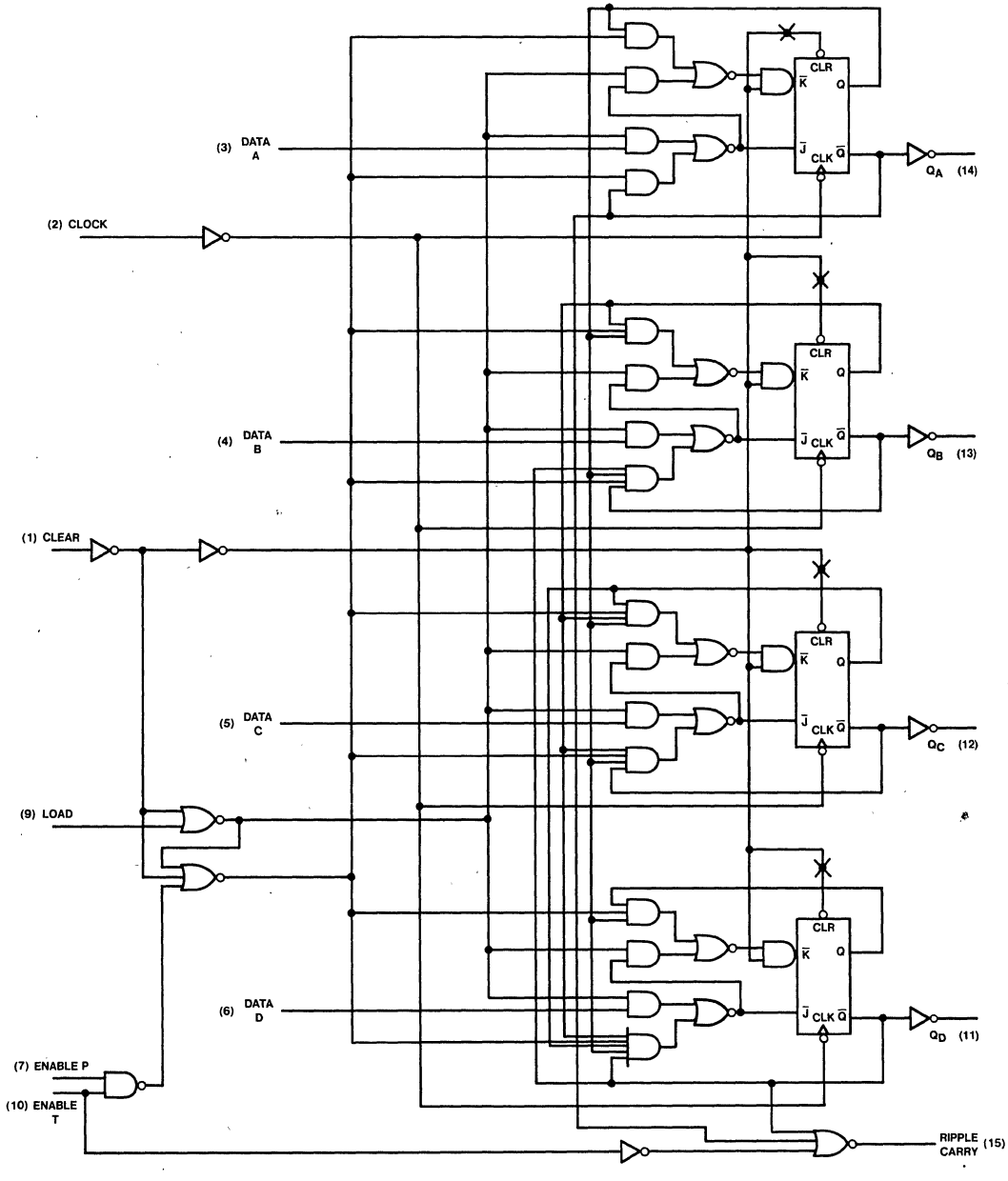
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Propagation delay for clearing is measured from clear input for 'S160 and 'S161 and from the clock input transition for the 'S162 and 'S163.

Logic Diagrams

S160, S162

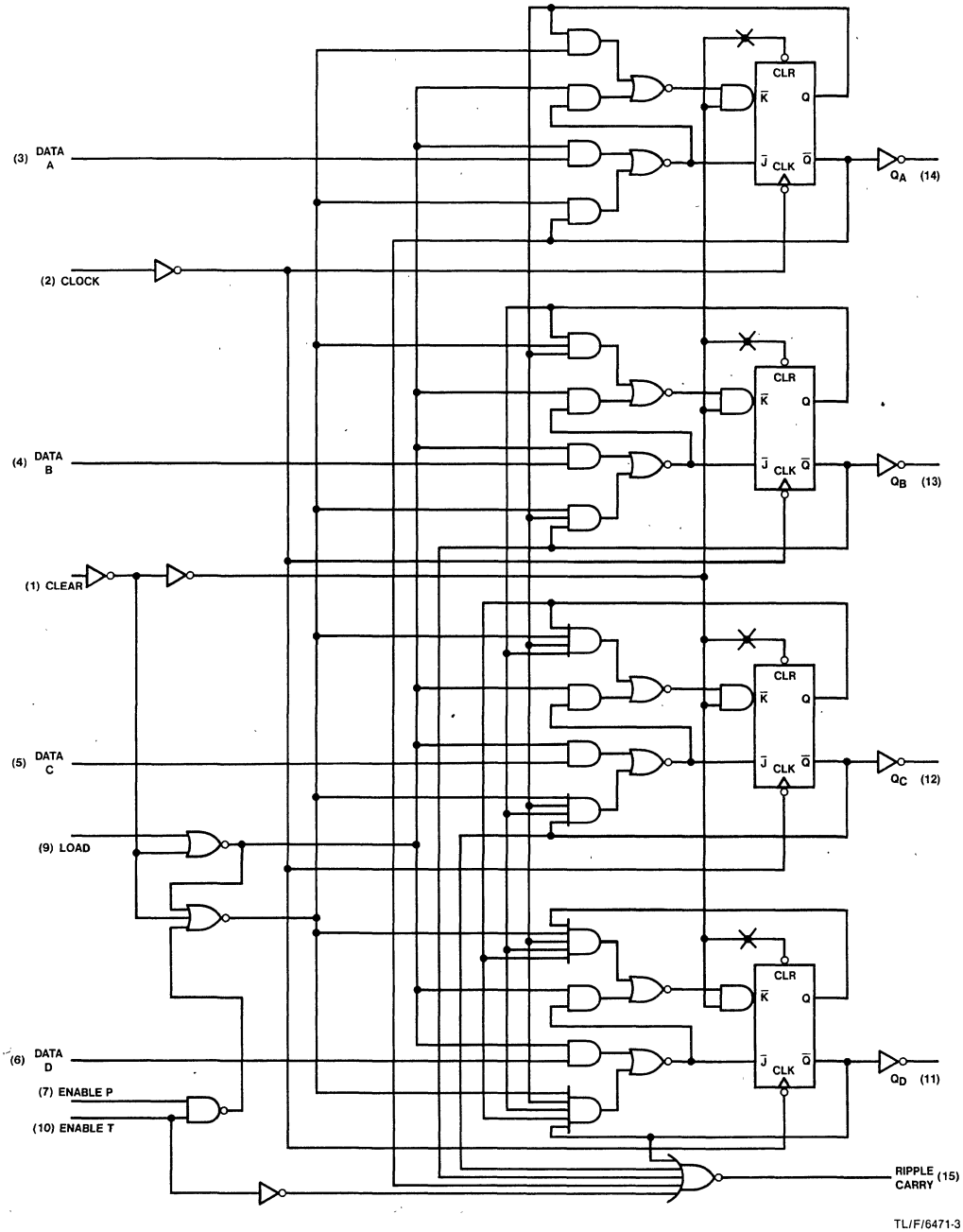


TL/F/6471-2

S160 option

Logic Diagrams (Continued)

S161, S163

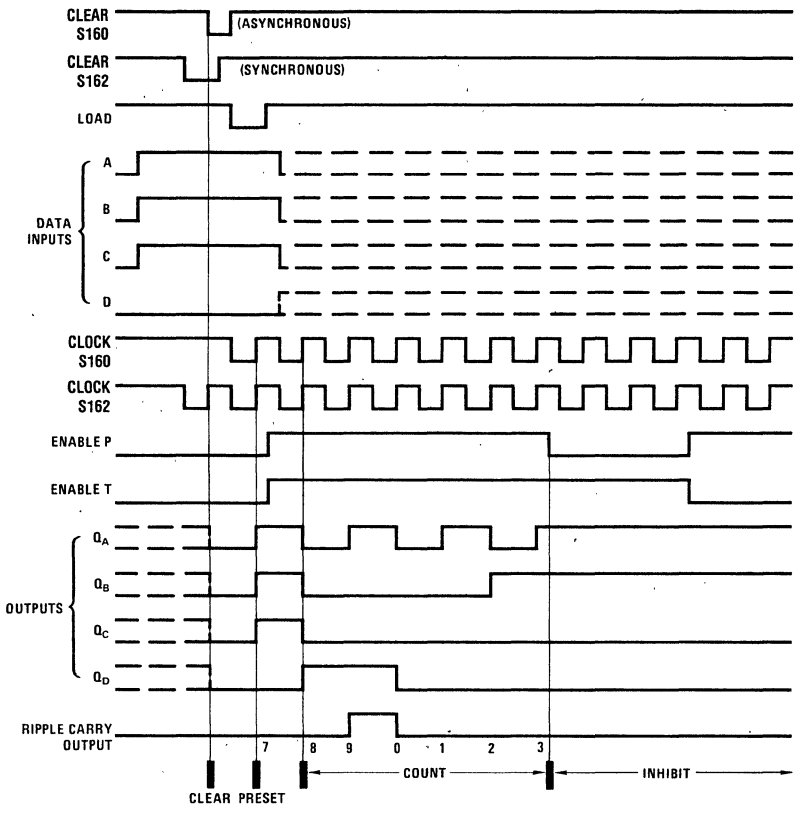


TL/F/6471-3

X S161 option

Timing Diagrams

S160, S162 Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequences



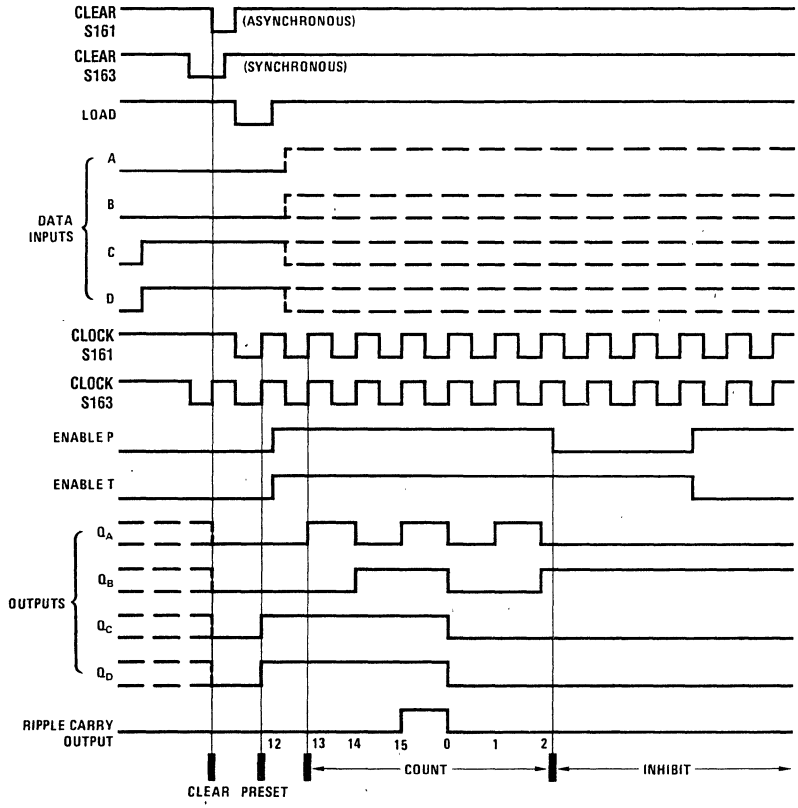
TL/F/6471-4

Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

Timing Diagrams (Continued)

S161, S163 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



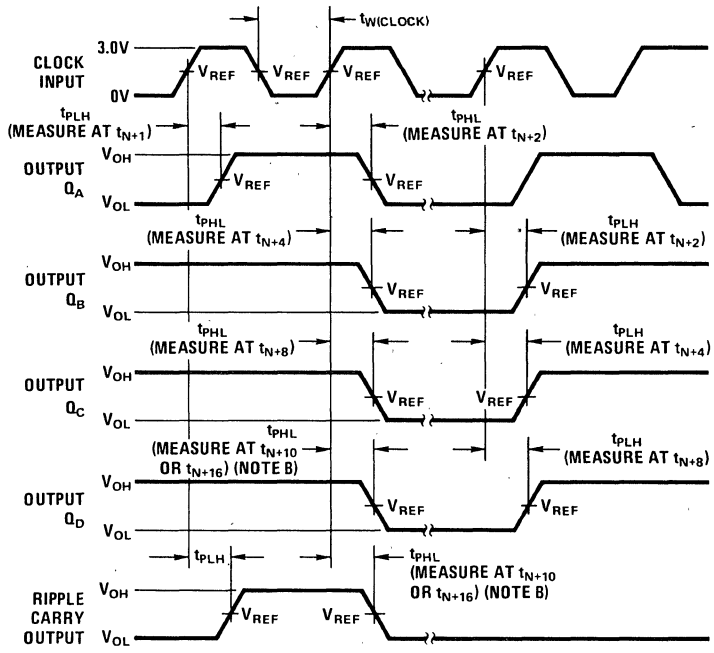
TL/F/6471-5

Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

SWITCHING TIME WAVEFORMS



TL/F/6471-6

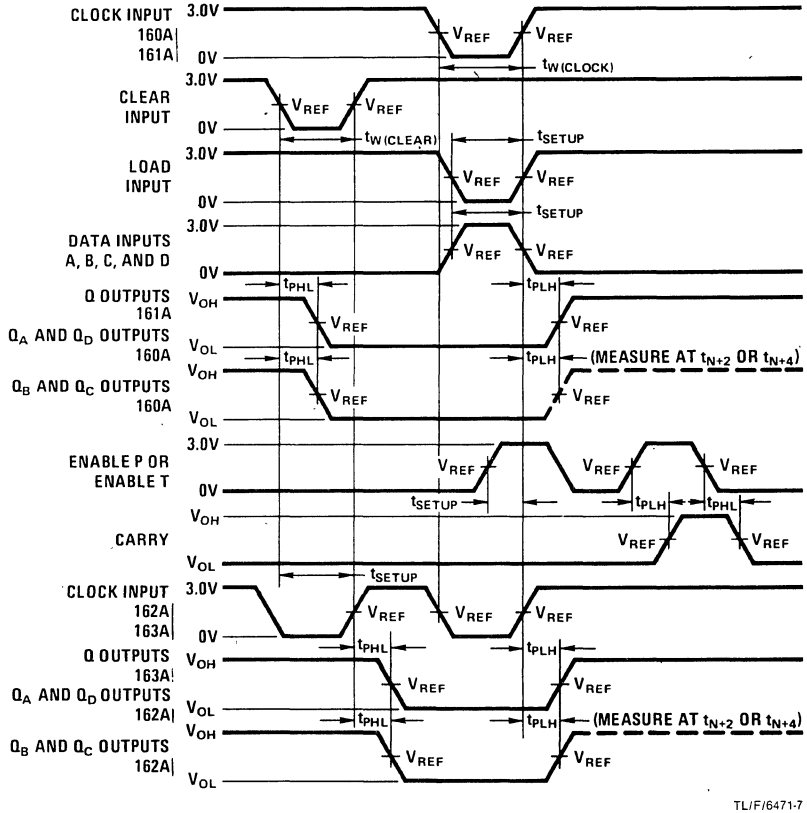
Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S160 through S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for S160, S162 and at t_{n+16} for S161, S163 where t_n is the bit time when all outputs are low.

Note C: For S160 through S163, $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

SWITCHING TIME WAVEFORMS



TL/F/6471-7

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S160 through S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at $t_n + 0$.

Note C: For S160 through S163, $V_{REF} = 1.5V$.

National Semiconductor

DM54S174/DM74S174, DM54S175/DM74S175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- S174 contain six flip-flops with single-rail outputs.
- S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75 mW

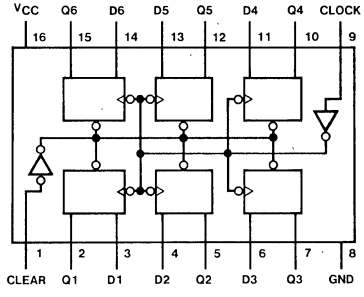
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

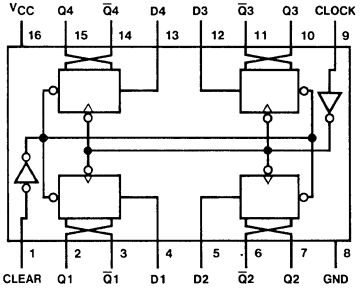
Dual-In-Line Package



TL/F/6472-1

54S174 (J) 74S174 (N)

Dual-In-Line Package



TL/F/6472-2

54S175 (J) 74S175 (N)

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = S175 only

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S174, S175			DM74S174, S175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	65	0	90	65	MHz
t_W	Pulse Width (Note 1)	Clock	7			7			ns
		Clear	10			10			
	Pulse Width (Note 2)	Clock	9			9			
		Clear	12			12			
t_{SU}	Data Setup Time (Note 1)		5			5			ns
	Data Setup Time (Note 2)		7			7			
t_H	Data Hold Time (Note 1)		3			3			ns
	Data Hold Time (Note 2)		5			5			
t_{REL}	Clear Release Time (Note 1)		5			5			ns
	Clear Release Time (Note 2)		7			7			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 280\Omega$.

Note 2: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current (S174)	V_{CC} = Max (Note 3)			90	144	mA
I_{CC}	Supply Current (S175)	V_{CC} = Max (Note 3)			60	96	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		75	110		65	90		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		8	12		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		12	17		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output (S175 Only)	Clear to $\overline{Q}$		10	15		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		13	22		15	23	ns

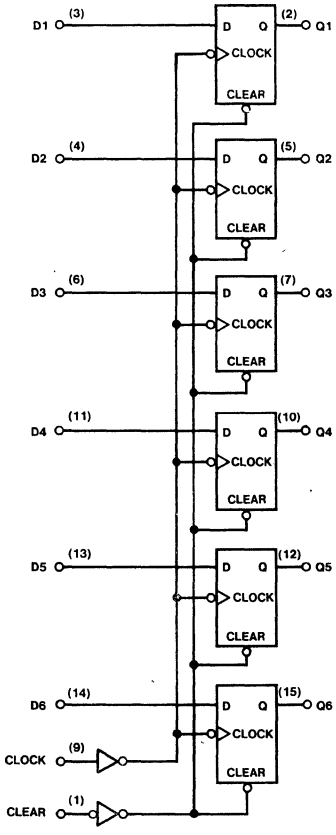
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

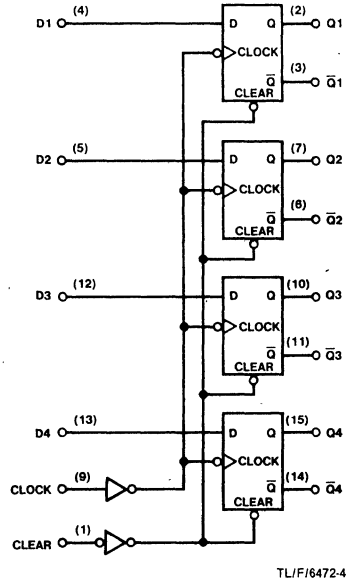
Logic Diagrams

S174



TL/F/6472-3

S175



TL/F/6472-4

5

National Semiconductor

DM54S181/DM74S181 Arithmetic Logic Unit/Function Generators

General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182. (Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

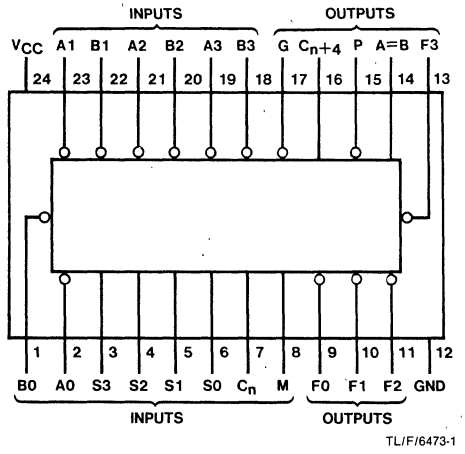
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6473-1

54S181 (J) **74S181 (N)**

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54S181/DM74S181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

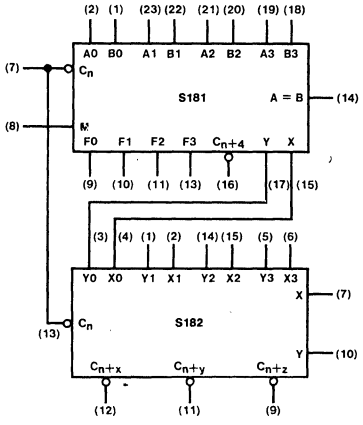
The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table II)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_{n+4}	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

General Description (Continued)



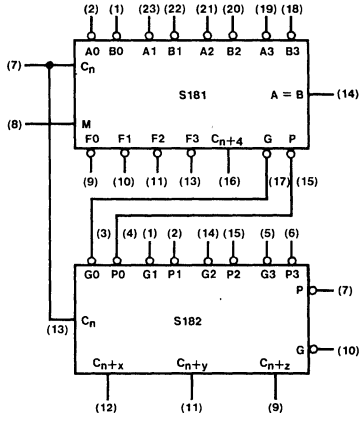
TL/F/6473-2

Figure 1

Table I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $A\overline{B}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A $\oplus$ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.



TL/F/6473-3

Figure 2

Table II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Recommended Operating Conditions

Sym	Parameter	DM54S181			DM74S181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5			5.5	V
I_{OH}	High Level Output Current (All Except A = B)			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OH}	High Level Output Voltage (All Except A = B)	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Mode			50	μA
			A or B			150	
			S			200	
			Carry			250	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Mode			−2	mA
			A or B			−6	
			S			−8	
			Carry			−10	
I_{OS}	Short Circuit Output Current (Any Output Except A = B)	V_{CC} = Max (Note 2)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			120	220	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured for the following conditions: A. S0 through S3, M, and A inputs at 4.5V, all other inputs grounded and all outputs open. B. S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter	From (Input)	To (Output)	Conditions	DM54/74 S181						Units
					R_L = 280 Ω, C_L = 15 pF			R_L = 280 Ω, C_L = 50 pF			
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+4}			7	10.5		9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	10.5		9	14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		12.5	18.5		14.5	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12.5	18.5		14.5	22	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15.5	23		17.5	27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15.5	23		17.5	27	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		7	12		9	14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7	12		9	14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		8	12		10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7.5	12		10	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15		12.5	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10.5	15		13	20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		7.5	12		9.5	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					7.5	12		10	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15		12.5	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10.5	15		13	20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		11	16.5		13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					11	16.5		13	20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		14	20		16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	22		16	24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5 V (logic mode)		14	20		16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	22		16	24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15	23		17	26	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					20	30		22	33	

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							

$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}							
t_{PLH}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All A	All B	Any F or C_{n+4}	In-Phase
t_{PHL}							
t_{PLH}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							

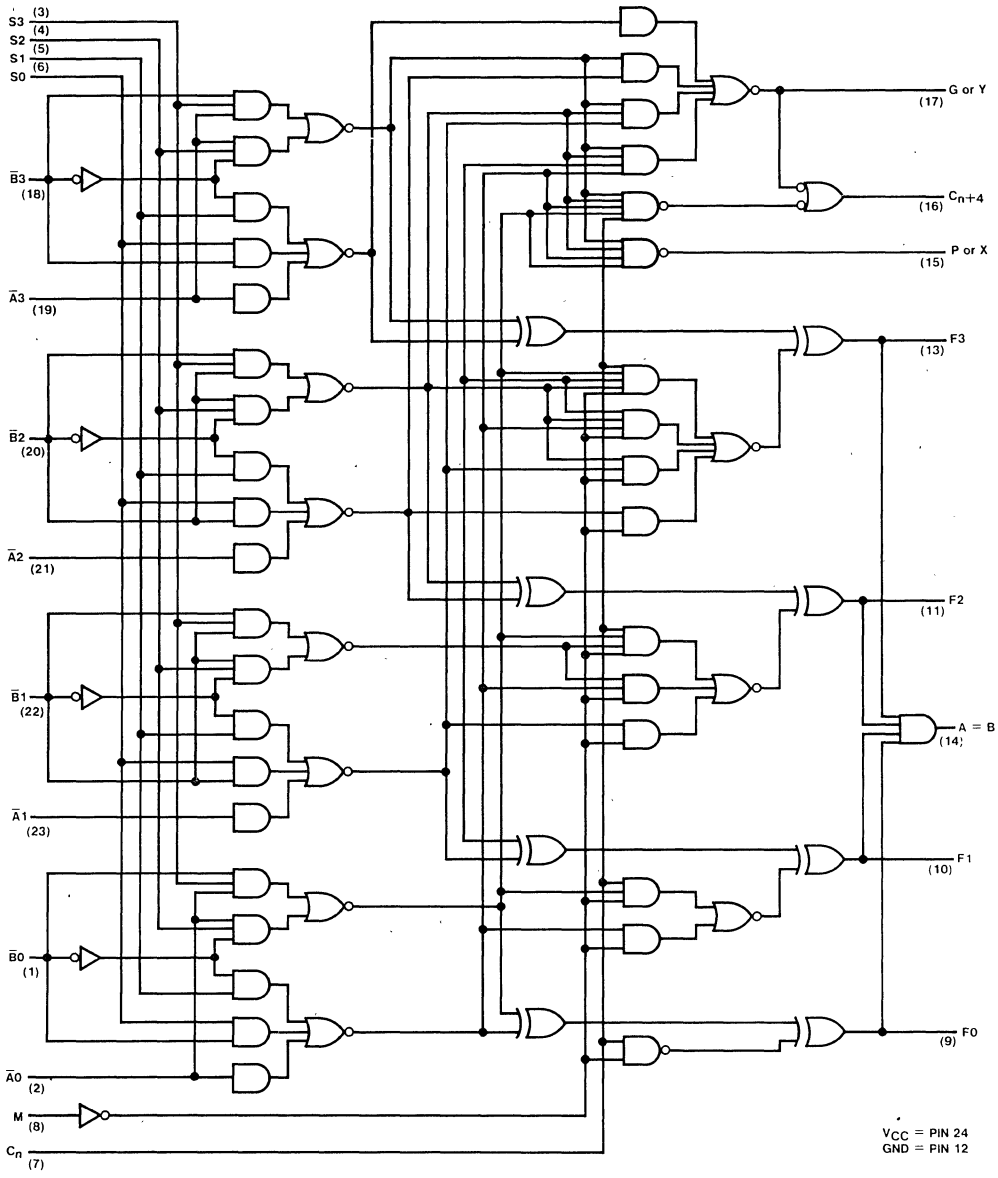
5

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase

Logic Diagram



National Semiconductor

DM54S182/DM74S182 Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:

$C_{n+x} = \overline{G}0 + \overline{P}0\ C_n$

$C_{n+y} = \overline{G}1 + \overline{P}1\ \overline{G}0 + \overline{P}1\ \overline{P}0\ C_n$

$C_{n+z} = \overline{G}2 + \overline{P}2\ \overline{G}1 + \overline{P}2\ \overline{P}1\ \overline{G}0 + \overline{P}2\ \overline{P}1\ \overline{P}0\ C_n$

$\overline{G} = \overline{G}3\ (\overline{P}3 + \overline{G}2)\ (\overline{P}3 + \overline{P}2 + \overline{G}1)\ (\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$

$\overline{P} = \overline{P}3\ \overline{P}2\ \overline{P}1\ \overline{P}0$

Features

- Typical propagation delay time 7 ns
- Typical power dissipation 260 mW

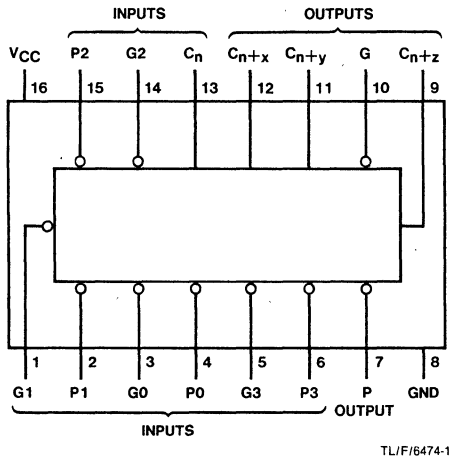
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6474-1

54S182 (J) **74S182 (N)**

Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

Recommended Operating Conditions

Sym	Parameter	DM54S182			DM74S182			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	P0, P1 or G3			200	μA
			P3			100	
			P2			150	
			C_n			50	
			G0, G2			350	
			G1			400	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	P0, P1 or G3			−8	mA
			P3			−4	
			P2			−6	
			C_n			−2	
			G0, G2			−14	
			G1			−16	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		39	55	mA
			DM74		39	55	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM54		69	99	mA
			DM74		69	109	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

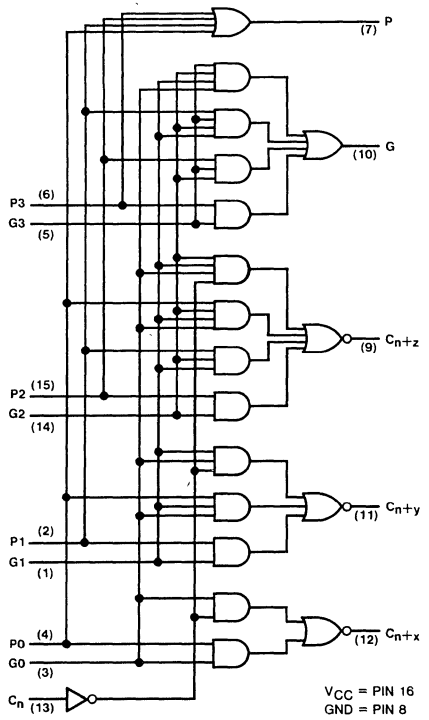
Note 3: I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open: Inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	GN or PN to $C_{n+x, y, z}$		4.5	7		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	GN or PN to $C_{n+x, y, z}$		4.5	7		7	11	ns
t_{PLH} Propagation Delay Time Low to High Level Output	GN or PN to G		5	7.5		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	GN or PN to G		7	10.5		9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	PN to P		4.5	6.5		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	PN to P		6.5	10		9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C_n to $C_{n+x, y, z}$		6.5	10		8.5	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C_n to $C_{n+x, y, z}$		7	10.5		8.5	14	ns

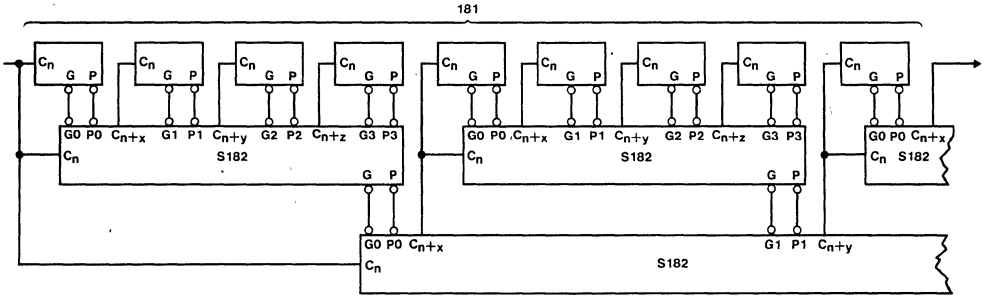
Logic Diagram



TL/F/6474-2

Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.

TL/F/6474-3

National Semiconductor

DM54S194/DM74S194
4-Bit Bidirectional Universal Shift Registers

General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 105 MHz
- Typical power dissipation 425 mW

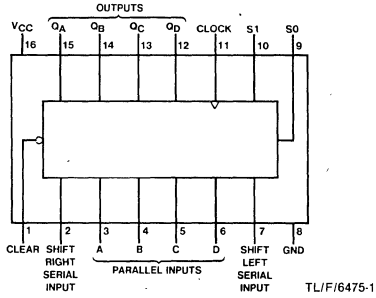
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6475-1

Function Table

54S194 (J) **74S194 (N)**

Inputs										Outputs			
Clear	Mode S1	Mode S0	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock

Recommended Operating Conditions

Sym	Parameter		DM54S194			DM74S194			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	105	70	0	105	70	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	60	0	90	60	MHz
t_W	Pulse Width	Clock	7			7			ns
		Clear	12			12			
t_{SU}	Setup Time	Mode	11			11			ns
		Data	5			5			
t_H	Hold Time		3			3			ns
t_{REL}	Clear Release Time		9			9			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 280\Omega$.

Note 2: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			85	135	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

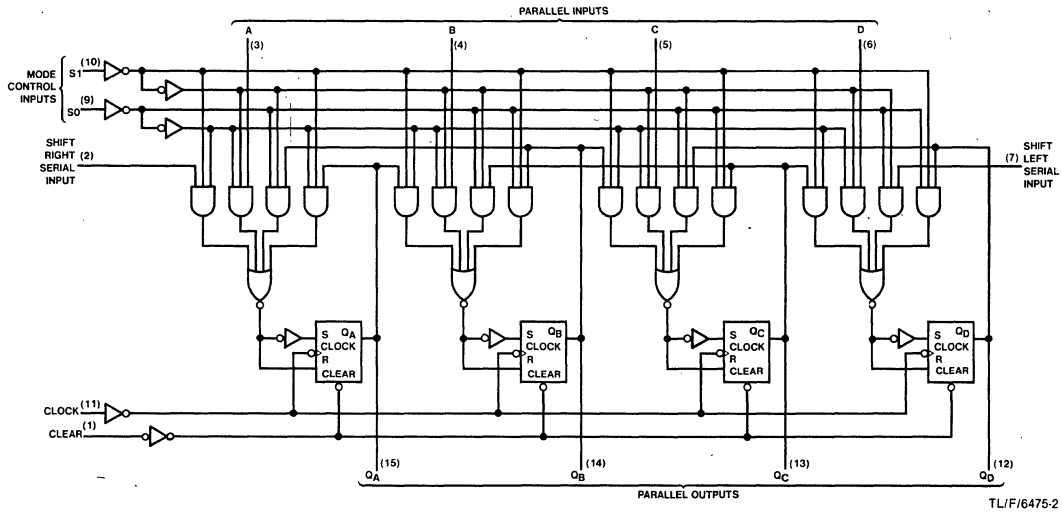
Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the SERIAL inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		70	105		60	90		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		8	12		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		11	16.5		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		13	18.5		15	23	ns

Logic Diagram

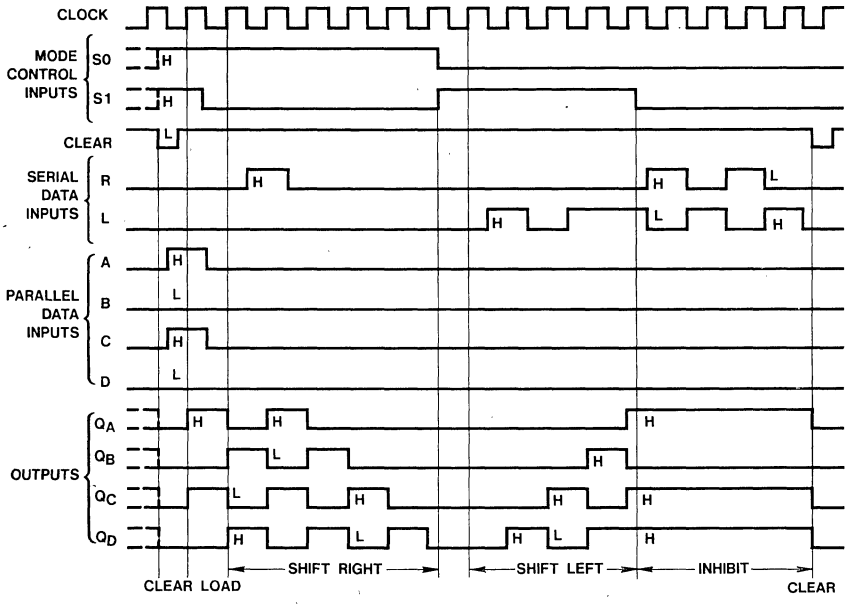
S194



TL/F/6475-2

Timing Diagram

TYPICAL CLEAR, LOAD , RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



TL/F/6475-3

National Semiconductor

DM54S195/DM74S195 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 105 MHz
- Typical power dissipation 350 mW

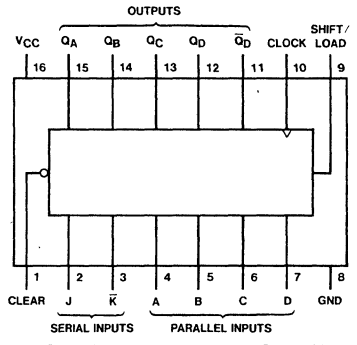
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6476-1

54S195 (J) **74S195 (N)**

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a,b,c,d = The level of steady state input at A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S195			DM74S195			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	105	70	0	105	70	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	60	0	90	60	MHz
t_W	Pulse Width	Clock	7			7			ns
		Clear	12			12			
t_{SU}	Setup Time	Shift/ Load	11			11			ns
		Data	5			5			
t_H	Data Hold Time		3			3			ns
t_{REL}	Shift/Load Release Time		6			6			ns
	Clear Release Time		9			9			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 280\Omega$.

Note 2: $C_L = 50$ pF and $R_L = 280\Omega$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			70	109	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

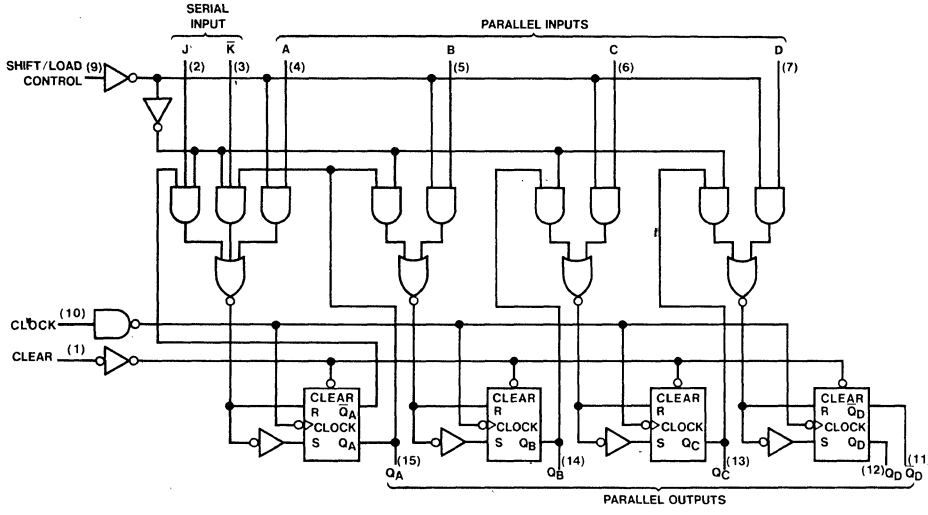
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		75	105		60	90		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		8	12		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		11	16.5		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		12	18.5		15	23	ns

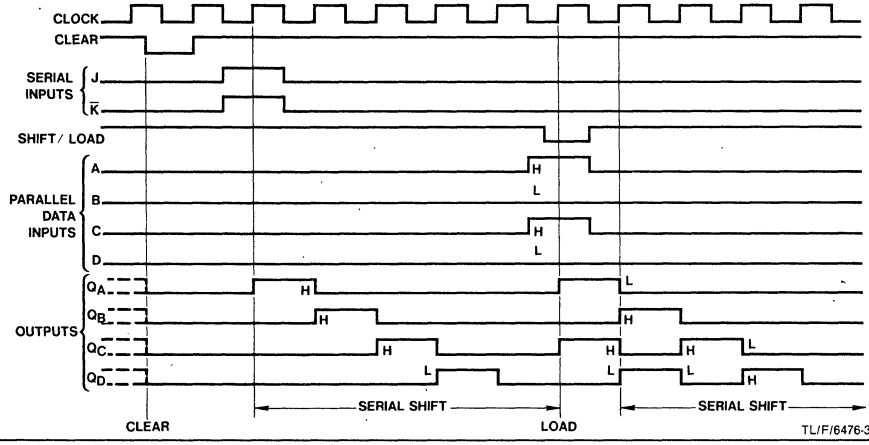
Logic Diagram



TL/F/6476-2

Timing Diagram

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



TL/F/6476-3

National Semiconductor

DM54S196/DM74S196, DM54S197/DM74S197 Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (S196) or a divide-by-two and a divide-by-eight counter (S197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive. (Continued)

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input
- Typical count frequency
  Clock 1 100 MHz
  Clock 2 50 MHz
- Typical power dissipation 375 mW

Absolute Maximum Ratings (Note 1)

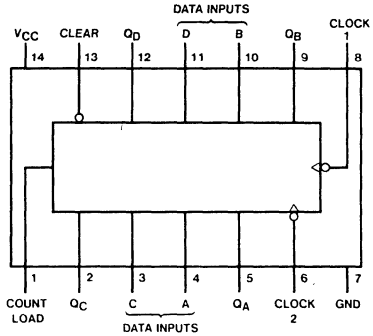
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

5

Connection Diagram

Dual-In-Line Package



Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low

TL/F/6477-1

54S196 (J) 74S196 (N)
54S197(J) 74S197 (N)

General Description (Continued)

TYPICAL COUNT CONFIGURATIONS S196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

S197

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Function Tables

S196

Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = High Level, L = Low Level

Note A: Output Q_A connected to clock-2 input
Note B: Output Q_D connected to clock-1 input

S196

(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

S197

(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S196, S197			DM74S196, S197			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	140	100	0	140	100	MHz
f_{CLK}	Clock Frequency (Note 3)		0	110	80	0	110	80	MHz
t_W	Pulse Width (Note 2)	Clock1	5			5			ns
		Clock2	10			10			
		Clear	30			30			
		Load	5			5			
	Pulse Width (Note 3)	Clock1	7			7			
		Clock2	12			12			
		Clear	35			35			
		Load	7			7			
t_{SU}	Data Setup Time (Notes 1 and 2)		6↑			6↑			ns
	Data Setup Time (Notes 1 and 3)		8↑			8↑			
t_H	Data Hold Time (Notes 1 and 2)		3↑			3↑			ns
	Data Hold Time (Notes 1 and 3)		5↑			5↑			
t_{EN}	Count Enable Time (Note 2 and 4)		12			12			ns
t_{EN}	Count Entable Time (Note 3 and 4)		14			14			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.

Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

Note 4: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

'S196 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max (Note 4)				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Clock1			−8	mA
			Clock2			−10	
			Others			−0.75	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			75	110	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the CLOCK2 input. This permits driving the CLOCK2 input while maintaining full fan-out capability.

'S196 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock1 to Q_A	100	140		80	110		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock1 to Q_A		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock1 to Q_A		6	10		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_B		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_B		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_C		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_C		16	24		18	27	ns

'S196 Switching Characteristics (Continued) at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_D		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_D		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		7	12		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		10	18		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		26	37		30	45	ns

'S197 Electrical Characteristics over recommended operating free air temperature

(unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = Min$, $I_I = -18$ mA				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = Min$, $I_{OH} = Max$, $V_{IL} = Max$, $V_{IH} = Min$	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = Min$, $I_{OL} = Max$, $V_{IH} = Min$, $V_{IL} = Max$ (Note 4)				0.5	V
I_I	Input Current@Max Input Voltage	$V_{CC} = Max$, $V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = Max$, $V_I = 2.7V$				50	μA
I_{IL}	Low Level Input Current	$V_{CC} = Max$, $V_I = 0.5V$	Clock1			−8	mA
			Clock2			−6	
			Others			−0.75	
I_{OS}	Short Circuit Output Current	$V_{CC} = Max$ (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	$V_{CC} = Max$ (Note 3)			75	110	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the CLOCK2 input. This permits driving the CLOCK2 input while maintaining full fan-out capability.

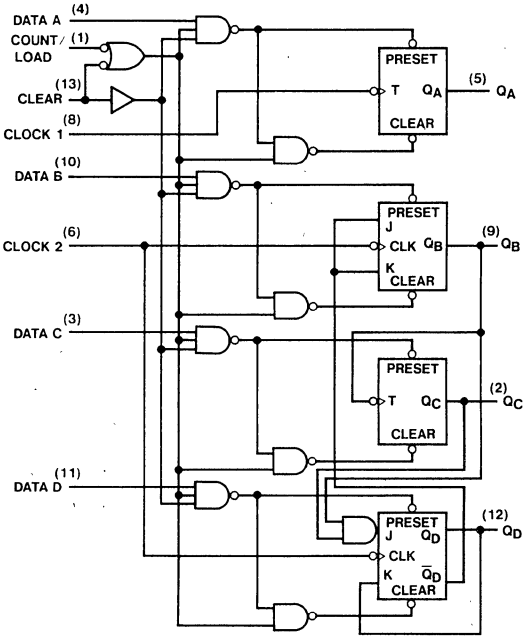
'S197 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock1 to QA	100	140		80	110		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock1 to Q_A		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock1 to Q_A		6	10		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_B		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_B		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_C		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_C		15	22		17	26	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_D		18	27		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_D		22	33		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		7	12		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		10	18		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		26	37		30	45	ns

Logic Diagrams

S196



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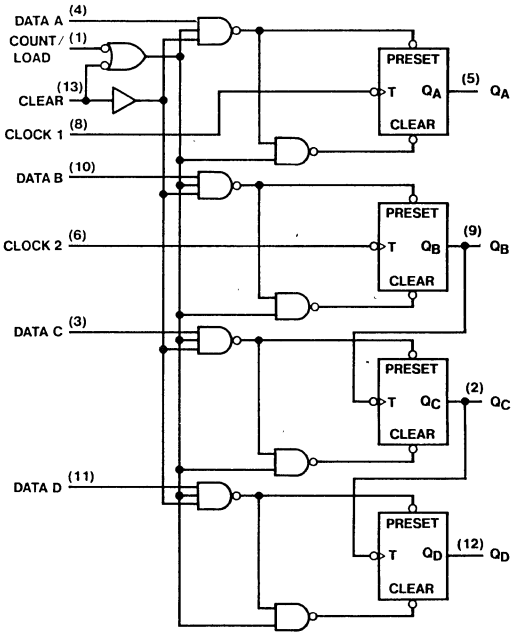
S197



TL/F/6477-3

5

National Semiconductor

DM54S240/DM74S240, DM54S241/DM74S241, DM54S244/DM74S244 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE® buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133 Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54S 48 mA
  - 74S 64 mA
- Typical I_{OH} (source current)
  - 54S −12 mA
  - 74S −15 mA
- Typical propagation delay times
  - Inverting 4.5 ns
  - Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
  - Inverting 450 mW
  - Noninverting 538 mW

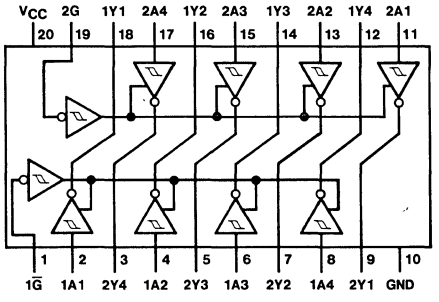
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

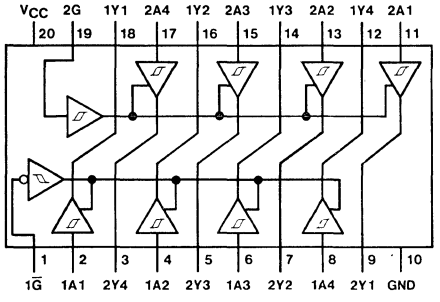
Dual-In-Line Package



TL/F/6478-1

54S240 (J) **74S240 (N)**

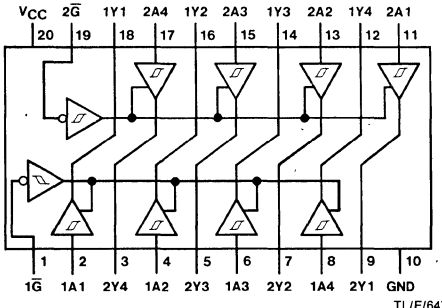
Dual-In-Line Package



TL/F/6478-2

54S241 (J) **74S241 (N)**

Dual-In-Line Package



TL/F/6478-3

54S244 (J) **74S244 (N)**

Recommended Operating Conditions

Symbol	Parameter	DM54S			DM74S			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	DM74	2.7			V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = 0.8V, V_{IH} = 2V	DM54			0.55	V
			DM74			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V, V_O = 2.4V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V, V_O = 0.5V				−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Any A			−400	μA
			Any G			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	DM54S240		80	123	mA
			DM74S240		80	135	
			DM54S241, 244		95	147	
			DM74S241, 244		95	160	
		Outputs Low	DM54S240		100	145	
			DM74S240		100	150	
			DM54S241, 244		120	170	
			DM74S241, 244		120	180	
		Outputs Disabled	DM54S240		100	145	
			DM74S240		100	150	
			DM54S241, 244		120	170	
			DM74S241, 244		120	180	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time and duration should not exceed one second

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S240	2	4.5	7	ns
			DM54/74S241, 244	2	6	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S240	2	4.5	7	ns
			DM54/74S241, 244	2	6	9	
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S240	3	10	15	ns
			DM54/74S241, 244	3	10	15	
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S240	2	6.5	10	ns
			DM54/74S241, 244	3	8	12	
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, $R_L = 90\Omega$	DM54/74S240	4	10	15	ns
			DM54/74S241, 244	2	10	15	
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, $R_L = 90\Omega$	DM54/74S240	2	6	9	ns
			DM54/74S241, 244	2	6	9	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S240	3	7	10	ns
			DM54/74S241, 244	4	9	12	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S240	3	7	10	ns
			DM54/74S241, 244	4	9	12	
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S240	6	14	21	ns
			DM54/74S241, 244	6	14	21	
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S240	4	9	12	ns
			DM54/74S241, 244	4	10	15	

National Semiconductor

DM54S242/DM74S242, DM54S243/DM74S243 Quadruple Bus Transceivers

General Description

These four data line transceivers are designed for asynchronous two-way communications between data buses. They can be used to drive terminated lines down to 133 ohms.

Features

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

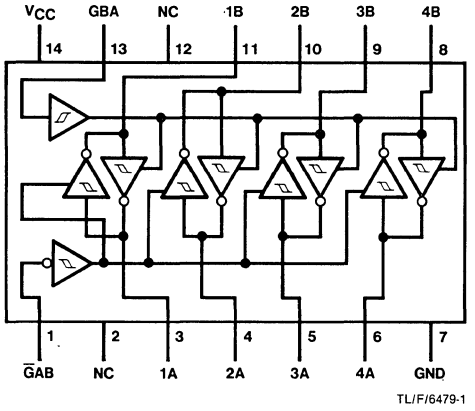
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

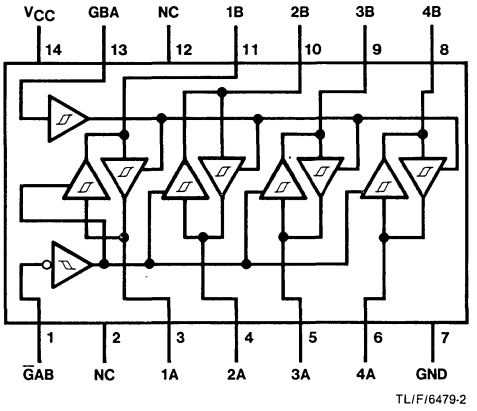
Dual-In-Line Package



TL/F/6479-1

54S242 (J) 74S242 (N)

Dual-In-Line Package



TL/F/6479-2

54S243 (J) 74S243 (N)

Function Table

Control Inputs		S242 Data Port Status		S243 Data Port Status	
$\overline{G}AB$	GBA	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	•	•	•	•
H	L	ISOLATED		ISOLATED	
L	L	I	$\overline{O}$	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

I = Input, O = Output, $\overline{O}$ = Inverting Output.

Recommended Operating Conditions

Symbol	Parameter	DM54S			DM74S			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −1 mA		2.7			V
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = 0.8V, V_{IH} = 2V	DM54			0.55	V
			DM74			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IL} = 0.8V, V_{IH} = 2V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{IH} = 2V, V_O = 0.5V, V_{IL} = 0.8V, V_{CC} = Max				−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Any A			−400	μA
			Any G			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	DM54S242		80	123	mA
			DM74S242		80	135	
			DM54S243		95	147	
			DM74S243		95	160	
		Outputs Low	DM54S242		100	145	
			DM74S242		100	150	
			DM54S243		120	170	
			DM74S243		120	180	
		Outputs Disabled	DM54S242		100	145	
			DM74S242		100	150	
			DM54S243		120	170	
			DM74S243		120	180	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S242	2	4.5	7	ns
			DM54/74S243	2	6	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S242	2	4.5	7	ns
			DM54/74S243	2	6	9	
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S242	3	10	15	ns
			DM54/74S243	3	10	15	
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S242	2	6.5	10	ns
			DM54/74S243	3	8	12	
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, $R_L = 90\Omega$	DM54/74S242	4	10	15	ns
			DM54/74S243	2	10	15	
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, $R_L = 90\Omega$	DM54/74S242	2	6	9	ns
			DM54/74S243	2	6	9	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S242	3	7	10	ns
			DM54/74S243	4	9	12	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S242	3	7	10	ns
			DM54/74S243	4	9	12	
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S242	6	14	21	ns
			DM54/74S243	6	14	21	
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S242	4	9	12	ns
			DM54/74S243	4	10	15	

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DM54S251/DM74S251 TRI-STATE® 1 of 8 Line Data Selector/Multiplexer

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

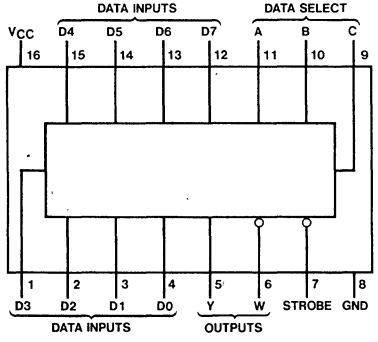
- TRI-STATE version of S151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Max no. of common outputs
  - 54S 39
  - 74S 129
- Typical propagation delay time (D to Y) 8 ns
- Typical power dissipation 275 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



TL/F/6480-1

54S251(J) 74S251(N)

Function Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1 . . . D7 = The Level of the respective D input.

Recommended Operating Conditions

Sym	Parameter	DM54S251			DM74S251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

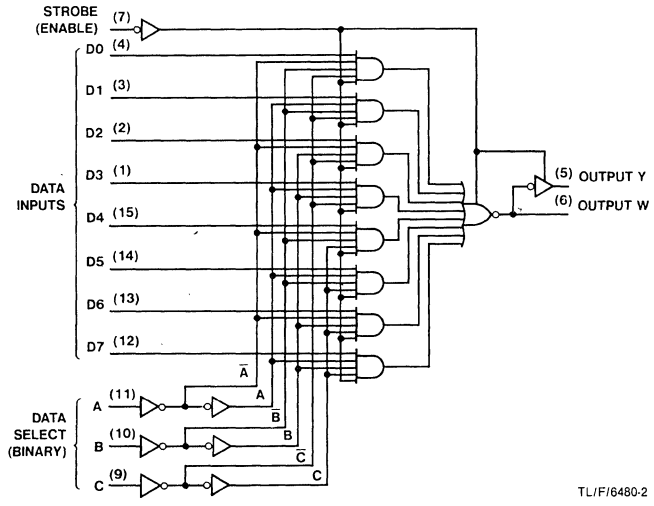
Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, or C (4 Levels) to Y		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, or C (4 Levels) to Y		13	19.5		15	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, or C (3 Levels) to W		10	15		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, or C (3 Levels) to W		9	13.5		11	17	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to Y		8	12		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to Y		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to W		4.5	7		6.5	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to W		4.5	7		6.5	10	ns
t_{PZH} Output Enable Time to High Level Output	Strobe to Y					13	19.5	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to Y					14	21	ns
t_{PHZ} Output Disable Time to High Level Output (Note 1)	Strobe to Y		5.5	8.5				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	Strobe to Y		9	14				ns
t_{PZH} Output Enable Time to High Level Output	Strobe to W					13	19.5	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to W					14	21	ns

Switching Characteristics (Continued) at $V_{CC} = 5V$ and $T_A = 25°C$

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PHZ} Output Disable Time to High Level Output (Note 1)	Strobe to W		5.5	8.5				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	Strobe to W		9	14				ns

Note 1: $C_L = 5$ pF.

Logic Diagram



National Semiconductor

DM54S253/DM74S253
Dual TRI-STATE® 1 of 4 Line Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of S153 with same pin-out
- Schottky-diode-clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs
- Typical propagation delay
  From data to output 6 ns
  From select to output 12 ns
- Typical power dissipation 275 mW

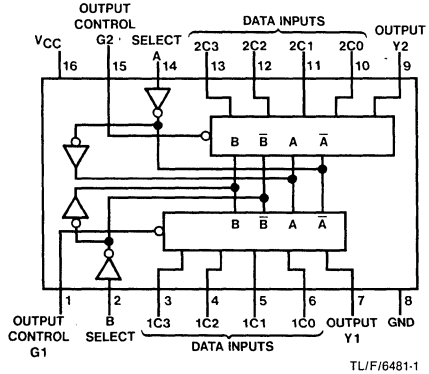
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6481-1

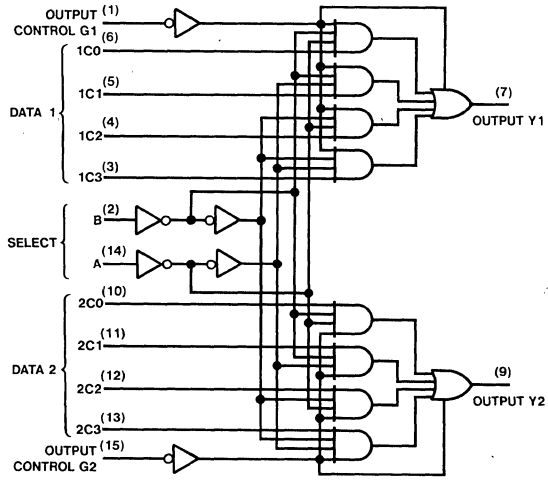
54S253 (J) **74S253(N)**

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Logic Diagram



TL/F/6481-2

Recommended Operating Conditions

Sym	Parameter	DM54S253			DM74S253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		6	9		8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		6	9		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		12	18		14	21	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y					13	19.5	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y					14	21	ns
t_{PHZ} Output Disable Time to High Level Output (Note 1)	Output Control to Y		5.5	8.5				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	Output Control to Y		9	14				ns

Note 1: $C_L = 5$ pF.

National Semiconductor

DM54S257/DM74S257, DM54S258/DM74S258 TRI-STATE® Quad 1 of 2 Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions S157, S158, with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input
  S257 4.8 ns
  S258 4 ns
- Typical power dissipation
  S257 320 mW
  S258 280 mW

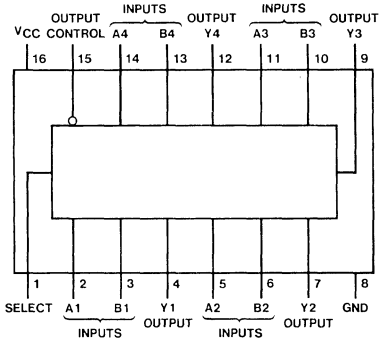
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

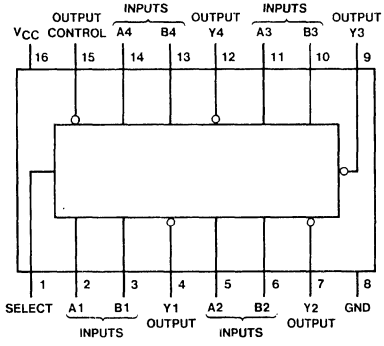
Dual-In-Line Package



TL/F/6482-1

54S257(J) 74S257(N)

Dual-In-Line Package



TL/F/6482-2

54S258(J) 74S258(N)

Function Table

Inputs				Output Y	
Output Control	Select	A	B	S257	S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

Recommended Operating Conditions

Sym	Parameter	DM54S257			DM74S257			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S257 Electrical Characteristics over recommended operating free air temperature

(unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			100	μA
			Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Select			−4	mA
			Other			−2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			44	68	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 3)			60	93	mA
I_{CCZ}	Supply Current With Outputs Disabled	V_{CC} = Max (Note 3)			64	99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'S257 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		5	7.5		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		4.5	6.5		6.5	10	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		8.5	15		11	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		8.5	15		11	16	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y		13	19.5		15	23	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y		14	21		16	24	ns
t_{PHZ} Output Disable Time to High Level Output (Note 1)	Output Control to Y		5.5	8.5				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	Output Control to Y		9	14				ns

Note 1: $C_L = 5$ pF.

Recommended Operating Conditions

Sym	Parameter	DM54S258			DM74S258			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S258 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			100	μA
			Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Select			−4	mA
			Other			−2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			36	56	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 3)			52	81	mA
I_{CCZ}	Supply Current With Outputs Disabled	V_{CC} = Max (Note 3)			56	87	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'S258 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

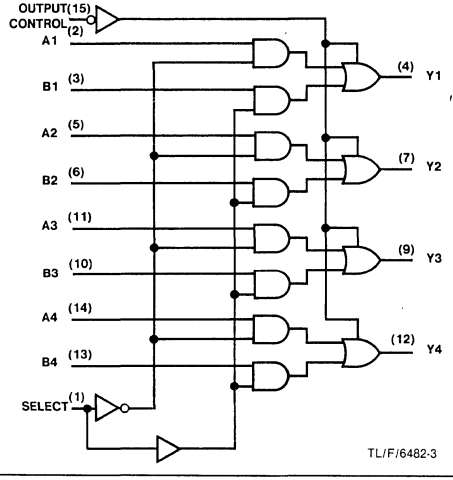
(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		4	6		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		4	6		6	9	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		8	12		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		7.5	12		9.5	15	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Y		13	19.5		15	23	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Y		14	21		16	24	ns
t_{PHZ} Output Disable Time to High Level Output (Note 1)	Output Control to Y		5.5	8.5				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	Output Control to Y		9	14				ns

Note 1: $C_L = 5$ pF.

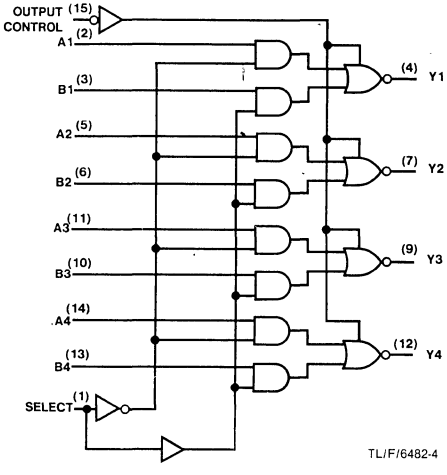
Logic Diagrams

S257



TL/F/6482-3

S258



TL/F/6482-4

National Semiconductor

DM54S280/DM74S280 9-Bit Parity Generators/Checkers

General Description

These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.

The S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4, and no internal connection at pin 3. This permits the S280 to be substituted for the 180 in existing designs to produce an identical function, even if S280's are mixed with existing 180's.

Input buffers are provided so that each input represents only one normal 74S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

Features

- Generates either odd or even parity for nine data lines
- Cascadable for n-bits
- Can be used to upgrade existing systems using MSI parity circuits
- Typical data-to-output delay—14 ns

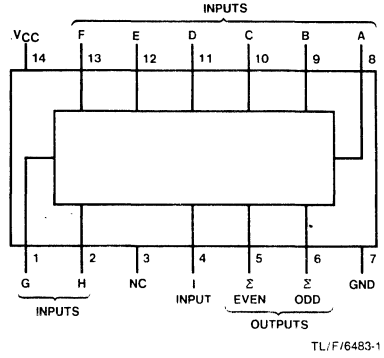
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6483-1

54S280(J) 74S280(N)

Function Table

Number of Inputs (A Thru I) that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Recommended Operating Conditions

Sym	Parameter	DM54S280			DM74S280			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			67	105	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

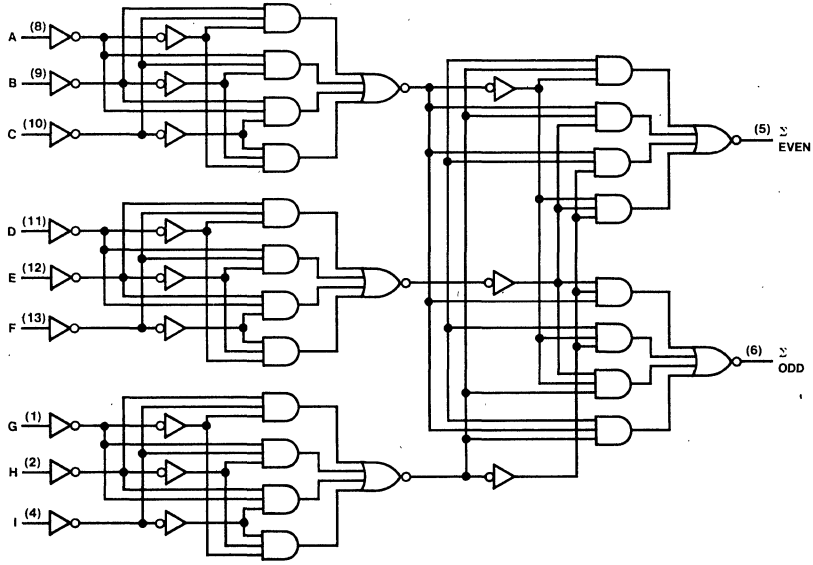
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 180\Omega$ $C_L = 15$ pF			$R_L = 280\Omega$ $C_L = 50$ pF			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Σ Even		14	21		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Σ Even		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Σ Odd		14	21		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Σ Odd		12	18		14	21	ns

Logic Diagram



TL/F/6483-2

Typical Applications

Three S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 ns. (See *Figure 1.*)

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (S86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading S280's. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits in typically 25 ns.

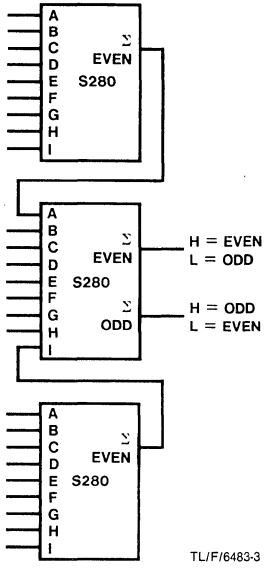


FIGURE 1. 25-Line Parity/Generator Checker

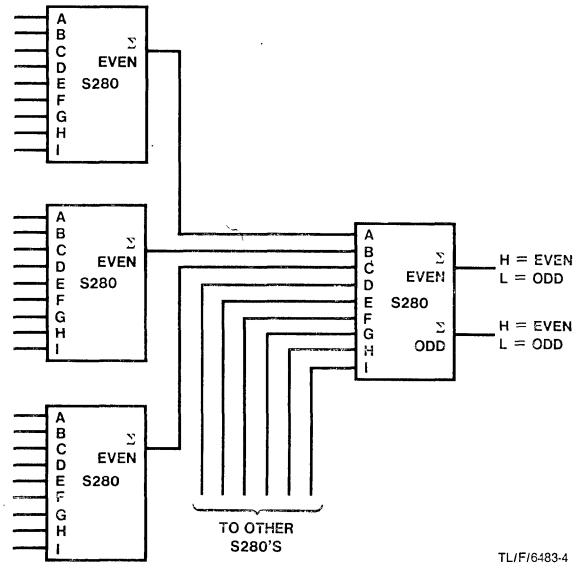


FIGURE 2. 81-Line Parity/Generator Checker

National Semiconductor

DM54S283/DM74S283 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 15 ns
  Two 16-bit words 30 ns
- Typical power dissipation 510 mW

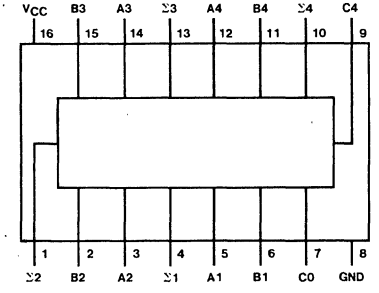
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams and Function Table

Dual-In-Line Package



TL/F/6484-1

54S283(J) **74S283(N)**

Input				Output					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Recommended Operating Conditions

Sym	Parameter	DM54S283			DM74S283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current (Output C4)			−0.5			−0.5	mA
	High Level Output Current (Other Outputs)			−1			−1	
I_{OL}	Low Level Output Current (Output C4)			10			10	mA
	Low Level Output Current (Other Outputs)			20			20	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	C4 Output	−20		−100	mA
			Other Outputs	−40		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			80	120	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			95	160	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs at 4.5V.

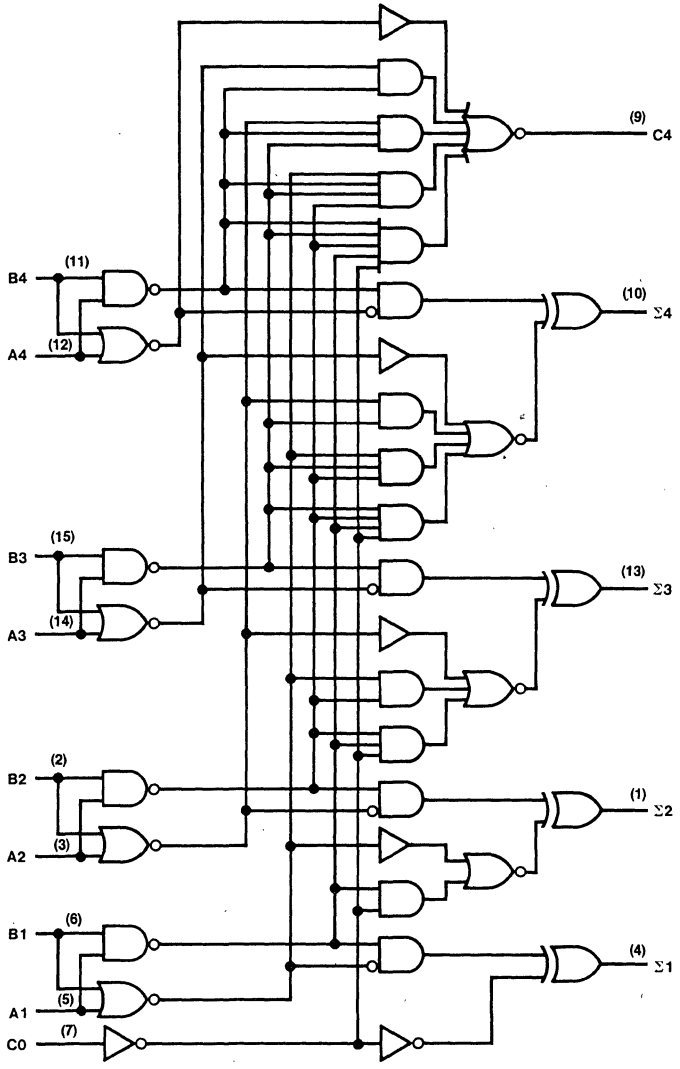
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ1 or Σ2		11	18		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ1 or Σ2		12	18		14	20	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ3		11	18		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ3		12	18		14	20	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ4		11	18		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ4		12	18		14	20	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A_i, B_i to S_i		11	18		14	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A_i, B_i to S_i		12	18		14	20	ns
t_{PLH} Propagation Delay Time Low to High Level Output (Note 1)	C0 to Σ4		6	11		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Note 1)	C0 to Σ4		7.5	11		12	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output (Note 1)	A_i, B_i to C4		7.5	12		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Note 1)	A_i, B_i to C4		8.5	12		13	16	ns

Note 1: $R_L = 560\Omega$.

Logic Diagram

S283



TL/F/6484-2

National Semiconductor

DM54S299/DM74S299
TRI-STATE® 8-Bit Universal Shift/Storage Registers

Description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Features

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Left
  - Shift Right
  - Load Data
- TRI-STATE Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Operates with Outputs Enabled or at High Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

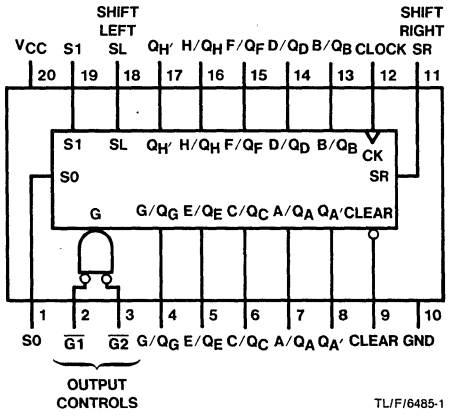
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54S299 (J) **74S299 (N)**

Function Table

Mode	Inputs							Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR									
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

$Q_{A0}...Q_{H0}$ = The output logic level of Q_X before the indicated input conditions were established.

H = high logic level, L = low logic level, x = either low or high logic level

$Q_{AN}...Q_{HN}$ = The output logic level before the active transition (↑) of the clock input.

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S299			DM74S299			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current (Q_A thru Q_H)				−2			−6.5	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				−0.5			−0.5	
I_{OL}	Low Level Output Current (Q_A thru Q_H)				20			20	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				6			6	
f_{CLK}	Clock Frequency (Note 2)		0	70	50	0	70	50	MHz
f_{CLK}	Clock Frequency (Note 3)		0	60	40	0	60	40	MHz
t_W	Pulse Width	Clock High	10			10			ns
		Clock Low	10			10			
		Clear Low	10			10			
t_{SU}	Setup Time (Note 4)	Select	15↑			15↑			ns
		Data High	7↑			7↑			
		Data Low	5↑			5↑			
t_H	Hold Time (Note 4)		5↑			5↑			ns
t_{REL}	Clear Release Time		10↑			10↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.
Note 4: Data includes the two serial inputs and the eight input/output data lines.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	Q_A thru Q_H	2.4	3.2		V
			Q_A', Q_H'	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A thru H, S0, S1			100	μA
			Any Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Clock, Clear			−2	mA
			Other			−0.25	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied Q_A thru Q_H	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				100	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied Q_A thru Q_H	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−250	μA
I_{OS}	Short Circuit Output Current (Q_A thru Q_H)	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
	Short Circuit Output Current (Q_A', Q_H')	V_{CC} = Max (Note 2)	DM54	−20		−100	
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			140	225	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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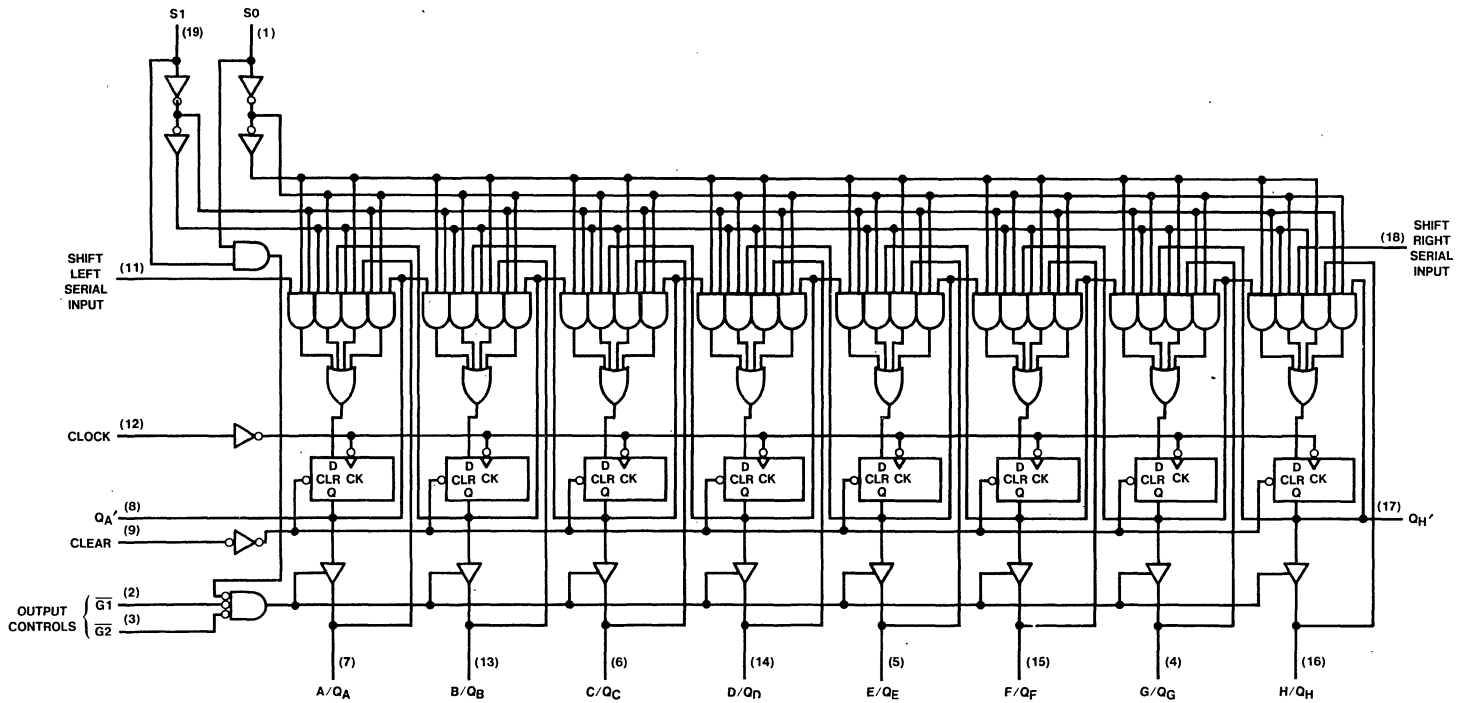
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$ (Note 2)						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	(Note 3)	50	70		40	60		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to $Q_{A'}$ or $Q_{H'}$		12	20		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to $Q_{A'}$ or $Q_{H'}$		13	20		19	29	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to $Q_{A'}$ thru $Q_{H'}$		15	21		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to $Q_{A'}$ thru $Q_{H'}$		15	21		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to $Q_{A'}$ or $Q_{H'}$		14	21		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q_A thru Q_H		16	24		19	29	ns
t_{PZH} Output Enable Time to High Level Output	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		10	18		13	20	ns
t_{PZL} Output Enable Time to Low Level Output	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		12	18		16	24	ns
t_{PHZ} Output Disable Time to High Level Output (Note 1)	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		7	12				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		7	12				ns

Note 1: $C_L = 5$ pF.
Note 2: $R_L = 1$ KΩ for delays measured to $Q_{A'}$ and $Q_{H'}$.
Note 3: For testing f_{MAX} all outputs are loaded simultaneously.

Logic Diagram



TL/F/6485-2

National Semiconductor

DM54S373/DM74S373, DM54S374/DM74S374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

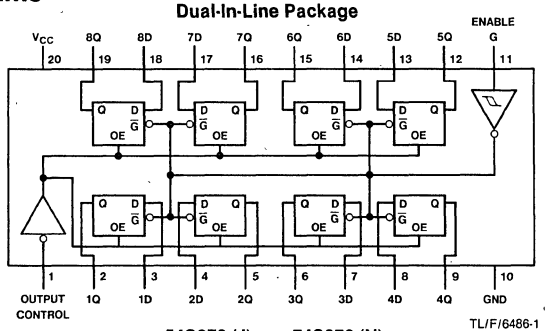
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- TRI-STATE Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

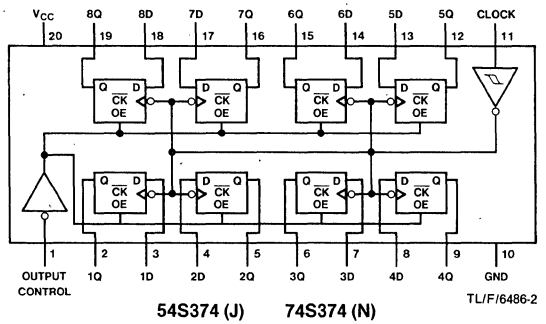
Connection Diagrams

Dual-In-Line Package



54S373 (J) 74S373 (N)

Dual-In-Line Package



54S374 (J) 74S374 (N)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Function Tables

DM54/74S373
Truth Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

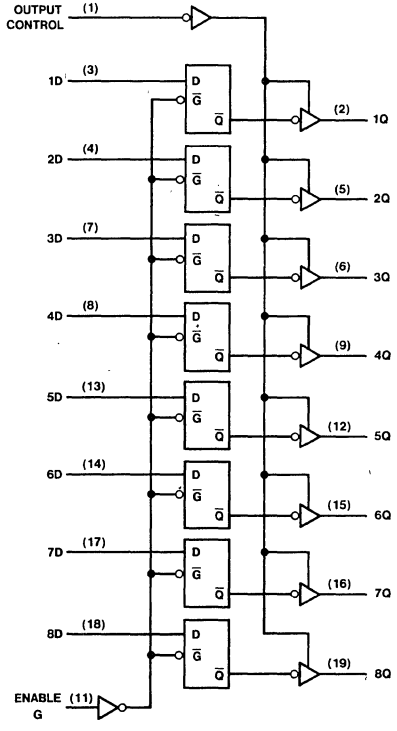
DM54/74S374
Truth Table

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

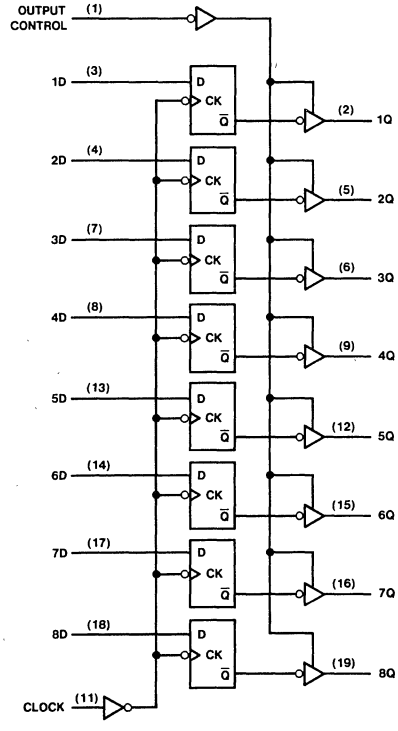
Logic Diagram

DM54/74S373
Transparent Latches



TL/F/6486-3

DM54/74S374
Positive-Edge-Triggered Flip-Flops



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'S373 Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S373			DM74S373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−6.5	mA
I_{OL}	Low Level Output Current				20			20	mA
t_W	Pulse Width (Note 2)	Enable High	6			6			ns
		Enable Low	7.3			7.3			
	Pulse Width (Note 3)	Enable High	15			15			
		Enable Low	15			15			
t_{SU}	Data Setup Time (Note 1)		0↓			0↓			ns
t_H	Data Hold Time (Note 1)		10↓			10↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

'S373 Electrical Characteristics over recommended operating free air temperature

(unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			105	160	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'S373 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		5	9		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		9	13		11	17	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Any Q		7	14		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Any Q		12	18		14	21	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Any Q		8	15		11	17	ns

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Switching Characteristics (Continued) at $V_{CC} = 5V$ and $T_A = 25°C$

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PZL} Output Enable Time to Low Level Output	Output Control to Any Q		11	18		15	23	ns
t_{PHZ} Output Disable Time to High Level Output (Note 1)	Output Control to Any Q		6	9				ns
t_{PLZ} Output Disable Time to Low Level Output (Note 1)	Output Control to Any Q		8	12				ns

Note 1: $C_L = 5$ pF.

'S374 Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S374			DM74S374			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−6.5	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	100	75	0	100	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	100	75	0	100	75	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
	Pulse Width (Note 3)	Clock High	15			15			
		Clock Low	15			15			
t_{SU}	Data Setup Time (Note 1)		5↑			5↑			ns
t_H	Data Hold Time (Note 1)		2↑			2↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.
Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

'S374 Electrical Characteristics over recommended operating free air temperature

(unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				250	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			90	140	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

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'S374 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency			75	100		75	100	MHz
t_{PLH} Propagation delay time Low to High Level Output	Clock to Any Q		8	15		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		11	17		13	20	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Any Q		8	15		11	17	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Any Q		11	18		15	23	ns
t_{PHZ} Output Disable Time from High Level Output (Note 1)	Output Control to Any Q		5	9				ns
t_{PLZ} Output Disable Time from Low Level Output (Note 1)	Output Control to Any Q		7	12				ns

Note 1: $C_L = 5$ pF.

National Semiconductor

DM54S381/DM74S381
Arithmetic Logic Unit/Function Generator

General Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package. The method of cascading 54S182/74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the 'S182. The typical addition times shown illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

Features

- A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-Inch Row Spacing
- Ideally Suited for High-Density Economical Processors
- Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility
- Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:
  - A Minus B
  - B Minus A
  - A Plus B
  - and Five Other Functions
- Schottky-Clamped for High Performance
  - 16-Bit Add Time...26 ns Typ Using Look-Ahead
  - 32-Bit Add Time...34 ns Typ Using Look-Ahead

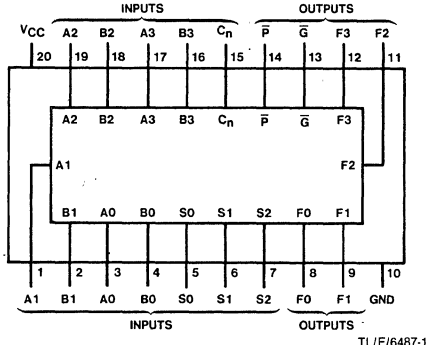
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6487-1

54S381 (J) **74S381 (N)**

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$	14	INVERTED CARRY PROPAGATE OUTPUT
$\overline{G}$	13	INVERTED CARRY GENERATE OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

Function Table

Selection			Arithmetic/Logic Operation
S2	S1	S0	
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

Recommended Operating Conditions

Symbol	Parameter	DM54S381			DM74S381			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Any S			50	μA
			Cn			250	
			Any Other			200	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Any S			−2	mA
			Cn			−8	
			Any Other			−6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			105	160	mA

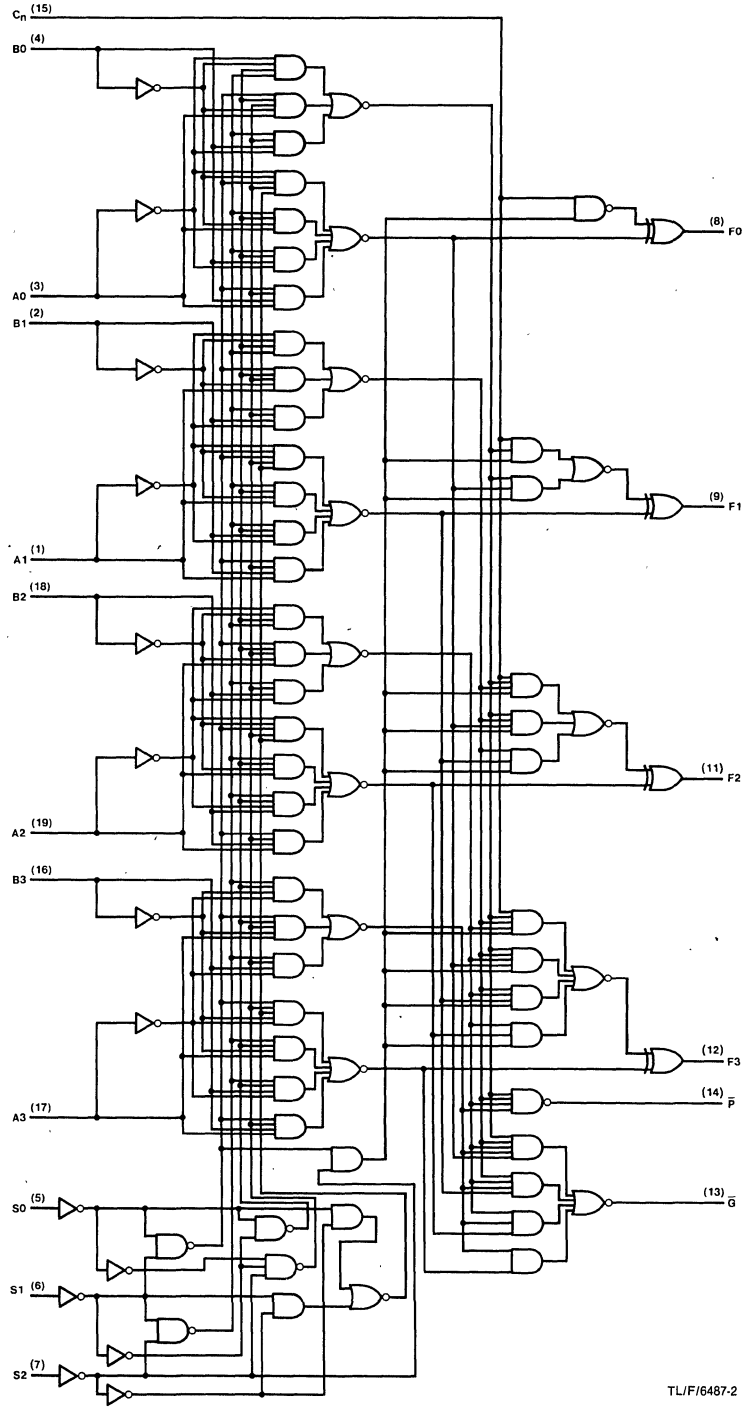
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Cn to Any F		10	17		12	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Cn to Any F		10	17		12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to $\overline{G}$		12	20		14	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to $\overline{G}$		12	20		14	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to $\overline{P}$		11	18		13	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to $\overline{P}$		11	18		13	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A_i or B_i to F_i		18	27		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A_i or B_i to F_i		16	25		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	S to Any		18	30		20	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	S to Any		18	30		20	33	ns

Logic Diagram



TL/F/6487-2

National Semiconductor

DM54S940/DM74S940, DM54S941/DM74S941 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133 Ω.

- Typical propagation delay times
  - Inverting 4.5 ns
  - Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
  - Inverting 450 mW
  - Noninverting 538 mW

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54S 48 mA
  - 74S 64 mA
- Typical I_{OH} (source current)
  - 54S − 12 mA
  - 74S − 15 mA

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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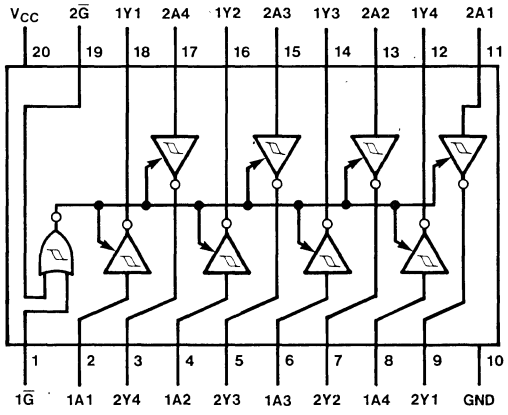
Connection Diagrams

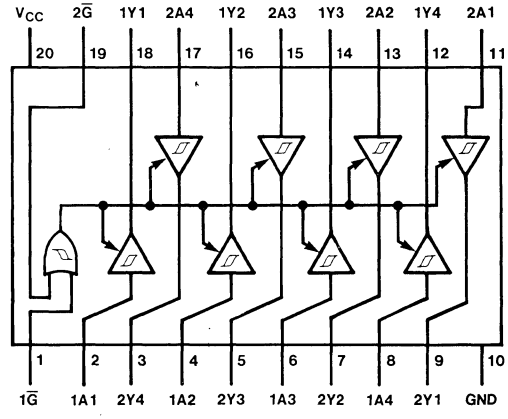
Dual-In-Line Package



TL/F/6488-1

54S940 (J) 74S940 (N)

Dual-In-Line Package



TL/F/6488-2

54S941 (J) 74S941 (N)

Recommended Operating Conditions

Symbol	Parameter	DM54S			DM74S			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	DM74	2.7			V
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = 0.8V, V_{IH} = 2V	DM54			0.55	V
			DM74			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V, V_O = 2.4V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V, V_O = 0.5V				−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Any A			−400	μA
			Any G			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	DM54S940		80	123	mA
			DM74S940		80	135	
			DM54S941		95	147	
			DM74S941		95	160	
		Outputs Low	DM54S940		100	145	
			DM74S940		100	150	
			DM54S941		120	170	
			DM74S941		120	180	
		Outputs Disabled	DM54S940		100	145	
			DM74S940		100	150	
			DM54S941		120	170	
			DM74S941		120	180	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S940	2	4.5	7	ns
			DM54/74S941	2	6	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S940	2	4.5	7	ns
			DM54/74S941	2	6	9	
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S940	3	10	15	ns
			DM54/74S941	3	10	15	
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF, $R_L = 90\Omega$	DM54/74S940	2	6.5	10	ns
			DM54/74S941	3	8	12	
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, $R_L = 90\Omega$	DM54/74S940	4	10	15	ns
			DM54/74S941	2	10	15	
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, $R_L = 90\Omega$	DM54/74S940	2	6	9	ns
			DM54/74S941	2	6	9	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S940	3	7	10	ns
			DM54/74S941	4	9	12	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S940	3	7	10	ns
			DM54/74S941	4	9	12	
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S940	6	14	21	ns
			DM54/74S941	6	14	21	
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF, $R_L = 90\Omega$	DM54/74S940	4	9	12	ns
			DM54/74S941	4	10	15	

Section 6

TTL

6

Section Contents

Section Contents (Continued)

Section Contents (Continued)

National Semiconductor

DM2502/DM2502C, DM2503/DM2503C, DM2504/DM2504C Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary (in combination with a D/A converter) to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

Features

- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

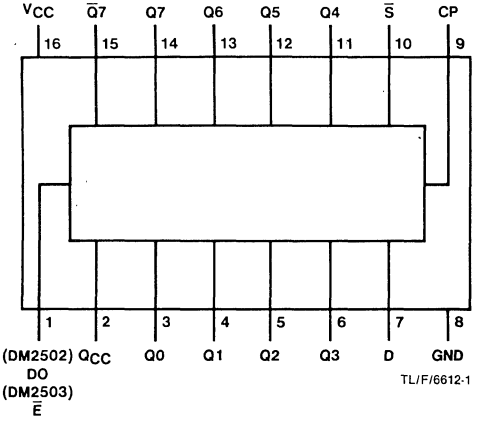
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

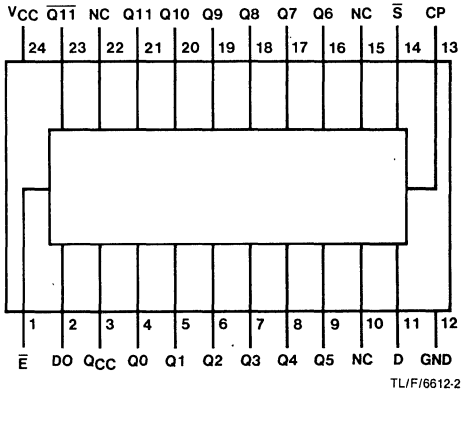
Dual-In-Line Package



TL/F/6612-1

2502 (J) 2502C (N)
2503 (J) 2503C (N)

Dual-In-Line Package



TL/F/6612-2

2504 (J) 2504C (N)

Recommended Operating Conditions

Sym	Parameter		DM2502			DM2502C			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.48	mA
I_{OL}	Low Level Output Current				9.6			9.6	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	Clock Low	42	30		42	30		ns
		Clock High	24	17		24	17		
t_{SU}	Setup Time	$\overline{S}$ Input	16	9		16	9		ns
		D Input	8	4		8	4		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

DM2502 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CP Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CP Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	2502	−10		−45	mA
			2502C	−10		−45	
I_{CC}	Supply Current	V_{CC} = Max	2502		65	85	mA
			2502C		65	95	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

DM2502 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	21		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	CP to Output	10	26	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	CP to Output	10	18	28	ns

Recommended Operating Conditions

Sym	Parameter		DM2503			DM2503C			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.48	mA
I_{OL}	Low Level Output Current				9.6			9.6	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	CP Low	42	30		42	30		ns
		CP High	24	17		24	17		
t_{SU}	Setup Time	$\overline{S}$	16	9		16	9		ns
		D	8	4		8	4		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

DM2503 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CP Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CP Input			− 1.6	mA
			Others			− 3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	2503	− 10		− 45	mA
			2503C	− 10		− 45	
I_{CC}	Supply Current	V_{CC} = Max	2503		60	80	mA
			2503C		60	90	

DM2503 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	21		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	CP to Output	10	26	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	CP to Output	10	18	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output (Note 3)	$\overline{E}$ to Q7		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Note 3)	$\overline{E}$ to Q7		16	24	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: CP = high logic level, $\overline{S}$ = low logic level.

Recommended Operating Conditions

Symbol	Parameter		DM2504			DM2504C			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.48	mA
I_{OL}	Low Level Output Current				9.6			9.6	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	CP Low	42	30		42	30		ns
		CP High	24	17		24	17		
t_{SU}	Setup Time	$\overline{S}$	16	9		16	9		ns
		D	8	4		8	4		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

DM2504 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CP Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CP Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	2504	−10		−45	mA
			2504C	−10		−45	
I_{CC}	Supply Current	V_{CC} = Max	2504		90	110	mA
			2504C		90	124	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.

DM2504 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	21		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	CP to Output	10	26	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	CP to Output	10	18	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output (Note 1)	$\overline{E}$ to Q11		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output (Note 1)	$\overline{E}$ to Q11		16	24	ns

Note 1: CP = high logic level, $\overline{S}$ = low logic level.

Function Table

Time	Inputs			Outputs (1)									
t_n	D	$\overline{S}$	$\overline{E}$ (2)	D0 (3)	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

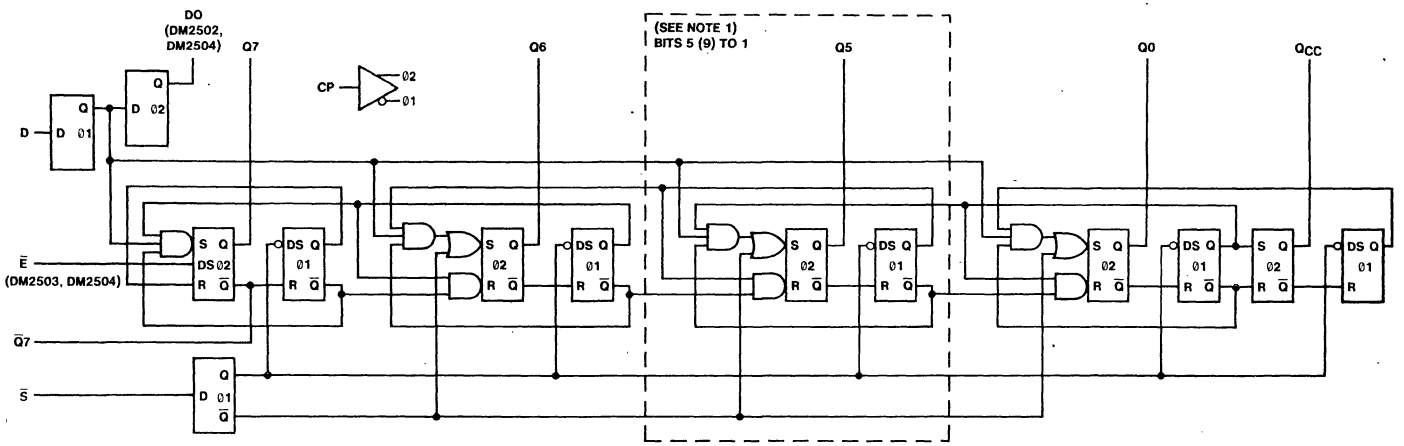
Note 1: Function table for DM2504 is extended to include 12 outputs.

Note 2: Function table for DM2502 does not include $\overline{E}$ column or last line in function table shown.

Note 3: Function table for DM2503 does not include D0 column.

H = High Level
L = Low Level
X = Don't Care
NC = No Change

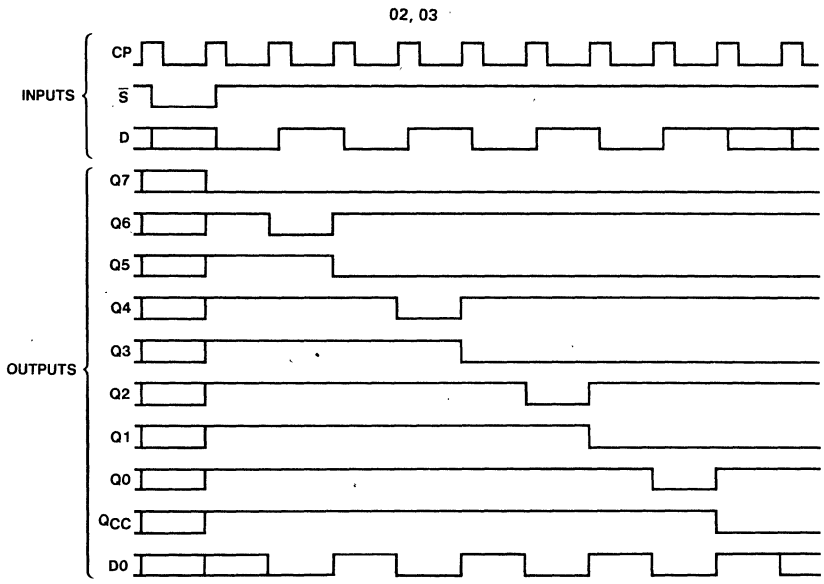
Logic Diagram



Note 1: Cell logic is repeated for register stages.
Q5 to Q1 DM2502, DM2503
Q9 to Q1 DM2504

TL/F/6612-3

Timing Diagram



TL/F/6612-4

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator ½ full range + ½ LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ± ½ LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +½ LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −½ LSB.

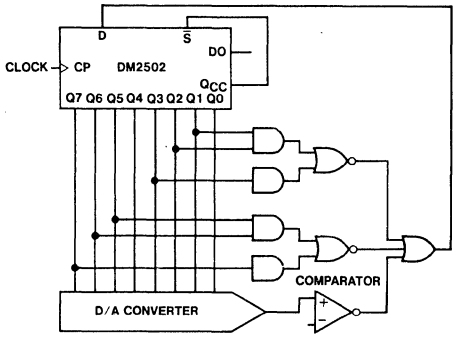
Definition of Terms (See Timing Diagram)

CP: The clock input of the register.
D: The serial data input of the register.
DO: The serial data out. (The D input delayed one bit).
$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).
Q_i i = 7 (11) to 0: The outputs of the register.
Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.
Q7 (11): The true output of the MSB of the register.
$\overline{Q7}$ (11): The complement output of the MSB of the register.
$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Typical Applications

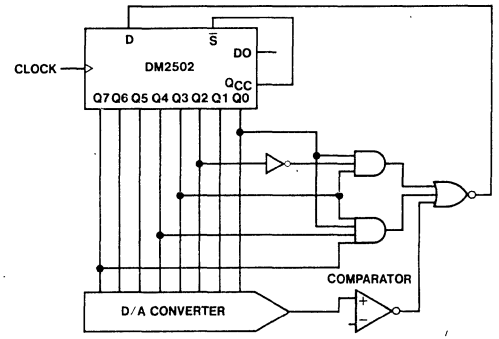
BCD Illegal Code Suppression

Active High



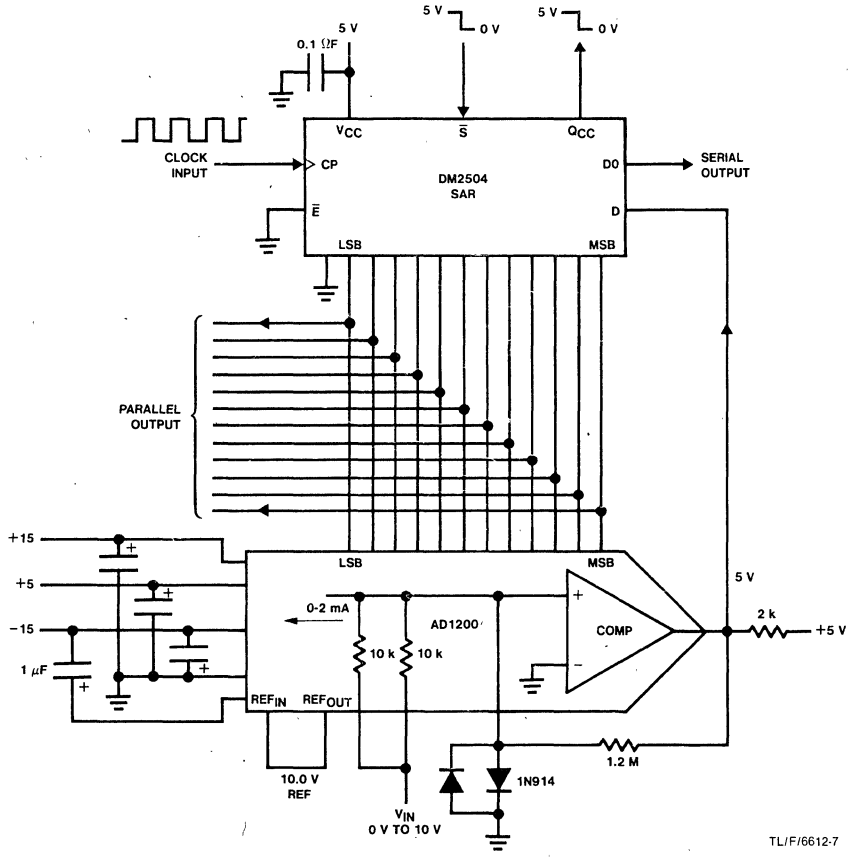
TL/F/6612-5

Active Low



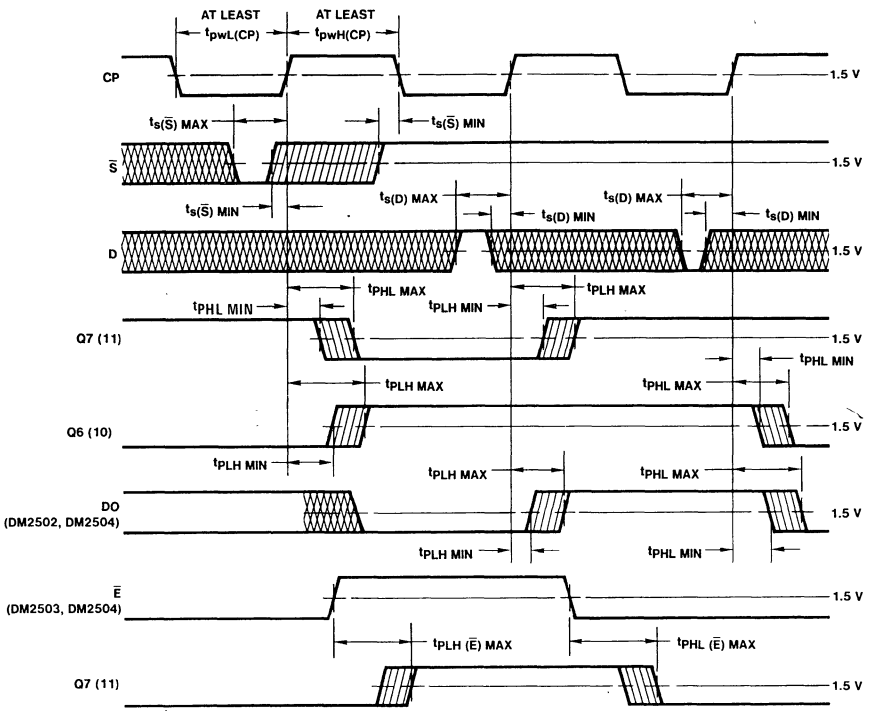
TL/F/6612-6

High Speed 12-BIT A/D Converter



TL/F/6612-7

Switching Time Waveforms



WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care: any change permitted	Changing: state unknown

ENABLE TO Q7 (11)
$\overline{CP}$ = H
$\overline{S}$ = L

TL/F/6612-8

National Semiconductor

DM5400/DM7400 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

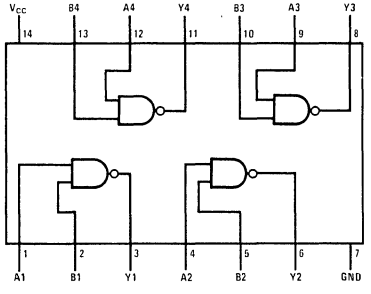
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6613-1

DM5400 (J) DM7400 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5400			DM7400			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			12	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			7	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5401/DM7401 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

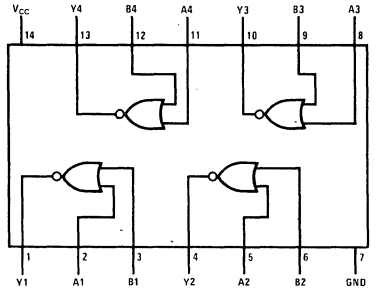
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6614-1

DM5401 (J) DM7401 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5401			DM7401			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5402/DM7402 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

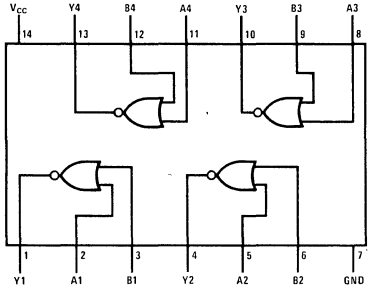
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6492-1

DM5402 (J) DM7402 (N)

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5402			DM7402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			8	16	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			14	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			12	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5403/DM7403 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

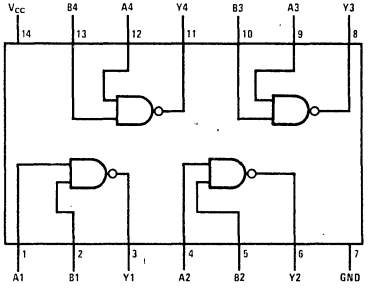
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6493-1

DM5403 (J) DM7403 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5403			DM7403			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5404/DM7404 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

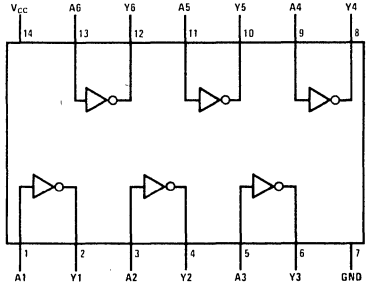
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6494-1

DM5404 (J) DM7404 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5404			DM7404			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			6	12	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			18	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			12	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5405/DM7405 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

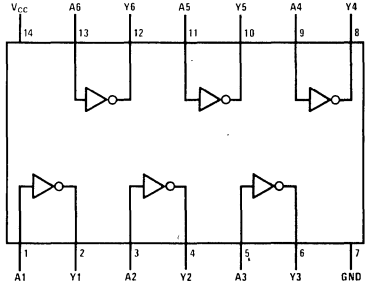
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6495-1

DM5405 (J) DM7405 (N)

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5405			DM7405			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		18	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			40	55	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5406/DM7406 Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent buffers each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

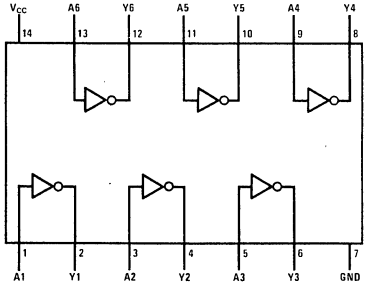
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6496-1

DM5406 (J) DM7406 (N)

Function Table

$Y = \bar{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5406			DM7406			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.7	V
		I_{OL} = 16 mA V_{CC} = Min			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		30	42	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		27	38	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 110Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output			15	23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5407/DM7407 Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

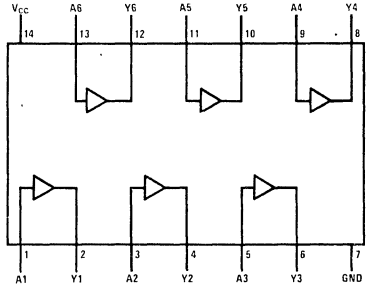
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6497-1

DM5407 (J) DM7407 (N)

Function Table

Y = A

Input	Output
A	Y
L	L
H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5407			DM7407			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA V_{CC} = Min			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		21	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 110Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			6	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output			20	30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5408/DM7408 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

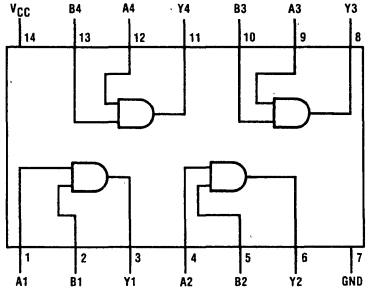
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6498-1

DM5408 (J) **DM7408 (N)**

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5408			DM7408			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			11	21	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			20	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			17	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output			12	19	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5409/DM7409 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

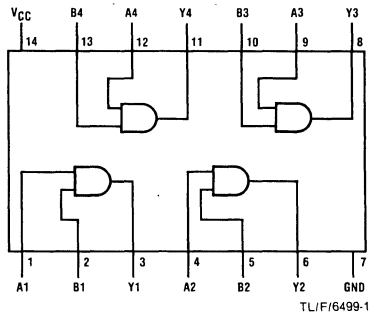
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6499-1

DM5409 (J) **DM7409 (N)**

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM5409			DM7409			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		11	21	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		20	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output			16	24	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5410/DM7410 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

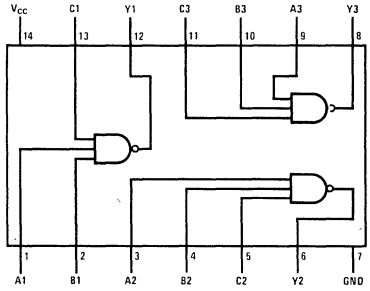
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6500-1

DM5410 (J) DM7410 (N)

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5410			DM7410			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			3	6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			9	16.5	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			11	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			7	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5411/DM7411 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

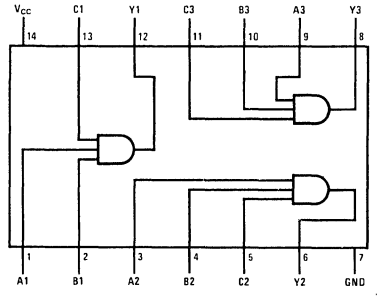
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6501-1

DM5411 (J) DM7411 (N)

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5411			DM7411			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			8	15	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			14	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			17	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output			12	19	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5413/DM7413 Dual 4-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains two independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

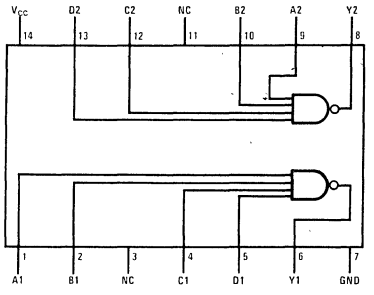
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6502-1

DM5413 (J) **DM7413 (N)**

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5413			DM7413			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-}$ Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_I = V_{T+}$ Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			−0.65		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			−0.85		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			14	23	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			20	32	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$C_L = 15$ pF, $R_L = 400\Omega$			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output			15	22	ns

National Semiconductor

DM5414/DM7414 Hex Inverter with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

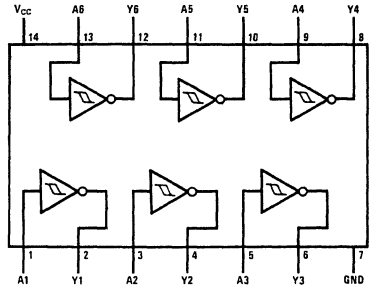
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6503-1

DM5414 (J) DM7414 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5414			DM7414			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-}$ Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_I = V_{T+}$ Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			−0.56		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			22	36	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			39	60	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$C_L = 15$ pF, $R_L = 400\Omega$			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			15	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			15	22	ns

National Semiconductor

DM5416/DM7416 Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

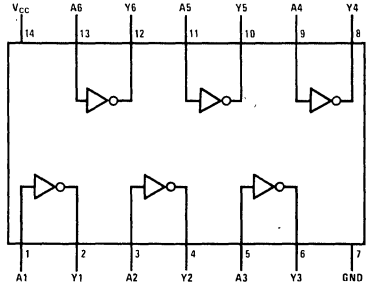
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6504-1

DM5416 (J) DM7416 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5416			DM7416			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 15V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.7	V
		I_{OL} = 16 mA V_{CC} = Min			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		30	42	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		27	38	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 110Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output			15	23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5417/DM7417 Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

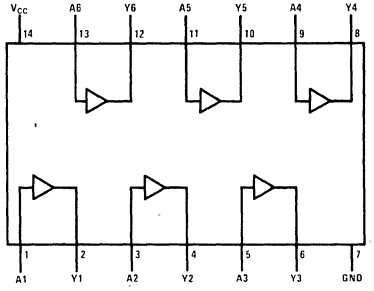
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6505-1

DM5417 (J) **DM7417 (N)**

Function Table

Y = A

Input	Output
A	Y
L	L
H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5417			DM7417			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 15V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA V_{CC} = Min			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		21	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 110Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			6	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output			20	30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5420/DM7420 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

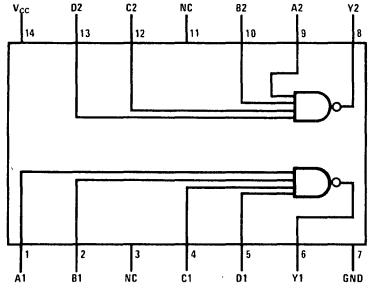
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6506-1

DM5420 (J) DM7420 (N)

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5420			DM7420			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			6	11	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			12	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5425/DM7425 Dual 4-Input NOR Gates with Strobe Input

General Description

This device contains two independent gates each of which performs the logic NOR function. A strobe input is also included which disables the A thru D inputs when low.

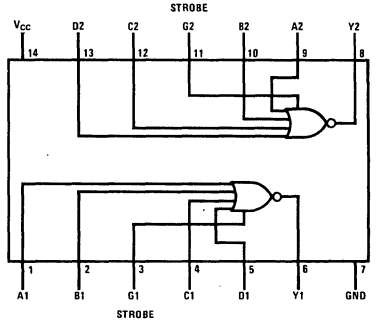
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6507-1

DM5425 (J) **DM7425 (N)**

Function Table

$$Y = \overline{G\,(A + B + C + D)}$$

Inputs					Output
G	A	B	C	D	Y
L	X	X	X	X	H
H	L	L	L	L	H
H	One or more Inputs H				L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5425			DM7425			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Data			40	μA
			Strobe			160	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Data			−1.6	mA
			Strobe			−6.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			8	16	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			10	19	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5426/DM7426 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

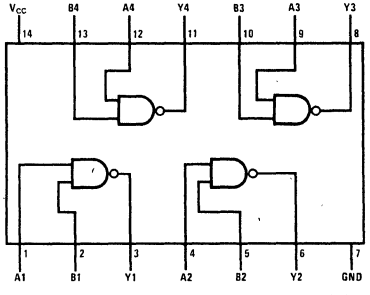
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6508-1

DM5426 (J) DM7426 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5426			DM7426			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{IL} = Max	V_O = 15V			1000	μA
			V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 1 kΩ (t_{PLH})			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output			11	17	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5427/DM7427 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

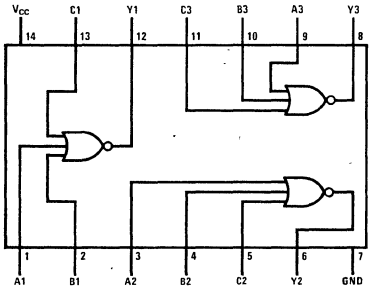
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6509-1

DM5427 (J) DM7427 (N)

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5427			DM7427			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
$-I_I$	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			10	16	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			16	26	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output			10	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5430/DM7430 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

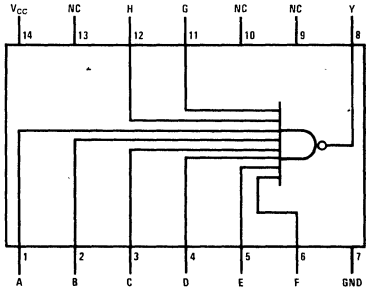
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6510-1

DM5430 (J) DM7430 (N)

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5430			DM7430			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1	2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			3	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5432/DM7432 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

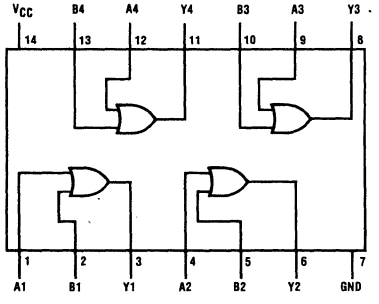
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6511-1

DM5432 (J) DM7432 (N)

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5432			DM7432			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			15	22	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			23	38	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output			14	22	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5437/DM7437 Quad 2-Input NAND Buffers

General Description

This device contains four independent gates each of which performs the logic NAND function.

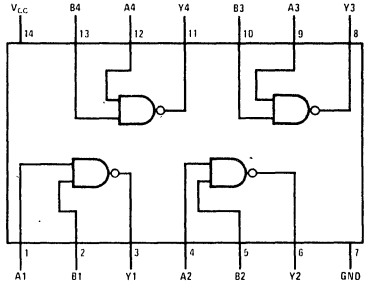
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6512-1

DM5437 (J) **DM7437 (N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5437			DM7437			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			9	15.5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			34	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 45 pF, R_L = 133Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5438/DM7438 Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

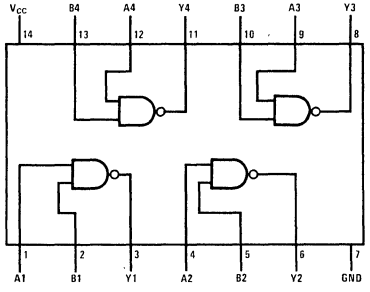
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6513-1

DM5438 (J) **DM7438 (N)**

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5438			DM7438			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		5	8.5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		34	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 45 pF R_L = 133Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			11	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5440/DM7440 Dual 4-Input NAND Buffers

General Description

This device contains two independent gates each of which performs the logic NAND function.

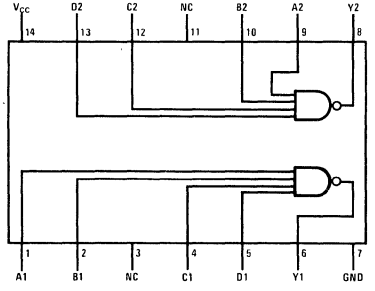
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6514-1

DM5440 (J) DM7440 (N)

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5440			DM7440			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			17	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 133Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5441A/DM7441A BCD to Decimal Decoders/Drivers

General Description

The DM5441A/DM7441A is a BCD-to-decimal decoder designed to drive gas-filled NIXIE tubes. The device is also capable of driving other types of low-current lamps and relays.

An over-range decoding feature provides that if binary numbers between 10 and 15 are applied to the input, the least significant bit (0-5) will be decoded on the output.

Input clamp diodes are also provided to clamp negative-voltage transitions in order to minimize transmission-line effects.

Features

- Drive cold-cathode, numeric indicator tubes directly
- Fully decoded inputs
- Low leakage current 1.8 μA @ 50 V
- Low power dissipation 105 mW typical

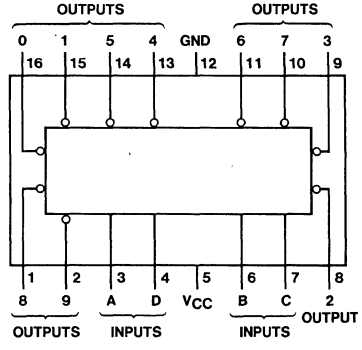
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6515-1

5441A (J) 7441A (N)

Function Table

5441A/7441A

Input				Output On*
D	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(Over Range)				
H	L	H	L	0
H	L	H	H	1
H	H	L	L	2
H	H	L	H	3
H	H	H	L	4
H	H	H	H	5

H = High Level, L = Low Level

*All other outputs are off

Recommended Operating Conditions

Sym	Parameter	DM5441A			DM7441A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OL}	Low Level Output Current			7			7	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

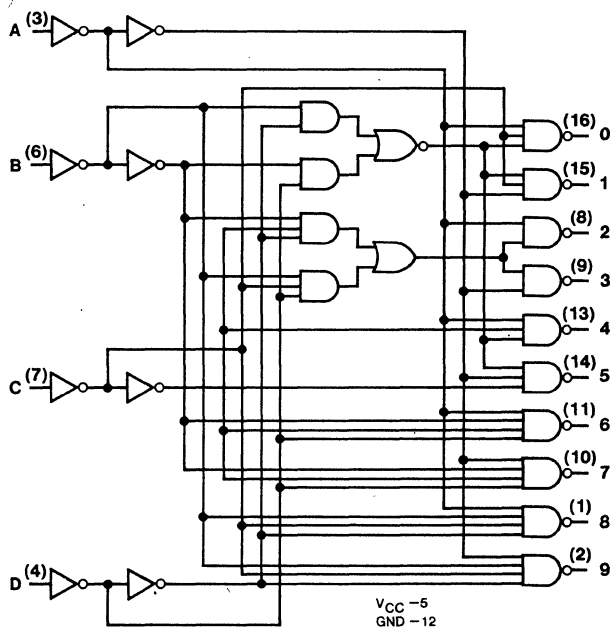
Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 1 mA V_{IL} = Max, V_{IH} = Min		70			V
I_{OH}	Off-State Reverse Current	V_{CC} = Min V_O = 50V	T_A = 125°C			60	μA
			T_A = 70°C			40	
			T_A = −55 to 70°C			1.8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	T_A = −55 to 70°C			2.5	V
			T_A = 125°C			3	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			21	36	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Logic Diagram

5441A/7441A



TL/F/6515-2

National Semiconductor

DM5442/DM7442 BCD to Decimal Decoders

General Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 140 mW
- Typical propagation delay 17 ns

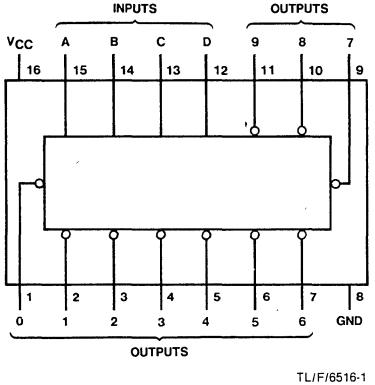
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

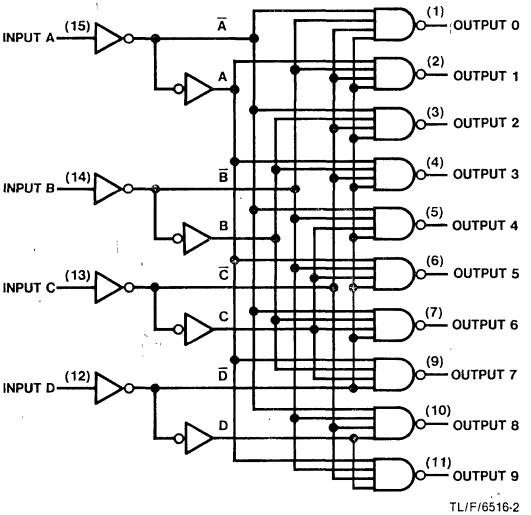
Dual-In-Line Package



TL/F/6516-1

5442 (J) 7442 (N)

Logic Diagram



TL/F/6516-2

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

6

Recommended Operating Conditions

Sym	Parameter	DM5442			DM7442			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		28	41	mA
			DM74		28	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$C_L = 15$ pF, $R_L = 400\Omega$			Units
		Min	Typ	Max	
t_{PHL} Propagation Delay Time High to Low Level Output From A, B, C or D Through 2 Levels of Logic			14	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output From A, B, C, or D Through 3 Levels of Logic			17	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output From A, B, C or D Through 2 Levels of Logic			10	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output From A, B, C or D Through 3 Levels of Logic			17	30	ns

National Semiconductor

DM5445/DM7445 BCD to Decimal Decoders/Drivers

General Description

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

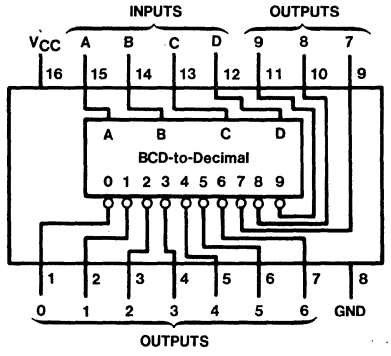
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6517-1

5445 (J) 7445 (N)

Function Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level (Off), L = Low Level (On)

Recommended Operating Conditions

Sym	Parameter	DM5445			DM7445			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
		I_{OL} = 80 mA V_{CC} = Min			0.5	0.9	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		43	62	mA
			DM74		43	70	

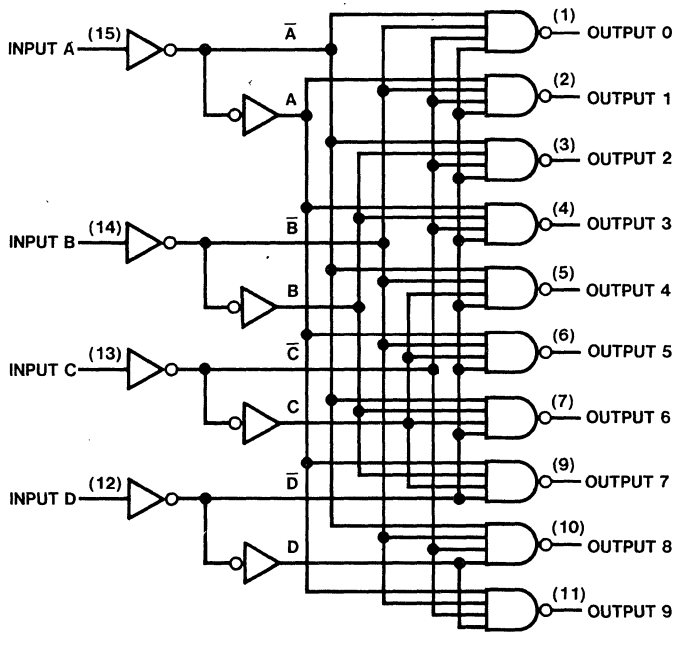
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 100Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output				30	ns
t_{PHL} Propagation Delay Time High to Low Level Output				30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

Logic Diagram



TL/F/6517-2

National Semiconductor

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448 BCD to 7-Segment Decoders/Drivers

General Description

The 46A and 47A feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly; and the 48 features active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

All of the circuits incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability

5446A/7446A, 5447A/7447A

- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

5448/7448

- Internal pull-ups eliminate need for external resistors
- Lamp-test provision
- Leading/trailing zero suppression

Absolute Maximum Ratings (Note 1)

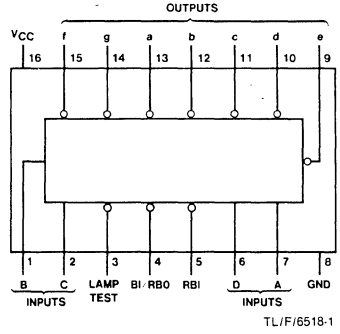
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Type	Driver Outputs				Typical Power Dissipation	Packages
	Active Level	Output Configuration	Sink Current	Max Voltage		
DM5446A	low	open-collector	40 mA	30 V	320 mW	J
DM5447A	low	open-collector	40 mA	15 V	320 mW	J
DM5448	high	2 kΩ pull-up	6.4 mA	5.5 V	265 mW	J
DM7446A	low	open-collector	40 mA	30 V	320 mW	N
DM7447A	low	open-collector	40 mA	15 V	320 mW	N
DM7448	high	2 kΩ pull-up	6.4 mA	5.5 V	265 mW	N

Connection Diagrams

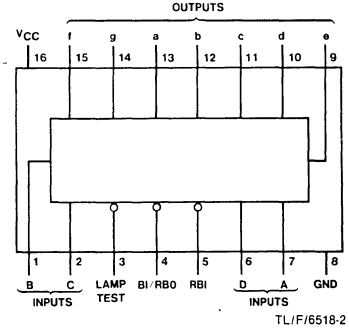
Dual-In-Line Package



TL/F/6518-1

5446A (J) 7446A (N)
5447A (J) 7447A (N)

Dual-In-Line Package



TL/F/6518-2

5448 (J) 7448 (N)

Recommended Operating Conditions

Sym	Parameter	DM5446A			DM7446A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			30			30	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'46A Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min (BI/RBO) I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 30V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current@Max. Input Voltage	V_{CC} = Max, V_I = 5.5V (Except BI/RBO)				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V (Except BI/RBO)				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		60	85	mA
			DM74		60	103	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'46A Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$C_L = 15$ pF, $R_L = 120\Omega$			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output				100	ns
t_{PHL} Propagation Delay Time High to Low Level Output				100	ns

Recommended Operating Conditions

Sym	Parameter	DM5447A			DM7447A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'47A Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min (BI/RBO) I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 15V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		60	85	mA
			DM74		60	103	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'47A Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 120Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output				100	ns
t_{PHL} Propagation Delay Time High to Low Level Output				100	ns

Recommended Operating Conditions

Sym	Parameter	DM5448			DM7448			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			5.5			5.5	V
I_{OH}	High Level Output Current (a thru g)			−0.4			−0.4	μA
	High Level Output Current (BI/RBO)			−0.2			−0.2	
I_{OL}	Low Level Output Current (a thru g)			6.4			6.4	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'48 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min (a thru g), I_{OH} = Max		2.4	4.2		V
		V_{CC} = Min (BI/RBO), I_{OH} = Max		2.4	3.7		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.27	0.4	V
$I_{O(OFF)}$	Off State Output Current (a thru g)	V_{CC} = Max, V_{IH} = Min V_{IL} = Max, V_O = 0.85V		−1.3	2		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V (Except BI/RBO)				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V (Except BI/RBO)				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)	DM54			−4	mA
			DM74			−4	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		50	76	mA
			DM74		50	90	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'48 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$C_L = 15$ pF, $R_L = 1k\Omega$			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output				100	ns
t_{PHL} Propagation Delay Time High to Low Level Output				100	ns

Function Tables

46A, 47A

Decimal or Function	Inputs						BI/RBO(1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(3)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(4)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(5)

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Decimal or Function	Inputs						BI/RBO(1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	(2)
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	(3)
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	(4)
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	(5)

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 2: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

Note 3: When a low logic level is applied directly to the blanking input (BI), all segment outputs are H (46, 47); L (48) regardless of the level of any other input.

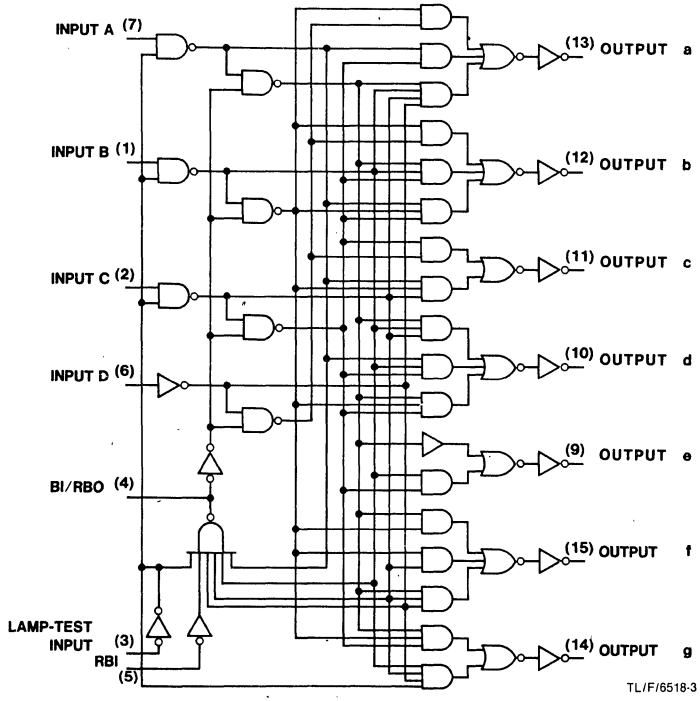
Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

H = High level, L = Low level, X = Don't Care

Logic Diagrams

46A, 47A



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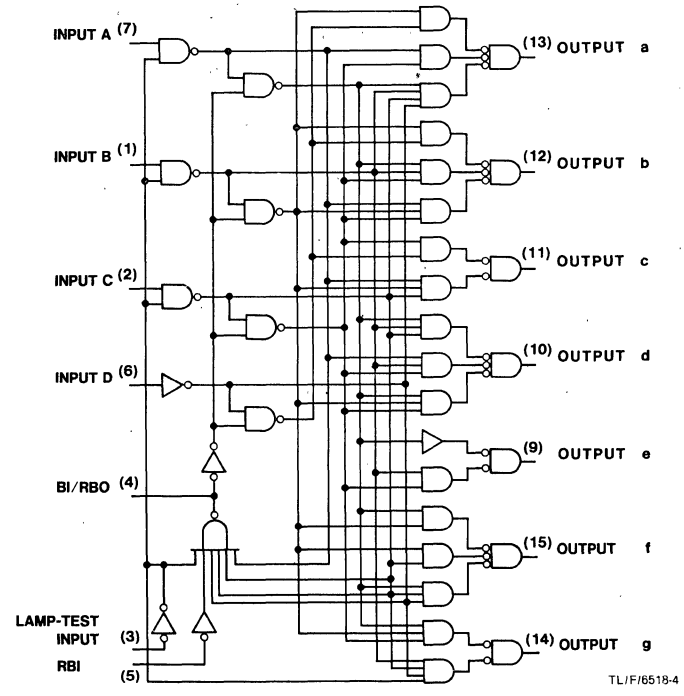


TL/F/6518-4

National Semiconductor

DM5450/DM7450 Dual Expandable 2-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains two combinations of gates each of which performs the logic AND-OR-INVERT function. The logic can be expanded by using the DM54/7460. Up to four DM54/7460's can be used

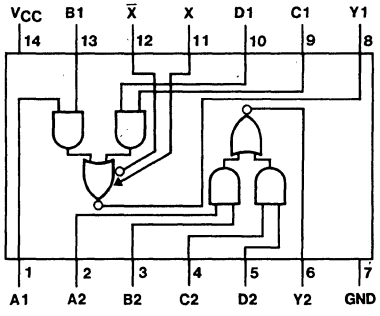
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6519-1

DM5450 (J) DM7450 (N)

Function Table

$$Y = \overline{AB + CD + X}$$

Inputs					Output
A	B	C	D	X	Y
H	H	Y	Y	Y	L
Y	Y	H	H	Y	L
Y	Y	Y	Y	H	L
Other Combinations					H

X = Output of 54/7460
H = High Logic Level
L = Low Logic Level
Y = Either Low or High Logic Level

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Recommended Operating Conditions

Sym	Parameter	DM5450			DM7450			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
		I_X = 150 μA $I_{\overline{X}}$ = −150 μA I_{OH} = Max	DM54	2.4	3.4		
		I_X = 270 μA $I_{\overline{X}}$ = −270 μA I_{OH} = Max	DM74	2.4	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
		$I_X + I_{\overline{X}}$ = 300 μA $R_{X\overline{X}}$ = 138Ω I_{OL} = Max	DM54		0.2	0.4	
		$I_X + I_{\overline{X}}$ = 430 μA $R_{X\overline{X}}$ = 130Ω I_{OL} = Max	DM74		0.2	0.4	
V_{BEQ}	Base-Emitter Voltage of Output Transistor Q	$I_X + I_{\overline{X}}$ = 410 μA $R_{X\overline{X}}$ = 0 I_{OL} = 16 mA	DM54			1.1	V
		$I_X + I_{\overline{X}}$ = 620 μA $R_{X\overline{X}}$ = 0 I_{OL} = 16 mA	DM74			1	
$I_{\overline{X}}$	Expander Current	$V_{X\overline{X}}$ = 0.4V I_{OL} = 16 mA	DM54			−2.9	mA
			DM74			−3.1	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			7.4	14	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	(Expander Pins Open)		13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	(From Input of 60 Expander)		15	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output			10	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5451/DM7451 Dual 2-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains two combinations of gates each of which performs the logic AND-OR-INVERT function.

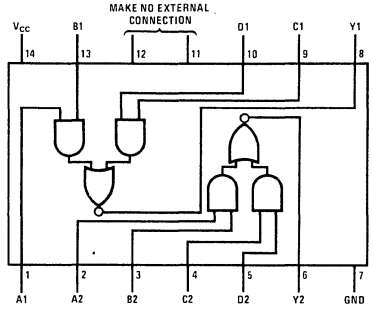
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6520-1

DM5451 (J) DM7451 (N)

Function Table

$$Y = \overline{AB + CD}$$

Inputs				Output
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All Other Combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5451			DM7451			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			7.4	14	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5453/DM7453 Expandable 4-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

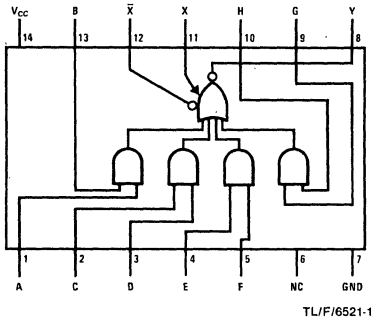
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6521-1

DM5453 (J) DM7453 (N)

Function Table

$$Y = \overline{AB + CD + EF + GH + X}$$

Inputs									Output
A	B	C	D	E	F	G	H	X	Y
H	H	Y	Y	Y	Y	Y	Y	Y	L
Y	Y	H	H	Y	Y	Y	Y	Y	L
Y	Y	Y	Y	H	H	Y	Y	Y	L
Y	Y	Y	Y	Y	Y	H	H	Y	L
Y	Y	Y	Y	Y	Y	Y	Y	H	L
All Other Combinations									H

H = High Logic Level

L = Low Logic Level

Y = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5453			DM7453			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
		I_X = 150 μA $I_{\overline{X}}$ = −150 μA I_{OH} = Max	DM54	2.4	3.4		
		I_X = 270 μA $I_{\overline{X}}$ = −270 μA I_{OH} = Max	DM74	2.4	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
		$I_X + I_{\overline{X}}$ = 300 μA $R_{X\overline{X}}$ = 138Ω I_{OL} = Max	DM54		0.2	0.4	
		$I_X + I_{\overline{X}}$ = 430 μA $R_{X\overline{X}}$ = 130Ω I_{OL} = Max	DM74		0.2	0.4	
V_{BEQ}	Base-Emitter Voltage of Output Transistor Q	$I_X + I_{\overline{X}}$ = 410 μA $R_{X\overline{X}}$ = 0 I_{OL} = 16 mA	DM54			1.1	V
		$I_X + I_{\overline{X}}$ = 620 μA $R_{X\overline{X}}$ = 0 I_{OL} = 16 mA	DM74			1	
$I_{\overline{X}}$	Expander Current	$V_{X\overline{X}}$ = 0.4V I_{OL} = 16 mA	DM54			−2.9	mA
			DM74			−3.1	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Parameter		Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			5.1	9.5	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	(Expander Pins Open)		13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5454/DM7454 4-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

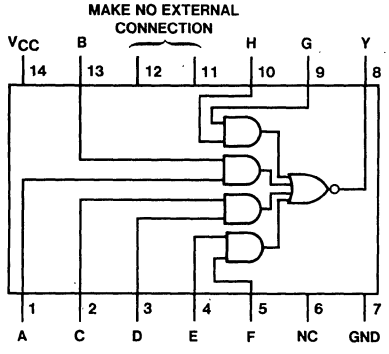
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6522-1

DM5454 (J) DM7454 (N)

Function Table

$$Y = \overline{AB + CD + EF + GH}$$

Inputs								Output
A	B	C	D	E	F	G	H	Y
H	H	X	X	X	X	X	X	L
X	X	H	H	X	X	X	X	L
X	X	X	X	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All Other Combinations								H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM5454			DM7454			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			5.1	9.5	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			13	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output			8	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5470/DM7470 AND-Gated Positive-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs

General Description

This device is a positive-edge-triggered J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. If the $\overline{J}$ and $\overline{K}$ inputs are not used they must be grounded for proper operation of the flip-flop. The J and K data is accepted by the flip-flop on the positive going edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the positive going edge of the clock pulse. The clear and preset inputs are asynchronous but it is necessary that the clock input be at a low level when they become active (low).

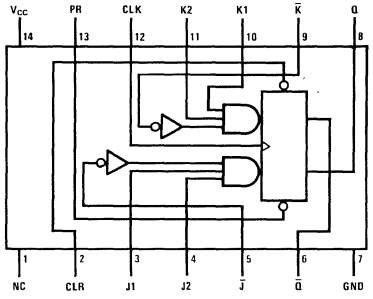
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6523-1

DM5470 (J) DM7470 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	Q_O	$\overline{Q}_O$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	Toggle	
H	H	L	X	X	Q_O	$\overline{Q}_O$

Note 1: $J = (J1)(J2)(\overline{J})$, $K = (K1)(K2)(\overline{K})$ if the $\overline{J}$ and $\overline{K}$ inputs are not used they must be grounded.

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↑ = Positive Going Transition

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each positive transition of the clock.

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Recommended Operating Conditions

Sym	Parameter		DM5470			DM7470			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	30			30			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		20↑			20↑			ns
t_H	Input Hold Time (Note 1)		5↑			5↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K, or $\overline{K}$			40	μA
			Clock			40	
			Clear			80	
			Preset			80	

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 5)	J, K, or $\overline{K}$			−1.6	mA
			Clock			−1.6	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			13	26	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	35		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$			50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q			50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q			50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$			50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$			50	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is at 4.5V.

Note 5: Clear is tested with preset high and preset is tested with clear high.

National Semiconductor

DM5472/DM7472 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear, and Complementary Outputs

General Description

This device is a positive pulse triggered J-K master-slave flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the J and K inputs must not be allowed to change while the clock is in the high state. Data is transferred to the output on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

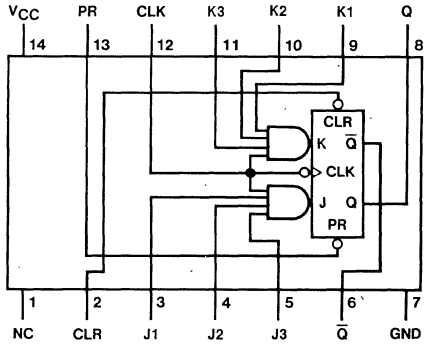
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6524-1

DM5472 (J) DM7472 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\overline{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

Note 1: J = (J1)(J2)(J3), K = (K1)(K2)(K3)

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each positive clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM5472			DM7472			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge (↓) for falling edge.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
			Preset			80	

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Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 5)	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9	17	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		16	25	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: Clear is tested with preset high and preset is tested with clear high.

National Semiconductor

DM5473/DM7473 Dual Master-Slave J-K Flip-Flops with Clear, and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data transfers to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

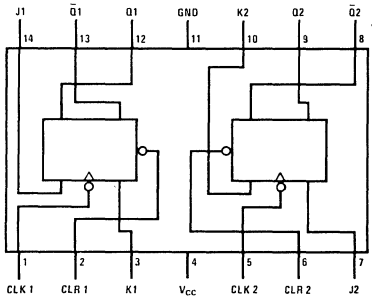
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6525-1

DM5473 (J) DM7473 (N)

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_O	$\overline{Q}_O$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each high level clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM5473			DM7473			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	47			47			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			18	34	mA

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		16	25	ns

National Semiconductor

DM5474/DM7474 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

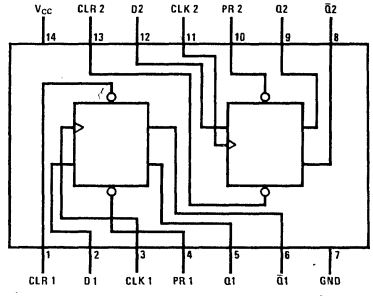
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6526-1

DM5474 (J) DM7474 (N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition of the clock.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

Recommended Operating Conditions

Sym	Parameter		DM5474			DM7474			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock High	30			30			ns
		Clock Low	37			37			
		Clear Low	30			30			
		Preset Low	30			30			
t_{SU}	Input Setup Time (Note 1)		20↑			20↑			ns
t_H	Input Hold Time (Note 1)		5↑			5↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			40	μA
			Clock			80	
			Clear			120	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 4)	D			− 1.6	mA
			Clock			− 3.2	
			Clear			− 3.2	
			Preset			− 1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	− 20		− 55	mA
			DM74	− 18		− 55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			17	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$			40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q			25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q			40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		14	25	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.
Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.
Note 4: Clear is tested with preset high and preset is tested with clear high.

National Semiconductor

DM5475/DM7475 Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch and are available in 16-pin packages.

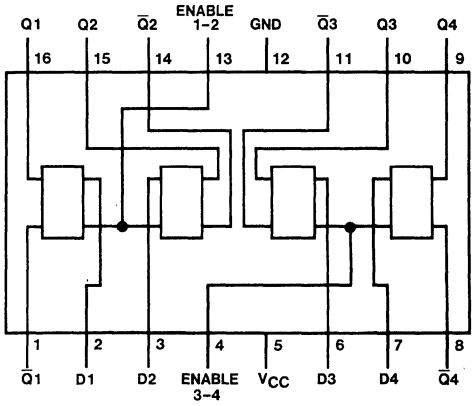
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6527-1

5475 (J) 7475 (N)

Function Table (Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

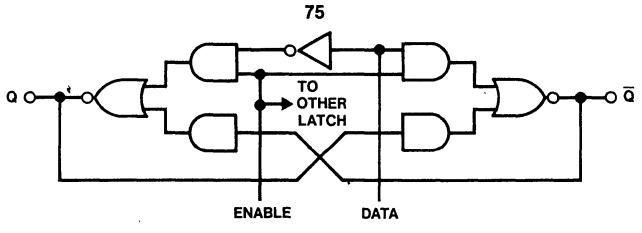
H = High Level

L = Low Level

X = Don't Care

Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)



TL/F/6527-2

Recommended Operating Conditions

Sym	Parameter	DM5475			DM7475			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_W	Enable Pulse Width	20			20			ns
t_{SU}	Setup Time	20			20			ns
t_H	Hold Time	5			5			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		32	46	mA
			DM74		32	50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PHL} Propagation Delay Time High to Low Level Output	D to Q		14	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to Q		16	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		7	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		24	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to Q		7	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to Q		16	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to $\overline{Q}$		7	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to $\overline{Q}$		16	30	ns

National Semiconductor

DM5476/DM7476 Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flip after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

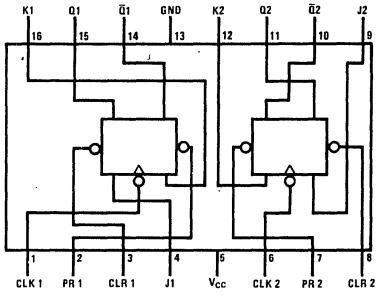
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6528-1

DM5476 (J) **DM7476 (N)**

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\overline{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM5476			DM7476			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
			Preset			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 5)	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			18	34	mA

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: Clear is measured with preset high and preset is measured with clear high.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		16	40	ns

National Semiconductor

DM5483/DM7483 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 23 ns
  Two 16-bit words 43 ns
- Typical power dissipation per 4-bit adder 290 mW

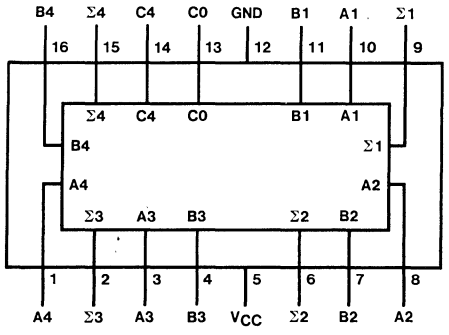
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6529-1

5483 (J) **7483 (N)**

6

Recommended Operating Conditions

Sym	Parameter	DM5483			DM7483			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current (Output C4)			−0.4			−0.4	mA
	High Level Output Current—Other Outputs			−0.8			−0.8	
I_{OL}	Low Level Output Current (Output C4)			8			8	mA
	Low Level Output Current—Other Outputs			16			16	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current (Output C4)	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
	Short Circuit Output Current (Other Outputs)	V_{CC} = Max (Note 2)	DM54	−20		−70	
			DM74	−18		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			58	79	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ1, Σ2		20	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ1, Σ2		22	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ3		22	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ3		28	47	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to Σ4		28	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to Σ4		28	47	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A_i, B_i to Σ_i			33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A_i, B_i to Σ_i			38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to C4		12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to C4		12	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A_i, B_i to C4		12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A_i, B_i to C4		12	19	ns

Function Table

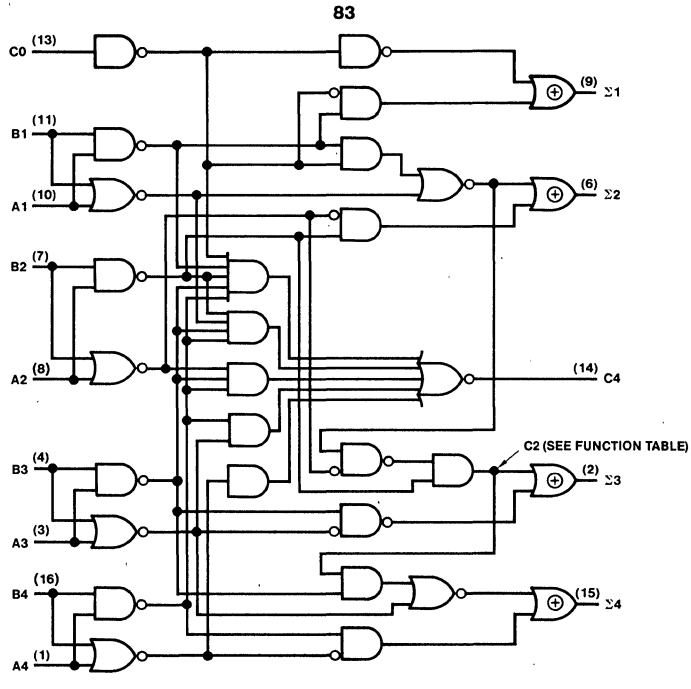
Input				Output					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram



TL/F/6529-2

National Semiconductor

DM5485/DM7485 4-Bit Magnitude Comparators

General Description

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 275 mW
- Typical delay (4-bit words) 23 ns

Absolute Maximum Ratings (Note 1)

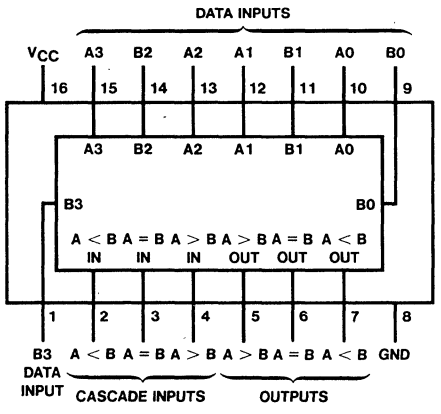
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

6

Connection Diagram

Dual-In-Line Package



TL/F/6530-1

5485 (J) **7485 (N)**

Recommended Operating Conditions

Sym	Parameter	DM5485			DM7485			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A < B			40	μA
			A > B			40	
			Others			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A < B			−1.6	mA
			A > B			−1.6	
			Others			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, A = B input grounded and all other inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

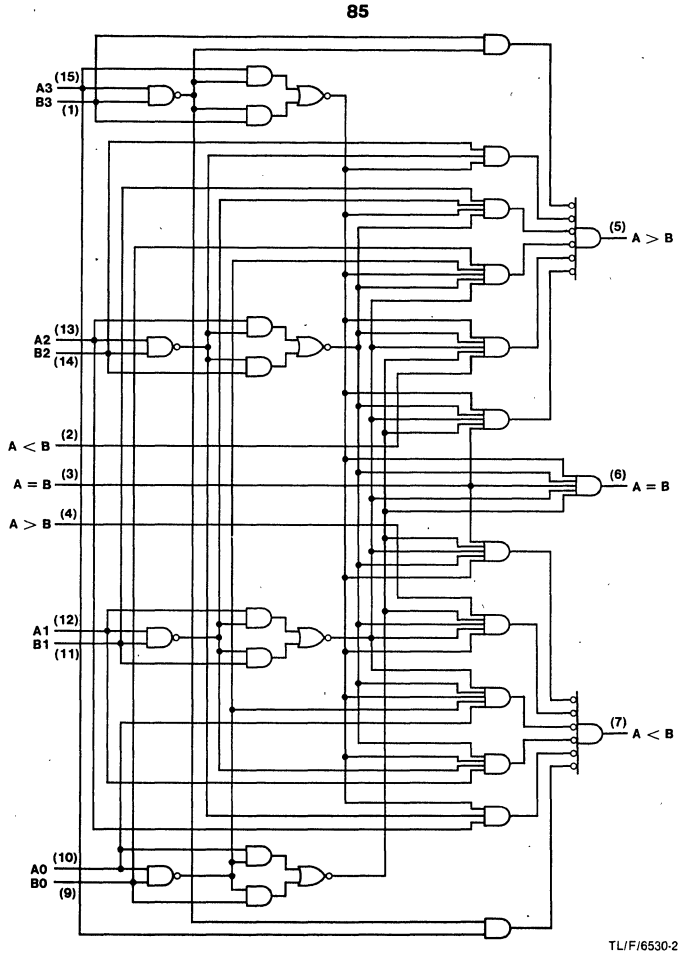
Parameter	From Input	To Output	Number of Gate Levels	$R_L = 400\Omega$, $C_L = 15$ pF			Units
				Min	Typ	Max	
t_{PLH} Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	1		7		ns
			2		12		
			3		17	26	
		A = B	4		23	35	
t_{PHL} Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	1		11		ns
			2		15		
			3		20	30	
		A = B	4		20	30	
t_{PLH} Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		7	11	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		11	17	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		13	20	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		11	17	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		7	11	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		11	17	ns

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



TL/F/6530-2

National Semiconductor

DM5486/DM7486 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

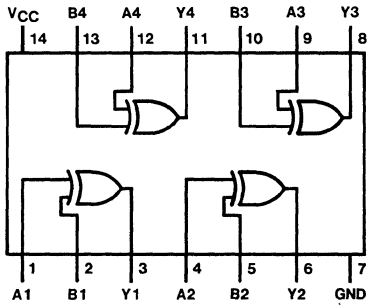
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6531-1

DM5486 (J) DM7486 (N)

Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

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Recommended Operating Conditions

Sym	Parameter	DM5486			DM7486			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)	DM54		30	43	mA
			DM74		30	50	
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			36	57	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open, and all inputs at ground.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output			11	17	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High		18	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output			13	22	ns

National Semiconductor

DM5490A/DM7490A, DM5492A/DM7492A, DM5493A/DM7493A Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, divide-by-six for the 92A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- Typical power dissipation
  - 90A 145 mW
  - 92A, 93A 130 mW
- Count frequency 42 MHz

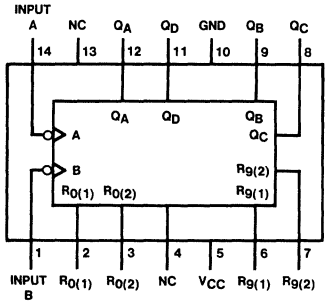
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

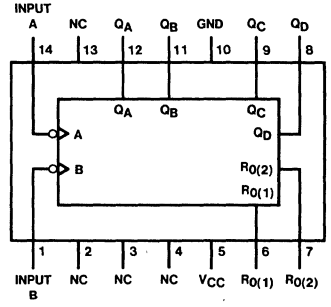
Dual-In-Line Package



TL/F/6533-1

5490A (J) **7490A (N)**

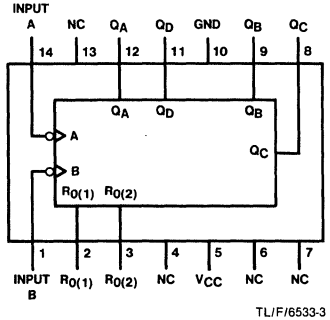
Dual-In-Line Package



TL/F/6533-2

5492A (J) **7492A (N)**

Dual-In-Line Package



TL/F/6533-3

5493A (J) **7493A (N)**

Recommended Operating Conditions

Sym	Parameter		DM5490A			DM7490A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	A	0		32	0		32	MHz
		Q_B	0		16	0		16	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'90A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A			80	μA
			Reset			40	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A			−3.2	mA
			Reset			−1.6	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			29	42	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'90A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		MHz
	B to Q_B	16			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		26	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40	ns

Recommended Operating Conditions

Sym	Parameter		DM5492A			DM7492A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	A	0		32	0		32	MHz
		Q_B	0		16	0		16	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'92A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			40	μA
			A			80	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−1.6	mA
			A			−3.2	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			26	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'92A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		MHz
	B to Q_B	16			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		34	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40	ns

Recommended Operating Conditions

Sym	Parameter		DM5493A			DM7493A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	A	0		32	0		32	MHz
		Q_B	0		16	0		16	
t_W	Pulse Width	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'93A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Reset			40	μA
			A			80	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−1.6	mA
			A			−3.2	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			26	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'93A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	32	42		MHz
	B to Q_B	16			
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_A		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_A		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		46	70	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		46	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_B		10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_C		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_C		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q_D		34	51	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to Q_D		34	51	ns
t_{PHL} Propagation Delay Time High to Low Level Output	SET-0 to Any Q		26	40	ns

Function Tables (Note D)

90A
BCD COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A
BI-QUINARY (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

92A
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

93A
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A
RESET/COUNT FUNCTION TABLE

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

92A, 93A
RESET/COUNT FUNCTION TABLE

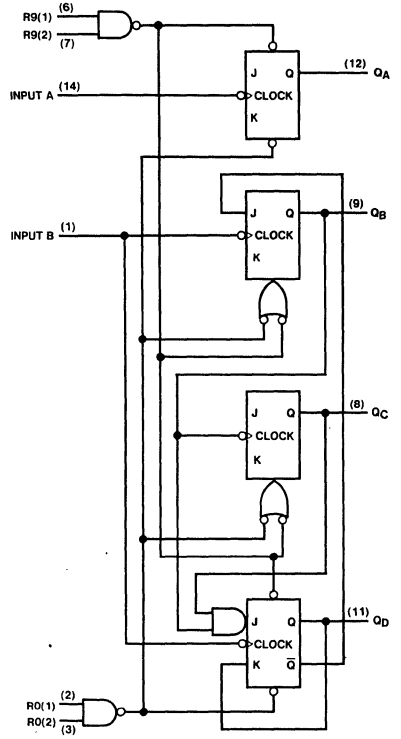
Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.
Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

6

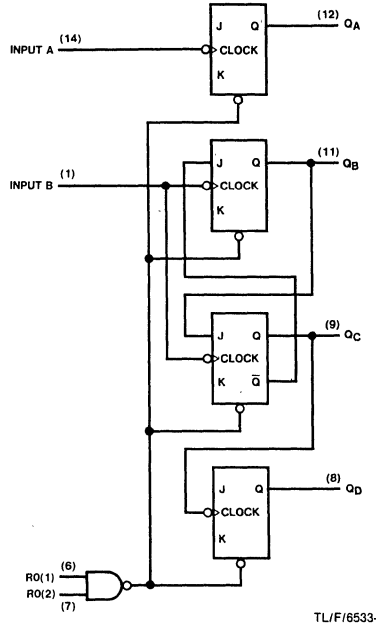
Logic Diagrams

90A



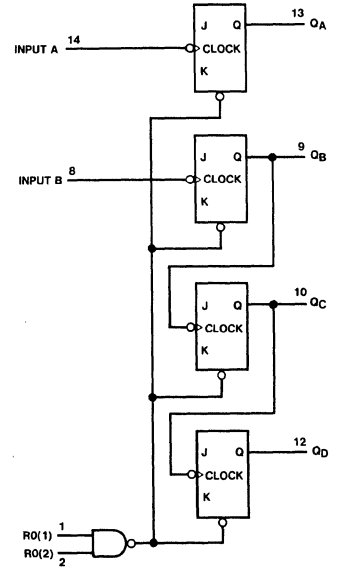
TL/F/6533-4

92A



TL/F/6533-5

93A



TL/F/6533-6

The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor

DM5495/DM7495 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 36 MHz
- Typical power dissipation 250 mW

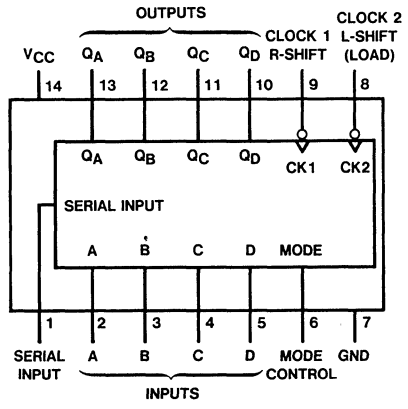
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6534-1

5495 (J) **7495 (N)**

Recommended Operating Conditions

Sym	Parameter		DM5495			DM7495			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Clock Pulse Width		15			15			ns
t_{SU}	Data Setup Time		20	10		20	10		ns
t_{EN}	Time to Enable Clock	Clock 1	20			20			ns
		Clock 2	15			15			
t_H	Data Hold Time		0	−10		0	−10		ns
t_{IN}	Time to Inhibit Clock 1 or 2		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			80	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Mode			−3.2	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−18		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded: Mode Control at 4.5V: and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	36		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		25	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		25	35	ns

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

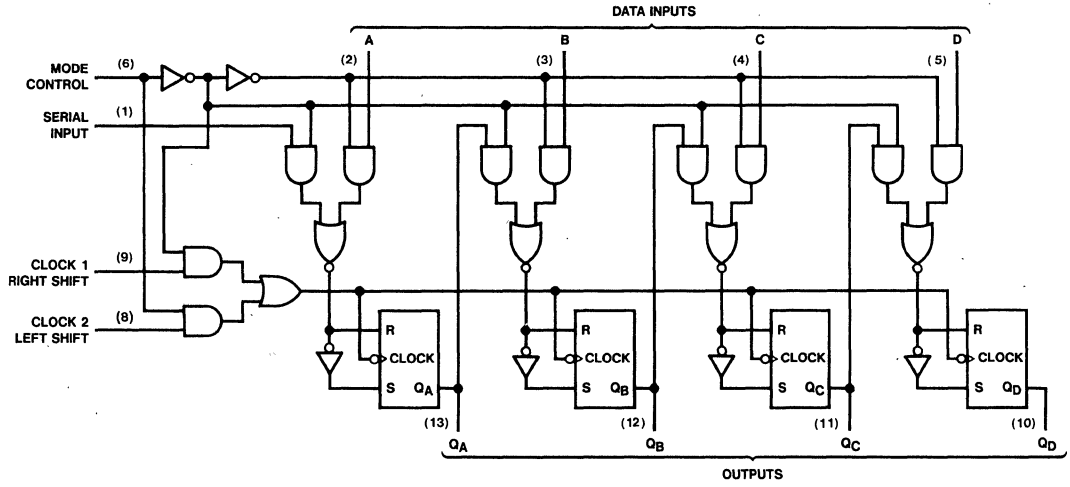
↓ = Transition from high to low level, ↑ = Transition from low to high level

a, b, c, d, = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Logic Diagram



TL/F/6534-2

National Semiconductor

DM5496/DM7496 5-Bit Shift Registers

General Description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may also be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is low. Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting is also independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

Features

- N-bit serial-to-parallel converter
- N-bit parallel-to-serial converter
- N-bit storage register

Absolute Maximum Ratings (Note 1)

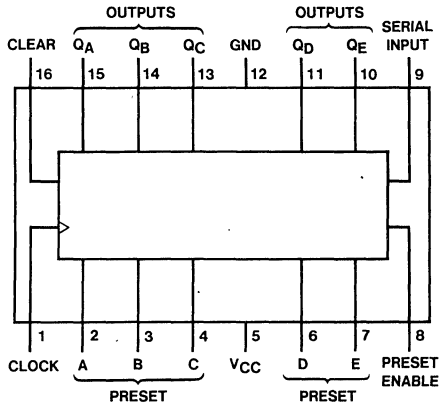
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

6

Connection Diagram

Dual-In-Line Package



TL/F/6535-1

5496 (J) 7496 (J, N)

Recommended Operating Conditions

Sym	Parameter		DM5496			DM7496			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		10	0		10	MHz
t_W	Pulse Width	Clock	35			35			ns
		Preset	30			30			
		Clear	30			30			
t_{SU}	Serial Setup Time		30			30			ns
t_H	Serial Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Preset Enable			200	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Preset Enable			−8	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		48	68	mA
			DM74		48	79	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

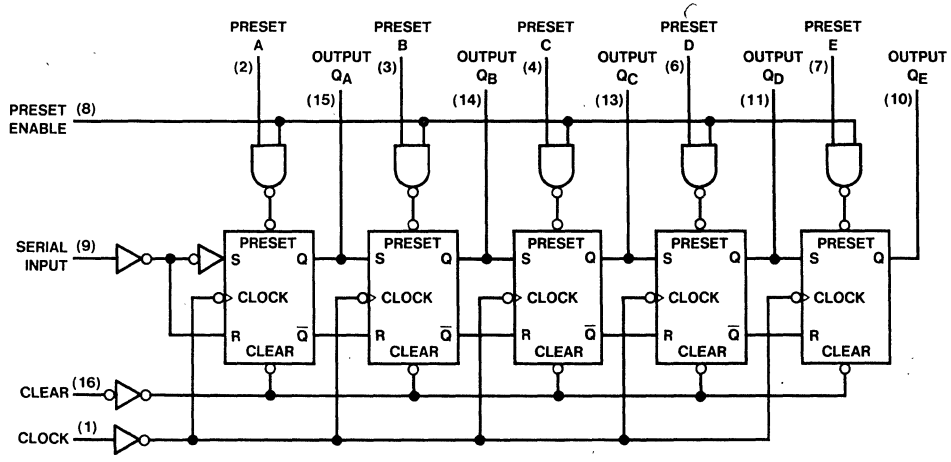
Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		10			MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		25	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Output		25	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output		25	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output			55	ns

Function Table

Inputs									Outputs				
Clear	Preset Enable	Preset A	Preset B	Preset C	Preset D	Preset E	Clock	Serial	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	↓	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	↓	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	↓	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = don't care (any input, including transitions)
↓ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc., respectively before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively before the most recent ↑ transition of the clock.

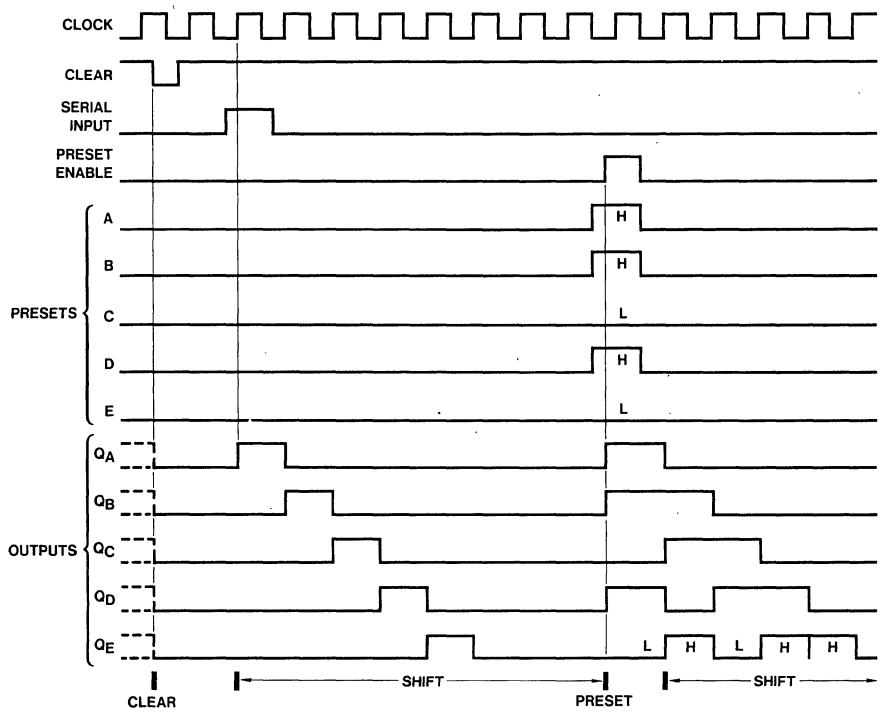
Logic Diagram



TL/F/6535-2

Timing Diagram

Typical Clear, Shift, Preset, and Shift Sequences



TL/F/6535-3

National Semiconductor

DM54107/DM74107 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the output regardless of the logic states of the other inputs.

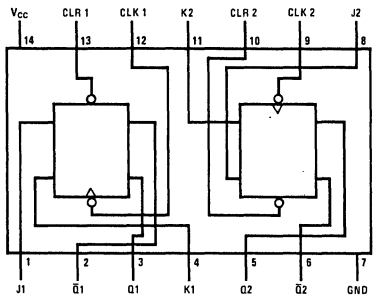
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6536-1

DM54107 (J) **DM74107 (N)**

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_O	$\overline{Q}_O$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete positive clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM54107			DM74107			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	20	15	0	20	15	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	47			47			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			18	34	mA

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse is used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to Q		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		25	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		16	25	ns

National Semiconductor

DM54109/DM74109 Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

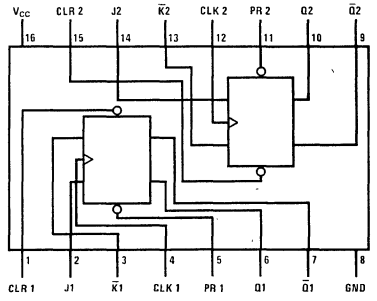
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6537-1

DM54109 (J) DM74109 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_O	$\overline{Q}_O$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_O	$\overline{Q}_O$

H = High Logic Level

L = Low Logic Level

↑ = Rising Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

6

Recommended Operating Conditions

Sym	Parameter		DM54109			DM74109			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1.2			−1.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		30	0		30	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	20			20			
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Input Setup Time (Note 1)		15↑			15↑			ns
t_H	Input Hold Time (Note 1)		10↑			10↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, $\overline{K}$			40	μA
			Preset			80	
			Clock			80	
			Clear			160	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 5)	J, $\overline{K}$			−1.6	mA
			Preset			−3.2	
			Clock			−3.2	
			Clear			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−30		−85	mA
			DM74	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			20	30	mA

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input grounded.

Note 5: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		18	29	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		19	28	ns

National Semiconductor

DM54121/DM74121 One-Shot with Clear and Complementary Outputs

General Description

The DM54/74121 is a monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 2kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. Inputs (A) are active-low trigger transition inputs and input (B) is an active-high transition Schmitt-trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal circuitry at the input stage.

To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

- Triggered from active-high transition or active-low transition inputs
- Variable pulse width from 30 ns to 28 seconds
- Jitter free Schmitt-trigger input
- Excellent noise immunity typically 1.2V
- Stable pulse width up to 90% duty cycle
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

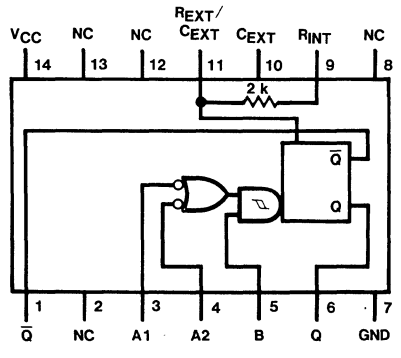
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Functional Description

The basic output pulse width is determined by selection of the internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few nano-seconds to 28 seconds by choosing appropriate R_X and C_X combinations. There are three trigger inputs from the device, two negative edge-triggering (A) inputs, one positive edge Schmitt-triggering (B) input.

Connection Diagram

Dual-In-Line Package



TL/F/6538-1

DM54121 (J) DM74121 (N)

Function Table

Inputs			Outputs	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎌
↓	H	H	⎍	⎌
↓	↓	H	⎍	⎌
L	X	↑	⎍	⎌
X	L	↑	⎍	⎌

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎌ = A Negative Pulse

Recommended Operating Conditions

Sym	Parameter		DM54121			DM74121			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)			1.4	2		1.4	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1.4		0.8	1.4		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1.5	2		1.5	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input		0.8	1.3		0.8	1.3		V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Input Pulse Width		50			50			ns
dV/dt	Rate of Rise or Fall of Schmitt Input (B)				1			1	V/s
dV/dt	Rate of Rise or Fall of Logic Input (A)				1			1	V/μs
R_{EXT}	External Timing Resistor		1.4		30	1.4		40	kΩ
C_{EXT}	External Timing Capacitance		0		1000	0		1000	μF
DC	Duty Cycle	R_T = 2 kΩ			67			67	%
		$R_T = R_{EXT}$(Max)			90			90	
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A1, A2			40	μA
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A1, A2			−1.6	mA
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		13	25	mA
			Triggered		23	40	

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output	A1, A2 to Q	C_{EXT} = 80 pF R_{INT} to V_{CC} C_L = 15 pF R_L = 400Ω		45	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q			35	55	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A1, A2 to $\overline{Q}$			50	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			40	65	ns
$t_{W(OUT)}$ Output Pulse Width using the Internal Timing Resistor	A1, A2 or B to Q,$\overline{Q}$	C_{EXT} = 80 pF R_{INT} to V_{CC} R_L = 400Ω C_L = 15pF	70	110	150	ns
$t_{W(OUT)}$ Output Pulse Width using Zero Timing Capacitance	A1, A2 to Q,$\overline{Q}$	C_{EXT} = 0 pF R_{INT} to V_{CC} R_L = 400Ω C_L = 15pF		30	50	ns
$t_{W(OUT)}$ Output Pulse Width using External Timing Resistor	A1, A2 to Q,$\overline{Q}$	C_{EXT} = 100 pF R_{EXT} = 10 kΩ R_L = 400Ω C_L = 15pF	600	700	800	ns
	A1, A2 to Q,$\overline{Q}$	C_{EXT} = 1 μF R_{EXT} = 10 kΩ R_L = 400Ω C_L = 15pF	6	7	8	ms

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

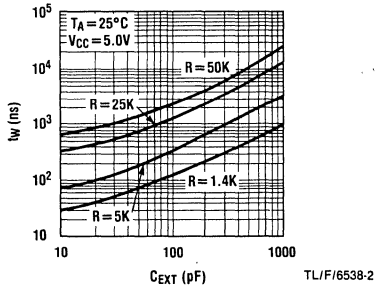
Note 2: Not more than one output should be shorted at a time.

Operating Rules

1. To use the internal 2 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (2 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For $C_X < 1000$ pF see *Figure 1* design curves on T_W as function of timing components value. For $C_X > 1000$ pF the output is defined as:

   $T_W = K R_X C_X$

   where [R_X is in Kilo-ohm]
   [C_X is in pico Farad]
   [T_W is in nano second]
   [$K \approx 0.7$]



TL/F/6538-2

FIGURE 1

4. If C_X is an electrolytic capacitor a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current (*Figure 2*).

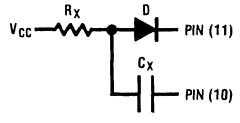
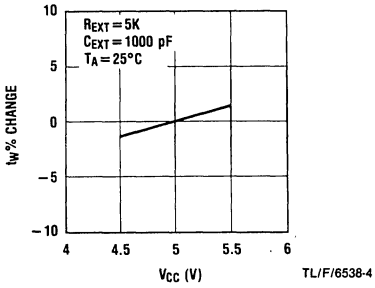


FIGURE 2

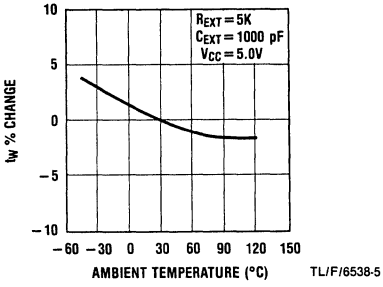
TL/F/6538-3

5. Output pulse width versus V_{CC} and operation temperatures: *Figure 3* depicts the relationship between pulse width variation versus V_{CC}. *Figure 4* depicts pulse width variation versus ambient temperature.



TL/F/6538-4

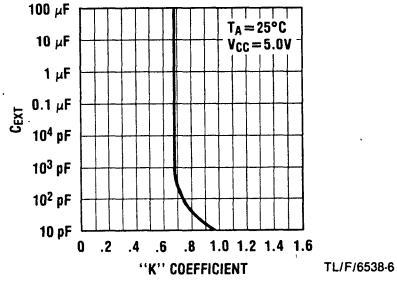
FIGURE 3



TL/F/6538-5

FIGURE 4

6. The "K" coefficient is not a constant, but varies as a function of the timing capacitor C_X. *Figure 5* details this characteristic.



TL/F/6538-6

FIGURE 5

7. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (10) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
8. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

*For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

6

National Semiconductor

DM54123/DM74123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading-edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components.

National's '123 device features an unique logic realization not implemented by other manufacturers. The "Clear" input will not trigger the device, a design tailored for applications where it shall only terminate or reduce a timing pulse.

To obtain the best and trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations
- DTL, TTL compatible
- Input clamp diodes

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

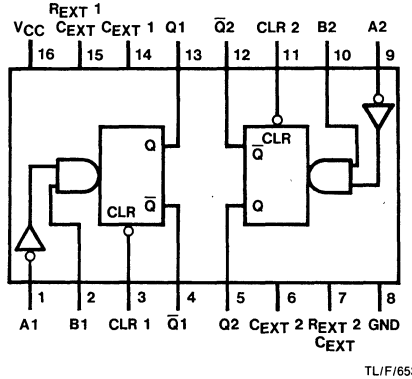
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low transition clear input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Connection Diagram

Dual-In-Line Package



TL/F/6539-1

DM54123 (J) DM74123 (N)

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎎ = A Negative Pulse

Recommended Operating Conditions

Sym	Parameter		DM54123			DM74123			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Pulse Width	A or B High	40			40			ns
		A or B Low	40			40			
		Clear Low	40			40			
T_{WQ} (Min)	Minimum Width of Pulse at Q	A or B		45	65		45	65	ns
R_{EXT}	External Timing Resistor		5		25	5		50	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50			50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Data			40	μA
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−10		−40	mA
			DM74	−10		−40	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3 and 4)			46	66	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) to (Output)	$R_L = 400\Omega$						Units
		$C_L = 15$ pF, $C_{EXT} = 0$ pF, $R_{EXT} = 5$ kΩ			$C_L = 15$ pF, $C_{EXT} = 1000$ pF, $R_{EXT} = 10$ kΩ			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q		22	33				ns
t_{PLH} Propagation Delay Time Low to High Level Output	B to Q		19	28				ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		30	40				ns
t_{PHL} Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		27	36				ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		30	40				ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		18	27				ns
$t_{W(out)}$ Output Pulse Width	A or B to Q				3.08	3.42	3.76	μs

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current (*Figure 2*). However, its use in general is not recommended with retriggerable operation.
3. The output pulse width (T_W) is defined as follows:

   $T_W = K R_X C_X (1 + 0.7/R_X)$

   where [R_X is in Kilo-ohm]
   [C_X is in pico Farad]
   [T_W is in nano second]
   [$K \approx 0.34$]
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

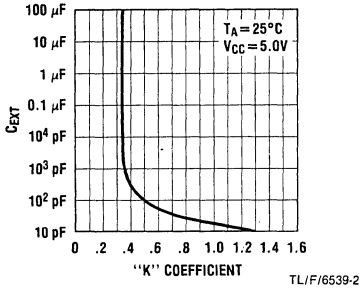


FIGURE 1

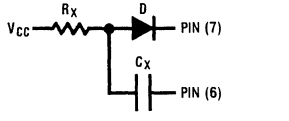


FIGURE 2

5. For $C_X < 1000$ pF see *Figure 3* for T_W vs C_X family curves with R_X as a parameter:

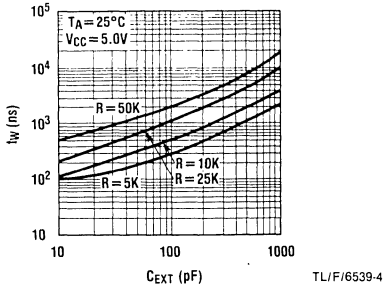
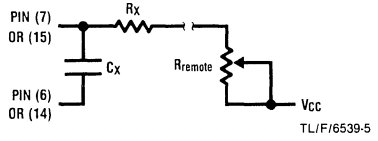


FIGURE 3

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



Note: "R_{remote}" should be as close to the one-shot as possible.

FIGURE 4

7. The retriggerable pulse width is calculated as shown below:

   $T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$

   The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 5)*.

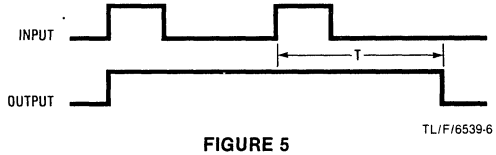


FIGURE 5

6

Operating Rules (Continued)

8. Output pulse width versus V_{CC} and Temperatures: *Figure 6* depicts the relationship between pulse width variation versus operating V_{CC}. *Figure 7* depicts pulse width variation versus ambient temperatures.

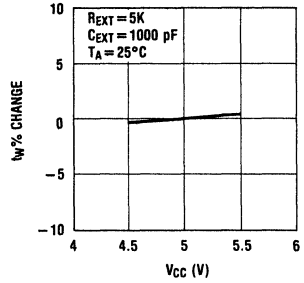


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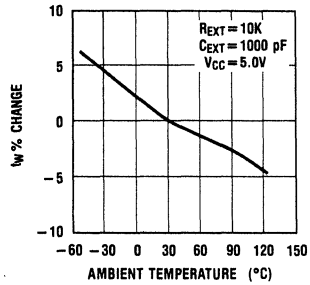
FIGURE 6



TL/F/6539-8

FIGURE 7

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.

10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.
    * However, it should be noted that although the 74221 series one-shot is pin-for-pin compatiable with the '123 device, its C_{EXT} pin is not an internal connection to ground. Hence, if substitution of an '221 on to an '123 design layout whose C_{EXT} pin is wired to the ground is attempted, the '221 device will not function!

11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

*For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

National Semiconductor

DM54125/DM74125 Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability at the high Logic level to permit the driving of bus lines without external pull-up resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

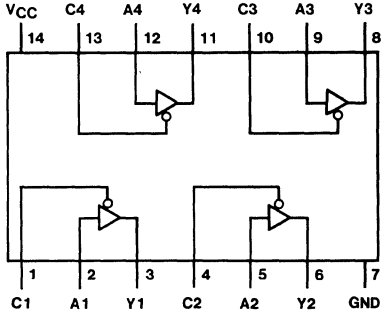
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6540-1

DM54125 (J) DM74125 (N)

Function Table

Y = A

Input		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

6

Recommended Operating Conditions

Sym	Parameter	DM54125			DM74125			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{IZL}	Off-State Input Current with Low Level Input Voltage Applied	V_{CC} = Max V_I = 0.4V				−40	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−28		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			36	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the output control (C) inputs at 4.5V, the data inputs grounded, and the outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output					12	18	ns
t_{PZH} Output Enable Time to High Level Output					12	18	ns
t_{PZL} Output Enable Time to Low Level Output					16	25	ns
t_{PHZ} Output Disable Time from High Level Output		5	8				ns
t_{PLZ} Output Disable Time from Low Level Output		9	14				ns

National Semiconductor

DM54126/DM74126 Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability at the high logic level to permit the driving of bus lines without external pull-up resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

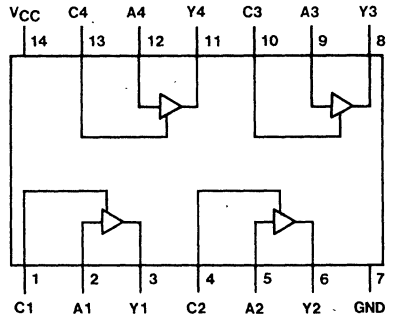
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6541-1

DM54126 (J) **DM74126 (N)**

Function Table

Y = A

Input		Output
A	C	Y
L	H	L
H	H	H
X	L	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Sym	Parameter	DM54126			DM74126			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{IZL}	Off-State Input Current with Low Level Input Voltage Applied	V_{CC} = Max V_I = 0.4V				−40	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−28		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			36	62	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with both the output control and data inputs grounded, and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output					12	18	ns
t_{PZH} Output Enable Time to High Level Output					13	19	ns
t_{PZL} Output Enable Time to Low Level Output					16	25	ns
t_{PHZ} Output Disable Time from High Level Output		10	16				ns
t_{PLZ} Output Disable Time from Low Level Output		14	20				ns

National Semiconductor

DM54132/DM74132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

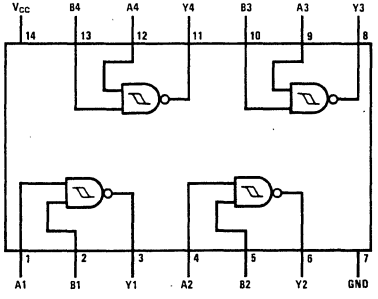
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6542-1

DM54132 (J) **DM74132 (N)**

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

6

Recommended Operating Conditions

Symbol	Parameter	DM54132			DM74132			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-} Min	DM54	2.4	3.4		V
			DM74	2.4	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+} Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.56		mA
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.8	−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			15	24	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			26	40	mA

Note 1: V_{CC} = 5V.
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$, $C_L = 15$ pF			Units
	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		15	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output		15	22	ns

National Semiconductor

DM54141/DM74141 BCD to Decimal Decoders/Drivers

General Description

The DM54141/DM74141 is a BCD-to-decimal decoder designed to drive cold-cathode indicator tubes.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display.

Input clamp diodes are also provided to clamp negative-voltage transitions in order to minimize transmission-line effects.

Features

- Drive cold-cathode, numeric indicator tubes directly
- Fully decoded inputs
- Low leakage current 50 μA @ 55 V
- Low power dissipation 55 mW typical

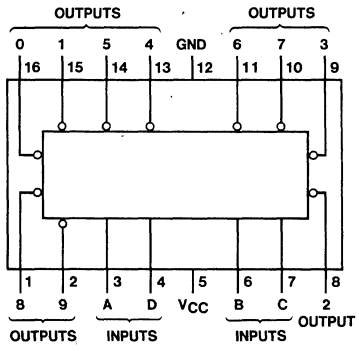
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6543-1

54141 (J) **74141 (N)**

Function Table

Input				Output
D	C	B	A	On*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(Over Range)				
H	L	H	L	None
H	L	H	H	None
H	H	L	L	None
H	H	L	H	None
H	H	H	L	None
H	H	H	H	None

H = High Level, L = Low Level
*All other outputs are off

Recommended Operating Conditions

Sym	Parameter	DM54141			DM74141			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OL}	Low Level Output Current			7			7	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

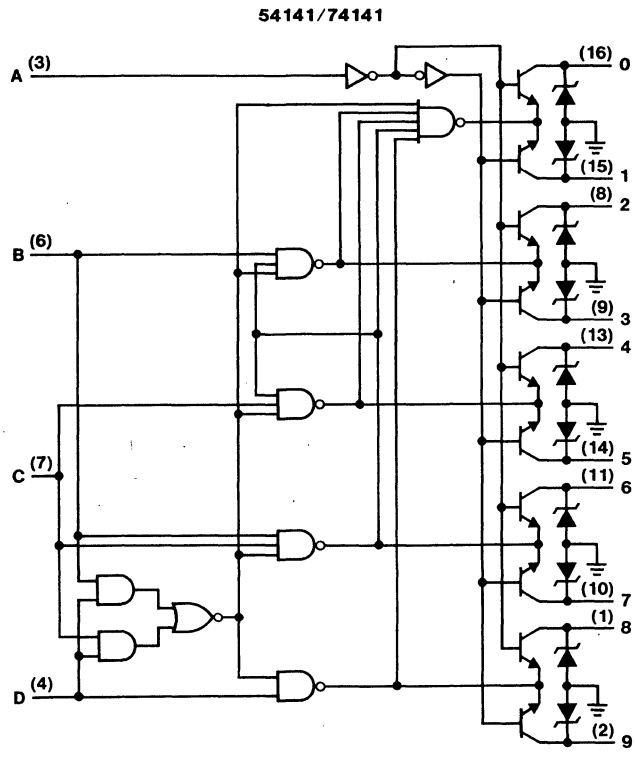
Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 0.5 mA		60			V
I_{OH}	Off-State Reverse Current for Input Counts 10-15	V_{CC} = Min, V_O = 30V	T_A = −55°C			5	μA
			T_A = 70°C			15	
I_{OH}	Off-State Reverse Current for Input Counts 0-9	V_{CC} = Min, V_O = 55V				50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	T_A = −55 to 70°C			2.5	V
			T_A = 125°C			3	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	A Input			40	μA
			B, C, D Inputs			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A Input			−1.6	mA
			B, C, D Inputs			−3.2	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			11	25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

Logic Diagram



TL/F/6543-2

National Semiconductor

DM54145/DM74145 BCD to Decimal Decoders/Drivers

General Description

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

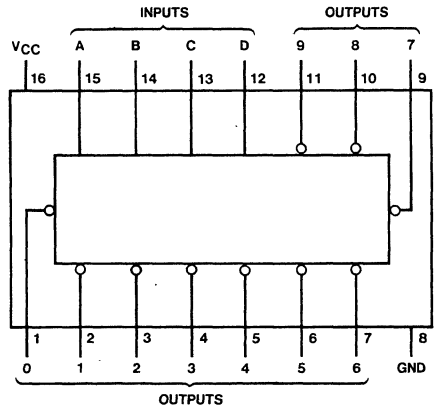
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6544-1

54145 (J) 74145 (N)

Recommended Operating Conditions

Sym	Parameter	DM54145			DM74145			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{OH} = Max V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min V_{IL} = Max				0.4	V
		I_{OL} = 80 mA V_{CC} = Min			0.5	0.9	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		43	62	mA
			DM74		43	70	

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 100Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output				30	ns
t_{PHL} Propagation Delay Time High to Low Level Output				30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

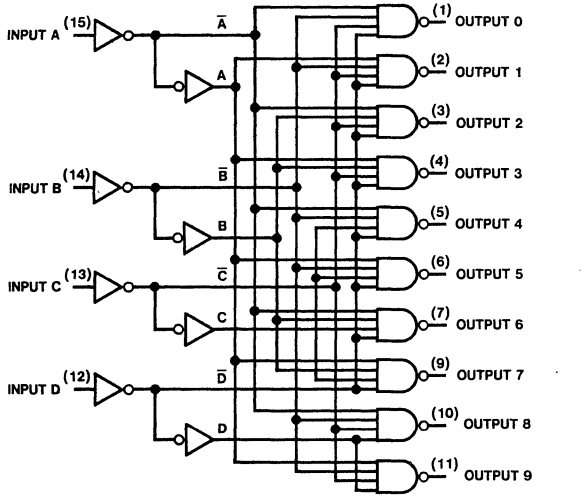
Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Function Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level (Off), L = Low Level (On)

Logic Diagram



TL/F/6544-2

National Semiconductor

DM54147/DM74147, DM54148/DM74148 Priority Encoders

General Description

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. The DM54147 and DM74147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All inputs are buffered to represent one normalized Series 54/74 load. The DM54148 and DM74148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

DM54147, DM74147

- Encodes 10-line decimal to 4-line BCD
- Applications include:
  - Keyboard encoding
  - Range selection
- Typical data delay 10 ns
- Typical power dissipation 225 mW

DM54148, DM74148

- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

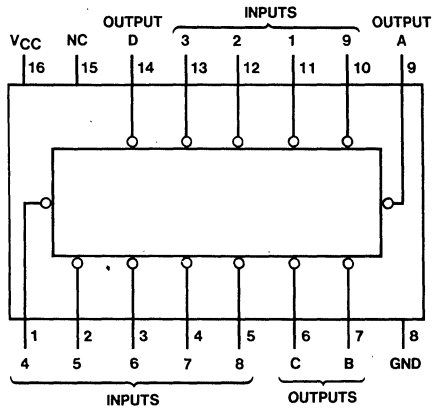
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

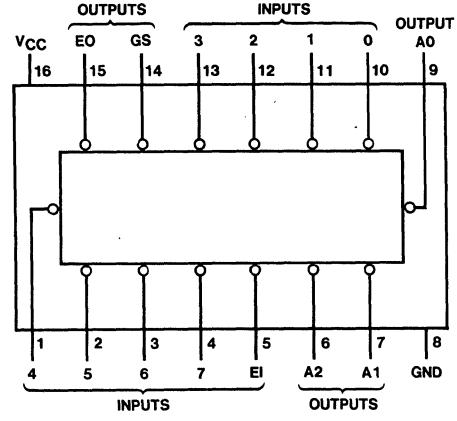
Dual-In-Line Package



TL/F/6545-1

54147 (J) 74147 (J,N)

Dual-In-Line Package



TL/F/6545-2

54148 (J) 74148 (J,N)

Recommended Operating Conditions

Sym	Parameter	DM54147			DM74147			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'147 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−35		−85	mA
			DM74	−35		−85	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			50	70	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			42	62	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with input 7 grounded, other inputs and outputs open.

Note 4: I_{CC2} is measured with all inputs and all outputs open.

'147 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Waveform	$R_L = 400\Omega$, $C_L = 15$ pF			Units
			Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 9 to Output	In-Phase Output		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 9 to Output			7	11	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 9 to Output	Out-of-Phase Output		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 9 to A, B, C, D			12	19	ns

Recommended Operating Conditions

Sym	Parameter	DM54148			DM74148			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'148 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−35		−85	mA
			DM74	−35		−85	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			40	60	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			35	55	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with inputs E1 and 7 grounded, other inputs and outputs open.

Note 4: I_{CC2} is measured with all inputs and all outputs open.

'148 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Waveform	$R_L = 400\Omega$, $C_L = 15$ pF			Units
			Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 9 to A0, 1, 2	In-Phase Output		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 9 to A0, 1, 2			9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 9 to A0, 1, 2	Out-of-Phase Output		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 9 to A0, 1, 2			12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 7 to E0	Out-of-Phase Output		6	10	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 7 to E0			14	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 7 to GS	In-Phase Output		18	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 7 to GS			14	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	E1 to A0, 1, 2	In-Phase Output		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	E1 to A0, 1, 2			10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	E1 to GS	In-Phase Output		8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	E1 to GS			10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	E1 to E0	In-Phase Output		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	E1 to E0			17	30	ns

Function Tables

54147/74147

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

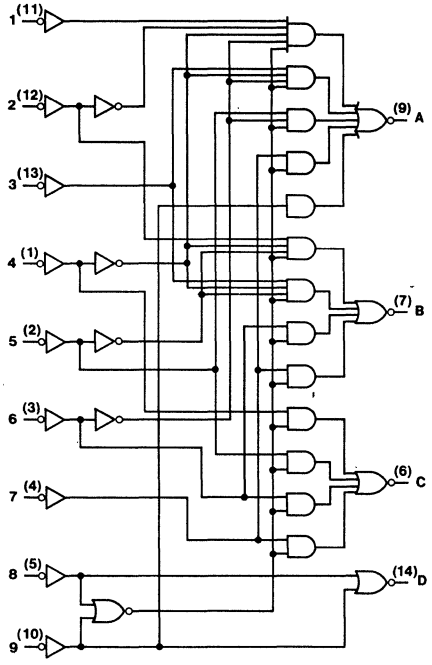
54148/74148

Inputs									Outputs				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't care

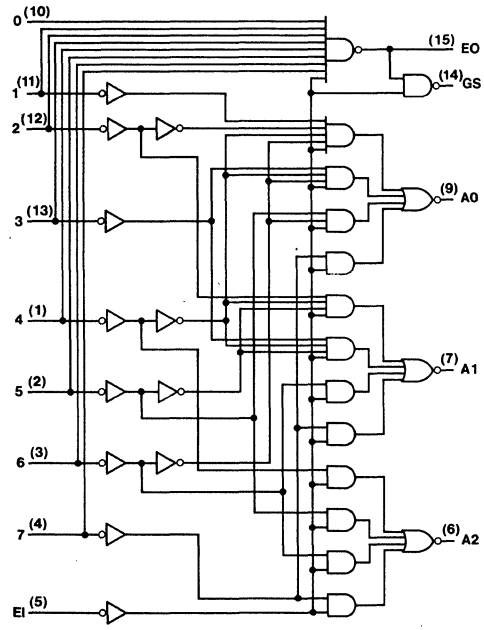
Logic Diagrams

147



TL/F/6545-3

148



TL/F/6545-4

National Semiconductor

DM54150/DM74150, DM54151A/DM74151A Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output (as applicable) low.

The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.

The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output
  - 150 11 ns
  - 151A 9 ns
- Typical power dissipation
  - 150 200 mW
  - 151A 135 mW

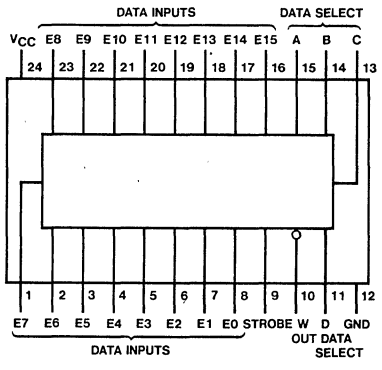
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

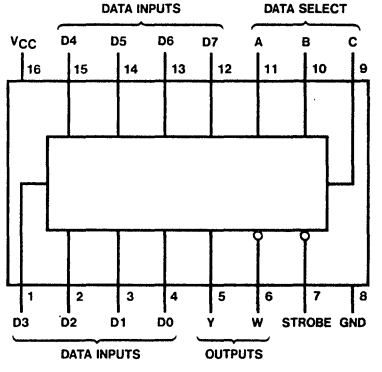
Dual-In-Line Package



TL/F/6546-1

54150 (J) 74150 (N)

Dual-In-Line Package



TL/F/6546-2

54151A (J) 74151A (N)

Recommended Operating Conditions

Sym	Parameter	DM54150			DM74150			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'150 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			40	68	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

'150 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to W		21	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to W		22	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to W		15	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to W		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	E0-E15 to W		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	E0-E15 to W		8.5	14	ns

Recommended Operating Conditions

Sym	Parameter	DM54151A			DM74151A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'151A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			27	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

'151A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		23	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		23	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		16	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		16	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		25	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		19	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to W		11	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to W		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D0-D7 to Y		17	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D0-D7 to Y		18	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D0-D7 to W		10	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D0-D7 to W		8	14	ns

Function Tables

54150/74150

Inputs					Output
Select				Strobe	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

54151A/74151A

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

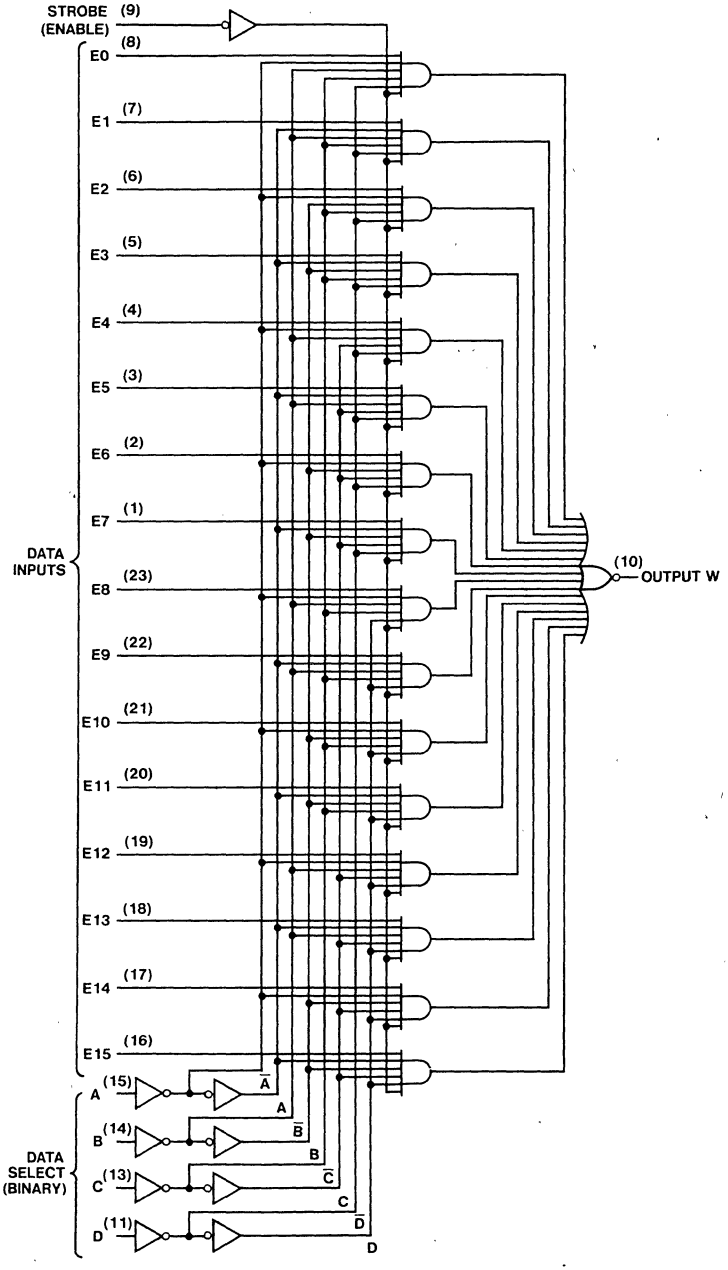
H = High Level, L = Low Level, X = Don't Care

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

D0, D1 . . . D7 = the level of the respective D input

Logic Diagrams

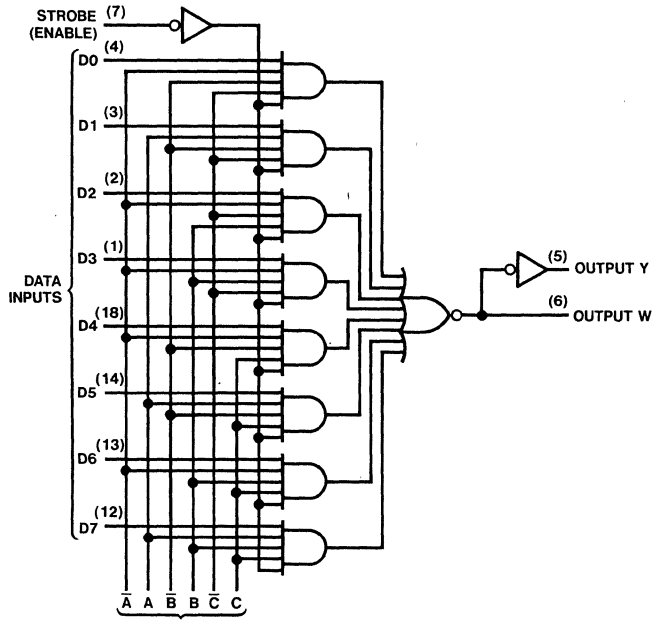
150



TL/F/6546-3

Logic Diagrams (Continued)

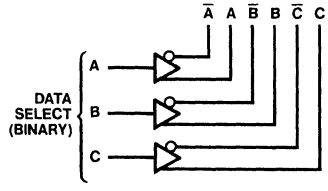
151A



See Address Buffers Below

TL/F/6546-4

Address Buffers for 54151A/74151A



TL/F/6546-5

National Semiconductor

DM54153/DM74153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  - From data 11 ns
  - From strobe 18 ns
  - From select 20 ns
- Typical power dissipation 170 mW

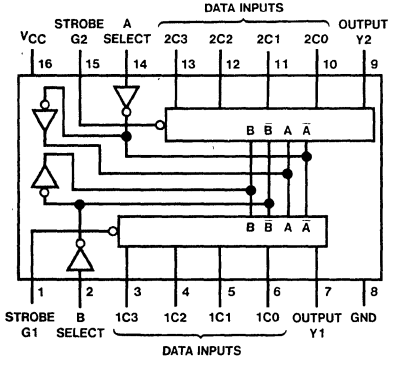
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6547-1

54153 (J) **74153 (N)**

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

6

Recommended Operating Conditions

Sym	Parameter	DM54153			DM74153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	52	mA
			DM74		34	60	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

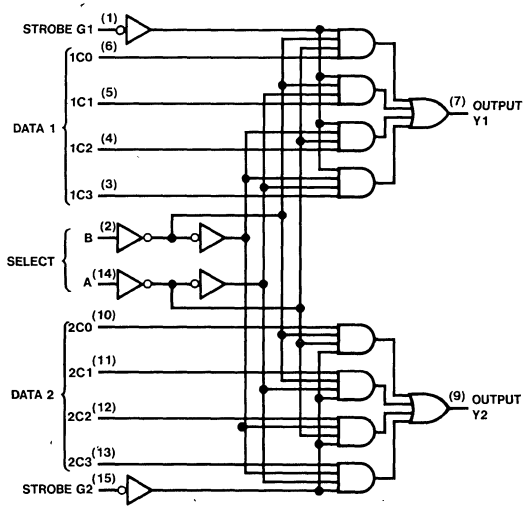
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 30$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		11	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		10	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		20	34	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		20	34	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		19	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		17	23	ns

Logic Diagram



TL/F/6547-2

6

National Semiconductor

DM54154/DM74154 4-Line to 16-Line Decoders/Demultiplexers

General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 19 ns
  Strobe 18 ns
- Typical power dissipation 170 mW

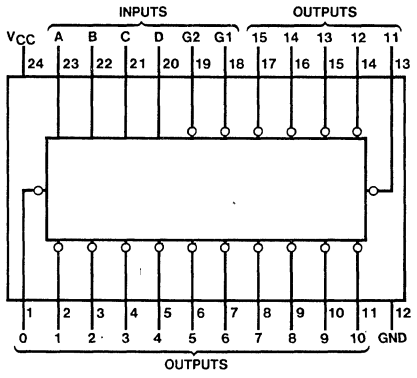
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6548-1

54154 (J) **74154 (N)**

Recommended Operating Conditions

Sym	Parameter	DM54154			DM74154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

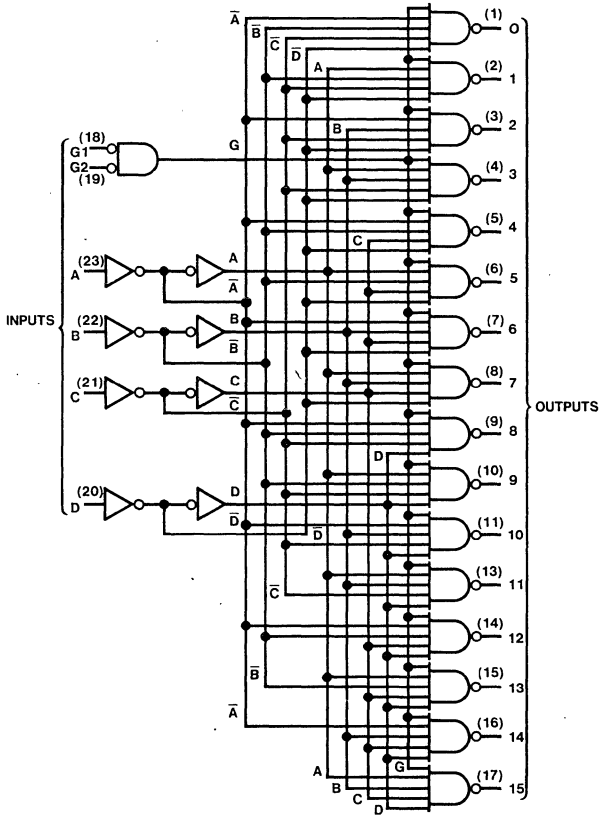
Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		18	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		21	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		17	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		18	27	ns

Function Table

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



TL/F/6548-2

National Semiconductor

DM54155/DM74155, DM54156/DM74156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demuliplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  - Totem-pole (155)
  - Open-collector (156)

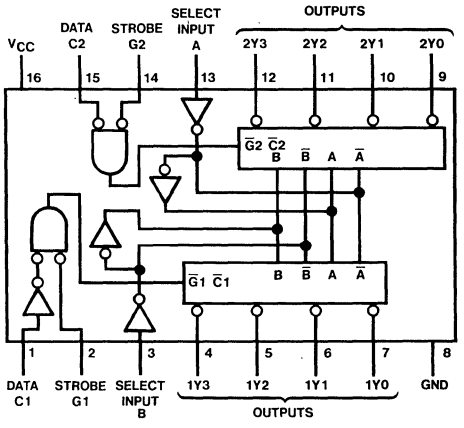
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (for 156)	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6549-1

54155 (J) 74155 (N)
54156 (J) 74156 (N)

Function Tables

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

Recommended Operating Conditions

Sym	Parameter	DM54155			DM74155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'155 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		25	35	mA
			DM74		25	40	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

'155 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C2 G1 or G2 to Y		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C2 G1 or G2 to Y		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y		17	26	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C1 to Y		17	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C1 to Y		17	26	ns

Recommended Operating Conditions

Sym	Parameter	DM54156			DM74156			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'156 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				− 1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		25	35	mA
			DM74		25	40	

'156 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

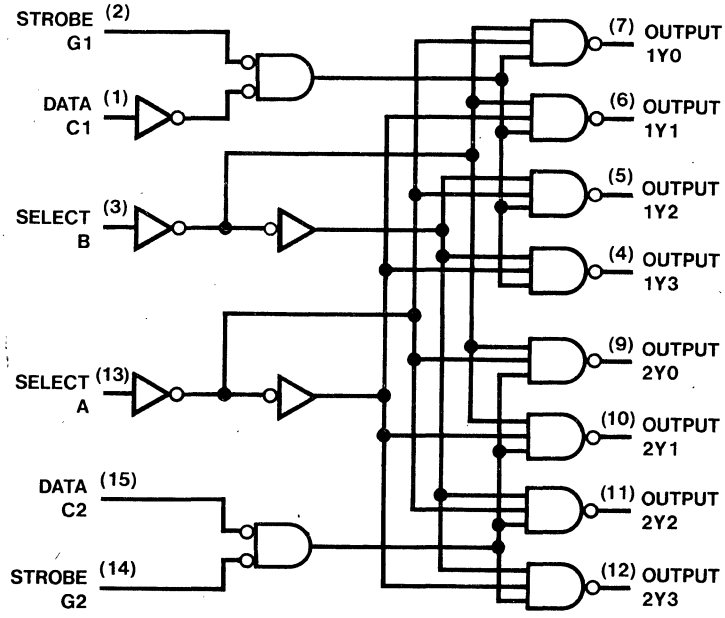
Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C2 G1 or G2 to Y		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C2 G1 or G2 to Y		19	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A or B to Y		21	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A or B to Y		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C1 to Y		19	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C1 to Y		18	27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

6

Logic Diagram



TL/F/6549-2

National Semiconductor

DM54157/DM74157 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Three speed/power ranges available
- Typical propagation time 9 ns
- Typical power dissipation 150 mW

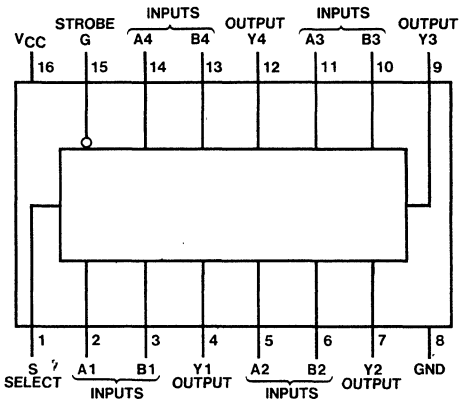
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6550-1

Low level at S selects A inputs
High level at S selects B inputs

54157 (J) **74157 (N)**

Function Table

Inputs				Output Y
Strobe	Select	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

6

Recommended Operating Conditions

Sym	Parameter	DM54157			DM74157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

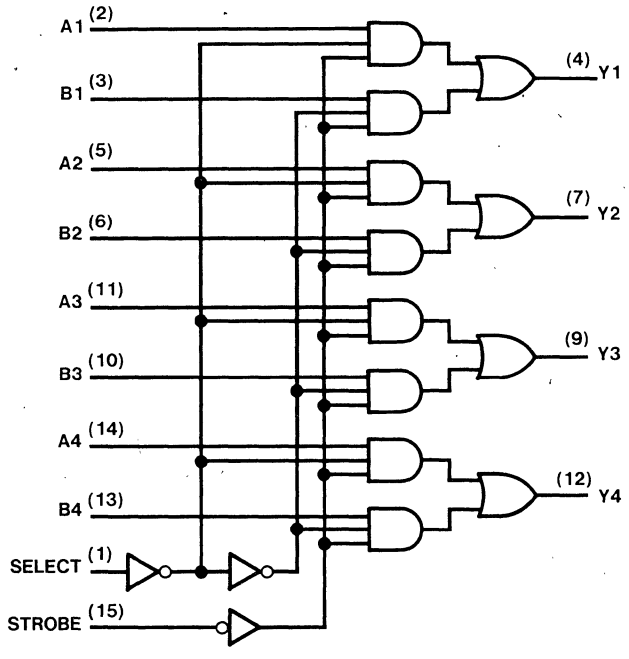
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		8	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		10	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		17	27	ns

Logic Diagram

157



TL/F/6550-2

National Semiconductor

DM54160A/DM74160A, DM54161A/DM74161A, DM54162A/DM74162A, DM54163A/DM74163A Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 160A and 162A are decade counters and the 161A and 163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input of the 160A through 163A are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 160A and 161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the 162A and 163A is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 162A and 163A are also permissible, regardless of the logic levels on the clock, enable, or load inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 160A through 163A may occur, regardless of the logic level on the clock.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 35 MHz
- Typical power dissipation 315 mW

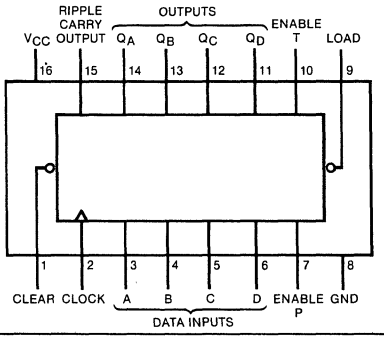
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6551-1

54160A (J) 74160A (N)
54161A (J) 74161A (N)
54162A (J) 74162A (N)
54163A (J) 74163A (N)

Recommended Operating Conditions

Sym	Parameter		DM54160A thru 163A			DM74160A thru 163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time	Data	20			20			ns
		Enable P	34			34			
		Load	25			25			
		Clear (Note 5)	20			20			
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Enable T			80	μA
			Clock			80	
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−3.2	mA
			Clock			−3.2	
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−20		−57	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)	DM54		59	85	mA
			DM74		59	94	
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)	DM54		63	91	mA
			DM74		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD high, then again with the LOAD low, with all inputs high and all outputs open.

Note 4: I_{CCL} is measured with the CLOCK high, then again with the CLOCK input low, with all inputs low and all outputs open.

Note 5: Applies to '162A and '163A which have synchronous clear inputs.

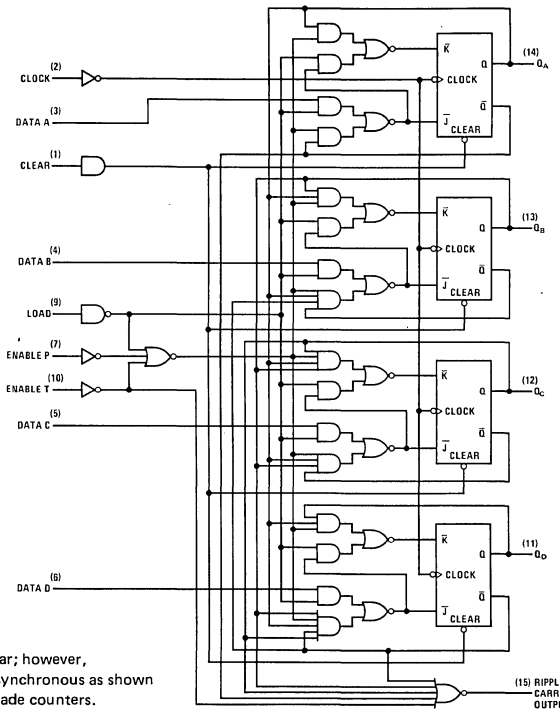
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock (Load High) to Q		14	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock (Load High) to Q		22	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock (Load Low) to Q		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock (Load Low) to Q		22	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		11	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear (Note 1) to Q		24	36	ns

Note 1: Propagation delay for clearing is measured from the clear input for the 160A and 161A or from the clock input transition for the 162A and 163A.

Logic Diagrams

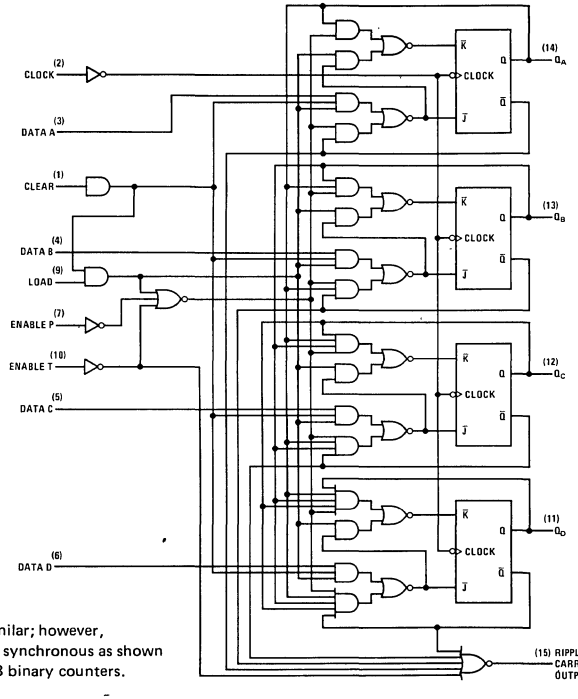
160A



161A is similar; however, the clear is asynchronous as shown for 160A decade counters.

TL/F/6551-2

163A

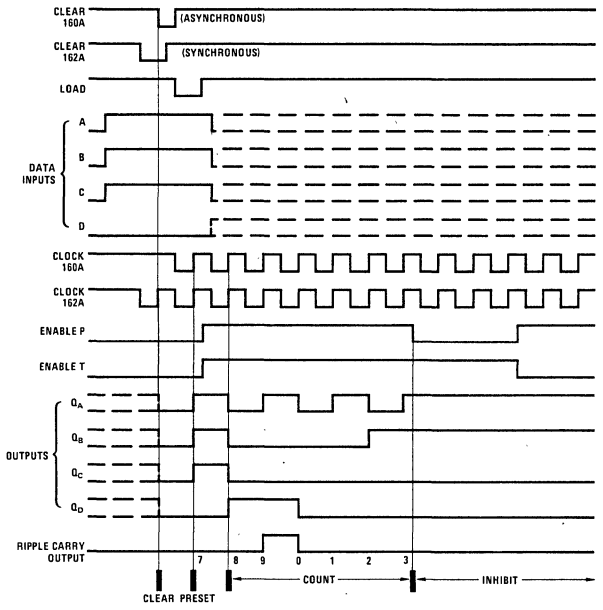


162A is similar; however, the clear is synchronous as shown for the 163 binary counters.

TL/F/6551-3

Timing Diagrams

160A, 162A SYNCHRONOUS DECADE COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

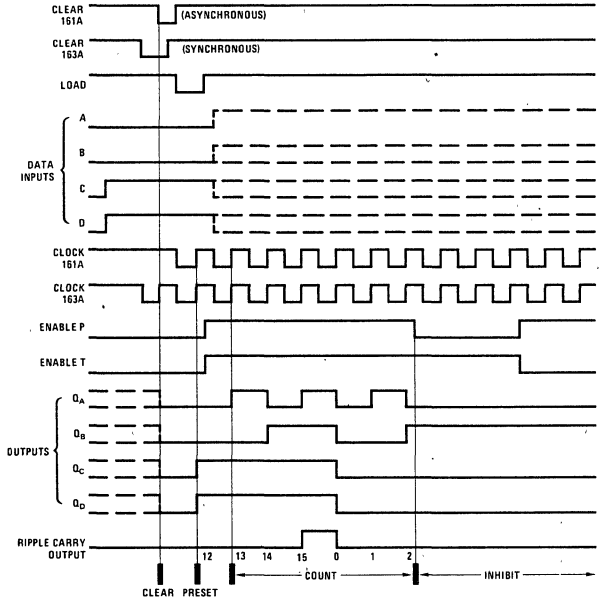


TL/F/6551-4

Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161A, 163A SYNCHRONOUS BINARY COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



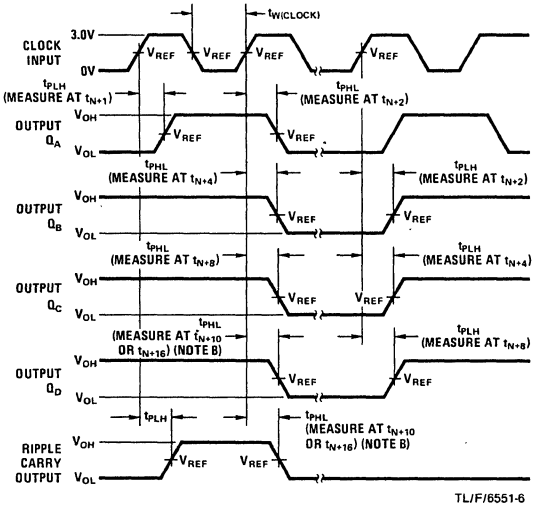
TL/F/6551-5

Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

SWITCHING TIME WAVEFORMS



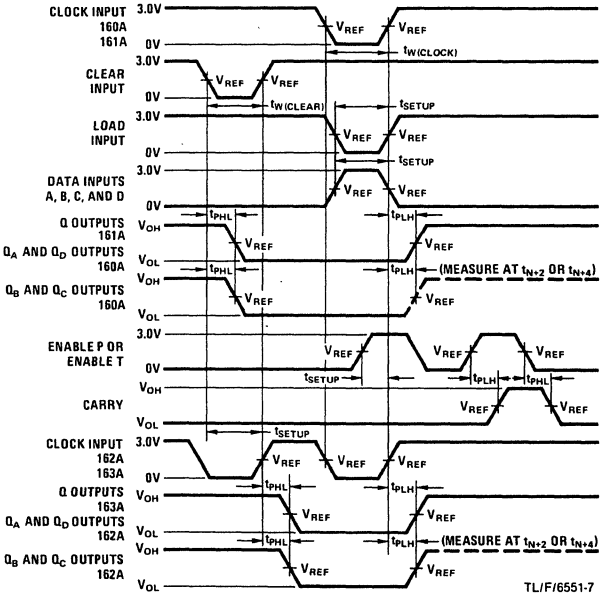
TL/F/6551-6

Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for 160A, 162A and at t_{n+16} for 161A, 163A where t_n is the bit time when all outputs are low.

Note C: For 160A through 163A, $V_{REF} = 1.5V$.

SWITCHING TIME WAVEFORMS



TL/F/6551-7

Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: For 160A through 163A, $V_{REF} = 1.5V$.

National Semiconductor

DM54164/DM74164 8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

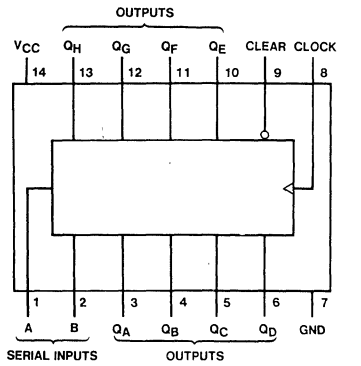
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6552-1

54164 (J) 74164 (N)

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Recommended Operating Conditions

Sym	Parameter		DM54164			DM74164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				8			8	mA
f_{CLK}	Clock Frequency		0	36	25	0	36	25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time		15			15			ns
t_H	Data Hold Time		5			5			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−10		−27.5	mA
			DM74	−9		−27.5	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			37	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

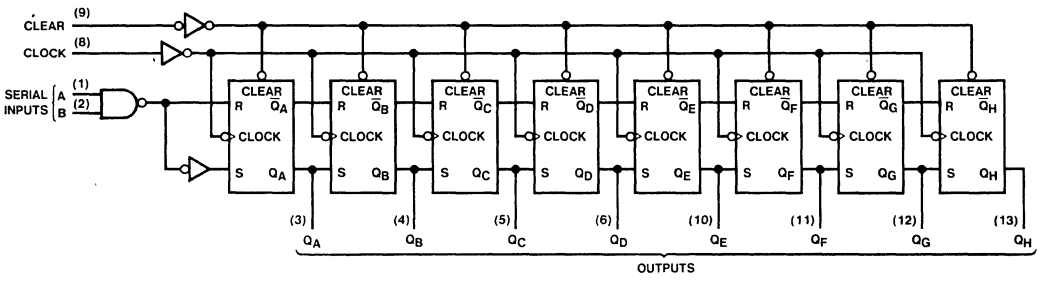
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

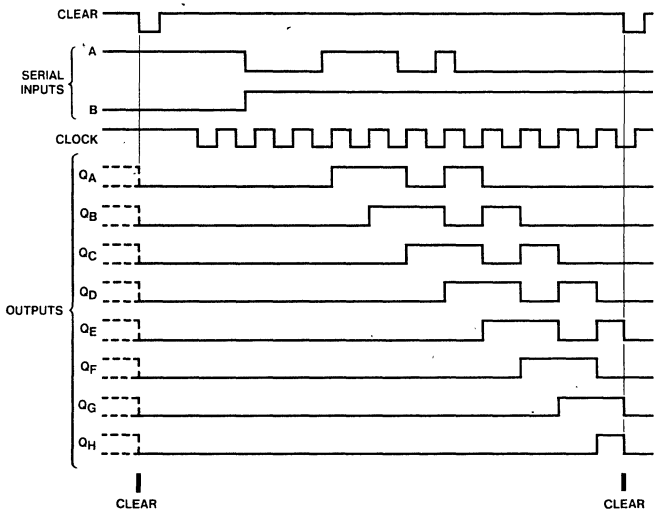
Parameter	From (Input) To (Output)	$R_L = 800\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	36					MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output	8	17	27	10	20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output	10	21	32	10	25	37	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		24	36		28	42	ns

Logic Diagram



TL/F/6552-2

Timing Diagram



TL/F/6552-3

National Semiconductor

DM54165/DM74165 8-Bit Parallel In/Serial Out Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 20 MHz
- Typical power dissipation 200 mW

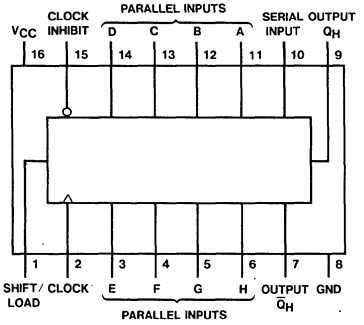
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6553-1

54165 (J) **74165 (N)**

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low-to-high level
a ... h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Recommended Operating Conditions

Sym	Parameter		DM54165			DM74165			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	20	14	0	20	14	MHz
t_W	Pulse Width	Clock	35			35			ns
		Load	35			35			
t_{SU}	Setup Time	Parallel	25			25			ns
		Serial	40			40			
t_H	Data Hold Time		5			5			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Shift/Load			80	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Shift/Load			−3.2	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			40	63	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

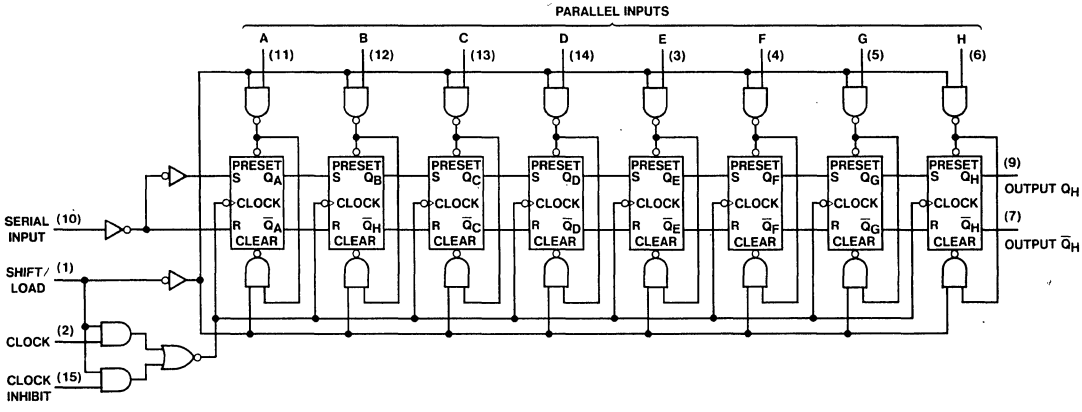
Note 2: Not more than one output should be shorted at a time.

Note 3: With the outputs open, the CLOCK inhibit and SHIFT/LOAD inputs at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then at ground.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		14	20		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		34	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		42	60	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		26	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		35	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to Q_H		25	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to Q_H		36	50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		25	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		36	50	ns

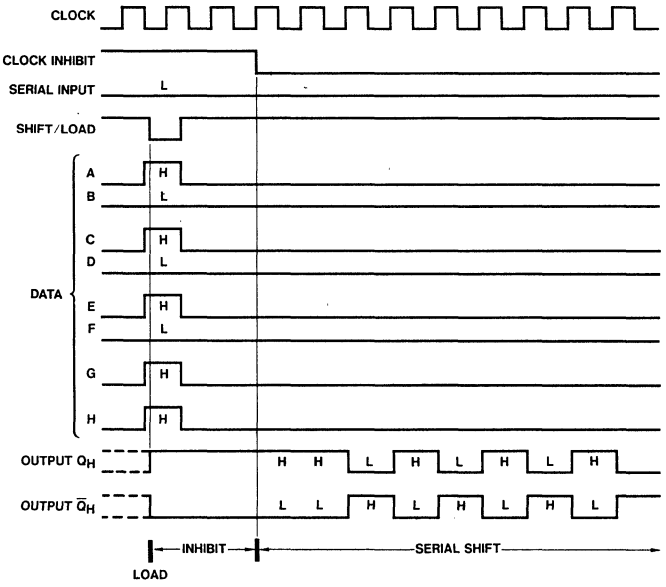
Logic Diagram



TL/F/6552-2

Timing Diagram

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES



TL/F/6552-3

National Semiconductor

DM54166/DM74166 8-Bit Parallel In/Serial Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

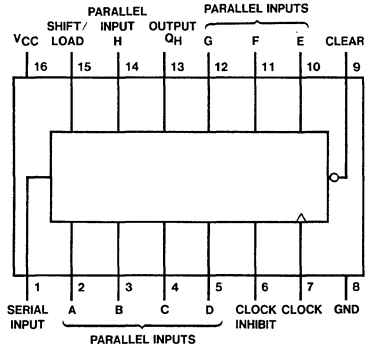
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6554-1

54166 (J) **74166 (N)**

Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a...h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Recommended Operating Conditions

Sym	Parameter		DM54166			DM74166			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	24			24			ns
		Clear	20			20			
t_{SU}	Setup Time	Mode	30			30			ns
		Data	20			20			
t_H	Data Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		72	104	mA
			DM74		72	116	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

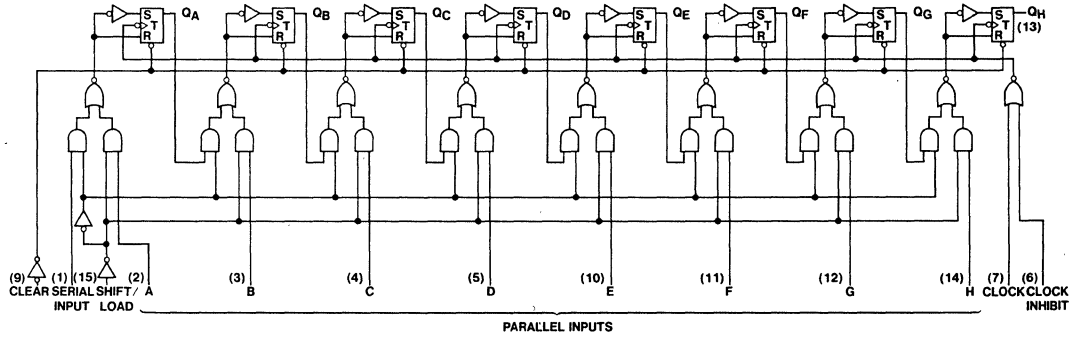
Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, 4.5V applied to the SERIAL input, all other inputs except CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output	8	17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output	8	20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		23	35	ns

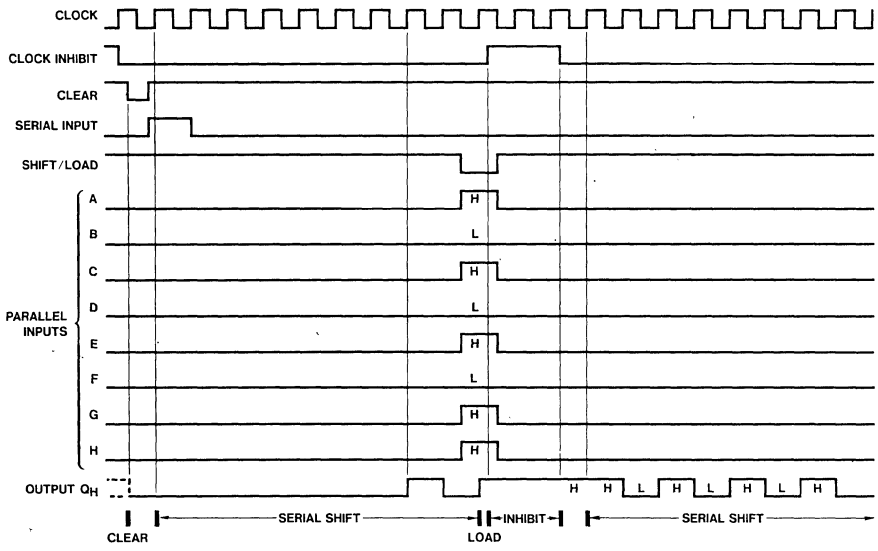
Logic Diagram



TL/F/6554-2

Timing Diagram

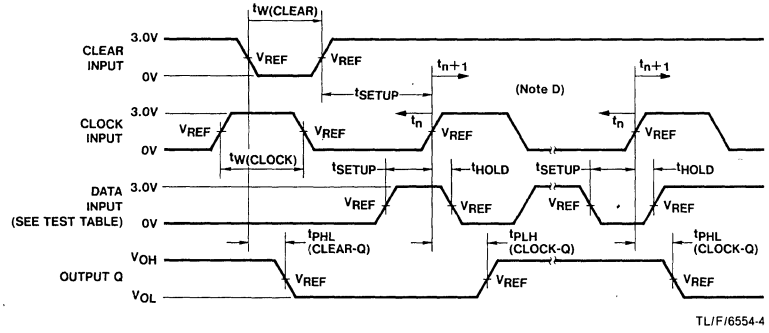
Typical Clear, Shift, Load, Inhibit, and Shift Sequences



TL/F/6554-3

Parameter Measurement Information

Voltage Waveforms



TL/F/6554-4

Test Table For Synchronous Inputs

Data Input For Test	Shift/Load	Output Tested (See Note C)
H Serial Input	0 V 4.5 V	Q_H at T_{N+1} Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns. When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

Note E: V_{REF} = 1.5 V for 166

National Semiconductor

DM74170 4 by 4 Register Files

General Description

These 16-bit TTL register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location and reading from another word location, simultaneously.

Four data inputs are available to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct reading of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 ns typical) and the read time (25 ns typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one standard load. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- Separate addressing permits simultaneous reading and writing
- Fast access times typically 20 ns
- Organized as 4 words of 4 bits
- Expandable to 1024 words of n-bits
- For use as:
  - Scratch-pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Open-collector outputs with low maximum off-state current:
  - 170 30 μA
- DM54LS670 and DM74LS670 are similar but have TRI-STATE outputs

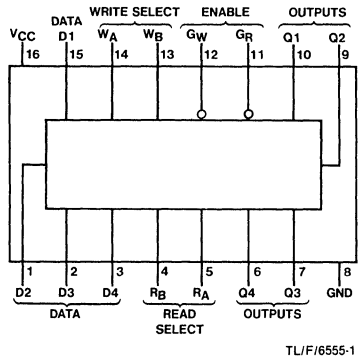
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6555-1

74170 (N)

Function Tables

WRITE TABLE (SEE NOTES A, B, AND C)

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (SEE NOTES A AND D)

Read Inputs			Outputs			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

Note A: H = High Level, L = Low Level, X = Don't Care

Note B: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Note C: Q_0 = The level of Q before the indicated input conditions were established.

Note D: W0B1 = The first bit of word 0, etc.

Recommended Operating Conditions

Symbol	Parameter		DM74170			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage				5.5	V
I_{OL}	Low Level Output Current				16	mA
t_W	Pulse Width	Write-Enable	25			ns
		Read-Enable	25			
t_{SU}	Setup Time (Note 1)	Data	10			ns
		Select	15			
t_H	Hold Time (Note 1)	Data	15			ns
		Select	5			
t_{LAT}	Latch Time for New Data (Note 2)		40			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			30	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)		127	150	mA

Note 1: Times are with respect to the Write-Enable input.

Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

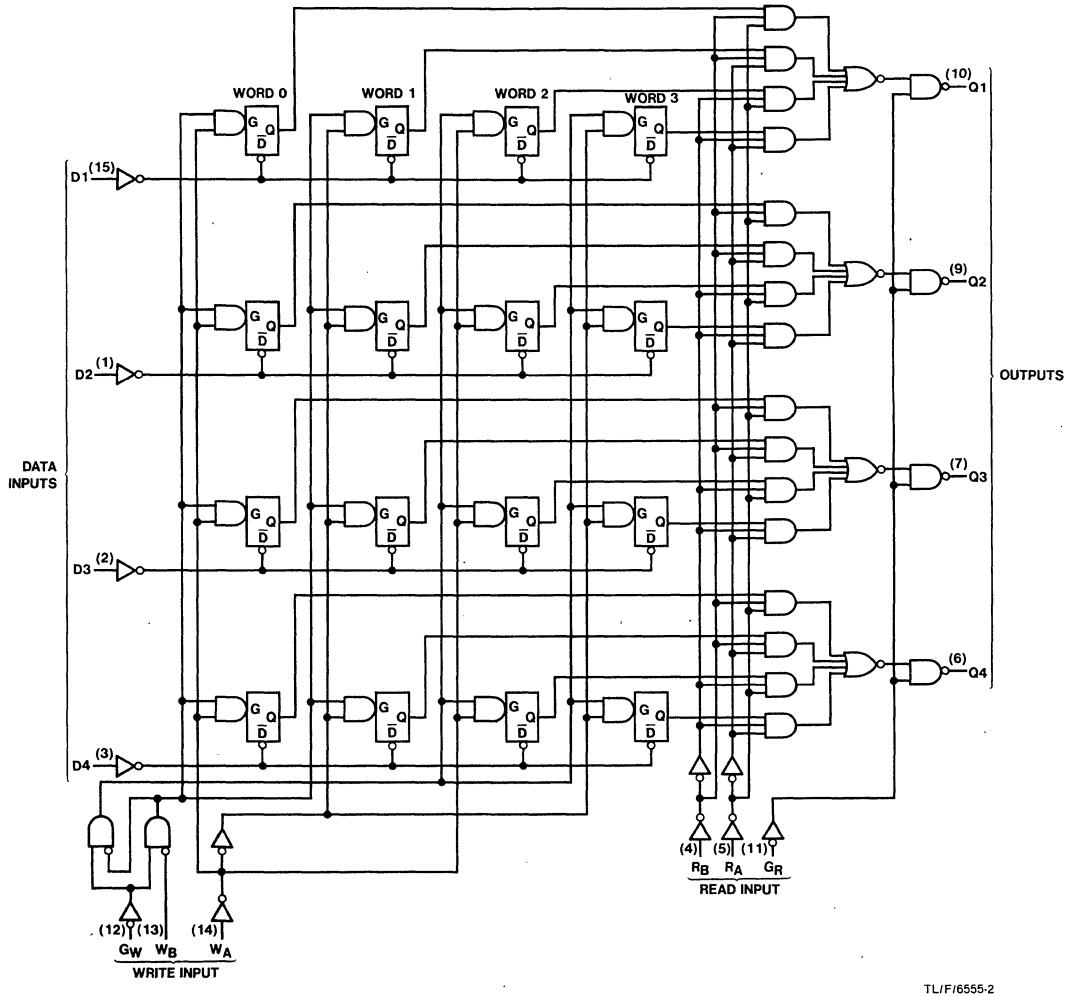
Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: I_{CC} is measured with all DATA and ENABLE inputs at 4.5V, all ADDRESS inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Read Enable to Any Q		17	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Read Enable to Any Q		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Read Select to Any Q		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Read Select to Any Q		30	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Write Enable to Any Q		25	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Write Enable to Any Q		34	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		30	45	ns

Logic Diagram



National Semiconductor

DM54173/DM74173 TRI-STATE® Quad D Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 18 ns
- Typical frequency 30 MHz
- Typical power dissipation 250 mW

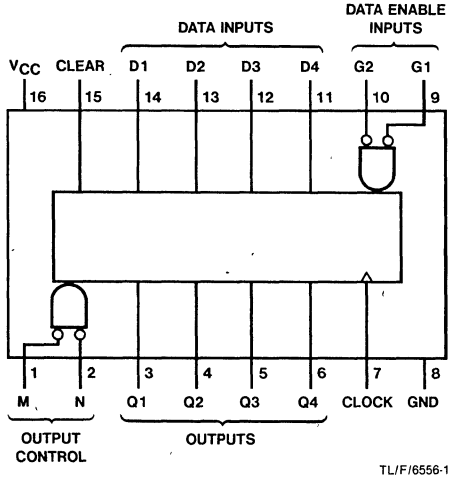
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6556-1

54173 (J) **74173 (N)**

Function Table

Inputs					Output Q
Clear	Clock	Data Enable G1	Data Enable G2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Recommended Operating Conditions

Sym	Parameter		DM54173			DM74173			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	Enable	17			17			ns
		Data	10			10			
t_H	Hold Time	Enable	2			2			ns
		Data	10			10			
t_{REL}	Clear Release Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	72	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

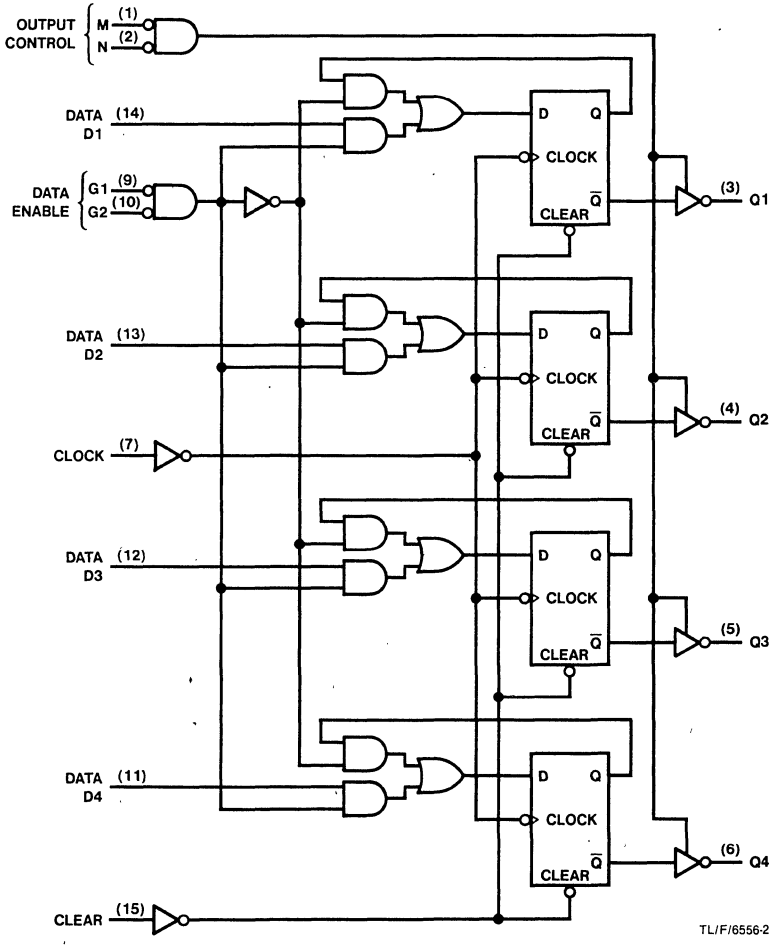
Note 3: I_{CC} is measured with all outputs open, CLEAR grounded after a momentary connection to 4.5V: N, G1, G2 and all DATA inputs grounded: and the CLOCK input and M input at 4.5V.

6

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency					25	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output					16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output					20	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output					18	27	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q				7	16	30	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q				7	21	30	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q	3	5	14				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q	3	11	20				ns

Logic Diagram



National Semiconductor

DM54174/DM74174, DM54175/DM74175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup and hold time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- 174 contains six flip-flops with single-rail outputs.
- 175 contains four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs.
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 38 mW

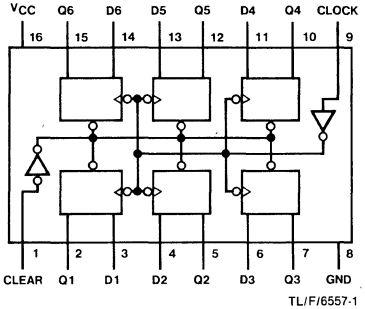
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

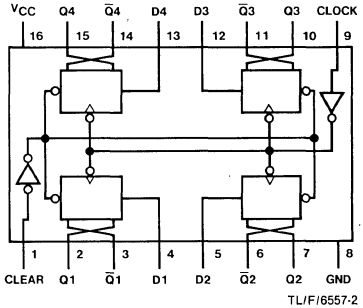
Dual-In-Line Package



TL/F/6557-1

54174 (J) **74174 (N)**

Dual-In-Line Package



TL/F/6557-2

54175 (J) **74175 (N)**

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	Q̄†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175 only

Recommended Operating Conditions

Sym	Parameter		DM54174			DM74174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		30	0		30	MHz
t_W	Pulse Width	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Data Hold Time		0			0			ns
t_{REL}	Clear Release Time		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'174 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and all DATA and CLEAR inputs at 4.5V, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

'174 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		14	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		17	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		30	40	ns

Recommended Operating Conditions

Sym	Parameter		DM54175			DM74175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		30	0		30	MHz
t_W	Pulse Width	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Data Hold Time		0			0			ns
t_{REL}	Clear Release Time		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'175 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				− 1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	− 20		− 57	mA
			DM74	− 18		− 57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	45	mA

'175 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		14	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to Any Q		14	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		30	40	ns

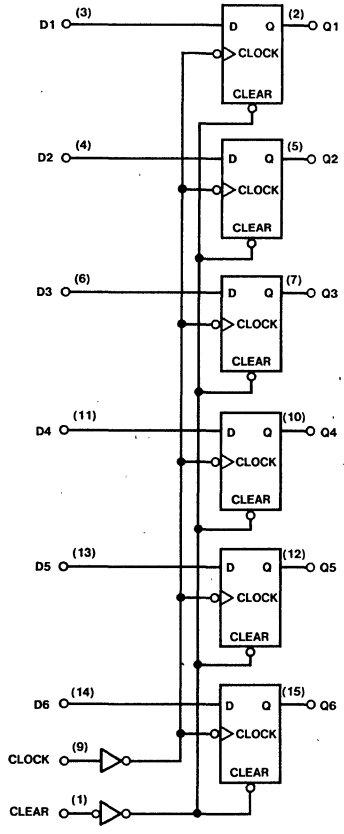
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground then 4.5V applied to the CLOCK.

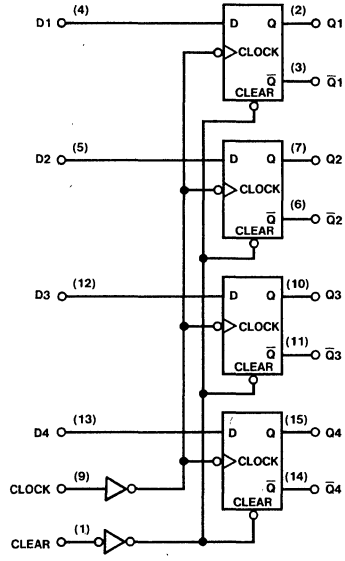
Logic Diagrams

174



TL/F/6557-3

175



TL/F/6557-4

National Semiconductor

DM54176/DM74176, DM54177/DM74177 Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (176) or a divide-by-two and a divide-by-eight counter (177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive. (Continued)

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input
- Typical count frequency
  - Clock 1 50 MHz
  - Clock 2 25 MHz
- Typical power dissipation 150 mW

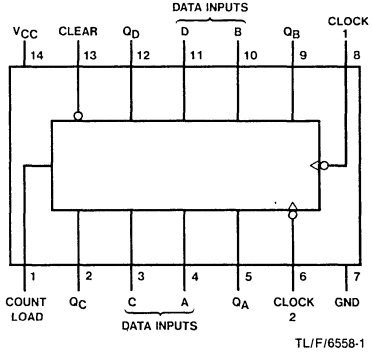
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6558-1

Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

54176 (J) **74176 (N)**
54177 (J) **74177 (N)**

General Description (Continued)

TYPICAL COUNT CONFIGURATIONS 176

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the biquinary function table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

177

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C and Q_D outputs as shown in the function table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Function Tables

176
Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

176
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

177
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Level, L = Low Level

Note A: Output Q_A connected to clock-2 input.
Note B: Output Q_D connected to clock-1 input.

Recommended Operating Conditions

Sym	Parameter		DM54176			DM74176			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Clock 1)		0		35	0		35	MHz
t_W	Pulse Width	Clock 1	14			14			ns
		Clock 2	28			28			
		Clear	25			25			
		Load	20			20			
t_{SU}	Setup Time	Data High	15			15			ns
		Data Low	20			20			
t_H	Data Hold Time		20			20			ns
t_{EN}	Count Enable Time (Note 1)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the count/load and clear inputs must both be high to ensure counting.

'176 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Count/Load			40	μA
			Data			40	
			Clear			80	
			Clock 1			80	
			Clock 2			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Count/Load			−1.6	mA
			Data			−1.6	
			Clear			−3.2	
			Clock 1			−4.8	
			Clock 2			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the Clock 2 input. This permits driving the Clock 2 input while maintaining full fan-out capability.

'176 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock 1 to Q_A	35	50		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		9	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		11	17	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		27	41	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		34	51	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		17	26	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		31	46	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		29	43	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		32	48	ns

Recommended Operating Conditions

Sym	Parameter		DM54177			DM74177			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Clock 1)		0		35	0		35	MHz
t_W	Pulse Width	Clock 1	14			14			ns
		Clock 2	28			28			
		Clear	25			25			
		Load	20			20			
t_{SU}	Setup Time	Data High	15			15			ns
		Data Low	20			20			
t_H	Hold Time		20			20			ns
t_{EN}	Count Enable Time (Note 1)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the count/load and clear inputs must both be high to ensure counting.

'177 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Count/Load			40	μA
			Data			40	
			Clear			80	
			Clock 1			80	
			Clock 2			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Count/Load			−1.6	mA
			Data			−1.6	
			Clear			−3.2	
			Clock 1			−4.8	
			Clock 2			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the Clock 2 input. This permits driving the Clock 2 input while maintaining full fan-out capability.

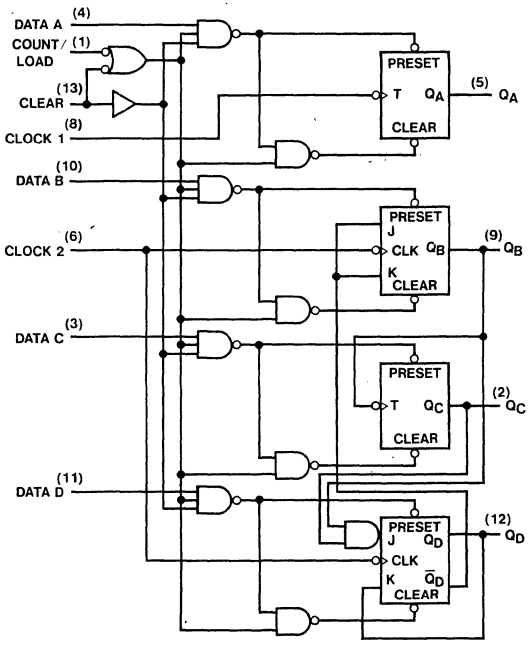
'177 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock 1 to Q_A	35	50		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		9	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		11	17	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		27	41	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		34	51	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		44	66	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		50	75	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		19	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		31	46	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		29	43	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		32	48	ns

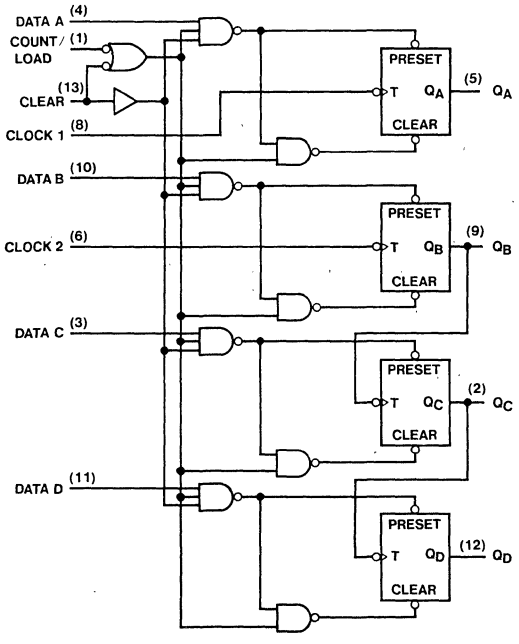
Logic Diagrams

'176



TL/F/6558-2

'177



TL/F/6558-3

6

National Semiconductor

DM54180/DM74180 9-Bit Parity Generators/Checkers

General Description

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

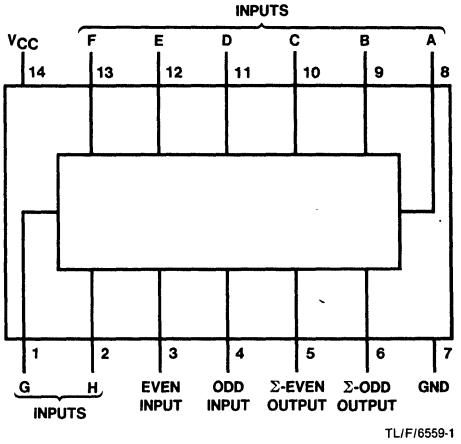
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6559-1

54180 (J) 74180 (N)

Function Table

Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Symbol	Parameter	DM54180			DM74180			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Odd or Even			80	μA
			Data			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Odd or Even			−3.2	mA
			Data			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

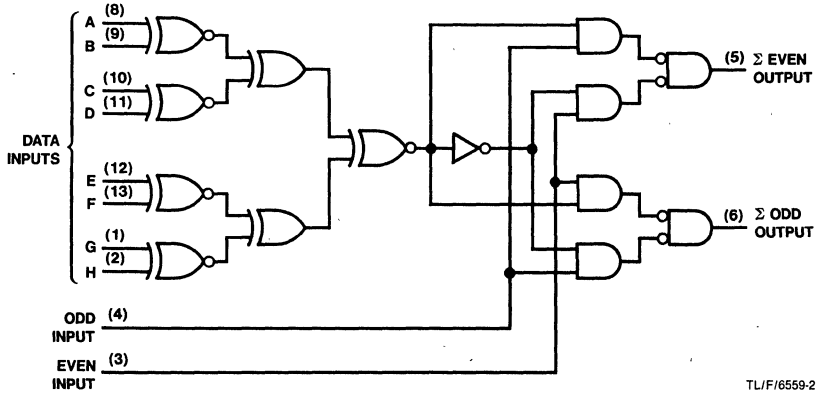
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with EVEN and ODD inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Σ Even	$C_L = 15$ pF, $R_L = 400\Omega$, Odd Input Low		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Σ Even			45	68	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Σ Odd			32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Σ Odd			25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Σ Even	$C_L = 15$ pF, $R_L = 400\Omega$, Odd Input High		32	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Σ Even			25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Σ Odd			40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Σ Odd			45	68	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Even or Odd to Σ Even or Σ Odd	$C_L = 15$ pF, $R_L = 400\Omega$		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Even or Odd to Σ Even or Σ Odd			7	10	ns

Logic Diagram



National Semiconductor

DM54181/DM74181
Arithmetic Logic Unit/Function Generators

General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182.

(Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

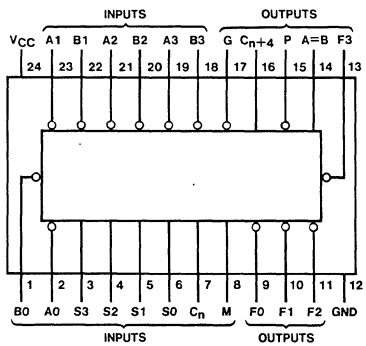
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6560-1

54181 (J) **74181 (N)**

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54181/DM74181 can be used with the signal designations of either *Figure 1* or *Figure 2.*

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table II)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_{n+4}	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

General Description (Continued)

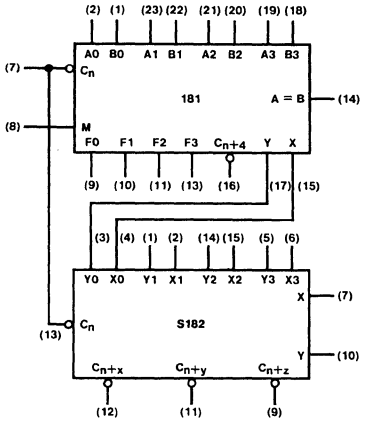


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Figure 1

Table I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	$F = A$ Plus $A\overline{B}$	$F = A$ Plus $A\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ Plus $A\overline{B}$	$F = (A + B)$ Plus $A\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F = (A + \overline{B})$ Plus AB	$F = (A + \overline{B})$ Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A + \overline{B}$	$F = (A + B)$ Plus A	$F = (A + B)$ Plus A Plus 1
H	H	H	L	$F = A + B$	$F = (A + \overline{B})$ Plus A	$F = (A + \overline{B})$ Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

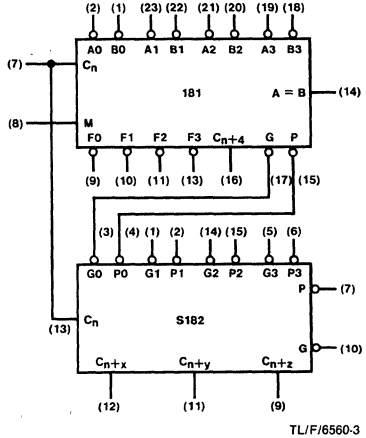

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Figure 2

Table II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus $(A + \overline{B})$	F = A Plus $(A + \overline{B})$ Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus $(A + B)$	F = AB Plus $(A + \overline{B})$ Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
H	L	L	L	$F = \overline{AB}$	F = A Plus $(A + B)$	F = A Plus $(A + B)$ Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F = A\overline{B}$ Plus $(A + B)$	$F = A\overline{B}$ Plus $(A + B)$ Plus 1
H	L	H	H	$F = A + B$	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	$F = A\overline{B}$ Plus A	$F = A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

6

Recommended Operating Conditions

Symbol	Parameter	DM54181			DM74181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5			5.5	V
I_{OH}	High Level Output Current (All except A = B)			−800			−800	μA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OH}	High Level Output Voltage (All except A = B)			2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			40	μA
			A or B			120	
			S			160	
			Carry			200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Mode			−1.6	mA
			A or B			−4.8	
			S			−6.4	
			Carry			−8	
I_{OS}	Short Circuit Output Current (All except A = B)	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC1}	Supply Current With Outputs High	V_{CC} = Max (Note 3)	DM54		88	127	mA
			DM74		88	140	
I_{CC2}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)	DM54		92	135	mA
			DM74		92	150	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

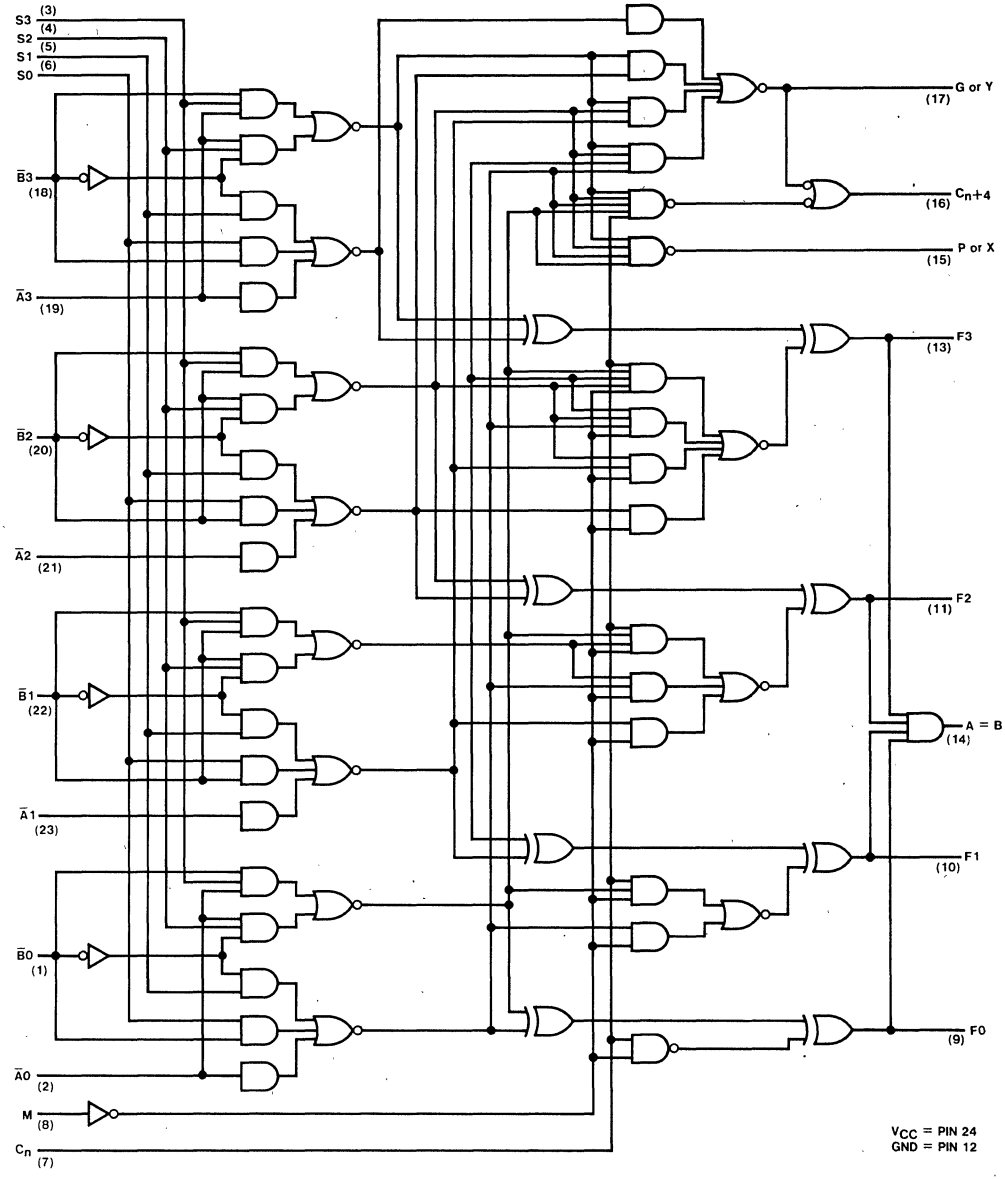
Note 3: I_{CC1} is measured with S0 through S3, M, and A inputs at 4.5V, all other inputs grounded, and all outputs open.

Note 4: I_{CC2} is measured with S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54/74 181 R_L = 400 Ω, C_L = 15 pF			Units
					Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+4}			9	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22	33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22	33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		11	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		12	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					17	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					17	25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0 V, S0 = S3 = 4.5 V S1 = S2 = 0 V ($\overline{SUM}$ mode)		18	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		14	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5 V (logic mode)		17	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		26	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	40	

Logic Diagram



Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}							
t_{PLH}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All A	All B	Any F or C_{n+4}	In-Phase
t_{PHL}							
t_{PLH}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase

National Semiconductor

DM54184/DM74184, DM54185A/DM74185A BCD-to Binary and Binary-to-BCD Converters

General Description

These monolithic converters are derived from the 256-bit read only memories, DM5488 and DM7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1, as shown in the function tables. These converters demonstrate the versatility of a read only memory in that an unlimited number of reference tables or conversion tables may be built into a system. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high. The outputs are of the open-collector type.

DM54184 AND DM74184 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM54184 and DM74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM54184 and DM74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7 and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table when the devices are connected as shown.

DM54185A AND DM74185A BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

(Continued)

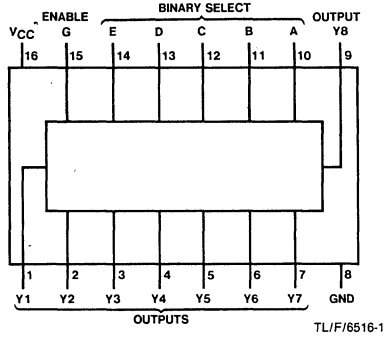
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6516-1

54184 (J) **74184 (N)**
54185A (J) **74185A (N)**

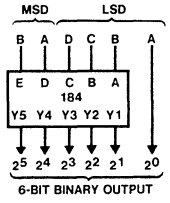
General Description (Continued)

DM54184 AND DM74184 BCD-TO-BINARY

TABLE I
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

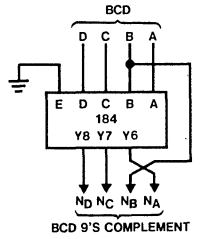
Input (Decades)	Packages Required	Total Delay Times (ns)	
		Typ	Max
2	2	56	80
3	6	140	200
4	12	196	280
5	19	280	400
6	28	364	520

6-Bit Converter



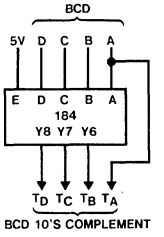
TL/F/6516-2

BCD 9's Complement Converter



TL/F/6516-3

BCD's 10's Complement Converter



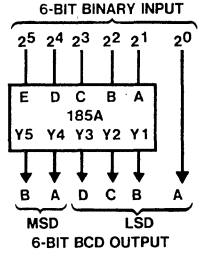
TL/F/6516-4

DM54185A AND DM74185A BINARY-TO-BCD

TABLE II
PACKAGE COUNT AND DELAY TIMES
FOR BINARY-TO-BCD CONVERSION

Input (Bits)	Packages Required	Total Delay Times (ns)	
		Typ	Max
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-Bit Converter



TL/F/6516-5

Function Tables

Binary Words		Inputs						Outputs							
		Binary Select					Enable								
		E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2	3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6	7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10	11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12	13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14	15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16	17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18	19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20	21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22	23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24	25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26	27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28	29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30	31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32	33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34	35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36	37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38	39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40	41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42	42	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44	45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46	47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48	49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50	51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52	53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54	55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56	57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58	59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60	61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62	63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL		X	X	X	X	X	H	H	H	H	H	H	H	H	H

BCD-TO-BINARY CONVERTER

BCD WORDS		Inputs (See Note A)						Outputs (See Note B)				
		E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	L	L	L	L	L
2	3	L	L	L	L	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	L	L	L	H	L
6	7	L	L	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	L	L	H	L	L
10	11	L	H	L	L	L	L	L	L	H	L	H
12	13	L	H	L	L	H	L	L	L	H	H	L
14	15	L	H	L	H	L	L	L	L	H	H	H
16	17	L	H	L	H	H	L	L	H	L	L	L
18	19	L	H	H	L	L	L	L	H	L	L	H
20	21	H	L	L	L	L	L	L	H	L	H	L
22	23	H	L	L	L	H	L	L	H	L	H	H
24	25	H	L	L	H	L	L	L	H	H	L	L
26	27	H	L	L	H	H	L	L	H	H	L	H
28	29	H	L	H	L	L	L	L	H	H	H	L
30	31	H	H	L	L	L	L	L	H	H	H	H
32	33	H	H	L	L	H	L	H	L	L	L	L
34	35	H	H	L	H	L	L	H	L	L	L	H
36	37	H	H	L	H	H	L	H	L	L	H	L
38	39	H	H	H	L	L	L	H	L	L	H	H
ANY		X	X	X	X	X	H	H	H	H	H	H

BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	Inputs (See Note C)						Outputs (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	L	H
7	H	L	H	H	H	L	L	L	L
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Note A: Input Conditions other than those shown produce highs at outputs Y1 through Y5.

Note B: Output Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

Note C: Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

Note D: Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

Recommended Operating Conditions

Symbol	Parameter	DM54184, 185A			DM74184, 185A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			12	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'184 and '185A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		65	95	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		80	99	mA

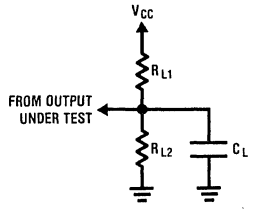
'184 and '185A Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_{L1} = 400Ω, R_{L2} = 600Ω C_L = 15 pF (See Test Circuit)			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Enable G to Output		20	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable G to Output		20	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Binary Select to Output		20	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Binary Select to Output		20	35	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Test Circuit



C_L includes probe and jig capacitance

Typical Applications

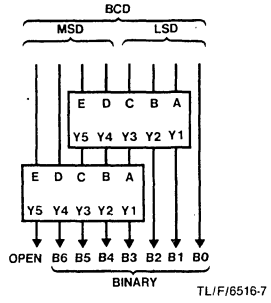


FIGURE 1. BCD-to-Binary Converter For Two BCD Decades

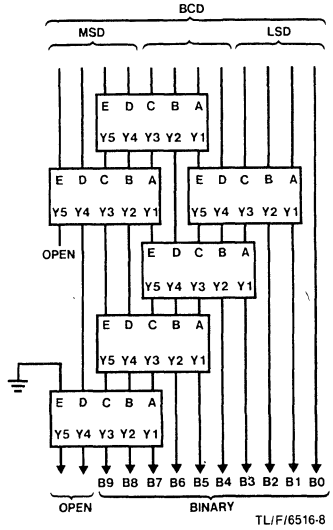


FIGURE 2. BCD-to-Binary Converter For Three BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM54184 or DM74184

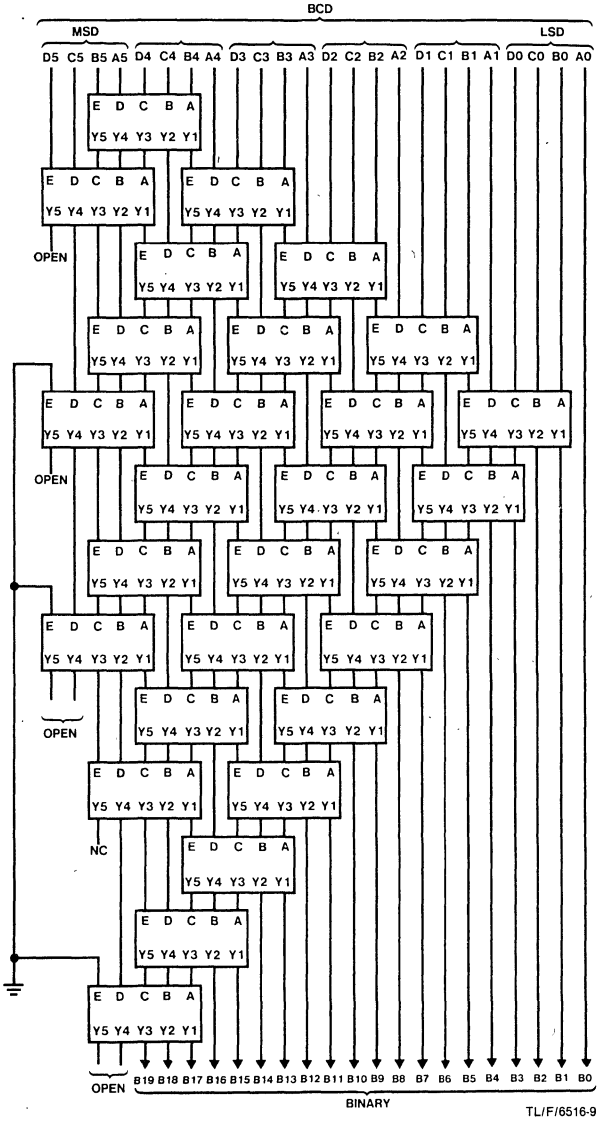


FIGURE 3. BCD-to-Binary Converter For Six BCD Decades

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Typical Applications (Continued)

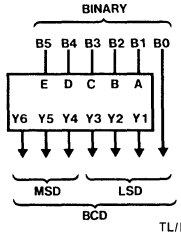


FIGURE 4. 6-Bit Binary-to-BCD Converter

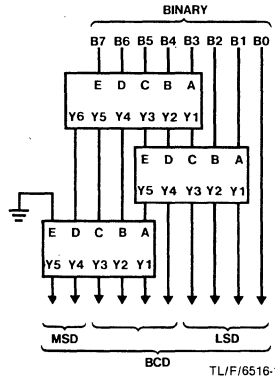


FIGURE 5. 8-Bit Binary-to-BCD Converter

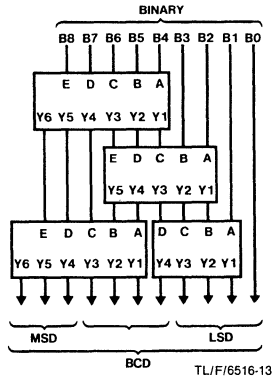


FIGURE 6. 9-Bit Binary-to-BCD Converter

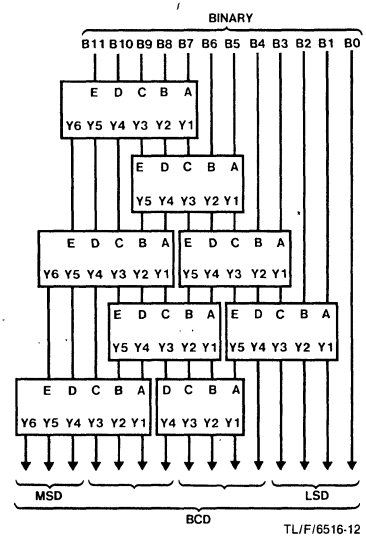


FIGURE 7. 12-Bit Binary-to-BCD Converter (See Note B)

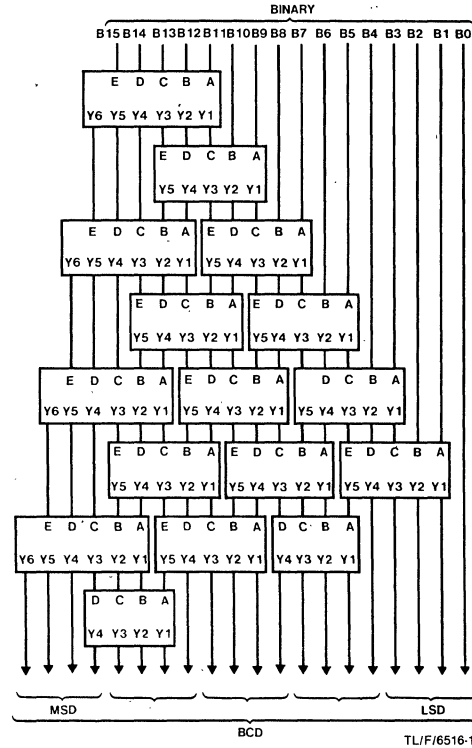


FIGURE 8. 16-Bit Binary-to-BCD Converter (See Note B)

MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM54185A or a DM74185A.
Note B: All unused E inputs are grounded.

National Semiconductor

DM54190/DM74190, DM54191/DM74191 Synchronous Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The 191 is a 4-bit binary counter and the 190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 325 mW

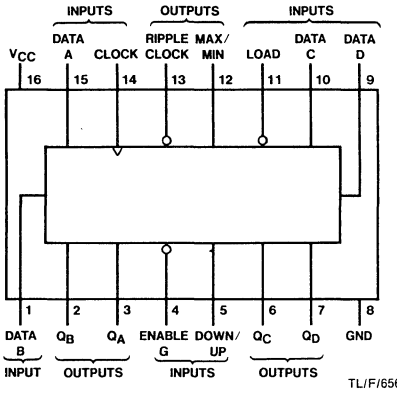
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6562-1

Asynchronous inputs: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

54190 (J) **74190 (N)**
54191 (J) **74191 (N)**

Recommended Operating Conditions

Sym	Parameter		DM54190, 191			DM74190, 191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time		28			28			ns
t_H	Hold Time		0			0			ns
t_{REL}	Load Release Time		30			30			nS
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'190 and '191 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Enable			120	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable			−4.8	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−65	mA
			DM74	−18		−65	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	99	mA
			DM74		65	105	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

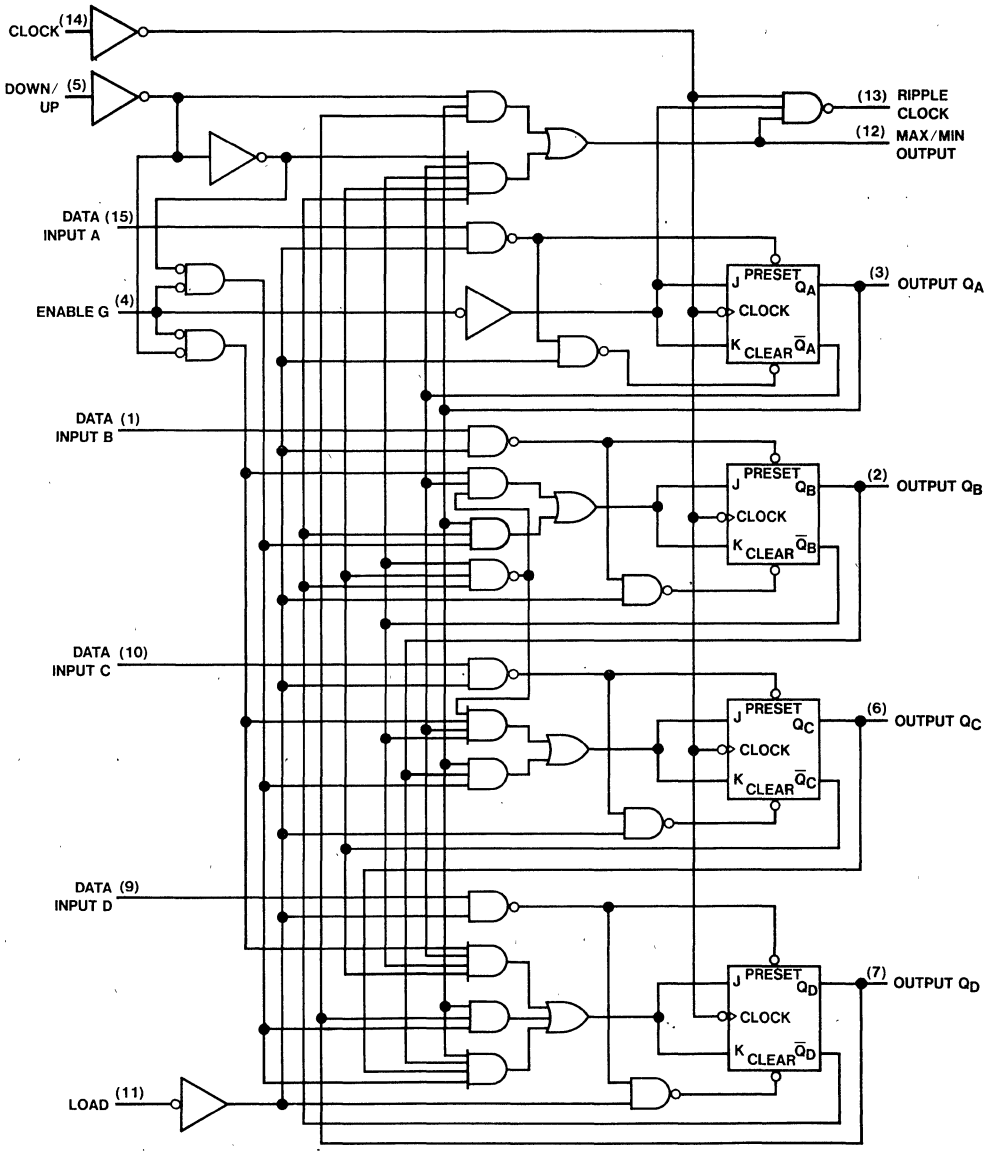
'190 and '191 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		48	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		46	70	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		24	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Max/Min		28	42	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Max/Min		37	52	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Down/Up to Ripple Carry		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Down/Up to Ripple Carry		30	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		21	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		22	33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable G to Ripple Carry			24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable G to Ripple Carry			24	ns

Logic Diagrams

190 Decade Counter

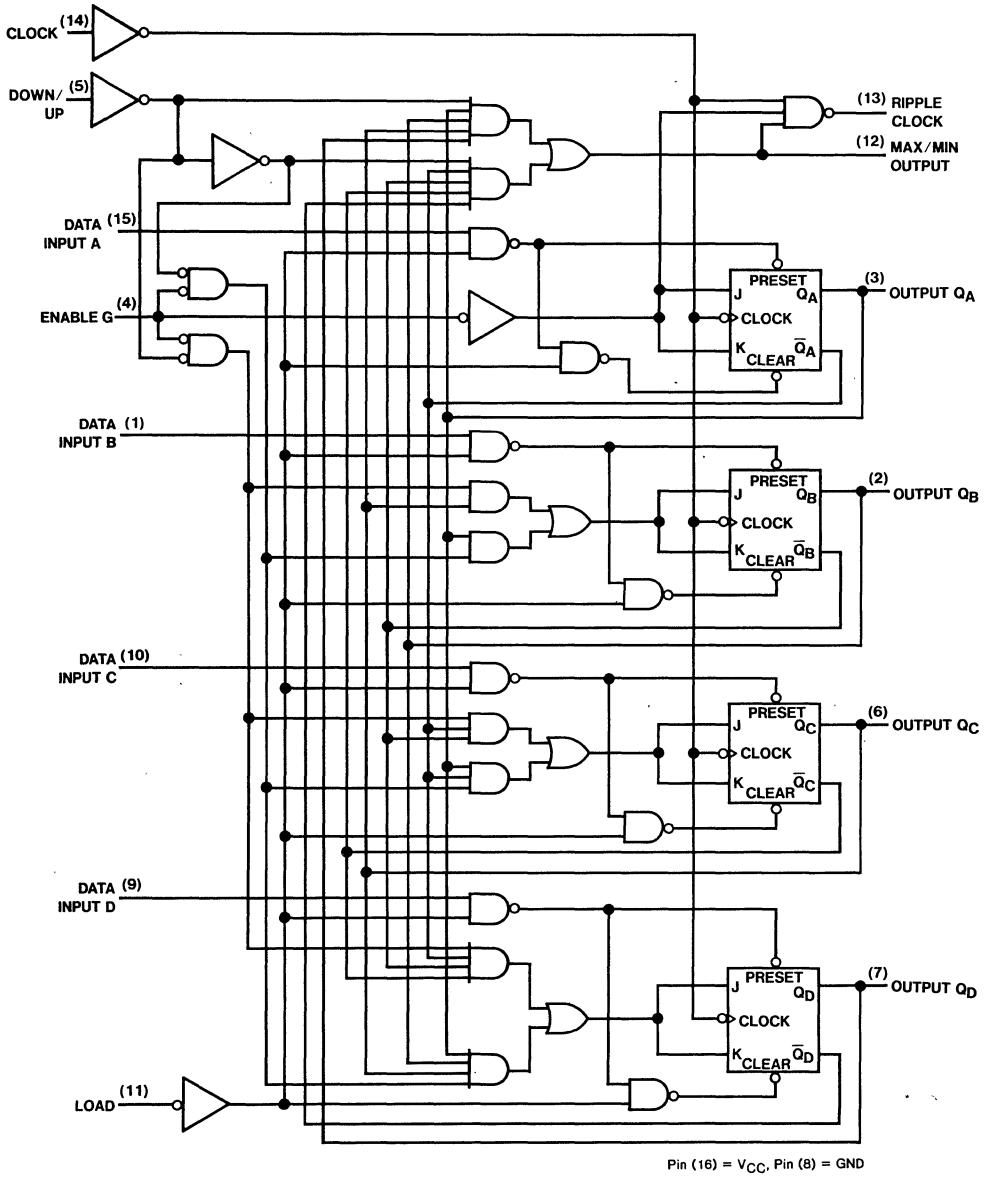


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6562-2

Logic Diagrams (Continued)

191 Binary Counter



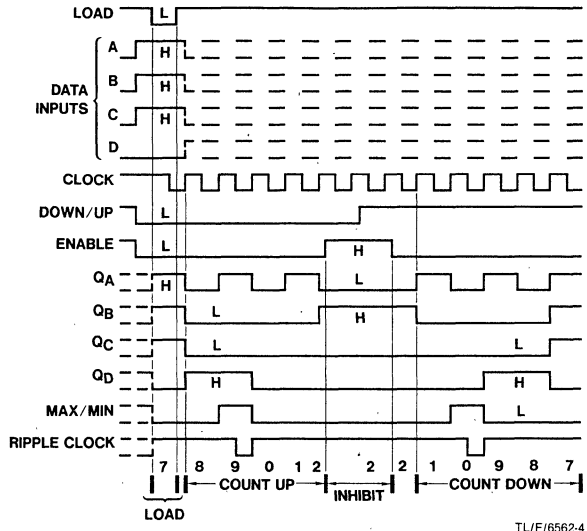
Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6562-3

6

Timing Diagrams

190 Decade Counter
Typical Load, Count, and Inhibit Sequences



TL/F/6562-4

Sequence:

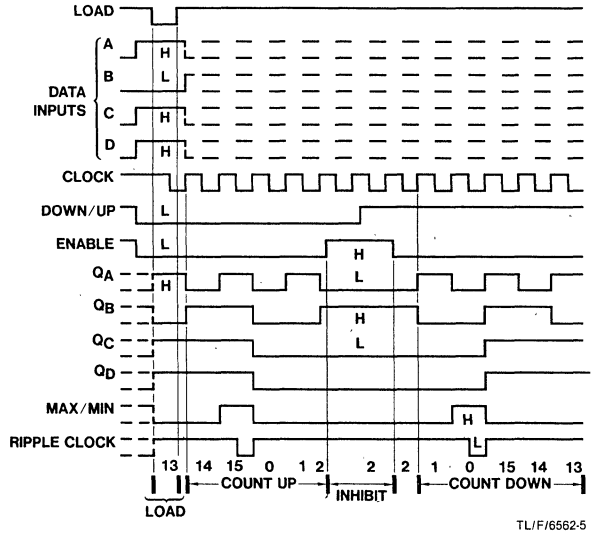
(1) Load (preset) to BCD seven

(2) Count up to eight, nine, zero, one, and two

(3) Inhibit

(4) Count down to one, zero, nine, eight, and seven

191 Decade Counter
Typical Load, Count, and Inhibit Sequences



TL/F/6562-5

Sequence:

(1) Load (preset) to binary thirteen

(2) Count up to fourteen, fifteen, zero, one, and two

(3) Inhibit

(4) Count down to one, zero, fifteen, fourteen, and thirteen

National Semiconductor

DM54192/DM74192, DM54193/DM74193 Synchronous Up/Down Counters with Dual Clock

General Description

These circuits are synchronous up/down counters; the 192 circuit is a BCD counter and the 193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop
- Typical count frequency 25 MHz
- Typical power dissipation 325 mW

Absolute Maximum Ratings (Note 1)

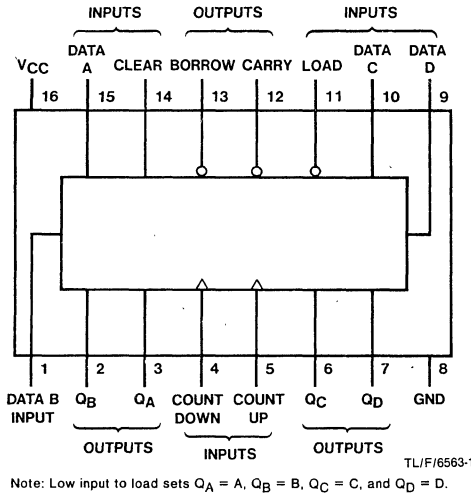
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

6

Connection Diagram

Dual-In-Line Package



TL/F/6563-1

54192 (J) 74192 (N)
54193 (J) 74193 (N)

Note: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D.

Recommended Operating Conditions

Sym	Parameter		DM54192			DM74192			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	25	20	0	25	20	MHz
t_W	Pulse Width	Clock Low	30			30			ns
		Clock, Clear High Load Low	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'192 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	89	mA
			DM74		65	102	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

'192 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count to Q		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count to Q		31	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Q		27	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Q		29	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		22	35	ns

Recommended Operating Conditions

Sym	Parameter		DM54193			DM74193			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	25	20	0	25	20	MHz
t_W	Pulse Width	Clock Low	30			30			ns
		Clock, Clear High Load Low	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'193 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	89	mA
			DM74		65	102	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

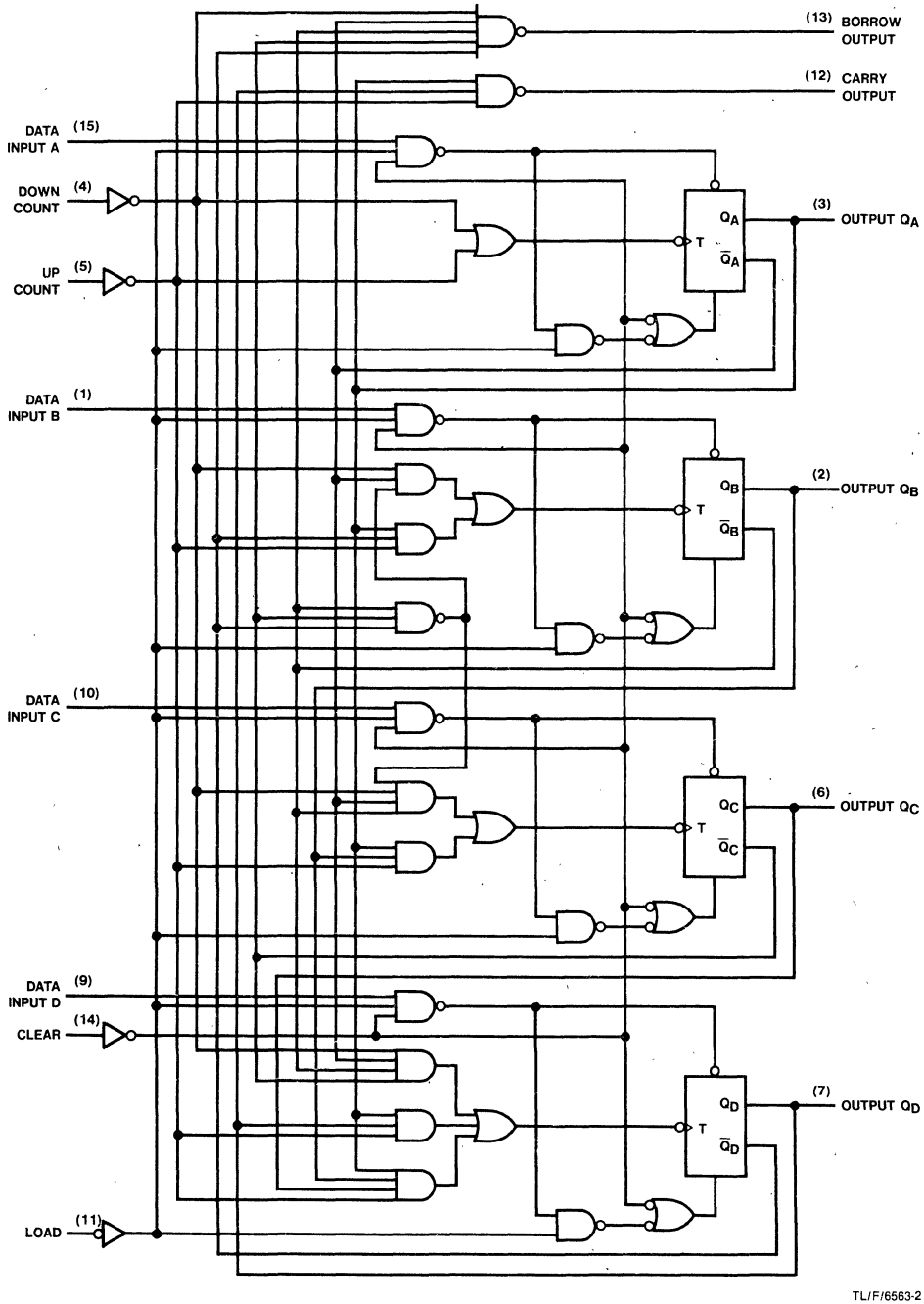
'193 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Either Count to Q		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Either Count to Q		31	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Q		27	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Q		29	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		22	35	ns

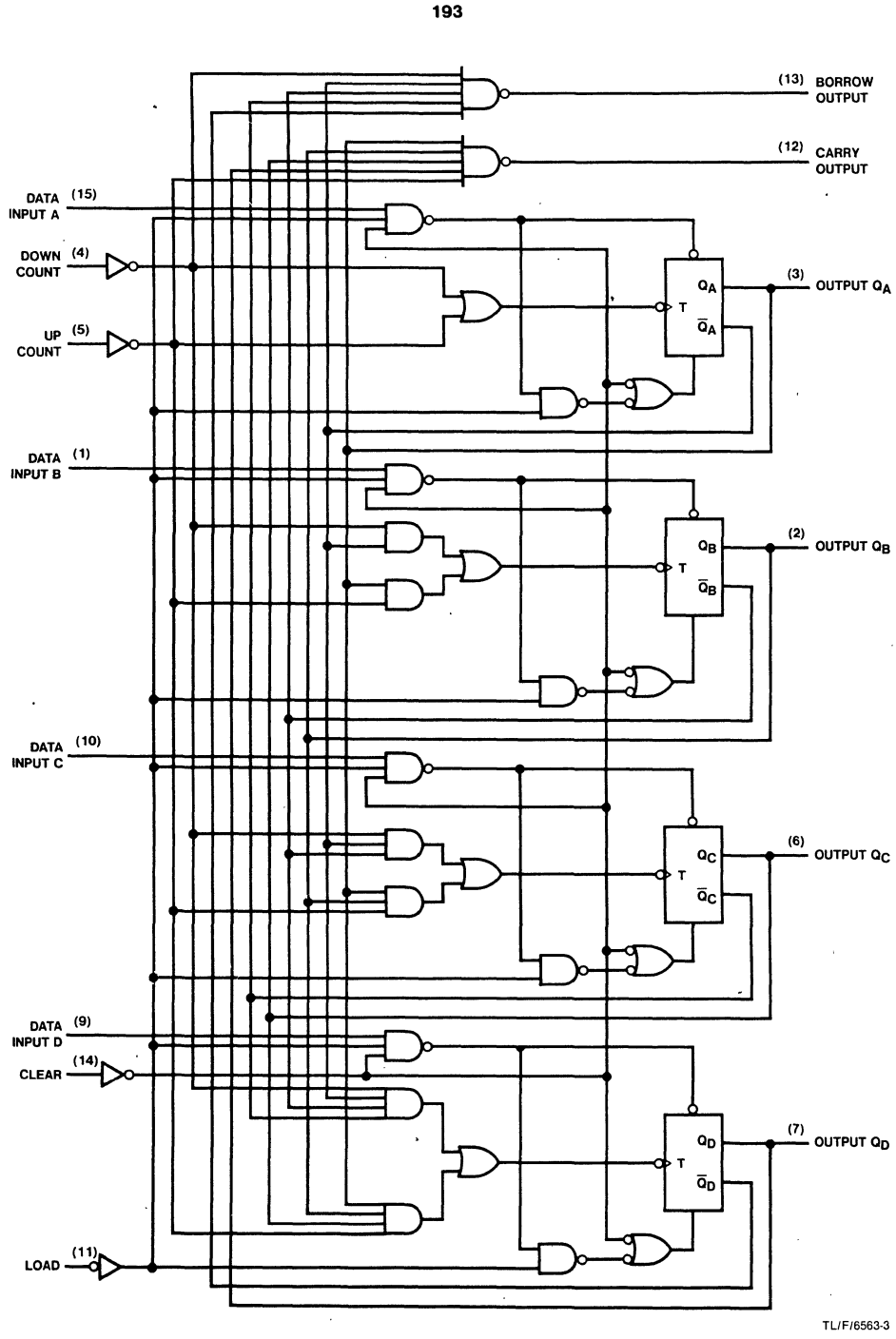
Logic Diagrams

192



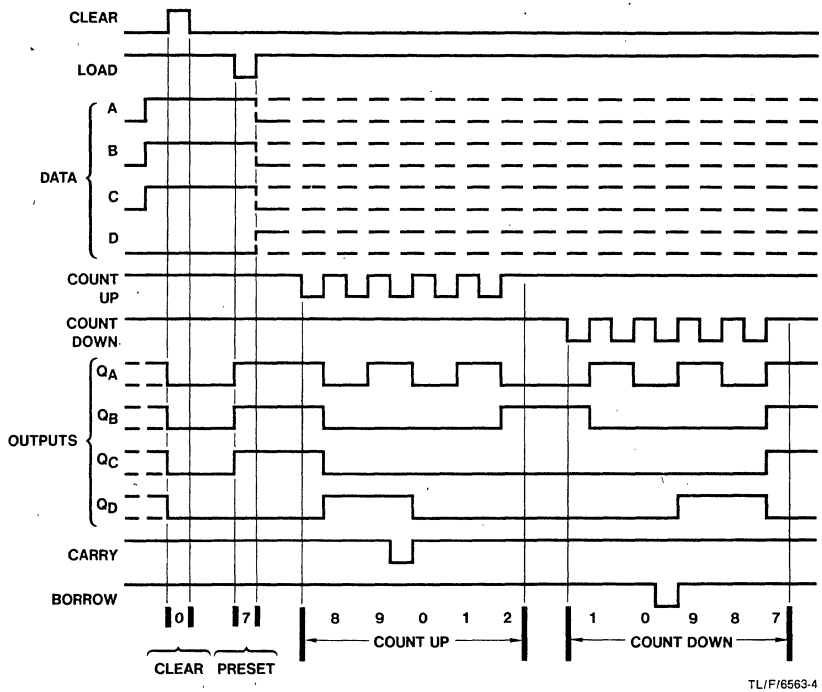
TL/F/6563-2

Logic Diagrams (Continued)



Timing Diagrams

192 DECADE COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



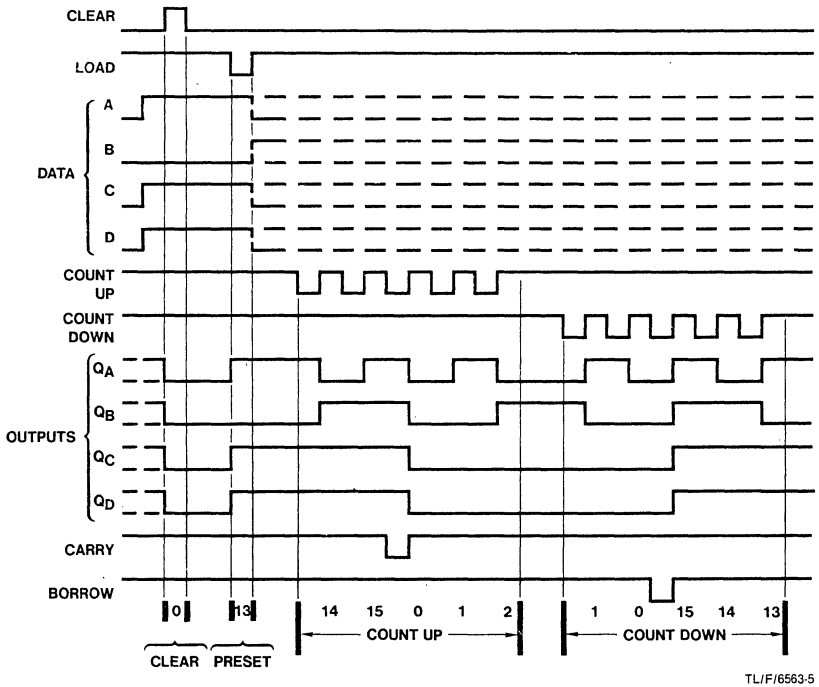
TL/F/6563-4

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

193 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



TL/F/6563-5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

6

National Semiconductor

DM54194/DM74194 4-Bit Bidirectional Universal Shift Registers

General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the of the DM54194/DM74194 should be changed only while the clock input is high.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 36 MHz
- Typical power dissipation 195 mW

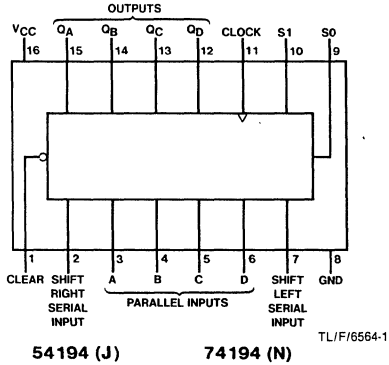
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6564-1

54194 (J) **74194 (N)**

Recommended Operating Conditions

Sym	Parameter		DM54194			DM74194			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	36	25	0	36	25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time		0			0			ns
t_{REL}	Clear Release Time		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			39	63	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	36		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		19	30	ns

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

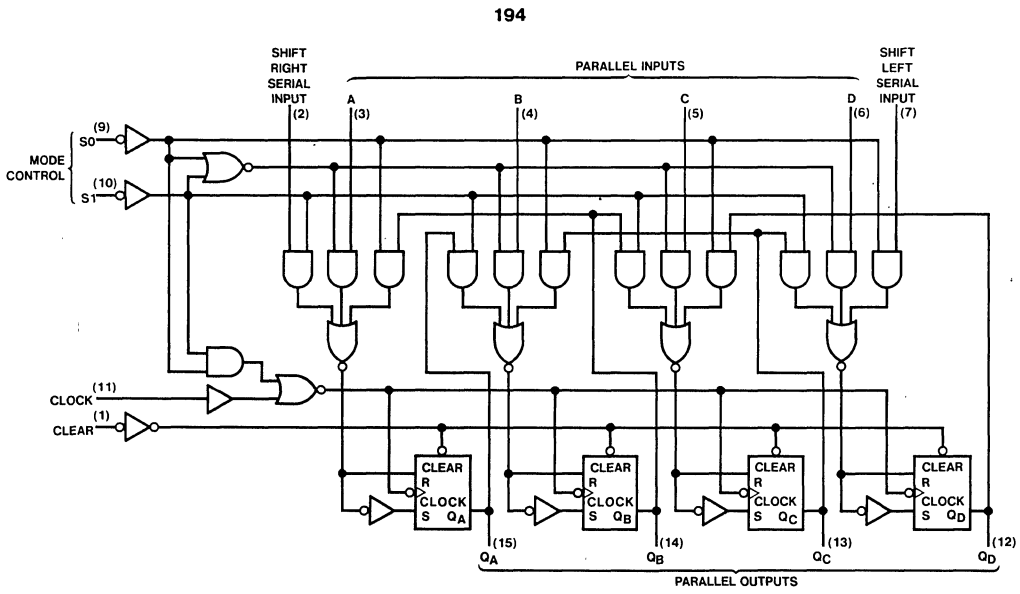
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

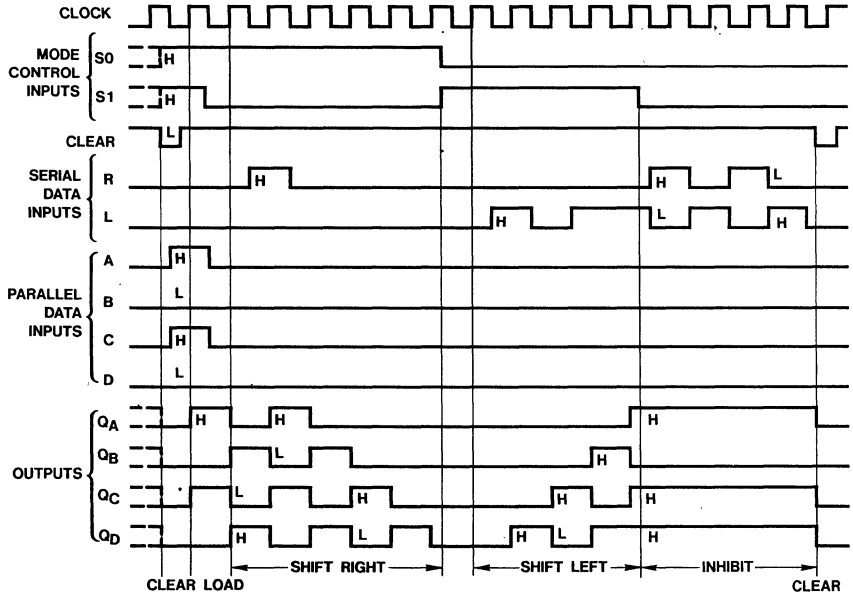
Logic Diagram



TL/F/6564-2

Timing Diagram

TYPICAL CLEAR, LOAD , RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



TL/F/6564-3

6

National Semiconductor

DM54195/DM74195 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the function table.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 39 MHz
- Typical power dissipation 195 mW

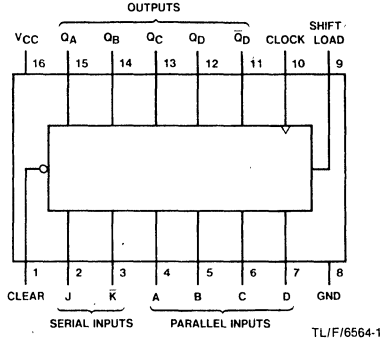
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6564-1

54195 (J) **74195 (N)**

Recommended Operating Conditions

Sym	Parameter		DM54195			DM74195			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	39	30	0	39	30	MHz
t_W	Pulse Width	Clock	16			16			ns
		Clear Low	12			12			
t_{SU}	Setup Time	Shift/Load	25			25			ns
		Data	15			15			
t_H	Hold Time		0			0			ns
t_{REL}	Release Time	Shift/Load	10			10			ns
		Clear	25			25			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			39	63	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, $\overline{K}$, and DATA inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to CLEAR and then a momentary ground then 4.5V applied to the CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	39		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		19	30	ns

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

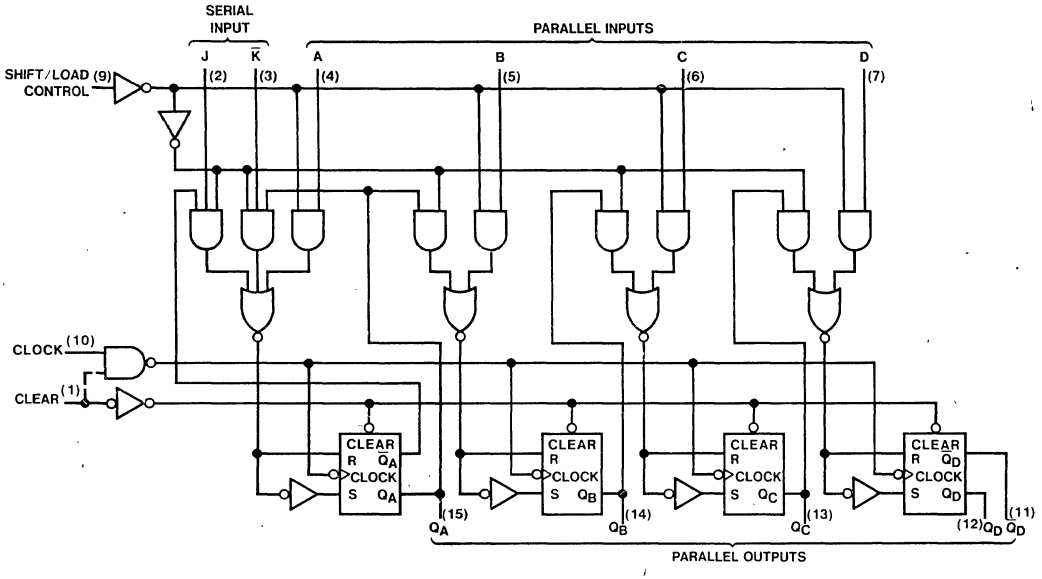
↑ = Transition from low to high level

a,b,c,d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

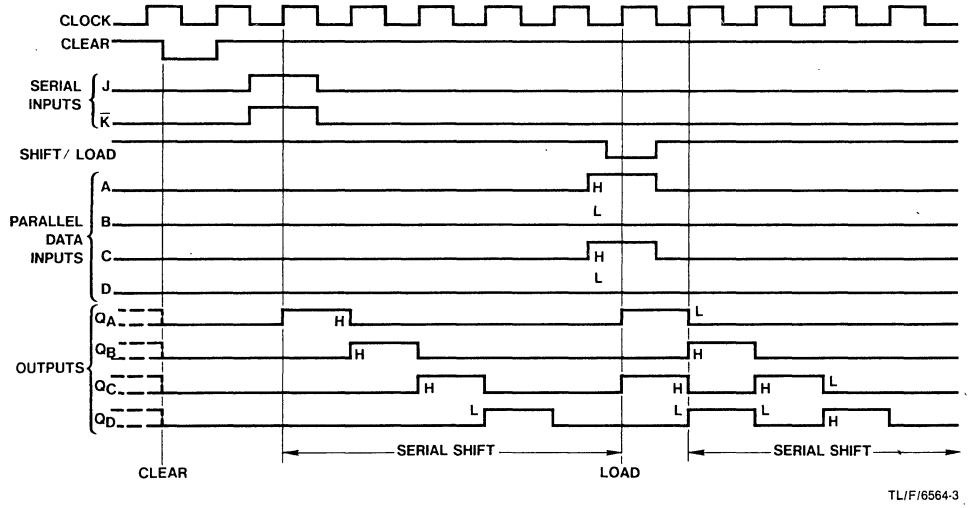
Logic Diagram



TL/F/6564-2

Timing Diagram

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



TL/F/6564-3

National Semiconductor

DM54196/DM74196, DM54197/DM74197 Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (196) or a divide-by-two and a divide-by-eight counter (197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive. (Continued)

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input
- Typical count frequency
  - Clock 1 50 MHz
  - Clock 2 25 MHz
- Typical power dissipation 240 mW

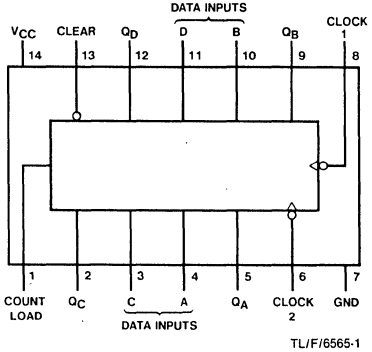
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6565-1

Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

54196 (J) 74196 (N)
54197 (J) 74197 (N)

General Description (Continued)

TYPICAL COUNT CONFIGURATIONS 196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the biquinary function table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

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The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C and Q_D outputs as shown in the function table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Function Tables

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Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = High Level, L = Low Level

Note A: Output Q_A connected to clock-2 input.
Note B: Output Q_D connected to clock-1 input.

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(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

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(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

6

Recommended Operating Conditions

Sym	Parameter		DM54196			DM74196			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−800			−800	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency	Clock 1	0	50	40	0	50	40	MHz
t_W	Pulse Width	Clock 1	14			14			ns
		Clock 2	28			28			
		Clear	25			25			
		Load	20			20			
t_{SU}	Setup Time	Data High	10			10			ns
		Data Low	15			15			
t_H	Hold Time	Data High	20			20			ns
		Data Low	20			20			
t_{ENABLE}	Count Enable Time (Note 1)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'196 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 5)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Clock 1			80	μA
			Clock 2			120	
			Clear			80	
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Clock 1			−4.8	mA
			Clock 2			−6.4	
			Clear			−3.2	
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)	DM54		39	54	mA
			DM74		39	54	

'196 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		40	50		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		9	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		11	16	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		16	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	ABCD to Any Q		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	ABCD to Any Q		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		25	37	ns

Note 1: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with all inputs grounded and all outputs open.

Note 5: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the CLOCK 2 input. This permits driving the CLOCK 2 input while maintaining full fan-out capability.

Recommended Operating Conditions

Sym	Parameter		DM54197			DM74197			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	50	40	0	50	40	MHz
t_W	Pulse Width	Clock 1	14			14			ns
		Clock 2	28			28			
		Clear	25			25			
		Load	20			20			
t_{SU}	Setup Time	Data High	10			10			ns
		Data Low	15			15			
t_H	Hold Time	Data High	20			20			ns
		Data Low	20			20			
t_{EN}	Count Enable Time (Note 1)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'197 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 5)			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Clock 1			80	μA
			Clock 2			80	
			Clear			80	
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Clock 1			−4.8	mA
			Clock 2			−3.2	
			Clear			−3.2	
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			39	54	mA

'197 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		40	50		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 1 to Q_A		9	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 1 to Q_A		11	16	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_B		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_B		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_C		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_C		28	42	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock 2 to Q_D		36	54	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock 2 to Q_D		42	63	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		24	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		25	37	ns

Note 1: Count enable time is the interval preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with all inputs grounded and all outputs open.

Note 5: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the CLOCK 2 input. This permits driving the CLOCK 2 input while maintaining full fan-out capability.

Logic Diagrams

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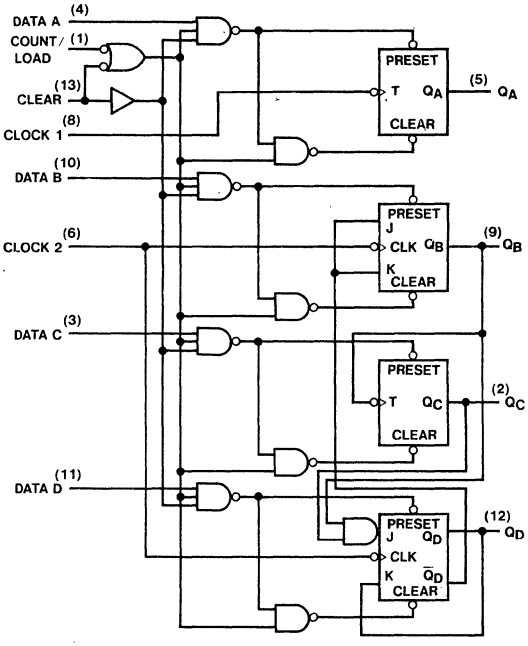

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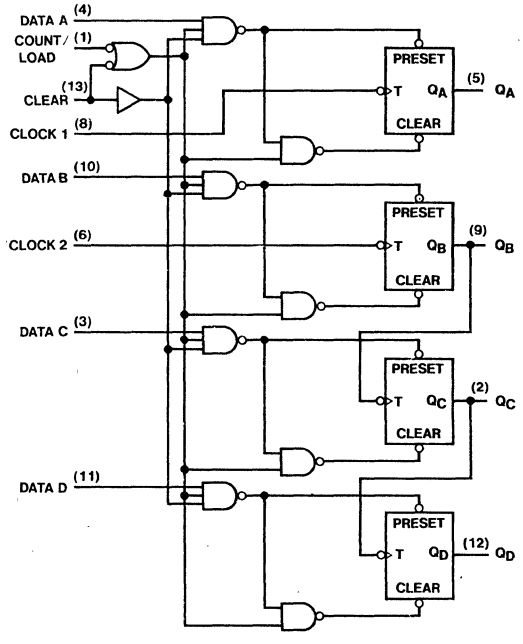


TL/F/6565-3

National Semiconductor

DM54198/DM74198, DM54199/DM74199 8-Bit Shift Registers

General Description

These 8-bit shift registers feature buffered inputs to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes to minimize switching transients and simplify system design. Maximum input clock frequency is typically 35 MHz and power dissipation is typically 360 mW.

DM54198/DM74198

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. They feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_H)
Shift left (in the direction Q_H toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S0 and S1 high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high. (Continued)

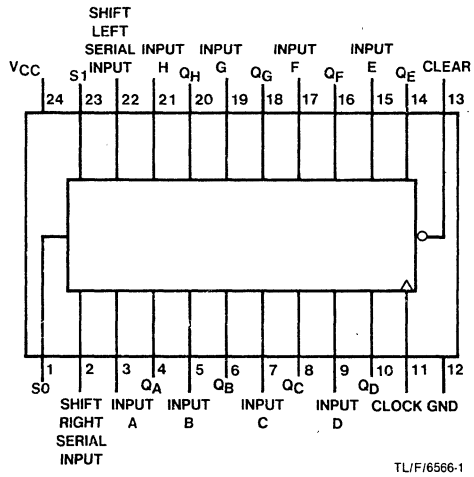
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



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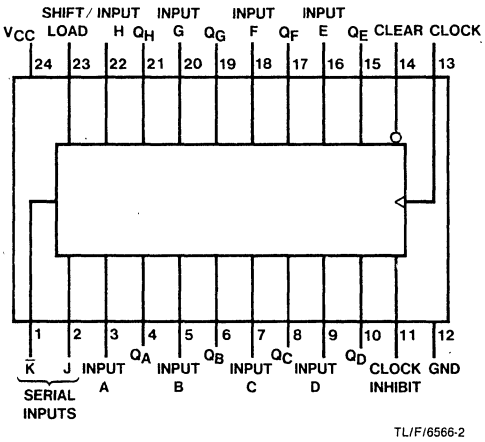
54198 (J) 74198 (N)

Dual-In-Line Package



TL/F/6566-2

54199 (J) 74199 (N)

General Description (Continued)

DM54199/DM74199

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_H)
Inhibit clock (do nothing)

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positve transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-K inputs. See the function table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either clock input high inhibits clocking; but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

Function Tables

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Inputs							Outputs				
Clear	Mode S1	Mode S0	Clock	Serial Left	Serial Right	Parallel A...H	Q_A	Q_B	...	Q_G	Q_H
L	X	X	X	X	X	X	L	L	...	L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}	...	Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a...h	a	b	...	g	h
H	L	H	↑	X	H	X	H	Q_{An}	...	Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}	...	Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}	...	Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}	...	Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}	...	Q_{G0}	Q_{H0}

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Inputs							Outputs				
Clear	Shift/ Load	Clock Inhibit	Clock	Serial J	Serial $\overline{K}$	Parallel A...H	Q_A	Q_B	Q_C	...	Q_H
L	X	X	X	X	X	X	L	L	L	...	L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	...	Q_{H0}
H	L	L	↑	X	X	a...h	a	b	c	...	h
H	H	L	↑	L	H	X	Q_{A0}	Q_{A0}	Q_{B0}	...	Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}	...	Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}	...	Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	...	Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}	...	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't care (any input, including transitions)
↑ = Transition from low to high level
a...h = The level of steady state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = The level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = The level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

Recommended Operating Conditions

Sym	Parameter		DM54198			DM74198			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	35	25	0	35	25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	Mode	30			30			ns
		Data	20			20			
t_H	Clear Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'198 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		72	104	mA
			DM74		72	116	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, inputs A thru H and CLEAR grounded, and 4.5V applied to S0, S1 and SERIAL inputs, I_{CC} is tested with a momentary ground then 4.5V applied to CLOCK.

'198 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		23	35	ns

Recommended Operating Conditions

Sym	Parameter		DM54199			DM74199			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	35	25	0	35	25	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'199 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		72	104	mA
			DM74		72	116	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, CLOCK INHIBIT, CLEAR and SHIFT LOAD grounded, and 4.5V applied to J, $\overline{K}$ and A thru H, I_{CC} is tested with a momentary ground then 4.5V applied to CLOCK.

'199 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		23	35	ns

Logic Diagrams

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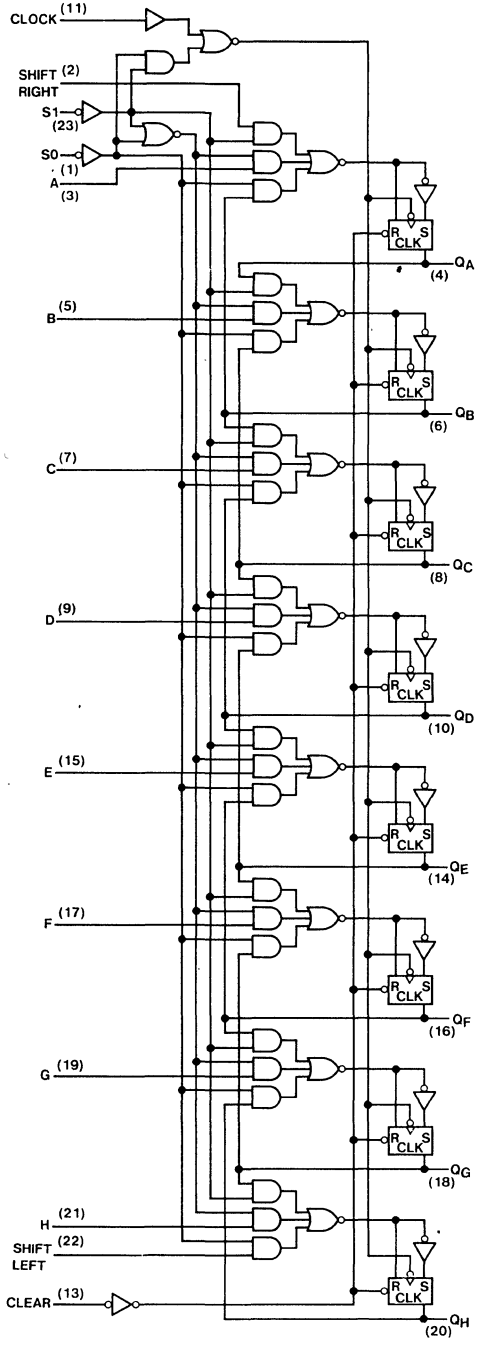

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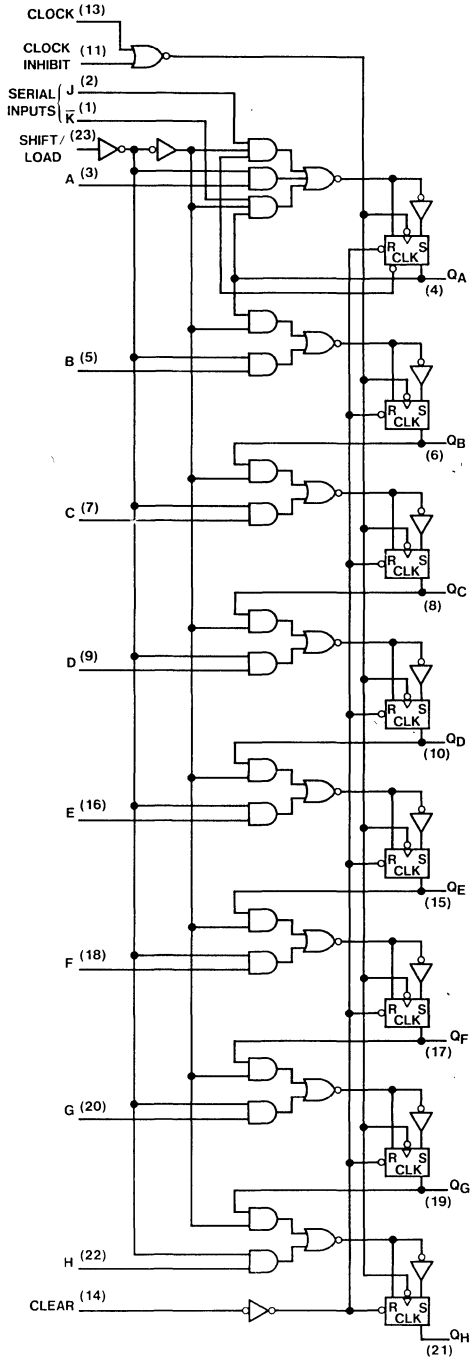

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Timing Diagrams

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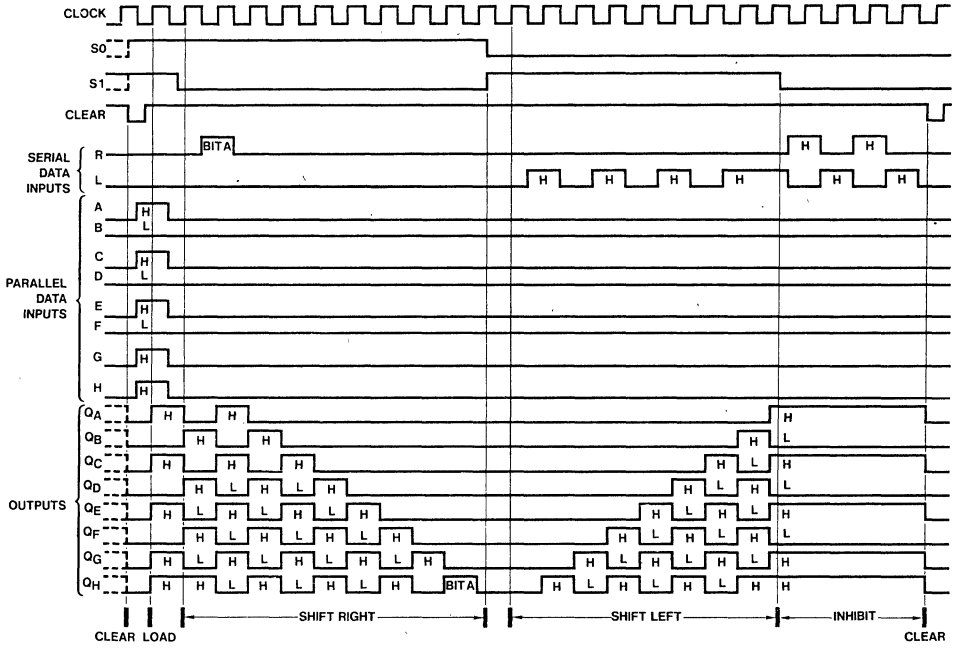
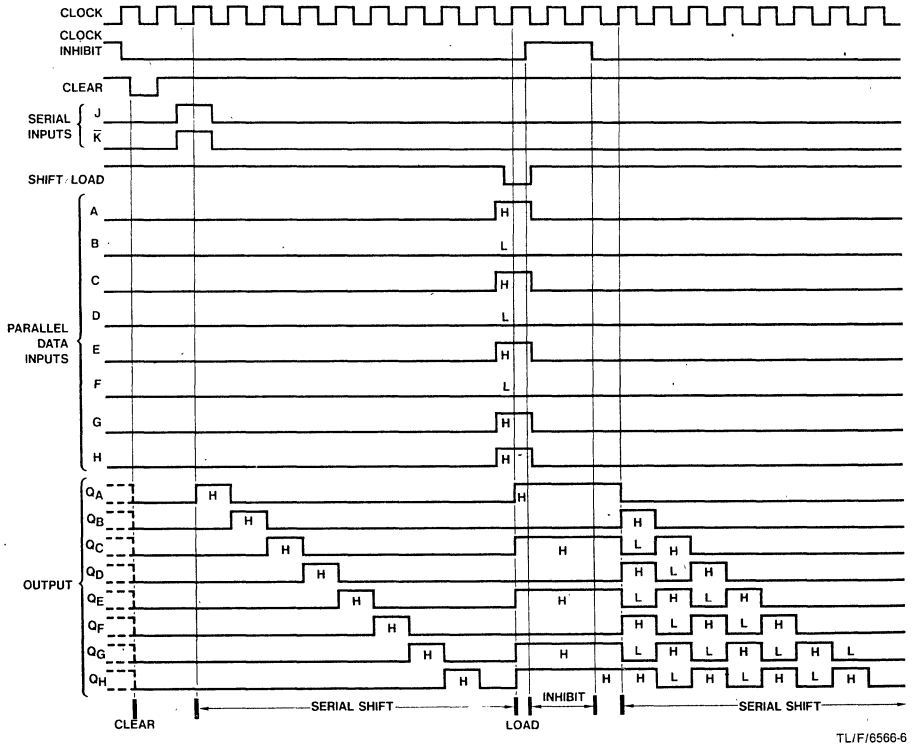
TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



TL/F/6566-5

199

TYPICAL CLEAR, SHIFT, LOAD, AND INHIBIT SEQUENCES



TL/F/6566-6

Parameter Measurement Information

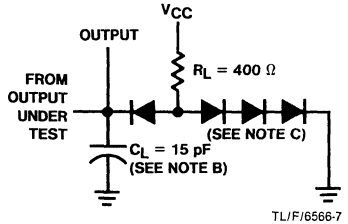
198
TEST TABLE FOR SYNCHRONOUS INPUTS

Data Input for Test	S_1	S_0	Output Tested (See Note E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

199
TEST TABLE FOR SYNCHRONOUS INPUTS

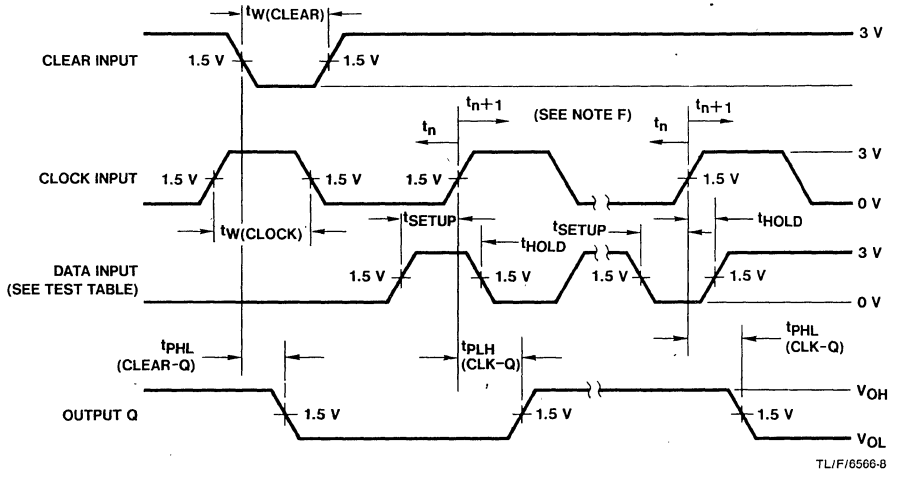
Data Input for Test	Shift/Load	Output Tested (See Note E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and $\overline{K}$	4.5 V	Q_H at t_{n+8}

LOAD FOR OUTPUT UNDER TEST



TL/F/6566-7

SWITCHING TIME WAVEFORMS



TL/F/6566-8

Note A: The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz.
The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns.
When testing f_{MAX}, vary the clock PRR.

Note B: C_L includes probe and jig capacitance.

Note C: All diodes are 1N3064.

Note D: A clear pulse is applied prior to each test.

Note E: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

Note F: t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after clocking transitions

National Semiconductor

DM54251/DM74251 TRI-STATE® 1 of 8 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of 151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Max no. of common outputs
  DM54251 49
  DM74251 129
- Typical propagation delay time (D to Y) 17ns
- Typical power dissipation 155 mW

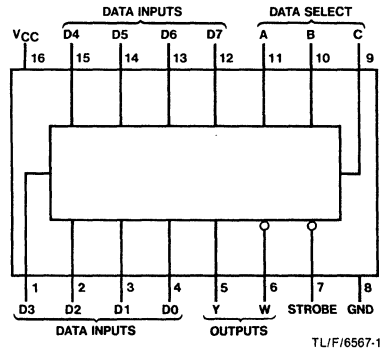
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6567-1

54251 (J) **74251 (N)**

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1...D7 = The Level of the respective D input.

Recommended Operating Conditions

Symbol	Parameter	DM54251			DM74251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−18		−70	mA
			DM74	−18		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			31	51	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

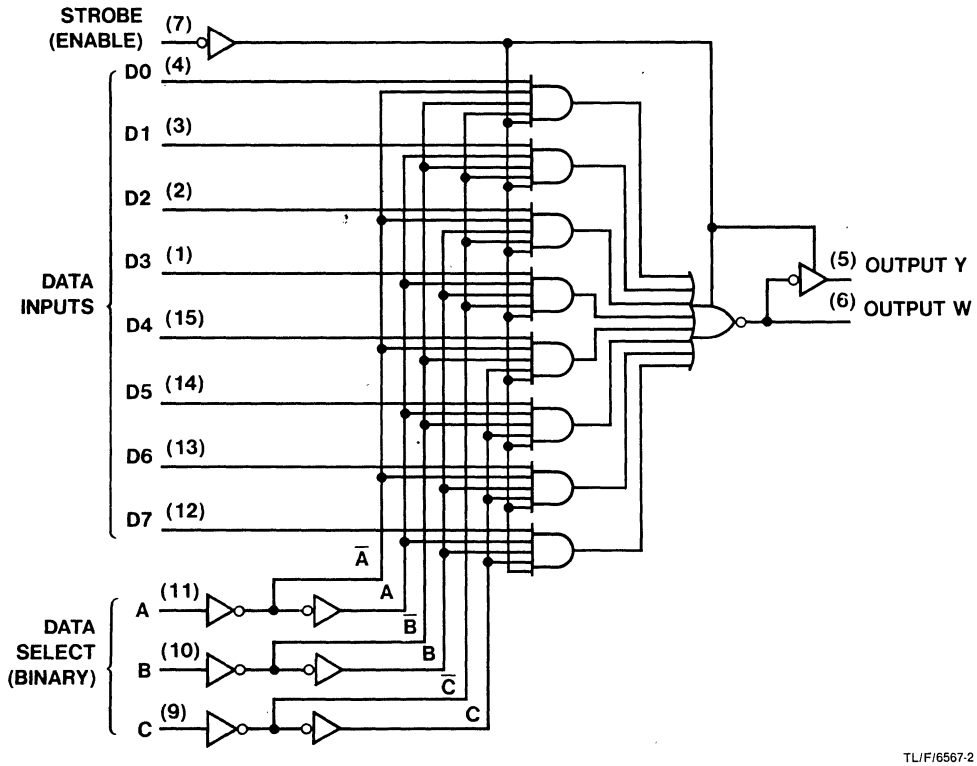
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the outputs open, STROBE at 4.5V or ground, and all other inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C (4 Levels) to Y					22	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C (4 Levels) to Y					23	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C (3 Levels) to W					18	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C (3 Levels) to W					16	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y					17	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y					18	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to W					11	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to W					10	15	ns
t_{PZH} Output Enable Time to High Level Output	Strobe to Y					15	27	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to Y					18	36	ns
t_{PZH} Output Enable Time to High Level Output	Strobe to W					15	27	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to W					19	38	ns
t_{PHZ} Output Disable Time from High Level Output	Strobe to Y	4	8					ns
t_{PLZ} Output Disable Time from Low Level Output	Strobe to Y	14	23					ns
t_{PHZ} Output Disable Time from High Level Output	Strobe to W	4	8					ns
t_{PLZ} Output Disable Time from Low Level Output	Strobe to W	15	23					ns

Logic Diagram



TL/F/6567-2

National Semiconductor

DM54253/DM74253 TRI-STATE® Dual 1 of 4 Line Data Selectors/Multiplexers

General Description

This device is a TRI-STATE version of the very popular DM54153 (DM7214) data selectors/multiplexers. It contains full on-chip decoding to select the desired data input. The DM54/74253 is a dual, four-line multiplexer that has common select lines which therefore select the same input line of both multiplexers. However, the two outputs can be individually controlled by means of the separate enable lines; which, when taken to a high logic level, places the output in the high-impedance TRI-STATE condition. The data at the output of the DM54/74253 is true.

Features

- TRI-STATE pin equivalents to popular 54/74 TTL devices DM7214/8214 — 54153/74153
- Typical propagation delay 13.5 ns
- Typical power dissipation 170 mW
- Strobe/enable override

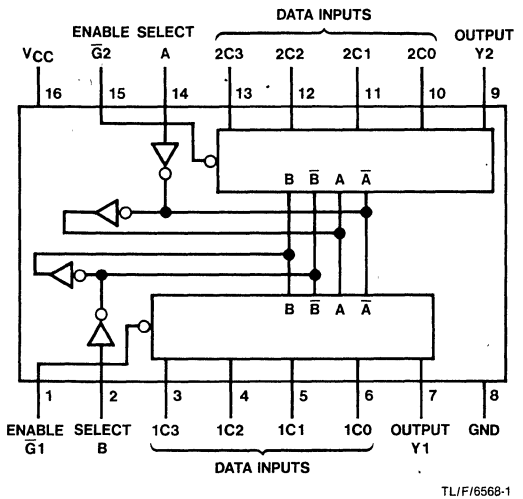
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TL/F/6568-1

54S253 (J) **74S253 (N)**

Recommended Operating Conditions

Symbol	Parameter	DM54253			DM74253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, , V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, , V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	56	mA
			DM74		34	65	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output					15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output					12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output					20	34	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output					20	34	ns
t_{PZH} Output Enable Time to High Level Output	Enable to Q					12	18	ns
t_{PZL} Output Enable Time to Low Level Output	Enable to Q					14	21	ns
t_{PHZ} Output Disable Time from High Level Output	Enable to Q		5	10				ns
t_{PLZ} Output Disable Time from Low Level Output	Enable to Q		15	23				ns

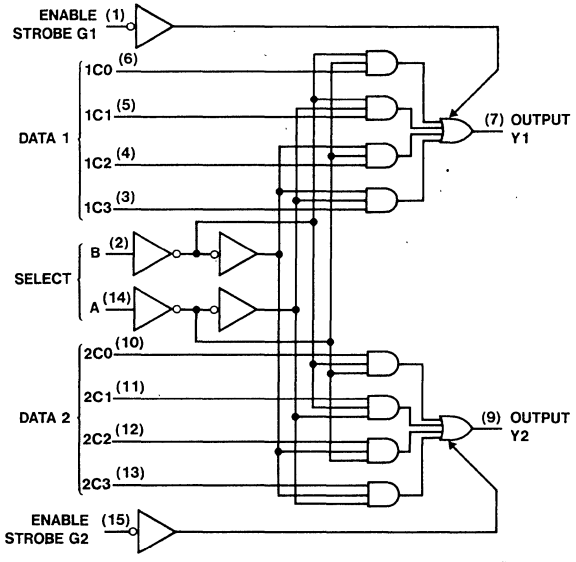
Function Table

Select Inputs		Data Inputs				Enable	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Hi-Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Hi-Z = High Impedance (Off) State

Logic Diagram

54/74253



TL/F/6568-2

National Semiconductor

DM54259/DM74259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possiblity of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Direct Replacement for Fairchild 9334
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Typical Propagation Delay Times:
  - Enable-to-Output 18 ns
  - Data-to-Output 21 ns
  - Address-to-Output 22 ns
  - Clear-to-Output 21 ns
- Fan-Out
  - I_{OL} (Sink Current) 16 mA
  - I_{OH} (Source Current) −0.8 mA
- Typical I_{CC} 60 mA

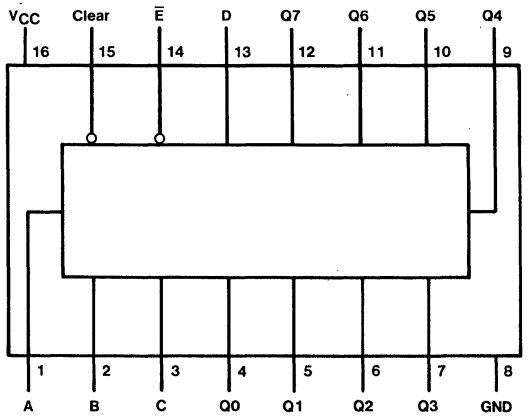
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54259 (J) **74259 (N)**

TL/F/6569-1

Recommended Operating Conditions

Symbol	Parameter		DM54259			DM74259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Pulse Width	Enable	19	13		19	13		ns
		Clear	19	13		19	13		
t_{SU}	Setup Time (Notes 1 and 2)	Data	20	13		20	13		ns
		Select	10	5		10	5		
t_H	Hold Time (Note 1)	Data	0	−10		0	−10		ns
		Select	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−55	mA
			DM74	−20		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)				90	mA

Note 1: Setup and hold times are with reference to the enable input.

Note 2: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time.

Note 5: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		24	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		19	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		21	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		21	31	ns

Function Tables

Inputs		Output Of Addressed Latch	Each Other Output	Function
Clear	$\overline{E}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H ≡ high level, L ≡ low level

D ≡ the level of the data input

Q_{i0} ≡ the level of Q_i ($i = 0, 1, \ldots 7$, as appropriate) before the indicated steady-state input conditions were established.

National Semiconductor

DM54365/DM74365 Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

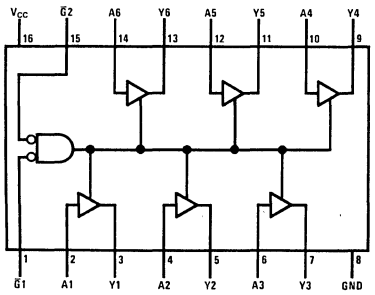
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6570-1

DM54365 (J) **DM74365 (N)**

Function Table

Y = A

Input			Output
$\overline{G1}$	$\overline{G2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Hi-Z
X	H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

6

Recommended Operating Conditions

Symbol	Parameter	DM54365			DM74365			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output					14	22	ns
t_{PZH} Output Enable Time to High Level Output					21	35	ns
t_{PZL} Output Enable Time to Low Level Output					24	37	ns
t_{PHZ} Output Disable Time from High Level Output		6	11				ns
t_{PLZ} Output Disable Time from Low Level Output		16	27				ns

National Semiconductor

DM54366/DM74366 Hex Inverting TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of the bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possiblity that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

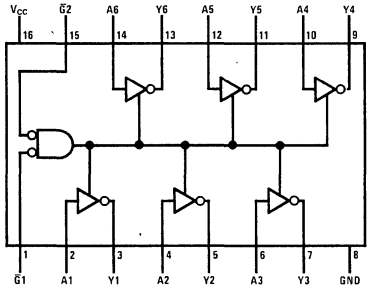
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6571-1

DM54366 (J) DM74366 (N)

Function Table

$Y = \overline{A}$

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Hi-Z
X	H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Symbol	Parameter	DM54366			DM74366			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	77	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					11	17	ns
t_{PHL} Propagation Delay Time High to Low Level Output					10	16	ns
t_{PZH} Output Enable Time to High Level Output					21	35	ns
t_{PZL} Output Enable Time to Low Level Output					24	37	ns
t_{PHZ} Output Disable Time from High Level Output		6	11				ns
t_{PLZ} Output Disable Time from Low Level Output		16	27				ns

National Semiconductor

DM54367/DM74367 Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possiblity that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

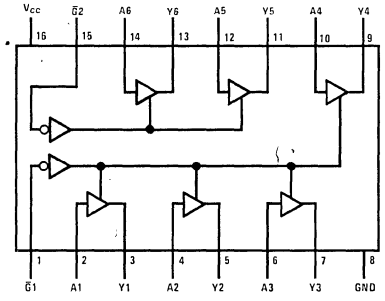
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6572-1

DM54367 (J) DM74367 (N)

Function Table

$Y = A$

Input		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

6

Recommended Operating Conditions

Symbol	Parameter	DM54367			DM74367			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			65	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					10	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output					14	22	ns
t_{PZH} Output Enable Time to High Level Output					21	35	ns
t_{PZL} Output Enable Time to Low Level Output					24	37	ns
t_{PHZ} Output Disable Time from High Level Output		6	11				ns
t_{PLZ} Output Disable Time from Low Level Output		16	27				ns

National Semiconductor

DM54368/DM74368 Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

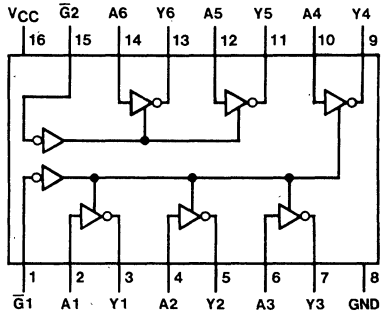
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6573-1

DM54368 (J) DM74368 (N)

Function Table

$Y = \overline{A}$

Input		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Recommended Operating Conditions

Symbol	Parameter	DM54368			DM74368			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	77	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with the data inputs grounded and the output controls at 4.5V.
Note 4: Both $\overline{G}$ inputs are at 2V.
Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					11	17	ns
t_{PHL} Propagation Delay Time High to Low Level Output					10	16	ns
t_{PZH} Output Enable Time to High Level Output					21	35	ns
t_{PZL} Output Enable Time to Low Level Output					24	37	ns
t_{PHZ} Output Disable Time from High Level Output		6	11				ns
t_{PLZ} Output Disable Time from Low Level Output		16	27				ns

National Semiconductor

DM7123/DM8123 Quad 2-Input Data Selectors/Multiplexers

General Description

This device contains four 2-input multiplexers with common input select logic and common output disable circuitry. The DM7123/8123 provides TRI-STATE® outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM7123/8123 go to the high-impedance third state. This device provides the designer with TRI-STATE and/or low power pin/pin replacements for the popular 9322 and 54/74157 multiplexers.

Features

- Pin equivalents popular 9322 and 54/74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Both conventional TTL and "one-tenth-power technology" available
- Typical propagation delay 9.5 ns
- Typical power dissipation 200 mW

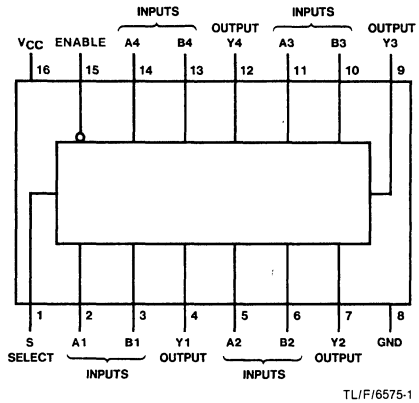
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6575-1

7123 (J) **8123 (N)**

Function Table

Enable	Select	Inputs		Output
		A	B	Y
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Hi-Z

Recommended Operating Conditions

Symbol	Parameter	DM7123			DM8123			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM71	2.4			V
			DM81	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, , V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM71	−30		−70	mA
			DM81	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			40	51	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

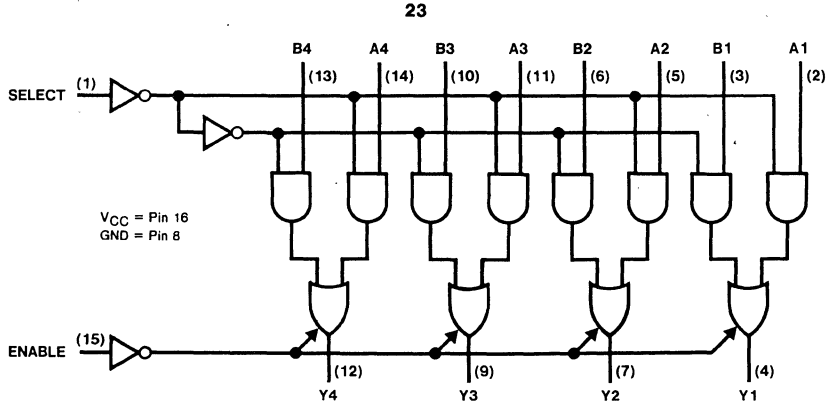
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded, and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 5$ pF			$C_L = 50$ pF			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output				4	8	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output				5	11	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output				5	15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output				8	17	24	ns
t_{PZH} Output Enable Time to High Level Output	Enable to Q				9	18	25	ns
t_{PZL} Output Enable Time to Low Level Output	Enable to Q				10	23	30	ns
t_{PHZ} Output Disable Time from High Level Output	Enable to Q	4	7	11				ns
t_{PLZ} Output Disable Time from Low Level Output	Enable to Q	9	19	27				ns

Logic Diagram



TL/F/6575-2

National Semiconductor

DM7130/DM8130 Magnitude Comparators

General Description

This device offers comparisons to determine equality between two binary words. The DM7130/DM8130 compares two ten-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open collector outputs for expansion.

Features

- Typical propagation delay 21 ns
- Typical power dissipation 240 mW
- Open-collector outputs for expansion

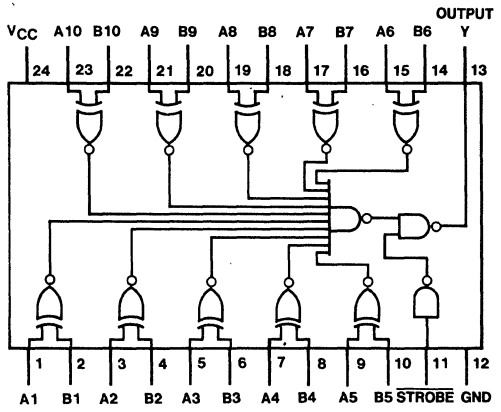
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6575-1

7130 (J) **8130 (N)**

Function Table

Condition	$\overline{\text{STROBE}}$ S	Output Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

Recommended Operating Conditions

Symbol	Parameter	DM7130			DM8130			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		48	70	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		27	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		9	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		20	30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

National Semiconductor

DM7131/DM8131 6-Bit Unified Bus Comparators

General Description

The DM7131/DM8131 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis, which provides 1.4V noise immunity. The DM7131/D8131 has active pull-up outputs and goes to the low state upon equality. The device has an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.4 V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

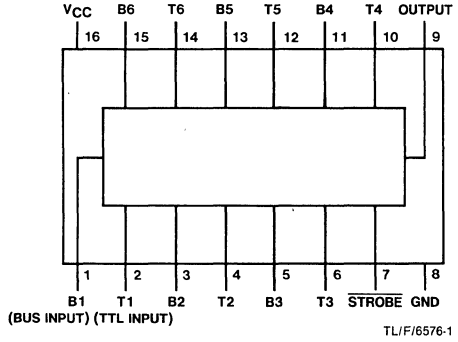
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6576-1

7131 (J) **8131 (N)**

Function Table

Condition	$\overline{\text{STROBE}}$	Output DM71/8131
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	L
T ≠ B	L	H

*Latched in previous state

Recommended Operating Conditions

Symbol	Parameter	DM7131			DM8131			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Postive-Going Input Threshold Voltage (Note 1)	1.4	1.75	2	1.45	1.75	1.95	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.9	1.1	1.35	0.95	1.1	1.3	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	TTL			1	mA
			Strobe			2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	TTL			40	μA
			Strobe			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	TTL			−1.6	mA
			Strobe			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max		15	50	μA
			V_{CC} = 0V		1	50	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM71	−18		−55	mA
			DM81	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			50	74	mA

Note 1. V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with all inputs grounded and all outputs open.

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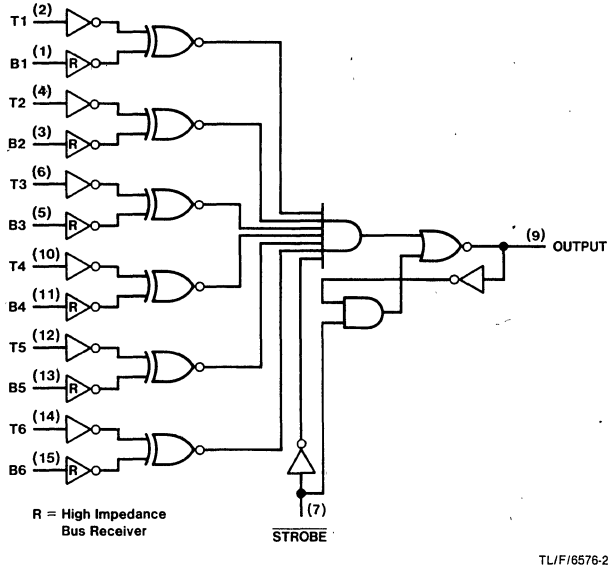
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	TTL to Output		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	TTL to Output		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Bus to Output		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Bus to Output		30	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		20	30	ns

Logic Diagram

DM71/8131



TL/F/6576-2

National Semiconductor

DM7136/DM8136 6-Bit Unified Bus Comparators

General Description

The DM7136/DM8136 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis which provides 1.4V noise immunity. The DM7136/DM8136 has open-collector outputs which go to the high state upon equality and is expandable to n bits by collector-ORing. The device has an output latch which is strobe controlled.

The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.4 V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

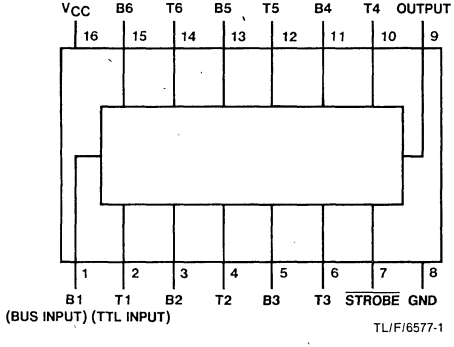
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6577-1

7136 (J) 8136 (N)

Function Table

Condition	$\overline{\text{STROBE}}$	Output DM71/8136
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	H
T ≠ B	L	L

*Latched in previous state

6

Recommended Operating Conditions

Symbol	Parameter	DM7136			DM8136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Postive-Going Input Threshold Voltage (Note 1)	1.4	1.75	2	1.45	1.75	1.95	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.9	1.1	1.35	0.95	1.1	1.3	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max V_I = 5.5V	TTL			1	mA
			Strobe			2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	TTL			40	μA
			Strobe			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	TTL			−1.6	μA
			Strobe			−2.4	
I_{IN}	Bias Input Current	V_I = 4V	V_{CC} = Max		15	50	mA
			V_{CC} = 0V		1	50	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	74	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

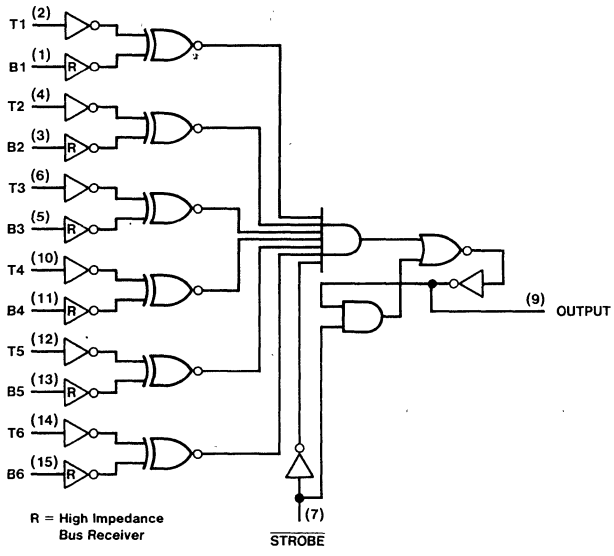
Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	TTL to Output		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	TTL to Output		20	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Bus to Output		30	45	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Bus to Output		30	45	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		20	30	ns

Logic Diagram

DM71/8136



TL/F/6577-2

6

National Semiconductor

DM7160/DM8160 Magnitude Comparators

General Description

This device offers comparisons to determine equality between two binary words. The DM7160/DM8160 compares two six-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open-collector outputs for expansion.

Features

- Typical propagation delay 21 ns
- Typical power dissipation 205 mW
- Open-collector outputs for expansion

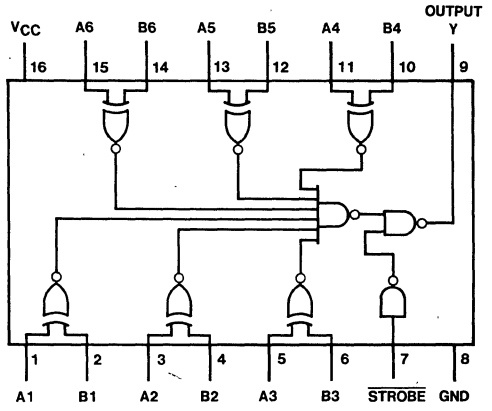
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6578-1

7160 (J) 8160 (N)

Function Table

Condition	$\overline{\text{STROBE}}$ S	Output Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

Recommended Operating Conditions

Symbol	Parameter	DM7160			DM8160			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		41	60	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		27	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		9	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		20	30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

National Semiconductor

DM7200/DM8200 4-Bit Magnitude Comparators

General Description

These devices compare two binary words of four bits in length; and the outputs indicate 1) word A > word B, 2) word A < word B, or 3) word A = word B. A strobe input overrides all other inputs, and when taken to a high logic level, places both outputs in the low state. Comparison of words longer than four bits each may be accomplished through the use of additional DM7200/DM8200 devices.

Features

- Typical power dissipation 175 mW
- Typical propagation delay 20 ns

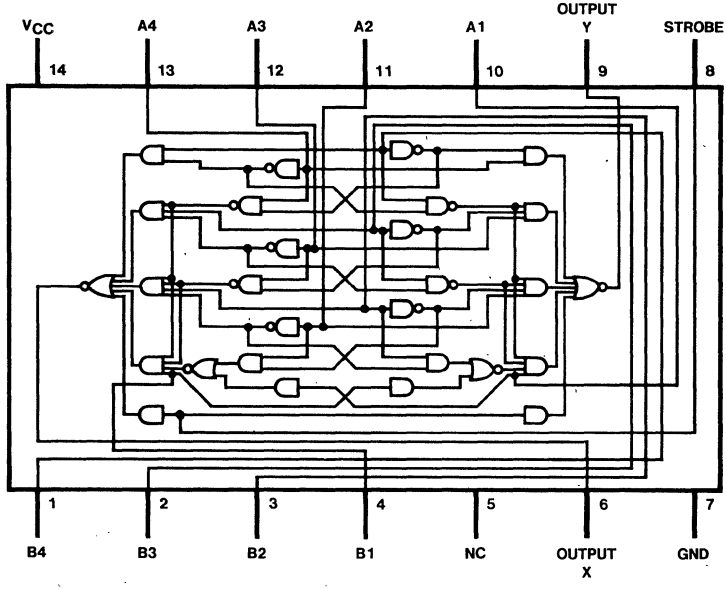
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



A4, B4 are most significant bits.

TL/F/6579-1

7200 (J) **8200 (N)**

Function Table

Inputs		Outputs	
Condition	**Strobe**	**X**	**Y**
Don't Care	H	L	L
A > B	L	H	L
A < B	L	L	H
A = B	L	H	H

Recommended Operating Conditions

Symbol	Parameter	DM7200			DM8200			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_{SU}	Setup Time	10	0		10	0		ns
t_H	Hold Time	0	−10		0	−10		ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM72	−18		−55	mA
			DM82	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max			35	53	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		24	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		17	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		15	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		8	18	ns

National Semiconductor

DM7220/DM8220 9-Bit Parity Generators/Checkers

General Description

These circuits can be used both to check for parity and to generate a parity bit. When the generation of a parity bit is desired, the eight data inputs are connected to the transmission lines. If a low logic level is then connected to the parity input, the circuit will generate odd parity. The succeeding parity checker will acknowledge an odd number of "1's" (odd parity) with a low logic level on its output. If a high logic level is connected to the parity input of the first parity generator, the parity checker will acknowledge even parity with a high logic level on its output, although the output of the parity generator will be low.

Features

- Typical propagation delay 34 ns
- Typical power dissipation 130 mW

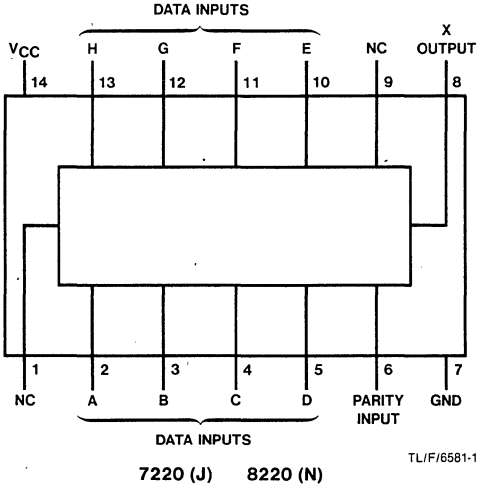
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6581-1

7220 (J) 8220 (N)

Recommended Operating Conditions

Symbol	Parameter	DM7220			DM8220			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM72	−20		−55	mA
			DM82	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max			26	35	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		36	58	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		32	52	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Parity to Output		21	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Parity to Output		14	25	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Function Table

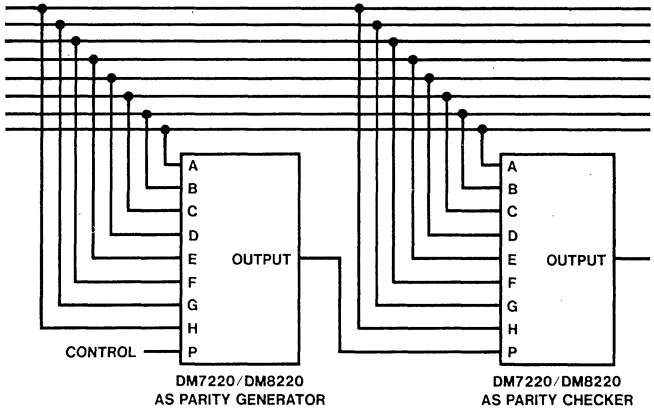
Parity Input	Output*	Inputs A Thru H
H	L	Even number of inputs are High
L	L	Odd number of inputs are High

*Single device

Typical Application

If the control line is a logical "0" the parity generator will generate odd parity. The parity checker will acknowledge the presence of an odd number of "1's" (odd parity) with a logical "0" on its output.

If the control line is a logical "1" the parity generator will generate even parity. The parity checker will acknowledge the presence of an even number of "1's" (even parity) with a logical "1" on its output.



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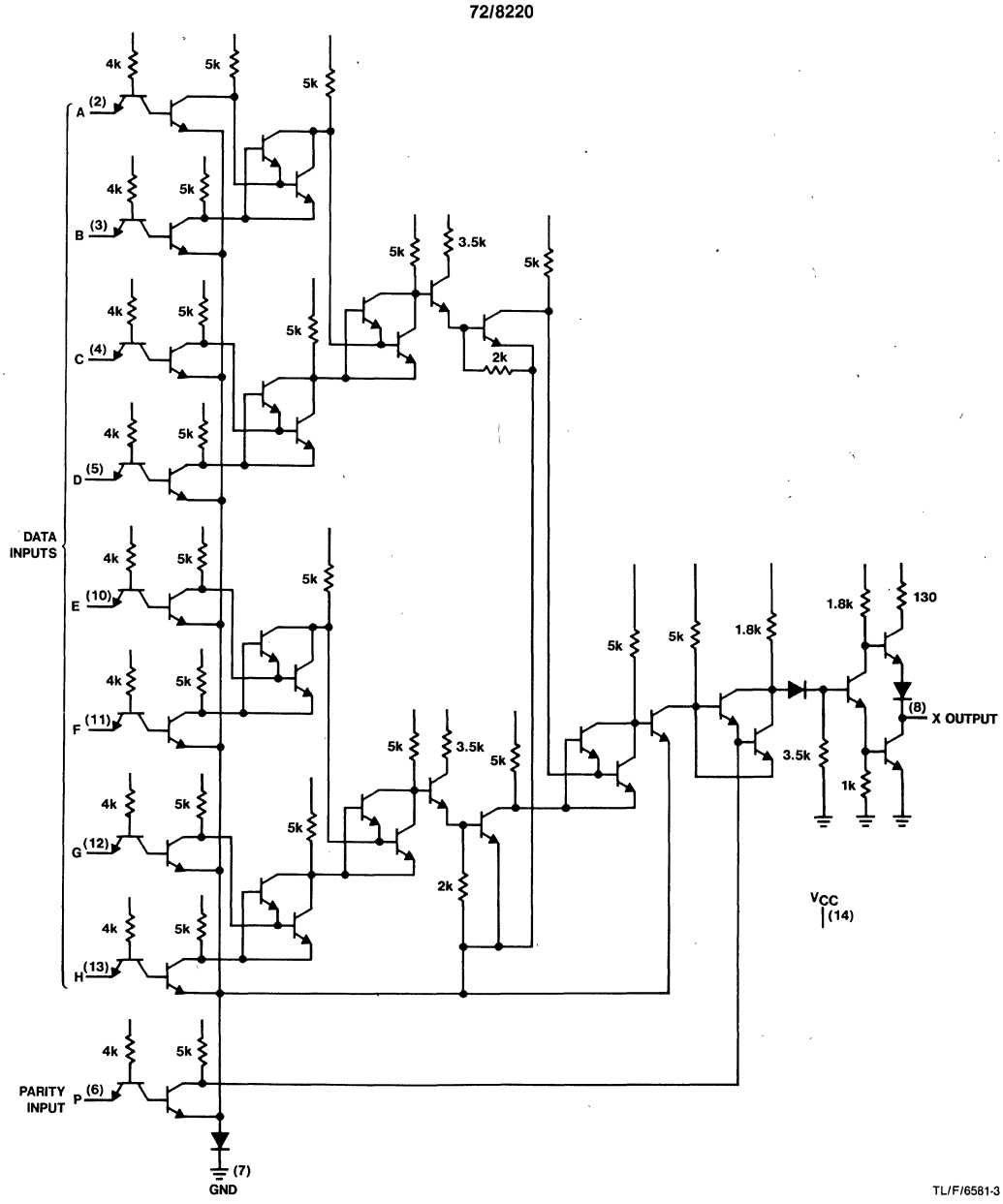
Schematic Diagram



TL/F/6581-3

National Semiconductor

DM7223/DM8223 1-Line to 8-Line Demultiplexers

General Description

These circuits demultiplex a data train, and route the data to one of eight outputs. The binary code which is applied to three address lines determines which unique output receives the data. When the data input is at a logical "0," only the addressed output will be a logical "0." When the data input is at a logical "1," all outputs, and therefore the addressed output, will be at a logical "1."

Features

- Typical power dissipation 140 mW
- Typical propagation delay 25 ns

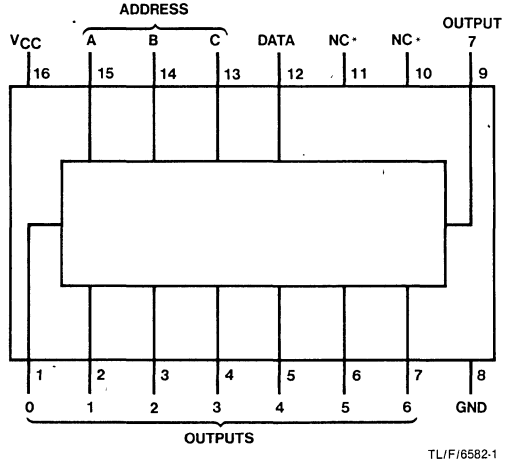
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6582-1

*Do not make connection to pins 10 or 11.

7223 (J) **8223 (N)**

Function Table

Data Input	Address Inputs			Outputs							
	C	B	A	0	1	2	3	4	5	6	7
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	H	H	H	H	H	H	H	H

X = Don't Care

Recommended Operating Conditions

Symbol	Parameter	DM7223			DM8223			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM72	−20		−55	mA
			DM82	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max			28	41	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			26	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output			24	35	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM7512/DM8512 Dual Gated Flip-Flop

General Description

The DM7512/8512 is a dual gated flip flop with two independent function controls. A low level on the MODE input creates a D flip flop, and a high level on the MODE input converts it to a JK flip flop.

These devices share a common asynchronous clear and a common clock. Clocking occurs on the positive edge of the clock pulse, while the clear function occurs at the logic high level, independent of the level on any other inputs.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

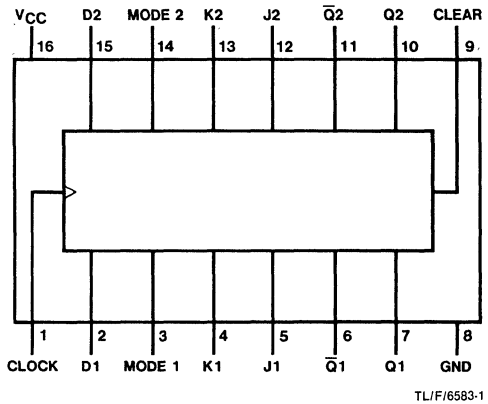
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Features

- Positive-edge triggered
- Do-nothing state
- Buffered inputs
- Typical toggle rate 28 MHz
- Typical power dissipation 220 mW

Connection Diagram

Dual-In-Line Package



TL/F/6583-1

7512 (J) **8512 (N)**

Recommended Operating Conditions

Symbol	Parameter		DM7512			DM8512			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock	25	15		25	15		ns
		Clear	25	13		25	13		
t_{SU}	Setup Time	J, D	15	9		15	9		ns
		K	20	13		20	13		
		Mode	30	20		30	20		
t_H	All Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−18		−55	mA
			DM85	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			44	57	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with CLEAR/CLOCK at 3V, all other inputs at 0V, and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	28		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		21	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		26	40	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		22	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		26	40	ns

Function Table

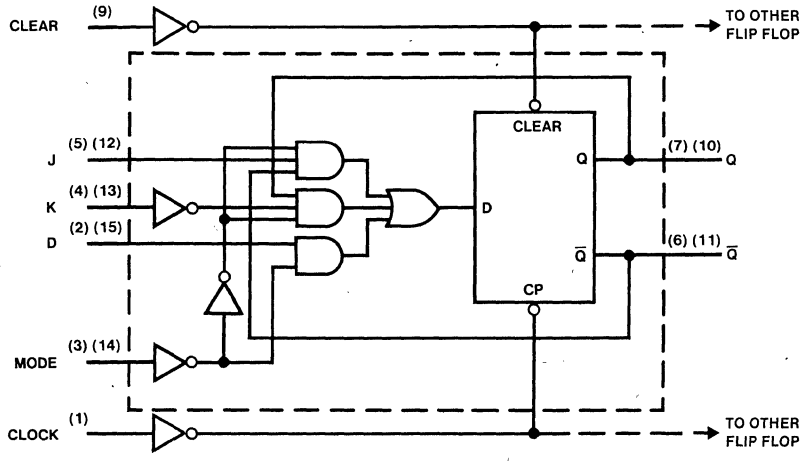
'12

Inputs						Outputs	
Clear	Mode	Clock	J	K	D	Q	$\overline{Q}$
H	X	X	X	X	X	L	H
L	H	↑	L	L	X	Q_O	$\overline{Q}_O$
L	H	↑	H	L	X	H	L
L	H	↑	L	H	X	L	H
L	H	↑	H	H	X	Toggle	
L	L	↑	X	X	L	L	H
L	L	↑	X	X	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↑ = Low-to-High Transition
Q_O = The output logic level of Q before the indicated input conditions were established.
Toggle = Each output change to the complement of its previous level on each active (↑) transition of the clock.

Logic Diagram

'12



TL/F/6583-2

6

National Semiconductor

DM7520/DM8520 Modulo-N Dividers

General Description

Although extremely versatile in a number of applications, the primary uses of these circuits are in two areas:

1. **MODULO-N DIVIDER**
   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.
2. **SHIFT REGISTER**
   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial-out shifting is required.

(Continued)

Features

- Fully programmable divider—any number from 2 to ∞
- Also functions as a four-bit parallel shift register
- Typical propagation delay 36 ns
- Typical power dissipation 250 mW

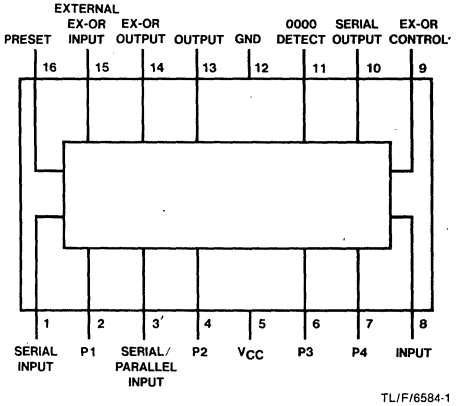
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6584-1

7520 (J) **8520 (N)**

Function Table

Table for Division By N

Setting				÷ BY
P1	P2	P3	P4	
H	H	H	L	2
H	H	L	L	3
H	L	L	L	4
L	L	L	H	5
L	L	H	L	6
L	H	L	L	7
H	L	L	H	8
L	L	H	H	9
L	H	H	L	10
H	H	L	H	11
H	L	H	L	12
L	H	L	H	13
H	L	H	H	14
L	H	H	H	15

General Description (Continued)

THEORY OF OPERATION

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed, the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is $2^n - 1$, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence this state is detected, and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16 m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidentally set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

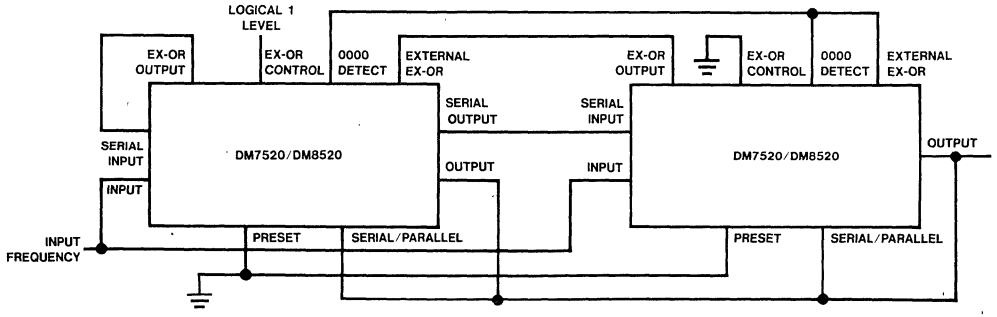
To summarize, the following connections should be made for operation of a single DM7520/DM8520.

Ex-Or Output to Serial Input
0000 Detect to External Ex-Or Input
Output to Serial/Parallel Input
Preset to Ground
Ex-Or Control to Ground

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs, thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255.

To divide by numbers between 16 and 255, the table in *Figure 2* will apply.



TL/F/6584-2

FIGURE 1. Connection for 2 Dividers for Maximum Frequency Division of 255

General Description (Continued)

Setting									Setting									Setting								
Divider 1				Divider 2				By	Divider 1				Divider 2				By	Divider 1				Divider 2				By
P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4	
L	H	H	H	H	H	H	H	255	H	L	L	L	H	L	L	H	195	L	L	H	H	H	L	L	H	135
H	L	H	H	H	H	H	H	254	H	H	L	L	L	H	L	L	194	H	L	L	H	H	H	L	L	134
L	H	L	H	H	H	H	H	253	H	H	H	L	L	L	H	L	193	L	H	L	L	H	H	H	L	133
L	L	H	L	H	H	H	H	252	L	H	H	H	L	L	L	H	192	H	L	H	L	L	H	H	H	132
H	L	L	H	L	H	H	H	251	L	L	H	H	H	L	L	L	191	H	H	L	H	L	L	H	H	131
L	H	L	L	H	L	H	H	250	L	L	L	H	H	H	L	L	190	L	H	H	L	H	L	L	H	130
L	L	H	L	L	H	L	H	249	H	L	L	L	H	H	H	L	189	H	L	H	H	L	H	L	L	129
L	L	L	H	L	L	H	L	248	L	H	L	L	L	H	H	H	188	L	H	L	H	H	L	H	L	128
L	L	L	L	H	L	L	H	247	H	L	H	L	L	L	H	H	187	H	L	H	L	H	H	L	H	127
L	L	L	L	L	H	L	L	246	H	H	L	H	L	L	L	H	186	L	H	L	H	L	H	H	L	126
L	L	L	L	L	L	H	L	245	L	H	H	L	H	L	L	L	185	L	L	H	L	H	L	H	H	125
L	L	L	L	L	L	L	H	244	L	L	H	H	L	H	L	L	184	H	L	L	H	L	H	L	H	124
H	L	L	L	L	L	L	L	243	H	L	L	H	H	L	H	L	183	L	H	L	L	H	L	H	L	123
H	H	L	L	L	L	L	L	242	L	H	L	L	H	H	L	H	182	H	L	H	L	L	H	L	H	122
H	H	H	L	L	L	L	L	241	L	L	H	L	L	H	H	L	181	H	H	L	H	L	L	H	L	121
L	H	H	H	L	L	L	L	240	H	L	L	H	L	L	H	H	180	H	H	H	L	H	L	L	H	120
H	L	H	H	H	L	L	L	239	L	H	L	L	H	L	L	H	179	L	H	H	H	L	H	L	L	119
H	H	L	H	H	H	L	L	238	L	L	H	L	L	H	L	L	178	H	L	H	H	H	L	H	L	118
L	H	H	L	H	H	H	L	237	H	L	L	H	L	L	H	L	177	H	H	L	H	H	H	L	H	117
L	L	H	H	L	H	H	H	236	H	H	L	L	H	L	L	H	176	H	H	H	L	H	H	H	L	116
L	L	L	H	H	L	H	H	235	H	H	H	L	L	H	L	L	175	H	H	H	H	L	H	H	H	115
L	L	L	L	H	H	L	H	234	L	H	H	H	L	L	H	L	174	H	H	H	H	H	L	H	H	114
L	L	L	L	L	H	H	L	233	H	L	H	H	H	L	L	H	173	L	H	H	H	H	H	L	H	113
L	L	L	L	L	L	H	H	232	L	H	L	H	H	H	L	L	172	H	L	H	H	H	H	H	L	112
H	L	L	L	L	L	L	H	231	H	L	H	L	H	H	H	L	171	H	H	L	H	H	H	H	H	111
L	H	L	L	L	L	L	L	230	H	H	L	H	L	H	H	H	170	H	H	H	L	H	H	H	H	110
L	L	H	L	L	L	L	L	229	L	H	H	L	H	L	H	H	169	L	H	H	H	L	H	H	H	109
H	L	L	H	L	L	L	L	228	H	L	H	H	L	H	L	H	168	L	L	H	H	H	L	H	H	108
H	H	L	L	H	L	L	L	227	H	H	L	H	H	L	H	L	167	H	L	L	H	H	H	L	H	107
L	H	H	L	L	H	L	L	226	L	H	H	L	H	H	L	H	166	H	H	L	L	H	H	H	L	106
H	L	H	H	L	L	H	L	225	H	L	H	H	L	H	H	L	165	L	H	H	L	L	H	H	H	105
L	H	L	H	H	L	L	H	224	L	H	L	H	H	L	H	H	164	L	L	H	H	L	L	H	H	104
L	L	H	L	H	H	L	L	223	L	L	H	L	H	H	L	H	163	L	L	L	H	H	L	L	H	103
L	L	L	H	L	H	H	L	222	H	L	L	H	L	H	H	L	162	L	L	L	L	H	H	L	L	102
L	L	L	L	H	L	H	H	221	H	H	L	L	H	L	H	H	161	H	L	L	L	L	H	H	L	101
L	L	L	L	L	H	L	H	220	H	H	H	L	L	H	L	H	160	H	H	L	L	L	L	H	H	100
H	L	L	L	L	L	H	L	219	H	H	H	H	L	L	H	L	159	L	H	H	L	L	L	L	H	99
H	H	L	L	L	L	L	H	218	L	H	H	H	H	L	L	H	158	L	L	H	H	L	L	L	L	98
L	H	H	L	L	L	L	L	217	H	L	H	H	H	H	L	L	157	H	L	L	H	H	L	L	L	97
H	L	H	H	L	L	L	L	216	H	H	L	H	H	H	H	L	156	L	H	L	L	H	H	L	L	96
L	H	L	H	H	L	L	L	215	L	H	H	L	H	H	H	H	155	H	L	H	L	L	H	H	L	95
H	L	H	L	H	H	L	L	214	H	L	H	H	L	H	H	H	154	L	H	L	H	L	L	H	H	94
H	H	L	H	L	H	H	L	213	H	H	L	H	H	L	H	H	153	H	L	H	L	H	L	L	H	93
H	H	H	L	H	L	H	H	212	H	H	H	L	H	H	L	H	152	L	H	L	H	L	H	L	L	92
L	H	H	H	L	H	L	H	211	L	H	H	H	L	H	H	L	151	L	L	H	L	H	L	H	L	91
L	L	H	H	H	L	H	L	210	H	L	H	H	H	L	H	H	150	L	L	L	H	L	H	L	H	90
L	L	L	H	H	H	L	H	209	L	H	L	H	H	H	L	H	149	H	L	L	L	H	L	H	L	89
L	L	L	L	H	H	H	L	208	L	L	H	L	H	H	H	L	148	L	H	L	L	L	H	L	H	88
H	L	L	L	L	H	H	H	207	L	L	L	H	L	H	H	H	147	H	L	H	L	L	L	H	L	87
L	H	L	L	L	L	H	H	206	H	L	L	L	H	L	H	H	146	L	H	L	H	L	L	L	H	86
H	L	H	L	L	L	L	H	205	H	H	L	L	L	H	L	H	145	H	L	H	L	H	L	L	L	85
H	H	L	H	L	L	L	L	204	L	H	H	L	L	L	H	L	144	H	H	L	H	L	H	L	L	84
H	H	H	L	H	L	L	L	203	H	L	H	H	L	L	L	H	143	H	H	H	L	H	L	H	L	83
H	H	H	H	L	H	L	L	202	H	H	L	H	H	L	L	L	142	H	H	H	H	L	H	L	H	82
L	H	H	H	H	L	H	L	201	L	H	H	L	H	H	L	L	141	H	H	H	H	H	L	H	L	81
L	L	H	H	H	H	L	H	200	L	L	H	H	L	H	H	L	140	H	H	H	H	H	H	L	H	80
H	L	L	H	H	H	H	L	199	H	L	L	H	H	L	H	H	139	L	H	H	H	H	H	H	L	79
L	H	L	L	H	H	H	H	198	H	H	L	L	H	H	L	H	138	L	L	H	H	H	H	H	H	78
L	L	H	L	L	H	H	H	197	H	H	H	L	L	H	H	L	137	H	L	L	H	H	H	H	H	77
L	L	L	H	L	L	H	H	196	L	H	H	H	L	L	H	H	136	H	H	L	L	H	H	H	H	76

FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations)

General Description (Continued)

Setting									Setting									Setting								
Divider 1				Divider 2				By	Divider 1				Divider 2				By	Divider 1				Divider 2				By
P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4		P1	P2	P3	P4	P1	P2	P3	P4	
H	H	H	L	L	H	H	H	75	L	L	H	H	H	H	L	L	50	L	H	H	L	L	H	H	L	25
H	H	H	H	L	L	H	H	74	L	L	L	H	H	H	H	L	49	H	L	H	H	L	L	H	H	24
H	H	H	H	H	L	L	H	73	H	L	L	L	H	H	H	H	48	H	H	L	H	H	L	L	H	23
L	H	H	H	H	H	L	L	72	H	H	L	L	L	H	H	H	47	H	H	H	L	H	H	L	L	22
L	L	H	H	H	H	H	L	71	L	H	H	L	L	L	H	H	46	H	H	H	H	L	H	H	L	21
L	L	L	H	H	H	H	H	70	L	L	H	H	L	L	L	H	45	L	H	H	H	H	L	H	H	20
L	L	L	L	H	H	H	H	69	L	L	L	H	H	L	L	L	44	H	L	H	H	H	H	L	H	19
L	L	L	L	L	H	H	H	68	H	L	L	L	H	H	L	L	43	L	H	L	H	H	H	H	L	18
H	L	L	L	L	L	H	H	67	L	H	L	L	L	H	H	L	42	H	L	H	L	H	H	H	H	17
L	H	L	L	L	L	L	H	66	L	L	H	L	L	L	H	H	41	L	H	L	H	L	H	H	H	16
H	L	H	L	L	L	L	L	65	L	L	L	H	L	L	L	H	40	H	L	H	L	H	L	H	H	15
L	H	L	H	L	L	L	L	64	H	L	L	L	H	L	L	L	39	L	H	L	H	L	H	L	H	14
L	L	H	L	H	L	L	L	63	L	H	L	L	L	H	L	L	38	H	L	H	L	H	L	H	L	13
L	L	L	H	L	H	L	L	62	L	L	H	L	L	L	H	L	37	H	H	L	H	L	H	L	H	12
L	L	L	L	H	L	H	L	61	H	L	L	H	L	L	L	H	36	L	H	H	L	H	L	H	L	11
H	L	L	L	L	H	L	H	60	L	H	L	L	H	L	L	L	35	L	L	H	H	L	H	L	H	10
L	H	L	L	L	L	H	L	59	H	L	H	L	L	H	L	L	34	L	L	L	H	H	L	H	L	9
L	L	H	L	L	L	L	H	58	L	H	L	H	L	L	H	L	33	H	L	L	L	H	H	L	H	8
L	L	L	H	L	L	L	L	57	L	L	H	L	H	L	L	H	32	H	H	L	L	L	H	H	L	7
L	L	L	L	H	L	L	L	56	H	L	L	H	L	H	L	L	31	H	H	H	L	L	L	H	H	6
H	L	L	L	L	H	L	L	55	H	H	L	L	H	L	H	L	30	H	H	H	H	L	L	L	H	5
H	H	L	L	L	L	H	L	54	L	H	H	L	L	H	L	H	29	H	H	H	H	H	L	L	L	4
H	H	H	L	L	L	L	H	53	L	L	H	H	L	L	H	L	28	H	H	H	H	H	H	L	L	3
H	H	H	H	L	L	L	L	52	H	L	L	H	H	L	L	H	27	H	H	H	H	H	H	H	L	2
L	H	H	H	H	L	L	L	51	H	H	L	L	H	H	L	L	26									

FIGURE 2. DM7520/DM8520 Shift Register Divider Input Coding Table (2 Package Combinations)

Recommended Operating Conditions

Symbol	Parameter	DM7520			DM8520			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
f_{CLK}	Clock Frequency	0		15	0		15	MHz
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	EX-OR			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	EX-OR			−3.2	mA
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−20		−55	mA
			DM85	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max			50	75	mA

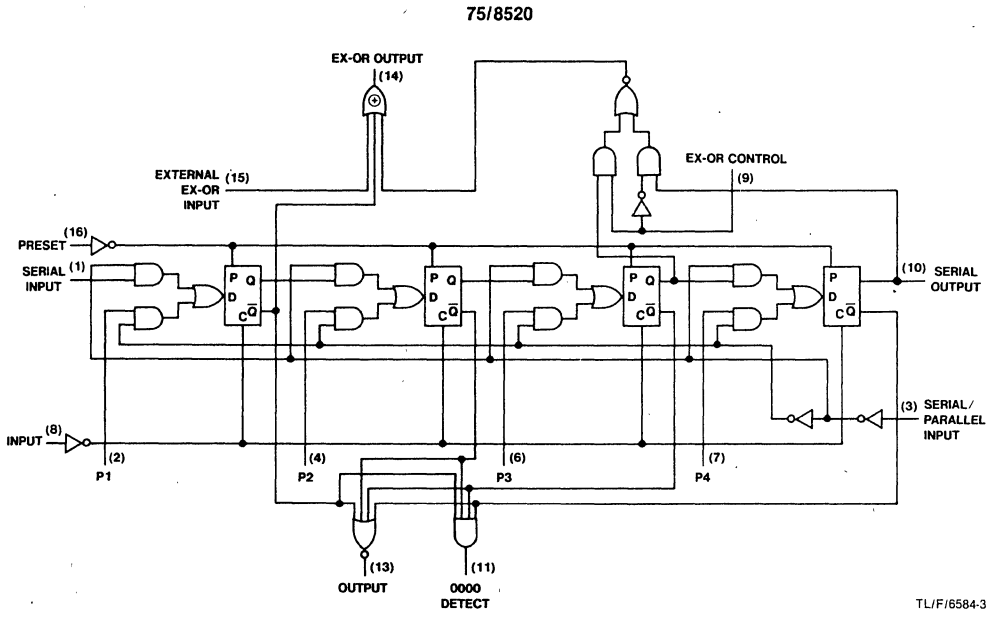
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF R_L = 100Ω			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		15	20		MHz
t_{PLH} Propagation Delay Time Low to High Level Output			35	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output			38	55	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Logic Diagram



6

National Semiconductor

DM7542/DM8542 TRI-STATE® Quad I/O Registers

General Description

These circuits are four-bit storage registers having two terminals per bit, which may be used as either inputs or outputs while tied to their individual bus lines. Storage capability is also provided by means of positive-edge triggered flip-flops having a common clock and asynchronous clear. Each I/O terminal can be forced into the high-impedance state by applying a high logic level to its disable control. The four A outputs are tied together on one disable control, while the four B outputs are tied together on a separate disable control.

Features

- TRI-STATE outputs
- Typical clock frequency 40 MHz
- Typical propagation delay 24 ns
- Typical power dissipation 400 mW

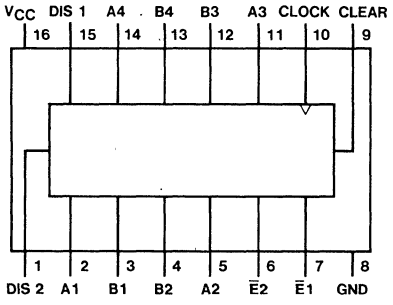
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6582-1

7542 (J) **8542 (N)**

Function Table

MODES OF OPERATION

DIS 1	DIS 2	$\overline{E}1$	$\overline{E}2$	A (1–4)	B (1–4)	Comments
L	H	H	H	Q	Hi-Z	Output data to Bus A
H	L	H	H	Hi-Z	Q	Output data to Bus B
L	L	H	H	Q	Q	Output data to both buses
H	H	H	H	Hi-Z	Hi-Z	Store data with output in high impedance state
X	L	L	H	Data	Qn	Enter data from Bus A
X	H	L	H	Data	Hi-Z	Enter data from Bus A
L	X	H	L	Q_n	Data	Enter data from Bus B
H	X	H	L	Hi-Z	Data	Enter data from Bus B
X	X	L	L	Data	Data	Enter data from both buses (logical "1" on either will dominate)

Clear = Logical "1," puts all outputs to L state.
X = Don't Care
Q_n = Data After Clock Transition

Recommended Operating Conditions

Symbol	Parameter		DM7542			DM8542			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		30	0		30	MHz
t_W	Pulse Width	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time	EN-HI	20	12		20	12		ns
		EN-LO	20	13		20	13		
		Data-1	5	−4		5	−4		
		Data-0	10	4.5		10	4.5		
t_H	Hold Time	Data-1	5	−3.5		5	−3.5		ns
		Data-0	10	4.5		10	4.5		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−25		−70	mA
			DM85	−25		−70	
I_{CC}	Supply Current	V_{CC} = Max			80	120	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

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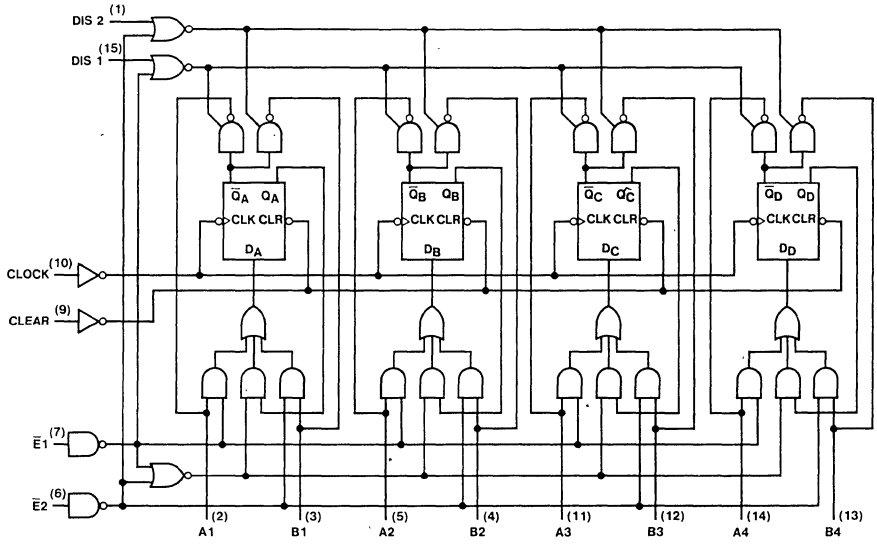
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency					30	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output					25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output					23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output					24	36	ns
t_{PZH} Output Enable Time to High Level Output	Output Disable to Q					20	30	ns
t_{PZL} Output Enable Time to Low Level Output	Output Disable to Q					17	25	ns
t_{PHZ} Output Disable Time from High Level Output	Output Disable to Q		6	15				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Disable to Q		15	25				ns

Logic Diagram



TL/F/6582-2

6

National Semiconductor

DM7544/DM8544 TRI-STATE® Quad Switch Debouncers

General Description

These circuits are for use in front panels, and similar applications where contact bounce must be eliminated. Within the single package, these circuits do the job of four R-S latches plus pull-up resistors. A strobe is also available which permits sampling of the switch information at a predetermined time. TRI-STATE outputs are also provided for direct connections to the switch line bus.

Features

- Replaces SN54279/74279
- Eliminates push-button noise
- Allows clocked devices to be operated from switches
- Maximum power dissipation 250 mW
- Bus-line connectable
- TRI-STATE outputs
- Typical propagation delay 18 ns

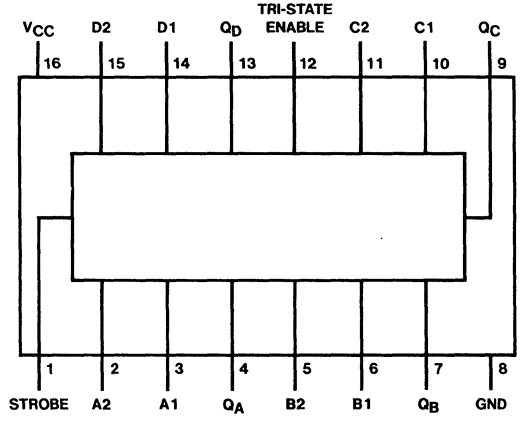
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



7544 (J) 8544 (N)

TL/F/6586-1

Function Table

A1	A2	TRI-STATE Enable	Strobe	$Q_{A(t)}$
X	X	H	X	Hi-Z
X	X	L	L	$Q_{A(t-1)}$
L	L	L	⌐	Indeterminate
L	H	L	H	L
H	L	L	H	H
H	H	L	H	$Q_{A(t)}$

Recommended Operating Conditions

Symbol	Parameter	DM7544			DM8544			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input current	V_{CC} = Max V_I = 0.4V	Data			−2.5	mA
			Other			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−18		−55	mA
			DM85	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max				50	mA

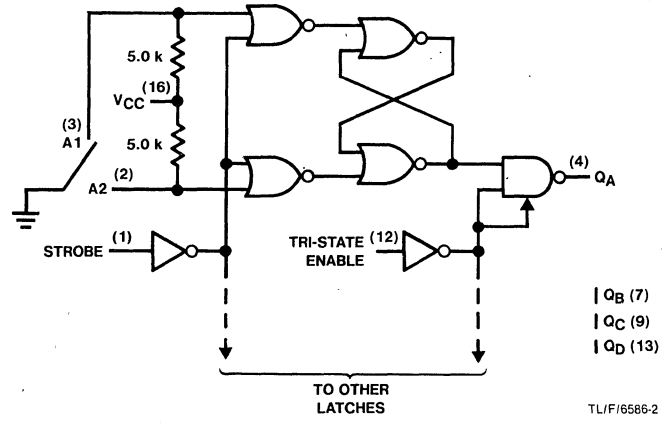
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output					20	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output					17	30	ns
t_{PZH} Output Enable Time to High Level Output	Enable to Q					15	25	ns
t_{PZL} Output Enable Time to Low Level Output	Enable to Q					12	24	ns
t_{PHZ} Output Disable Time from High Level Output	Enable to Q		5	10				ns
t_{PLZ} Output Disable Time from Low Level Output	Enable to Q		10	20				ns

Logic Diagram



National Semiconductor

DM7546/DM8546 TRI-STATE® 8-Bit Universal I/O Shift Registers

General Description

These circuits are TRI-STATE, 8-bit, edge-triggered, universal shift registers which are capable of operating in any of the following modes: shift left, shift right, parallel load, or inhibit. Since the clock is edge-triggered, the control lines which determine the mode of operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

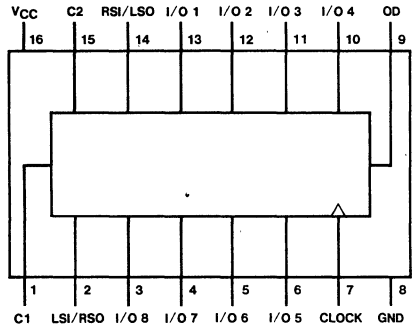
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Features

- Positive-edge triggered clock
- "Do nothing" state without gating the clock
- Both parallel and serial data lines are TRI-STATE
- High impedance state does not impede shift mode with parallel outputs

Connection Diagram

Dual-In-Line Package



TL/F/6587-1

7546 (J) **8546 (N)**

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Recommended Operating Conditions

Symbol	Parameter		DM7546			DM8546			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Clock Pulse Width		18	12		18	12		ns
$t_{SETUP\ (HIGH)}$	Serial Data	$C_L = 50$ pF	38	25		38	25		ns
$t_{SETUP\ (HIGH)}$	Parallel Data	$R_L = 400\Omega$	33	22		33	22		ns
$t_{SETUP\ (LOW)}$	Serial Data		21	14		21	14		ns
$t_{SETUP\ (LOW)}$	Parallel Data		18	12		18	12		ns
$t_{HOLD\ (HIGH)}$	Serial Data		0	−11		0	−11		ns
$t_{HOLD\ (HIGH)}$	Parallel Data		0	−11		0	−11		ns
$t_{HOLD\ (LOW)}$	Serial Data		0	−22		0	−22		ns
$t_{HOLD\ (LOW)}$	Parallel Data		0	−21		0	−21		ns
SETUP AND HOLD TIMES BETWEEN CHANGES IN MODE CONTROL AND CLOCKING									
t_{SETUP}	Parallel Load to Right Shift	$C_L = 50$ pF	32	21		32	21		ns
t_{SETUP}	Parallel Load to Left Shift	$R_L = 400\Omega$	40	27		40	27		ns
t_{SETUP}	Right Shift to Parallel Load		60	40		60	40		ns
t_{SETUP}	Left Shift to Parallel Load		53	35		53	35		ns
t_{SETUP}	Right Shift to Left Shift		33	21		33	21		ns
t_{SETUP}	Left Shift to Right Shift		56	37		56	37		ns
t_{SETUP}	Inhibit to Right Shift		57	38		57	38		ns
t_{SETUP}	Inhibit to Left Shift		65	43		65	43		ns
t_{SETUP}	Right Shift to Inhibit		50	33		50	33		ns
t_{SETUP}	Left Shift to Inhibit		50	32		50	32		ns
t_{HOLD}	Parallel Load to Right Shift		9	6		9	6		ns
t_{HOLD}	Parallel Load to Left Shift		6	4		6	4		ns
t_{HOLD}	Right Shift to Parallel Load		0	−13		0	−13		ns
t_{HOLD}	Left Shift to Parallel Load		0	−46		0	−46		ns
t_{HOLD}	Right Shift to Left Shift		0	−10		0	−10		ns
t_{HOLD}	Left Shift to Right Shift		0	−23		0	−23		ns
t_{HOLD}	Inhibit to Right Shift		0	−18		0	−18		ns
t_{HOLD}	Inhibit to Left Shift		0	−16		0	−16		ns
t_{HOLD}	Right Shift to Inhibit		0	−12		0	−12		ns
t_{HOLD}	Left Shift to Inhibit		0	−29		0	−29		ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	C2			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	C2			−3.2	mA
			Other			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−30		−70	mA
			DM85	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max	DM75		80	115	mA
			DM85		80	125	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency					15	22		MHz
t_{PLH} Propagation Delay Time Low to High Level Output						16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output						27	40	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q					22	33	ns
t_{PZH} Output Enable Time to High Level Output	Mode Control (C1/C2) to Q					13	20	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q					18	27	ns
t_{PZL} Output Enable Time to Low Level Output	Mode Control (C1/C2) to Q					15	23	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q		5	8				ns
t_{PHZ} Output Disable Time from High Level Output	Mode Control (C1/C2) to Q		9	14				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q		16	24				ns
t_{PLZ} Output Disable Time from Low Level Output	Mode Control (C1/C2) to Q		17	26				ns

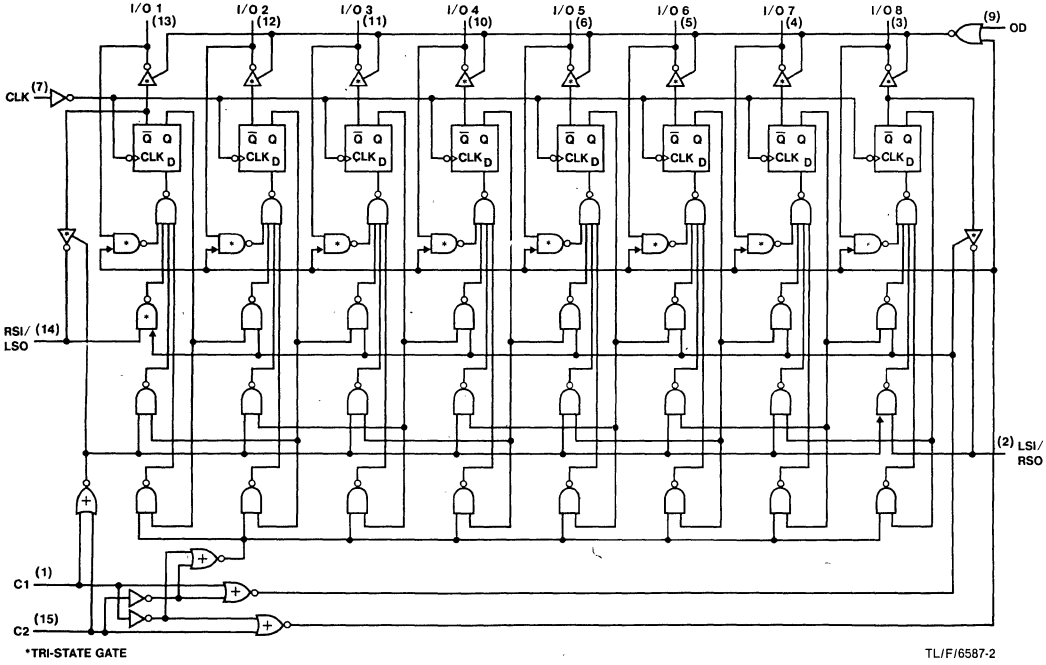
Function Table

OD	C1	C2	Mode of Operation	State of Parallel I/O	State of Serial I/O	
					RSI/LSO	LSI/RSO
L	H	H	Inhibit	Q_{OUT}	Hi-Z*	Hi-Z*
H	H	H	Inhibit	Hi-Z*	Hi-Z*	Hi-Z*
X	H	L	Parallel Load	Data In	Hi-Z*	Hi-Z*
L	L	H	Right Shift	Q_{OUT}	Data In	Q_{OUT} 8
H	L	H	Right Shift	Hi-Z*	Data In	Q_{OUT} 8
L	L	L	Left Shift	Q_{OUT}	Q_{OUT} 1	Data In
H	L	L	Left Shift	Hi-Z*	Q_{OUT} 1	Data In

OD = Output Disable (C1, C2 = Mode Controls)

*Both Input and Output of the I/O pin are in the high impedance state.

Logic Diagram



TL/F/6587-2

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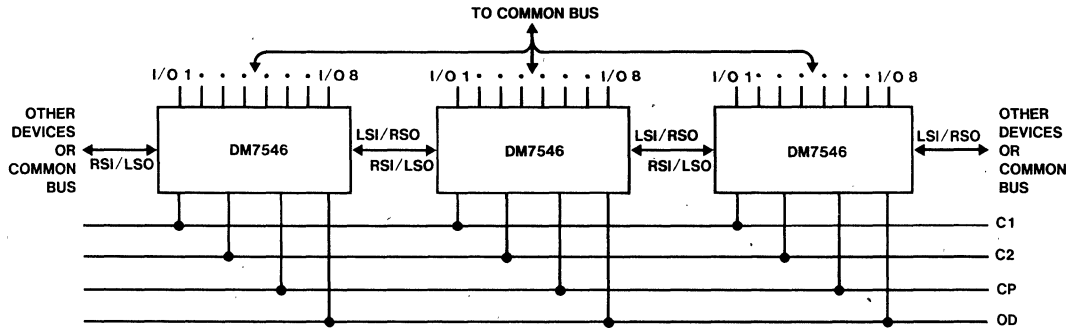
Typical Applications

Cascading Devices



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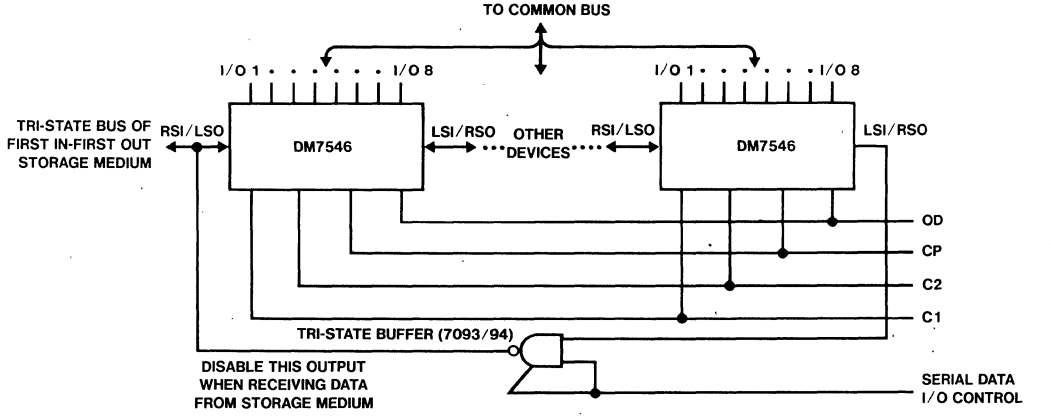
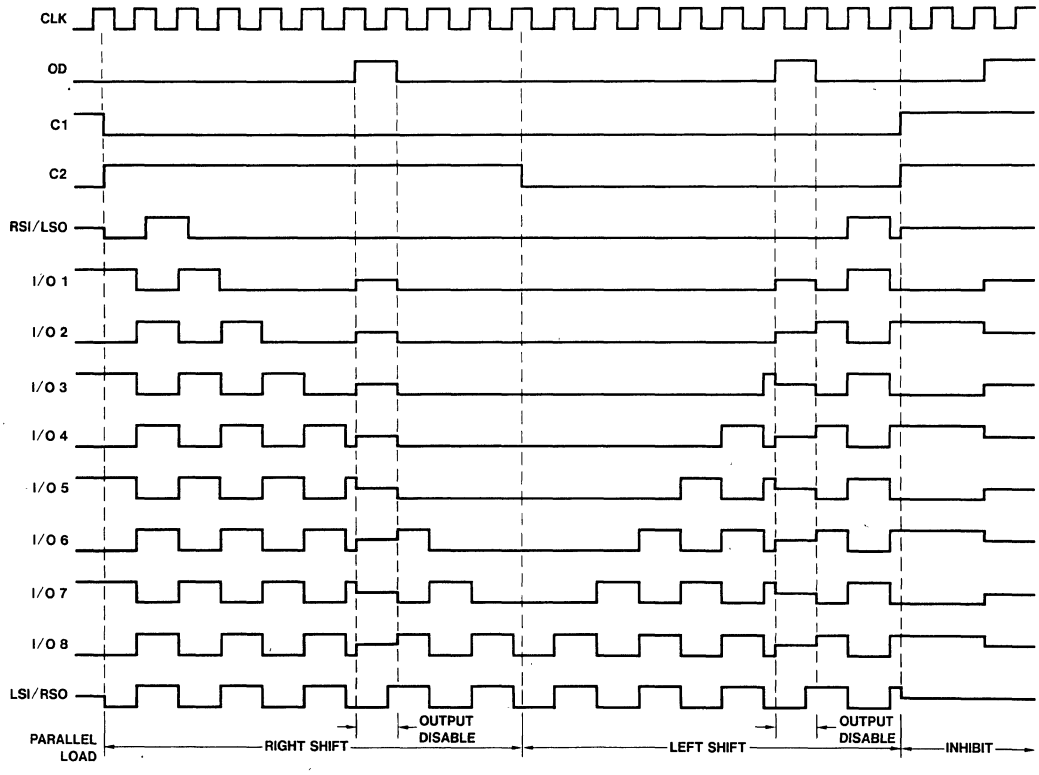
Serial Data Transfer to a First In-First Out Storage Medium



TL/F/6587-4

Typical Applications (Continued)

Typical Parallel Load, Right Shift, Left Shift and Inhibit Sequences



TL/F/6587-5

National Semiconductor

DM7556/DM8556 TRI-STATE® Programmable Binary Counters

General Description

These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high-impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input of the next counter.

Features

- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

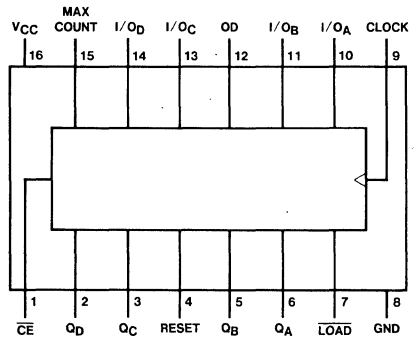
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6588-1

7556 (J) **8556 (N)**

Function Table

Control Inputs					I/O Ports				Active Outputs			
$\overline{LOAD}$	$\overline{CE}$	CLK	OD	Reset	I/O_A	I/O_B	I/O_C	I/O_D	Q_A	Q_B	Q_C	Q_D
H	X	X	L	H	L	L	L	L	L	L	L	L
H	X	X	H	H	Z	Z	Z	Z	L	L	L	L
H	X	L	L	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	X	L	H	L	Z	Z	Z	Z	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	↑	L	L	a	b	c	d	A	B	C	D
H	L	↑	L	L		COUNT				COUNT		
H	L	↑	H	L	Z	Z	Z	Z		COUNT		

The I/O pins are used as inputs when they are TRI-STATED, and the $\overline{LOAD}$ input is Low. They are outputs and active when $\overline{LOAD}$ input is High and OD is Low.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care including transitions

a, b, c, d = The level of the steady state input at inputs A, B, C, D respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D repectively, before the indicated steady state input conditions were established.

Recommended Operating Conditions

Symbol	Parameter		DM7556			DM8556			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	25			25			ns
		Clear	20			20			
		Load	30			30			
$t_{\overline{CE}}$	Count Enable Time	Setup				30			ns
		Hold				−30			
$t_{SETUP(1)}$	Setup Time High Logic Level	Data				25			ns
		Load				30			
$t_{HOLD(1)}$	Hold Time High Logic Level	Data				5			ns
		Load				−10			
$t_{SETUP(0)}$	Setup Time Low Logic Level	Data				30			ns
		Load				25			
$t_{HOLD(0)}$	Hold Time Low Logic Level	Data				5			ns
		Load				−10			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				− 1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				− 40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	− 25		− 70	mA
			DM85	− 25		− 70	
I_{CC}	Supply Current	V_{CC} = Max			75	100	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

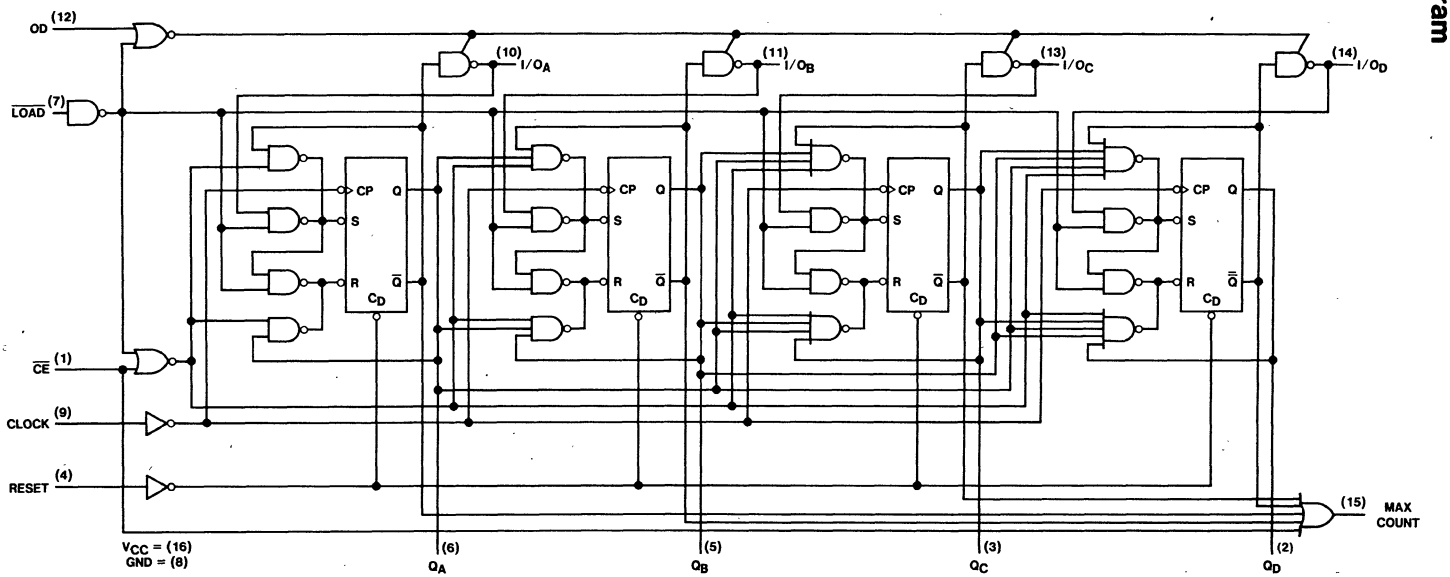
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency					25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output					15	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output					34	44	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to MAX-CNT					23	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to MAX-CNT					23	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Reset to Output					30	44	ns
t_{PZH} Output Enable Time to High Level Output	Output Disable to Q					13	20	ns
t_{PZL} Output Enable Time to Low Level Output	Output Disable to Q					14	20	ns
t_{PHZ} Output Disable Time from High Level Output	Output Disable to Q		6	12				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Disable to Q		12	20				ns

Logic Diagram

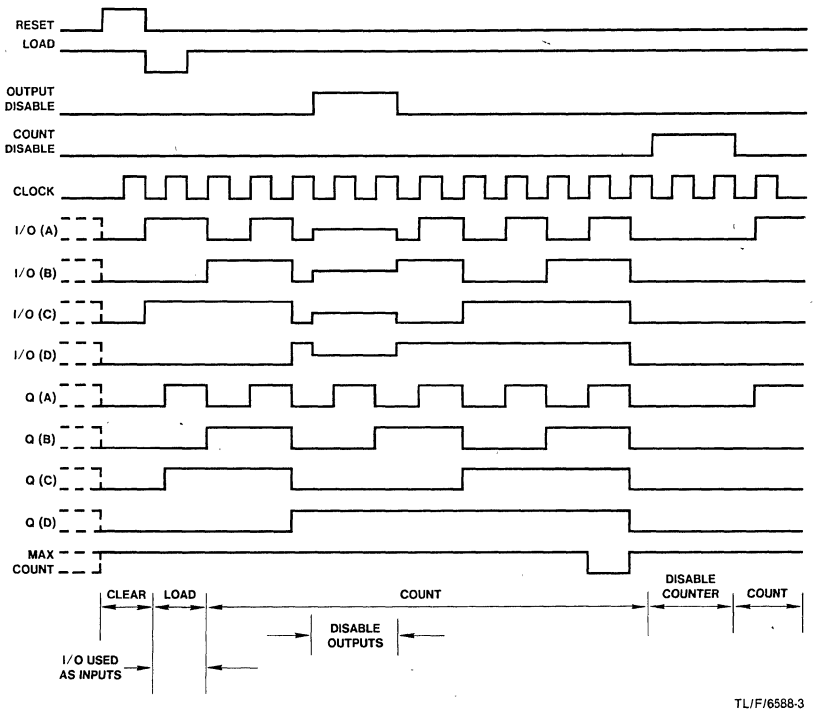
75/8556



TL/F/6588-2

Timing Diagram

75/8556 Typical Clear, Preset, Count, Inhibit Sequence



TL/F/6588-3

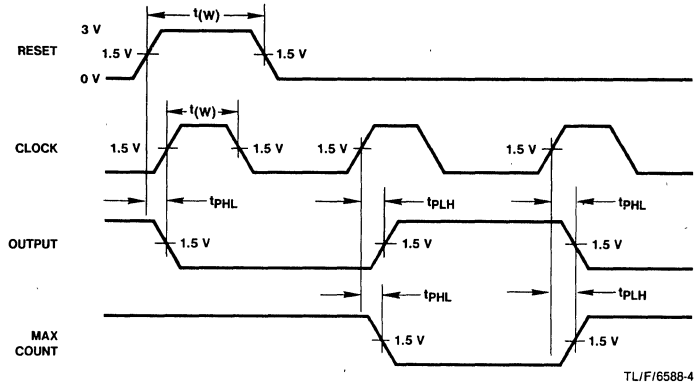
Sequence

(1) Clear to zero.
(2) Load binary five.
(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to one.

6

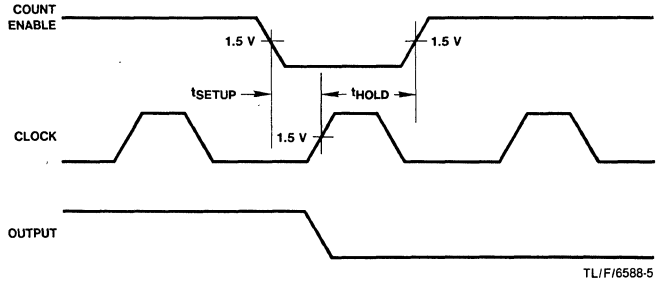
Switching Time Waveforms

Clock and Reset Voltage



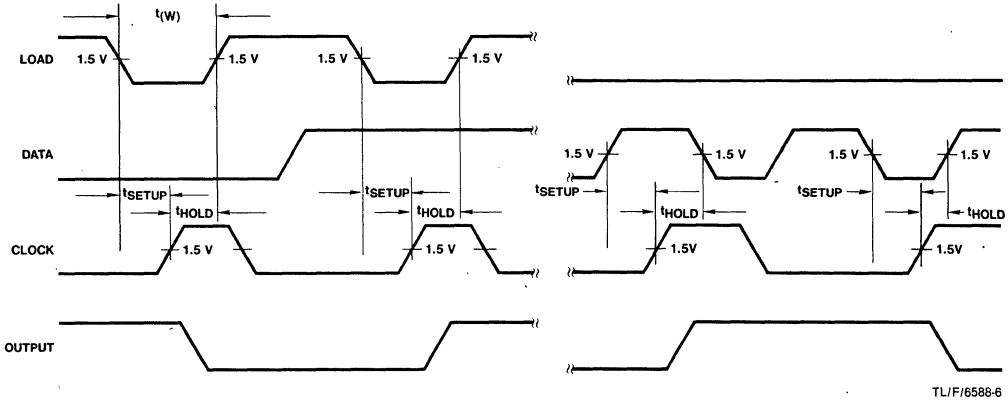
TL/F/6588-4

Count Enable and Clock



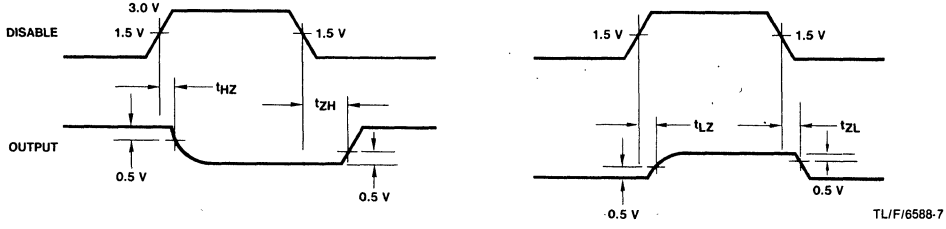
TL/F/6588-5

Load, Data and Clock



TL/F/6588-6

Output Disable



TL/F/6588-7

National Semiconductor

DM7613/DM8613 Dual/Quad Gated Flip-Flops

General Description

The DM7613/8613 is a quad, gated, D-type flip-flop with common clock, common clear, and gated input. When a high logic level is applied to the gated input, data entry to the flip-flop is inhibited.

Features

- Positive-edge triggered
- Do-nothing state
- Buffered inputs
- Typical toggle rate 30 MHz
- Typical power dissipation 290 mW

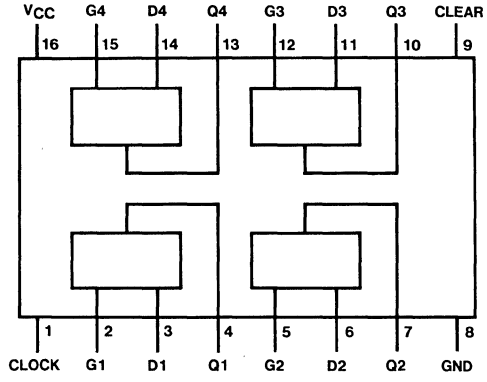
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6590-1

7613 (J) **8613 (N)**

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Recommended Operating Conditions

Symbol	Parameter		DM7613			DM8613			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock	24	16		24	16		ns
		Clear	27	18		27	18		
t_{SU}	Setup Time	D	24	16		24	16		ns
		G	30	21		30	21		
t_H	All Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM76	−18		−55	mA
			DM86	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			58	76	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with CLEAR/CLOCK at 3V, all other inputs at 0V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	30		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		17	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		21	31	ns

Function Table

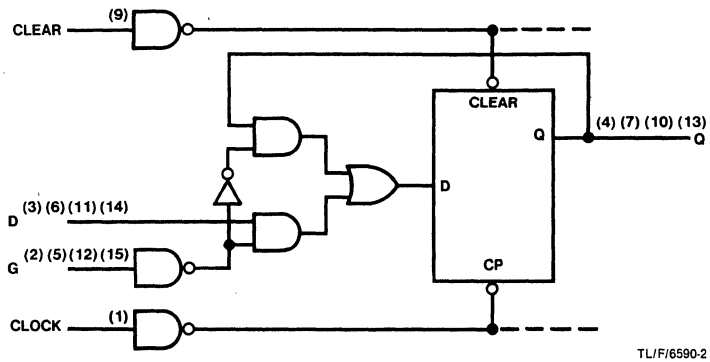
13

D	G	CLR	Q_{n+1}
H	L	L	H
L	L	L	L
X	H	L	Q_n
X	X	H	L*

*Asynchronous Transition
X = Don't Care

Logic Diagram

76/8613



TL/F/6590-2

National Semiconductor

DM7875A/DM8875A, DM7875B/DM8875B TRI-STATE® 4-Bit Parallel Binary Multipliers

General Description

These circuits are capable of multiplying together two 4-bit binary numbers when used together in pairs. The DM7875A/8875A provides the most significant four bits, and the DM7875B/8875B provides the least significant four bits. Since the largest number that can be obtained by multiplying two 4-bit numbers is 225 (15 x 15), the eight output pins (four from each package) are sufficient to produce this number. Both the multiplier and the multiplicand must be connected to the eight input pins of each device. These devices are pin compatible with the SN54284/74284, and SN54285/74285; but have the advantage that these circuits provide either standard totem-pole TTL or TRI-STATE outputs. A gated two-input strobe control is provided. When either one, or both, of the strobe inputs is raised to a high logic level the outputs are forced into the high-impedance state. Thus, multiple devices may be connected to a common bus line.

Features

- Pin compatible replacements for
  SN54284/74284 (DM7875A/8875A)
  SN54285/74285 (DM7875B/8875B)
- TRI-STATE outputs
- Typical propagation delay 35 ns

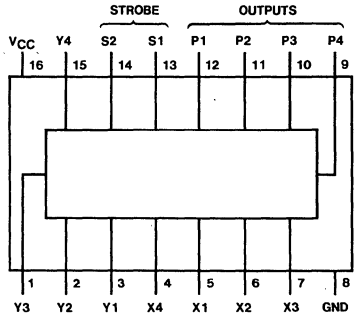
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

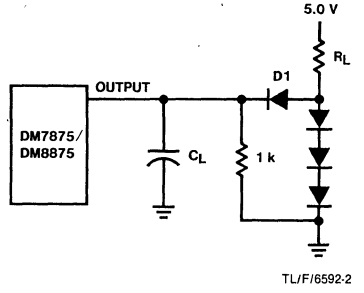
Dual-In-Line Package



TL/F/6592-1

7875A (J) **8875A (N)**
7875B (J) **8875B (N)**

AC Test Circuit



TL/F/6592-2

Recommended Operating Conditions

Symbol	Parameter	DM7875A			DM8875A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

DM78/8875A Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM78	−20		−70	mA
			DM88	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max			75	110	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded.

DM78/8875A Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output					35	60	ns
t_{PZH} Output Enable Time to High Level Output					20	30	ns
t_{PZL} Output Enable Time to Low Level Output					20	30	ns
t_{PHZ} Output Disable Time from High Level Output		20	30				ns
t_{PLZ} Output Disable Time from Low Level Output		20	30				ns

Recommended Operating Conditions

Symbol	Parameter	DM7875B			DM8875B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

DM78/8875B Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM78	−20		−70	mA
			DM88	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			75	110	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

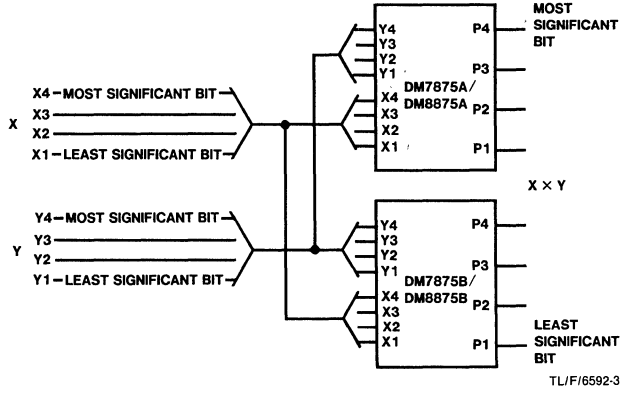
Note 3: I_{CC} is measured with all inputs grounded.

DM78/8875B Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

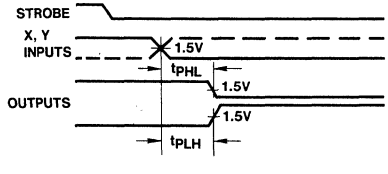
Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output					35	60	ns
t_{PZH} Output Enable Time to High Level Output					20	30	ns
t_{PZL} Output Enable Time to Low Level Output					20	30	ns
t_{PHZ} Output Disable Time from High Level Output		20	30				ns
t_{PLZ} Output Disable Time from Low Level Output		20	30				ns

Typical Application



TL/F/6592-3

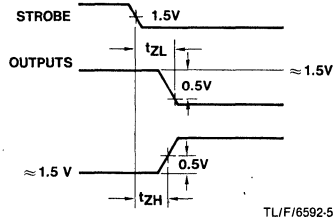
Switching Time Waveforms



INPUT PULSES:
$t_r = t_f \leq 10$ ns
f = 1 MHz

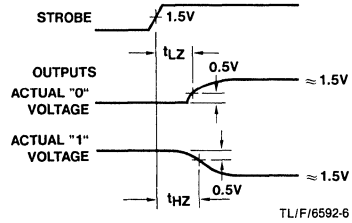
TL/F/6592-4

t_{ZL} & t_{ZH}



TL/F/6592-5

t_{LZ} & t_{HZ}



TL/F/6592-6

National Semiconductor

DM8898/DM8899 TRI-STATE® BCD to Binary/Binary to BCD Converters

General Description

These circuits are the TRI-STATE versions of the popular BCD to binary and binary to BCD converters, DM74184 and DM74185A respectively. They are derived from the 256-bit ROM, DM8598. Emitter connections are made to provide direct read out of converted codes at outputs Y8 though Y1, as shown in the truth tables. Both converters comprehend the fact that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter. Thus a 6-bit converter is produced in each case, and both devices are cascadable.

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go into the high-impedance state. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmmed high.

DM8898 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM8898 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM8898 is programmed to generate BCD 9's complement or BCD 10's complement. In each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table when the devices are connected as shown.

DM8899 BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

Features

- TRI-STATE versions of DM74184, DM74185A
- Typical propagation delay 30 ns

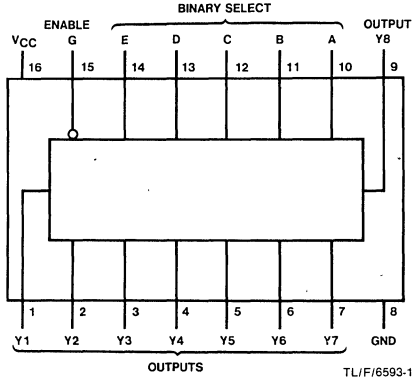
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6593-1

8898 (N) **8899 (N)**

Recommended Operating Conditions

Symbol	Parameter	DM8898			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−5.2	mA
I_{OL}	Low Level Output Current			12	mA
T_A	Free Air Operating Temperature	0		70	°C

DM8898 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max		70	99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

DM8898 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 400\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					29	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output					33	50	ns
t_{PZH} Output Enable Time to High Level Output					16	25	ns
t_{PZL} Output Enable Time to Low Level Output					26	40	ns
t_{PHZ} Output Disable Time from High Level Output		13	20				ns
t_{PLZ} Output Disable Time from Low Level Output		24	36				ns

Recommended Operating Conditions

Symbol	Parameter	DM8899			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−5.2	mA
I_{OL}	Low Level Output Current			12	mA
T_A	Free Air Operating Temperature	0		70	°C

6

DM8899 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA			− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			− 1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			− 40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	− 20		− 70	mA
I_{CC}	Supply Current	V_{CC} = Max		70	99	mA

DM8899 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 400Ω						Units
	C_L = 5 pF			C_L = 50 pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					29	50	ns
t_{PHL} Propagation Delay Time High to Low Level Output					33	50	ns
t_{PZH} Output Enable Time to High Level Output					16	25	ns
t_{PZL} Output Enable Time to Low Level Output					26	40	ns
t_{PHZ} Output Disable Time from High Level Output		13	20				ns
t_{PLZ} Output Disable Time from Low Level Output		24	36				ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Function Tables

BCD-TO-BINARY CONVERTER

BCD WORDS		Inputs (See Note A)						Outputs (See Note B)				
		E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	L	L	L	L	L
2	3	L	L	L	L	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	L	L	L	H	L
6	7	L	L	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	L	L	H	L	L
10	11	L	H	L	L	L	L	L	L	H	L	H
12	13	L	H	L	L	H	L	L	L	H	H	L
14	15	L	H	L	H	L	L	L	L	H	H	H
16	17	L	H	L	H	H	L	L	H	L	L	L
18	19	L	H	H	L	L	L	L	H	L	L	H
20	21	H	L	L	L	L	L	L	H	L	H	L
22	23	H	L	L	L	H	L	L	H	L	H	H
24	25	H	L	L	H	L	L	L	H	H	L	L
26	27	H	L	L	H	H	L	L	H	H	L	H
28	29	H	L	H	L	L	L	L	H	H	H	L
30	31	H	H	L	L	L	L	L	H	H	H	H
32	33	H	H	L	L	H	L	H	L	L	L	L
34	35	H	H	L	H	L	L	H	L	L	L	H
36	37	H	H	L	H	H	L	H	L	L	H	L
38	39	H	H	H	L	L	L	H	L	L	H	H
ANY		X	X	X	X	X	H	Z	Z	Z	Z	Z

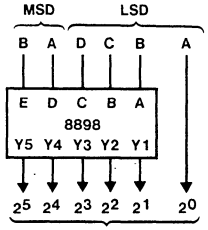
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	Inputs (See Note C)						Outputs (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	Z	Z	Z

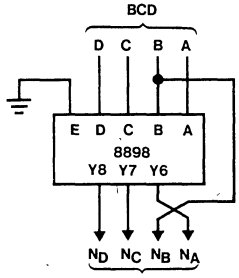
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

6-BIT Converter



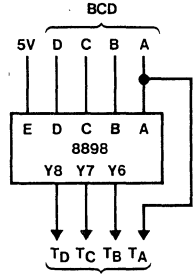
TL/F/6593-2

BCD 9's Complement Converter



TL/F/6593-3

BCD 10's Complement Converter



TL/F/6593-4

Note A: Input conditions other than those shown produce highs at outputs Y1 through Y5.

Note B: Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

Note C: Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

Note D: Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

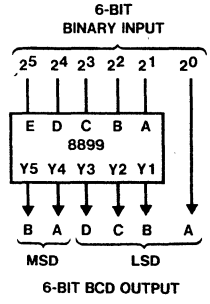
6

Function Tables (Continued)

Binary Words		Inputs						Outputs							
		Binary Select					Enable								
		E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2	3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6	7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10	11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12	13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14	15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16	17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18	19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20	21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22	23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24	25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26	27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28	29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30	31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32	33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34	35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36	37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38	39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40	41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42	43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44	45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46	47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48	49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50	51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52	53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54	55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56	57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58	59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60	61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62	63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL		X	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

6-Bit Converter



TL/F/6593-5

National Semiconductor

DM9002C Quad 2-Input NAND Gates

General Description

The DM9002C device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. The DM9002C circuit offers several significant advantages over 9000 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9002C circuit is in most cases lower than that for the equivalent 9002 type.

The DM9002C circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalent is available for the following SSI type:

DM9000C Series	Equivalent Series 74
DM9002C	DM7400

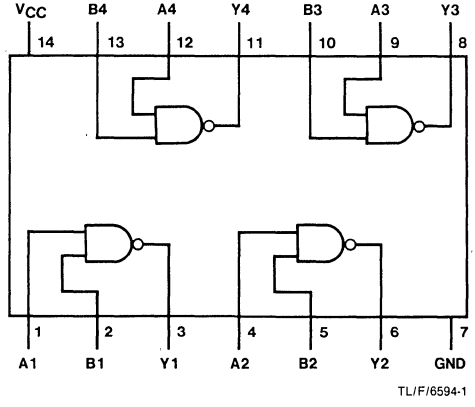
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TL/F/6594-1

9002C (J,N) **9012C (J,N)**

Recommended Operating Conditions

Symbol	Parameter		DM9002C Min	DM9002C Nom	DM9002C Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	0°C	1.9			V
		25°C	1.8			
		75°C	1.6			
V_{IL}	Low Level Input Voltage				0.85	V
I_{OH}	High Level Output Current				−1.2	mA
I_{OL}	Low Level Output Current				50	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Max, I_{OL} = 16 mA V_{IH} = Min				0.45	V
		I_{OL} = 14.1 mA V_{CC} = Min				0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V Other Input at 0V				60	μA
I_{IL}	Low Level Input Current	V_I = 4.5V	V_{CC} = 5.25V			−1.6	mA
			V_{CC} = 4.75V			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−18		−55	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = 5V				1.7	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = 5V				6.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output		3		13	ns
t_{PHL} Propagation Delay Time High to Low Level Output		3		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM9003C Triple 3-Input NAND Gates

General Description

The DM9003C device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. The DM9003C circuit offers several significant advantages over 9003 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9003C circuts is in most cases lower than that for the equivalent 9003 type.

The DM9003C circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalent is available for the following SSI type:

DM9000C Series	Equivalent Series 74
DM9003C	DM7410

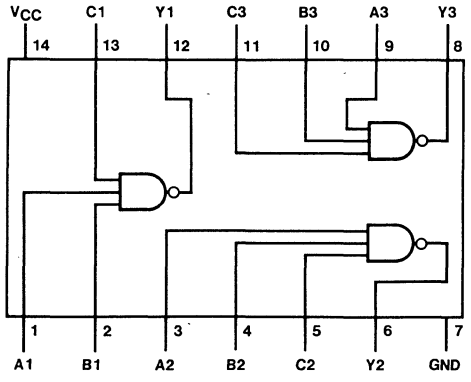
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TL/F/6595-1

9003C (J,N)

Recommended Operating Conditions

Symbol	Parameter		DM9003C Min	DM9003C Nom	DM9003C Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	0°C	1.9			V
		25°C	1.8			
		75°C	1.6			
V_{IL}	Low Level Input Voltage				0.85	V
I_{OH}	High Level Output Current				− 1.2	mA
I_{OL}	Low Level Output Current				50	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Max, I_{OL} = 16 mA V_{IH} = Min				0.45	V
		I_{OL} = 14.1 mA V_{CC} = Min				0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V Other Input at GND				60	μA
I_{IL}	Low Level Input Current	V_I = 4.5V Other Inputs at 5.25V	V_{CC} = Max			− 1.6	mA
			V_{CC} = Min			− 1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		− 18		− 55	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = 5V				1.7	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = 5V				6.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output		3		13	ns
t_{PHL} Propagation Delay Time High to Low Level Output		3		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM9004C Dual 4-Input NAND Gates

General Description

The DM9004C device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. The DM9004C circuit offers several significant advantages over 9000 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9004C circuits is in most cases lower than that for the equivalent 9004 type.

The DM9004C circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalent is available for the following SSI type:

DM9000C Series	Equivalent Series 74
DM9004C	DM7420

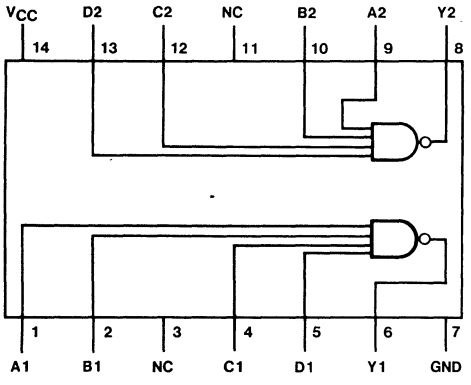
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6596-1

9004C (J,N)

Recommended Operating Conditions

Symbol	Parameter		DM9004C Min	DM9004C Nom	DM9004C Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	0°C	1.9			V
		25°C	1.8			
		75°C	1.6			
V_{IL}	Low Level Input Voltage				0.85	V
I_{OH}	High Level Output Current				−1.2	mA
I_{OL}	Low Level Output Current				50	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Max, I_{OL} = 16 mA V_{IH} = Min				0.45	V
		I_{OL} = 14.1 mA V_{CC} = Min				0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V Other Inputs at GND				60	μA
I_{IL}	Low Level Input Current	V_I = 4.5V Other Inputs at 5.25V	V_{CC} = Max			−1.6	mA
			V_{CC} = Min			−1.41	
I_{OS}	Short Circuit	V_{CC} = Max (Note 2)		−18		−55	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = 5V				1.7	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = 5V				6.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output			3	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output			3	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM9012C Quad 2-Input NAND Gates with Open Collector Outputs

General Description

The DM9012C device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. The DM9012C circuit offers several significant advantages over 9000 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9012C circuits is in most cases lower than that for the equivalent 9012 type.

The DM9012C circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalent is available for the following SSI type:

DM9000C Series	Equivalent Series 74
DM9012C	DM7403

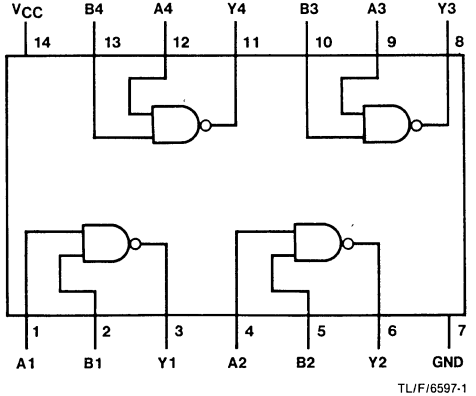
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



TL/F/6597-1

9012C (J,N)

Recommended Operating Conditions

Symbol	Parameter		DM9012C Min	DM9012C Nom	DM9012C Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	0°C	1.9			V
		25°C	1.8			
		75°C	1.6			
V_{IL}	Low Level Input Voltage				0.85	V
V_{OH}	High Level Output Voltage				5.5	V
I_{OL}	Low Level Output Current				50	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Max, I_{OL} = 16 mA V_{IH} = Min				0.45	V
		I_{OL} = 14.1 mA V_{CC} = Min				0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V Other Input at GND				60	μA
I_{IL}	Low Level Input Current	V_I = 4.5V Other Inputs at 5.25V	V_{CC} = Max			− 1.6	mA
			V_{CC} = Min			− 1.41	
I_{CCH}	Supply Current With Outputs High	V_{CC} = 5V				1.7	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = 5V				6.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output		3		45	ns
t_{PHL} Propagation Delay Time High to Low Level Output		3		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM9016C Hex Inverters

General Description

The DM9016C device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. The DM9016C circuit offers several significant advantages over 9000 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9016C circuits is in most cases lower than that for the equivalent 9016 type.

The DM9016C circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalent is available for the following SSI type:

DM9000C Series	Equivalent Series 74
DM9016C	DM7404

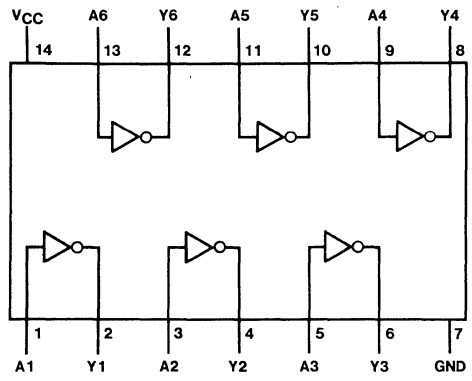
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6598-1

9016C (J,N)

Recommended Operating Conditions

Symbol	Parameter		DM9016C Min	DM9016C Nom	DM9016C Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	0°C	1.9			V
		25°C	1.8			
		75°C	1.6			
V_{IL}	Low Level Input Voltage				0.85	V
I_{OH}	High Level Output Current				−1.2	mA
I_{OL}	Low Level Output Current				50	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Max, I_{OL} = 16 mA, V_{IH} = Min				0.45	V
		I_{OL} = 14.1 mA, V_{CC} = Min				0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V, Other Inputs at 0V				60	μA
I_{IL}	Low Level Input Current	V_I = 4.5V, Other Inputs at 5.25V	V_{CC} = Max			−1.6	mA
			V_{CC} = Min			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−18		−55	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = 5V				1.7	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = 5V				6.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output		3		13	ns
t_{PHL} Propagation Delay Time High to Low Level Output		3		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM9024/DM8024 Dual J-K Flip-Flops with Preset and Clear

General Description

The DM9024 series device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. Thes DM9024 circuits offer several significant advantages over 9024 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9024 circuits is in most cases lower than that for the equivalent 9024 type.

The DM9024 circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalents are available for the following SSI types:

DM9000 Series	Equivalent Series 74
DM9024	DM74109

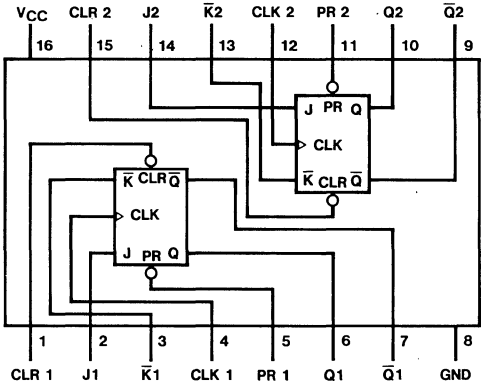
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6599-1

9024 (J) **8024 (N)**

6

Recommended Operating Conditions

Symbol	Parameter		DM9024			DM8024			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5.0	5.5	4.75	5.0	5.25	V
V_{IH}	High Level Input Voltage	T_A = Min	2.0			1.9			V
		T_A = 25°C	1.7			1.8			
		T_A = Max	1.4			1.6			
V_{IL}	Low Level Input Voltage				0.9			0.85	V
I_{OH}	High Level Output Current				−1.2			−1.2	mA
I_{OL}	Low Level Output Current				12.4			14.1	mA
f_{CLK}	Clock Frequency		0	40	30	0	40	30	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	20			20			
		PR, CLR Low	20			20			
t_{SU}	Setup Time (Note 1)		15↑			15↑			ns
t_H	Hold Time (Note 1)		10↑			10↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates rising edge of clock pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				− 1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM90			0.4	V
			DM80			0.45	
		I_{OL} = 16 mA V_{CC} = Max	DM90			0.4	
			DM80			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 4.5V Other Inputs at Ground	J, K			60	μA
			Clock			120	
			Preset			120	
			Clear			240	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.40V (DM90) V_I = 0.45V (DM80) Other Inputs at 4.5V	J, K			− 1.6	mA
			Clock			− 3.2	
			Preset			− 3.2	
			Clear			− 4.8	
		V_{CC} = Min V_I = 0.40V (DM90) Other Inputs at 4.5V	J, K			− 1.24	
			Clock			− 2.48	
			Preset			− 2.48	
			Clear			− 3.72	
		V_{CC} = Min V_I = 0.40V (DM80) Other Inputs at 4.5V	J, K			− 1.41	
			Clock			− 2.82	
			Preset			− 2.82	
			Clear			− 4.23	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM90	− 30		− 85	mA
			DM80	− 30		− 85	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				28	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, first with PRESET at 4.5V and all other inputs grounded, then with CLEAR at 4.5V and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	40		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		18	29	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q, $\overline{Q}$		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q, $\overline{Q}$		19	28	ns

Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	Q0	$\overline{Q}$0
H	H	↓	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

H = High Level (Steady State), L = Low Level (Steady State),
X = Don't Care
↓ = Transition from low to high level
Q0 = The level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable. That is, it will not persist when preset and clear inputs return to their inactive (high) level.

National Semiconductor

DM9300/DM8300 4-Bit Parallel-Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, $J\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the $J\overline{K}$ inputs. These inputs permit the first stage to perform as a $J\overline{K}$, D or T-type flip-flop as shown in the function table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

Features

- Direct replacement for Fairchild 9300
- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

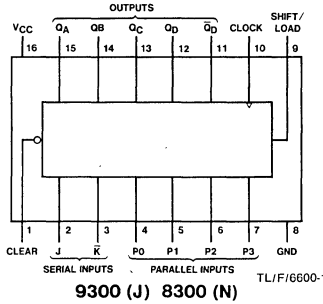
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6600-1

9300 (J) 8300 (N)

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	P0	P1	P2	P3					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from low-to-high level
a, b, c, d = The level of steady state input at P0, P1, P2, or P3, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B or Q_C, respectively, before the most recent ↑ transition of the clock.

Recommended Operating Conditions

Symbol	Parameter		DM9300			DM8300			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		30	0		30	MHz
t_W	Pulse Width	Clock	16	11		16	11		ns
		Clear	30	15		30	15		
t_{SU}	Setup Time	S/L	30	13		30	13		ns
		Data	20	13		20	13		
		Clear	30	13		30	13		
t_H	Data Hold Time		0	−11		0	−11		ns
t_{REL}	S/L Release Time (Note 1)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM93	−18		−55	mA
			DM83	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)	DM93			86	mA
			DM83			92	

Note 1: RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

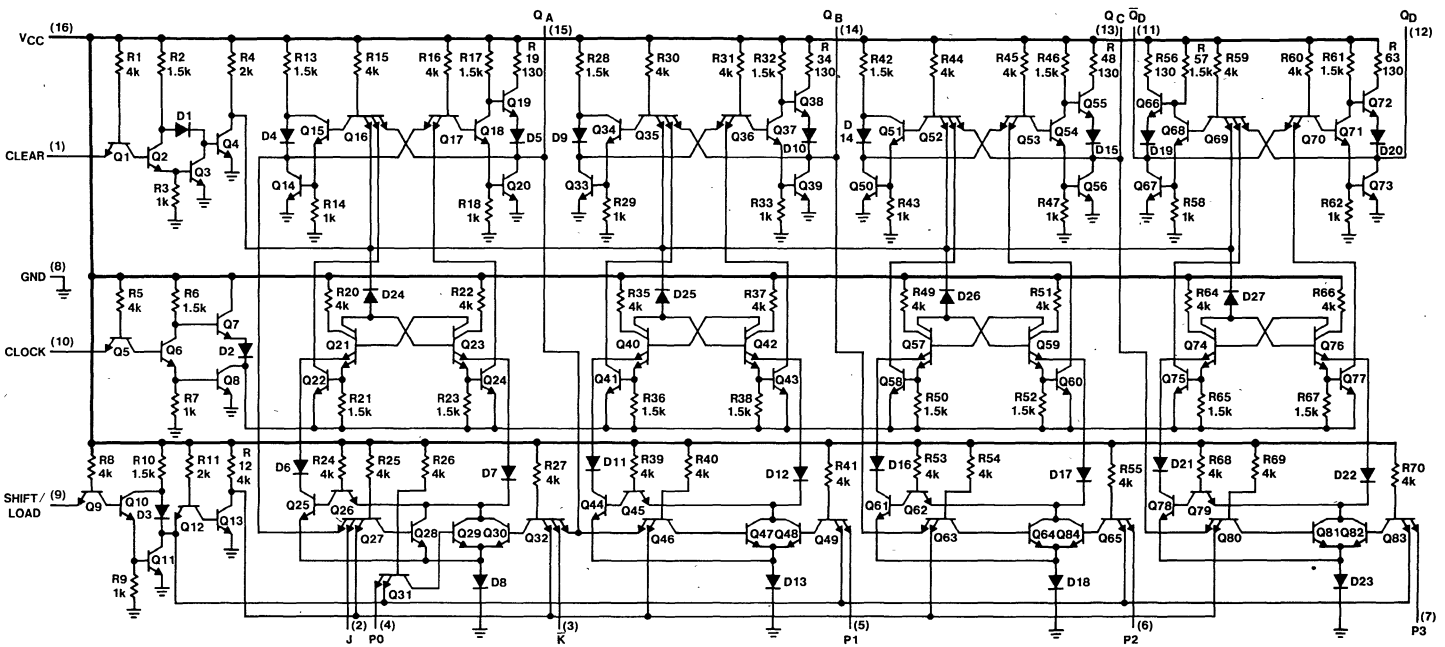
Note 4: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to J, K, and data inputs, I_{CC} is measured by applying momentary ground, then 4.5V to CLEAR, and then to CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		30	39		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		14	22	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		19	30	ns

Schematic Diagram

DM93/8300



TL/F/6600-2

National Semiconductor

DM9301/DM8301 1 of 10 Decoders

General Description

These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.

These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1 V and power dissipation is typically 125 mW. The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

Features

- Direct replacement for Fairchild 9301 and Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns

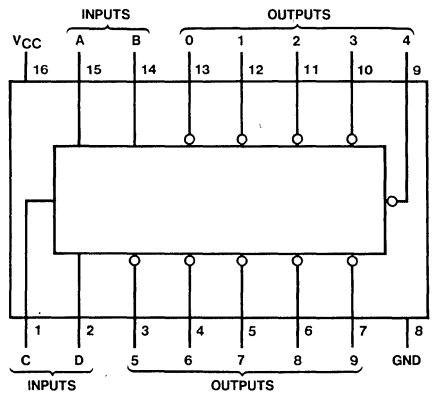
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6601-1

9301 (J) 8301 (N)

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Recommended Operating Conditions

Symbol	Parameter	DM9301			DM8301			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−55	mA
			DM83	−20		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			25	41	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	C_L = 15 pF, R_L = 400Ω			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output			19	30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

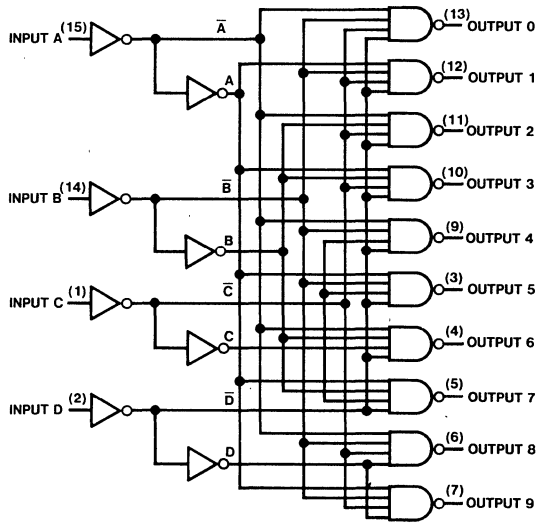
Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Logic Diagram

DM93/8301



TL/F/6601-2

6

National Semiconductor

DM9309/DM8309 Dual 4-Bit Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

The DM9309/8309 contains two separate 4-bit multiplexers with complementary Y and $\overline{Y}$ outputs; however, the two sections have common address select inputs.

Features

DM9309/8309

- Direct replacement for Fairchild 9309
- Complementary outputs
- Dual one-of-four data selectors

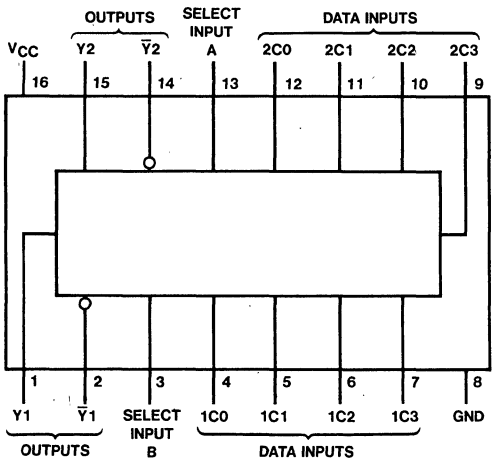
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6602-1

9309 (J) 8309 (N)

Function Table

Inputs						Outputs	
Select		Data				Y	$\overline{Y}$
B	A	C0	C1	C2	C3		
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	H	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care.

Recommended Operating Conditions

Symbol	Parameter	DM9309			DM8309			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.4	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−30		−85	mA
			DM83	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			27	44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

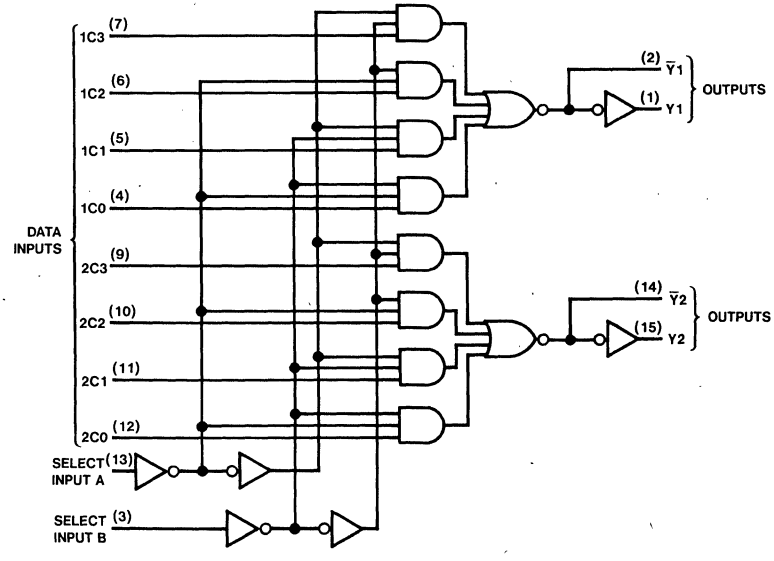
Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		27	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		23	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		17	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		20	29	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		23	34	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		9	13	ns

Logic Diagram

DM93/8309



TL/F/6602-2

National Semiconductor

DM9310/DM8310 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9310/DM8310 are decade counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-foward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Direct replacement for Fairchild 9310
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters
  9310 — 54160A/74160A (decade)

Absolute Maximum Ratings (Note 1)

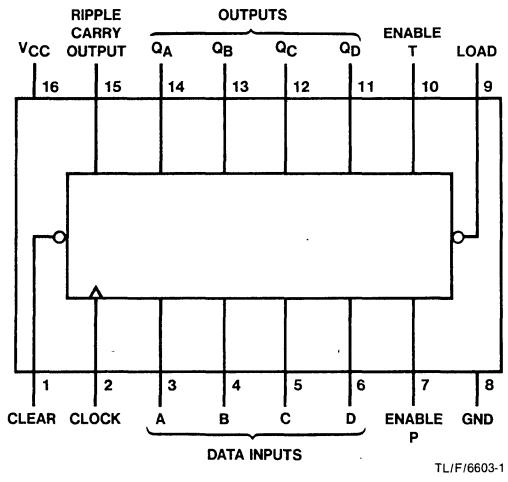
Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

6

Connection Diagram

Dual-In-Line Package



TL/F/6603-1

9310 (J) 8310 (N)

Recommended Operating Conditions

Symbol	Parameter		DM9310			DM8310			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.4	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Note 1)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	CLK, EN T			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	CLK, EN T			−3.2	μA
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−57	mA
			DM83	−18		−57	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)	DM93		59	85	mA
			DM83		59	94	
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)	DM93		63	91	mA
			DM83		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

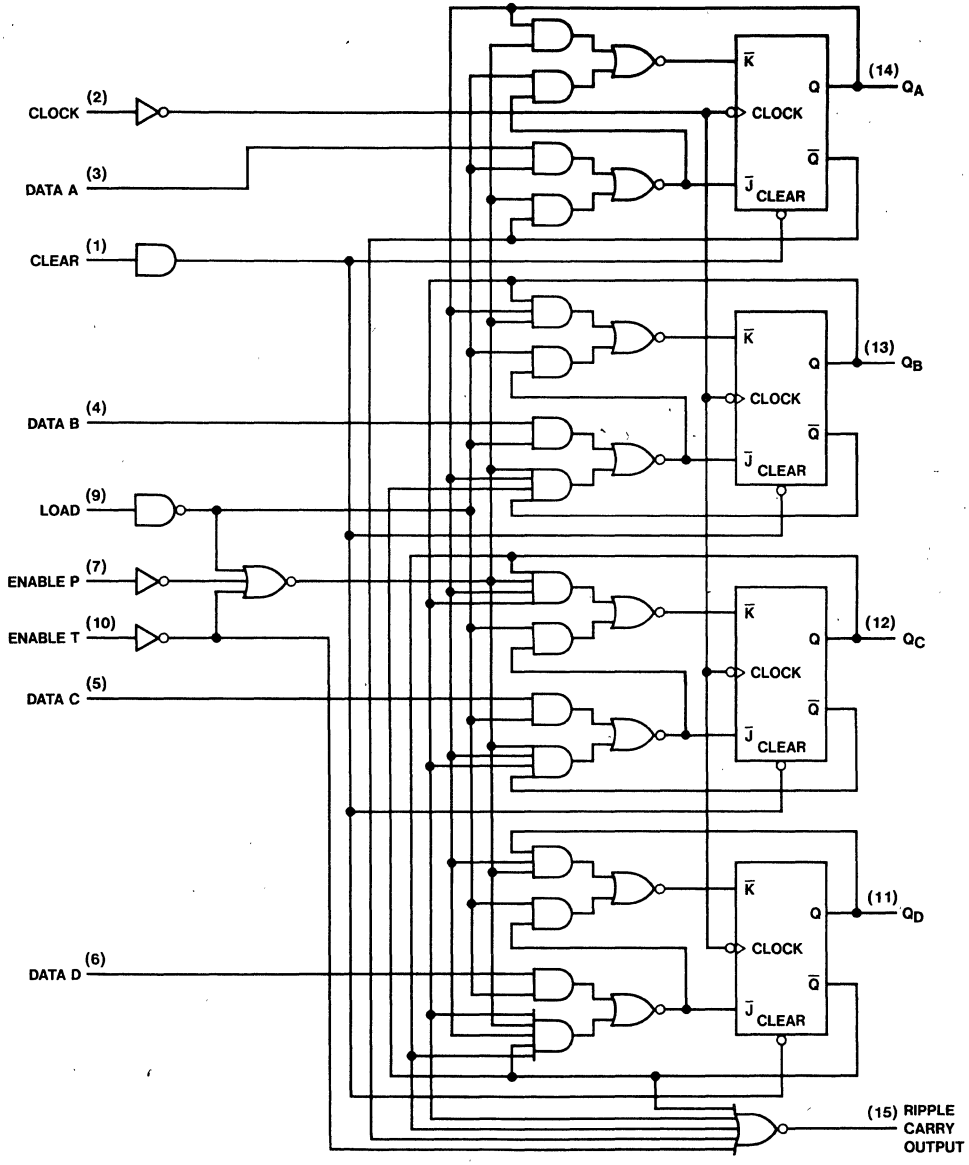
Note 4: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		14	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		16	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		18	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		24	36	ns

Logic Diagram

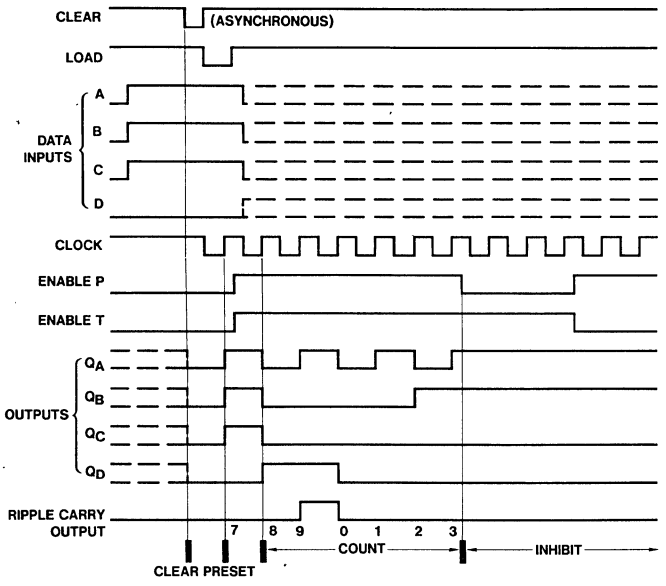
DM93/8310



TL/F/6603-2

Timing Diagram

9310/8310 Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequences

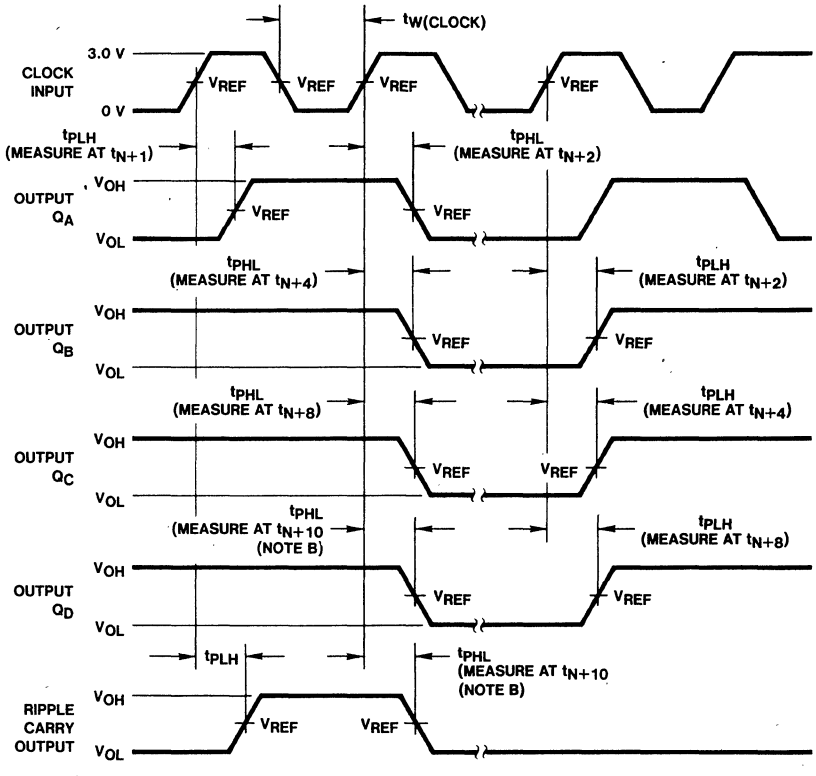


TL/F/6603-3

Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms



TL/F/6603-4

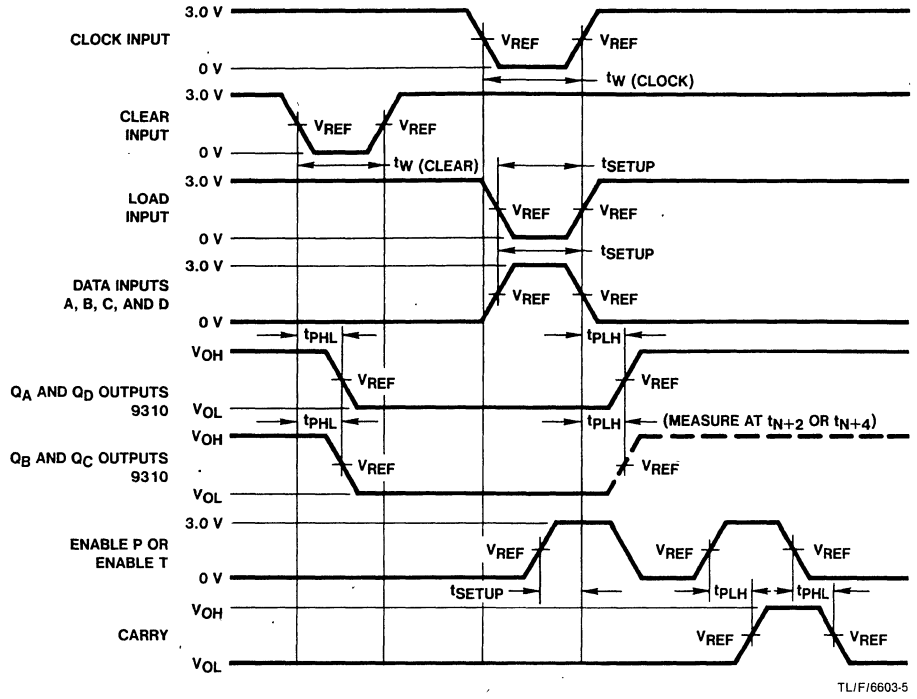
Note A: The input pulses are supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\ \Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for 9310/8310, where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5$ V.

Parameter Measurement Information (Continued)

Switching Time Waveforms



TL/F/6603-5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\ \Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
Note B: Enable P and enable T setup times are measured at t_{n+10} for 8310/9310.
Note C: $V_{REF} = 1.5$ V.

6

National Semiconductor

DM9311/DM8311 4-Line to 16-Line Decoders/Demultiplexers

General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Direct replacement for Fairchild 9311
- Pin for pin with popular 54154/74154
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay 19 ns
- Typical power dissipation 170 mW

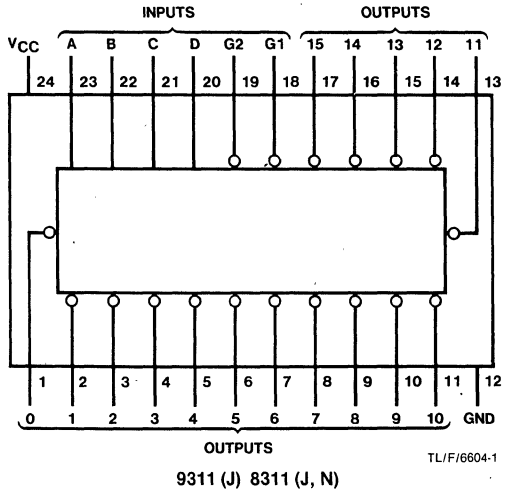
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6604-1

9311 (J) 8311 (J, N)

Recommended Operating Conditions

Symbol	Parameter	DM9311			DM8311			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−55	mA
			DM83	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM93		34	49	mA
			DM83		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		21	30	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		17	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		18	27	ns

Function Table

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
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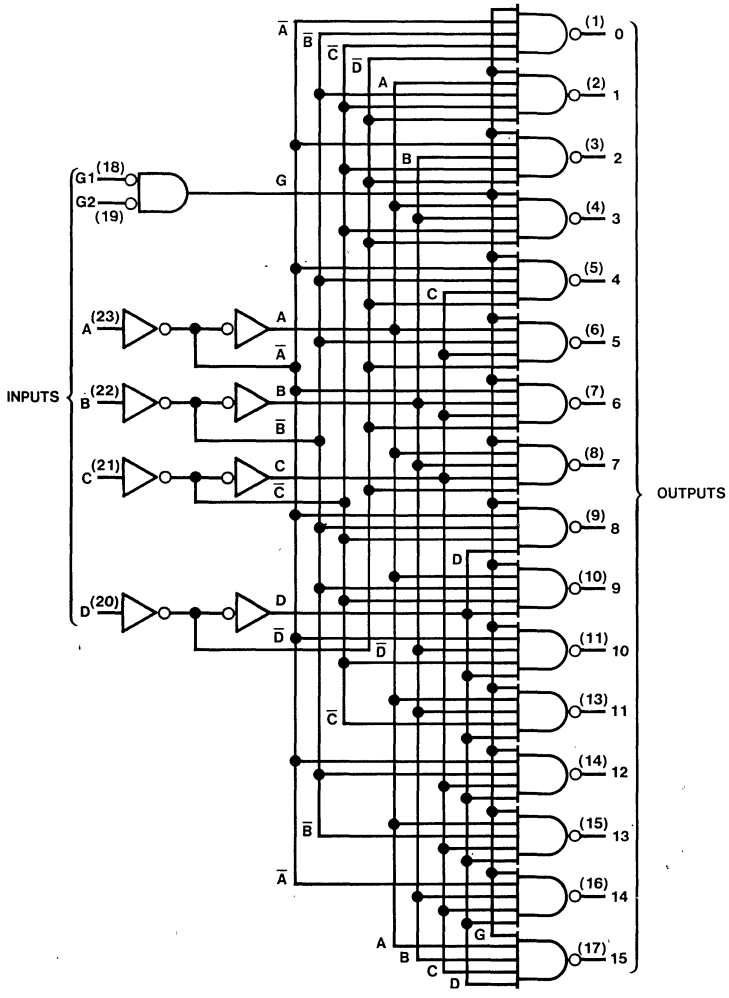
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Logic Diagram

DM93/8311



TL/F/6604-2

National Semiconductor

DM9312/DM8312 Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

The DM9312/8312 is a single 8-bit multiplexer with complementary outputs and a strobe control. When the strobe is low, the function is enabled. When a high logic level is applied to the strobe, the output is forced to the logic zero state regardless of the logic level of the data inputs.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

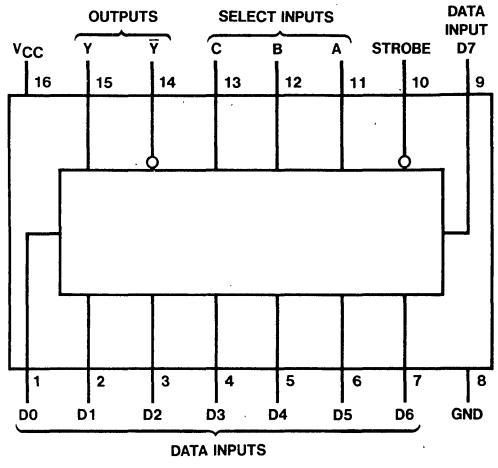
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Features

- Direct replacement for Fairchild 9312
- Selects one-of-eight data sources
- Performs parallel to serial conversion
- Strobe controlled outputs
- Complementary outputs

Connection Diagrams

Dual-In-Line Package



TL/F/6605-1

9312 (J) 8312 (N)

Function Tables

DM93/8312

Inputs				Outputs	
Select			Strobe	Y	$\overline{Y}$
C	B	A	G		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care.
D0, D1 . . . D7 = The level of the respective D input.

Recommended Operating Conditions

Symbol	Parameter	DM9312			DM8312			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−30		−85	mA
			DM83	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			27	44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

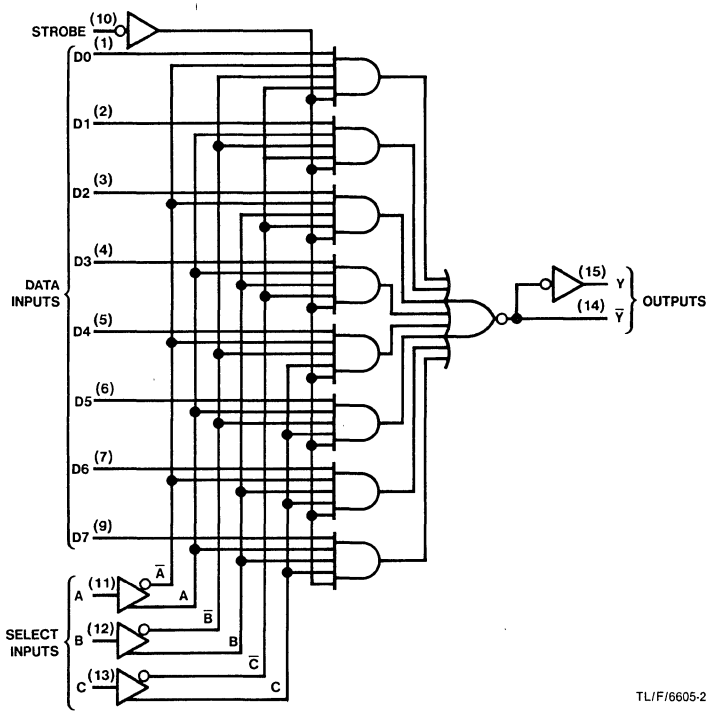
Note 3: I_{CC} is measured with the STROBE and DATA SELECT inputs at 4.5V and all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		23	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		18	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		16	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		16	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		17	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		9	13	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		9	13	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		22	33	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		21	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to $\overline{Y}$		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to $\overline{Y}$		15	21	ns

Logic Diagram

DM93/8312



TL/F/6605-2

National Semiconductor

DM9316/DM8316 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9316/DM8316 is a 4-bit binary counter. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enables inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-foward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Direct replacement for Fairchild 9316
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters

  9316 — 54161A/74161A (binary)

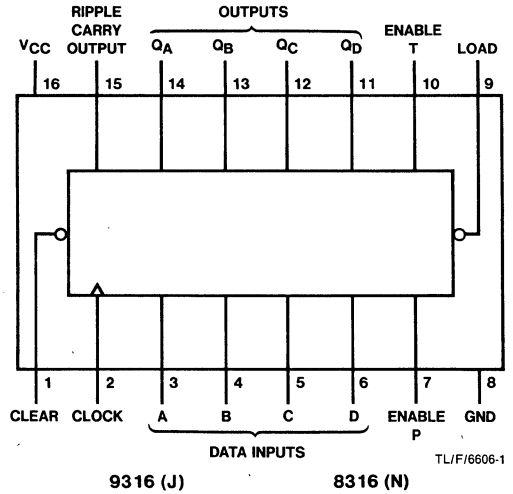
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



9316 (J) **8316 (N)**

Recommended Operating Conditions

Symbol	Parameter		DM9316			DM8316			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.4	5.0	5.5	4.75	5.0	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		25	0		25	MHz
t_W	Pulse Width	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Note 1)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Clock			80	μA
			Enable T			80	
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−3.2	μA
			Enable T			−3.2	
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM93	−20		−57	mA
			DM83	−18		−57	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 4)	DM93		59	85	mA
			DM84		59	94	
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 5)	DM93		63	91	mA
			DM83		63	101	

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

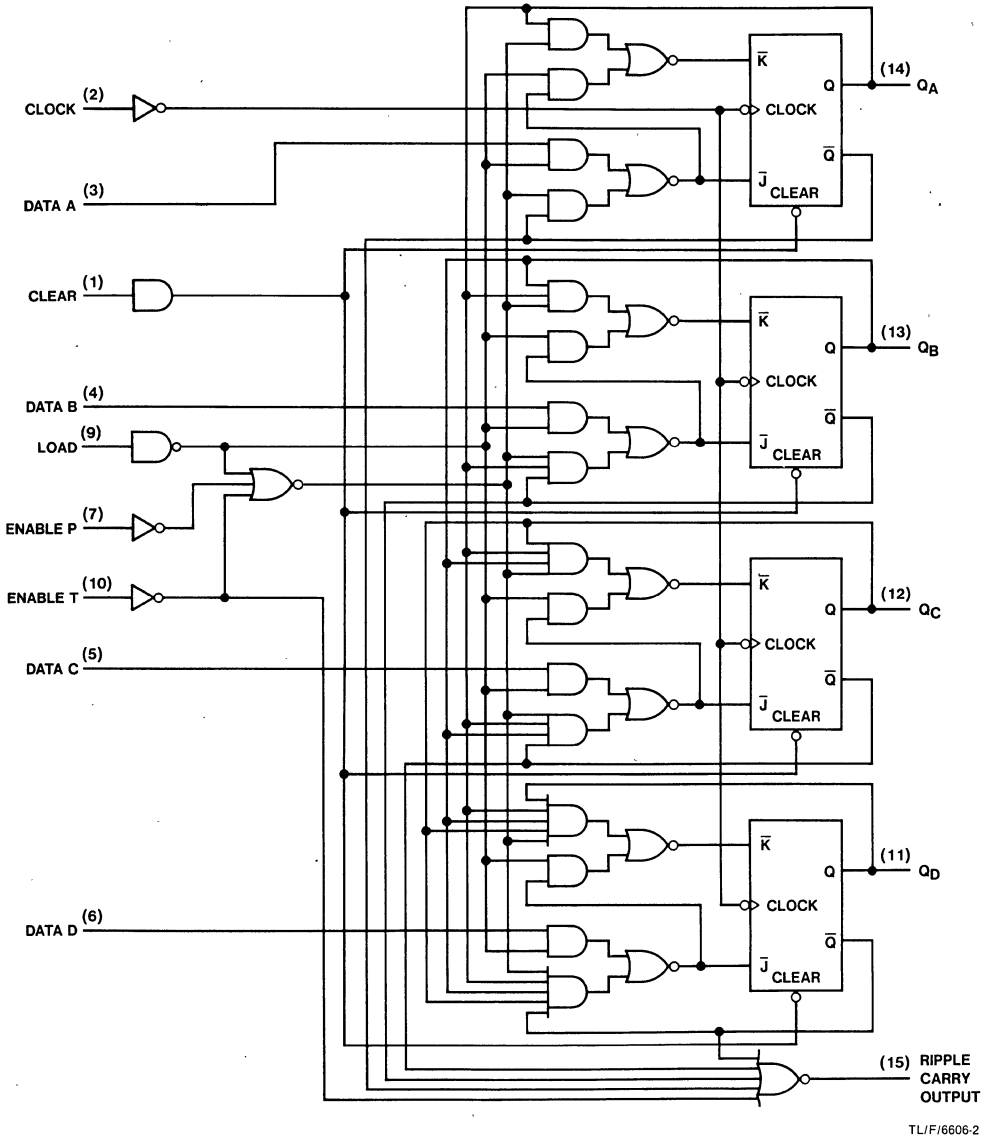
Note 5: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		25	35		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to RC		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to RC		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		14	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		16	23	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		18	25	ns
t_{PLH} Propagation Delay Time Low to High Level Output	ENT to RC		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	ENT to RC		12	16	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		24	36	ns

Logic Diagram

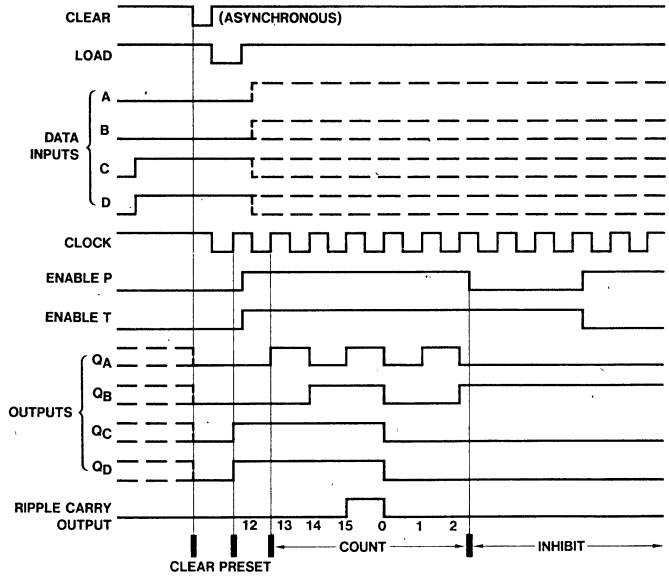
DM93/8316



TL/F/6606-2

Timing Diagram

9316/8316 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences

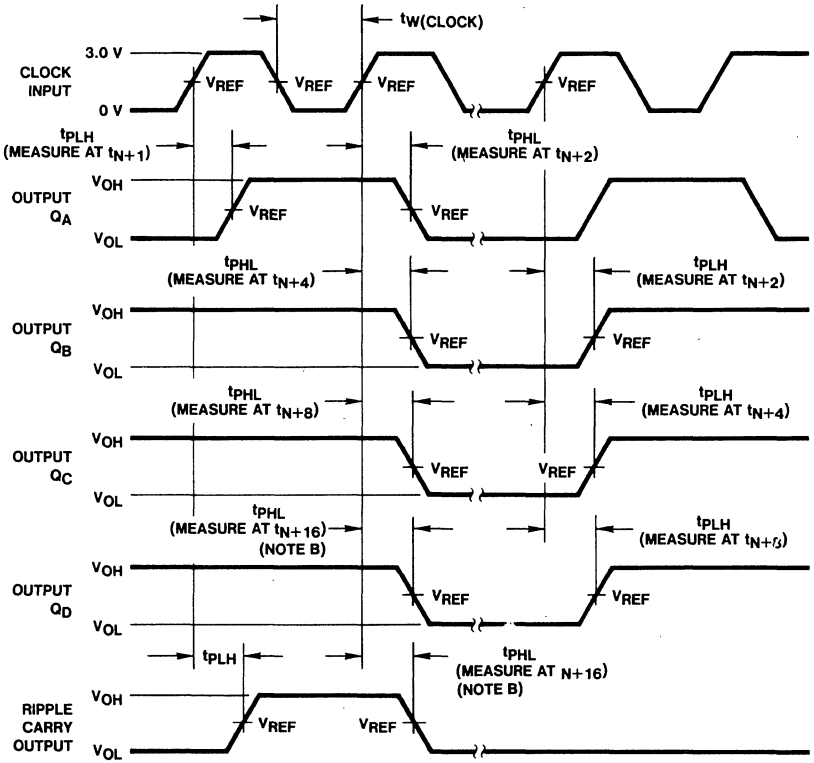


TL/F/6606-3

Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms



TL/F/6606-4

Note A: The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\,\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

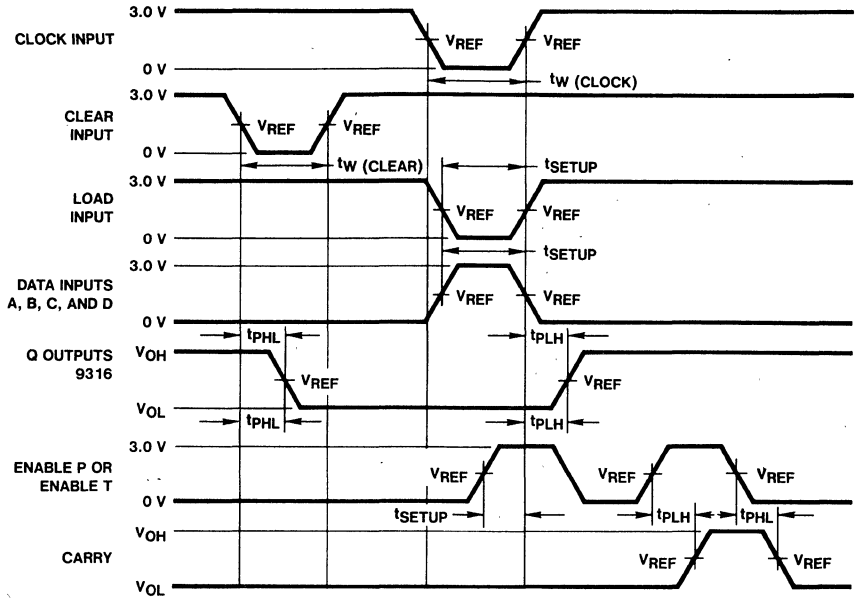
Note B: Outputs Q_D and carry are tested at t_{n+16} for 9316/8316, where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5$ V.

6

Parameter Measurement Information (Continued)

Switching Time Waveforms



TL/F/6606-5

Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\ \Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
Note B: Enable P and enable T setup times are measured at t_{n+16} for 8316/9316.
Note C: $V_{REF} = 1.5$ V.

National Semiconductor

DM9318/DM8318 Priority Encoders

General Description

These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Direct replacement for Fairchild 9318
- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

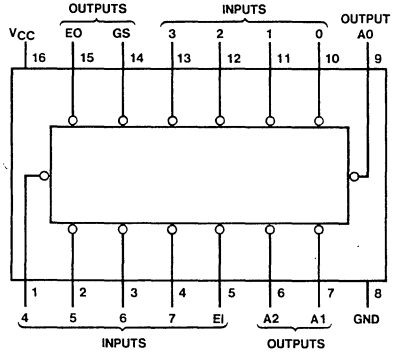
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6607-1

9318 (J) 8318 (N)

Function Table

Inputs									Outputs				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

6

Recommended Operating Conditions

Symbol	Parameter	DM9318			DM8318			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−35		−85	mA
			DM83	−35		−85	
I_{CC1}	Supply Current Condition 1	V_{CC} = Max (Note 3)			35	55	mA
I_{CC2}	Supply Current Condition 2	V_{CC} = Max (Note 4)			40	60	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with all inputs and outputs open.

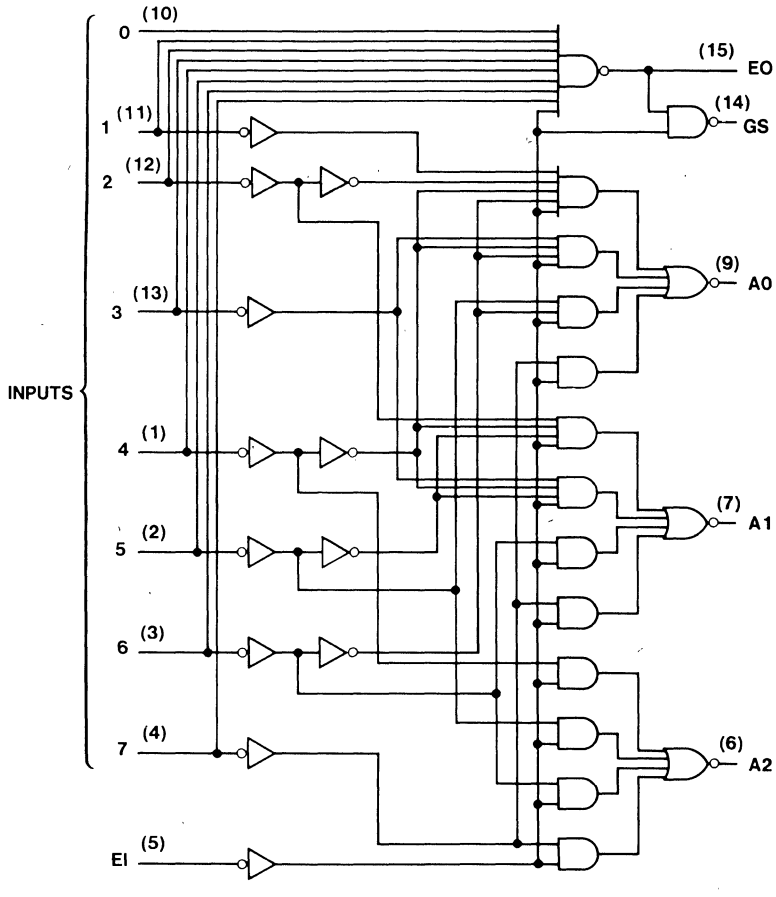
Note 4: I_{CC2} is measured with inputs 7 and EI grounded and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD In Phase		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD In Phase		9	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD Out of Phase		13	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD Out of Phase		12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 7 to E0 Out of Phase		6	9	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 7 to E0 Out of Phase		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	0 thru 7 to GS In Phase		18	27	ns
t_{PHL} Propagation Delay Time High to Low Level Output	0 thru 7 to GS In Phase		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	EI to A0, 1, 2 In Phase		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	EI to A0, 1, 2 In Phase		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	EI to GS In Phase		8	12	ns
t_{PHL} Propagation Delay Time High to Low Level Output	EI to GS In Phase		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	EI to E0 In Phase		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	EI to E0 In Phase		17	26	ns

Logic Diagram

DM93/8318



TL/F/6607-2

National Semiconductor

DM9322/DM8322 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

Features

- Direct replacement for Fairchild 9322
- Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

Applications

- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

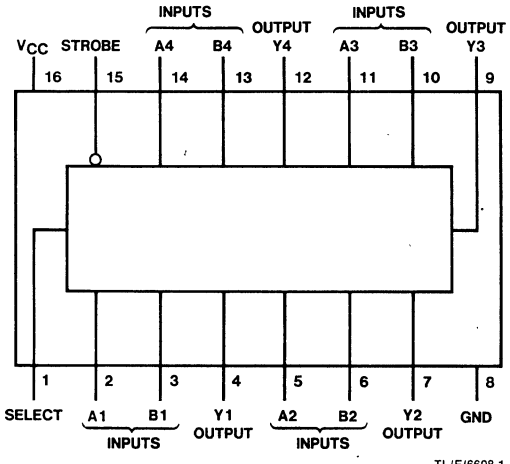
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6608-1

9322 (J) 8322 (N)

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

6

Recommended Operating Conditions

Symbol	Parameter	DM9322			DM8322			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−55	mA
			DM83	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

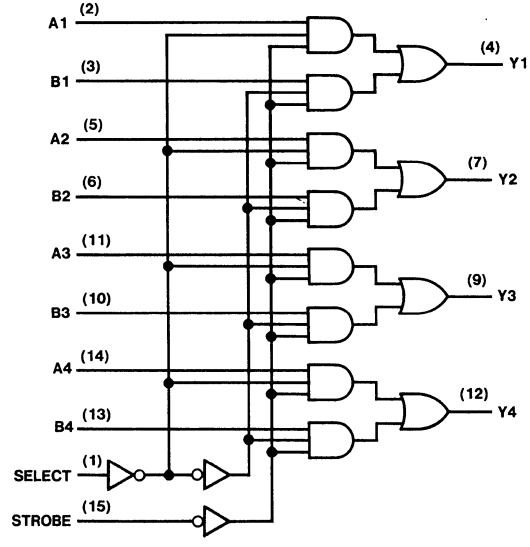
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		8	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		10	14	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		13	20	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output		15	23	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output		17	27	ns

Logic Diagram

DM93/8322



TL/F/6608-2

National Semiconductor

DM9334/DM8334 8-Bit Addressable Latches

General Description

The DM9334/DM8334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334/DM8334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The function tables summarize the operation of the product.

Features

- Direct replacement for Fairchild 9334
- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability

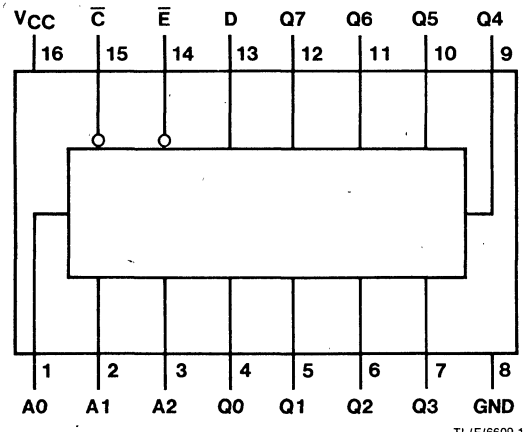
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6609-1

9334 (J) 8334 (N)

Recommended Operating Conditions

Symbol	Parameter		DM9334			DM8334			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	ENABLE Pulse Width (Fig. 1)		19	13		19	13		ns
t_{SU}	Setup Time	Data 1 (Fig. 4)	20	13		20	13		ns
		Data 0 (Fig. 4)	20	14		20	14		
		Address (Fig. 6) (Note 1)	10	5		10	5		
t_H	Hold Time	Data 1 (Fig. 4)	0	−10		0	−10		ns
		Data 0 (Fig. 4)	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	$\overline{E}$ Input			60	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	$\overline{E}$ Input			−2.4	μA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM93	−30		−100	mA
			DM83	−30		−100	
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Note 1: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Enable to Output Fig. 1		19	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable to Output Fig. 1		18	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output Fig. 2		24	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output Fig. 2		19	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Address to Output Fig. 3		23	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Address to Output Fig. 3		21	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output Fig. 5		21	31	ns

Function Tables

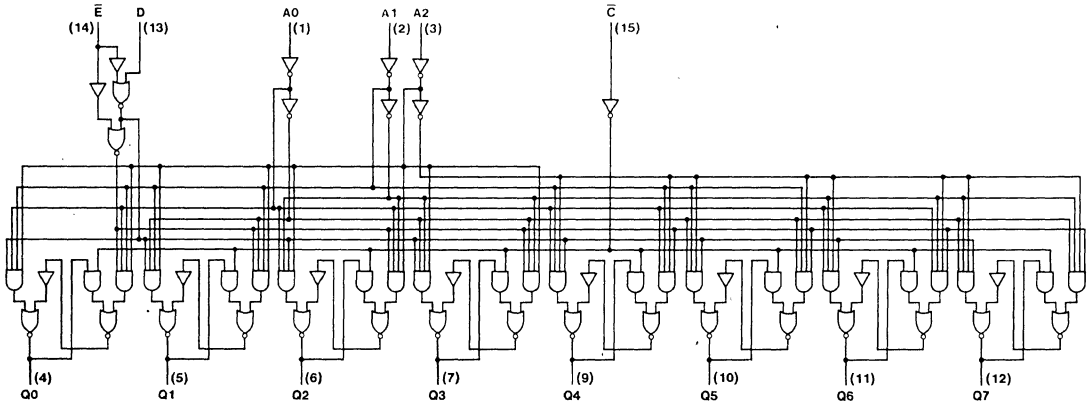
$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active High Eight Channel Demultiplexer
H	L	Clear

X = Don't Care Condition
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State

Inputs						Present Output States								Mode
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					Addressable Latch
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

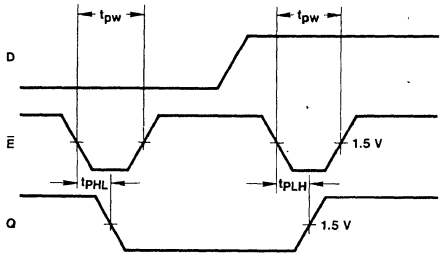
Logic Diagram

DM93/8334



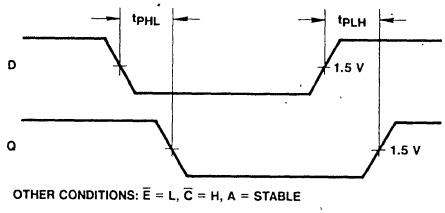
TL/F/6609-2

Switching Time Waveforms



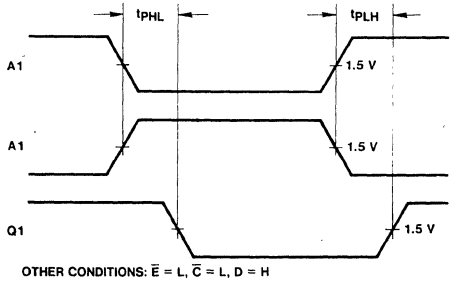
TL/F/6609-3

FIGURE 1



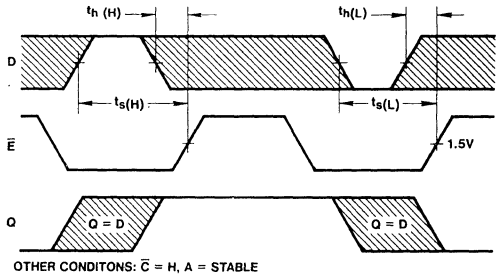
TL/F/6609-4

FIGURE 2



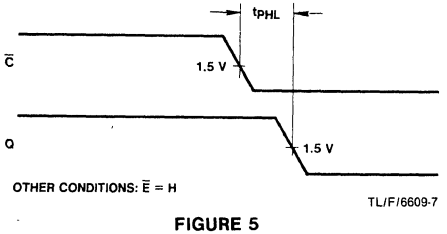
TL/F/6609-5

FIGURE 3



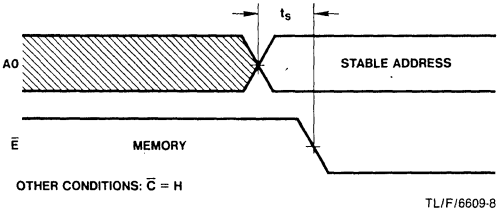
TL/F/6609-6

FIGURE 4



TL/F/6609-7

FIGURE 5



TL/F/6609-8

FIGURE 6

Note: The shaded areas indicate when the inputs are permitted to change for predictable output performance.

National Semiconductor

DM9601/DM8601 Retriggerable One Shots

General Description

These retriggerable one shots provide the designer with four inputs; two active high and two active low. This permits a choice of either leading-edge or trailing-edge triggering, independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge again. The retriggerable feature allows for output pulse widths to be expanded. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. Retriggering may be inhibited by tying the $\overline{Q}$ output to an active low input.

Features

- High speed operation—input repetition rate > 10 MHz
- Flexibility of operation—optional retriggering/lock-out capability
- Output pulse width range—50 ns to ∞
- Leading or trailing edge triggering
- Complementary outputs/inputs
- Input clamping diodes
- DTL/TTL compatible logic levels

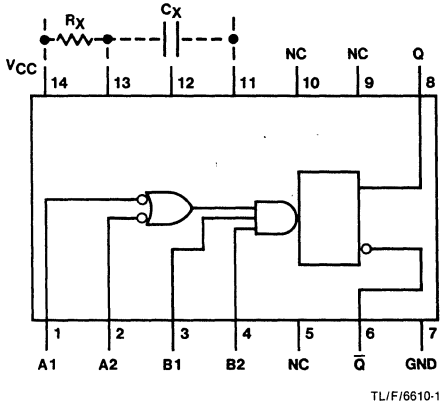
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6610-1

9601 (J) 8601 (N)

Function Table

Inputs				Outputs	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎍
L	X	H	↑	⎍	⎍
X	L	H	H	L	H
X	L	↑	H	⎍	⎍
X	L	H	↑	⎍	⎍
H	↓	H	H	⎍	⎍
↓	↓	H	H	⎍	⎍
↓	H	H	H	⎍	⎍

Recommended Operating Conditions

Sym	Parameter		DM9601			DM8601			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.6			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.72			−0.96	mA
I_{OL}	Low Level Output Current				10			12.8	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min (Note 4)	DM96			0.4	V
			DM86			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V				60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	DM96 V_{IN} = 0.40V			−1.6	mA
			DM86 V_{IN} = 0.45V			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Notes 2 and 4)	DM96	−10		−40	mA
			DM86	−10		−40	
I_{CC}	Supply Current	V_{CC} = Max				25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Unless otherwise noted, R_X = 10k between PIN 13 and V_{CC} on all tests.

Note 4: Ground PIN 11 for V_{OL} test on PIN 6, V_{OH} and I_{OS} tests on PIN 8. Open PIN 11 for V_{OL} test on PIN 8, V_{OH} and I_{OS} tests on PIN 6.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output	Negative Trigger Input to True Output	$C_L = 15$ pF, $C_X = 0$, $R_X = 5$ kΩ		25	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Negative Trigger Input to Complement Output			25	40	ns
$t_{PW(MIN)}$ Minimum True Output Pulse Width				45	65	ns
t_{PW} Pulse Width		$R_X = 10$ kΩ, $C_X = 1000$ pF	3.08	3.42	3.76	μs
C_{STRAY} Maximum Allowable Wiring Capacitance		Pin 13 to GND			50	pF
R_X External Timing Resistor		DM96	5		25	kΩ
R_X External Timing Resistor		DM86	5		50	kΩ

Operating Rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown in switching characteristics. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{PW} may be calculated as follows:

$$t_{PW} = K R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X > 10^3 \text{ pF)}$$
$$K \approx 0.34$$

   R_X in kΩ, C_X in pF and t_{PW} in ns.
   (For $C_X < 10^3$ pF, see curve.)
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$.
4. Set-up time (t_1) for input trigger pulse must be > 40 ns. (See *Figure 1*).
   Release time (t_2) for input trigger pulse must be > 40 ns. (See *Figure 2*).

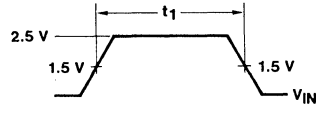


FIGURE 1

TL/F/6610-2

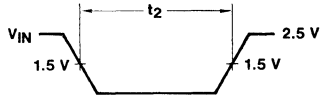


FIGURE 2

TL/F/6610-3

5. Retrigger pulse width (see *Figure 3*) is calculated as follows:

$$t_W = t_{PW} + t_{PLH} = K R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{PLH}$$

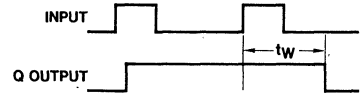
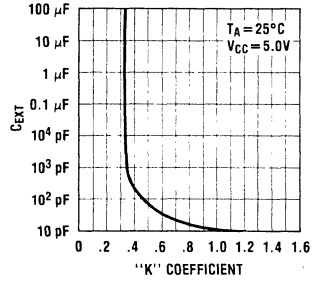


FIGURE 3

TL/F/6610-4

TYPICAL "K" COEFFICIENT VARIATION VS TIMING CAPACITANCE

The multiplicative factor "K" varies as a function of the timing capacitor, C_X. The graph below details this characteristic:

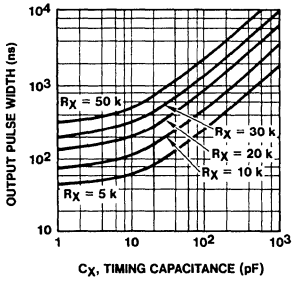


TL/F/6610-5

*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

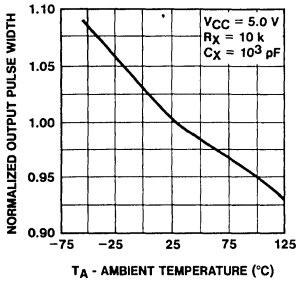
Typical Performance Characteristics

Output Pulse Width vs Timing Resistance And Capacitance For $C_X < 10^3$ pF



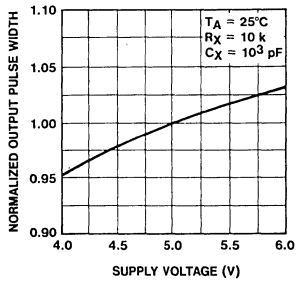
TL/F/6610-6

Normalized Output Pulse Width vs Ambient Temperature



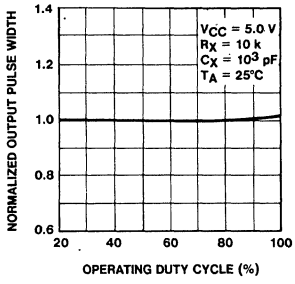
TL/F/6610-7

Normalized Output Pulse Width vs Supply Voltage



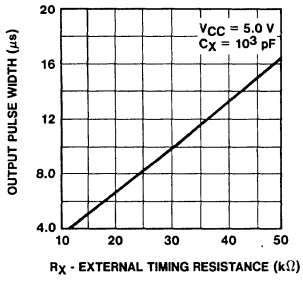
TL/F/6610-8

Normalized Output Pulse Width vs Operating Duty Cycle



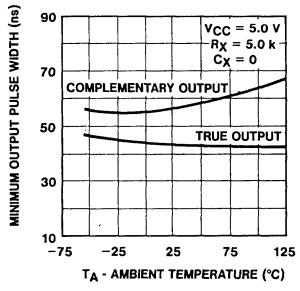
TL/F/6610-9

Pulse Width vs Timing Resistance



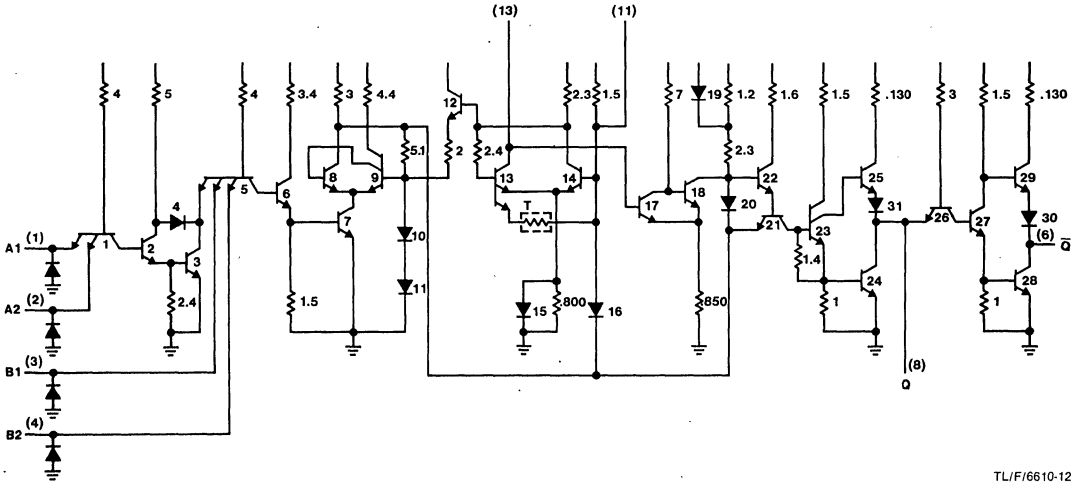
TL/F/6610-10

Output Pulse Width vs Ambient Temperature



TL/F/6610-11

Schematic Diagram



TL/F/6610-12

National Semiconductor

DM9602/DM8602 Dual Retriggerable, Resettable One Shots

General Description

These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active high input, or the $\overline{Q}$ output to an active low input.

Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for V_{CC} and temperature variations

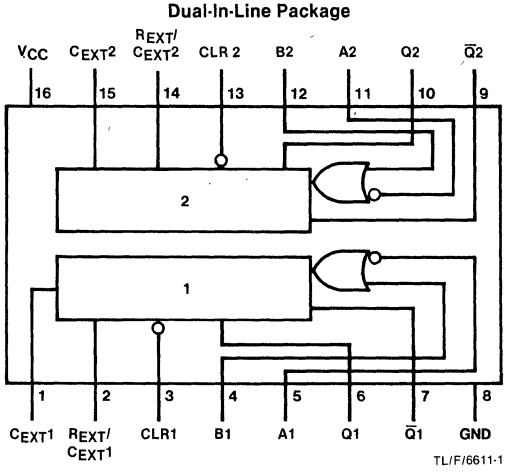
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6611-1

9602 (J) 8602 (N)

Function Table

Pin No's. A	Pin No's. B	Pin No's. CLR	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Recommended Operating Conditions

Sym	Parameter		DM9602			DM8602			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.65			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM96			0.4	V
			DM86			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V				60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	DM96 V_I = 0.40V			−1.6	mA
			DM86 V_I = 0.45V			−1.6	
		V_{CC} = Min	DM96 V_I = 0.40V			−1.24	
			DM86 V_I = 0.45V			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Notes 2 and 4)	DM96			−25	mA
			DM86			−35	
I_{CC}	Supply Current	V_{CC} = Max	DM96		39	45	mA
			DM86		39	50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

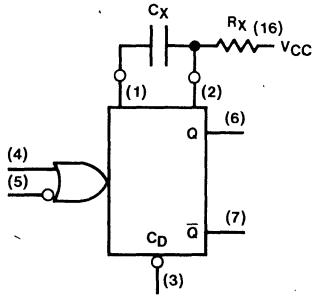
Note 3: Unless otherwise noted, R_X = 10k for all tests.

Note 4: Ground PIN 1(15) for V_{OL} on PIN 7(9) or V_{OH} and I_{OS} on PIN 6(10) and apply momentary ground to PIN 4(12). Open PIN 1(15) for V_{OL} on PIN 6(10) or V_{OH} and I_{OS} on PIN 7(9).

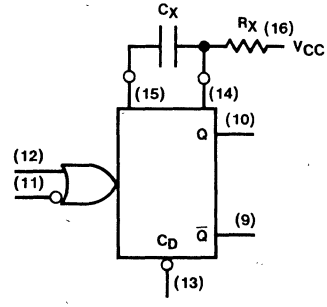
Switching Characteristics V_{CC} = 5 V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		Conditions	DM96 02			DM86 02			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Negative Trigger Input to True Output	C_L = 15 pF, C_X = 0, R_X = 5 kΩ		25	35		25	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Negative Trigger Input To Complement Output			29	43		29	48	ns
t_{PW} (MIN)	Minimum True Output Pulse Width				72	90		72	100	ns
	Minimum Complement Pulse Width				78	100		78	110	
t_{PW}	Pulse Width		R_X = 10 kΩ, C_X = 1000 pF	3.08	3.42	3.76	3.08	3.42	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pins 2, 14 to GND			50			50	pF
R_X	External Timing Resistor			5		25	5		50	kΩ

Logic Diagrams



TL/F/6611-2



TL/F/6611-3

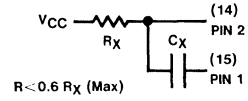
Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
3. The output pulse with (t) is defined as follows:

$$t = K\, R_X C_X \left[1 + \frac{1}{R_X}\right] \quad \text{for } C_X > 10^3 \text{ pF}, \; K \approx 0.34$$

where R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see *Figure 1.*
for K vs C_X see *Figure 6.*

4. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 3 μA, and the inverse capacitor leakage at 1.0 V is less than 5 μA over the operational temperature range.

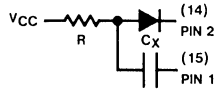


TL/F/6611-4

Operating Rules (Continued)

B. Use with high inverse leakage current electrolytic capacitors:
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\ RC_X$$



TL/F /6611-5

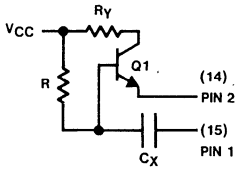
C. Use to obtain extended pulse widths:
This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

$R < R_X$ (0.7) (h_{FE} Q1) or $< 2.5\ M\Omega$, whichever is the lesser

R_X (min) $< R_Y < R_X$ (max)
(5 kΩ ≤ R_Y ≤ 10 kΩ is recommended)

Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

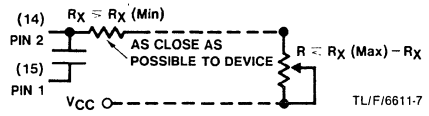
$$t \approx 0.3\ RC_X$$



TL/F/6611-6

This configuration is not recommended with retriggerable operation.

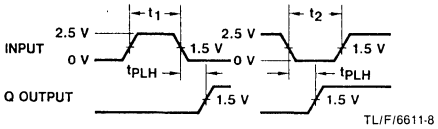
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6611-7

6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

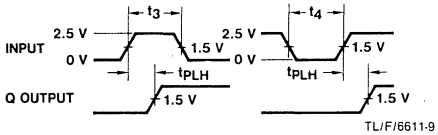
7. Input Trigger Pulse Rules (See Triggering Truth Table)



TL/F/6611-8

Input to Pin 5 (11), (Pin 3 (13) = HIGH)
Pin 4 (12) = LOW

t_1, t_3 = Min. Positive Input Pulse Width > 40 ns
t_2, t_4 = Min. Negative Input Pulse Width > 40 ns

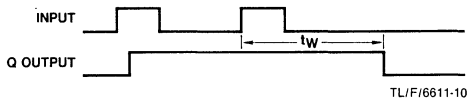


TL/F/6611-9

Input to Pin 4 (12) (Pin 3 (13) = HIGH)
Pin 5 (11) = HIGH

8. The retriggerable pulse width is calculated as shown below:

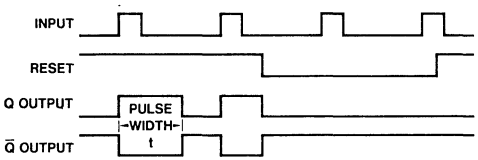
$$t_W = t + t_{PLH} = K R_X C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



TL/F/6611-10

The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X (ns) after the initial trigger pulse (i.e., during the discharge cycle).

9. Reset Operation — An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



TL/F/6611-11

10. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the DM9602/DM8602 is recommended.

*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics

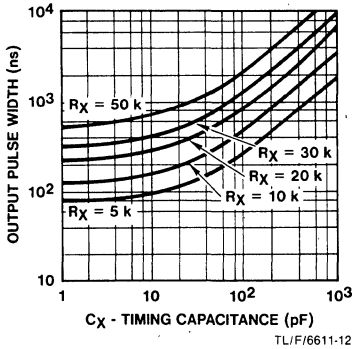


FIGURE 1. Output Pulse Width vs Timing Resistance and Capacitance For $C_X < 10^3$ pF

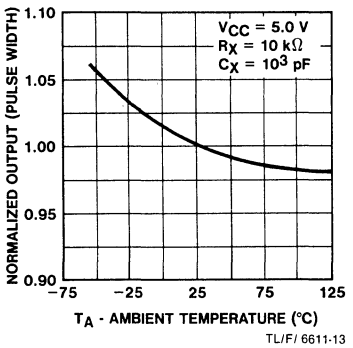


FIGURE 2. Normalized Output Pulse Width vs Ambient Temperature

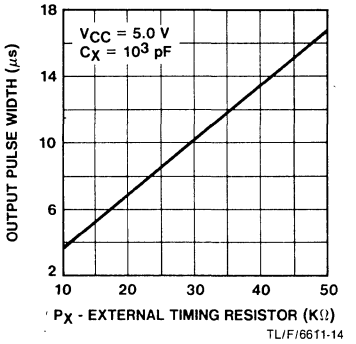


FIGURE 3. Pulse Width vs Timing Resistor

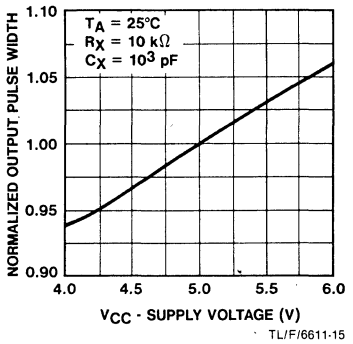


FIGURE 4. Normalized Output Pulse Width vs Supply Voltage

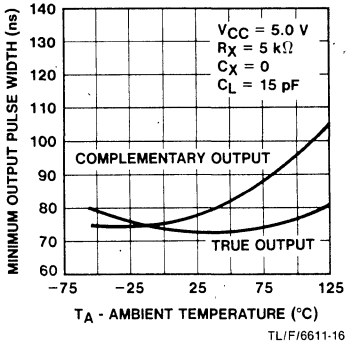


FIGURE 5. Minimum Output Pulse Width vs Ambient Temperature

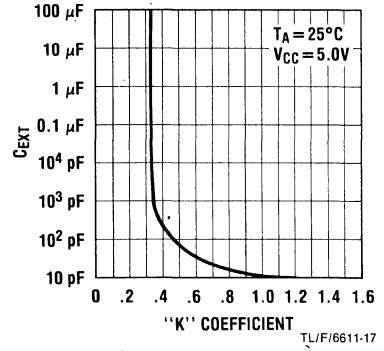


FIGURE 6. Typical "K" Coefficient Variation vs Timing Capacitance

Section 7

Low Power

7

Section Contents

National Semiconductor

DM54L00/DM74L00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

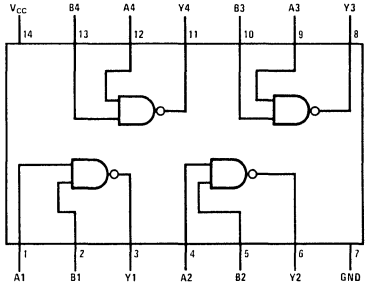
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6654-1

DM54L00 (J) DM74L00 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

7

Recommended Operating Conditions

Symbol	Parameter	DM54L00			DM74L00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.44	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.16	2.04	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			31	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L01/DM74L01 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

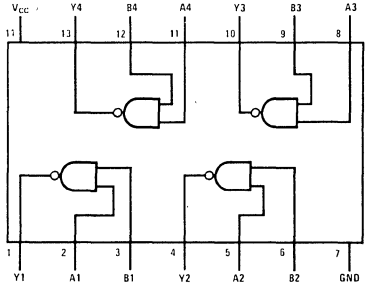
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Output Voltage	8V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6655-1

DM54L01 (J) DM74S01 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L01			DM74L01			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.6			0.6	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.44	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.16	2.04	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			60	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			33	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54L02/DM74L02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

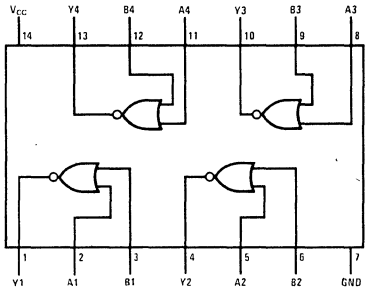
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6656-1

DM54L02 (J) DM74L02 (N)

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L02			DM74L02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.4	2.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			31	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			35	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L03/DM74L03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

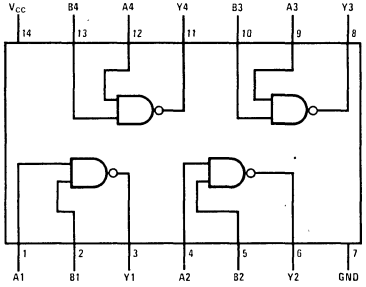
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Output Voltage	8V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6615-1

DM54L03 (J) DM74L03 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L03			DM74L03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.6			0.6	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.44	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.2	2.04	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			60	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			33	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54L04/DM74L04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

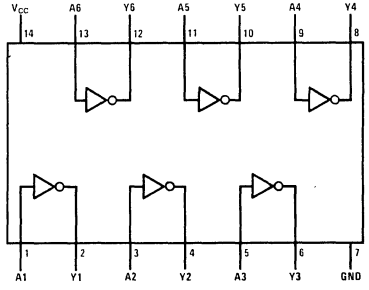
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6616-1

DM54L04 (J) DM74L04 (N)

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L04			DM74L04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.6	1.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.7	3.06	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			31	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time

National Semiconductor

DM54L05/DM74L05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

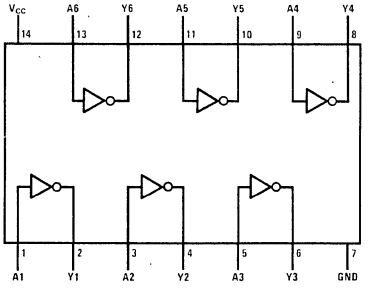
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Output Voltage	8V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6617-1

DM54L05 (J) DM74L05 (N)

Function Table

$$Y = \bar{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L05			DM74L05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.6			0.6	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.66	1.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.74	3.06	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			60	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			33	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54L08/DM74L08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

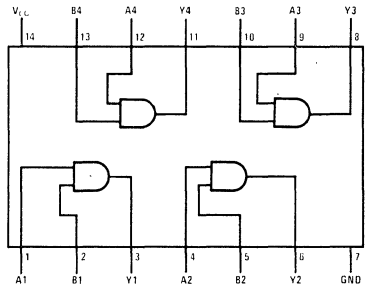
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6618-1

DM54S08 (J) DM74S08 (N)

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

7

Recommended Operating Conditions

Symbol	Parameter	DM54L08			DM74L08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.1	2.1	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			2.0	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ, C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			45	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			45	90	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L10/DM74L10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

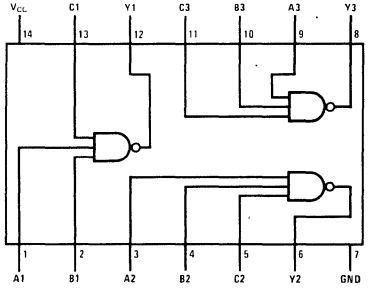
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6619-1

DM54L10 (J), DM74L10 (N)

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

7

Recommended Operating Conditions

Symbol	Parameter	DM54L10			DM74L10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.33	0.6	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.87	1.53	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			31	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L11/DM74L11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

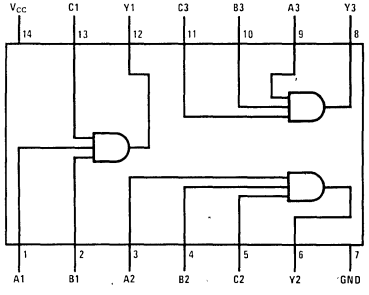
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6620-1

DM54L11 (J) DM74L11 (N)

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L11			DM74L11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			1.0	1.5	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.6	2.2	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ, C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			40	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output			45	90	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L20/DM74L20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

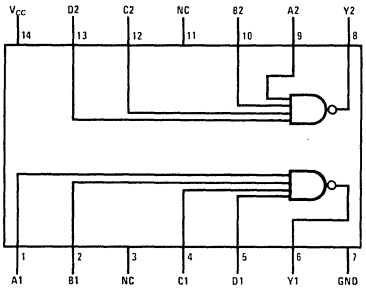
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6621-1

DM54L20 (J) DM74L20 (N)

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L20			DM74L20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.22	0.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.58	1.02	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			31	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L26/DM74L26 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

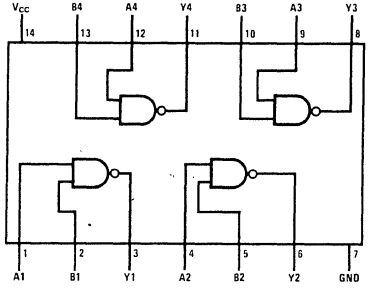
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6622-1

DM54L26 (J) DM74S26 (N)

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

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Recommended Operating Conditions

Symbol	Parameter	DM54L26			DM74L26			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 12V V_{IL} = Max				200	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.48	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			1.32	2.04	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 15 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			40	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			25	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM54L30/DM74L30 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

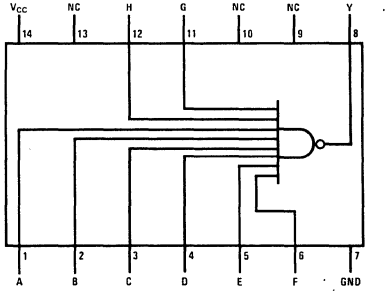
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6623-1

DM54L30 (J) DM74L30 (N)

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM54L30			DM74L30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.11	0.2	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.29	0.51	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ, C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			70	100	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM54L42A/DM74L42A BCD/Decimal Decoders

General Description

These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10-15) input conditions.

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 15 mW
- Typical propagation delay 53 ns

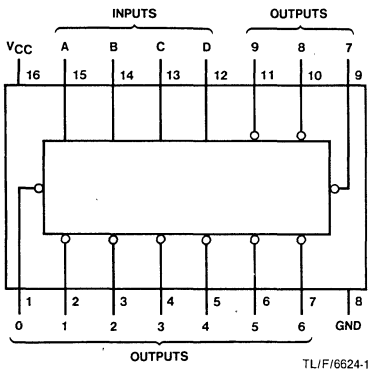
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

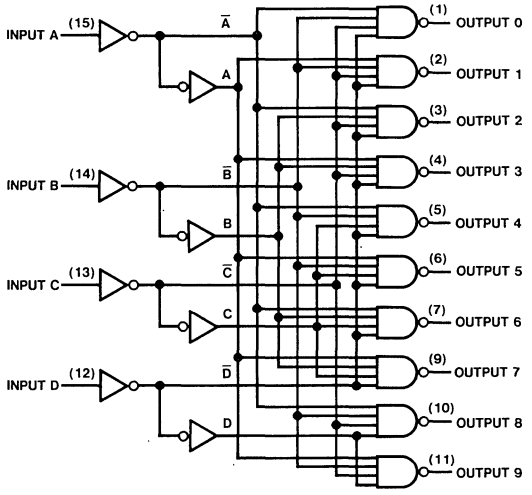
Dual-In-Line Package



TL/F/6624-1

54L42A (J) 74L42A (N)

Logic Diagram



TL/F/6624-2

Function Table

No.	L42A BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

Recommended Operating Conditions

Sym	Parameter	DM54L42A			DM74L42A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			3.0	5.3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C or D through 2 Levels of Logic		65	130	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C or D through 3 Levels of Logic		70	140	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C or D through 2 Levels of Logic		30	60	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C or D through 3 Levels of Logic		35	70	ns

National Semiconductor

DM54L51/DM74L51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

General Description

This device contains two combinations of gates each of which performs the logic AND-OR-INVERT function.

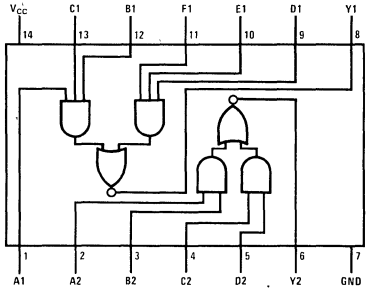
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6625-1

DM54L51 (J) DM74L51 (N)

Function Table

$$Y1 = \overline{[(A1)(B1)(C1)] + [(CD1)(E1)(F1)]}$$

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Other Combinations						H

$$Y2 = \overline{[(A2)(B2)] + [(C2)(D2)]}$$

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54L51			DM74L51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.44	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.76	1.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			50	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			35	60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

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National Semiconductor

DM54L54/DM74L54 4-Wide AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

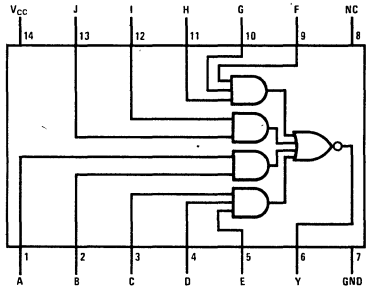
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6626-1

DM54L54 (J) DM74L54 (N)

Function Table

$$Y = \overline{AB + CDE + FGH + IJ}$$

Inputs										Output
A	B	C	D	E	F	G	H	I	J	Y
H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	X	X	L
X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	H	H	L
All other combinations										H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54L54			DM74L54			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.39	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.6	0.99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			50	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			35	60	ns

National Semiconductor

DM54L55/DM74L55 2-Wide, 4 Input AND-OR-INVERT Gates

General Description

This device contains a combination of gates which perform the logic AND-OR-INVERT function.

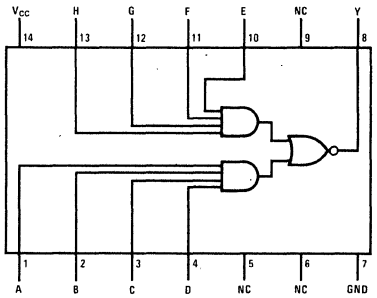
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6627-1

DM54L55 (J) DM74L55 (N)

Function Table

$$Y = \overline{ABCD} + \overline{EFGH}$$

Inputs								Output
A	B	C	D	E	F	G	H	Y
H	H	H	H	X	X	X	X	L
X	X	X	X	H	H	H	H	L
All other combinations								H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Sym	Parameter	DM54L55			DM74L55			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			0.22	0.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			0.38	0.65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output			50	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output			35	60	ns

National Semiconductor

DM54L71/DM74L71 AND-Gated Master-Slave R-S Flip-Flop with Preset, Clear and Complementary Outputs

General Description

This device contains a positive pulse triggered master-slave R-S flip-flop with complementary outputs. Multiple R and S inputs are ANDed together to produce the internal R and S functions for the flip-flop. The R and S data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive-going transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data is transferred from the master to the slave. The R and S inputs must be held constant while the clock is high. Data is transferred to the output on the falling edge of the clock pulse. A low level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

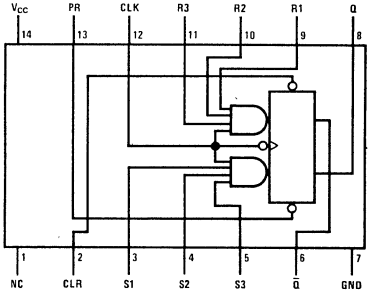
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6628-1

DM54L71 (J) DM74L71 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	S(1)	R(1)	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\bar{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Indeterminate	

Note 1: S = (S1)(S2)(S3), R = (R1)(R2)(R3)

H = High Logic Level

X = Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse. The R and S inputs must be held constant while the clock is high. Data is transferred to the output on the falling edge of the clock pulse.

Q_O = The level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs returned to their inactive (high) level.

Recommended Operating Conditions

Sym	Parameter		DM54L71			DM74L71			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock High	100			100			ns
		Clock Low	100			100			
		Preset Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	R, S			100	mA
			Clear			200	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	R, S			10	μA
			Clear			20	
			Preset			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	R, S			−0.18	mA
			Clear			−0.36	
			Preset			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			0.76	1.44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	11		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	60	150	ns

National Semiconductor

DM54L72/DM74L72 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear and Complementary Outputs

General Description

This device contains a positive pulse triggered master-slave J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the J and K inputs must not be allowed to change while the clock is in the high state. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

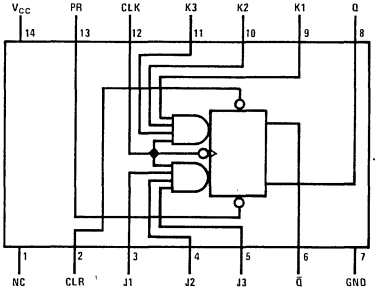
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6629-1

DM54L72 (J) DM74L72 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\bar{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

Note 1: J = (J1)(J2)(J3), K = (K1)(K2)(K3)

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_O = The output logic level before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

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Recommended Operating Conditions

Sym	Parameter		DM54L72			DM74L72			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock High	100			100			ns
		Clock Low	100			100			
		Preset Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	mA
			Clear			200	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			20	
			Preset			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	J, K			−0.18	mA
			Clear			−0.36	
			Preset			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			0.76	1.44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	11		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	60	150	ns

National Semiconductor

DM54L73/DM74L73 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high, the data from the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

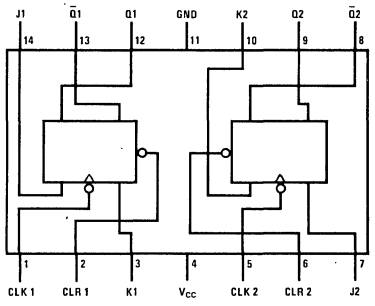
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6630-1

DM54L73 (J) DM74L73 (N)

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

Recommended Operating Conditions

Sym	Parameter		DM54L73			DM74L73			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock High	100			100			ns
		Clock Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

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Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	mA
			Clear			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−0.18	mA
			Clear			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.5	2.88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	11		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		35	75	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	35	75	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	60	150	ns

National Semiconductor

DM54L74/DM74L74 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

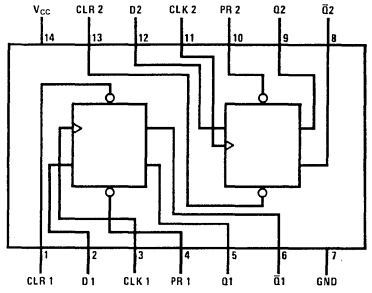
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6631-1

DM54L74 (J) DM74L74 (N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition.

Q_0 = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs returned to their inactive (high) level.

7

Recommended Operating Conditions

Sym	Parameter		DM54L74			DM74L74			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock High	75			75			ns
		Clock Low	75			75			
		Preset Low	75			75			
		Clear Low	75			75			
t_{SU}	Input Setup Time (Note 1)		50↑			50↑			ns
t_H	Input Hold Time (Note 1)		15↑			15↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	D			100	mA
			Clear			300	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			10	μA
			Clear			30	
			Preset			20	
			Clock			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	D			−0.18	mA
			Clear			−0.36	
			Preset			−0.18	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.6	3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	11		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		60	120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		40	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		60	120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	50	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	60	120	ns

National Semiconductor

DM54L75A/DM74L75A Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

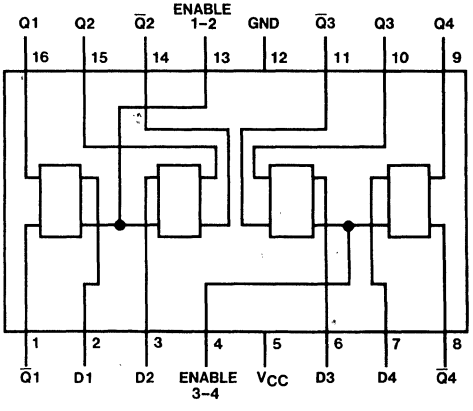
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



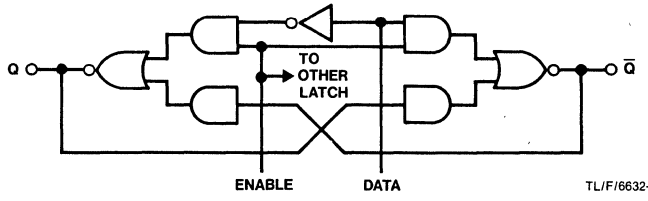
54L75A (J) 74L75A (N) TL/F/6632-1

Function Table (Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care
Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)



TL/F/6632-2

Recommended Operating Conditions

Sym	Parameter	DM54L75A			DM74L75A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
t_W	Enable Pulse Width	100			100			ns
t_{SU}	Setup Time	100			100			ns
t_H	Hold Time	25			25			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	D Input			0.2	mA
			G Input			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D Input			20	μA
			G Input			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	D Input			−0.36	mA
			G Input			−0.72	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			3.5	5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	D to Q		55	100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to Q		50	100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		75	120	ns
t_{PHL} Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		32	80	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to Q		50	100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to Q		32	80	ns
t_{PLH} Propagation Delay Time Low to High Level Output	G to $\overline{Q}$		48	100	ns
t_{PHL} Propagation Delay Time High to Low Level Output	G to $\overline{Q}$		38	80	ns

National Semiconductor

DM54L78/DM74L78 Dual Master-Slave J-K Flip-Flops with Preset, Common Clear, Common Clock, and Complementary Outputs

General Description

This device contains two master-slave J-K flip-flops with complementary outputs. The J-K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive going transition of the clock the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative going transition of the clock the data from the master is transferred to the slave. The data on the J and K inputs must not be allowed to change while the clock is high. The data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

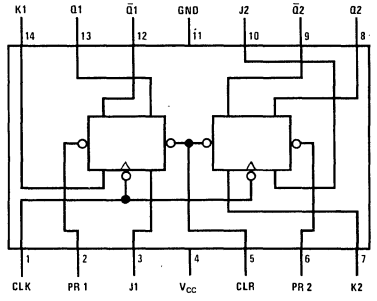
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6633-1

DM54L78 (J) **DM74L78 (N)**

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_O	$\bar{Q}_O$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse. J-K inputs must be held constant while the clock is high. Data is transferred to the output on the falling edge of the clock.

* = This configuration is nonstable; that is, it will not persist when the clear and/or preset inputs return to their inactive (high) level.

Q_O = The level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

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Recommended Operating Conditions

Sym	Parameter		DM54L78			DM74L78			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock High	100			100			ns
		Clock Low	100			100			
		Preset Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Note 1)		0↑			0↑			ns
t_H	Input Hold Time (Note 1)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	mA
			Clear			400	
			Preset			200	
			Clock			400	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			40	
			Preset			20	
			Clock			−400	

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.18	mA
			Clear			−0.72	
			Preset			−0.36	
			Clock			−0.72	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.5	2.88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	11		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		60	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	35	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	60	150	ns

National Semiconductor

DM54L85/DM74L85 4-Bit Magnitude Comparators

General Description

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and low-level voltages applied to the A > B and A < B inputs.

Features

- Typical power dissipation 20 mW
- Typical delay (4-bit words) 55 ns

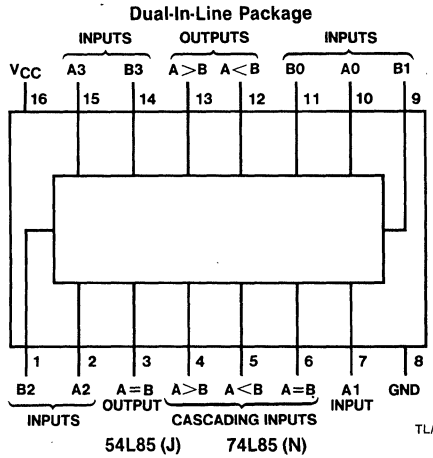
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6634-1

54L85 (J) 74L85 (N)

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = High Level, L = Low Level, X = Don't Care (Either Low or High Logic Level)

Recommended Operating Conditions

Sym	Parameter	DM54L85			DM74L85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	A < B			0.1	mA
			A > B			0.1	
			A = B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A < B			10	μA
			A > B			10	
			A = B			10	
			Others			30	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	A < B			−0.18	mA
			A > B			−0.18	
			A = B			−0.18	
			Others			−0.54	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)				6.6	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)				7.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

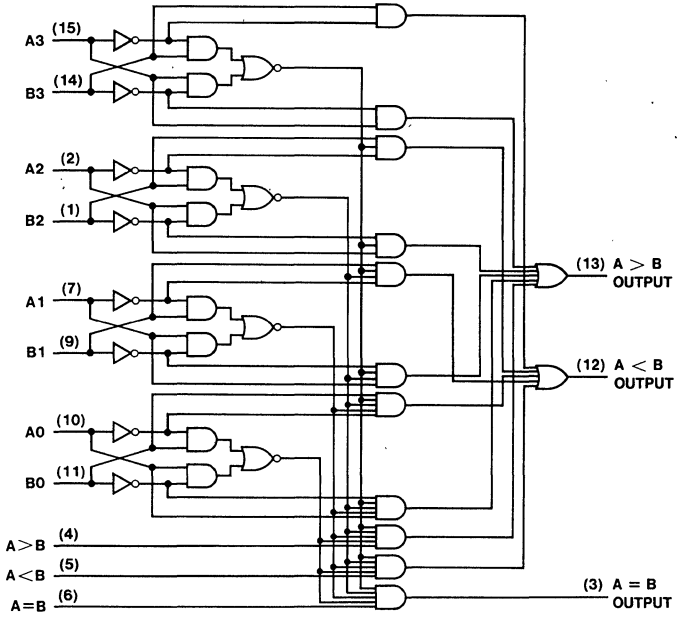
Note 3: I_{CC1} is measured with all outputs open and all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From Input	To Output	Number of Gate Levels	$R_L = 4\ k\Omega$, $C_L = 50\ pF$ Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A<B, A>B	1		70	115	ns
			2		70	115	
			3		70	115	
		A=B	4		70	115	
t_{PHL} Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A<B, A>B	1		55	90	ns
			2		55	90	
			3		55	90	
		A=B	4		55	90	
t_{PLH} Propagation Delay Time Low-to-High Level Output	A<B or A=B	A>B	1		55	100	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A<B or A=B	A>B	1		40	65	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A=B	A=B	2		55	100	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A=B	A=B	2		40	65	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A>B or A=B	A<B	1		55	100	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A>B or A=B	A<B	1		40	65	ns

Logic Diagram



TL/F/6634-2

National Semiconductor

DM54L86/DM74L86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic Exclusive-OR function.

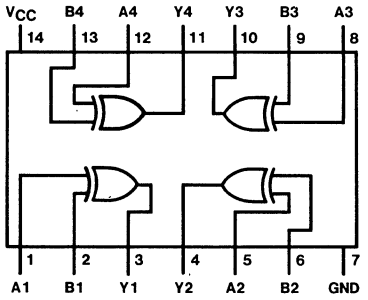
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6635-1

DM74L86 (N) **DM54L86 (J)**

Function Table

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

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Recommended Operating Conditions

Sym	Parameter	DM54L86			DM74L86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max (Note 3)			2.2	4.4	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max (Note 4)			3.8	6.68	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs at ground.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 4k\Omega$, $C_L = 50$ pF			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input Low		37	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			21	60	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Other Input High		25	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output			35	60	ns

National Semiconductor

DM54L90/DM74L90, DM54L93/DM74L93 Decade, Divide-by-12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the L90 and divide-by-eight for the L93.

All of these counters have a gated zero reset and the L90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the L90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- Typical power dissipation
  - L90 20 mW
  - L93 16 mW
- Count frequency
  - L90 11 MHz
  - L93 15 MHz

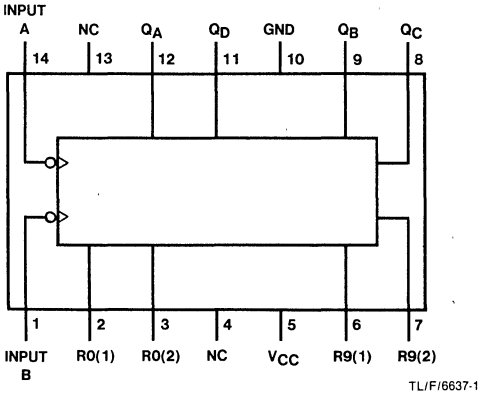
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

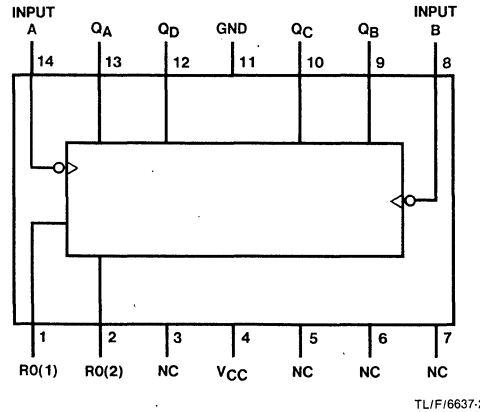
Dual-In-Line Package



TL/F/6637-1

54L90 (J) 74L90 (N)

Dual-In-Line Package



TL/F/6637-2

54L93 (J) 74L93 (N)

Function Tables

L90
BCD COUNT SEQUENCE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

L90
BI-QUINARY (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

L93
COUNT SEQUENCE
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

L90
RESET/COUNT TRUTH TABLE

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

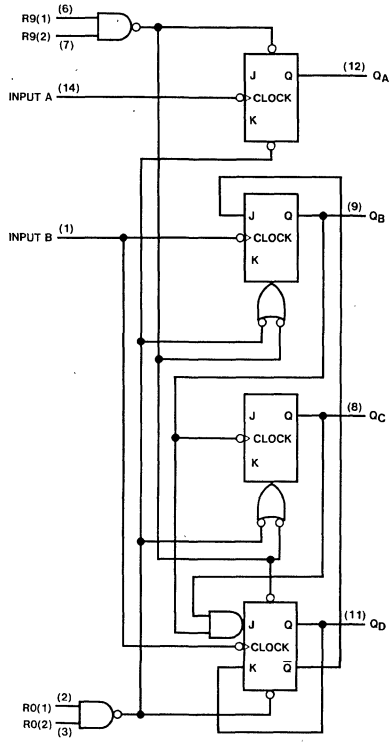
L93
RESET/COUNT TRUTH TABLE

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.
Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

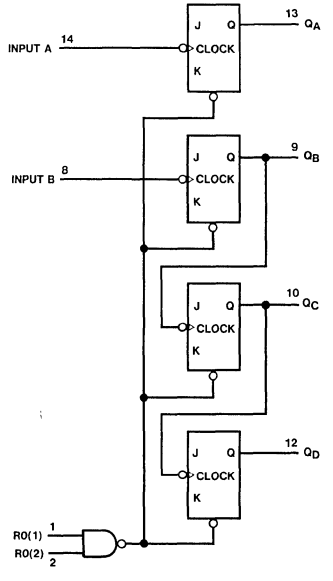
Logic Diagrams

L90



TL/F/6637-3

L93



TL/F/6637-4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

Recommended Operating Conditions

Sym	Parameter		DM54L90			DM74L90			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	A	90			90			ns
		B	90			90			
		Reset	200			200			
t_{REL}	Reset Release Time		200			200			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'L90 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min (Note 4)	DM54		0.15	0.3	V
			DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	Reset			0.1	mA
			A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			10	μA
			A			20	
			B			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Reset			−0.18	mA
			A			−0.36	
			B			−0.72	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				5.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'L90 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	6	11		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		175	300	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		190	300	ns

Recommended Operating Conditions

Sym	Parameter		DM54L93			DM74L93			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	A	90			90			ns
		B	90			90			
		Reset	200			200			
t_{REL}	Reset Release Time		200			200			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'L93 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min (Note 4)	DM54		0.15	0.3	V
			DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			10	μA
			A			20	
			B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Reset			−0.18	mA
			A			−0.36	
			B			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				5.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'L93 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	A to Q_A	6	15		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	A to Q_D		210	400	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A to Q_D		230	400	ns

National Semiconductor

DM54L95/DM74L95 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 14 MHz
- Typical power dissipation 24 mW

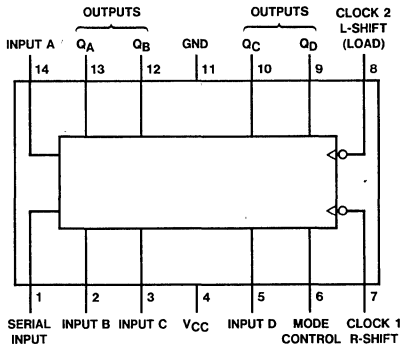
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



54L95 (J) 74L95 (N)

TL/F/6638-1

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

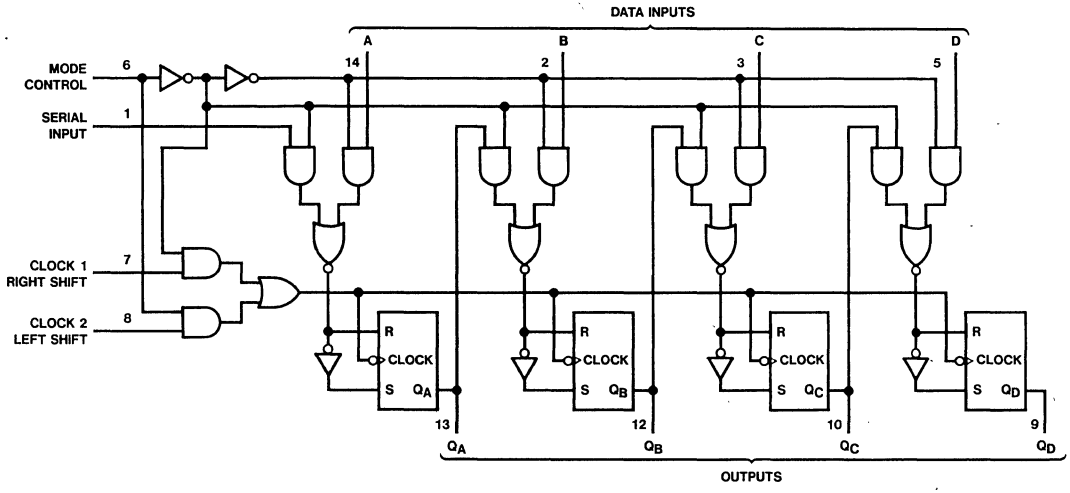
↓ = *Transition from high to low level*, ↑ = *Transition from low to high level*

a, b, c, d, = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Logic Diagram



TL/F/6638-2

Recommended Operating Conditions

Sym	Parameter		DM54L95			DM74L95			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
$t_{W(CLK)}$	Pulse Width of Clock		90			90			ns
t_{SU}	Data Setup Time		50			50			ns
t_{EN}	Time to Enable Clock	Clock 1	120			120			ns
		Clock 2	100			100			ns
t_H	Data Hold Time		0			0			ns
t_{IN}	Time to Inhibit Clock 1 or Clock 2		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

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Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.13	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	Mode			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Mode			−0.36	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4.8	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	14		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		42	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		48	90	ns

National Semiconductor

DM54L98/DM74L98 4-Bit Storage Registers

General Description

These data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high level input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical clock frequency is 12 MHz.

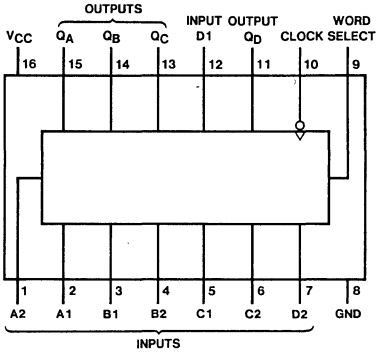
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package

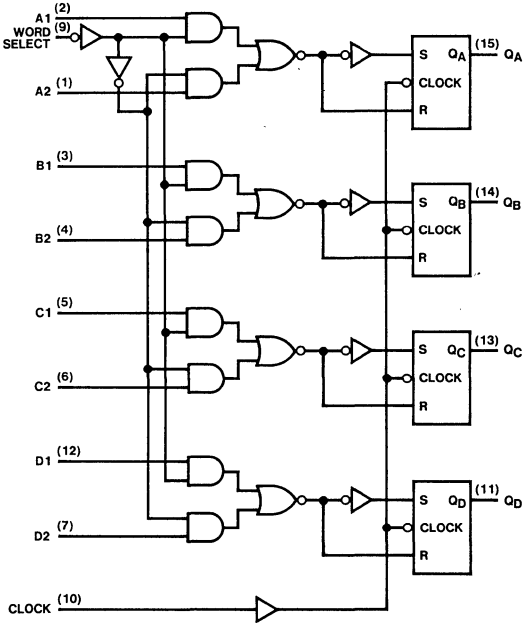


TL/F/6639-1

54L98 (J) 74L98 (N)

Word select low for word 1, word select high for word 2, see description

Logic Diagram



TL/F/6639-2

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Recommended Operating Conditions

Sym	Parameter		DM54L98			DM74L98			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Clock Pulse Width		100	65		100	65		ns
t_{SU}	Setup Time	Data High	100			100			ns
		Data Low	120			120			
		Select High	150			150			
		Select Low	100			100			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			6	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	12		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		40	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		65	100	ns

National Semiconductor

DM54L157A/DM74L157A Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

Features

- Buffered inputs and outputs
- Three speed/power ranges available
- Typical propagation time 40 ns
- Typical power dissipation 15 mW

Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

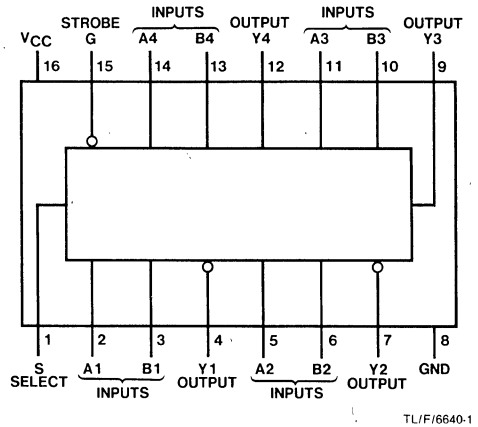
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6640-1

Low level at S selects A inputs
High level at S selects B inputs

DM54L157A (J) **DM74L157A (N)**

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Sym	Parameter	DM54L157A			DM74L157A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			3	4	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

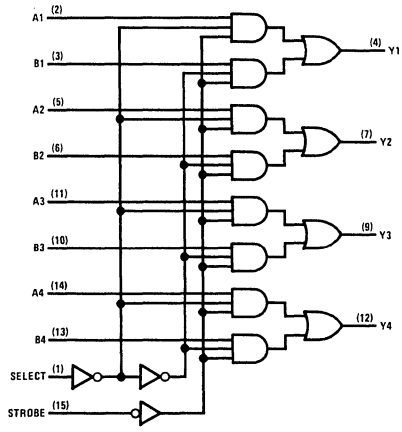
Note 2: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	Min	$R_L = 4\ k\Omega$ $C_L = 50\ pF$ Typ	Max	Units
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y		40	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y		40	80	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Y		60	120	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Y		60	120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Y		70	140	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Y		50	100	ns

Logic Diagram



National Semiconductor

DM54L164A/DM74L164A 8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 14 MHz
- Typical power dissipation 30 mW

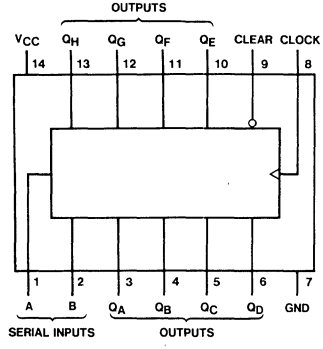
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6641-1

54L164A (J) **74L164A (N)**

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

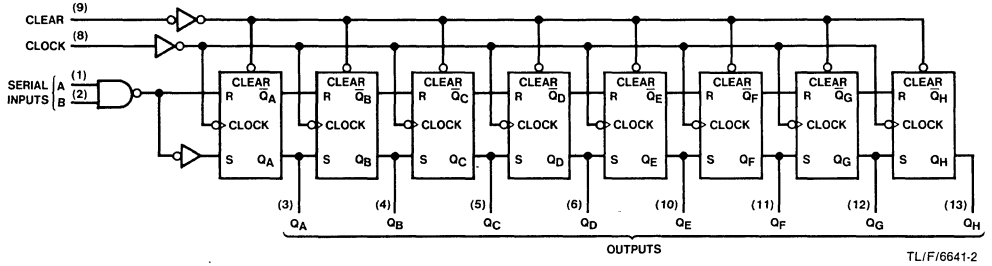
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



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Recommended Operating Conditions

Sym	Parameter		DM54L164A			DM74L164A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock	60	40		60	40		ns
		Clear	60	40		60	40		
t_{SU}	Data Setup Time		40	20		40	20		ns
t_H	Data Hold Time		20	−5		20	−5		ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	Clear			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Clear			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Clear			−0.36	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6	9	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

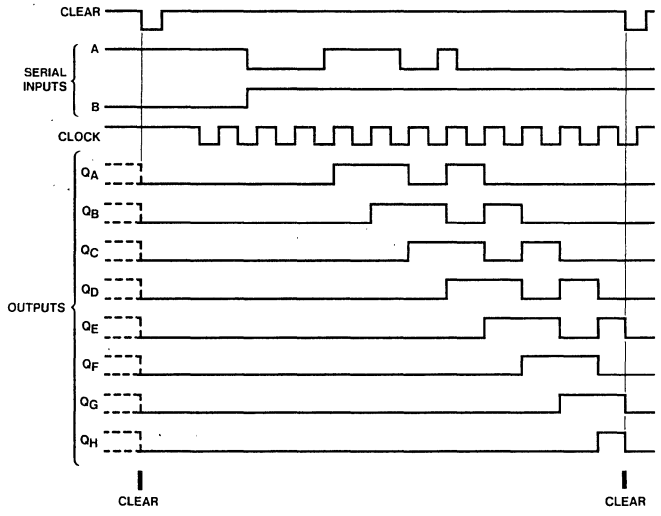
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	14		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		50	85	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		90	135	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		75	120	ns

Timing Diagram



TL/F/6641-3

7

National Semiconductor

DM54L165A/DM74L165A 8-Bit Parallel In/Serial Out Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical clock frequency 14 MHz
- Typical power dissipation 30 mW

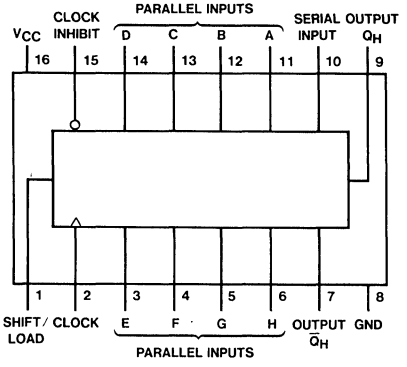
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6642-1

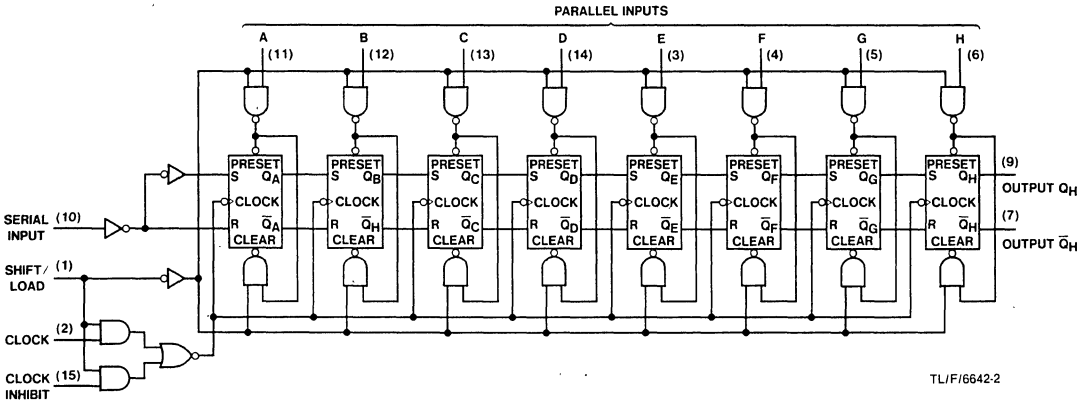
54L165A (J) **74L165A (N)**

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low-to-high level
a...h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

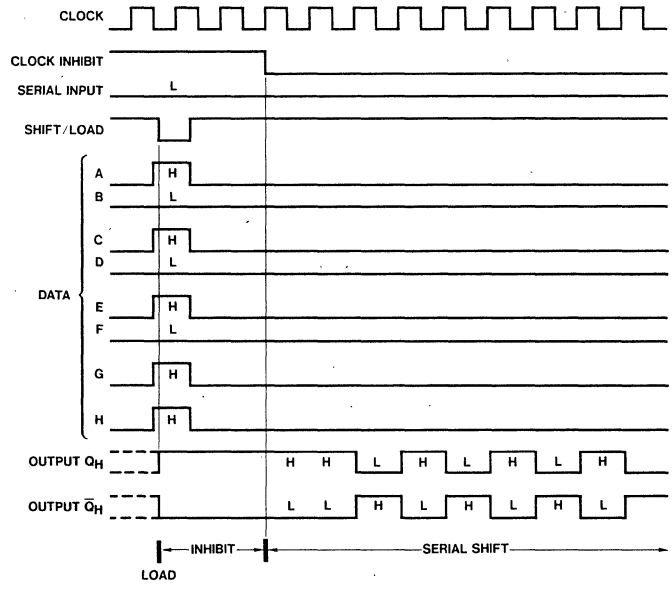
Logic Diagram



TL/F/6642-2

Timing Diagram

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES



TL/F/6642-3

Recommended Operating Conditions

Sym	Parameter		DM54L165A			DM74L165A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock	100			100			ns
		Clear	100			100			
t_{SU}	Setup Time		44			44			ns
t_H	Hold Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Shift/Load			30	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Shift/Load			−0.54	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				9.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, CLOCK INHIBIT and SHIFT/LOAD at 4.5V, and a clock pulse applied to the CLOCK, I_{CC} is measured first with the parallel inputs at 4.5V, then a second time grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	14		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		44	88	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		62	124	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		35	70	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		50	100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to Q_H		33	66	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to Q_H		56	112	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to Q_H		33	66	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to Q_H		56	112	ns

National Semiconductor

DM54L192/DM74L192, DM54L193/DM74L193 Synchronous Up/Down Counters with Dual Clock

General Description

These circuits are synchronous up/down counters; the L192 circuits are BCD counters and the L193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop
- Typical count frequency 12 MHz
- Typical power dissipation 40 mW

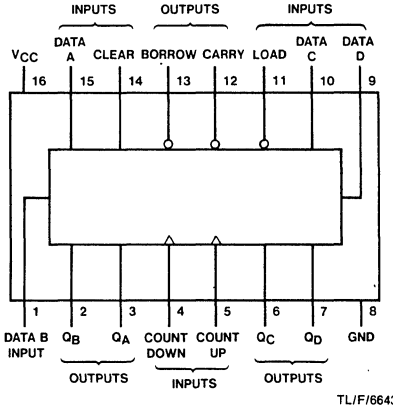
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6643-1

Note: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D.

DM54L192, L193 (J) DM74L192, L193 (N)

Recommended Operating Conditions

Sym	Parameter	DM54L192, L193			DM74L192, L193			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency	0		6	0		6	MHz
t_W	Pulse Width of Any Input	70			70			ns
t_{SU}	Data Setup Time	30			30			ns
t_H	Data Hold Time	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'L192 and 'L193 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				5.5	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

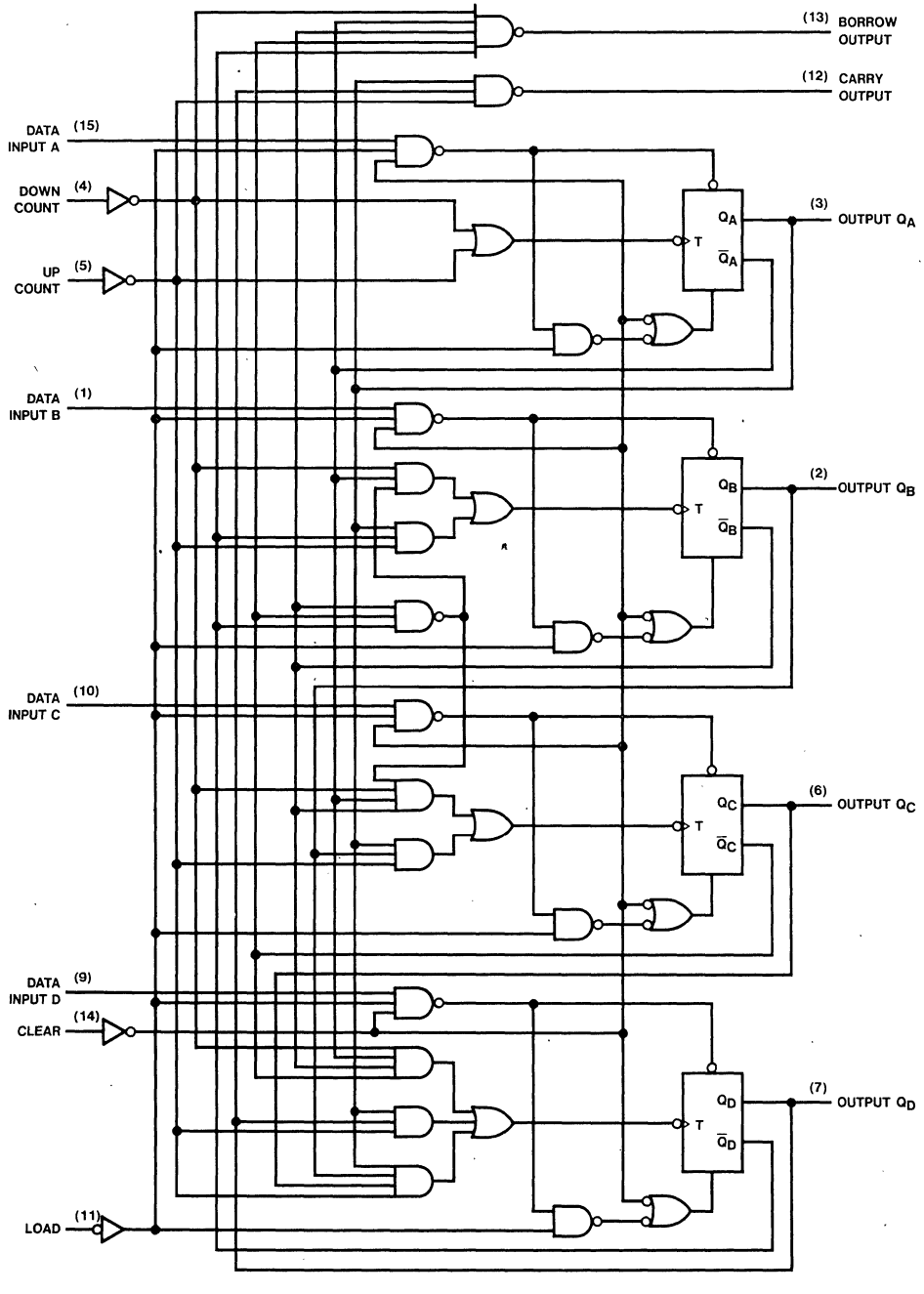
'L192 and 'L193 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	8		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		30	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		60	120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		30	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		50	100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Either Count to Any Q		45	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Either Count to Any Q		75	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		55	110	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		105	200	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		95	190	ns

Logic Diagrams

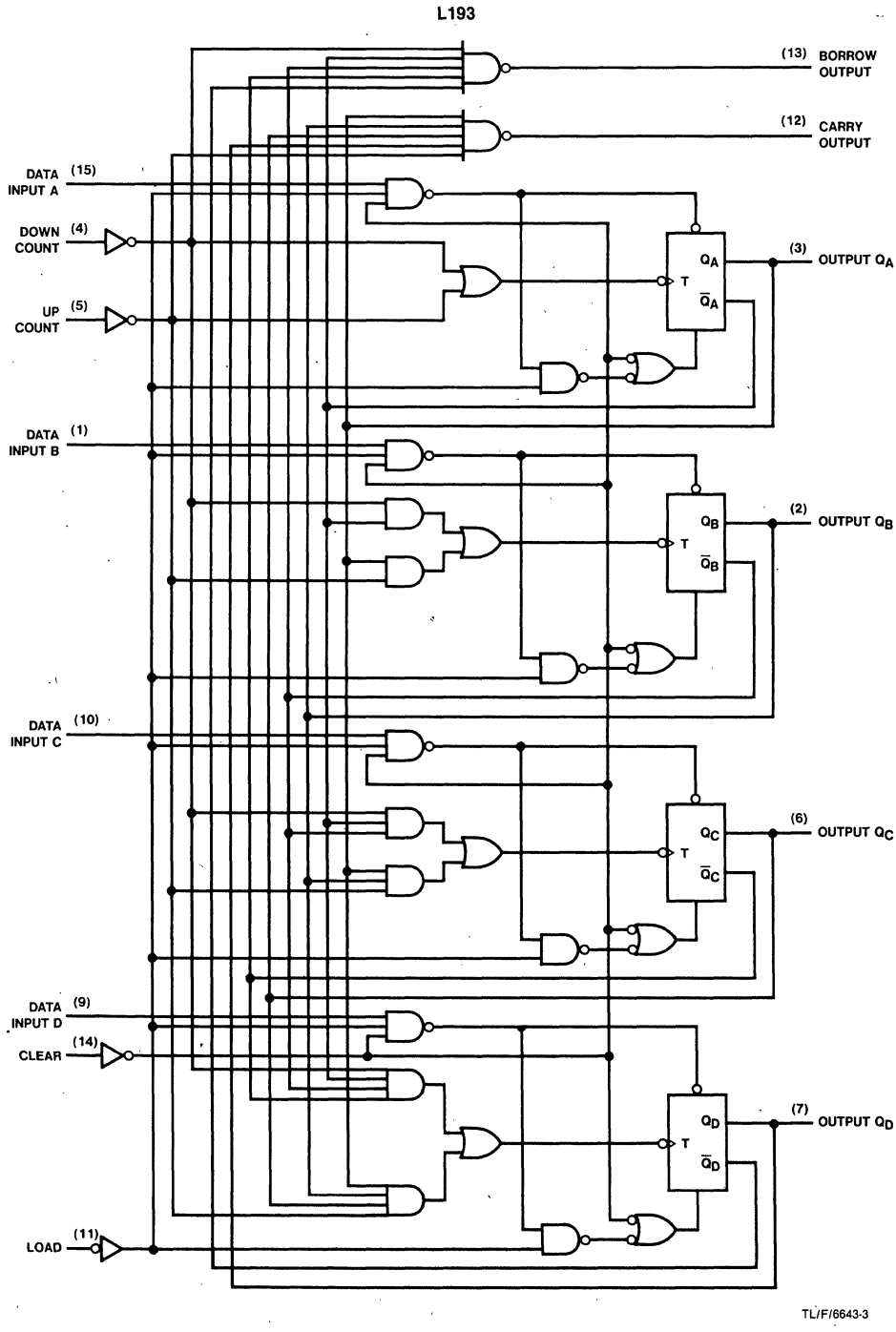
L192



TL/F/6643-2

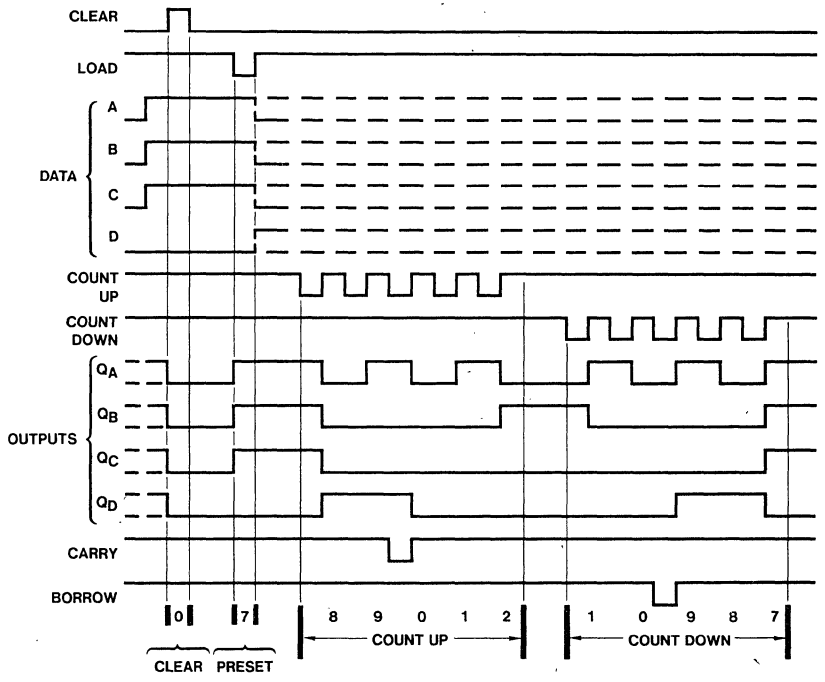
7

Logic Diagrams (Continued)



Timing Diagrams

L192 Decade Counters
Typical Clear, Load and Count Sequences



TL/F/6643-4

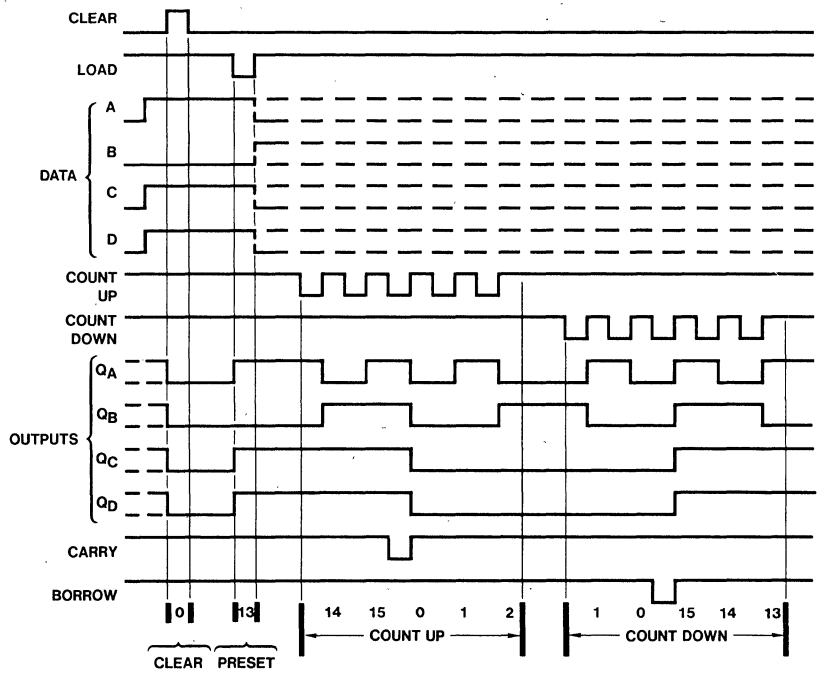
Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

7

Timing Diagrams (Continued)

L193 Binary Counters
Typical Clear, Load and Count Sequences



TL/F/6643-5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

DM80L06 Quad 2-Input NAND Gates with Resistive Pull Up

General Description

These quad two-input NAND gates feature internally connected, 20 kΩ pull-up resistors on the outputs. The pinout is the same as the very popular DM54L03/DM74L03, and these devices provide the same "one-tenth-power technology" as well.

Features

- Typical power dissipation 12 mW
- Typical propagation delay 115 ns

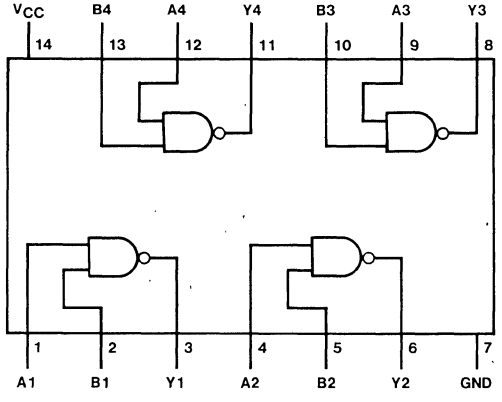
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6644-1

DM80L06 (N)

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

7

Recommended Operating Conditions

Sym	Parameter	DM80L06			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.2	mA
I_{OL}	Low Level Output Current			3.6	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max	2	2.5		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min			0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V		−0.12	−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−0.17	−0.25	−0.33	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max		0.48	0.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max		2.4	3.68	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	R_L = 4 kΩ C_L = 15 pF			Units
	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output		193	290	ns
t_{PHL} Propagation Delay Time High to Low Level Output		37	56	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM70L98/DM80L98 TRI-STATE® Hex Buffers

General Description

These devices provide six, two-input buffers in each package. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. On this device, four buffers are enabled from a common line, and the other two buffers from a separate common line. The outputs are placed in the TRI-STATE condition by applying a high logic level to the control pins. With the low power versions of these circuits, it is possible to connect over 100 like devices to a common bus line and still have adequate drive capability.

Features

- Typical power dissipation 15 mW
- Typical propagation delay 31 ns
- Pin equivalent to DM54368 (98)

Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

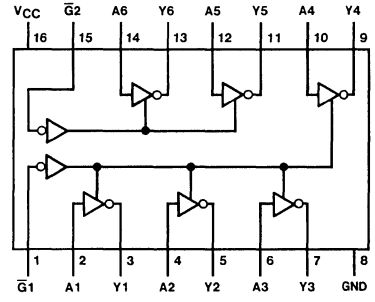
Function Table (Each Driver)

Inputs		Output
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

L = Low Logic Level
H = High Logic Level
Hi-Z = High Impedance (Off) State

Connection Diagram

Dual-In-Line Package



TL/F/6645-1

DM70L98 (J) **DM80L98 (N)**

Recommended Operating Conditions

Sym	Parameter	DM70L98			DM80L98			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM70			0.3	V
			DM80			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	A (Note 3)			−10	mA
			A (Note 4)			−0.18	
			$\overline{G}$			−0.18	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4 V_{IH} = Min, V_{IL} = Max				10	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.3 V_{IH} = Min, V_{IL} = Max				−10	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM70	−3		−15	mA
			DM80	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max			3	4.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Both $\overline{G}$ inputs at 2V.

Note 4: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 4\ k\Omega$						Units
	$C_L = 5$ pF			$C_L = 50$ pF			
	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output					26	48	ns
t_{PHL} Propagation Delay Time High to Low Level Output					35	53	ns
t_{PZH} Output Enable Time to High Level Output					42	90	ns
t_{PZL} Output Enable Time to Low Level Output					42	75	ns
t_{PHZ} Output Disable Time from High Level Output		25	43				ns
t_{PLZ} Output Disable Time from Low Level Output		34	63				ns

National Semiconductor

DM71L22/DM81L22, DM71L23/DM81L23 Quad 2-Input Data Selectors/Multiplexers

General Description

These devices contain four, two-input multiplexers with common input select logic and common output disable circuitry. The DM71L22/81L22 provides conventional totem-pole output TTL construction, whereas DM71L23/81L23 provides TRI-STATE® outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM71L22/81L22 go to the low logic state, and the outputs of the DM71L23/81L23 go to the high-impedance third state. These devices provide the designer with TRI-STATE and/or low power pin/pin replacements for the popular 9322 and 54/74157 multiplexers.

Features

- Pin equivalents popular 9322 and 54/74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Typical propagation delay 40 ns
- Typical power dissipation
  - L22 15 mW
  - L23 20 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Function Tables

L22

Strobe	Select	Inputs		Output Y
		A	B	
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	L

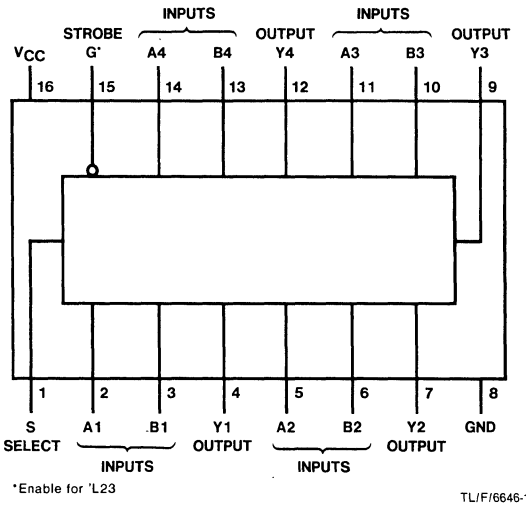
L23

Enable	Select	Inputs		Output Y
		A	B	
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Hi-Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Hi-Z = High Impedance (Off) State

Connection Diagram

Dual-In-Line Package



*Enable for 'L23

TL/F/6646-1

71L22 (J) 81L22 (N)
71L23 (J) 81L23 (N)

Recommended Operating Conditions

Sym	Parameter	DM71L22			DM81L22			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'L22 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	2.8		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM71		0.15	0.3	V
			DM81		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM71	−3		−15	mA
			DM81	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			3	4	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded, and all outputs open.

'L22 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	Conditions	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output	20	40	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output	20	40	80	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output	30	60	120	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output	30	60	120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output	35	70	140	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output	25	50	100	ns

Recommended Operating Conditions

Sym	Parameter	DM71L23			DM81L23			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'L23 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	2.8		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM71		0.15	0.3	V
			DM81		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.3V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM71	−3		−15	mA
			DM81	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	5.3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded, and all outputs open.

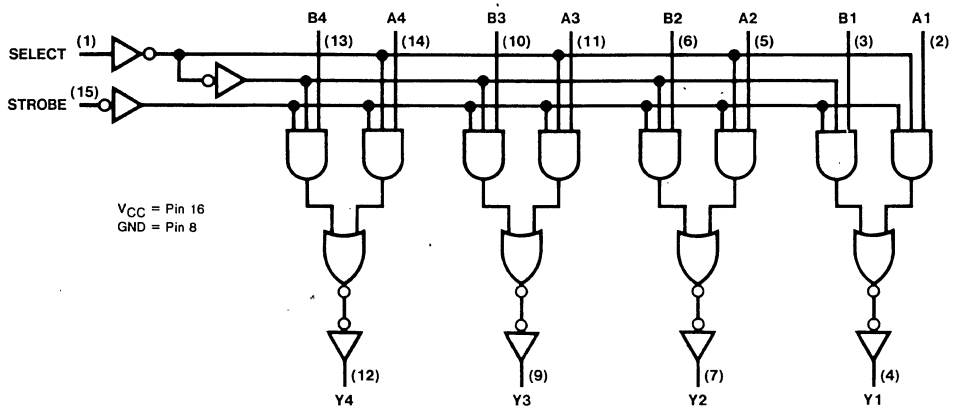
'L23 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$						Units
		$C_L = 5\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output				20	40	80	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output				20	40	80	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Select to Output				35	70	140	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Select to Output				25	50	100	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q				15	30	60	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q				20	35	70	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q	15	30	60				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q	35	75	100				ns

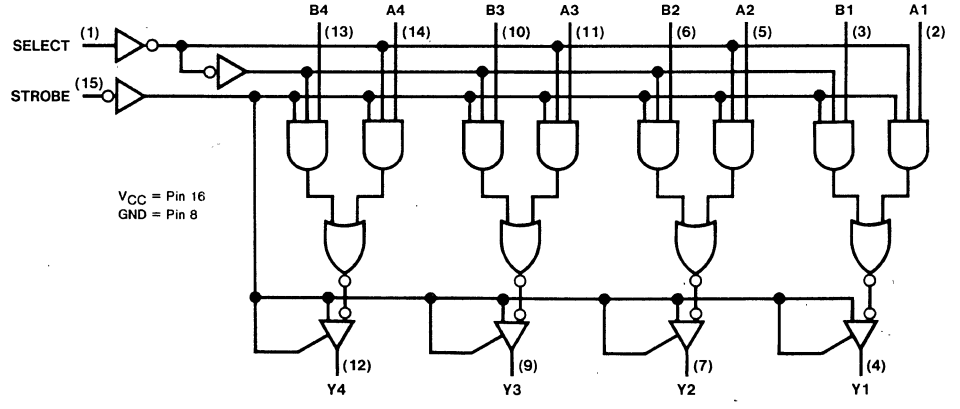
Logic Diagrams

L22



TL/F/6646-2

L23



TL/F/6646-3

7

National Semiconductor

DM75L51/DM85L51 TRI-STATE® 4-Bit D Type Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus lines. Detailed operation is given in the truth table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 59 ns
- Typical frequency 15 MHz
- Typical power dissipation 27.5 mW

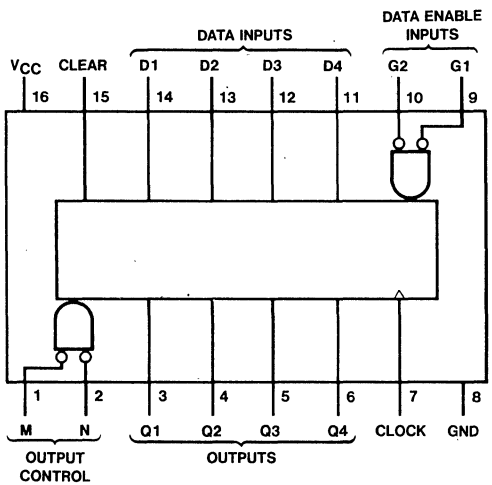
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6647-1

75L51 (J) 85L51 (N)

Function Table

Inputs					Output
Clear	Clock	Data Enable G1	Data Enable G2	Data D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Recommended Operating Conditions

Sym	Parameter		DM75L51			DM85L51			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width Clock or Clear		100			100			ns
t_{SU}	Setup Time	Enable	45			45			ns
		Data	30			30			
t_H	Hold Time	Enable	0			0			ns
		Data	10			10			
t_{REL}	Clear Release Time		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM75		0.15	0.3	V
			DM85		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.3V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−3		−15	mA
			DM85	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			5.5	9	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

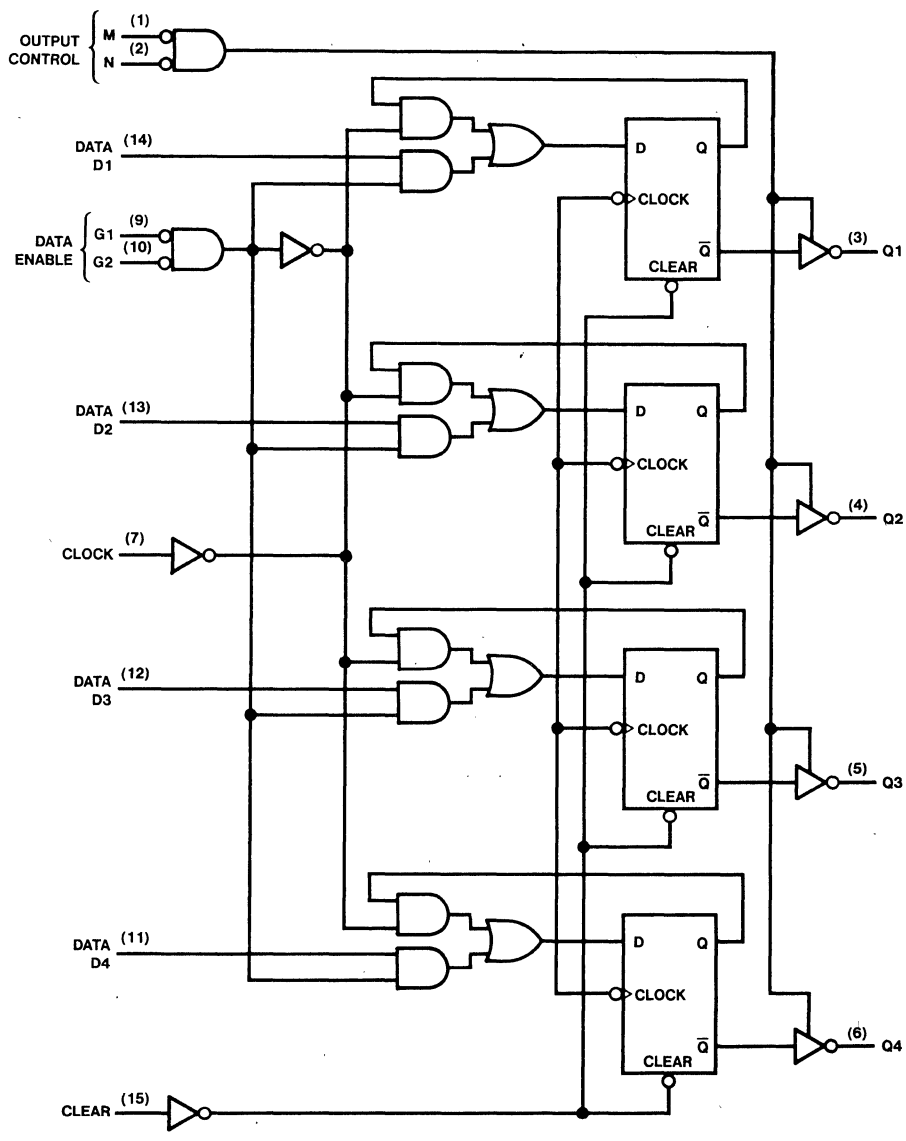
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open; CLEAR grounded following momentary connection to 4.5V; N, G1, G2, and all DATA inputs grounded; and the CLOCK and M at 4:5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency					6	15		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output					39	70	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output					77	120	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output					72	110	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q					28	55	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q					35	60	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q		18	50				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q		32	75				ns

Logic Diagram



TL/F/6647-2

National Semiconductor

DM75L52/DM85L52, DM75L54/DM85L54 TRI-STATE® Synchronous Counters/Latches

General Description

These circuits logically combine the functions of counters for frequency division, latches to store the data from the counters, and output buffer gates which provide both standard TTL outputs as well as high-impedance outputs for multiplexing of data. The counters are fully synchronous, and are made up of four edge-triggered JK flip-flops. To further facilitate operation, the Count Mode and Terminal Count outputs are also operable when the data outputs are in the high-impedance state or the latch mode.

Features

- DM75L52/85L52 Decade counter/latch
- DM75L54/85L54 Binary counter/latch
- Typical power dissipation 38 mW
- Typical clock frequency 11 MHz

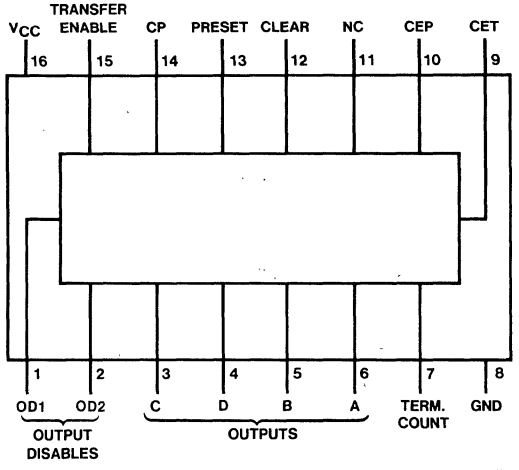
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6648-1

75L52 (J) 85L52 (N)
75L54 (J) 85L54 (N)

Function Table

Inputs							Outputs				
OD1	OD2	CEP	CET	Clear	Preset	TE	A	B	C	D	TC
H	X	X	X	X	X	X	"High Impedance State"				*
X	H	X	X	X	X	X	"High Impedance State"				*
L	L	X	X	H	X	H	L	L	L	L	L
L	L	X	X	L	H	H	H	H	H	H	*
L	L	X	X	X	X	L	LATCH				*
L	L	H	H	L	L	H	COUNT				*

*Function of the count sequence.

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
TE = Transfer Enable
TC = Term. Count

Recommended Operating Conditions

Sym	Parameter	DM75L52, L54			DM85L52, L54			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current (Except Terminal Count Input)			−1			−1	mA
I_{OH}	High Level Output Current (Terminal Count)			0.2			0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency	0		6	0		6	MHz
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'L52 and 'L54 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM75	2.4			V
			DM85	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM75		0.15	0.3	V
			DM85		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V	CET			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	CET			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	CET			−0.36	mA
			Others			−0.18	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.3V, V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−3		−15	mA
			DM85	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max			7.6	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'L52 and 'L54 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$						Units
		$C_L = 5\ pF$			$C_L = 50\ pF$			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency				6	11			MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output					115	220	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output					75	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Transfer Enable to Output					90	160	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Transfer Enable to Output					90	160	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q					75	150	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q					90	150	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q		8	15				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q		57	105				ns

Mode of Operation

When the Transfer Enable (TE) is at a logical "1" level, the data transfer paths between the counter outputs and the output buffer gates are maintained. When the Transfer Enable is at a logical "0" level, the data transfer paths are inhibited, and the state of the output buffer gates are locked in by the latches. The counter and Terminal Count (TC) output remain operable during this time.

Asynchronous Clear resets the counter to 0000.

Asynchronous Preset sets the counter to 1111. The 1111 state may be used in the L52 for blanking out leading zeroes in visual displays. The next clock pulse will advance the L52 to 0001 which denotes the first count of the blanked zero. The next clock pulse will advance the L54 to 0000.

The Terminal Count (TC) output is active high when the counters are at terminal count and the CET is high. The Terminal Count logic equations are:

(L52) $TC = CET \cdot A \cdot \overline{B} \cdot \overline{C} \cdot D$
(L54) $TC = CET \cdot A \cdot B \cdot C \cdot D$

The following logic levels control the device:

- The counters change state on the positive-going transition of the clock.
- Clearing or presetting is enabled by taking the respective input to a logical "1" level.
- To enable the count mode both CET and CEP inputs must be at a logical "1" level.
- To latch the outputs the Transfer Enable (TE) input must be taken to the logical "0" level.
- To place the TRI-STATE outputs into the "third-state," either of the Output Disable (OD) inputs must be taken to the logical "1" level.

The clock input must be high during the high to low transition of CEP and/or CET for correct logic operation. The CEP and CET inputs may be used in a high speed look ahead technique.

Counter stages can be cascaded to provide multiple stage BCD or Binary synchronous counting by using the L52 or the L54, respectively. With a Terminal Count (TC) fan out of ten, eleven stages are able to operate at the maximum frequency equivalent to a two stage counter.

The characters displayed can be held with a low level on the TE input while the counters can continue counting. The display can be updated at any time by applying a positive pulse to the TE input.

DM75L52/DM85L52
DECADE COUNT SEQUENCE

Count	Outputs				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H
**If Preset Applied Next Count	H H	H L	H L	H L	L L

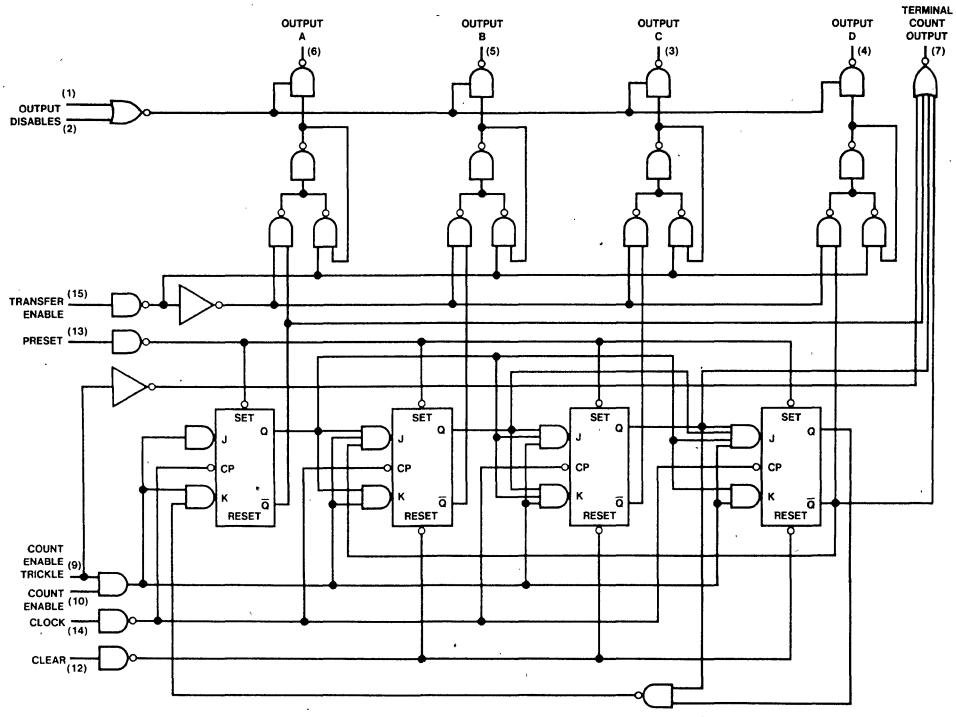
**The 111 state may be used in conjunction with certain decoder/drivers (DM7446A, 7447A, 7448) for blanking leading zeroes.

DM75L54/DM85L54
BINARY COUNT SEQUENCE

Count	Outputs				
	A	B	C	D	TC
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

Logic Diagrams

L52



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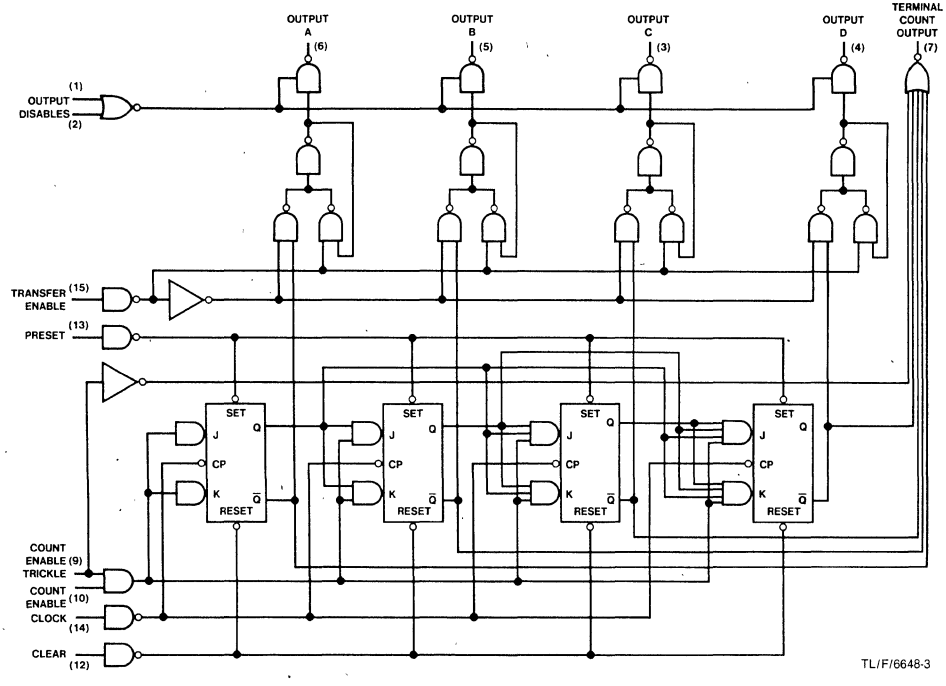
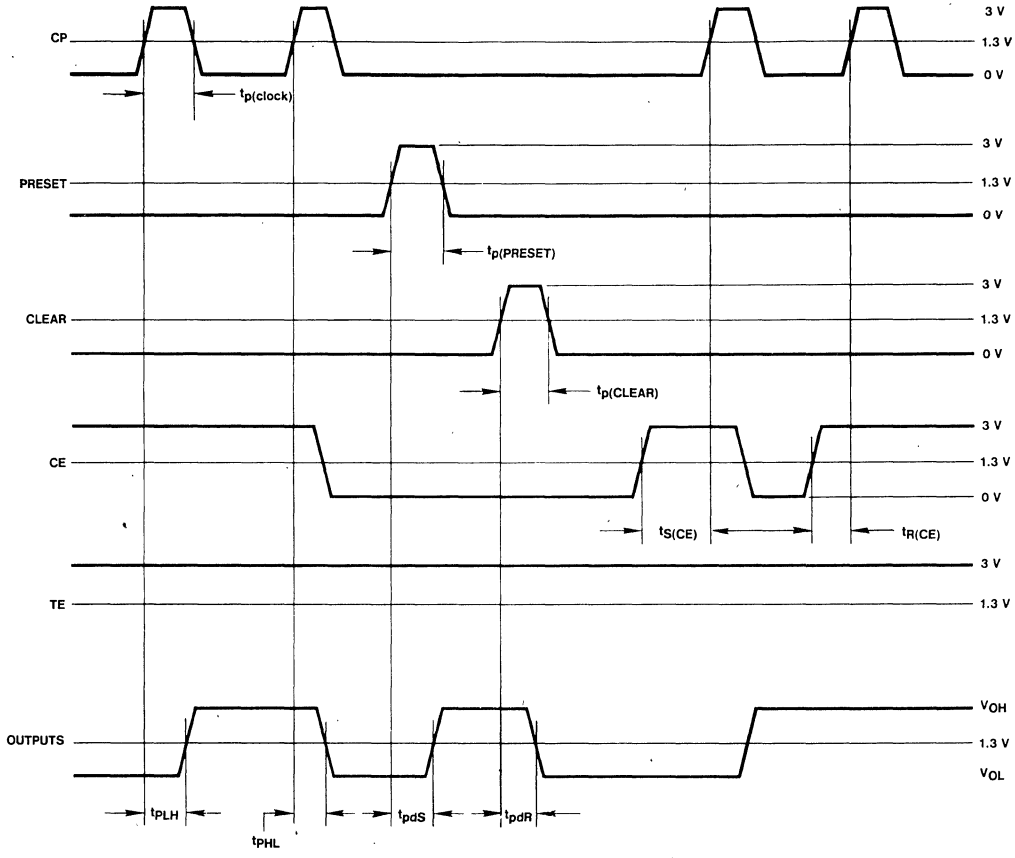
L54



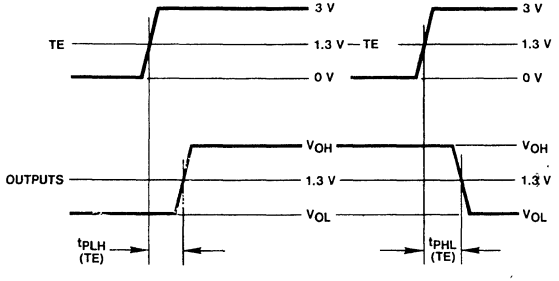
TL/F/6648-3

Switching Time Waveforms

L52, L54



TL/F/6648-4



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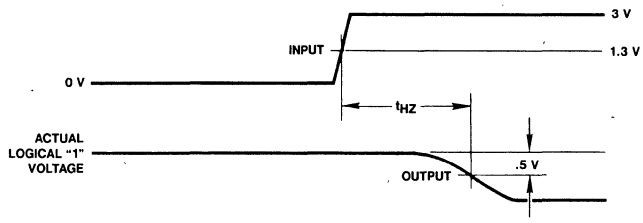
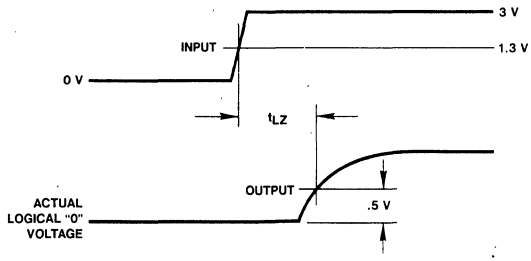
Switching Time Waveforms (Continued)

t_{HZ}



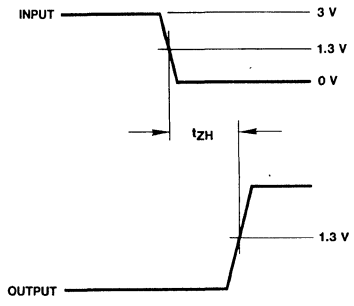
TL/F/6648-6

t_{LZ}



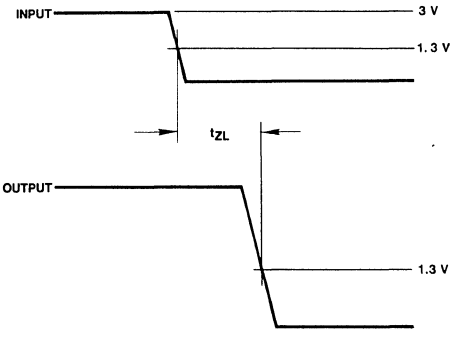
TL/F/6648-7

t_{ZH}



TL/F/6648-8

t_{ZL}



TL/F/6648-9

National Semiconductor

DM75L60/DM85L60, DM75L63/DM85L63 Synchronous 4-Bit Up/Down Decade/Binary Counters

General Description

These circuits are synchronous up/down counters; the L60 circuit is a BCD counter and the L63 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

Features

- **Fully independent clear input**
- **Synchronous operation**
- **Cascading circuitry provided internally**
- **Individual preset for each flip-flop**
- Typical count frequency 12 MHz
- Typical power dissipation 40 mW

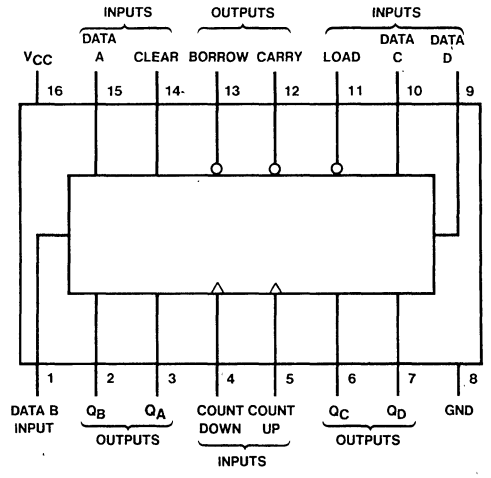
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6649-1

DM75L60 (J) **DM85L60 (N)**
DM75L63 (J) **DM85L63 (N)**

7

Recommended Operating Conditions

Sym	Parameter	DM75L60, L63			DM85L60, L63			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency	0		6	0		6	MHz
t_W	Pulse Width of Any Input	70			70			ns
t_{SU}	Data Setup Time	30			30			ns
t_H	Data Hold Time	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS60 and 'LS63 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM75		0.15	0.3	V
			DM85		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−3		−15	mA
			DM85	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			8	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

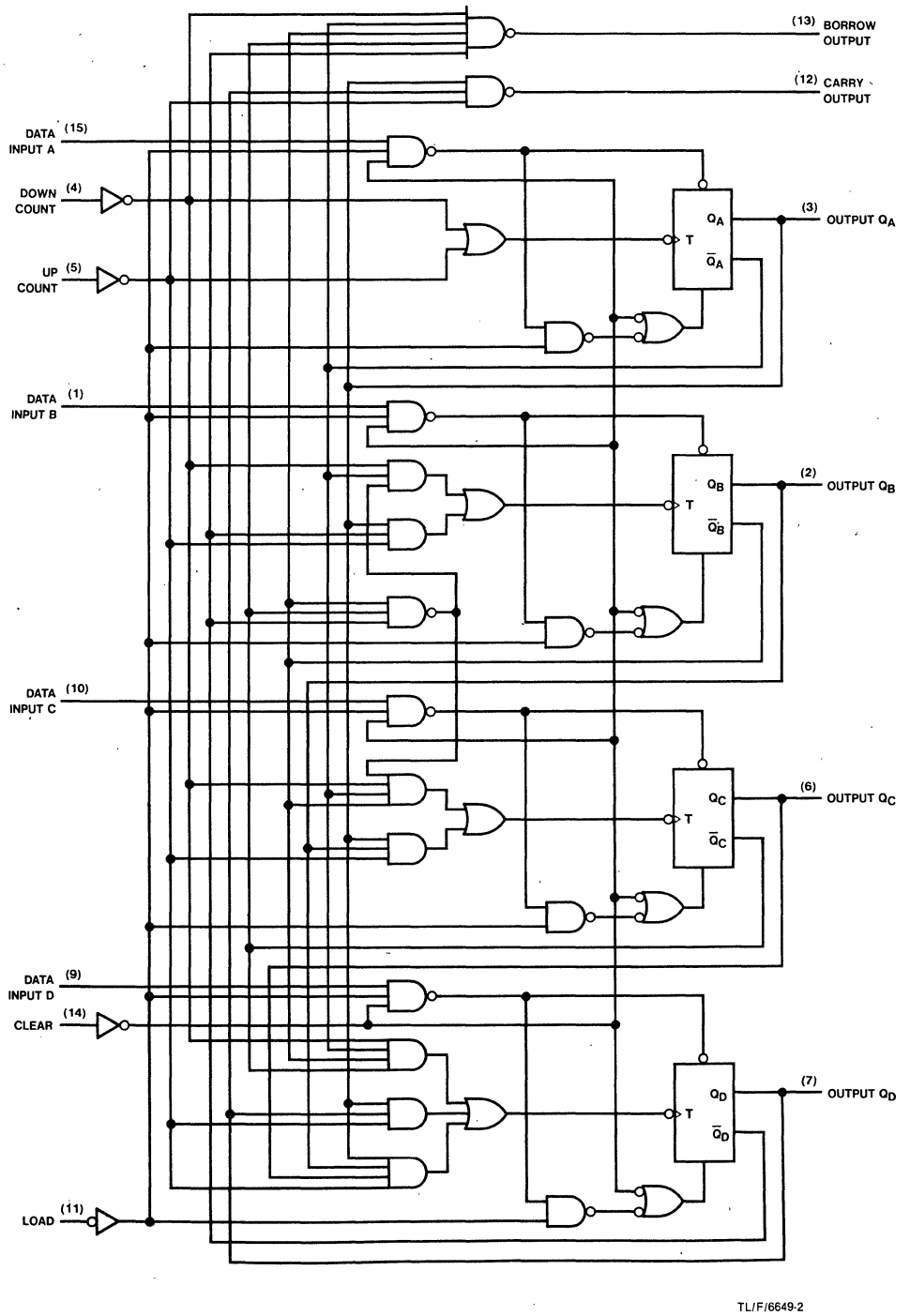
'**L60 and 'L63 Switching Characteristics** at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	12		ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		30	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		60	120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		30	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		50	100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Either Count to Q		45	90	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Either Count to Q		75	150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Q		55	110	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Q		105	200	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		95	190	ns

Logic Diagrams

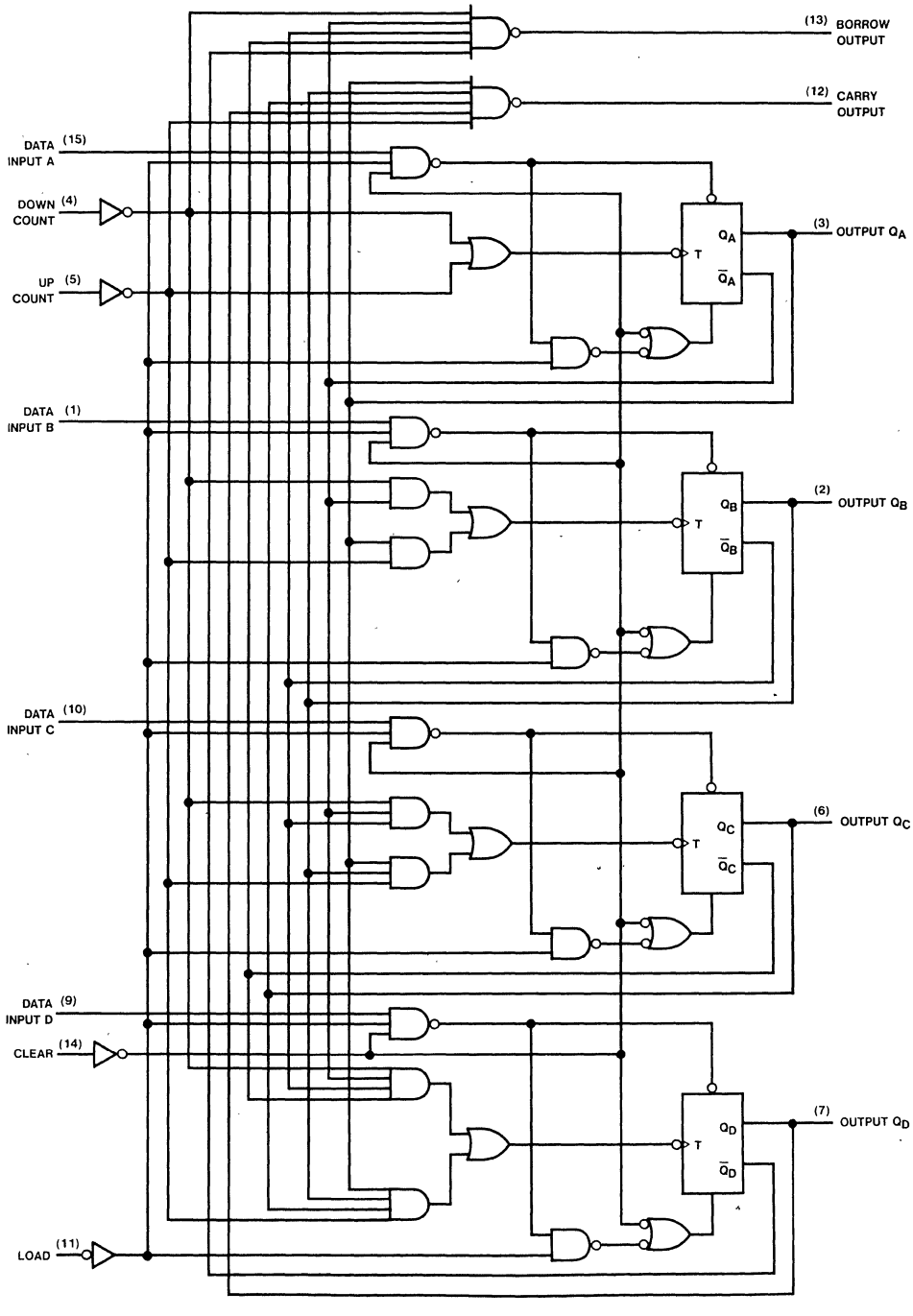
L60



TL/F/6649-2

Logic Diagrams (Continued)

L63



TL/F/6649-3

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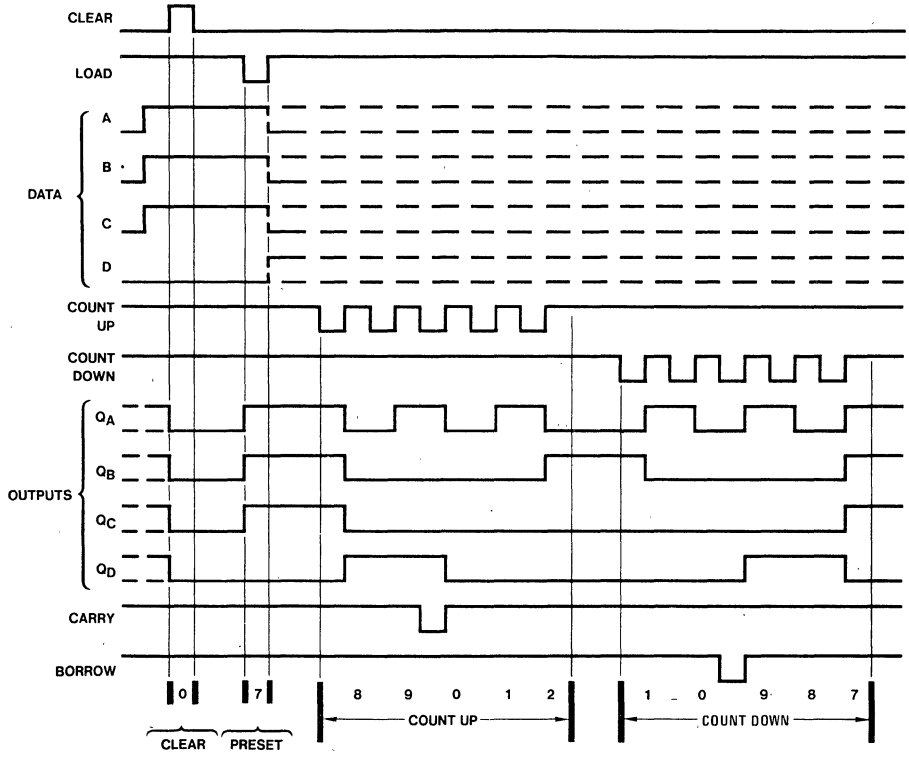
Timing Diagrams

L60 Decade Counters
Typical Clear, Load and Count Sequences



TL/F/6649-4

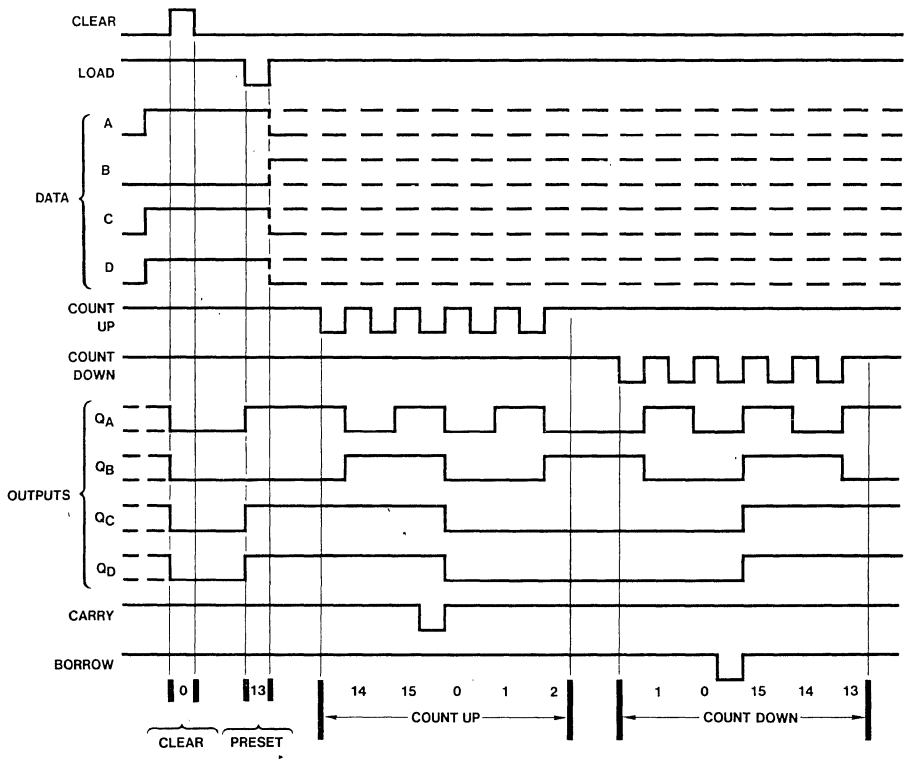
Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

L63 Binary Counters
Typical Clear, Load and Count Sequences



TL/F/6649-5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

7

National Semiconductor

DM76L70/DM86L70 8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 14 MHz
- Typical power dissipation 30 mW

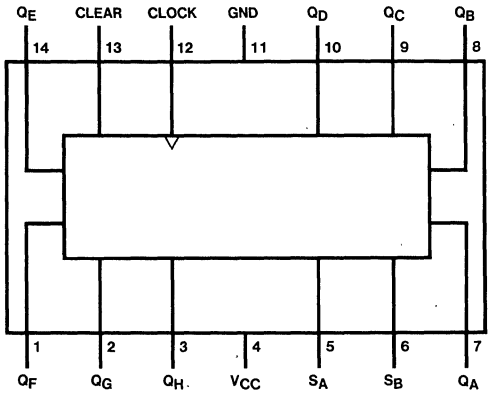
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6650-1

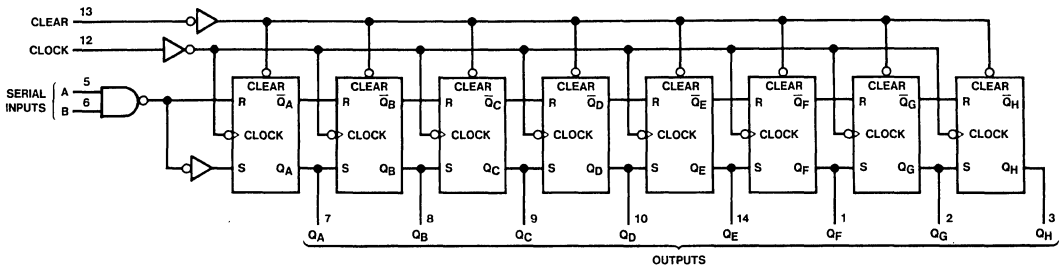
76L70/86L70 (W)

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

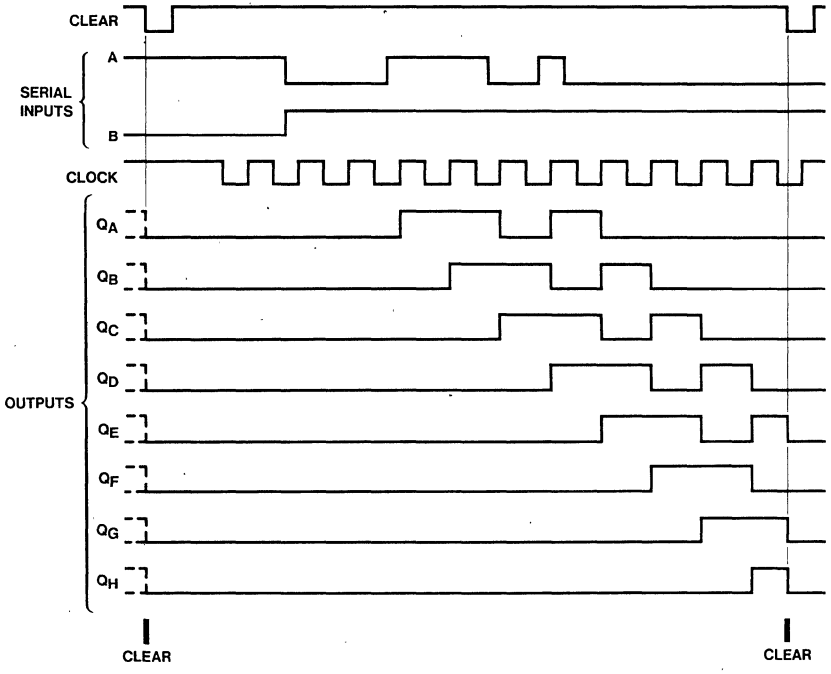
Logic Diagram



TL/F/6650-2

Timing Diagram

Typical Clear, Shift, and Clear Sequences



TL/F/6650-3

Recommended Operating Conditions

Sym	Parameter	DM76L70			DM86L70			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA

Recommended Operating Conditions (Continued)

Sym	Parameter		DM76L70			DM86L70			Units
			Min	Nom	Max	Min	Nom	Max	
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock	60	40		60	40		ns
		Clear	60	40		60	40		
t_{SU}	Data Setup Time		40	20		40	20		ns
t_H	Data Hold Time		20	−5		20	−5		ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM76			0.3	V
			DM86			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	Clear			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Clear			20	μA
			Other			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Clear			−0.36	mA
			Other			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM76	−3		−15	mA
			DM86	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6	9	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF (Note 4)			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	14		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		50	85	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		90	135	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		75	120	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to CLEAR.

Note 4: C_L = 15 pF for f_{MAX} only.

National Semiconductor

DM76L75/DM86L75, DM76L76/DM86L76 Presettable Decade/Binary Counters

General Description

These synchronous, presettable counters are true tenth-power versions of the popular DM54160A/DM74160A, DM54161A/DM74161A, DM9310, and DM9316 counters. They feature an internal carry/look ahead for high-speed cascading, and trigger on the positive-going transition of the clock pulse. The counters are fully programmable; and, since presetting is synchronous, applying a low logic level to the load input disables the counter and forces the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs. Low-to-high transitions at the load inputs are acceptable, regardless of the logic levels on the clock or enable inputs. The clear (reset) function is asynchronous, and a low level applied to the clear input sets all four outputs low regardless of the levels on the clock, load, or enable inputs. In high-speed cascading arrangements, both count-enable inputs (P, T) must be high to count, and input T is fed forward to enable the ripple carry output. This high-level overflow ripple carry pulse can be used to enable successive stages. High-to-low level transitions at the P or T enable inputs are permitted, regardless of the logic level on the clock.

Features

- Low power versions popular counters
  DM76L75/DM86L75 = DM54160A/DM74160A, DM9310—decade counter
  DM76L76/DM86L76 = DM54161A/DM74161A, DM9316—binary counter
- Internal look-ahead for fast cascading
- Counters are fully synchronous and presettable
- Typical power dissipation 33 mW

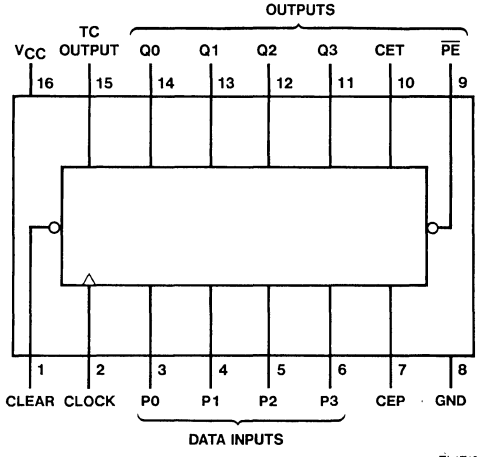
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6651-1

76L75 (J) 86L75 (N)
76L76 (J) 86L76 (N)

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Recommended Operating Conditions

Sym	Parameter		DM76L75, L76			DM86L75, L76			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock	60	25		60	25		ns
		Reset	80	30		80	30		
t_{SU}	Setup Time	CE	65	40		65	40		ns
		Data	30	15		30	15		
		PE	65	40		65	40		
t_H	Hold Time	CE	80	50		80	50		ns
		Data	30	15		30	15		
		PE	65	40		65	40		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'L75 and 'L76 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM76		0.2	0.3	V
			DM86		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	CET			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CET			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	CET			−0.36	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM76	−3		−15	mA
			DM86	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max			6.5	9	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

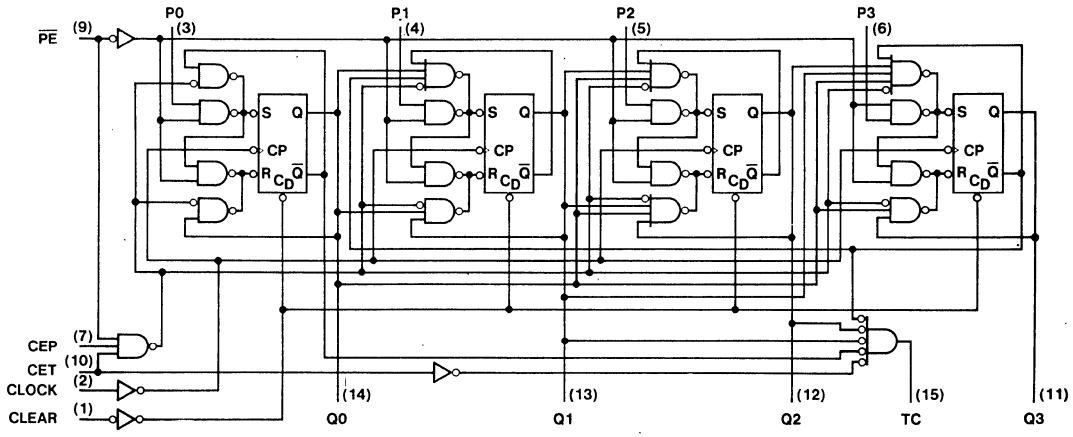
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	13		ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q		45	75	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q		65	110	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to TC		70	115	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to TC		85	140	ns
t_{PLH} Propagation Delay Time Low to High Level Output	CET to TC		35	60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	CET to TC		35	60	ns

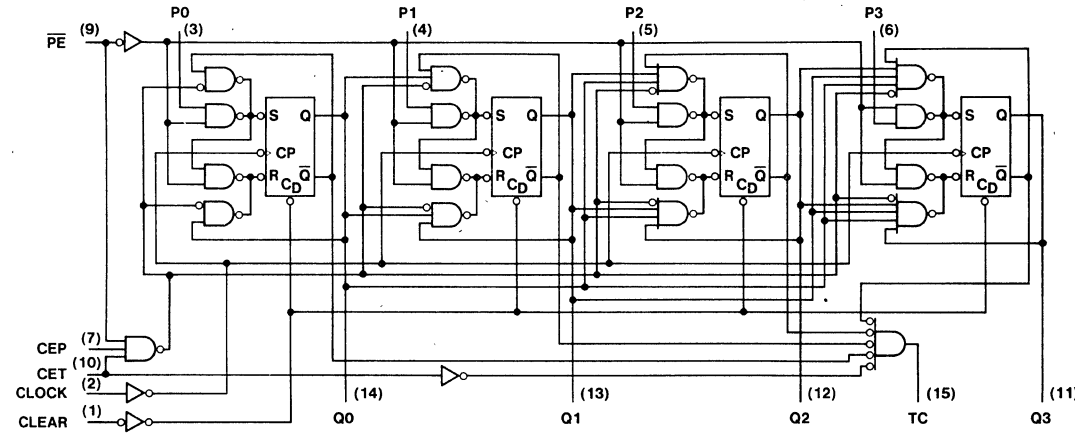
Logic Diagrams

76L75/86L75 (Decade)



TL/F/6651-2

76L76/86L76 (Binary)



V_{CC} = (16)
GND = (8)

TL/F/6651-3

National Semiconductor

DM76L90/DM86L90 8-Bit Parallel In/Serial Out Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 14 MHz
- Typical power dissipation 80 mW

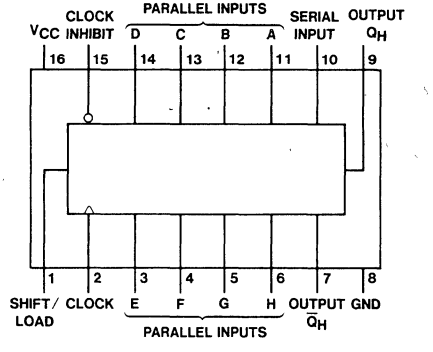
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6652-1

DM76L90 (J) DM86L90 (N)

Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

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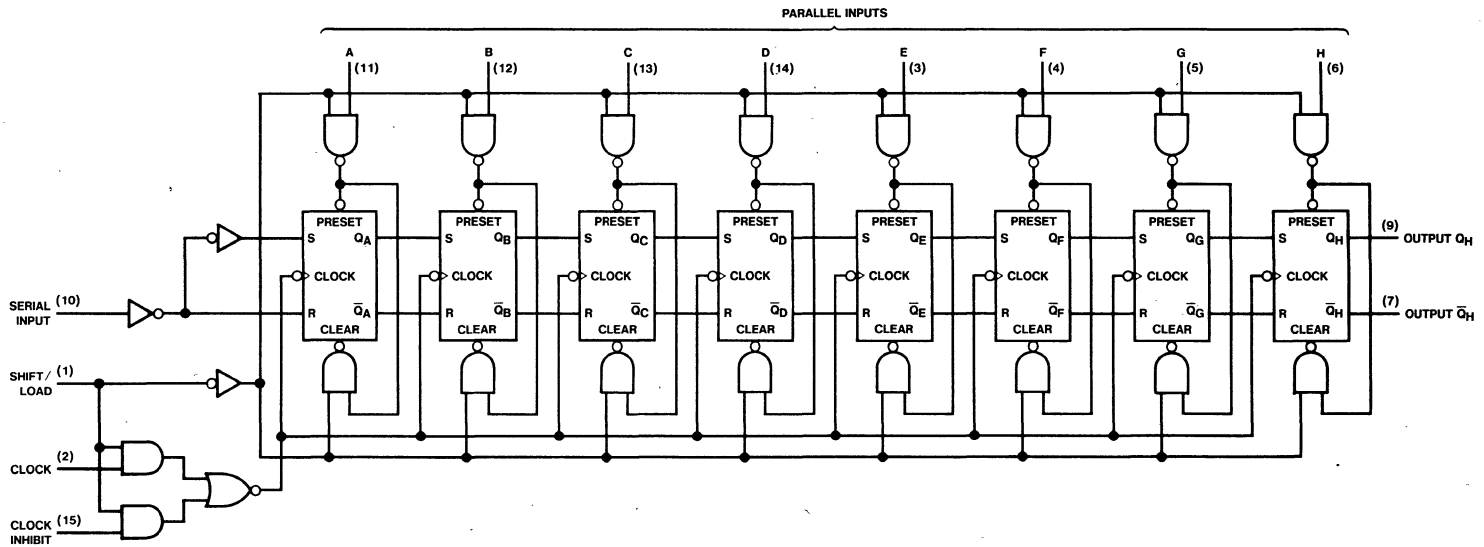
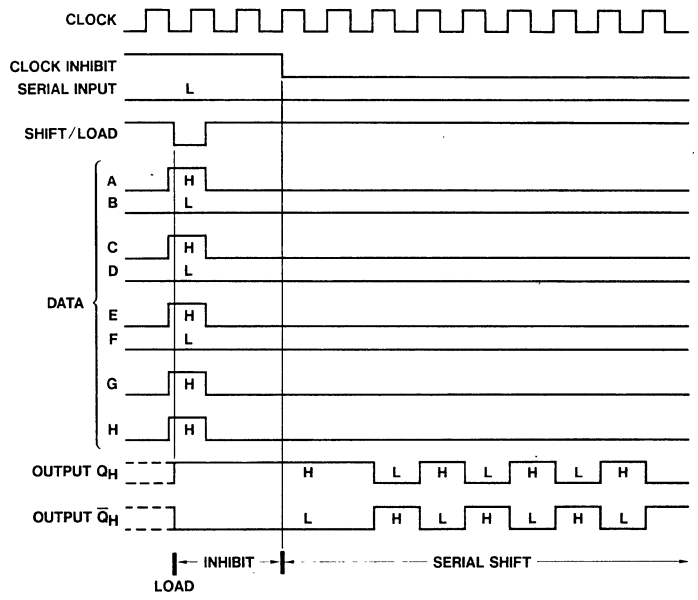
Logic Diagram



Timing Diagram

Typical Shift, Load and Inhibit Sequences



TL/F/6652-2

Recommended Operating Conditions

Sym	Parameter	DM76L90			DM86L90			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency	0		6	0		6	MHz
t_W	Pulse Width (Clock, Load)	100			100			ns
t_{SU}	Data Setup Time	44	22		44	22		ns
t_H	Data Hold Time	10			10			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM76			0.3	V
			DM86			0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Load			30	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Load			−0.54	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM76	−3		−15	mA
			DM86	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				9.5	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ C_L = 50 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	14		ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		44	88	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		62	124	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		35	70	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		50	100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to Q_H		33	66	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to Q_H		56	112	ns
t_{PLH} Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		33	66	ns
t_{PHL} Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		56	112	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With the outputs open, CLOCK INHIBIT and SHIFT/LOAD at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then with them at 0V.

Section 8
Appendices/
Physical Dimensions

8

Section Contents

INTRODUCTION TO THE RELIABILITY MILITARY/AEROSPACE PROGRAMS

History

In the mid 1960's the various government agencies responsible for semiconductor reliability saw that screenable defects were resulting in an in-equipment failure rate of about 1% per thousand hours. In-depth failure analysis allowed them to determine what the predominate failure mechanisms were. The Solid State Applications Branch of the Air Force's Rome Air Development Center (RADC) was assigned the task of developing a screening procedure which would remove the infant mortality failures which had led to the high failure rate previously encountered. Working closely with other semiconductor reliability experts, the RADC staff developed MIL-STD-883, which was first issued in 1968. The objective of MIL-STD-883 was to create an economically feasible, standardized integrated circuit screening flow which would achieve an in-equipment failure rate of 0.08% per thousand hours for Class B and 0.004% per thousand hours for Class A (which was later superseded by Class S). Over the years this standard has grown and matured with a number of new test methods added as reliability information and failure analysis results became more detailed. These developments have led to one of the strongest and most comprehensive screening specs available, MIL-STD-883.

Purpose and Structure

MIL-STD-883 states: this standard establishes uniform methods and procedures for testing microelectronic devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations, and physical and electrical tests. What does this mean to the semiconductor user? To understand this, one must subdivide MIL-STD-883 into two primary areas: 1) Detailed how-to specifications (methods 1001 through 4007) and 2) Screening and qualification and/or quality conformance testing requirements (methods 5001 through 5009). By examining each of these areas the thrust of MIL-STD-883 will become apparent.

Detailed How-to Specifications

MIL-STD-883 is a collection of environmental, mechanical, visual, and electrical test methods. These methods define tests which enable manufacturers and users to screen for specific reliability concerns. The tests covered include moisture resistance, high temperature storage, neutron irradiation, shock and acceleration tests, visual radiography, and dimensional tests, to mention only a few. In the electrical test section, there are tests to examine load conditions, power supplies, short circuit currents, and other tests. Each of these tests is designed to look at specific reliability and quality concerns that affect semiconductor products.

Screening Flows

The overall reliability requirements for a system depend upon a number of factors, including cost-effectiveness. For example, a deep space probe, where component replacement is impossible once the system is launched, requires very high reliability, despite the inherent cost of complex screening. On the other hand, a ground-based radio unit can use a less stringent reliability testing sequence, since a failed component can be easily replaced at moderate cost. In line with this range of needs, MIL-STD-883 established three distinct product assurance levels to provide reliability commensurate with the product's intended application. The three levels are Class S (intended for critical applications, such as space), Class B (intended for less critical applications, such as airborne or ground systems), and Class C (intended for easily replaceable systems, which has since been eliminated).

National and MIL-M-38510

A major thrust exists among integrated circuit users, suppliers, and the U.S. Government to avoid proliferation of military procurement specifications by turning instead to standardized high reliability microcircuits. National Semiconductor endorses and supports this trend.

One major program to which National is heavily committed is the JAN MIL-M-38510 IC program. This is a standardization program administered by the U.S. Defense Department which allows a user to purchase a broad line of standard products from a variety of qualified suppliers.

There is only one MIL-M-38510 program. National is committed to supplying only QPL devices, and discourages any "pseudo-38150" alternates.

There are two levels specified within MIL-M-38510 — Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems.

MIL-M-38510

The Defense Electronic Supply Center (DESC) administers the integrated circuit standardization program known as MIL-M-38510 (sometimes referred to as the JAN IC Program). The specification set used to define the program consists of four documents: general specification MIL-M-38510, which is an overall definition of the processing and testing to be performed; detail specifications (referred to as "slash sheets"), each of which defines the performance parameters for a unique generic device or a family of devices; MIL-STD-883, which defines specific screening procedures; and MIL-STD-976, which defines line certification requirements.

When a user orders a MIL-M-38510 device, he is guaranteed that he will get a device fully conformant with the detail specification and which has also met all of the general testing and processing requirements. DESC requires semiconductor suppliers to become formally qualified under the MIL-M-38510 program and to be listed on the current Qualification Products List (QPL) before they are allowed to legally ship JAN devices.

Advantages to the User

The JAN 38510 program has numerous advantages for the integrated circuit user.

- A single explicit specification eliminates guesswork concerning device electrical characteristics or processing flow.
- The rigorous schedule of quality conformance testing that is a mandatory part of the MIL-M-38510 program assures the user of long-term stability.
- Since the electrical characteristics of the devices are at least as tight as the "standard industry data sheet" parameters, device performance will meet the vast majority of system design requirements. Additionally, min./max. limits replace many data sheet typicals, making circuit design and worst case design analysis decisions easier.
- The user is spared the expense of researching and preparing his own procurement document.
- The user is spared the expense of qualification testing. The QPL tells him which suppliers have qualified the device he requires.
- The QPL gives the user a choice of qualified suppliers for devices that are fully interchangeable. In addition, the presence of several sources guarantees competitive pricing that is typically lower than for devices to a user's own specifications.
- Since MIL-M-38510 is a standard program, procurement lead times will be shorter. With a large number of programs using JAN devices, distributors and manufacturers are able to establish inventories of JAN devices. National in particular is committed to maintaining finished goods and work-in-process inventories to support our customers' needs.
- Spare parts will be readily available without excessive minimum order requirements.
- Standard parts with volume requirements will remain in production longer.
- Device markings are consistent from one manufacturer to another.
- The program is extremely cost-effective. A user can purchase a few devices for engineering evaluation and prototyping and know that they will be identical to the devices he will get during production. When the cost factors associated with spec. writing, supplier qualification, maintaining voluminous parts control documentation, and the more intangible benefits of device availability are totaled, use of JAN ICs is overwhelmingly the most cost-effective approach.

Advantages to the Supplier

What motivates a supplier like National Semiconductor to be so heavily committed to the MIL-M-38510 program? National has the *broadest* range of reliability processed products available in the semiconductor industry. A program such as MIL-M-38510 helps to standardize the processing required and to minimize the number of individual user specifications. This allows National to concentrate more resources on this program, thereby improving product quality and availability.

The Most Frequently Asked Questions and Answers about MIL-M-38510

There are many questions which are frequently asked regarding the MIL-M-38510 program. We would like to answer some of them.

Q. WHAT MUST A MANUFACTURER DO TO GET HIS PARTS LISTED ON THE QPL?

A. There are two things which a manufacturer is required to do. First, he must get his facilities (including wafer fab, assembly, and rel processing areas) certified by DESC. This requires that each fab area used for QPL devices must be approved. Second, for each specific device and package combination listed on the QPL, the manufacturer must perform extensive qualification testing and provide detailed device information to DESC. This data is typically supplied in two phases.

In the first phase, the manufacturer must supply detailed information concerning the device construction and electrical characteristics. Once this data has been verified by DESC to confirm that the manufacturer's device meets the MIL-M-38510 requirements, the manufacturer is listed on Part II of the QPL. At this point the manufacturer is legally able to supply full JAN qualified devices meeting ALL of the MIL-M-38510 requirements. The manufacturer must then perform the full qualification testing of Method 5005 of MIL-STD-883 as specified in paragraph 4.4 of MIL-M-38510. Once this data has been reviewed and accepted by DESC, the manufacturer is listed on Part I of the QPL.

Q. IS THERE ANY DIFFERENCE IN DEVICES PRODUCED WHILE A MANUFACTURER IS LISTED ON PART II OF THE QPL AND THOSE PRODUCED AFTER PART I QUALIFICATION IS COMPLETED?

A. There is absolutely *no difference*. A supplier must meet all of the device screening and quality conformance requirements no matter what his QPL status.

Q. HOW DOES A USER KNOW WHAT DEVICES ARE COVERED BY SLASH SHEET SPECIFICATIONS?

A. Supplement 1 to MIL-M-38510 contains a listing of the slash sheet specifications and a cross reference to the generic part type. This is updated as new slash sheets are released. National's Reliability Handbook also contains a cross reference.

Q. HOW CAN A USER OBTAIN COPIES OF THE QPL, SUPPLEMENT 1 OF MIL-M-38510, MIL-M-38510 ITSELF, AND MIL-STD-883?

A. Copies of these and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

Q. WHAT ABOUT THOSE DEVICES FOR WHICH NO DETAIL SPECIFICATION EXISTS?

A. The ultimate aim of a standardization program must be to furnish *all* parts. Requests for addition of a part to MIL-M-38510 should be made to DESC Directorate of Engineering, Dayton, Ohio 45444, indicating a need for slash sheets and/or suppliers to be qualified for the additional devices. National has a form (available through local sales offices) which may be used for this purpose. In addition, if only some parts are available, a user can still see significant savings on those that are available.

Q. HOW IS A JAN QPL DEVICE MARKED?

A. Tables I and II explain the details of the marking for JAN ICs.

TABLE I. MIL-M-38510 Part Marking

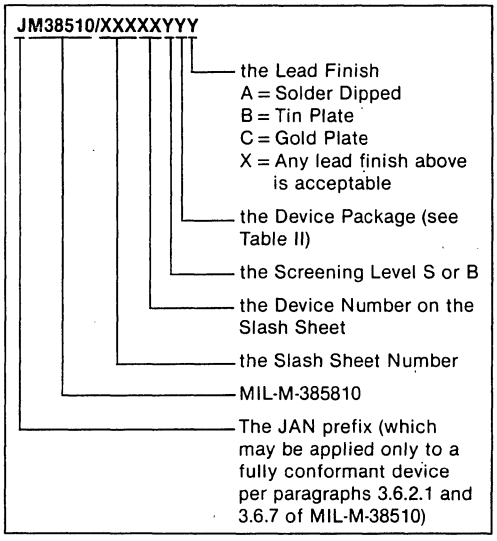


TABLE II. JAN Package Codes

38510 PACKAGE DESIGNATION	MICROCIRCUIT INDUSTRY DESCRIPTION
A	14-pin 1/4″ x 1/4″ (metal) flatpack
B	14-pin 3/16″ x 1/4″ flatpack
C	14-pin 1/4″ x 3/4″ dual-in-line
D	14-pin 1/4″ x 3/8″ (ceramic) flatpack
E	16-pin 1/4″ x 7/8″ dual-in-line
F	16-pin 1/4″ x 3/8″ (metal or ceramic) flatpack
G	8-pin TO-99 can or header
H	10-pin 1/4″ x 1/4″ (metal) flatpack
I	10-pin TO-100 can or header
J	24-pin 1/2″ x 1-1/4″ dual-in-line
K	24-pin 3/8″ x 5/8″ flatpack
M	12-pin TO-101 can or header
P	8-pin 1/4″ x 3/8″ dual-in-line
Q	40-pin 8/16″ x 2-1/16″ dual-in-line
R	26-pin 1/4″ x 1-1/16″ dual-in-line
S	20-pin 1/4″ x 1/2″ flatpack
V	18-pin 3/8″ x 1-15/16″ dual-in-line
W	22-pin 3/8″ x 1-1/8″ dual-in-line
X, Y, Z	Unassigned — Reserved for identifying special packages whose dimensions are carried in the detail specifications.

Q. ARE DEVICES CALLED "M38510, JAN PROCESSED, JAN EQUIVALENT, ETC." REALLY QPL PRODUCTS?

A. *Absolutely not*. There is only one QPL product — it is a JM38510 marked device. "JAN Equivalent" is expressly forbidden by para-

graphs 3.1 and 3.6.7 of MIL-M-38510. MIL-M-38510 does provide for the production of devices when no qualified sources exist, but this may be done only with prior DESC approval, and products produced under this provision must meet all requirements of MIL-M-38510 other than qualification.

Q. HOW LONG CAN A SUPPLIER REMAIN ON PART II OF THE QPL?

A. For Class B, a manufacturer can remain on Part II for two years or until 90 days after another supplier becomes qualified for the same device package, screening level, and lead finish combination on Part I of the QPL. Class S devices may remain on Part II for one year after another manufacturer reaches Part I.

Q. WHEN ANOTHER SUPPLIER OBTAINS PART I QUALIFICATION, ARE THE OTHER QUALIFIED SUPPLIERS REMOVED FROM PART II IMMEDIATELY?

A. No. The supplier is given 90 days before being removed from Part II for a Class B device and one year for a Class S device. During that time a supplier may legally accept orders for those devices. After the end of the 90-day or one year period, he may no longer accept orders but may complete and ship those orders received prior to that time, no matter how long it takes him to complete them.

Q. IS A SUPPLIER EVER REMOVED FROM PART I QUALIFICATION?

A. Generally not. As long as a supplier continues to manufacture the device, maintains appropriate facility approvals, and submits all required reports and information to DESC within stipulated time limits, he will retain QPL I listing. Violation of these requirements can be cause for removal from QPL.

Q. CAN AN AUTHORIZED DISTRIBUTOR SHIP JAN DEVICES FROM HIS SHELVES IF THE MANUFACTURER HAS LOST HIS QPL LISTING FOR THOSE DEVICES?

A. Yes. As long as those devices were ordered by the authorized distributor while the manufacturer had QPL listing for those devices, the distributor may subsequently ship those devices from his shelves.

Q. CAN A MANUFACTURER LEGALLY SHIP JAN QPL MATERIAL HE ASSEMBLED AND TESTED BEFORE HE RECEIVED A QPL LISTING?

A. Yes. The manufacturer must assemble and screen parts to prove his ability to comply with the specifications before he can be placed on QPL. As a result, his first lot of material, which is fully conformant to QPL product requirements, will have a date code that is earlier than the date he is placed on the QPL. However, the manufacturer may *not* begin to assemble and test unless he has a line certification and an approval to proceed with qualification.

Q. WHAT IS THE RELATIONSHIP BETWEEN MIL-M-38510 AND MIL-STD-883?

A. MIL-M-38510 defines complete program requirements and the detail device electrical performance parameters. The device processing requirements are specified in MIL-STD-883.

Q. SUPPOSE DEVICES ARE KEPT ON A MANUFACTURER'S OR DISTRIBUTOR'S SHELVES FOR A PERIOD OF TIME; MUST THEY EVER BE RETESTED TO VALIDATE THAT THEY STILL MEET SLASH SHEET CHARACTERISTICS?

A. Yes. Devices held by a manufacturer or by his authorized distributor which have a date code older than 36 months must be retested by the manufacturer in accordance with Group A sampling requirements prior to shipment to a customer or return to inventory.

Q. WHY SHOULD A USER SPECIFY "X" IN THE LEAD FINISH DESIGNATION FOR A PART TYPE?

A. A manufacturer who receives an order for a specific lead finish for which he is qualified but has no inventory at the time of order may not be able to fill the order in a timely manner, even though he might have substantial inventory of another lead finish. Unless a user has a specific reason for wanting a particular lead finish, he should allow his suppliers the flexibility of shipping whatever finish is available.

Q. WHAT DATA IS A MANUFACTURER REQUIRED TO SHIP WITH A JAN PART?

A. A certificate of conformance is all that is required. However, he must retain all data for three years.

Q. CAN A DEVICE FOR WHICH THERE IS NO SLASH SHEET BE PROCESSED TO MIL-M-38510?

A. Since MIL-M-38510 invokes a combination of the processing requirements of MIL-STD-883 and the detail device performance parameters contained in each individual slash sheet, the answer is obviously no. However, National's 883B/RETS™ program does provide parts which meet all of the screening requirements of the MIL-STD-883 specification and which have been subjected to all of the MIL-M-38510 controls (except for domestic assembly).

TABLE III. Sample MIL-M-38510 Listing

GOVERNMENT DESIGNATION				TEST REPORT NUMBER	MANUFACTURER'S NAME
DEVICE TYPE*	DEVICE CLASS	CASE OUTLINE	LEAD MATERIAL AND FINISH		
M38510/008					
01	S only	A	C	38510-953-81	National Semiconductor Corp.
01	B	C	A	38510-953-81	National Semiconductor Corp.
02		D	B	38510-30-7T	
03	B	C	A	38510-520-83	National Semiconductor Corp.
			B		

*"M38510" is the military designator for MIL-M-38510. The QPL shows this notation even though the parts are fully qualified devices and are marked JM38510/XXXXXYYY.

Q. WHAT DOES A QPL LISTING LOOK LIKE AND HOW DO YOU READ IT?

A. Sample QPL listings are shown in Table III.

JM38510/00801SAC
JM38510/00801BCA
JM38510/00801BCB
JM38510/00801BDA
JM38510/00801BDB
JM38510/00802BCA
JM38510/00802BCB
JM38510/00802BDA
JM38510/00802BDB
JM38510/00803BCA
JM38510/00803BCB

Q. WHAT QUALITY CONFORMANCE TESTS ARE CONDUCTED? ARE ALL DEVICES IN A GENERIC FAMILY EVENTUALLY SUBJECTED TO QUALITY CONFORMANCE TESTING?

A. For B level devices quality conformance tests must be conducted as follows:

Group A—Each inspection lot or sublot.

Group B—Each inspection lot for each package type and lead finish on each detail specification.

Group C—Periodically at 3-month intervals on one device type or one inspection lot from each mircocircuit group in which a manufacturer has qualified device types (die related tests).

Group D—Periodically at a 6-month interval for each package type for which a manufacturer holds qualifications (package related tests).

Different devices within a generic family are chosen for successive quality conformance tests until all of the devices have been subjected to testing. The sequence is then repeated. The manufacturer must submit attributes data to DESC for all quality conformance tests performed.

Q. HOW IS AN INSPECTION LOT DEFINED?

A. For Class B devices, each inspection lot shall consist of microcircuits of a single device type, in a single package type and lead finish, or may consist of inspection sublots of several different device types, in a single package type and lead finish, defined by a single detail specification. Each inspection lot shall be manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and case with the same material requirements, and sealed within the same period not exceeding 6 weeks.

Q. WHAT IS NATIONAL SEMICONDUCTOR'S COMMITMENT TO MIL-M-38510?

A. National Semiconductor is convinced that the level of standardization offered by a program like MIL-M-38510 is the key to long-term military component procurement viability. We have a corporate commitment to MIL-M-38510. We believe that the program will be of significant benefit in lessening the problem of product obsolescence, for the volume provided will help to keep many key devices in production. We believe that the program will make possible the procurement of devices in small quantities with reasonable lead times for long-term spares or field maintenance requirements.

National Semiconductor will continue to maintain a broad base of line certifications and an extensive list of Class B and Class S device qualifications. We will continue to work with the Department of Defense, concerned users, and other semiconductor manufacturers to update and redefine the applicable specifications. We feel that this level of support is essential if MIL-M-38510 is to remain the strongest standardization program available.

In addition, we will continue to add capacity and to build up substantial inventories of a large spectrum of products to ensure the

availability and the lead times that are needed for key military programs.

National Mil/Aero Standardization Programs

Your customer has imposed upon you requirements for product reliability that you must meet on every single component you buy. In most cases, these requirements mandate that you buy JAN MIL-M-38510 parts where they are available, and that all other devices must be as close to JAN as is achievable. We don't consider this unreasonable. In fact, we believe that this is the only reasonable and intelligent approach.

To meet this objective, we designed our 883B/RETS program around requirements that were already imposed for the MIL-M-38510 program.* We realize that there are many so-called standardization programs available in the marketplace which lack the compliance that you need. Our 883B/RETS program is totally compliant. We invite you to make this comparison between what we offer and what you need. Our screening flow, our 5% PDA, our quality conformance test frequency, and the other items that you consider important, match exactly the requirements defined in MIL-M-38510.** If they did not, we could not offer ***Total Standardization***.

Standardization provides the manufacturing efficiencies needed by the semiconductor manufacturers if they are to meet military semiconductor needs. To the user, standardization offers the highest guarantee of quality and reliability through production consistency and uniformity. The most significant benefit of standardization to the Department of Defense, however, is that it ensures the availability of component level spares to key programs with the pricing, delivery, and reliability needed for the field support and maintenance of our key defense electronics systems.

National's MIL-M-38510 Emphasis

To implement this view of standardization, we have based our entire approach to military screening upon the Class S and Class B requirements of MIL-M-38510. We are convinced that to do less than this would be to provide an inferior product, one that does not meet the true needs of the Department of Defense. Our 883B/RETS microcircuits are processed through the most comprehensive and compliant Class B screening program offered by any semiconductor manufacturer. We have tried to emulate MIL-M-38510 to the fullest extent possible, with the same production controls, calibration schedules, rework and resubmission procedures, operator certification requirements, and all of the other key elements of MIL-M-38510. The procedures that we employ in the production of MIL-M-38510 devices are used for all of the military devices we manufacture.

Our 883S/RETS microcircuits are processed through a screening flow that matches the MIL-M-38510 Class S flow exactly. Our commitment to MIL-M-38510 Class S is such that once qualified for a given device type we will sell that part only as a JAN Class S part. Class S QPL listing will result in the immediate removal from production of the 883S/RETS version of the device.

National's Commitment

But compliance flows are obviously meaningless unless the capacity is in place to support them. We have the industry's largest screening capacity. Over the past few years we have reinvested substantial sums in additional capital equipment in both buildings and the equipment with which to fill those buildings. Our Tucson, Arizona plant was the first plant in the entire industry to be totally dedicated to the production of military integrated circuits. We will continue to add capacity for military assembly and test, even during those periods when others turn away from the military marketplace in pursuit of what they view to be the more attractive commercial market. We feel that a commitment to the needs of the military/aerospace user community should not be based upon the conditions encountered in the commercial marketplace. We have no plans for other than a continued long-term commitment to military/aerospace component production and screening. And we will not deviate from the highest standards of quality and reliability in our execution of that commitment. There are no shortcuts to semiconductor reliability. It can only be achieved through rigid adherence to established standards.

However, we also acknowledge the quite obvious fact that through refinement and redefinition, standards are subject to change. As those changes occur, we will update our current procedures to reflect the changes that find their way into MIL-M-38510 and MIL-STD-883. We will, where our understanding of semiconductor reliability and screening indicates the need, actively pursue those changes that we feel will allow our industry to provide a better product to the systems manufacturers. We will also steadfastly resist those changes which we feel sacrifice reliability to the less important question of expediency.

*Requirements that were subsequently incorporated into MIL-STD-883

**and MIL-STD-883.

National's Standard Programs

MIL-M-38510 is the key military standardization program for ICs. National is equally committed to the support of the requirements of the space segment of the market for MIL-M-38510 Class S devices. To support these needs we have established dedicated Class S assembly and test facilities. The realization that users could not obtain all the device types they required through these programs led National's Military/Aerospace Products Group to the development of two of the strongest and most compliant in-house programs in the industry. National programs for 883B/RETS and 883S/RETS microcircuits provide the systems manufacturer with an easy mechanism for obtaining those devices not listed on the MIL-M-38510 QPL. In response to other user needs, National also developed a program for radiation hardened devices (both CMOS and linear), a comprehensive program for radiation susceptibility testing for Class S devices, and a program for the production of devices in leadless chip carriers (LCCs).

RETS and Burn-In

One of the primary advantages of MIL-M-38510 is its clear definition and standardization of electrical test and burn-in requirements. One of the major drawbacks seen in the standard reliability screening programs of most semiconductor manufacturers is that electrical testing is invariably performed to some document that is not available to the user. The user has the right to know what he is buying. At National that testing is never vague or undefined. Both in-house programs (883B/RETS and 883S/RETS) are based upon a document called the RETS (an acronym for Reliability Electrical Test Specification. The RETS is a simplified but complete description of the testing performed as part of National's standard Rel electrical test programs, and is controlled by our QA department. The burn-in circuits and electrical test parameters for the MIL-M-38510 Class S and Class B devices produced by National Semiconductor are defined by the applicable detail specification.

Ordering ICs from National

Ordering National Semiconductor High Reliability integrated circuits is very simple. National sales offices and sales representatives can provide price and delivery information on our entire line of JM38510 Class B, JM38510 Class S, 883B/RETS and 883S/RETS microcircuits. A large percentage of these devices are available from inventory at either the factory or at one of our many distributors.

Ordering to Control Specifications

We also acknowledge the fact that many military systems manufacturers must, for contractual purposes, maintain their own specifications for many of the devices that they purchase. We have no objection to the use of contractor prepared procurement specifications, for we have found that the majority of these documents are written in compliance with the requirements of MIL-M-38510. Where this is true, we have found that they are also totally compatible with our in-house standardization programs. Where drawings submitted to National differ from the requirements outlined in MIL-M-38510, we welcome the opportunity to work with our customers to develop specifications which do meet the intent of MIL-M-38510.

Where customer specifications and our 883B/RETS product specifications correspond, we have the ability to expedite delivery by adding the customer part number in addition to the basic 883B/RETS part number. Customers who understand our program and wish to use the program in their parts procurement may order by placing "M/O" after their part number on their purchase order, thus allowing us to mark their part number on our 883B/RETS devices without the lengthy delay normally required for a comprehensive specifications review cycle. We have tried to provide programs that offer the maximum level of flexibility within the constraints of standardization.

Standardization is the key to cost-effective procurement of high reliability semiconductor devices. National Semiconductor Corporation is committed to that standardization.

Military Processing: A Corporate Commitment

The National Semiconductor Military/Aerospace Products Division draws upon the total resources of National Semiconductor. National is one of the world's largest manufacturers of semiconductor products, offering the largest number of product types available from any single source in the industry. This product line is growing faster than that of any other worldwide semiconductor manufacturer. Each new product is carefully evaluated for possible military/aerospace usage potential, and new product designs must comply with the reliability and quality constraints required by that segment of the industry. All new product designs are targeted to full military temperature range operation.

In addition, a dedicated Reliability Engineering Department within the Military/Aerospace Prod-

ucts Division coordinates burn-in circuit design, test tape development, test fixturing, support documentation, and new product release paperwork to ensure the earliest possible introduction of fully compliant 883B/RETS versions of the new products introduced by the company.

We are able to do this well, for National is no newcomer to this business. Founded in Danbury, Connecticut in 1959, National acquired an entire new management team in 1967 and moved corporate headquarters to Santa Clara, California. The new management team focused its attention on the transistor product line, and rapidly made that line profitable. Then the company's talents were turned to the development of linear, digital, and MOS integrated circuits — the fastest-growing segments of the semiconductor marketplace. Finally, an OEM representative and distributor network was established to develop and service a broad customer base, and facilities were added around the world to provide competitive products to worldwide markets.

The Reliability Test Department was initially formed in 1968 and reported at that time to the Director of Quality Assurance. The Rel Department developed the same rapid growth rate that the company as a whole had shown. From a small staff occupying several thousand square feet in Santa Clara, these reliability test operations grew until today they employ over 3000 people worldwide. Well over 200,000 square feet are devoted to the testing and assembly of high reliability products. During 1981, the Military/Aerospace Products Group became the Military/Aerospace Products Division. The company is currently involved in a number of military research and development programs, including a Phase I VHSIC contract.

VHSIC involvement was natural since National's technological leadership has enabled the company to consistently be one of the major suppliers of military/aerospace semiconductors. Having continued to develop a high technology image through the development olf Megarad hardened CMOS and linear device types, and the development of TRI-CODE™ logic, National is now expanding technology frontiers in the areas of memory, microprocessor, and data acquisition products. As a result of all this innovation, National has become the only company in the entire semiconductor industry capable of providing high reliability devices from all of the following product lines:

linear
hybrid
CMOS logic
Megarad CMOS logic
bipolar memory
MOS RAMs
CMOS RAMs
MOS EPROMs
CMOS EPROMs
MOS EEPROMs
data acquisition devices
standard TTL
low power TTL
low power Schottky
standard Schottky
interface devices
bipolar microprocessors
MOS microprocessors
CMOS microprocessors
COPS™ microcontrollers
high-speed CMOS Schottky
advanced low power Schottky
advanced Schottky

National Semiconductor has wafer fabrication plants in Santa Clara, California; Salt Lake City, Utah; Arlington, Texas; and Danbury, Connecticut. Many of these fabrication plants, along with our assembly and test lines in Santa Clara, California and Tucson, Arizona, have been fully certified for the production of Class S and Class B MIL-M-38510 circuits.

To support the requirements of the Class S marketplace, we have our own SEM and radiation testing facilities. Our screening capabilities are backed up by one of the most extensive failure analysis labs in the industry.

National is the leader in the military/aerospace integrated circuit market. We have achieved that leadership by offering an unmatched combination of technology, product breadth, understanding, commitment and capacity.

REFER TO THE RELIABILITY HANDBOOK FOR LIST OF PARTS AVAILABLE

883B/883S/RETS Screening Flows

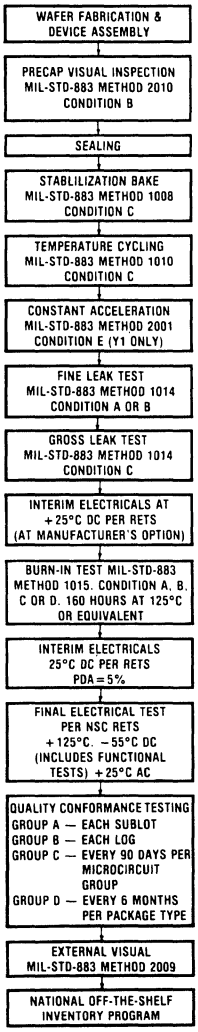
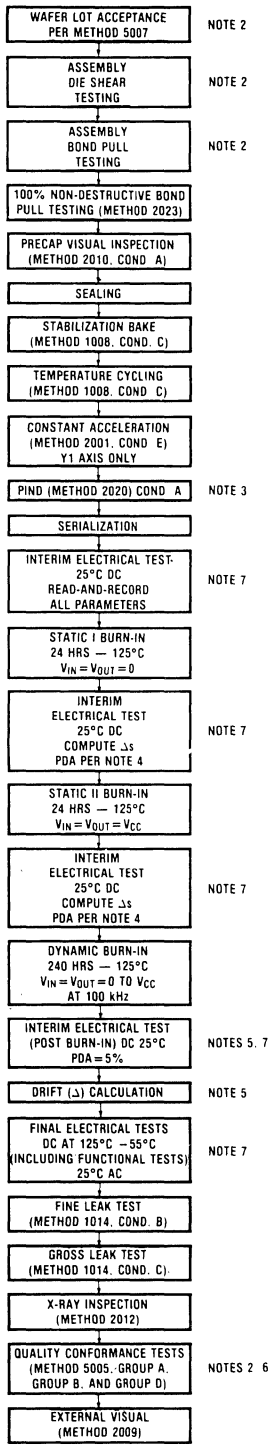


FIGURE 1. National's 883B/RETS Class B Screening Flow



NOTES:
1. ALL METHODS REFERENCED ARE MIL-STD-883 TEST METHODS.
2. THESE TESTS ARE PERFORMED ON A SAMPLE BASIS ALL OTHER TESTS ARE PERFORMED 100%.
3. ACCEPTANCE CRITERIA SHALL BE IN ACCORDANCE WITH MIL-M-38510.
4. THE PDA FOR STATIC I AND STATIC II BURN-IN SHALL BE 5% TOTAL.
5. THE PDA INCLUDES Δ FAILURES.
6. GROUP A AND BOND PULL AND DIE SHEAR TESTING OF GROUP B MAY BE PERFORMED ON-LINE.
7. ALL ELECTRICAL TESTING SHALL BE IN ACCORDANCE WITH THE APPLICABLE RETS OR THE APPLICABLE MIL-S-38510 DETAIL SPECIFICATION.

FIGURE 2. National's 883S/RETS Class S Screening Flow

National Semiconductor Corporation

883/RETS* PROGRAM CERTIFICATE OF CONFORMANCE

TEST	MIL-STD-883 METHOD**	REQUIREMENT
INTERNAL VISUAL	2010 B	100%
STABILIZATION BAKE	1008 C 24 HRS @ +150°C	100%
TEMPERATURE CYCLING	1010 C 10 CYCLES −65°C/+150°C	100%
CONSTANT ACCELERATION	2001 E	100%
FINE LEAK	1014 B 5 x 10^{-8}	100%
GROSS LEAK	1014 C2	100%
BURN-IN	1015 160 HRS @ +125°C	100%
FINAL ELECTRICAL	+25°C DC PER NSC RETS	100%
PDA	10% MAX ALLOWABLE	
	+125°C DC PER NSC RETS	100%
	−55°C DC PER NSC RETS	100%
	+25°C AC PER NSC RETS	100%
QA ACCEPTANCE	LTPD SAMPLE	
EXTERNAL VISUAL	2009	100%

* RETS = REL ELECTRICAL TEST SPECIFICATION
** ALL METHODS TO CURRENT REVISION LEVELS

THIS IS TO CERTIFY THAT ALL 883/RETS MATERIALS SUPPLIED TO YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS, AND DOCUMENTS PERTINENT TO THE NATIONAL 883/RETS PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

Part Number _____

P.O. Number _____

Date Code(s) _____

Lot Code(s) _____

_____

QUALITY ASSURANCE REPRESENTATIVE

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or do not wish to do so, yet need significantly better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quailty are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the precentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

Five Temperature Cycles (70°C to 100°C)

Exercising each device over a 100° temperature range provides an additional die and package stress.

National's A+ Program (Continued)

High Temperature (100°C) Functional Electrical Test

A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-in Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96eV activation energy. All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

National's B+ Program

B+ Program: a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality *and* the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.

Reliability Saves You Money

With the increases population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at least two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair, and rework costs have risen—and promise to continue to rise—but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be—literally—hundreds of times more than the cost of the failed IC itself.

Improving The Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

Quality Improvement

When an IC vendor specifies 100 percent final testing of its parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality *and* the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

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This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test

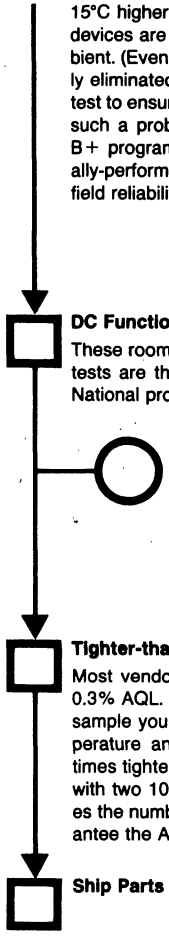
A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–

Five Temperature Cycles (70°C to 100°C)

Exercising each device over a 100° temperature range provides an additional die and package stress.

National's B+ Program (Continued)

15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.)



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Ship Parts

Here are the QC sampling plans used in our B+ test program:

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Parametric, DC		
Mechanical		
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Major	—	0.28%

RELIABILITY REPORT

Reliability
of
Advanced Low Power Schottky (ALS) Devices

Prepared By:

Krishna Singh—Reliability Engineering Section Head

Gary Tietz—Design Engineering Manager

Approved by:

J. Huljev—Reliability Engineering Manager

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RELIABILITY REPORT

ALS CHARACTERISTICS AND PROCESS OVERVIEW

The primary reasons for the popularity of LS logic circuits are:
- —Improved speed-power product
- —Excellent reliability
- —Functional equivalency with older TTL products

The LS family was developed to meet the needs of system designers through the 1970s and 1980s, with regard to reduced propagation delays and power dissipation.

The Advanced Low Power Schottky (ALS) family was designed to meet the needs of the next generation of systems. These systems will require higher performance than is currently available with standard Low Power Schottky.

The ALS family offers the system designer the next generation state-of-the-art digital products. ALS devices operate at one-half the propagation delay and one-half the power of the LS family circuits.

The ALS family is also backed by National's commitment to be an industry leader in quality and reliability, a commitment that National takes very seriously!

The Key Features of the ALS Family Are:

1. Improved propagation delay (50% of LS)
2. Improved power dissipation (50% of LS)
3. Improved input characteristics
   - —PNP inputs for reduced I_{IL} current (Fan-In)
   - —ESD protection
   - —Thresholds typically 1.4 volts
4. Improved line driving capability
5. Reduced supply current spikes

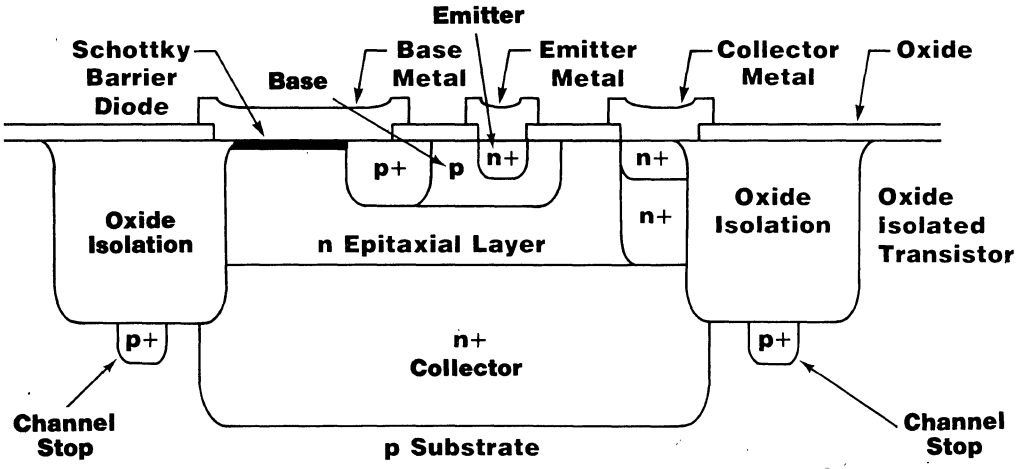
Key Physical Features Are:

1. Oxide isolation
2. Walled emitters
3. 2.5 micron emitter widths
4. Ion implanted
5. 5 GHz Ft transistors

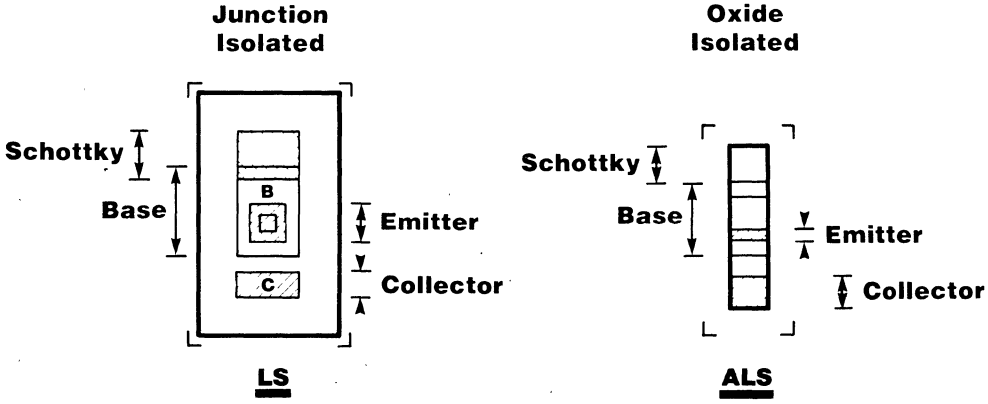
ALS	LS	IMPACT
Oxide isolation	Junction isolation	Reduced capacitance Smaller geometries Improved propagation
Implanted transistor	Diffused transistor	Shallow junctions Improved uniformity Less thermal damage
Composed geometries	Non-composed	Self-alignment
Thin EPI	Thick EPI	Reduced capacitance Improved propagation
Nitride passivation		Improved reliability
A/C Spec Full temperature range Full V_{CC} range 50 pF load	A/C Spec 25 degrees 5.0 volts 15 pF load	
DM74ALS V_{CC} 4.5 to 5.5V	DM74LS V_{CC} 4.75 to 5.25V	

RELIABILITY REPORT

Cross Sectional View of the ALS Process:



Top View:



4.68 mil^2	Device Area	2.03 mil^2
0.67 mil^2	Base Area	0.24 mil^2
0.16 mil^2	Emitter Area	0.03 mil^2

- Reduced geometry
- Walled emitter
- Low capacitance
- Improved speed

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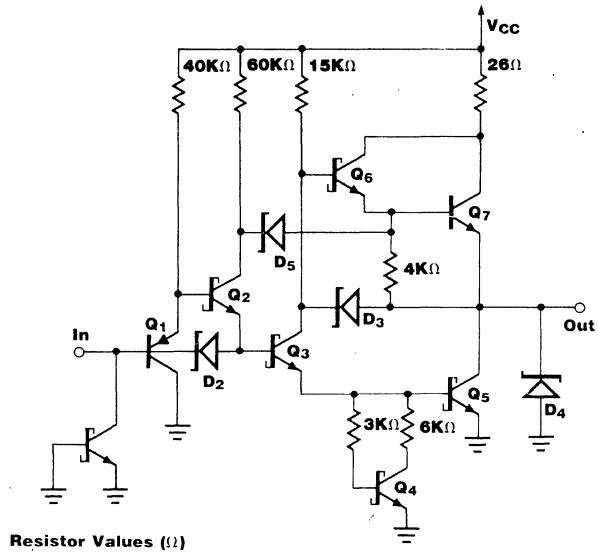
Typical Circuit Schematic:



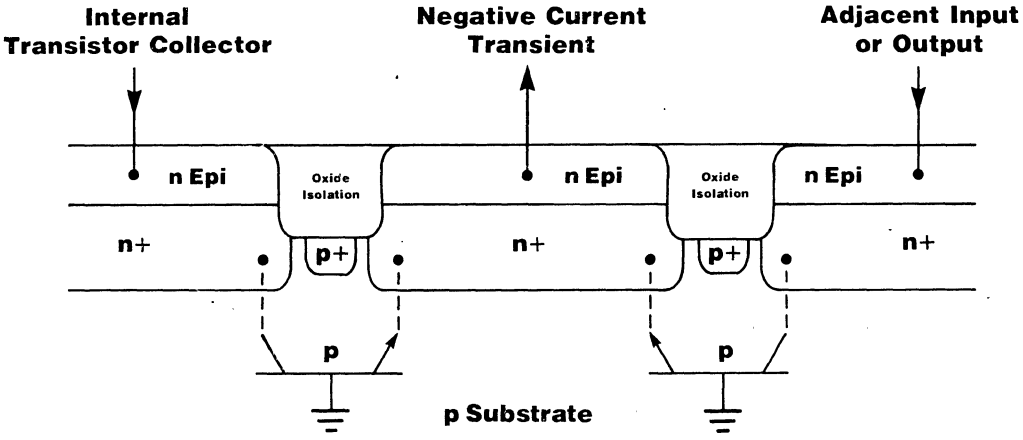
Protection from Negative Transients:

The high transition rates associated with oxide-isolated logic families can generate a -2.5V reflection when terminated into a high impedance.

Schottky clamp diodes are provided on both the input and outputs of all devices to limit such reflection. Clamp diodes may have to handle peak currents of 30 to 60 mA. Substrate junctions will become forward biased at these currents.

If substrate junction becomes forward biased, it is possible to produce parasitic transistor action which can cause functional or parametric problems during the time span of the reflection.

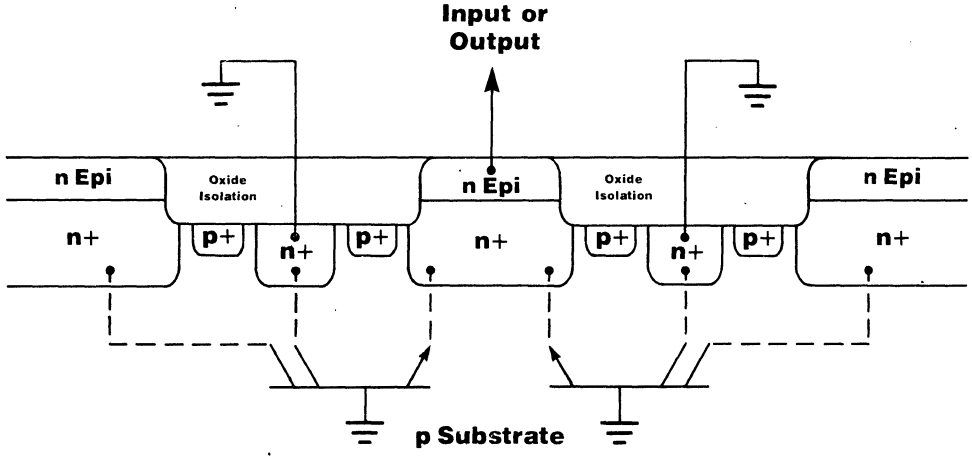
Parasitic Failure Modes:



Parastic transistor to adjacent input can cause input leakage far in excess of I_{IH} spec.

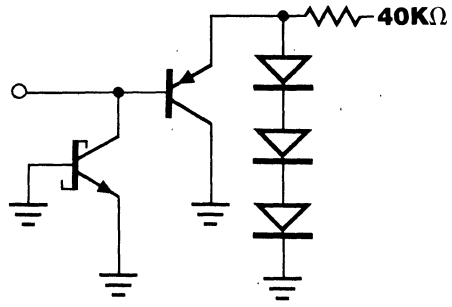
Parasitic transistor to internal collector can cause outputs to change state and flip-flops to change state.

Transient Protection:



In the case of ALS devices, transient protection is provided by a grounded buried n^+ ring on all input and output epi islands.

Improved Input Characteristics:

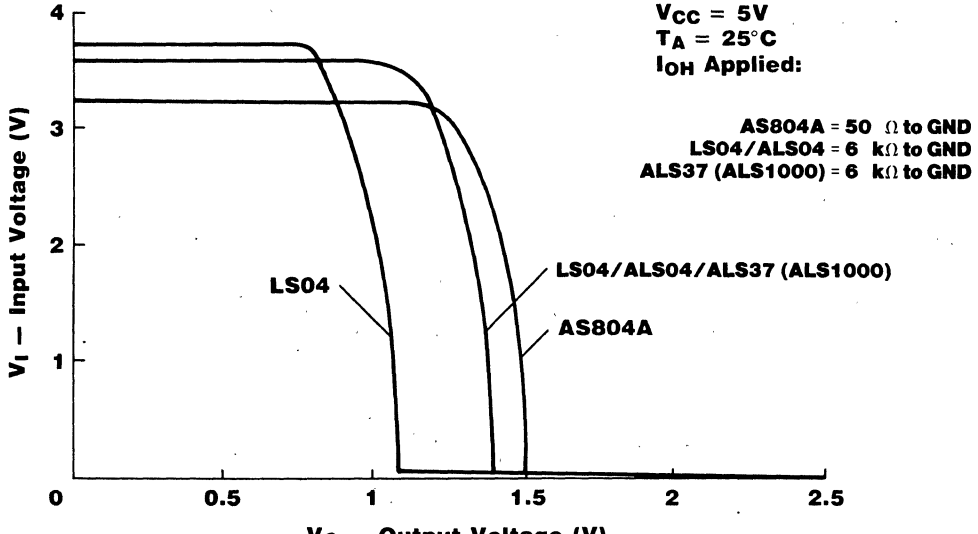


ALS

Equivalent Input Circuit

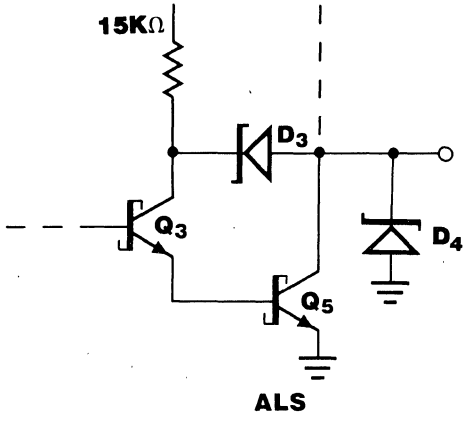
- PNP inputs for reduced input current typical I_{IL} of -10 μA
- Two diode equivalent input threshold typically 1.4V
- ESD protection

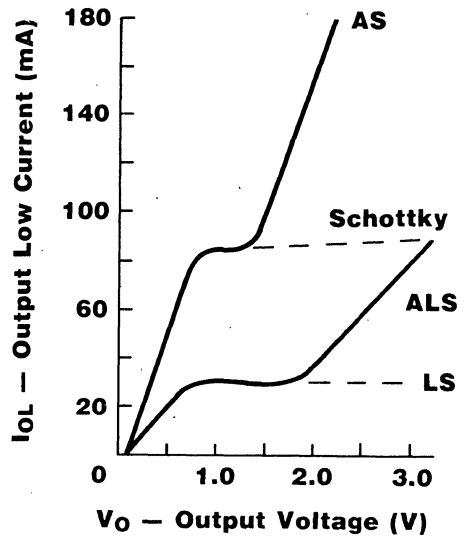
Improved Input Threshold:



Transfer Function (Room Temperature)

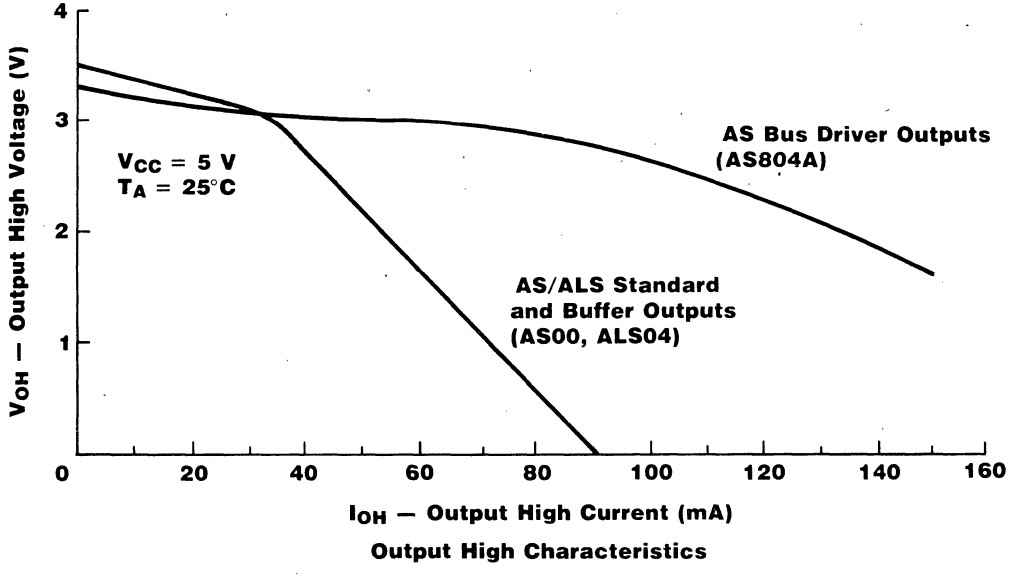
Improved Lower Output Characteristic:





Feedback Diode D_3 provides additional base drive for output transistor

Darlington Upper Output Characteristic:



Output High Characteristics

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RELIABILITY REPORT

Reliability Test Results:

Accelerated operating life testing at elevated temperatures is a principal method of simulating long-term operation within a short period of time. This method is particularly useful because it provides a means of accelerating time-to-failure of temperature-sensitive failure mechanisms. As a result, data is gathered for failure rate predictions at any operating field ambient.

The following tests have been conducted at an ambient temperature (T_A) of 150°C with devices biased at a maximum voltage of 5.5 volts. Complete functional and parametric testing to data sheet specifications was performed at reported data points.

TABLE I.

150°C High Temperature Bias Reliability Test Results

DEVICE	NO. LEADS	DATE CODE	RESULTS 168 Hours	500 Hours	1000 Hours	REL. LOT NO.
DM74ALS00N	14	8228	0/83	0/83	0/83	22128
DM74ALS04N	14	8235	0/90	0/90	0/90	22188
DM74ALS373N	20	8237	0/100	0/100	0/100	22192
DM74ALS137N	16	8239	0/90	0/90	0/90	22214
		Total:	0/363	0/363	0/363	

Total device hours at 150°C: 363,000; Actual Failure Rate = 0/363,000 device hours.

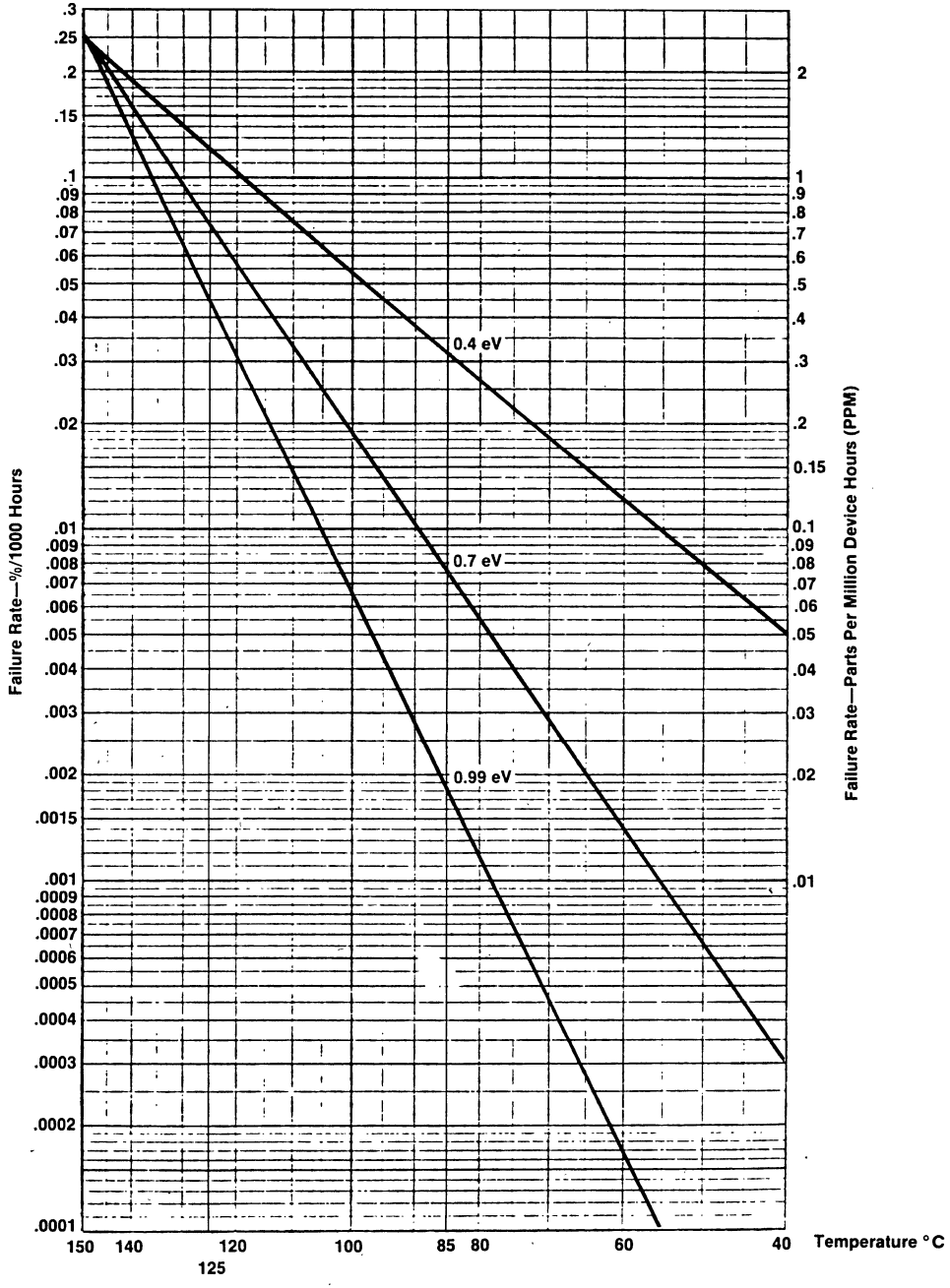
Table 2 shows failure rates calculated with 60% confidence at stress, and at two different temperatures and activation engeries.

TABLE II.

DEVICE HOURS	ACTUAL NO. OF REJECTS	FAILURE RATE AT STRESS, 150°C %/1k HRS.	PPM	ACTIVATION ENERGY, eV	CALCULATED FAILURE RATE AT 125°C %/1k HRS.	PPM	85°C %/1k HRS.	PPM
363,000	0	0.25	2.5	0.4	0.126	1.26	0.034	0.34
363,000	0	0.25	2.5	0.99	0.045	0.45	0.0018	0.018

The above data can be further extrapolated to lower temperatures at different activation energies, as illustrated in the graph on the following page showing failure rate in %/1000 Hrs. and PPM units.

RELIABILITY REPORT



At 60% confidence limit, using three different activation energies, above is the failure rate in % per 1000 Hours and also in PPM.

8

RELIABILITY REPORT

Temperature Humidity Bias Test

The Temperature and Humidity test involves stress levels considerably in excess of the field-use levels encountered by a device. The test is intended to trigger moisture-related failure mechanisms occurring over a period of months or years in the field.

These tests have been conducted at an ambient temperature (T_A) of 85° C and a relative humidity of 85%. Complete functional and parametric testing to data sheet specifications is performed at reported data points.

TABLE III.

85° C/85% RH Temperature Humidity Bias Test Results

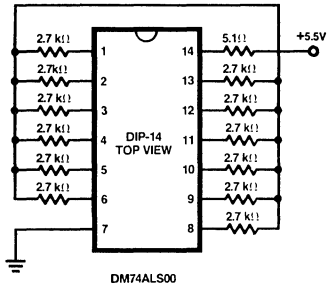
DEVICE	NO. LEADS	DATE CODE	RESULTS 168 Hours	500 Hours	1000 Hours	REL. LOT NO.
DM74ALS00N	14	8228	0/100	0/100	0/100	22128
DM74ALS04N	14	8235	0/100	0/100	0/100	22188
DM74ALS373N	20	8237	0/66	0/66	0/66	22192
DM74ALS137N	16	8239	0/200	0/200	0/200	22214
		Total:	0/466	0/466	0/466	

Actual Failure Rate = 0/466,000 device hours.

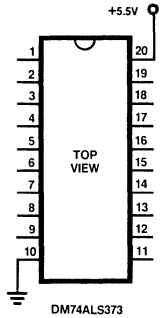
Conclusion

Reliability performance of ALS products in Epoxy B molded packages on accelerated reliability tests is excellent and will insure field reliability performance under the most adverse applications.

High Temperature Bias Test Burn-In Circuits:

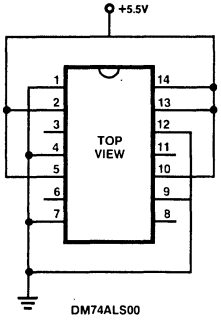


DM74ALS00
DM74ALS04
DM74ALS137

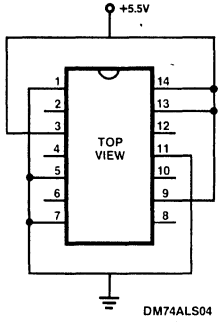


DM74ALS373

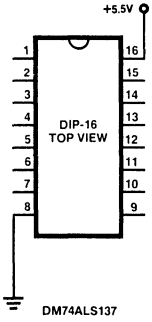
Temperature Humidity Bias Test Burn-in Circuits:



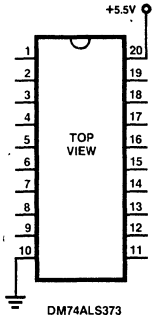
DM74ALS00



DM74ALS04



DM74ALS137



DM74ALS373

8

Thermal Ratings for IC's

MAXIMUM POWER DISSIPATION

To insure reliable long term operation of its Integrated Circuits, National Semiconductor has specified maximum junction temperature (T_j) limits. These limits are at 150°C for circuits packaged in a molded dual-in-line package (Epoxy B), and 175°C for all other package types.

Maximum power dissipation (P_D) of an integrated circuit is limited by maximum allowable junction temperature of the silicon die, and thermal resistance (θ_{J-X}) of the package. *Figure 1* illustrates the relationship between power dissipation and junction temperature.

The line indicating "Maximum Power Rating of Package" is projected from the maximum junction temperature limit (150°C in this example) at a slope corresponding to the package thermal resistance ($1/\theta_{J-X}$). Below this line is the safe operating area of the device. Additional constraint are Maximum Power Dissipation and Maximum Operatin Temperature (T_A). These parameters may be determine from device data sheets. For this example, $P_{D(MAX)}$ = 30 mW and $T_{A(MAX)}$ = 70 °C.

Point "A" in *Figure 1* is an operating point corresponding t T_A = 50°C and P_D = 100 mW. Determine device junctio temperature by projecting a line from point "A", parallel t the Maximum Power Rating curve, until it intersects th horizontal axis. T_j is determined from the point of intersec tion with the horizontal axis. For this example, T_j is 45°C.

THERMAL INFORMATION

Figure 2 illustrates thermal resistance characteristics fo Integrated Circuit packages.

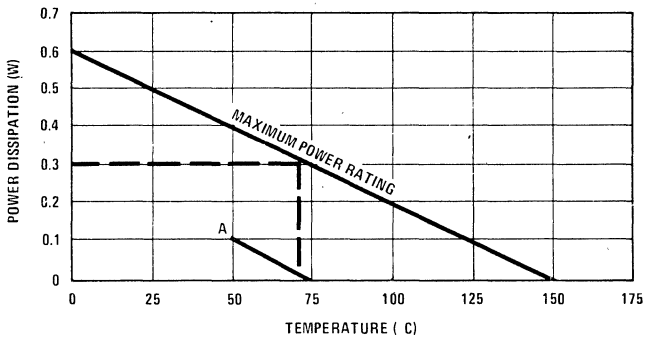


FIGURE 1. Power Dissipation vs Temperature

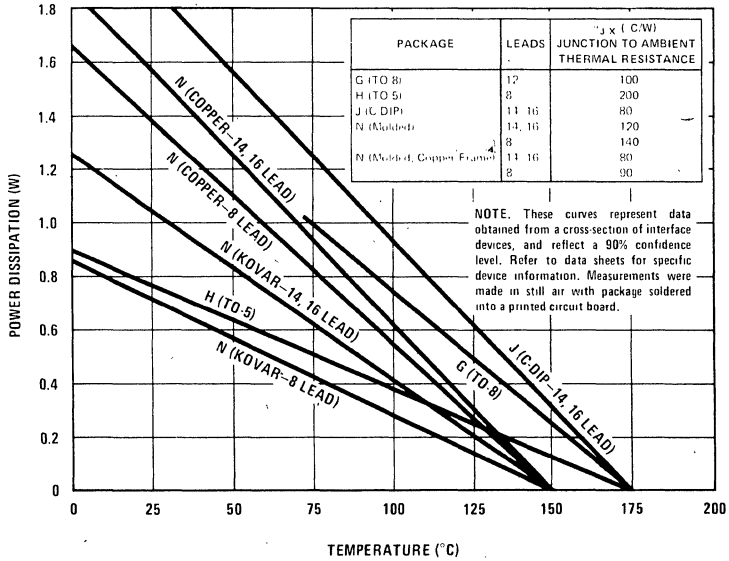
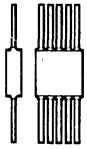
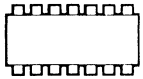
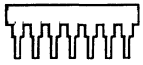
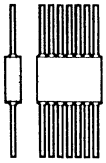


FIGURE 2. Maximum θ_{J-X} Values for IC Packages

ıdustry Package Cross Reference Guide

	NSC (DM) (1)	Signetics (N)	Fairchild —	Motorola (SN)	TI (SN)	AMD (AM)
 Glass/Metal Flat-Pack	F	Q	F	F	F, S	F
 14 and 16-Lead Low-Temperature Ceramic DIP	J	F	R, D	U	J	
 14 and 16-Lead Plastic DIP	N	V, B	T, P	P	P, N	PC
 Low Temperature Glass Hermetic Flat Pack	W		F	F	W	FM

Note 1: Denotes common suffix for logic products.

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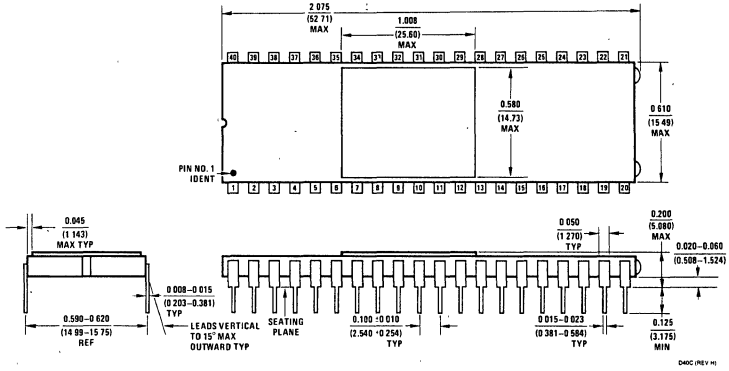
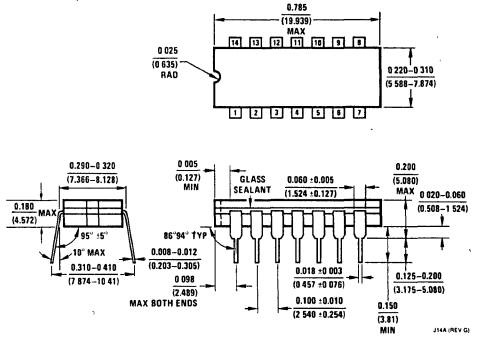
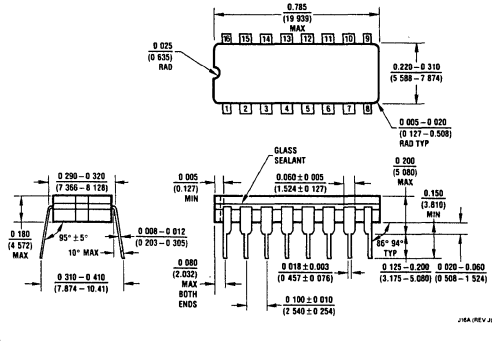
all dimensions are in inches (millimeters)



40-Lead Hermetic DIP (D)
NS Package Number D40C



14-Lead CERDIP (J)
NS Package Number J14A



16-Lead CERDIP (J)
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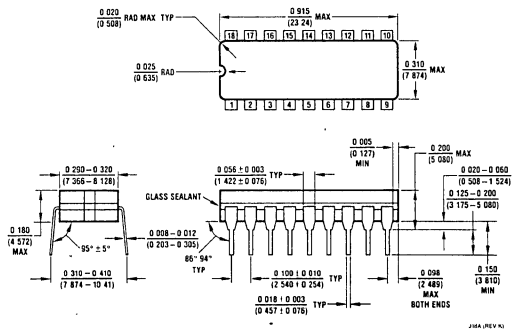
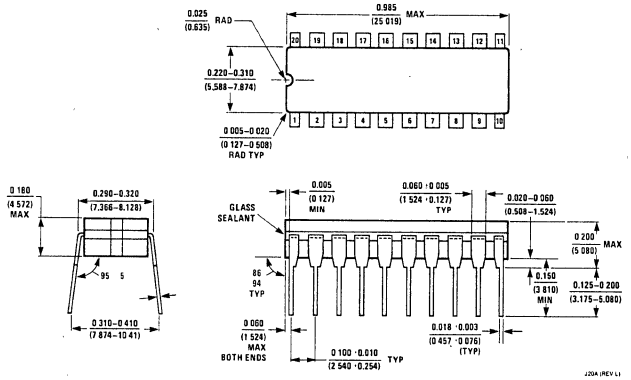


18-Lead CERDIP (J)
NS Package Number J18A



20-Lead CERDIP (J)
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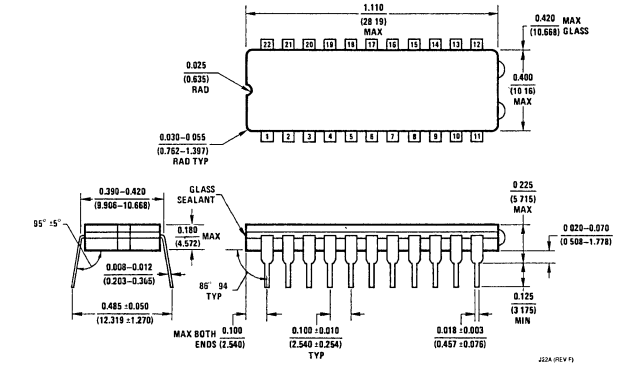
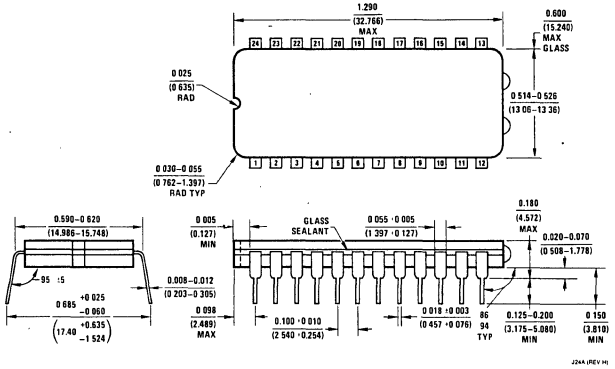
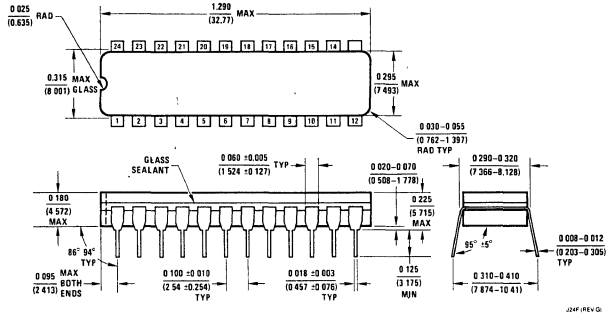


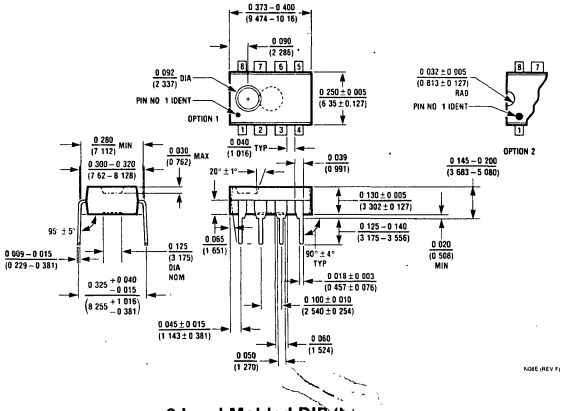
22-Lead CERDIP (J)
NS Package Number J22A



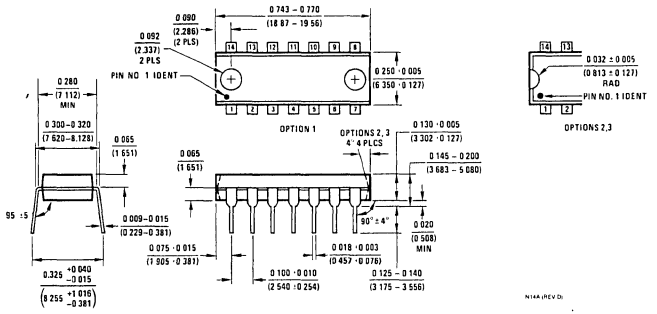
24-Lead CERDIP (J)
NS Package Number J24A



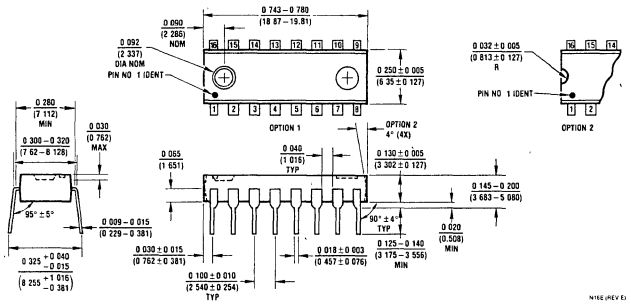
24-Lead CERDIP (J)
0.300 Centers
NS Package Number J24F



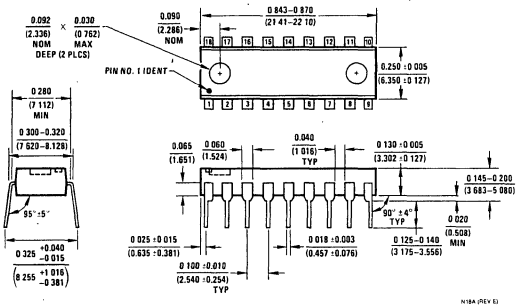
8-Lead Molded DIP (N)
NS Package Number N08E



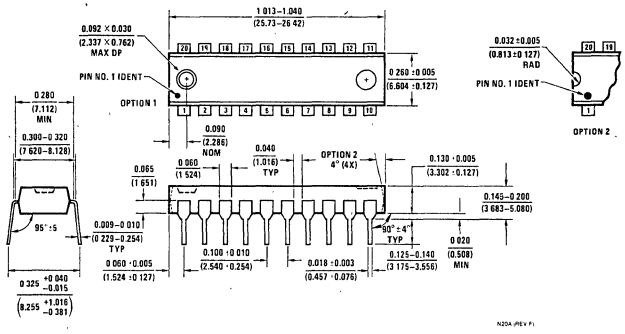
14-Lead Molded DIP (N)
NS Package Number N14A



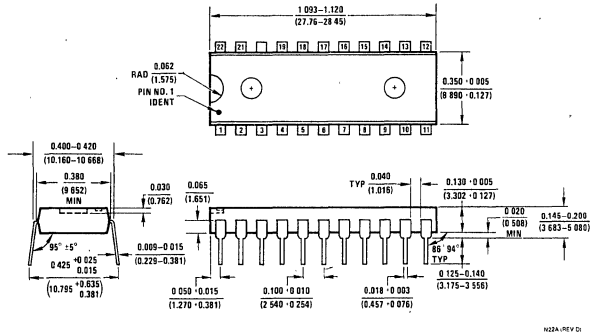
16-Lead Molded DIP (N)
NS Package Number N16E



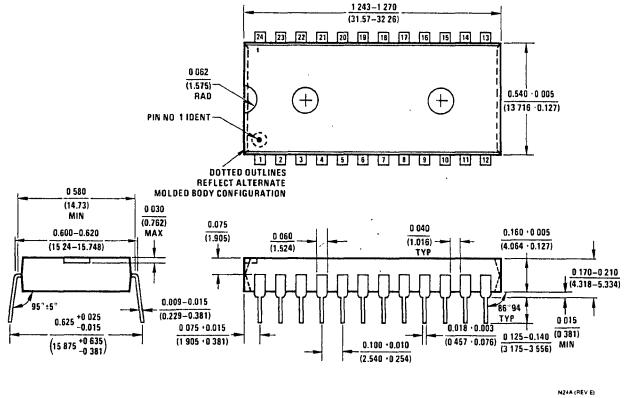
18-Lead Molded DIP (N)
NS Package Number N18A



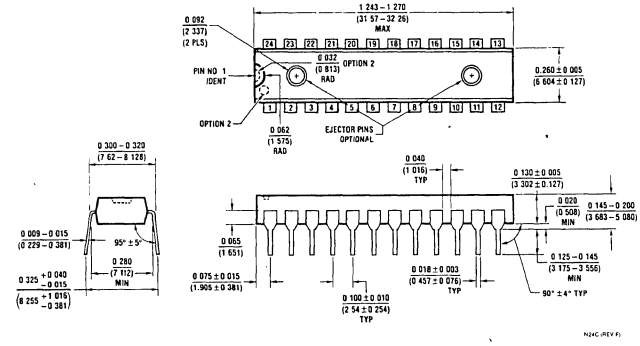
20-Lead Molded DIP (N)
NS Package Number N20A



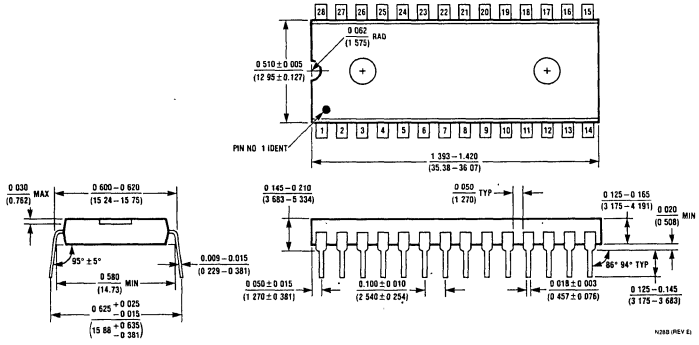
22-Lead Molded DIP (N)
NS Package Number N22A



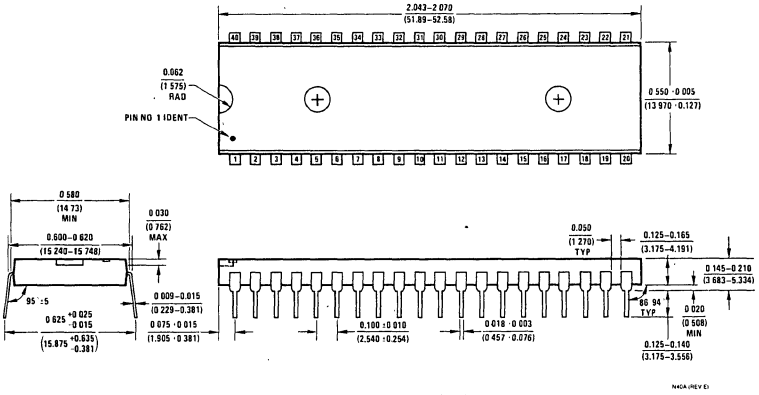
24-Lead Molded DIP (N)
NS Package Number N24A



24-Lead Skinny DIP (SD)
0.300 Centers Molded DIP (N)
NS Package Number N24C

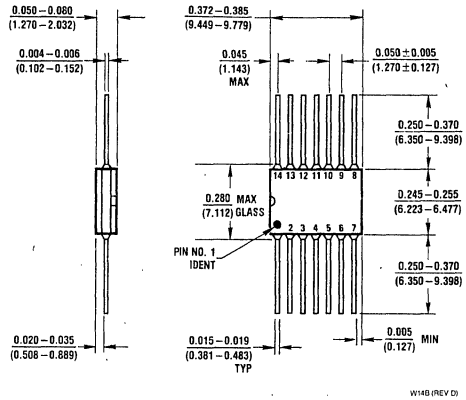


28-Lead Molded DIP (N)
NS Package Number N28B



40-Lead Molded DIP (N)
NS Package Number N40A

8



14-Lead CERPAC (W)
NS Package Number W14B

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 TL/F/5534 IM-RRD150M124/Printed in U.S.A.