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APPS:™ Handbook 2

Memory Support

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MEMORY SUPPORT

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Introduction

Advanced Peripheral Processing Solutions APPS™

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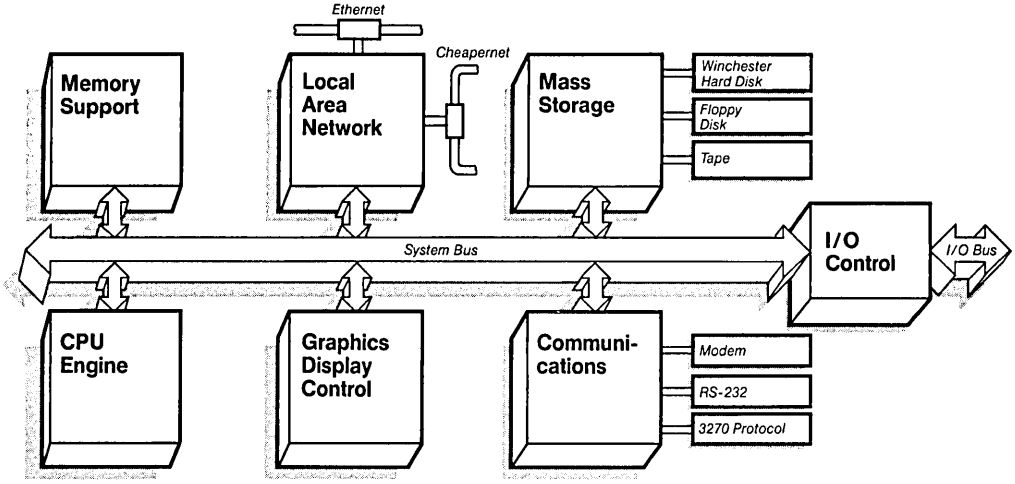

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Among the APPS books are the following titles:

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The National Semiconductor family of mass storage interface products offers the industry's highest performance and broadest range of products for Winchester hard disks and floppy disks. The Mass Storage Handbook includes complete product information and datasheets as well as a comprehensive design guide for disk controller systems.

MEMORY SUPPORT

Today's large Dynamic Random Access Memory (DRAM) arrays require sophisticated high performance devices to provide timing and control. National Semiconductor offers the broadest range of DRAM controllers with the highest performance available on the market. Controllers are available for DRAMs from 64k bit through 1M bit devices, supporting memory arrays up to 8 Mbyte in size. For critical applications, National Semiconductor has developed several Error Checking and Correction (ECC) devices to provide maximum data integrity. The Memory Support Handbook contains complete product information and several application notes detailing complete memory system design.

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Sophisticated human interface is a mark of the newest computer systems designs. Today's personal computer may have better graphics display capability than engineering workstations of a few years ago. National Semiconductor has developed a new family of Advanced Graphics products to provide extremely high performance, high resolution color graphics displays. The graphics chip set is designed to provide the highest level of performance with minimum demands and loading on the system CPU. The graphics system may be expanded to any number of color planes with virtually unlimited resolution. The Graphics Databook lays it all out and makes the display system design easy.

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The DP8400 Family of Memory Interface Circuits

National Semiconductor
Application Note 302
Charles Carinalli
Mike Evans

INTRODUCTION

The rapid development in dynamic random access memory (DRAM) chip storage capability, coupled with significant component cost reductions, has allowed designers to build large memory arrays with high performance specifications. However, the development of memory arrays continues to have a common set of problems generated by the complex timing and refresh requirements of DRAMs. These include: how to quickly drive the memories to take advantage of their speed, minimization of board space required by the support circuitry and the need for error detection and correction. Unfortunately, these problems must be addressed with each new system design. Full system solutions will vary greatly, depending on the DRAM array size, memory speed, and the processor.

This application note introduces a complete family of DRAM support circuits that provides a straightforward solution to the above problems while allowing a high degree of flexibility in application with little or no performance penalty. The DP8400 family (Table I) includes DRAM controllers, error detection/correction circuits, octal address buffers and system control circuits. The LSI blocks are designed with flexible interfaces, making application possible with all existing DRAMs including the recently announced 1 Mbit devices. Additionally, interface is easy to all popular microprocessors with memory word widths possible from 8 to 80 bits.

TABLE I. DP8400 Family Members

DP8400-2, DP8402A	16 and 32 Bit Error Checker/Correctors
DP8408A, DP8409A, DP8417, DP8418, DP8419, DP8428, DP8429	DRAM Controller/Drivers
DP8420, DP84244	DRAM Buffer Drivers
DP84XX2	Microprocessor Interface Circuits

FULL FUNCTION DRAM CONTROLLER

The heart of any DRAM array design is the controller function. Previous LSI controllers supplied a minimum function of address multiplexing with an on-board refresh counter. This required external delay line timing and logic to control memory access, additional logic to perform memory refresh, and external drivers to drive the capacitive memory array. The complete solution results in significant access delay in relation to DRAM speeds and skews in output sequencing, as well as a large component count.

A previous LSI solution brought much of this logic on-chip. However, it is limited in application to certain microprocessors and has the disadvantage of all access timing originating from an external clock, whose phase uncertainty generates a delay in actually knowing when an access has started.

The DP8409A multi-mode dynamic RAM controller/driver was the first controller to resolve all of these problems. This Schottky bipolar device provides the flexibility of external access control, along with automatic access timing generation, without the need for an external timing generator clock. In addition, on-board capacitive drivers allow direct drive for over 88 DRAMs. With the simple addition of refresh clocks, the circuit can perform hidden refresh automatically. It is the DP8409A design that has been used as the spring board for a whole family of controllers with faster speed performance while maintaining maximum pin upgrade compatibility.

All Control On-Chip

Figure 1 is a block diagram of the DP8409A. the ADS input strobes the parallel memory address into the row latches R0–8, the column latches C0–8, and bank select B0 and B1. The nine output drivers may be multiplexed between the row or column input latches, or the 9-bit on-chip refresh counter. One of four $\overline{RAS}$ outputs is selected during an access cycle by setting the bank select inputs B0 or B1. All four $\overline{RAS}$ outputs are active during refresh. Either external or automatic control is available on-chip for the $\overline{CAS}$ output, while an on-chip buffer is provided to minimize skew associated with $\overline{WE}$ output generation.

All DRAM address and control outputs on the DP8409A can directly drive in excess of 500 pF, or the equivalent of 88 DRAMs (4 banks of 22 DRAMs). All output drivers are closely matched, significantly reducing output skew. Each output stage has symmetrical high and low logic level drive capability, insuring matched rise and fall time characteristics.

Flexibility and Upgradability to 256k or 1 Mbit DRAMs

The 9 multiplexed address outputs and 9-bit internal refresh counter of the DP8409A direct addressing capability for 256k DRAMs. Careful design of memory boards, using 64k DRAMs with the DP8409A, insures direct upgradability to 256k DRAMs. This can be done by simply allowing for board address extension by two bits and designing the ninth address trace (Q8) of the DP8409A to connect to pin 1 of the DRAMs (A8). This is, in general, a non-connected pin in 64ks and the ninth address in 256ks. All that need be done is to remove the 64ks and replace them with 256ks, thereby increasing the memory on the same board by a 4 to 1 ratio. The resulting development cost saving can be significant.

Although the new 1 Mbit DRAMs require the larger 18 pin package, which will require a memory board redesign, upgrading the controller portion of the board may need no redesign when converting from the DP8409A or DP8419 to the new DP8429 1 Mbit DRAM controller driver.

Three mode pins (M0, M1 and M2) offer externally selectable modes of operation, a key reason for the DP8409A's application flexibility (Table II). The operational modes are divided between external and automatic memory control.

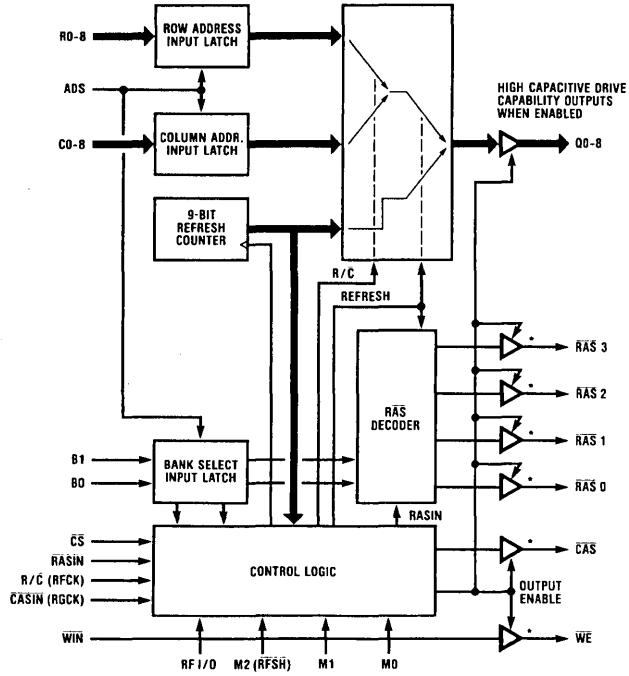

FIGURE 1. DP8409A Block Diagram

TABLE II. DP8409A Mode Select Options

Mode	($\overline{RFSH}$) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto Refresh—Forced	RF I/O = Refresh Request ($\overline{RFRQ}$)
2	0	1	0	Internal Auto Burst Refresh	RF I/O = $\overline{EOC}$
3a	0	1	1	All $\overline{RAS}$ Auto Write	RF I/O = $\overline{EOC}$
3b	0	1	1	Externally Controlled All $\overline{RAS}$ Access	All $\overline{RAS}$ Active
4	1	0	0	Externally Controlled Access	
5	1	0	1	Auto Access, Slow t_{RAH}, Hidden Refresh	
6	1	1	0	Auto Access, Fast t_{RAH}	
7	1	1	1	Set End of Count	

Modes 0, 3b, and 4 provide full control of access and refresh for systems with external memory controllers or for special purpose applications. Here all timing can be directly controlled by the external system as shown in *Figure 2*.

Modes 1, 5 and 6 provide on-chip automatic access sequencing with hidden refresh capability. A graphic example of the automatic access modes of the DP8409A is shown in *Figure 3*. All DRAM access timing and control is generated from one input strobe, $\overline{RASIN}$; no external clock is required. On-chip delays insure proper address and control sequencing once the valid parallel address is presented to the fall-through input latches of the DP8409A. When the $\overline{RASIN}$ transitions high-to-low, the decoded $\overline{RAS}$ output transitions low, strobing the row address into the DRAM array. An on-chip delay automatically generates a guaranteed selectable (mode 5 or 6) row address hold time. At this point, the DP8409A switches the address outputs from the row latch to the column latch. Then another on-chip delay generates a guaranteed column address set-up time before $\overline{CAS}$, so that the $\overline{CAS}$ output automatically strobes the column address into the DRAM array. Read or write cycles are controlled by the system through independent control of the $\overline{WE}$ buffer that is provided on-chip to minimize delay skewing. The automatic access mode makes the dynamic RAM appear static with respect to access timing. In this mode, only one signal, $\overline{RASIN}$, is needed after valid parallel addresses are presented to the DP8409A to initiate proper access sequencing. Access timing ($\overline{RASIN}$ to $\overline{CAS}$), with full output loading of 88 DRAMs in the auto access mode, is determined by the dash number given on the DP8409A data sheet. All performance characteristics are specified over the full operating temperature and supply ranges.

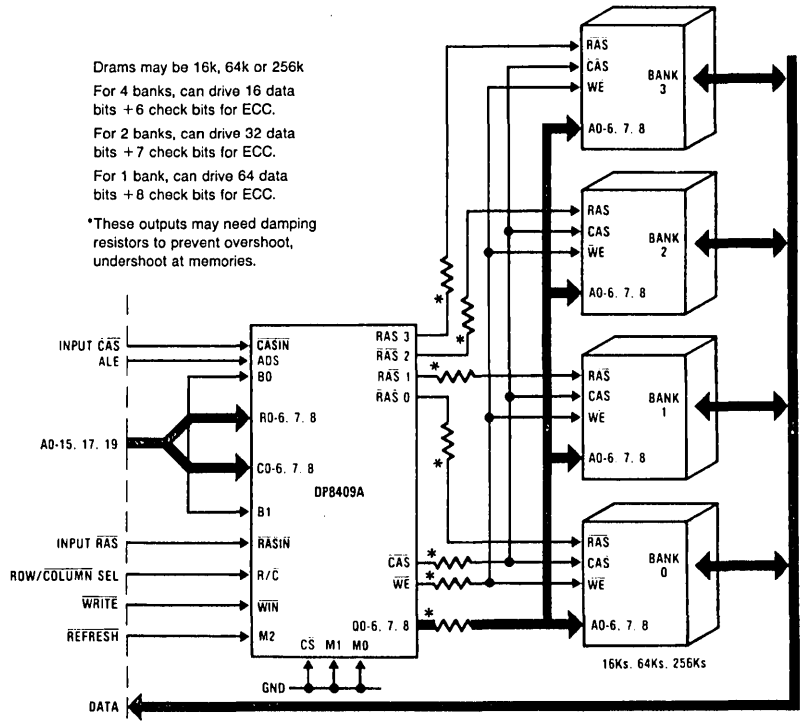

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FIGURE 2. Typical Application of DP8409A Using External Control and Refresh in Modes 0 and 4

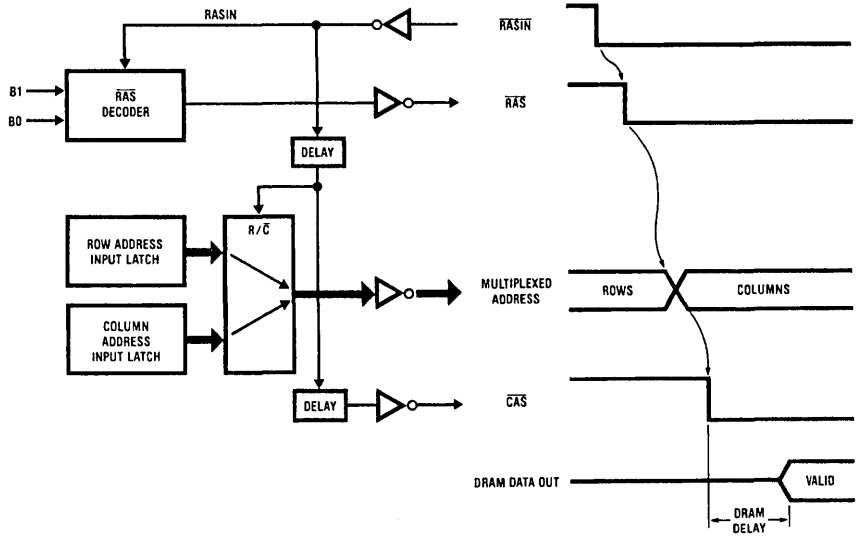

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FIGURE 3. This figure demonstrates the automatic accessing capability of the DP8409A. Only one strobing edge, RASIN, is required for generation of all DRAM access timing signals. This is accomplished with on-chip delay generators, eliminating the need for external delay lines. No access timing clock is necessary.

Refreshing

The DP8409A also provdes hidden refresh capability while in one of the automatic access modes (*Figure 4*). In this mode, it will automatically perform a refresh without the system being interrupted. To do this, the DP8409A requires two clock signals, refresh clock (RFCK) which defines the refresh period (usually 16 μs), and $\overline{RAS}$ generator clock (RGCK), which is typically the microprocessor clock.

Highest priority is given to hidden refreshing through use of level sensing of RFCK. A refresh cycle begins when RFCK transitions to a high level. If during the time RFCK is high the DP8409A is deselected ($\overline{CS}$ in the high state) and the processor is accessing another portion of the system such as another memory segment, or ROM, or a peripheral, then a hidden refresh is performed. When a read or write cycle is initiated by the processor, the $\overline{RASIN}$ input on the DP8409A transitions low. With $\overline{CS}$ high, this causes the present state of the internal refresh counter to be placed on the address outputs, followed by the four $\overline{RAS}$ outputs transitioning low, strobing the refresh address into the DRAM array. When the cycle ends, $\overline{RASIN}$ will terminate, thus forcing the $\overline{RAS}$ outputs back to their inactive state and ending the hidden refresh. The refresh counter is then incremented and another microprocssor cycle can begin immediately. However, to save power, the DP8409A will allow only one hidden refresh to occur during a given RFCK cycle.

In the event that a hidden refresh does not occur, the DP8409A must force a refresh before the RFCK's next positive-going transition. The system is notified after the negative-going RFCK transition that a hidden refresh has not occurred, via the refresh request output (RF I/O pin). The system acknowledges the request for a forced refresh by setting M2 (refresh) low on the DP8409A and preventing further access to the DP8409A. The DP8409A then uses RGCK to generate an automatic forced refresh. The refresh request pin then returns to the inactive state, and the DP8409A allows the processor to take full system control after the forced refresh has been completed.

OCTAL MEMORY DRIVERS

For those applications where the memory array is extremely large or the controller design is unique to a particular application requirement, specialized high capacitive load address and control buffers are required. However, like any other element in a DRAM system, selection of the improper driver can have significant impact on system performance.

In the past, this function has been performed using Schottky logic family circuits such as the DM74S240 octal inverter or the DM74S244 octal buffer. The output stages of these devices have good drive capability, but their performance with heavy capacitive loads is not ideal for DRAM arrays. The key disadvantage of these devices is their non-symmetrical rise and fall time characteristics and their long propagation delays with heavy load capacitance. The former is a result of impedance mismatch in the upper and lower output stages. The latter stems from process capability and circuit design techniques not tailored to the DRAM application. The combined result of all these factors is increased output skew in address and control lines when these devices are used as buffers.

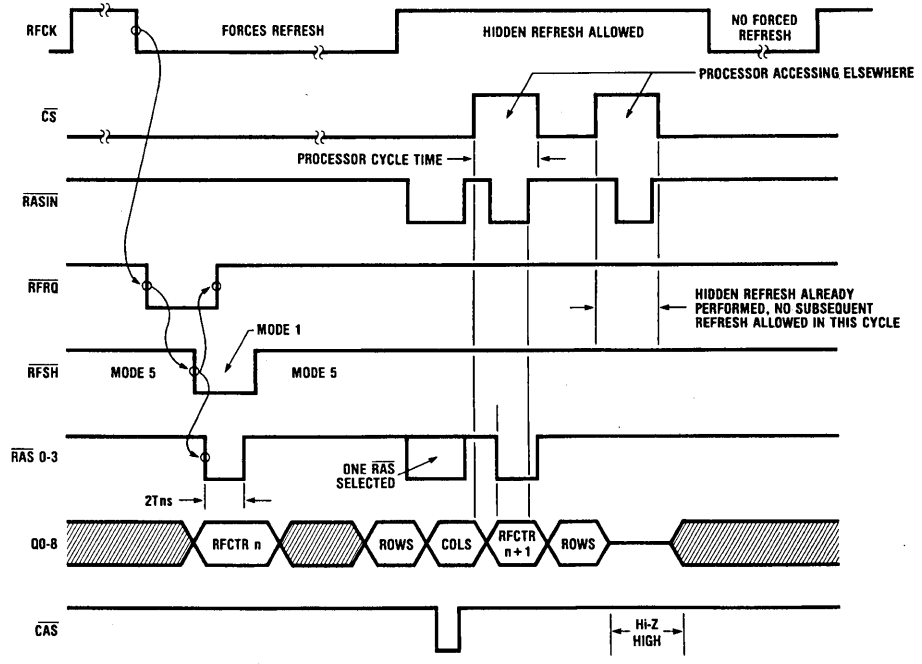

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FIGURE 4. Hidden and Forced Refresh Timing of the DP8409A

Two new devices are now available for this application. The DP84240 is pin and function compatible with the DM74S240. The DP84244 is likewise compatible with the DM74S244. However, this is where the similarity between the devices ends. Both the DP84240 and the DP84244 have been designed specifically to drive DRAM arrays. *Figure 5* shows a typical application of the DP84244, used in conjunction with the DP8409A, to drive a very large memory array.

Figures 6a, 6b show some typical performance curves for these circuits. Note that, at over 500 pF, the propagation delay through these drivers is on the order of 15 ns. This delay includes propagation delay and rise or fall time. Even with this high speed, chip power dissipation is still maintained at a reasonable level as demonstrated by the graphs shown in *Figures 7a, 7b* of power versus frequency.

The DP84240 and the DP84244 are fabricated on a high performance oxide-isolated Schottky bipolar process. Special circuit techiques have been used to minimize internal delays and skews. Additionally, both rise and fall time characteristics track closely as a function of load capacitance. This has been accomplished through impedance matching of the upper and lower output stages. The result of these characteristics is a substantial reduction of skew in both the address and control lines to the DRAM array.

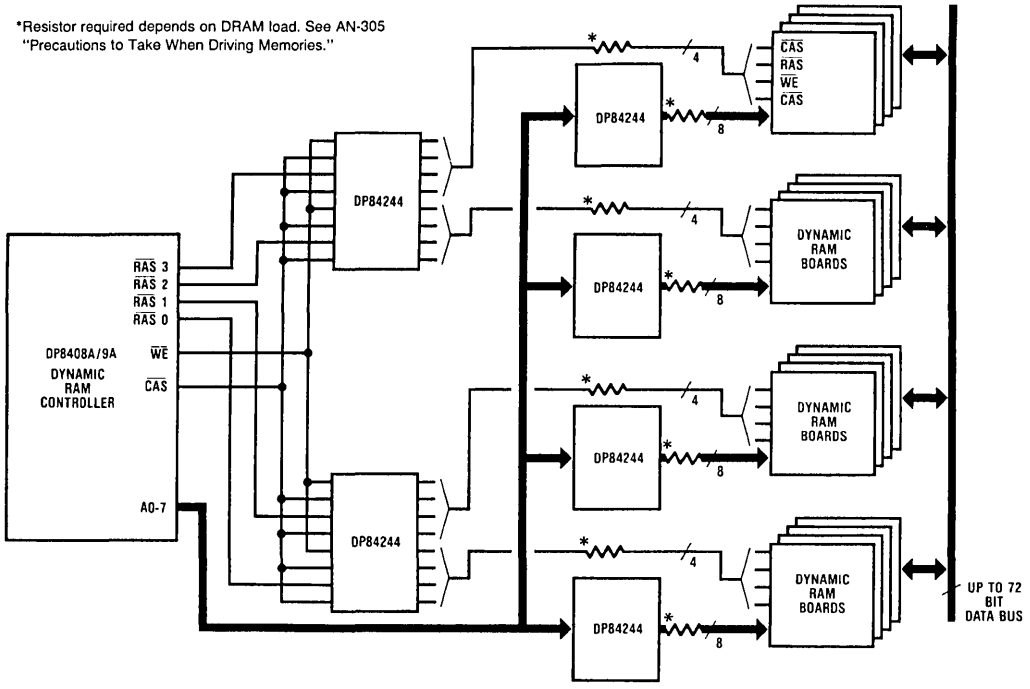

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FIGURE 5. The DP84244 Used as a Buffer in a Large Memory Array (greater than 88 DRAMs) Controlled by the DP8409A

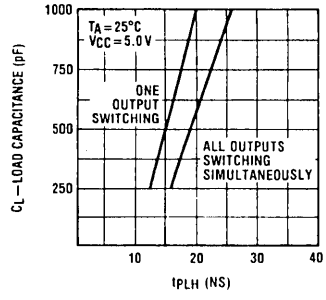

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FIGURE 6a. t_{PLH} Measured to 2.7V on Output vs. C_L

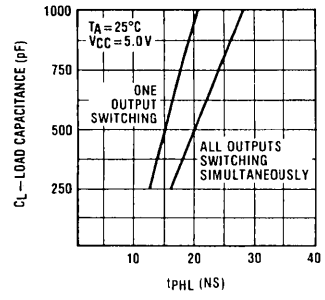

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FIGURE 6b. t_{PHL} Measured to 0.8V on Output vs. C_L

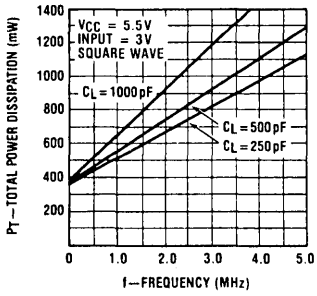

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FIGURE 7a. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

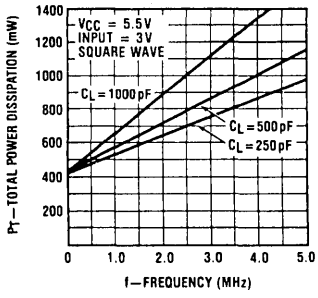

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FIGURE 7b. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

The output stages of the DP84240 and the DP84244, although well matched, are relatively low impedance. Output impedance is under 10Ω. Some DRAM arrays will require the addition of damping resistors in series with the outputs of the drivers. These damping resistors are used to minimize undershoot which may have a harmful effect on the DRAMs if allowed to become large. This undershoot is caused by the high transient currents from the drivers necessary to drive the capacitive loads. These high currents pass through a distributed inductive/capacitive circuit created by the board traces and the DRAM load, causing the undershoot.

The damping resistor has specifically not been placed on-chip because its value is dependent on the DRAM array size and board layout. In fact, address lines will quite often require a different resistor value from the DRAM control lines. The resistor must be tuned for a particular board layout since too high a resistor will produce an excessively slow edge and too low a resistor will not remove the udershoot. Values for damping resistors may vary from 15Ω to 150Ω, depending on the application. Placing any value of damping resistor on-chip, other than a value less than the minimum, severely restricts the application of these high performance circuits.

Another key advantage of both the DP84240 and the DP84244 is their low input capacitance. Previous address buffer/drivers (such as the DM74S240/244) have high input capacitance. Fast edges at the inputs of these drivers become slower and distorted due to this dynamic input capacitance. This problem must be factored as an additional delay through these drivers—a delay not shown by the data sheet specifications. Additionally, the problem becomes increasingly severe as multiple driver inputs are used in parallel for bus expansion applications.

Both the DP84240 and the DP84244 are designed to significantly reduce both static and dynamic input capacitance. When these devices are driven with standard logic circuits, no appreciable overhead delay need be added to the basic device delay specifications due to input pulse distortion.

ERROR CORRECTION

The determination of whether a DRAM system requires error correction must be resolved early in the system design. A positive answer to this question may have far-reaching impact on board development time and component cost. It is clear, however, that such a decision cannot be taken lightly.

The type and origin of errors in DRAM systems are many and can result from a number of sources (Table III). Current estimates of soft error rates due to alpha particles in 64k RAMs indicate some hope that these error rates will be similar or possibly better than those found in 16k DRAMs—but the facts are still somewhat unclear. However, it is clear that the use of 256k DRAMs and the introduction in the near future of 1 Mbit DRAMs with even smaller memory cells and greater chip densities will place a significant challenge on DRAM chip designers to keep these rates down. It is believed by some that error correction may become mandatory in future DRAM system designs. Currently, the decision to add error correction is not so straightforward. It depends on many factors, not the least of which is the end user's perception of its value to system uptime and reliability.

TABLE III. The Sources and Types of Memory Errors

Error Type	Sources	System Action
Soft	• Alpha Particles • System Noise • Chip Patterns • Power Glitches	Temporary system error—may be overwritten with a low probability of repetition
Hard	• Stuck Memory Bit • Memory Chip Interface • Interface Circuit Failure	Permanent failure—may act as logic 1 or 0

Generally, error correction will always be found in highly reliable systems during DRAMs, such as process control equipment, banking terminals, and military systems where high data integrity and minimum downtime are priorities. However, the importance of error correction has grown substantially, to the point that it is now used as selling feature in the vast majority of large memory-based systems. In fact, some major computer houses have adopted quidelines for use by their designers in the development of DRAM arrays. A somewhat common set has been found—if the memory array is on the order of ¼ million bytes, then word parity should be used. This permits the detection of single bit errors but does not allow error correction. When the total memory approaches ½ million bytes, then double bit error detection and single bit error correction should be added.

The decision to add error correction to a system is costly, both in memory overhead and control hardware. Table IV

TABLE IV. Check Bit Overhead for Multiple Bit Error Detection and Single Bit Error Correction

Number of Bits in Memory Data Word	Number of Check Bits Required	Percentage of Excess Memory
8	5	63%
16	6	38%
24	6 (7)	25% (29%)
32	7	22%
48	7 (8)	15% (17%)
64	8	13%

Note: The number stated assumes the use of the DP8400; the number in parentheses is required by other error correction circuits.

lists the number of additional memory chips required to support single bit error correction and double bit error detection as a function of the memory data word width.

This table also shows the percentage of DRAM overhead required to implement this function. Adding error correction also increases the memory access delay, since the information contained in the overhead chips must be analyzed in each read and generated in each write operation.

DP8400 16-Bit Expandable Error Correction Chip

The DP8400 expandable error checker/corrector is shown in block diagram form in *Figure 8*. This circuit offers a high degree of flexibility in applications which range from 8-bit to 80-bit data words. It is a 16-bit chip that is easily expandable with the simple addition of more DP8400s for each 16-bit word increment.

Figures 9a, 9b and *9c* demonstrate its basic operation in the write and read memory access cycles. *Figure 9a* shows the normal write cycle, where system data is used by the DP8400 to generate parity bits, called check bits, based on certain combinations of the data bits. This combination is defined by the DP8400's matrix shown in *Figure 10*. Whenever a "1" occurs in any row, the corresponding input data bit at the top of the column helps determine the parity for that check bit labeled at the end of the row. These check bits are written along with the data at the same memory address. Also, during a memory write cycle the DP8400 checks system byte parity. This is parity associated with the data bytes transmitted between the processor and the memory card. This is an optional feature that may prove very valuable in multiple board memory systems.

Sometime later a read will occur at this same memory address. The reading of memory data may be performed in two ways, as shown in *Figures 9b* and *9c*. In the read cycle, the DP8400 uses the data read from memory and internally regenerates check bits using the same matrix. These newly generated check bits are then compared (using X-OR gates) with the check bits read from memory to detect errors. The result of this comparison is called a syndrome word. Any differences in the generated versus read check bits will result in at least one syndrome bit true. This indicates an error in either the read data or check bit field or both.

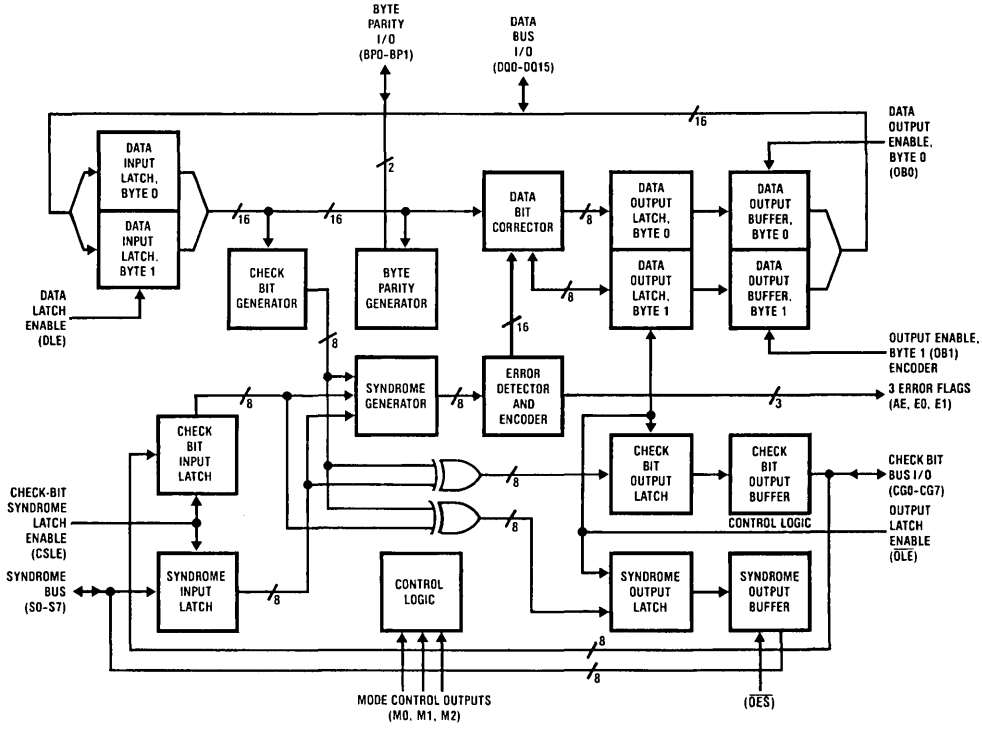

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FIGURE 8. DP8400 Simplified Block Diagram

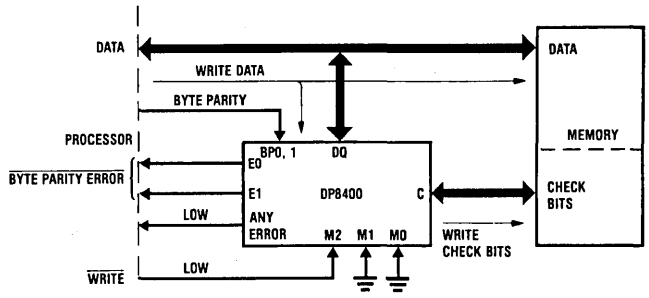

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FIGURE 9a. Normal Write Mode with DP8400

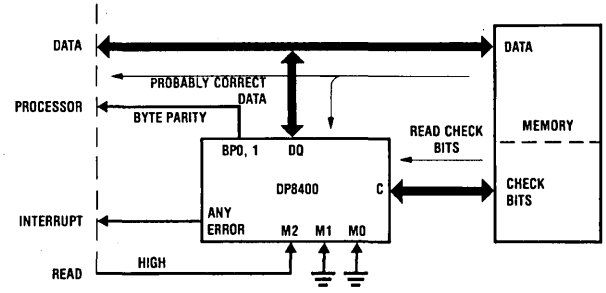

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FIGURE 9b. Normal Read Mode Using the Error Monitoring Method with the DP8400

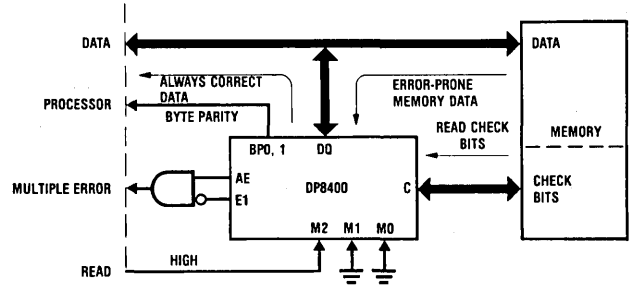

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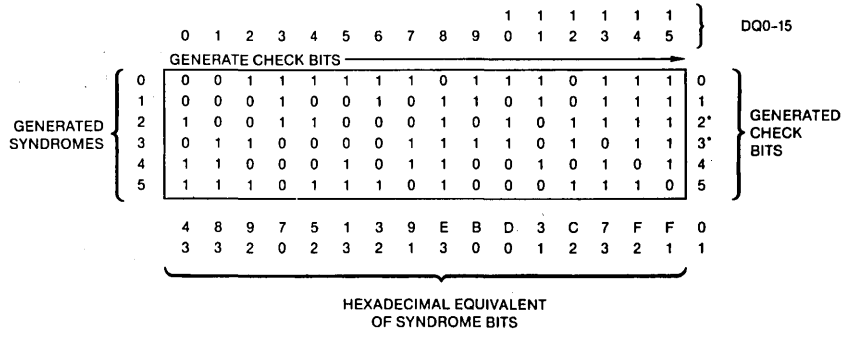
FIGURE 9c. Normal Read Mode Using the Always Correct Method with the DP8400



*C2, C3 generate odd parity

TL/F/5012–14

FIGURE 10. DP8400 Matrix

A key advantage of the DP8400 is that it has three error flags detailing the type of error occurrence. These are generated using the syndrome word in the manner shown in *Figure 11*. The resulting error type identifications are shown in Table V. The three error flags allow complete error type identification, plus the unique determination of double bit errors, which will be key during the discussion of double bit error correction. Also, on a memory read, the DP8400 generates byte parity bits for transmission to the processor along with the data.

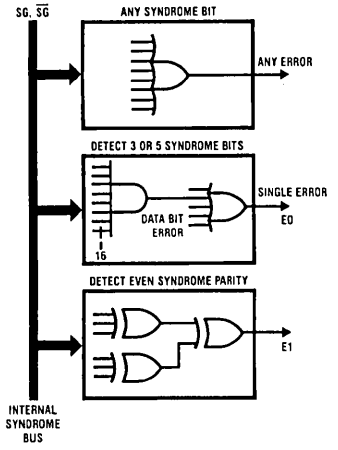


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TABLE V. Error Flags after Normal Read

AE	E1	E0	Error Type
0	0	0	No Error
1	1	0	Single Check Bit Error
1	1	1	Single Data Error
1	0	0	Double-Bit Error
All Others			Invalid Conditions

There are two basic memory read methods that may be used with the DP8400. The first is shown in *Figure 9b* and is called the error monitoring method. Here, the read data is assumed to be correct and the processor immediately acts on the data. If the DP8400 detects an error, the processor is interrupted using the any error flag (AE). Using this method, there is no detection delay in most memory reads since errors seldom occur, but when an error does occur, the processor must be capable of accepting an interrupt and a read cycle extension to obtain the corrected data from the DP8400.

A second approach is called the always correct method, *Figure 9c*. In this case, the data is always assumed to be in error and the processor always waits for the DP8400 to analyze whether an error exits. Then the corrected or unchanged data is read from the DP8400. Although this method results in longer memory read time, every memory read will always be of the same delay except when a double error occurs. The selection of which method to use depends on many factors, including the processor, system structure, and performance.

Double Bit Error Correct

The probability of double bit errors in DRAM systems is relatively low, but as memory array sizes grow, the occurrence of these error types must be considered. Adopting certain practices, such as rewriting a memory location whenever an error is detected, or using "memory scrubbing" techniques, can significantly reduce the probability of a double soft error occurrence. Memory scrubbing is when the system, during low usage, actually accesses memory solely for the purpose of identifying and correcting single soft errors. This is an important technique if there are segments of the memory that are not always being accessed so that soft error occurrences would not be quickly found.

The occurrence of a double error comprising one soft and one hard must now be considered. This type of error has a higher probability than two soft errors. The hard error may be due to a catastrophic chip failure, and a subsequent soft error will create two errors. This can be a source of concern since most error correction chips cannot handle double errors of this type. Therefore, most systems will "crash" when a catastrophic chip failure is coupled with a soft error in the same memory address.

The DP8400 has been designed to handle just such an occurrence. It can correct any double bit error, as long as at least one of the errors is a hard error. The DP8400 does this without the need for extra hardware required for the basic double bit detect/single bit correct system implementation. This method is called the double complement correct technique and is demonstrated in *Figure 12* using a 4-bit data word for simplicity. In this example, a single hard error is located in the most significant bit of a particular memory location and a soft error occurs at the next bit. The position of the errors is not important since the errors may be distributed in either the data or check bit field or both. First, the data word and corresponding check bits are written to this memory location. When a later read of this location occurs, step A, two errors are directly reported by the DP8400 error flags. The system detects this, disables memory; and places the DP8400 in the complement write mode. This causes the previously read data and check bits to be complemented in the DP8400 and written back to the same memory address, step B, writing over the previous soft error. Obviously this does not modify the cell where the hard error exits. The system then reads from the same address again, but this time it places the DP8400 in the complement read mode, step C. The DP8400 again complements the memory data and check bits and generates new check bits based on the new data word. At this point, the chip detects a single bit error in the bit position where the soft error occurred, and using the conventional single error correction procedure, returns corrected data to the system, step D.

In the second read, the complement read, the hard error repeats since this bit location again receives a bit which is complemented with respect to itself. But the soft error has been overwritten and does not repeat. Effectively, the memory has complemented the hard bit error position twice and the soft bit error position only once, while the DP8400 complements both positions twice. Therefore, after the second read, there is only one error left, the soft error. Since this is now a single error it can be directly corrected.

After the complement correct cycle, the memory must be rewritten with the corrected data since the address now contains data that is complemented. Full error reporting is available from the DP8400 after the second read, the complement read, of memory. This is shown in Table VI.

This method is a very effective tool to avoid system crash due to memory chip failure, and can do much to reduce unscheduled field service calls. The only time the system will see a double error that is not directly correctable is when a double soft error occurs. The probability of this is very low if the previously discussed techniques are used. The extra time taken to do an additional read and write of memory is insignificant when the alternative is a system that has a catastrophic failure that requires immediate field service. Using this technique, software may be provided in the system to warn the operator that the system is in a degraded operational mode and that field service should occur shortly. In the meantime, the system will continue to operate properly. The key to the effectiveness of the DP8400 in this application is its three error flags which allow complete error reporting—including a unique double error indication.

DP8402A, 3, 4, 5 32-Bit Error Detector and Corrector (EDAC)

In addition to the popular DP8400-2 16-bit error checker/corrector, National offers a family of 32-bit Error Detector and Correctors (EDACs). With a few exceptions, the DP8402A, 3, 4, 5 function in a similar manner to the DP8400-2. One major exception is that the DP8402A, 3, 4, 5 are not expandable beyond 32 bits.

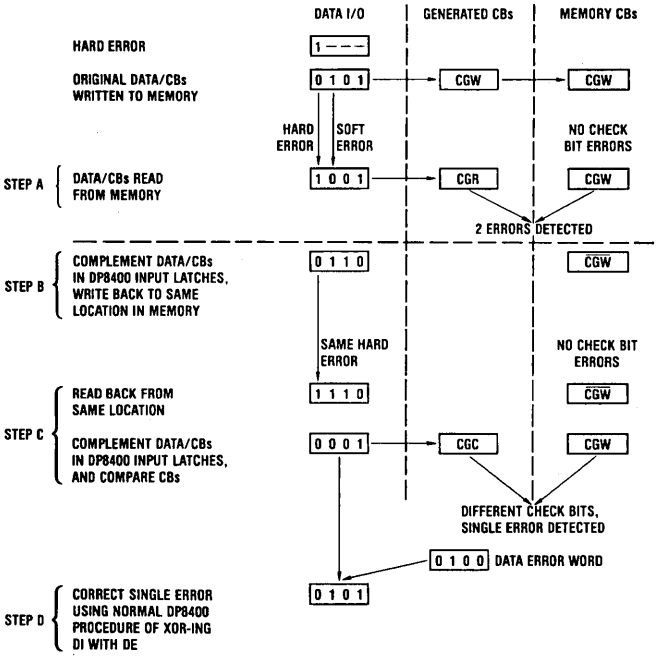

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FIGURE 12. Double Error Correct Complement Hard Error Method—1 Hard Error and 1 Soft Error in Data Bits

TABLE VI. DP8400 Error Flags after a Complement Read

AE	E1	E0	Error Type
0	0	0	Two Hard Errors
1	1	0	One Hard Error, One Soft Check Bit Error
1	1	1	One Hard Error, One Soft Data Bit Error
1	0	0	Two Soft Errors, Not Corrected

MICROPROCESSOR INTERFACE CIRCUITS

The major 8-bit, 16-bit and 32-bit microprocessors have different control signal timing. There are also a number of speed options. The DP8400 family was designed, not for a specific microprocessor, but rather, significant control flexibility has been provided on both the DP84XX DRAM controller/drivers and the DP84XX error correction devices for easy interface to any microprocessor. However, a certain amount of "glue" is necessary to interface to these LSI circuits, usually in the form of a number of MSI/SSI logic circuits. Not only can this be costly in board space utilization, but it is usually the one place where the most design related problems occur in system development.

Figures 13 and *14* show the DP8400 family solution to this problem—the DP84XX2 series of microprocessor interface circuits. *Figure 13* shows how the DP84300 refresh timer and the DP84XX2 microprocessor interface circuit connect to the DP8409A and various microprocessors for a typical application. *Figure 14* shows the DP8409A and the DP8400 together in a microprocessor-based memory system using DRAMs, with double bit error detect and single bit error correct capability. In addition, it shows that with the simple addition of some standard data buffers, how the system can implement byte writing to the DRAM array.

This system structure requires the insertion of few or no wait states during a memory access cycle, thus maximizing throughput. The DP84XX2 circuits have been designed to work with all of National's DRAM controller/drivers to control refreshing so that system throughput is affected only when absolutely necessary. First, in any refresh clock period of 16 μs, hidden refreshing is given maximum opportunity. This can be helped with the optional DP84300 refresh interval generator which offers maximum high-to-low ratioing of RFCK. Second, when a hidden refresh does not occur in a particular RFCK cycle, a forced refresh may still not affect a slow access cycle. The worst-case is when an access is pending during a forced refresh, in which case a three wait state delay is usually the maximum penalty.

Usually two DP84XX2 type chips would be required to interface between any microprocessor and the DP8400/DP8409A combined system. These chips would handle the read/write control as well as error detection and correction control. Table VII shows the individual DP84XX2 circuits that would be used in systems with no error correction, thus requiring only the DP84XX DRAM controller/driver function.

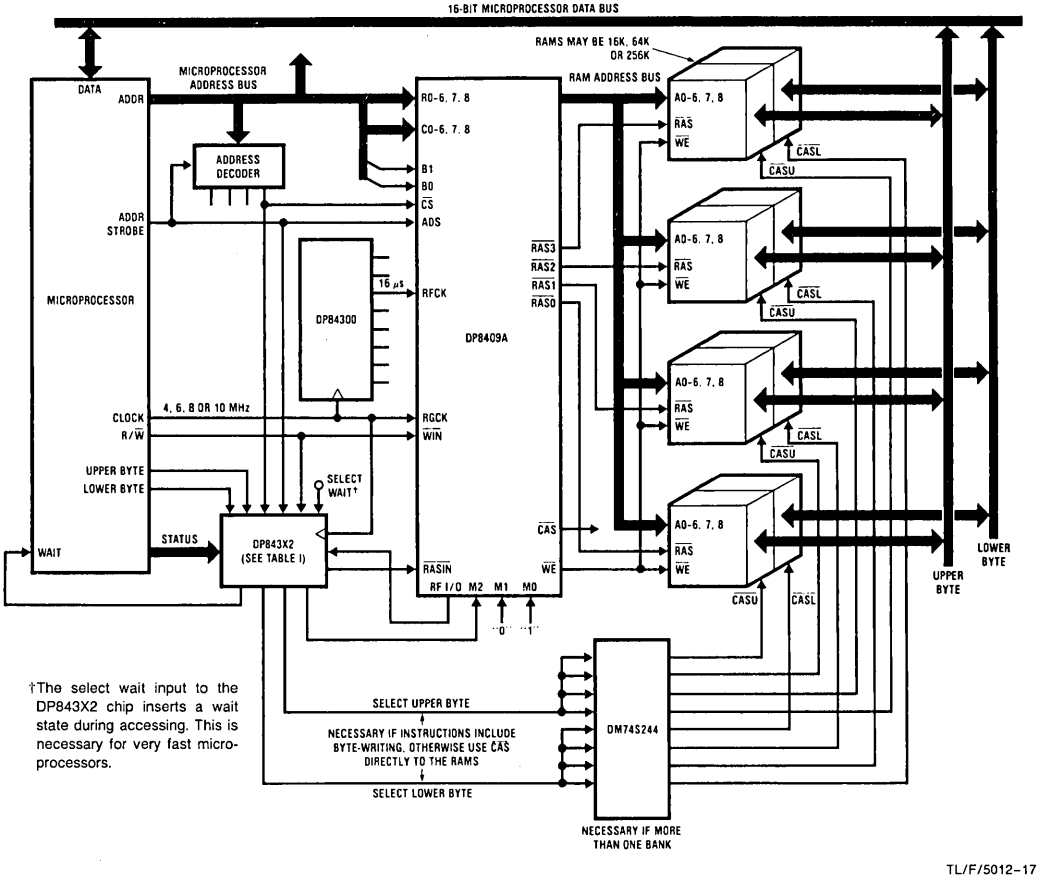

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FIGURE 13. Connecting the DP8409A between 16-Bit Microprocessor and Memory

The DP8400 DRAM interface family provides complete solutions to memory support. This begins with the LSI functions such as the DP8400 expandable error checker/corrector and the DP8409A DRAM controller/driver. It continues with the DP84240 and the DP84244 high performance buffer/drivers. Finally, it concludes with easy interface to popular microprocessors with the use of the DP84XX2 series. It is the first family of DRAM support circuits designed for universal applications with multiple microprocessors, with no manufacturers CPU enjoying a favorite role.

Data sheets and more detailed application information are available for all the members of the DP8400 family. Contact your local National Semiconductor representative or National Semiconductor directly.

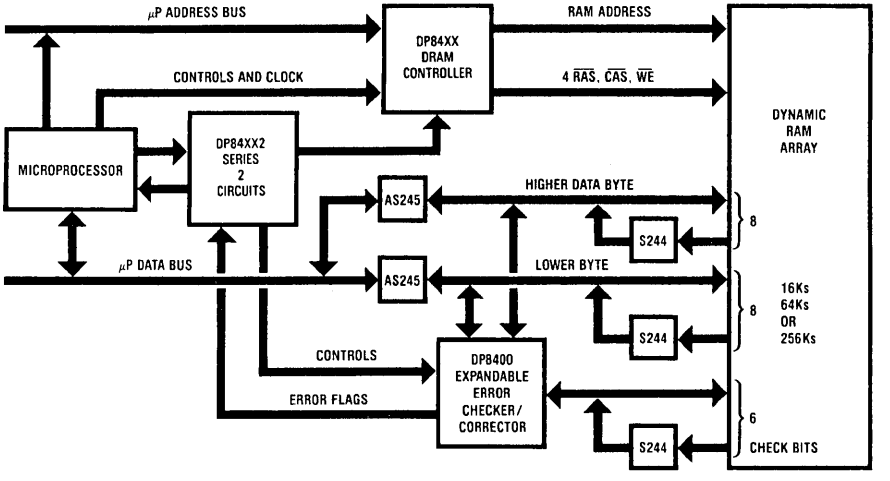

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FIGURE 14. Flexible Application of the DP8409A and DP8400. This Figure Shows an Application with a 16-Bit Microprocessor.

TABLE VII. The DP84300 Series of Interface Circuits for Various 16-Bit Microprocessors

Microprocessor	System Using DP84XX DRAM Controller/Driver
National & TI Series 32000	DP84412
National & TI Series 32332	DP84512
Motorola 68000/08/10	DP84322 or DP84422
Motorola 68020	DP84522
Intel 80286	DP84532
Intel 8086/186/88/188	DP84432
Zilog 8000	(2) 74S64 (1) 74S04

Section 1

Dynamic Memory Control

Section Contents

DRAM Controller Master Selection Guide

The data below is intended to highlight the key differentiable features of each DRAM Controller/Driver offered by National Semiconductor. All NSC DRAM controllers integrate onboard delay line timing, high capacitive drive, row/column muxing logic, refresh counter, row and column input latches, memory bank select logic. As a result of the family feature commonality, most devices offer pin for pin up/downward compatiblity. Beyond this however, the process and design differences between the devices result in a broad selection of feature and performance options for the best system fit.

Device # & Speed Options	DRAMS Supported	Process	Typ I_{CC}	A.C. Specified Word Width	Max $\overline{RAS}$ to $\overline{CAS}$ Out *Fast Mode | Slow Mode	Guaranteed Row Address Hold *Fast Mode | Slow Mode	V_{CC}	Operating Temp Range	Package	PAGE No.
DP8408A A-2 A-3	16, 64k	Junction Isolated (S)	210 mA	4 Banks of 16 Bit Data w/ 6 Bit ECC ea.	105 ns/125 ns 85 ns/100 ns 120 ns/145 ns	20 ns/30 ns 12 ns/20 ns 20 ns/30 ns	+5V ±5%	0°–70°C 0°–85°C	48N 48D	1-4
DP8409A A-2 A-3	16, 64, 256k	Junction Isolated (S)	210 mA	4 Banks of 16 Bit Data w/ 6 Bit ECC ea.	105 ns/125 ns 85 ns/100 ns 120 ns/145 ns	20 ns/30 ns 12 ns/20 ns 20 ns/30 ns	+5V ±5%	0°–70°C 0°–85°C	48N 48D 68V	1-22
DP8417-80 -70	16, 64, 256k	Oxide Isolated (ALS)	150 mA	4 Banks of 16 Bit Data w/ 6 Bit ECC ea.	63 ns/80 ns 50 ns/72 ns	15 ns/25 ns 15 ns/25 ns	+5V ±10%	0°–70°C −40°–+85°C −55°–+125°C	48 N 48D 68V	1-44
DP8418-80 -70	16, 64, 256k	Oxide Isolated (ALS)	150 mA	2 Banks of 32 Bit Data w/ 7 Bit ECC ea.	63 ns/80 ns 50 ns/72 ns	15 ns/25 ns 15 ns/25 ns	+5V ±10%	0°–70°C −40°–+85°C −55°–+125°C	48 N 48D 68V	1-44
DP8419-80 -70	16, 64, 256k	Oxide Isolated (ALS)	150 mA	4 Banks of 16 Bit Data w/ 6 Bit ECC ea.	63 ns/80 ns 50 ns/72 ns	15 ns/25 ns 15 ns/25 ns	+5V ±10%	0°–70°C −40°–+85°C −55°–+125°C	48 N 48D 68V	1-44
DP8420 & DP8422	16, 64, 256k & 1 Mega Bit	2μ CMOS	5 mA	2 Banks of 32 Bit Data w/ 7 Bit ECC ea.	—	—	+5V ±10%	0°–70°C −40°–+85°C −55°–+125°C	68V	1-92
DP8428-80 -70	16, 64, 256k & 1 Mega Bit	Oxide Isolated (ALS)	150 mA	2 Banks of 32 Bit Data w/ 7 Bit ECC ea.	63 ns/80 ns 50 ns/72 ns	15 ns/25 ns 15 ns/25 ns	+5V ±10%	0°–70°C −40°–+85°C −55°–+125°C	52D 68V	1-69
DP8429-80 -70	16, 64, 256k & 1 Mega Bit	Oxide Isolated (ALS)	150 mA	4 Banks of 16 Bit Data w/ 6 Bit ECC ea.	63 ns/80 ns 50 ns/72 ns	15 ns/25 ns 15 ns/25 ns	+5V ±10%	0°–70°C −40°–+85°C −55°–+125°C	52D 68V	1-69

*All AC valves shown factor in worst case loading (including all ouputs switching simultaneously), operating temperature, and V_{CC} supply variables. All delays assume the use of National's on-board automatic timing and delay line logic although external delay line control timing is allowed and supported.

National Semiconductor Corporation

DP8408A Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC . . . the DP8408A Dynamic RAM Controller/Driver. The DP8408A is capable of driving all 16k and 64k Dynamic RAMs (DRAMs). Since the DP8408A is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8408A's 6 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing less complicated.

The DP8408A is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 25 ns. The DP8408A timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8408A has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 6 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 8 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 8-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

The DP8408A can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, or 64k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

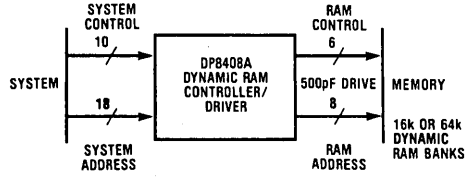
Operational Features

- All DRAM drive functions on one chip—minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drive directly all 16k and 64k DRAMs
- Capable of addressing 64k and 256k words
- Propagation delays of 25 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{\text{RAS}}$, Row to Column, select, then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- End-of-Count indicated by RF I/O pin going low at 127 or 255
- Low input on RF I/O resets 8-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 6 modes of operation: 3 access, 1 refresh, and 2 set-up
- 2 externally controlled modes: 1 access (Mode 4) and 1 refresh (Modes 0, 1 , 2)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with t_{RAH} = 20 or 30 ns minimum (Modes 5, 6)
- Externally controlled All-$\overline{\text{RAS}}$ Access modes for memory initialization (Mode 3)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)

DP8408A Interface Between System & DRAM Banks



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Block Diagram

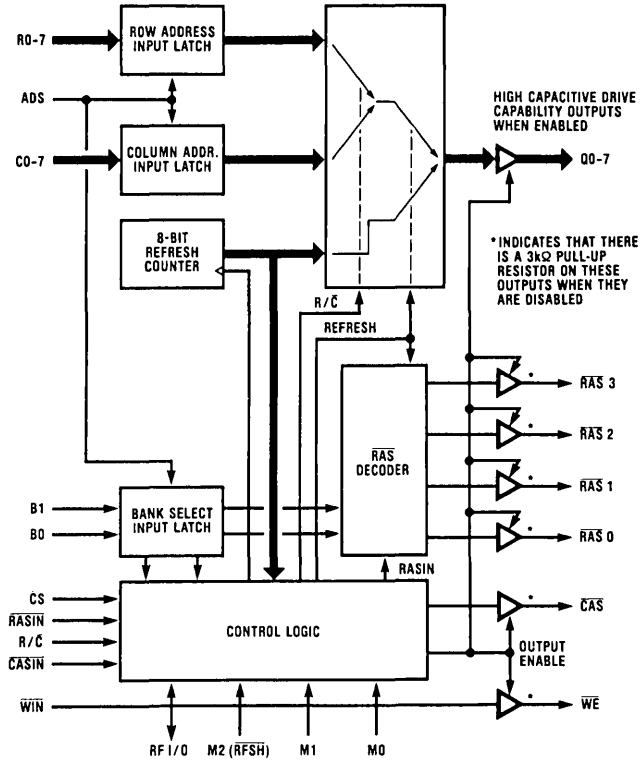

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TABLE I. DP8408A Mode Select Options

Mode	(RFSH) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = EOC
1	0	0	1		
2	0	1	0		
3	0	1	1	Externally Controlled All-RAS Write	All-RAS Active
4	1	0	0	Externally Controlled Access	Active RAS defined by Table II
5	1	0	1	Auto Access, Slow t_{RAH}	Active RAS defined by Table II
6	1	1	0	Auto Access, Fast t_{RAH}	Active RAS defined by Table II
7	1	1	1	Set End of Count	See Table III for Mode 7

Pin Definitions

V_{CC}, GND, GND—V_{CC} = 5V ±5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to pins 36 and 38 to reduce lead inductance. See *Figure* below.

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*Capacitor values should be chosen depending on the particular application.

R0–R7: Row Address Inputs.

C0–C7: Column Address Inputs.

Q0–Q7: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.*

$\overline{\text{RASIN}}$: Row Address Strobe Input—Enables selected $\overline{\text{RAS}}_n$ output when M2 ($\overline{\text{RFSH}}$) is high, or all $\overline{\text{RAS}}_n$ outputs when $\overline{\text{RFSH}}$ is low.

R/$\overline{\text{C}}$: Row/Column Select Input—Selects either the row or column address input latch onto the output bus.

$\overline{\text{CASIN}}$: Column Address Strobe Input—Inhibits $\overline{\text{CAS}}$ output when high in Modes 4 and 3. In Mode 6 it can be used to prolong $\overline{\text{CAS}}$ output.

ADS: Address (Latch) Strobe Input—Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; Latches on high-to-low transition.

$\overline{\text{CS}}$: Chip Select Input—TRI-STATE the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (except in Mode 0); enables all outputs when low.

M0, M1, M2: Mode Control Inputs—These 3 control pins determine the 6 major modes of operation of the DP8408A as depicted in Table I.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low when M2 = 0 and the End-of-Count output is at 127 or 255 (see Table III).

$\overline{\text{WIN}}$: Write Enable Input.

$\overline{\text{WE}}$: Write Enable Output—Buffered output from $\overline{\text{WIN}}$.*

$\overline{\text{CAS}}$: Column Address Strobe Output—In Modes 5 and 6, $\overline{\text{CAS}}$ goes low following valid column address. In Modes 3 and 4, it transitions low after R/$\overline{\text{C}}$ goes low, or follows $\overline{\text{CASIN}}$ going low if R/$\overline{\text{C}}$ is already low. $\overline{\text{CAS}}$ is high during refresh.*

$\overline{\text{RAS}}$ 0–3: Row Address Strobe Outputs—Selects a memory bank decoded from B1 and B0 (see Table II), if $\overline{\text{RFSH}}$ is high. If $\overline{\text{RFSH}}$ is low, all banks are selected.*

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{\text{RAS}}$ outputs when $\overline{\text{RASIN}}$ goes low. Also used to define End-of-Count in Mode 7 (Table III).

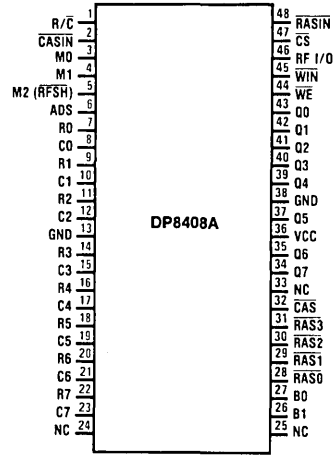
*These outputs may need damping resistors to prevent overshoot, undershoot. See AN-305 "Precautions to Take When Driving Memories."

TABLE II. Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{\text{RAS}}_n$
B1	B0	
0	0	$\overline{\text{RAS}}_0$
0	1	$\overline{\text{RAS}}_1$
1	0	$\overline{\text{RAS}}_2$
1	1	$\overline{\text{RAS}}_3$

Connection Diagram

Dual In-Line Package



NC = No Connection

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Top View

Order Number DP8408AD, DP8408AN or DP8408AN-3
See NS Package Number D48A or N48A

Conditions for all Modes

INPUT ADDRESSING

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go TRI-STATE and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other DP8408As for multi-addressing. All outputs go active about 50 ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

DRIVE CAPABILITY

The DP8408A has timing parameters that are specified with up to 600 pF loads. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of *Figure 6*. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To remove these spikes, a damping resistor (low inductance, carbon) can be inserted between the DP8408A driver outputs and the DRAMs, as close as possible to the DP8408A. The values of the damping resistors may differ between the different control outputs; $\overline{RAS}$'s $\overline{CAS}$, Q's and $\overline{WE}$. The damping resistors should be determined by the first prototypes (not wire-wrapped due to larger distributed capacitance and inductance). The best values for the damping resistors are the critical values giving a critically damped transition on the control outputs. Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading the higher the value. (For more information, see AN-305 "Precautions to Take When Driving Memories.")

DP8408A DRIVING ANY 16K OR 64K DRAMS

The DP8408A can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8408A can drive all 16k DRAMS (see *Figure 1a*).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8408A can drive all three configurations, and at the same time allows them all to be interchangeable (as shown in *Figure 1b* and *1c*), providing maximum flexibility in the choice of DRAMs. Since the 8-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2 ms (i.e. 256 rows in 4 ms) all DRAM types are correctly refreshed.

When the DP8408A is in a refresh mode, the RF I/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127 or 255 to accommodate 16k or 64k DRAMs, respectively. Although the end-of-count may be chosen to be either of these values, the counter is not reset and always counts to 255 before rolling over to zero.

READ, WRITE AND READ-MODIFY-WRITE CYCLES

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

POWER-UP INITIALIZE

When V_{CC} is first applied to the DP8408A, an initialize pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3V, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to TRI-STATE. As V_{CC} increases above 2.3V, control of these outputs is granted to the system.

DP8408A Driving any 16k or 64k Dynamic RAMs

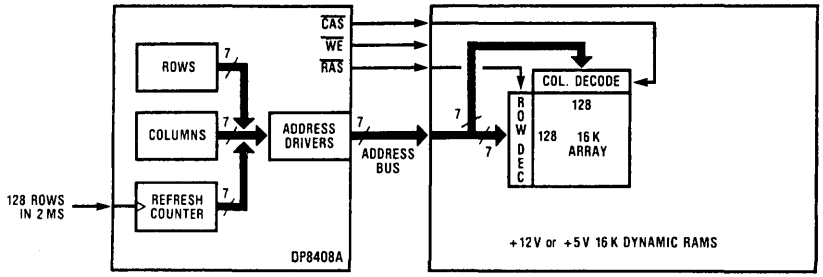

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FIGURE 1a. DP8408A with any 16k DRAMS

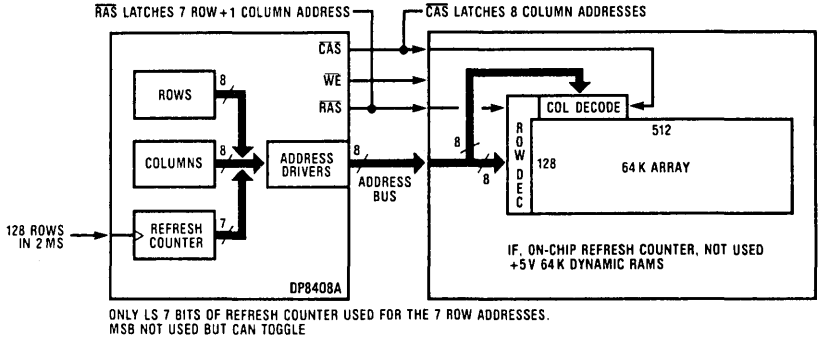

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FIGURE 1b. DP8408A with 128 Row × 512 Column 64k DRAM

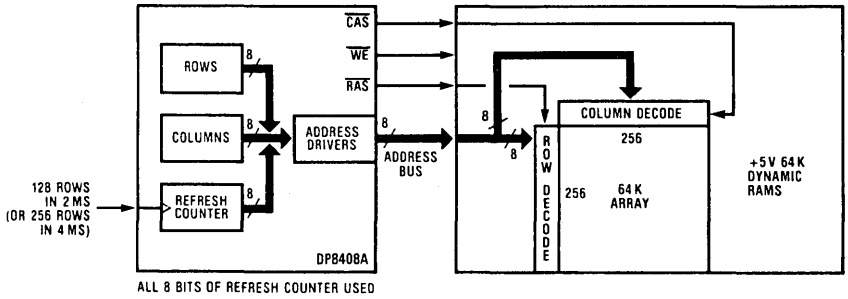

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FIGURE 1c. DP8408A with 256 × 256 Column 64k DRAM

Functional Mode Descriptions

Note: All delay parameters stated in text refer to the DP8408A. Substitute the respective delay numbers for the DP8408-2 or DP8408-3 when using these devices.

MODES 0, 1, 2 — EXTERNALLY CONTROLLED REFRESH

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed. In the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $\overline{RFSH}$ goes low-to-high after a refresh. RF I/O goes low when the count is 127 or 255, as set by End-of-Count (see Table III), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeros, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and RFSH must be skewed transitioning low such that the refresh address is valid on the address outputs of the controller before the $\overline{RAS}$ outputs go low. The amount of time that RFSH should go low before $\overline{RASIN}$ does depends on the capacitive loading of the address and $\overline{RAS}$ lines. For the load specified in the switching characteristics of this data sheet, 10 ns is sufficient. Refer to *Figure 2*.

To perform externally controlled burst refresh, $\overline{RASIN}$ is toggled while RFSH is held low. The refresh counter increments with $\overline{RASIN}$ going low to high, so that the DRAM rows are refreshed in succession by $\overline{RASIN}$ going high to low.

MODE 3 — EXTERNALLY CONTROLLED ALL-$\overline{RAS}$ WRITE

This mode is useful at system initialization. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the DP8408A for the next write cycle.

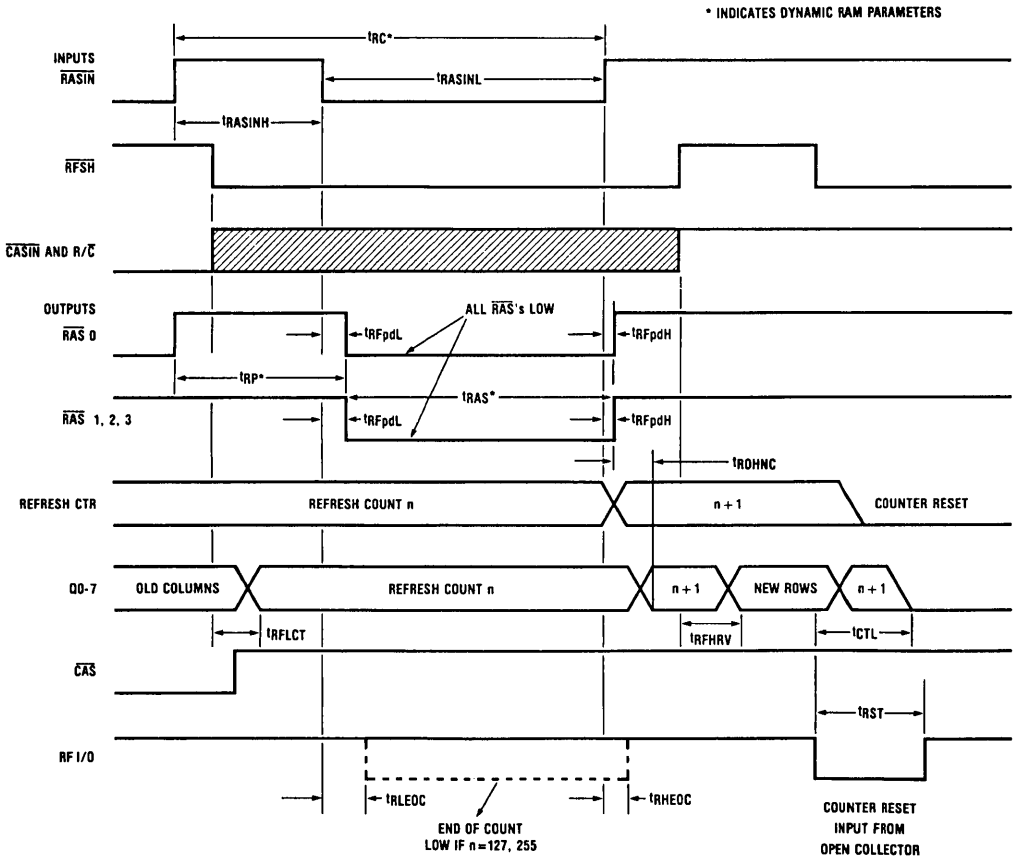

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FIGURE 2. External Control Refresh Cycle (MODES 0, 1, 2)

Functional Mode Descriptions (Continued)

MODE 4 — EXTERNALLY CONTROLLED ACCESS

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in *Figure 3*.

Output Address Selection

Refer to *Figure 4a*. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0–Q7, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0–Q7. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see *Figure 4b*). If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ will be automatically generated, following the row to column transition by about 20 ns (see *Figure 4a*). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

AC parameters t_{DIF1}, t_{DIF2} may be used to determine the minimum delays required between $\overline{RASIN}$, R/$\overline{C}$, and $\overline{CASIN}$ (see Application Brief 9; "Fastest DRAM Access Mode").

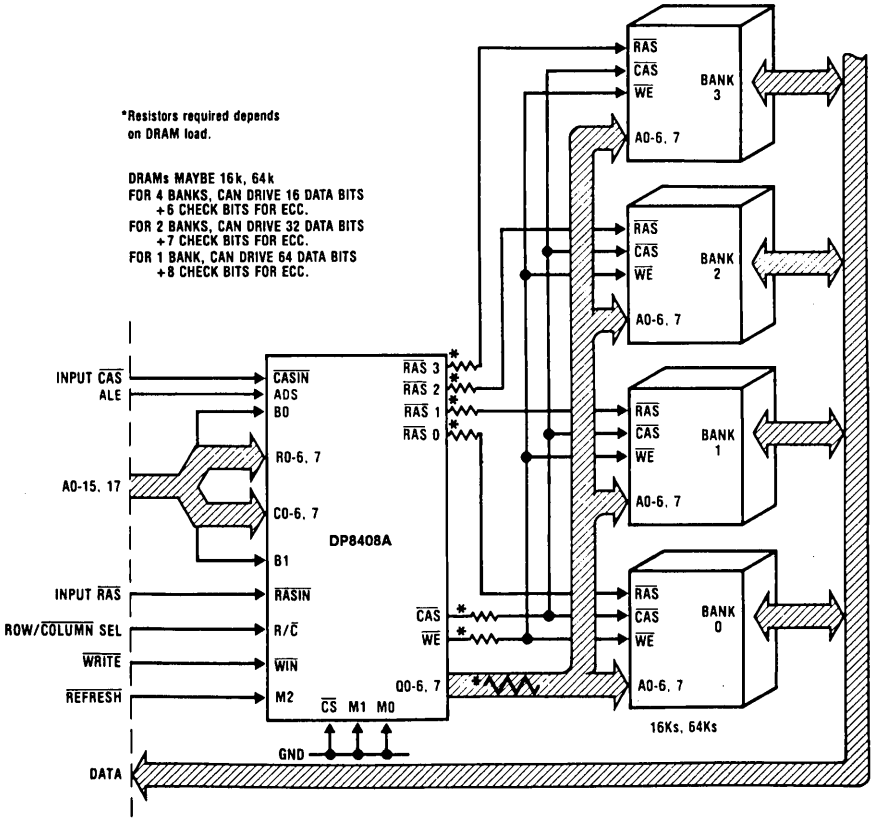

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FIGURE 3. Typical Application of DP8408A Using Externally Controlled Access and Refresh in Modes 0 and 4

Timing Diagrams

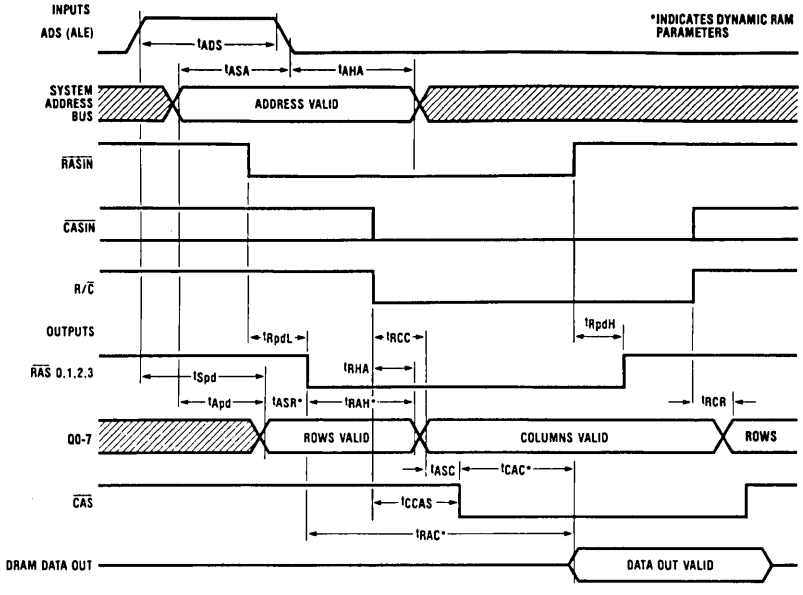

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FIGURE 4a. Read Cycle Timing (Mode 4)

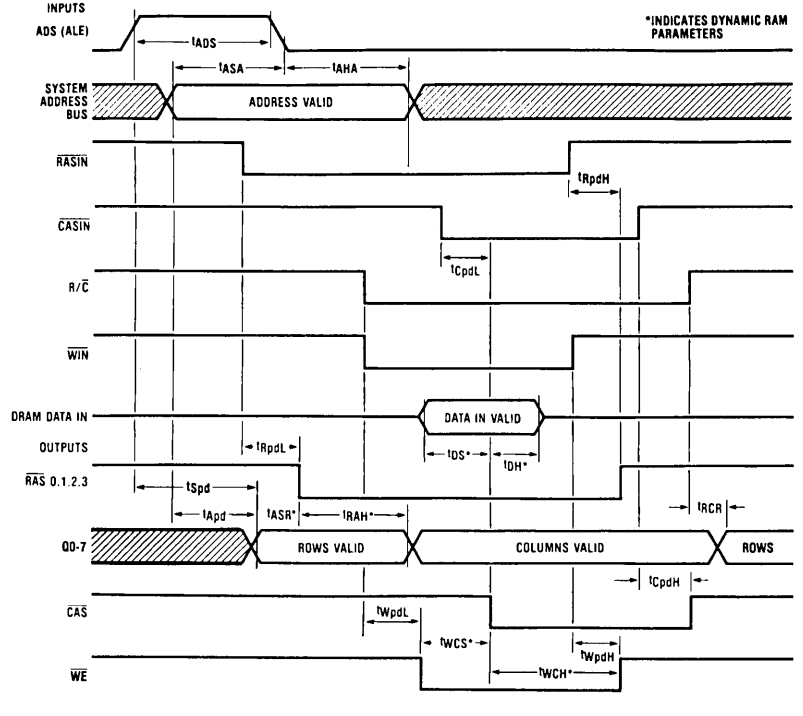

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FIGURE 4b. Write Cycle Timing (Mode 4)

Functional Mode Descriptions (Continued)

MODE 5—AUTOMATIC ACCESS

The Auto Access mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary. Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 (and Mode 6) of the DP8408A make DRAM accessing appear essentially "static".

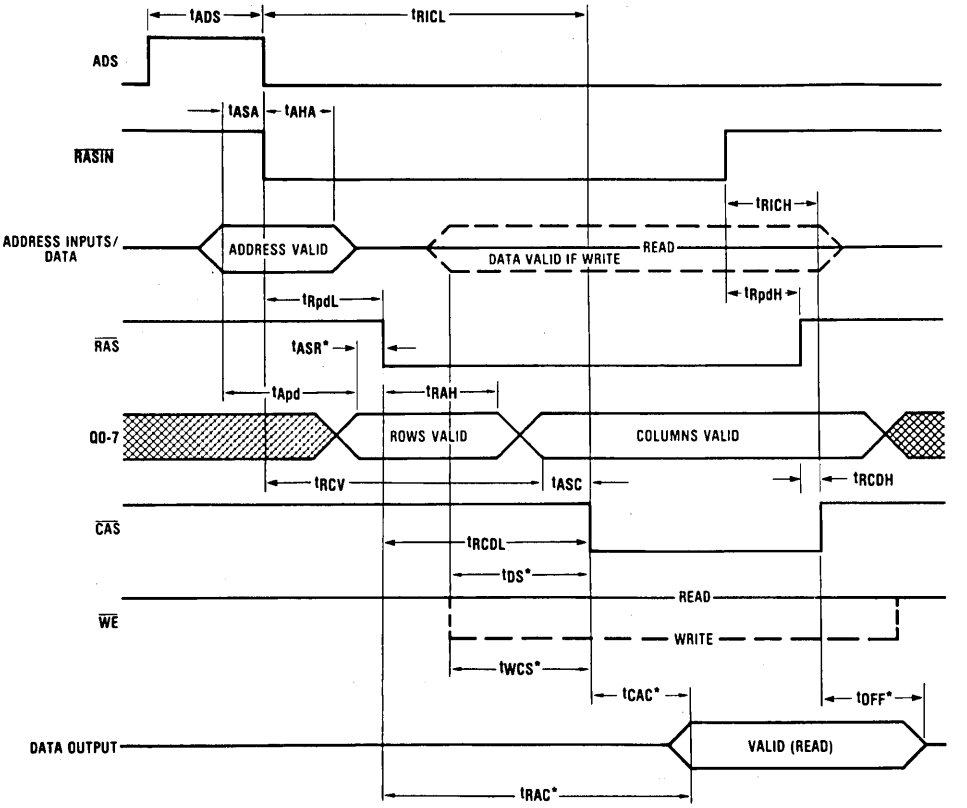
AUTOMATIC ACCESS CONTROL

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the DP8408A in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the DP8408A. The Address Setup-Up time (t_{ASR}), is 0 ns on most DRAMs. The DP8408A in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see *Figure 5a*).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$

Timing Diagram



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*Indicates Dynamic RAM Parameters

FIGURE 5a. Modes 5, 6 Timing ($\overline{CASIN}$) High in Mode 6

Functional Mode Descriptions (Continued)

occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

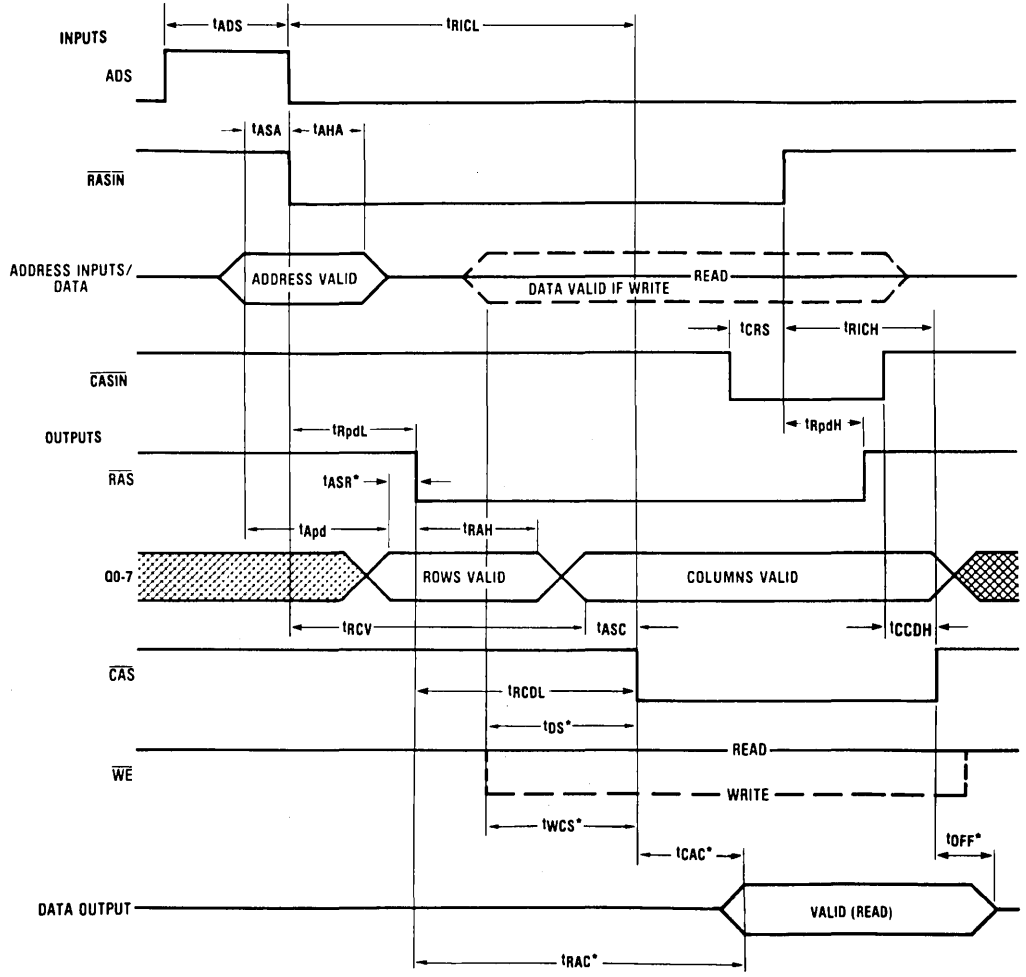
This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$. All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

MODE 6—FAST AUTOMATIC ACCESS

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ pin is not used, but $\overline{CASIN}$ is used to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to *Figure 5b*. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

Timing Diagram



*Indicates Dynamic RAM Parameters

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FIGURE 5b. Mode 6 Timing, Extended $\overline{CAS}$

Functional Mode Descriptions (Continued)

MODE 7—SET END-OF-COUNT

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table III). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

TABLE III. Mode 7

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	127
1	1	127

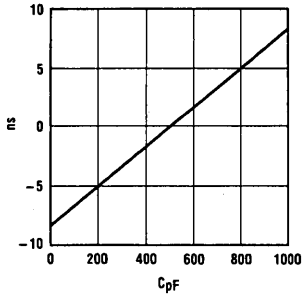

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FIGURE 6. Change in Propagation Delay vs. Loading Capacitance Relative to a 500 pF Load

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150 mA
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 23.6 mW/°C above 25°C; derate molded package 22.7 mW/°C above 25°C.

Maximum Power Dissipation* at 25°C	
Cavity Package	3542 mW
Molded Package	2833 mW

Operating Conditions

		Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min., I_C = −12 mA		−0.8	−1.2	V
I_{IH1}	Input High Current for ADS, R/$\overline{C}$ only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input High Current for All Other Inputs*	V_{IN} = 2.5V		1.0	50	μA
I_I RSI	Output Load Current for RF I/O	V_{IN} = 0.5V, Output High		−1.5	−2.5	mA
I_I CTL	Output Load Current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, Chip Deselect		−1.5	−2.5	mA
I_{IL1}	Input Low Current for ADS, R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input Low Current for All Other Inputs*	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	I_{OL} = 20 mA		0.3	0.5	V
V_{OL2}	Output Low Voltage for RF I/O	I_{OL} = 10 mA		0.3	0.5	V
V_{OH1}	Output High Voltage*	I_{OH} = −1 mA	2.4	3.5		V
V_{OH2}	Output High Voltage for RF I/O	I_{OH} = − 100 μA	2.4	3.5		V
I_{1D}	Output High Drive Current*	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output Low Drive Current*	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	TRI-STATE Output Current (Address Outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, $\overline{CS}$ = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply Current	V_{CC} = Max.		210	285	mA

*Except RF I/O Output.

Switching Characteristic DP8408A/DP8408-3

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each of 88 DRAMs including trace capacitance. These values are: Q0–Q7, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, unless otherwise noted. See *Figure 7* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8408A			8408-3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*	95	125	160	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 5a, 5b*	80	105	140	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*	40	48	60	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 5a, 5b*	50	63	80	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*		98	125		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 5a, 5b*		78	105		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 5a*		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 5b*	40	54	70	40	54	80	ns
t_{RAH}	Row Address Hold Time (Mode 5)	*Figure 5a*	30			30			ns
t_{RAH}	Row Address Hold Time (Mode 6)	*Figures 5a, 5b*	20			20			ns
t_{ASC}	Column Address Setup Time (Mode 5)	*Figure 5a*	8			8			ns
t_{ASC}	Column Address Setup Time (Mode 6)	*Figures 5a, 5b*	6			6			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	*Figure 5a*		90	120		90	140	ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	*Figures 5a, 5b*		75	105		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 4a, 4b, 5a, 5b*	20	27	35	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 4a, 4b, 5a, 5b*	15	23	32	15	23	37	ns
t_{APDL}	Address Input to Output Low Delay	*Figures 4a, 4b, 5a, 5b*		25	40		25	46	ns
t_{APDH}	Address Input to Output High Delay	*Figures 4a, 4b, 5a, 5b*		*25*	*40*		*25*	*46*	*ns*
t_{SPDL}	*Address Strobe to Address Output Low*	*Figures 4a, 4b,*		40	60		40	70	ns
t_{SPDH}	Address Strobe to Address Output High	*Figures 4a, 4b,*		40	60		40	70	ns
t_{ASA}	Address Setup Time to ADS	*Figures 4a, 4b, 5a, 5b*	15			15			ns
t_{AHA}	Address Hold Time from ADS	*Figures 4a, 4b, 5a, 5b*	15			15			ns
t_{ADS}	Address Strobe Pulse Width	*Figures 4a, 4b, 5a, 5b*	30			30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 4b*	15	25	30	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 4b*	15	30	60	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ Setup Time to $\overline{RASIN}$ High (Mode 6)	*Figure 5b*	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	*Figure 4b*	32	41	68	32	41	77	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay	*Figure 4b*	25	39	50	25	39	60	ns
t_{RCC}	Column Select to Column Address Valid	Figure 4a		40	58		40	67	ns
t_{RCR}	Row Select to Row Address Valid	*Figures 4a, 4b*		40	58		40	67	ns
t_{RHA}	Row Address Held from Column Select	*Figure 4a*	10			10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	*Figure 7a*		65	90				ns

Switching Characteristics DP8408A/DP8408-3 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each of 88 DRAMs including trace capacitance. These values are: Q0–Q7, C_L = 500 pF; $\overline{RAS}$0–$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, unless otherwise noted. See *Figure 7* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8408A			8408-3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 description			13			18	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 description			13			18	ns
Refresh Parameter									
t_{RC}	Refresh Cycle Period	*Figure 2*	100			100			ns
$t_{RASINL, H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2*	50			50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figure 2*	35	50	70	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figure 2*	30	40	55	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, *Figure 2*		47	60		47	70	ns
t_{RFHRV}	RFSH High to Row Address Valid	*Figure 2*		45	60		45	70	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figure 2*		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50 pF, *Figure 2*			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50 pF, *Figure 2*			80			80	ns
t_{RST}	Counter Reset Pulse Width	*Figure 2*	70			70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	*Figure 2*			100			100	ns
TRI-STATE Parameter									
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	*Figure 8* R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	C_L = 15 pF, *Figure 8* R2 = 1k, S1 open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	*Figure 8* R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15 pF, *Figure 8* R1 = 1k, S2 open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	*Figure 8* R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15 pF, *Figure 8* R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	*Figure 8* S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15 pF, *Figure 8*, R2 = 750Ω, S1 open		50	80		50	80	ns

Switching Characteristics DP8408-2

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5, 7). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMS including trace capacitance. These values are: Q0–Q7, C_L = 500 pF; $\overline{RAS}$0–$\overline{RAS}$3, C_L = 150 pF, $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, unless otherwise noted. See *Figure 7* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8408-2			Units
			Min	Typ	Max	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 5a, 5b*	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 5a, 8b*	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 5a, 5b*		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 5a*		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 5a*		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 5b*	40	54	70	ns
t_{RAH}	Row Address Hold Time (Mode 5) (Note 7)	*Figure 5a*	20			ns
t_{RAH}	Row Address Hold Time (Mode 6) (Note 7)	*Figures 5a, 5b*	12			ns
t_{ASC}	Column Address Setup Time (Mode 5)	*Figure 5a*	3			ns
t_{ASC}	Column Address Setup Time (Mode 6)	*Figures 5a, 8b*	3			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	*Figure 5a*		80	105	ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	*Figures 5a, 5b*		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 4a, 4b, 5a, 5b*	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 4a, 4b, 5a, 5b*	15	23	32	ns
t_{APDL}	Address Input to Output Low Delay	*Figures 4a, 4b, 5a, 5b*		25	40	ns
t_{APDH}	Address Input to Output High Delay	*Figures 4a, 4b, 5a, 5b*		25	40	ns
t_{SPDL}	Address Strobe to Address Output Low	*Figures 4a, 4b*		40	60	ns
t_{SPDH}	Address Strobe to Address Output High	*Figures 4a, 4b*		40	60	ns
t_{ASA}	Address Set-up Time to ADS	*Figures 4a, 4b, 5a, 5b*	15			ns
t_{AHA}	Address Hold Time from ADS	*Figures 4a, 4b, 5a, 5b*	15			ns
t_{ADS}	Address Strobe Pulse Width	*Figures 4a, 4b, 5a, 5b*	30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 4b*	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 4b*	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ Set-up Time to $\overline{RASIN}$ High (Mode 6)	*Figure 5b*	35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	*Figure 4b*	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	*Figure 4b*	25	39	50	ns
t_{RCC}	Column Select to Column Address Valid	*Figure 4a*		40	58	ns
t_{RCR}	Row Select to Row Address Valid	*Figures 4a, 4b*		40	58	ns
t_{RHA}	Row Address Held from Column Select	*Figure 4a*	10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	*Figure 7a*		55	75	ns

Switching Characteristics DP8408-2 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5, 7). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMS including trace capacitance. These values are: Q0–Q7, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF, $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, unless otherwise noted. See *Figure 7* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8408-2			Units
			Min	Typ	Max	
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 description			13	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 description			13	ns
Refresh Parameter						
t_{RC}	Refresh Cycle Period	*Figure 2*	100			ns
$t_{RASINL, H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2*	50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figure 2*	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figure 2*	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, *Figure 2*		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figure 2*		45	60	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figure 2*		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50 pF, *Figure 2*			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50 pF, *Figure 2*			80	ns
t_{RST}	Counter Reset Pulse Width	*Figure 2*	70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	*Figure 2*			100	ns
TRI-STATE Parameter						
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	*Figures 9, 12* R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	C_L = 15 pF, *Figures 9, 12* R2 = 1k, S1 open		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	*Figures 9, 12* R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15 pF, *Figures 9, 12* R1 = 1k, S2 open		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	*Figures 9, 12* R2 = 750Ω, S1 open		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15 pF, *Figures 9, 12* R2 = 750Ω, S1 open		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	*Figure 12,* S1, S2 open		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15 pF, *Figure 12,* R2 = 750Ω, S1 open		50	80	ns

Input Capacitance T_A = 25°C (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Note 6: Applies to all DP8408A versions unless otherwise specified.

Note 7: The DP8408-2 device can only be used with memory devices that meet the t_{RAH} specification indicated.

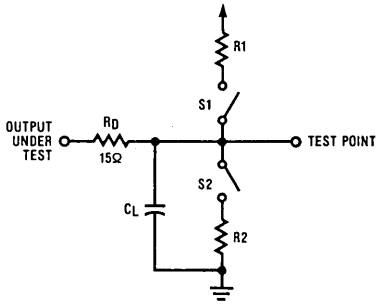

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FIGURE 7. Output Load Circuit

Timing Waveform

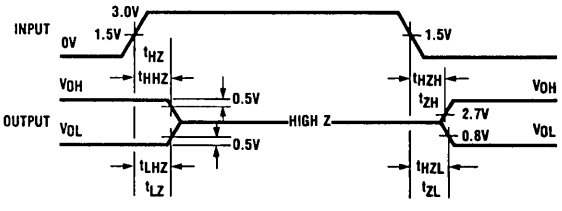

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FIGURE 8

Applications

If external control is preferred, the DP8408A may be used in Modes 0 or 4, as in *Figure 3*.

If basic auto access and refresh are required, then in cases where the user requires the minimum of external complexity, Modes 0 and 5 are ideal, as shown in *Figure 9a*. The DP843X2 is used to provide proper arbitration between memory access and refresh. This chip supplies all the necessary control signals to the processor as well as the DP8408A. Furthermore, two separate $\overline{CAS}$ outputs are also included for systems using byte-writing. The refresh clock RFCK may be divided down from either RGCK using an IC counter such as the DM74LS393 or better still, the DP84300 Programmable Refresh Timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on the input clock of 2 to 10 MHz. *Figure 9b* shows the general timing diagram for interfacing the DP8408A to different microprocessors using the interface controller DP843X2.

Applications (Continued)

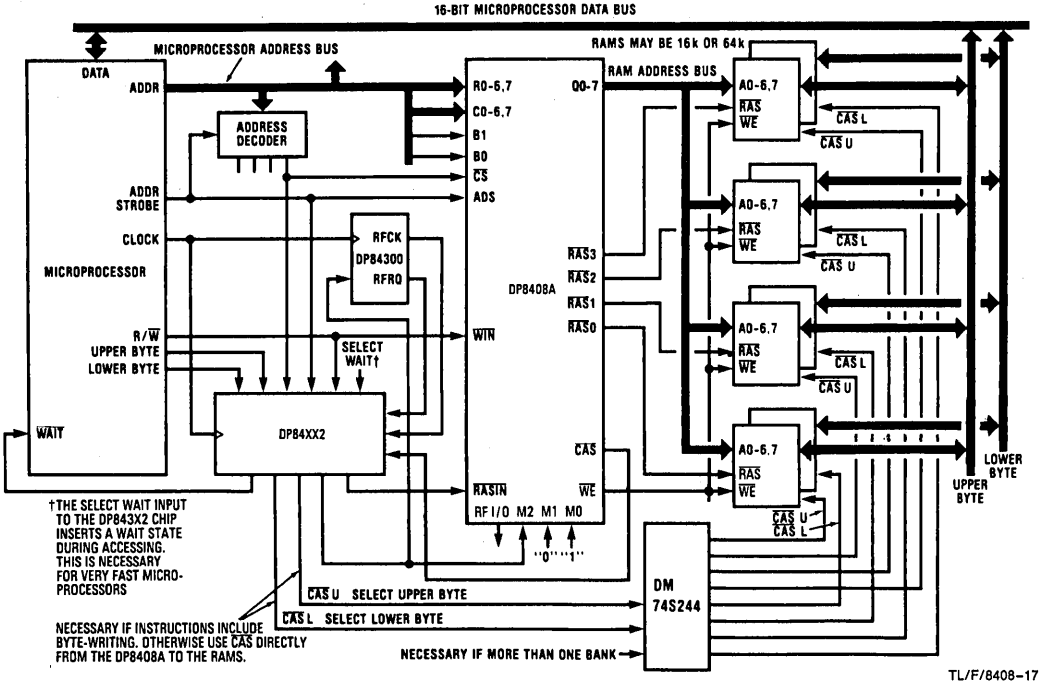

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FIGURE 9a. Connecting the DP8408A between the 16-Bit Microprocessor and Memory

Applications (Continued)

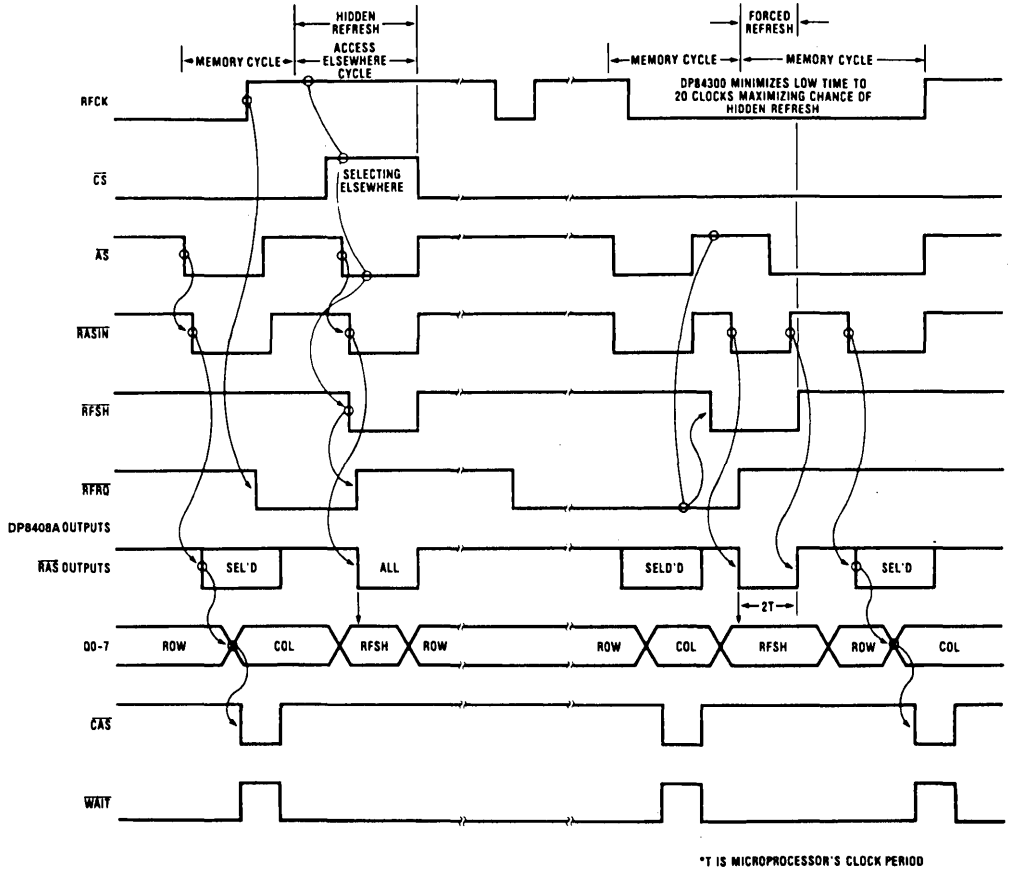

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FIGURE 9b. DP8408A Auto Refresh

National Semiconductor Corporation

DP8409A Multi-Mode Dynamic RAM Controller/Driver

General Description

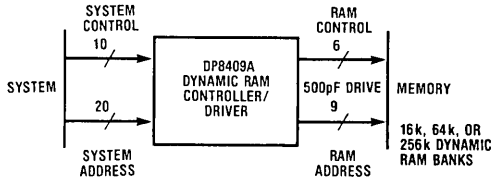
Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC ... the DP8409A Multi-Mode Dynamic RAM Controller/Driver. The DP8409A is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the DP8409A is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8409A's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409A is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 25 ns. The DP8409A timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8409A has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

The DP8409A can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.



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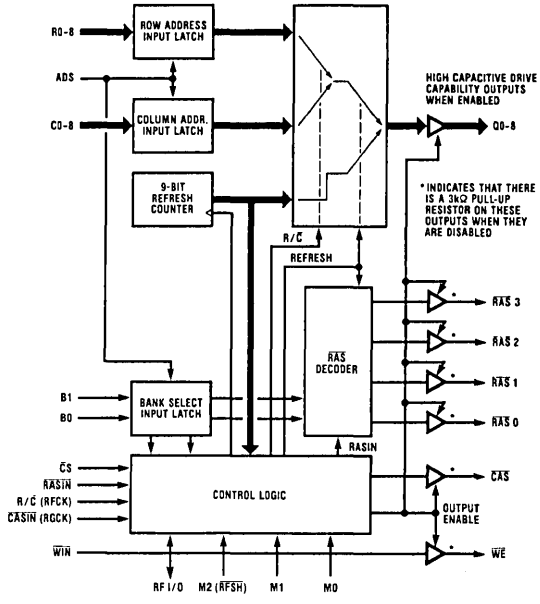
Operational Features

- All DRAM drive functions on one chip—minimizes skew on outputs, maximizes AC peformance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k, 64k, and 256k DRAMs
- Capable of addressing 64k, 256k, or 1M words
- Propagation delays of 25 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{\text{RAS}}$, row to column select, then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)
- End-of-Count indicated by RF I/O pin going low at 127, 255 or 511
- Low input on RF I/O resets 9-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 8 modes of operation: 3 access, 3 refresh, and 2 set-up
- 2 externally controlled modes: 1 access and 1 refresh (Modes 0, 4)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with t_{RAH} = 20 or 30 ns minimum (Modes 5, 6)
- Auto-access mode allows Hidden Refreshing (Mode 5)
- Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)
- Forced Refresh performed after system acknowledge of request (Mode 1)
- Automatic Burst Refresh mode stops at End-of-Count of 127, 255, or 511 (Mode 2)
- 2 All-$\overline{\text{RAS}}$ Acces modes externally or automatically controlled for memory initialization (Modes 3a, 3b)
- Automatic All-$\overline{\text{RAS}}$ mode with external 8-bit counter frees system for other set-up routines (Mode 3a)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)

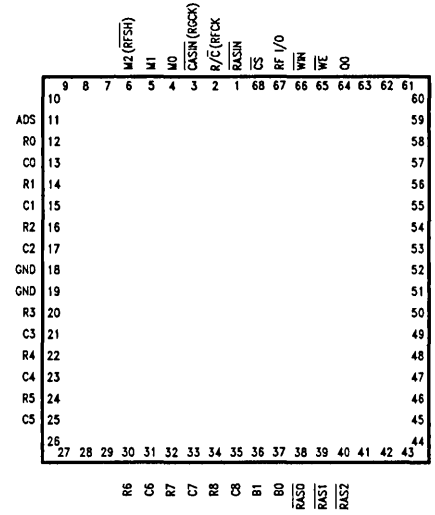
Block and Connection Diagrams



TL/F/8409-2

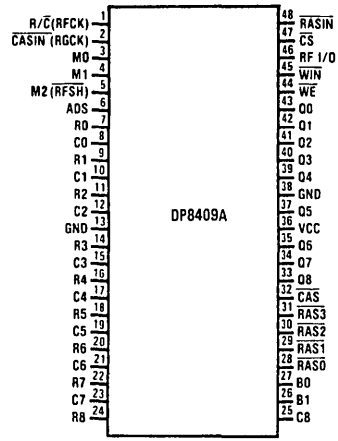
Order Number DP8409AD, DP8409AN, DP8409AN-3 or DP8409AV-2
See NS Package Number D48A, N48A or V68A

68 Pin PCC



TL/F/8409-3

Dual-In-Line Package



TL/F/8409-5

Top View

Pin Definitions

V_{CC}, GND, GND—V_{CC} = 5V ±5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to pins 36 and 38 to reduce lead inductance. See figure below.

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*Capacitor values should be chosen depending on the particular application.

R0–R8: Row Address Inputs.

C0–C8: Column Address Inputs.

Q0–Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.*

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high, or all $\overline{RAS}_n$ outputs when $\overline{RFSH}$ is low.

R/$\overline{C}$ (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input: selects either the row or column address input latch onto the output bus.

Pin Definitions (Continued)

TABLE I. DP8409A Mode Select Options

Mode	($\overline{RFSH}$) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto Refresh—Forced	RF I/O = Refresh Request ($\overline{RFRQ}$)
2	0	1	0	Internal Auto Burst Refresh	RF I/O = $\overline{EOC}$
3a	0	1	1	All $\overline{RAS}$ Auto Write	RF I/O = $\overline{EOC}$; All $\overline{RAS}$ Active
3b	0	1	1	Externally Controlled All $\overline{RAS}$ Access	All $\overline{RAS}$ Active
4	1	0	0	Externally Controlled Access	Active $\overline{RAS}$ Defined by Table II
5	1	0	1	Auto Access, Slow t_{RAH}, Hidden Refresh	Active $\overline{RAS}$ Defined by Table II
6	1	1	0	Auto Access, Fast t_{RAH}	Active $\overline{RAS}$ Defined by Table II
7	1	1	1	Set End of Count	See Table III for Mode 7

$\overline{CASIN}$ (RGCK)—In Auto-Refresh Mode, Auto Burst Mode, and All-$\overline{RAS}$ Auto-Write Mode, this pin is the $\overline{RAS}$ Generator Clock input. In all other modes it is $\overline{CASIN}$ (Column Address Strobe Input), which inhibits $\overline{CAS}$ output when high in Modes 4 and 3b. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; Latches on high-to-low transition.

$\overline{CS}$: Chip Select Input—The TRI-STATE mode will Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2: Mode Control Inputs—These 3 control pins determine the 8 major modes of operation of the DP8409A as depicted in Table I.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0 and 2 when the End-of-Count output is at 127, 255, or 511 (see Table III). In Auto-Refresh Mode it is the Refresh Request output.

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.*

$\overline{CAS}$: Column Address Strobe Output—In Modes 3a, 5, and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high duing refresh.*

$\overline{RAS}$ 0–3: Row Address Strobe Outputs—Selects a memory bank decoded from B1 and B0 (see Table II), if $\overline{RFSH}$ is high. If $\overline{RFSH}$ is low, all banks are selected.*

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low. Also used to define End-of-Count in Mode 7 (Table III).

Conditions for All Modes

INPUT ADDRESSING

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go TRI-STATE and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other DP8409As for multi-addressing. All outputs go active about 50 ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

DRIVE CAPABILITY

The DP8409A has timing parameters that are specified with up to 600 pF loads. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of *Figure 10*. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To remove these spikes, a damping resistor (low inductance, carbon) can be inserted between the DP8409A driver outputs and the DRAMs, as close as possible to the DP8409A. The values of the damping resistors may differ between the different control outputs; $\overline{RAS}$s, $\overline{CAS}$, Q's, and $\overline{WE}$. The damping resistors should be determined by the first prototypes (not wire-wrapped due to the larger distributed capacitance and inductance). The best values for the damping resistors are the critical values giving a critically damped transition on the control outputs. Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading the higher the value. (For more information, see AN-305 "Precautions to Take When Driving Memories.")

Conditions for All Modes (Continued)

DP8409A DRIVING ANY 16k OR 64k DRAMs

The DP8409A can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8409A can drive all 16k DRAMs (see *Figure 1a*).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8409A can drive all three configurations, and at the same time allows them all to be interchangeable (as shown in *Figures 1b* and *1c*), providing maximum flexibility in the choice of DRAMs. Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2 ms (i.e. 256 rows in 4 ms) all DRAM types are correctly refreshed.

DP8409A Interface between System and DRAM Banks

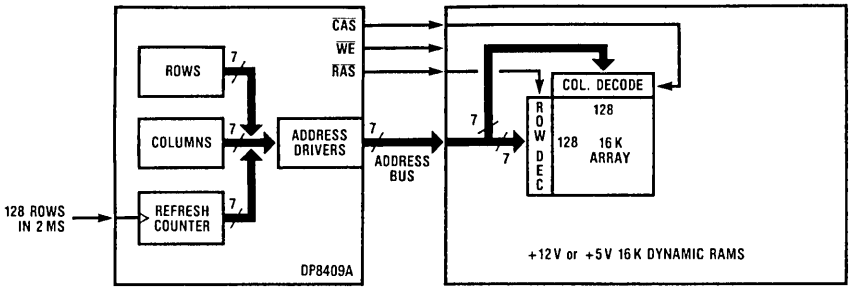

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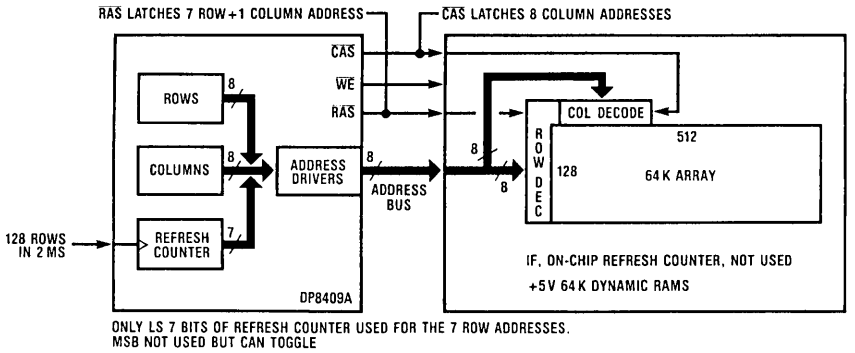
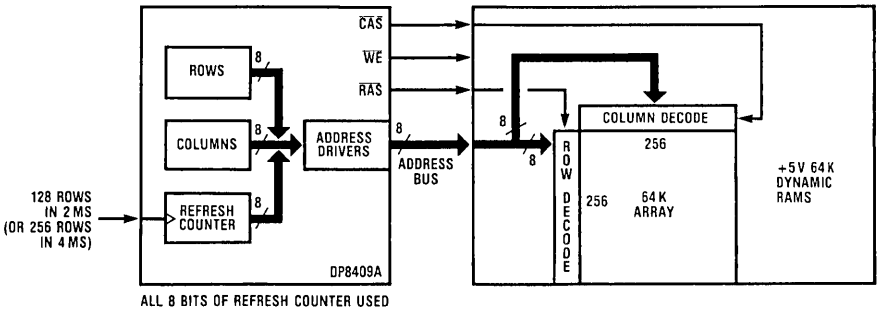
FIGURE 1a. DP8409A with any 16k DRAMs



ONLY LS 7 BITS OF REFRESH COUNTER USED FOR THE 7 ROW ADDRESSES.
MSB NOT USED BUT CAN TOGGLE

TL/F/8409–7

FIGURE 1b. DP8409A with 128 Row x 512 Column 64k DRAM



ALL 8 BITS OF REFRESH COUNTER USED

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FIGURE 1c. DP8409A with 256 x 256 Column 64k DRAM

Conditions for All Modes (Continued)

When the DP8409A is in a refresh mode, the RF I/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 512 to accommodate 16k, 64k or 256k DRAMs. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 before rolling over to zero.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

POWER-UP INITIALIZE

When V_{CC} is first applied to the DP8409A, an initialize pulse clears the refresh counter, the internal control flip-flops, and set the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3V, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to TRI-STATE. As V_{CC} increases above 2.3V, control of these outputs is granted to the system.

DP8409A Functional Mode Descriptions

Note: All delay parameters stated in text refer to the DP8409A. Substitute the respective delay numbers for the DP8409-2 or DP8409-3 when using these devices.

MODE 0—EXTERNALLY CONTROLLED REFRESH

Figure 2 is the Externally Controlled Refresh Timing. In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed. In the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $\overline{RFSH}$ goes low-to-high after a refresh. RF I/O goes low when the count is 127, 255, or 511, as set by End-of-Count (see Table III), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeros, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and RFSH must be skewed transitioning low such that the refresh address is valid on the address outputs of the controller before the $\overline{RAS}$ outputs go low. The amount of time that RFSH should go low before $\overline{RASIN}$ does depends on the capacitive loading of the address and $\overline{RAS}$ lines. For the load specified in the switching characteristics of this data sheet, 10 ns is sufficient. Refer to *Figure 2*.

To perform externally controlled burst refresh, $\overline{RASIN}$ is toggled while RFSH is held low. The refresh counter increments with $\overline{RASIN}$ going low to high, so that the DRAM rows are refreshed in succession by $\overline{RASIN}$ going high to low.

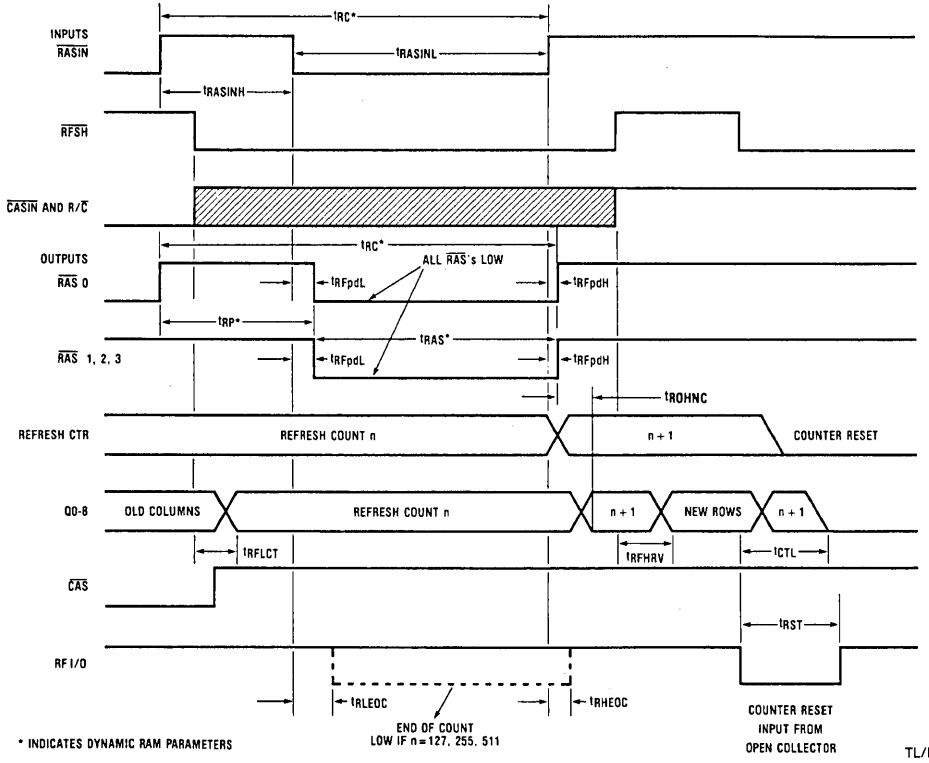

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FIGURE 2. External Control Refresh Cycle (Mode 0)

DP8409A Functional Mode Descriptions (Continued)

MODE 1—AUTOMATIC FORCED REFRESH

In Mode 1, the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock), instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high, then whenever M2 ($\overline{RFSH}$) goes low, an externally controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but when set low externally through an open-collector driver, the refresh counter resets as normal. This externally controlled method may be preferred when operating in the Automatic Access mode (Mode 5), where hidden or forced refreshing is undesirable, but refreshing is still necessary.

If RFCK is an input clock signal, one (and only one) refresh cycle must take place every RFCK cycle. Refer to *Figure 9*. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O ($\overline{Refresh\ Request}$) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is requested. The system must allow a forced refresh to take place while RFCK is low (refer to *Figure 3*). The $\overline{Refresh\ Request}$ signal on RF I/O may be connected to a $\overline{Hold}$ or $\overline{Bus\ Request}$ input to the system. The system acknowledges the $\overline{Hold}$ or $\overline{Bus\ Request}$ when ready, and outputs Hold Acknowledge or $\overline{Bus\ Request\ Acknowledge}$. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the DP8409A, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, to strobe the refresh counter contents on the address outputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock (RGCK) is required for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the next falling edge of RGCK. The $\overline{Refresh\ Request}$ on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may be high earlier than t_{RQHRF} after RGCK goes low and $\overline{RAS}$ will go high t_{RFRH} after M2, if $\overline{CS}$ is low. If $\overline{CS}$ is high, the $\overline{RAS}$ will go high after 25 ns after M2 goes high.

To allow the forced refresh, the system will have been inactive for about 4 periods of RGCK, which can be as fast as 400 ns every RFCK cycle. To guarantee a refresh of 128 rows every 2 ms, a period of up to 16 μs is required for RFCK. In other words, the system may be down for as little as 400 ns every 16 μs, or 2.5% of the time. Although this is not excessive, it may be preferable to perform a Hidden Refresh each RFCK cycle, which is allowed while still in the Auto-Access mode, (Mode 5).

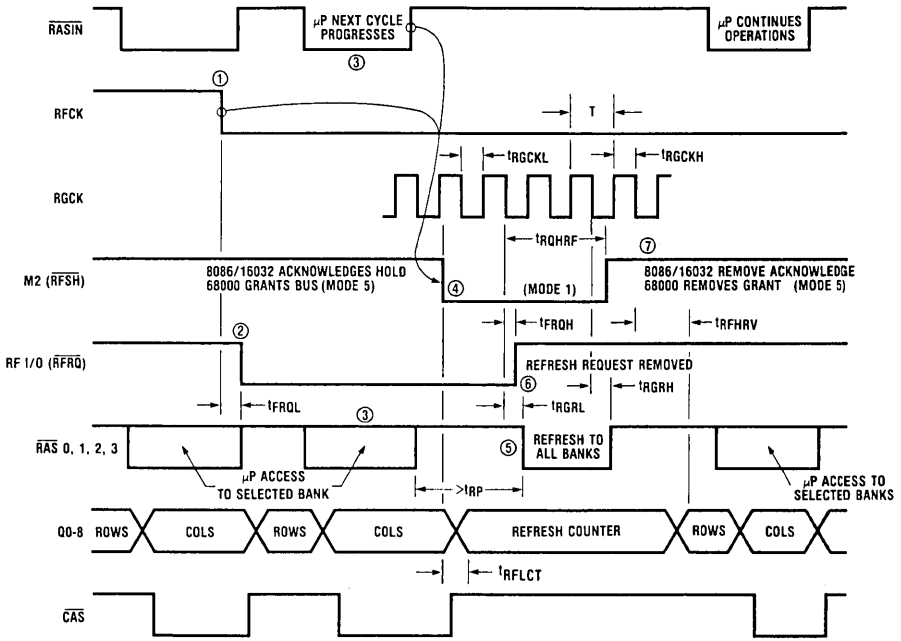

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FIGURE 3. DP8409A Performing a Forced Refresh (Mode 5 → 1 → 5) with Various Microprocessors

DP8409A Functional Mode Descriptions (Continued)

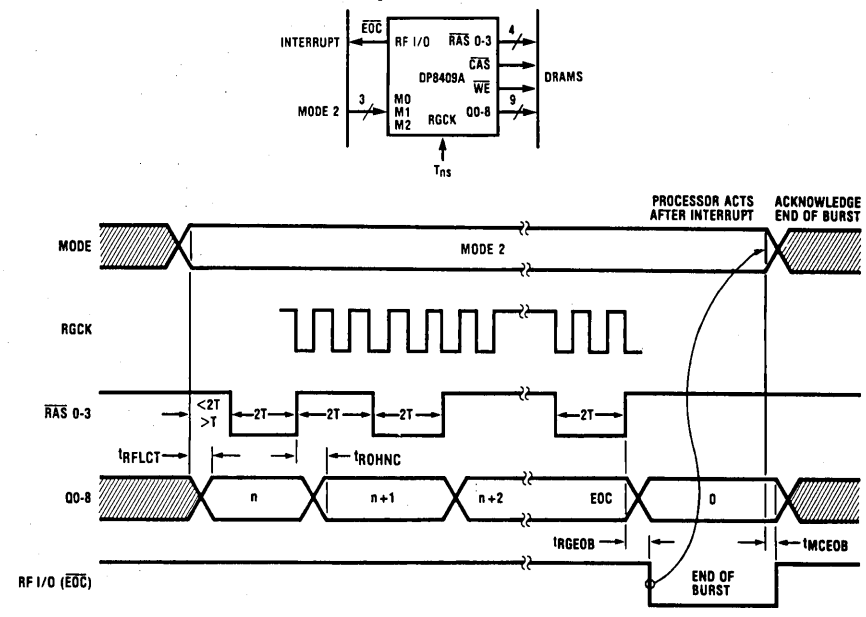

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FIGURE 4. Auto-Burst Mode, Mode 2

MODE 2—AUTOMATIC BURST REFRESH

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see *Figure 4*). When the DP8409A enters this mode, $\overline{\text{CASIN}}$ (RGCK) becomes the $\overline{\text{RAS}}$ Generator Clock (RGCK), and $\overline{\text{RASIN}}$ is disabled. $\overline{\text{CAS}}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{\text{RAS}}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst conditions.

The signal on all four $\overline{\text{RAS}}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{\text{RAS}}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{\text{RAS}}$, starting from the count it contained when the mode was entered. If this was zero, then for a RGCK with a 100 ns period with End-of-Count set to 127, RF I/O will go low after 128 × 0.4 μs, or 51.2 μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the DP8409A (set to Mode 2), causing it to perform a complete burst refresh. When end-of-burst occurs (after 26 μs), power can then be removed from the DP8409A for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the DP8409A.

MODE 3a—ALL-$\overline{\text{RAS}}$ AUTOMATIC WRITE

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeros in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{\text{RAS}}$ outputs are activated, as in refresh, and so are $\overline{\text{CAS}}$ and $\overline{\text{WE}}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations.

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16k DRAMs, B1 and B0 are 00. For 64k DRAMs, B1 and B0 are 01, so that for the configuration of *Figure 1b*, the 8 refresh counter bits are strobed by $\overline{\text{RAS}}$ into the 7 row addresses and the ninth column address. After this Automatic-Write process, B1 and B0 must be set again in Mode 7 to 00 to set End-of-Count to 127. For the configuration of *Figure 1c*, B1 and B0 set to 01 will work for Automatic-Write and End-of-Count equals 255.

In this mode, R/$\overline{\text{C}}$ is disabled, $\overline{\text{WE}}$ is permanently enabled low, and $\overline{\text{CASIN}}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{\text{RAS}}$ outputs are active.

Referring to *Figure 5a*, an external 8-bit counter (for 64k DRAMs) with TRI-STATE outputs is required and must be connected to the column address inputs. It is enabled only during this mode, and is clocked from RF I/O. The DP8409A refresh counter is used to address the rows, and the column address is supplied by the external counter. Every row for each column address is written to in all four banks. At the End-of-Count RF I/O goes low, which clocks the external counter.

Therefore, for each column address, the refresh counter first outputs row-0 to the address bus and all four $\overline{\text{RAS}}$ outputs strobe this row address into the DRAMs (see *Figure 5b*). A minimum of 30 ns after $\overline{\text{RAS}}$ goes low (t_{RAH} = 30 ns), the refresh counter is disabled and the column ad-

DP8409A Functional Mode Descriptions (Continued)

dress input latch is enabled onto the address bus. About 14 ns after the column address is valid, $\overline{CAS}$ goes low, (t_{ASC} = +14 ns), strobing the column address into the DRAMs. When $\overline{RAS}$ and $\overline{CAS}$ go high the refresh counter increments to the next row and the cycle repeats. Since $\overline{WE}$ is kept low in this mode, the data at DI (input data) of the DRAMs is written into each row of the latched column. During each cycle $\overline{RAS}$ is high for two periods of RGCK and low for two periods, giving a total write-cycle time of 400 ns minimum, which is adequate for most 16k and 64k DRAMs. On the last row of a column, RF I/O increments the external counter to the next column address.

At the end of the last column address, an interrupt is generated from the external counter to let the system know that initialization has been completed. During the entire initialization time, the system can be performing other initialization functions. This approach to memory initialization is both automatic and fast. For instance, if four banks of 64k DRAMs are used, and RGCK is 100 ns, a write cycle to the same location in all four banks takes 400 ns, so the total time taken in initializing the 64k DRAMs is 65k × 400 ns or 26 ms. When the system receives the interrupt, the external counter must be permanently disabled. ADS and $\overline{CS}$ are interfaced by the system, and the DP8409A mode is changed. The interrupt must then be disabled.

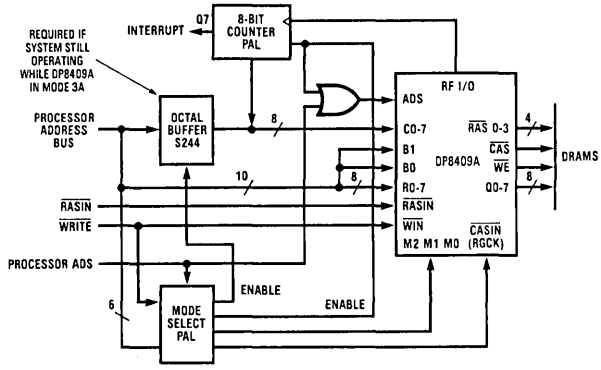

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FIGURE 5a. DP8409A Extra Circuitry Required for All-$\overline{RAS}$ Auto Write Mode, Mode 3a

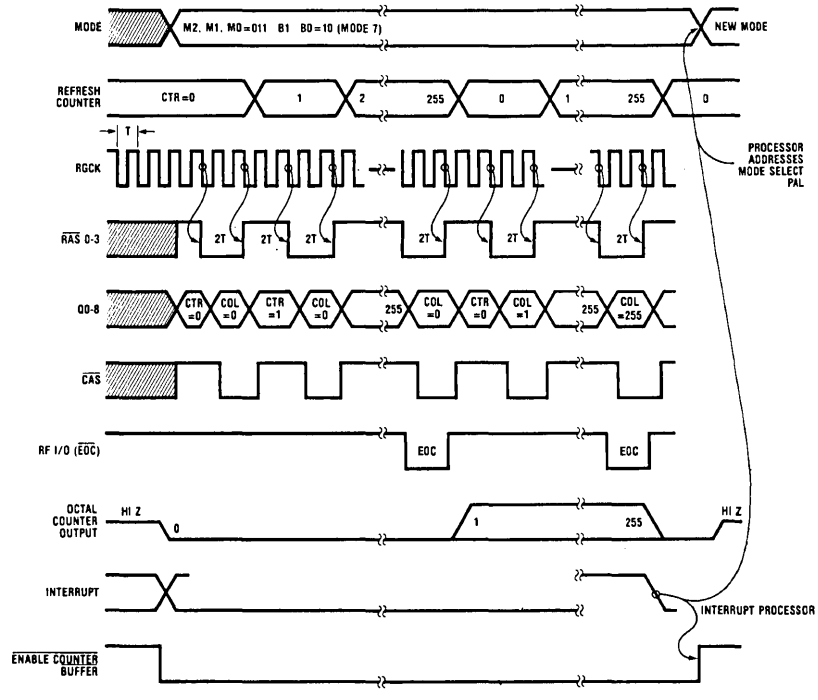

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FIGURE 5b. DP8409A All-$\overline{RAS}$ Auto Write Mode, Mode 3a, Timing Waveform

DP8409A Functional Mode Descriptions (Continued)

MODE 3b—EXTERNALLY CONTROLLED ALL-$\overline{RAS}$ WRITE

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the DP8409A for the next write cycle. This method is slower than Mode 3a since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

MODE 4—EXTERNALLY CONTROLLED ACCESS

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in *Figure 6*.

Output Address Selection

Refer to *Figure 7a*. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0–Q8, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0–Q8. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

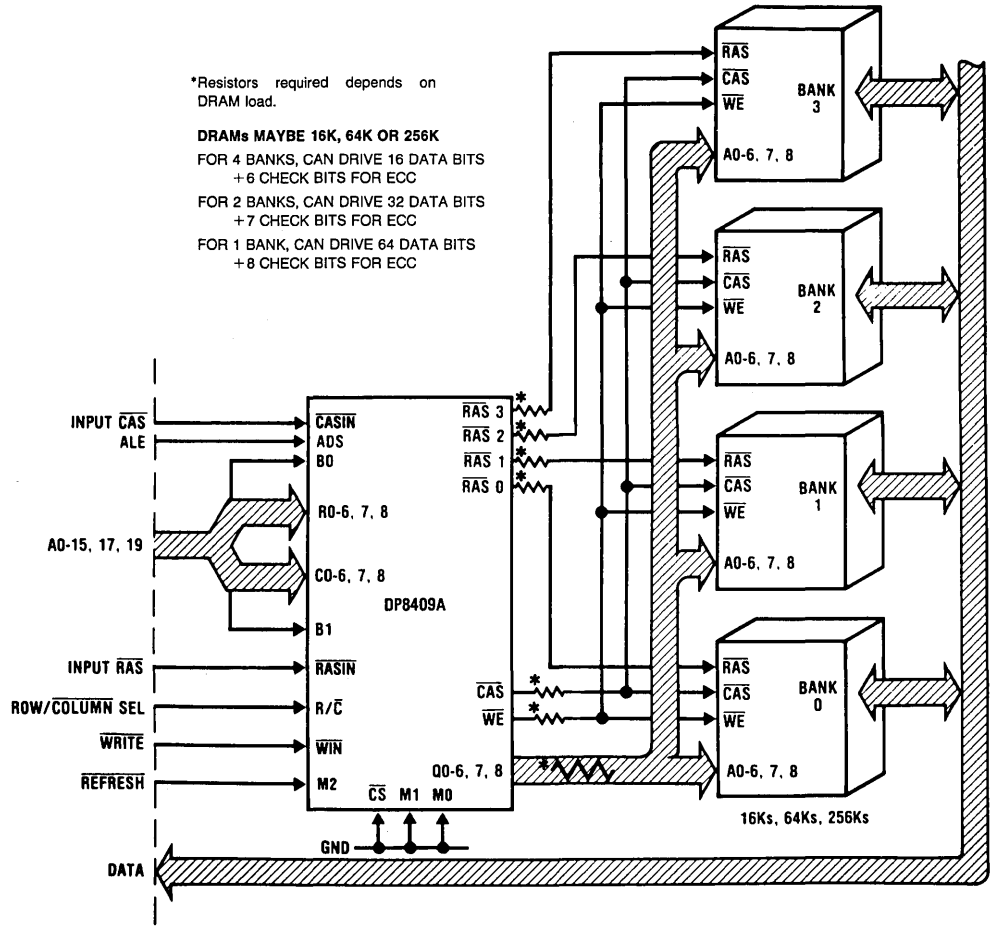

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FIGURE 6. Typical Application of DP8409A Using External Control Access and Refresh in Modes 0 and 4

DP8409A Functional Mode Descriptions (Continued)

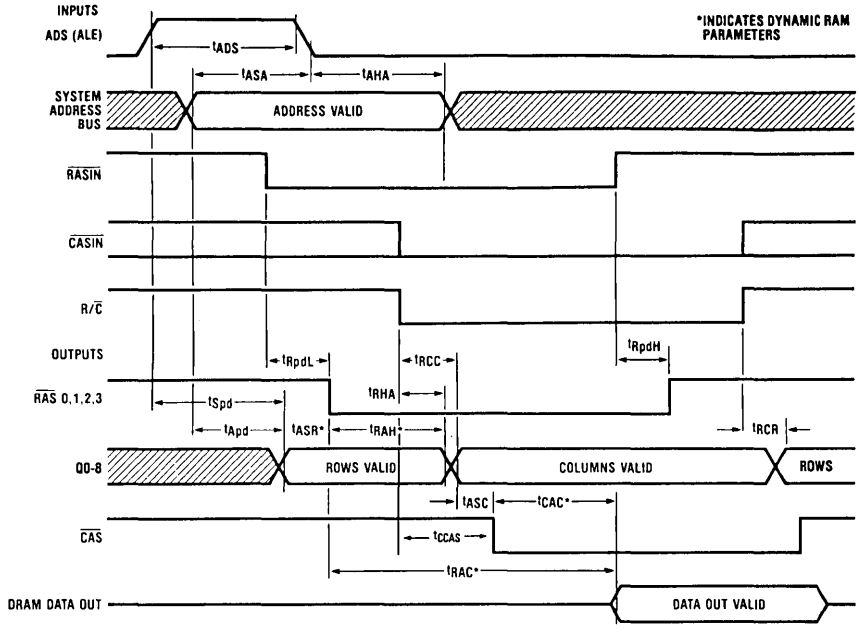

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FIGURE 7a. Read Cycle Timing (Mode 4)

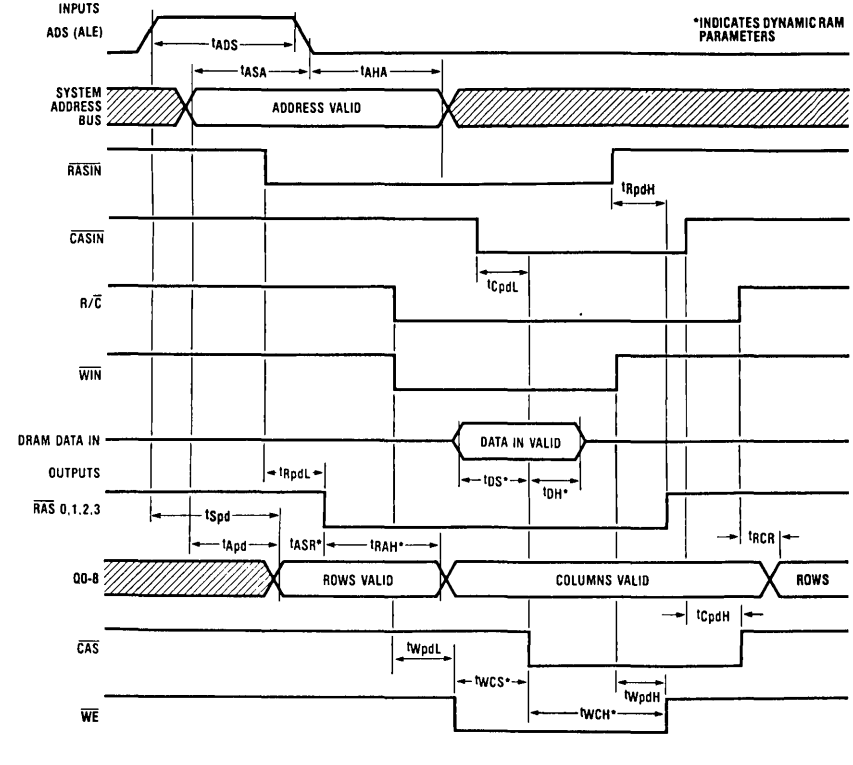

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FIGURE 7b. Write Cycle Timing (Mode 4)

DP8409A Functional Mode Descriptions (Continued)

Automatic CAS Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/C going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see *Figure 7b*). If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ will be automatically generated, following the row to column transition by about 20 ns (see *Figure 7a*). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe.

Fast Memory Access

AC parameters t_{DIF1}, t_{DIF2} may be used to determine the minimum delays required between $\overline{RASIN}$, R/$\overline{C}$, and $\overline{CASIN}$ (see Application Brief 9; "Fastest DRAM Access Mode").

MODE 5—AUTOMATIC ACCESS WITH HIDDEN REFRESH

The Auto Access with Hidden Refresh mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and can be used for other functions (see Refreshing, below). Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 (and Mode 6) of the DP8409A make DRAM accessing appear essentially "static".

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the DP8409A in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the DP8409A. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The DP8409A in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see *Figure 8a*).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typcial figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Refreshing

Because R/$\overline{C}$ and $\overline{CASIN}$ are not used in this mode, R/$\overline{C}$ becomes RFCK (refresh clock) and $\overline{CASIN}$ becomes RGCK ($\overline{RAS}$ generator clock). With these two signals it is possible to peform refreshing without extra ICs, and without holding up the processor.

One refresh cycle must occur during each refresh clock period and then the refresh address must be incremented to the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16k and 64k DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flip-flop. First the DP8409A will attempt to perform a hidden refresh so that the system throughput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the DP8409A goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the DP8409A will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flip-flop is reset so no further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK. Refer to *Figure 9*.

To determine the probability of a Hidden Refresh occurring, assume each system cycle takes 400 ns and RFCK is high for 8 μs, then the system has 20 chances to not select the DP8409A. If during this time a hidden refresh did not occur, then the DP8409A forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the DP8409A initiate a forced refresh (which is performed automatically). Refer to Mode 1, and *Figure 3*. The internal refresh request flip-flop is then reset.

Figure 9 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go TRI-STATE until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50-percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the DP8409A's forced-refresh request.

DP8409A Functional Mode Descriptions (Continued)

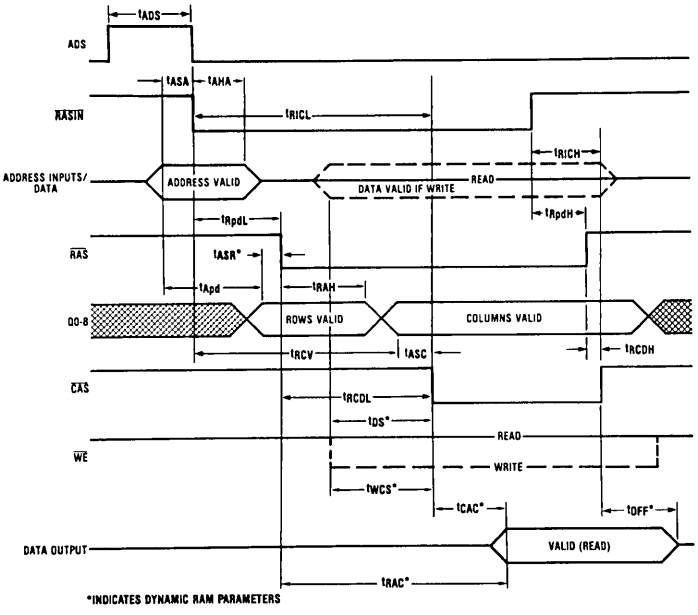

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FIGURE 8a. Modes 5, 6 Timing ($\overline{\text{CASIN}}$ High in Mode 6)

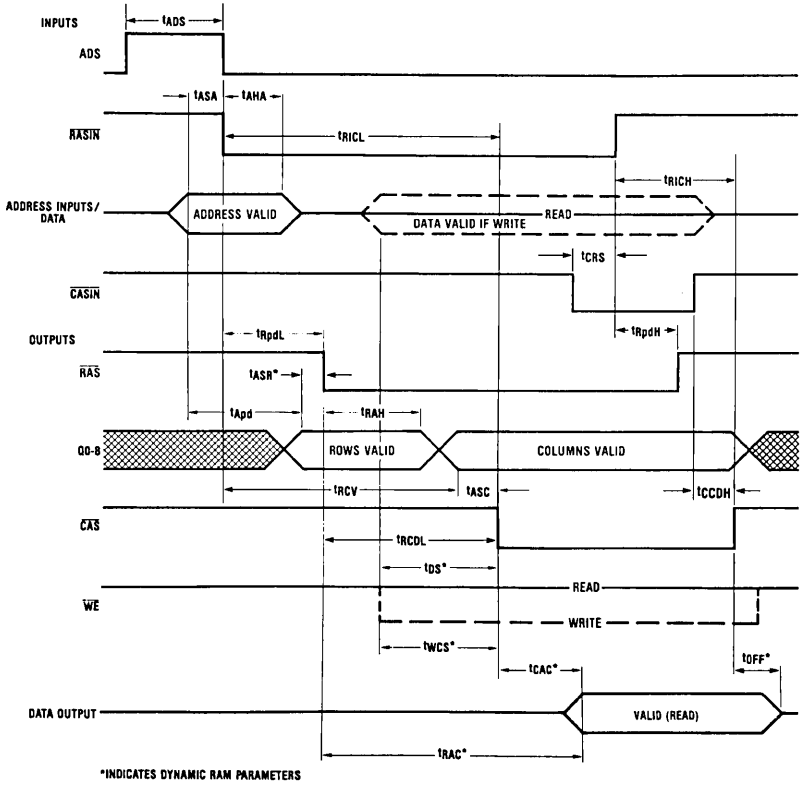

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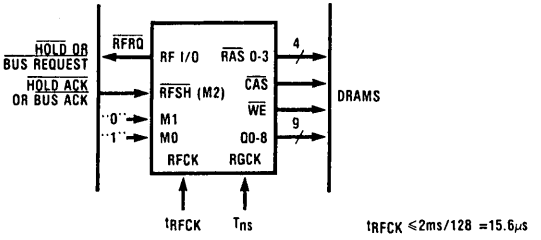
FIGURE 8b. Mode 6 Timing, Extended $\overline{\text{CAS}}$

DP8409A Functional Mode Descriptions (Continued)



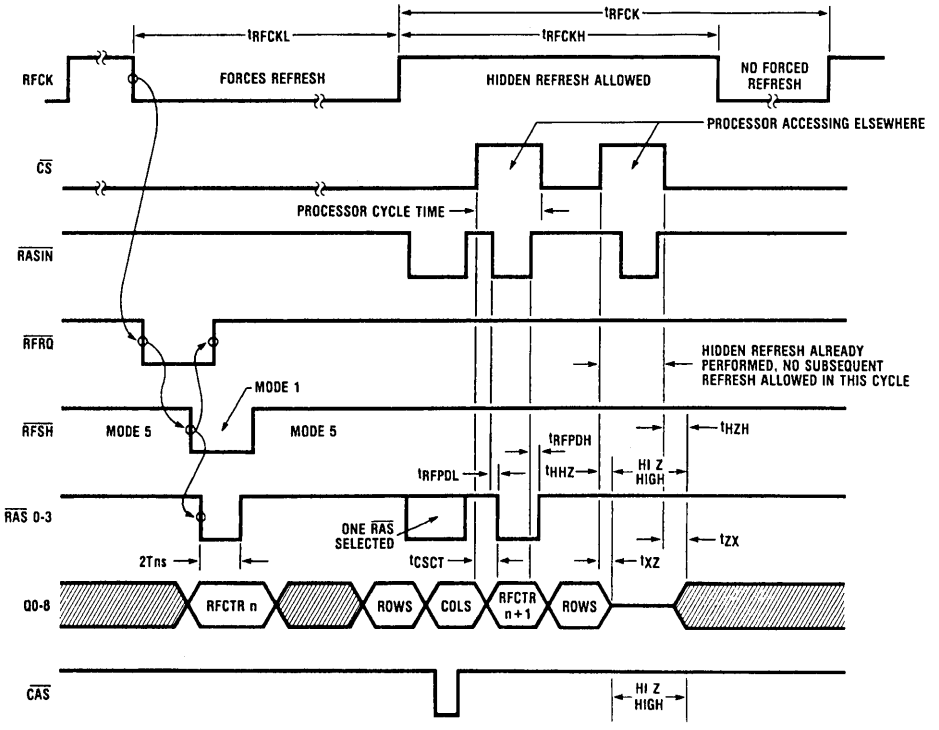


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FIGURE 9. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

DP8409A Functional Mode Descriptions (Continued)

TABLE II. Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Note that $\overline{RASIN}$ going low earlier than t_{CSRL} after $\overline{CS}$ goes low may result in the DP8409A interpreting the $\overline{RASIN}$ as a hidden refresh $\overline{RASIN}$ if no hidden refresh has occurred in the current RFCK cycle. In this case, all $\overline{RAS}$ outputs would go low for a short time. Thus, it is suggested that when using Mode 5, $\overline{RASIN}$ should be held high until t_{CSRL} after $\overline{CS}$ goes low if a refresh is not intended. Similarly, $\overline{CS}$ should be held low for a minimum of t_{CSRL} after $\overline{RASIN}$ returns high when ending the access in Mode 5.

MODE 6—FAST AUTOMATIC ACCESS

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to *Figure 8b*. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

There is no internal refresh-request flip-flop in this mode, so any refreshing required must be done by entering Mode 0 or Mode 2.

MODE 7—SET END-OF-COUNT

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table III). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

TABLE III. Mode 7

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

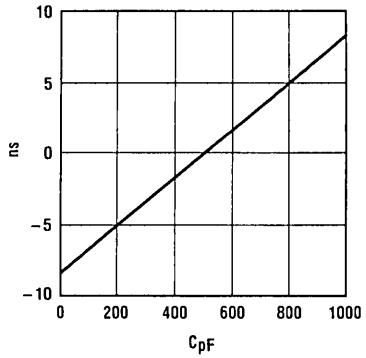

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FIGURE 10. Change in Propagation Delay vs. Loading Capacitance Relative to a 500 pF Load

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Maximum Power Dissipation* at 25°C	
Cavity Package	3542 mW
Molded Package	2833 mW

*Derate cavity package 23.6 mW/°C above 25°C; derate molded package 22.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.75	5.25	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 6)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min, I_C = −12 mA		−0.8	−1.2	V
I_{IH1}	Input High Current for ADS, R/$\overline{C}$ Only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input High Current for All Other Inputs*	V_{IN} = 2.5V		1.0	50	μA
I_I RSI	Output Load Current for RF I/O	V_{IN} = 0.5V, Output High		−1.5	−2.5	mA
I_I CTL	Output Load Current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, Chip Deselect		−1.5	−2.5	mA
I_{IL1}	Input Low Current for ADS, R/$\overline{C}$ Only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input Low Current for All Other Inputs*	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	I_{OL} = 20 mA		0.3	0.5	V
V_{OL2}	Output Low Voltage for RF I/O	I_{OL} = 10 mA		0.3	0.5	V
V_{OH1}	Output High Voltage*	I_{OH} = −1 mA	2.4	3.5		V
V_{OH2}	Output High Voltage for RF I/O	I_{OH} = − 100 μA	2.4	3.5		V
I_{1D}	Output High Drive Current*	V_{OUT} = 0.8V (Note 3)		−200		mA
I_{0D}	Output Low Drive Current*	V_{OUT} = 2.7V (Note 3)		200		mA
I_{OZ}	TRI-STATE Output Current (Address Outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, $\overline{CS}$ = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply Current	V_{CC} = Max		250	325	mA

*Except RF I/O Output.

Switching Characteristics: DP8409A/DP8409A-3

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409			8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
ACCESS									
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	95	125	160	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	80	105	140	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	40	48	60	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	50	63	80	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		98	125		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*		78	105		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8a*		40	65		40	65	ns

Switching Characteristics: DP8409A/DP8409A-3 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	DP8409A			DP8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
ACCESS (Continued)									
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8b*	40	54	70	40	54	80	ns
t_{RAH}	Row Address Hold Time (Mode 5)	*Figure 8a*	30			30			ns
t_{RAH}	Row Address Hold Time (Mode 6)	*Figures 8a, 8b*	20			20			ns
t_{ASC}	Column Address Setup Time (Mode 5)	*Figure 8a*	8			8			ns
t_{ASC}	Column Address Setup Time (Mode 6)	*Figures 8a, 8b*	6			6			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	*Figure 8a*		90	120		90	140	ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	*Figures 8a, 8b*		75	105		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 7a, 7b, 8a, 8b*	20	27	35	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 7a, 7b, 8a, 8b*	15	23	32	15	23	37	ns
t_{APDL}	Address Input to Output Low Delay	*Figures 7a, 7b, 8a, 8b*		25	40		25	46	ns
t_{APDH}	Address Input to Output High Delay	*Figures 7a, 7b, 8a, 8b*		25	40		25	46	ns
t_{SPDL}	Address Strobe to Address Output Low	*Figures 7a, 7b*		40	60		40	70	ns
t_{SPDH}	Address Strobe to Address Output High	*Figures 7a, 7b*		40	60		40	70	ns
t_{ASA}	Address Set-Up Time to ADS	*Figures 7a, 7b, 8a, 8b*	15			15			ns
t_{AHA}	Address Hold Time from ADS	*Figures 7a, 7b, 8a, 8b*	15			15			ns
t_{ADS}	Address Strobe Pulse Width	*Figures 7a, 7b, 8a, 8b*	30			30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 7b*	15	25	30	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 7b*	15	30	60	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ Set-Up Time to $\overline{RASIN}$ High (Mode 6)	*Figure 8b*	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	*Figure 7b*	32	41	68	32	41	77	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	*Figure 7b*	25	39	50	25	39	60	ns
t_{RCC}	Column Select to Column Address Valid	*Figure 7a*		40	58		40	67	ns
t_{RCR}	Row Select to Row Address Valid	*Figures 7a, 7b*		40	58		40	67	ns
t_{RHA}	Row Address Held from Column Select	*Figure 7a*	10			10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	*Figure 7a*		65	90				ns
t_{DIF1}	Maximum (t_{RPDL} − t_{RHA})	See Mode 4 Descrip.			13			18	ns
t_{DIF2}	Maximum (t_{RCC} − t_{CPDL})	See Mode 4 Descrip.			13			18	ns
REFRESH									
t_{RC}	Refresh Cycle Period	*Figure 2*	100			100			ns
$t_{RASINL, H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2*	50			50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figures 2, 9*	35	50	70	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figures 2, 9*	30	40	55	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, *Figures 2, 3, 4*		47	60		47	70	ns

Switching Characteristics: DP8409A/DP8409A-3 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	DP8409A			DP8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
REFRESH (Continued)									
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figures 2, 3*		45	60		45	70	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figures 2, 4*		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50 pF, *Figure 2*			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50 pF, *Figure 2*			80			80	ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	C_L = 50 pF, *Figure 4*			95			95	ns
t_{MCEOB}	Mode Change to End-of-Burst High	C_L = 50 pF, *Figure 4*			75			75	ns
t_{RST}	Counter Reset Pulse Width	*Figure 2*	70			70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	*Figure 2*			100			100	ns
$t_{RFCKL, H}$	Minimum Pulse Width of RFCK	*Figure 9*	100			100			ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	100			100			ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	35			40			ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	35			40			ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	C_L = 50 pF, *Figure 3*		20	30		20	30	ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	C_L = 50 pF, *Figure 3*		50	75		50	75	ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	50	65	95	50	65	95	ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	40	60	85	40	60	85	ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	*Figure 3*	2T			2T			ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (ending forced RFSH)	See Mode 1 Descrip.	55	80	110	55	80	125	ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-Up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35			40			ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	*Figure 9*		55	70		55	75	ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrip.	30			30			ns
TRI-STATE									
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	*Figures 9, 12,* R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	C_L = 15 pF, *Figures 9, 12,* R2 = 1k, S1 Open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	*Figures 9, 12,* R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15 pF, *Figures 9, 12,* R1 = 1k, S2 Open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	*Figures 9, 12,* R2 = 750Ω, S1 Open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15 pF, *Figures 9, 12,* R2 = 750Ω, S1 Open		40	75		40	75	ns

Switching Characteristics: DP8409A/DP8409A-3 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	DP8409A			DP8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
TRI-STATE (Continued)									
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	*Figure 12*, S1, S2 Open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15 pF, *Figure 12*, R2 = 750Ω, S1 Open		50	80		50	80	ns

Switching Characteristics: DP8409A-2

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409A-2			Units
			Min	Typ	Max	
ACCESS						
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8a*		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8b*	40	54	70	ns
t_{RAH}	Row Address Hold Time (Mode 5) (Note 7)	*Figure 8a*	20			ns
t_{RAH}	Row Address Hold Time (Mode 6) (Note 7)	*Figures 8a, 8b*	12			ns
t_{ASC}	Column Address Set-Up Time (Mode 5)	*Figure 8a*	3			ns
t_{ASC}	Column Address Set-Up Time (Mode 6)	*Figures 8a, 8b*	3			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	*Figure 8a*		80	105	ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	*Figures 8a, 8b*		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 7a, 7b, 8a, 8b*	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 7a, 7b, 8a, 8b*	15	23	32	ns
t_{APDL}	Address Input to Output Low Delay	*Figures 7a, 7b, 8a, 8b*		25	40	ns
t_{APDH}	Address Input to Output High Delay	*Figures 7a, 7b, 8a, 8b*		25	40	ns
t_{SPDL}	Address Strobe to Address Output Low	*Figures 7a, 7b*		40	60	ns
t_{SPDH}	Address Strobe to Address Output High	*Figures 7a, 7b*		40	60	ns
t_{ASA}	Address Set-Up Time to ADS	*Figures 7a, 7b, 8a, 8b*	15			ns
t_{AHA}	Address Hold Time from ADS	*Figures 7a, 7b, 8a, 8b*	15			ns
t_{ADS}	Address Strobe Pulse Width	*Figures 7a, 7b, 8a, 8b*	30			ns

Switching Characteristics: DP8409A-2 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409A-2			Units
			Min	Typ	Max	
ACCESS (Continued)						
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 7b*	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 7b*	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ Set-Up Time to $\overline{RASIN}$ High (Mode 6)	*Figure 8b*	35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	*Figure 7b*	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	*Figure 7b*	25	39	50	ns
t_{RCC}	Column Select to Column Address Valid	*Figure 7a*		40	58	ns
t_{RCR}	Row Select to Row Address Valid	*Figures 7a, 7b*		40	58	ns
t_{RHA}	Row Address Held from Column Select	*Figure 7a*	10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	*Figure 7a*		55	75	ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 Descript.			13	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 Descript.			13	ns
REFRESH						
t_{RC}	Refresh Cycle Period	*Figure 2*	100			ns
$t_{RASINL, H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2*	50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figures 2, 9*	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figures 2, 9*	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, *Figures 2, 3, 4*		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figures 2, 3*		45	60	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figures 2, 4*		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50 pF, *Figure 2*			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50 pF, *Figure 2*			80	ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	C_L = 50 pF, *Figure 4*			95	ns
t_{MCEOB}	Mode Change to End-of-Burst High	C_L = 50 pF, *Figure 4*			75	ns
t_{RST}	Counter Reset Pulse Width	*Figure 2*	70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	*Figure 2*			100	ns
$t_{RFCKL, H}$	Minimum Pulse Width of RFCK	*Figure 9*	100			ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	100			ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	35			ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	35			ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	C_L = 50 pF, *Figure 3*		20	30	ns

Switching Characteristics: DP8409A-2 (Continued)

V_{CC} = 5.0V ±5%, 0°C ≤ T_A ≤ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409A-2			Units
			Min	Typ	Max	
REFRESH (Continued)						
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	C_L = 50 pF, *Figure 3*		50	75	ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	50	65	95	ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	40	60	85	ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	*Figure 3*	2T			ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (Ending Forced RFSH)	See Mode 1 Descrip.	55	80	110	ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-Up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35			ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	*Figure 9*		55	70	ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrip.	30			ns
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	*Figures 9, 12,* R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	C_L = 15 pF, *Figures 9, 12,* R2 = 1k, S1 Open		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	*Figures 9, 12,* R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15 pF, *Figures 9, 12,* R1 = 1k, S2 Open		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	*Figures 9, 12,* R2 = 750Ω, S1 Open		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15 pF, *Figures 9, 12,* R2 = 750Ω, S1 Open		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	*Figure 12,* S1, S2 Open		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15 pF, *Figure 12,* R2 = 750Ω, S1 Open		50	80	ns

Input Capacitance T_A = 25°C (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing these parameters. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, t_R = t_F = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

Note 6: Applies to all DP8409A versions unless otherwise specified.

Note 7: The DP8409A-2 device can only be used with memory devices that meet the t_{RAH} specification indicated.

Applications

If external control is preferred, the DP8409A may be used in Mode 0 or 4, as in *Figure 6*.

If basic auto access and refresh are required, then in cases where the user requires the minimum of external complexity, Modes 1 and 5 are ideal, as shown in *Figure 13a*. The DP843X2 is used to provide proper arbitration between memory access and refresh. This chip supplies all the necessary control signals to the processor as well as the DP8409A. Furthermore, two separate $\overline{CAS}$ outputs are also included for systems using byte-writing. The refresh clock RFCK may be divided down from either RGCK using an IC counter such as the DM74LS393 or better still, the DP84300 Programmable Refresh Timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on the input clock of 2 to 10 MHz. *Figure 13b* shows the general timing diagram for interfacing the DP8409A to different microprocessors using the interface controller DP843X2.

If the system is complex, requiring automatic access and refresh, burst refresh, and all-banks auto-write, then more circuitry is required to select the mode. This may be accomplished by utilizing a PAL®. The PAL has two functions. One as an address comparator, so that when the desired port address occurs (programmed in the PAL), the comparator gates the data into a latch, where it is connected to the mode pins of the DP8409A. Hence the mode of the DP8409A can be changed as desired with one PAL chip merely by addressing the PAL location, and then outputting data to the mode-control pins. In this manner, all the automatic modes may be selected, assigning R/C as RFCK always, and $\overline{CASIN}$ as RGCK always. The output from RF I/O may be used as End-of-Count to an interrupt, or $\overline{Refresh\ Request}$ to $\overline{HOLD}$ or $\overline{BUS\ REQUEST}$. A complex system may use Modes 5 and 1 for automatic access and refresh, Modes 3a and 7 for system initialization, and Mode 2 (auto-burst refresh) before and after DMA.

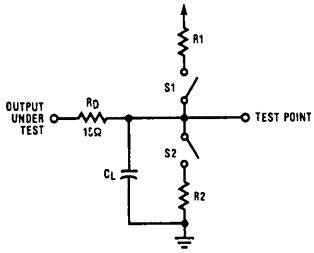

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FIGURE 11. Output Load Circuit

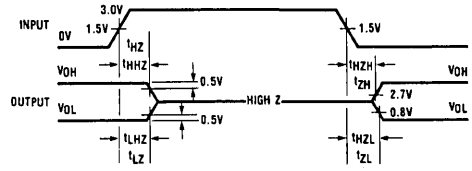

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FIGURE 12. Waveform

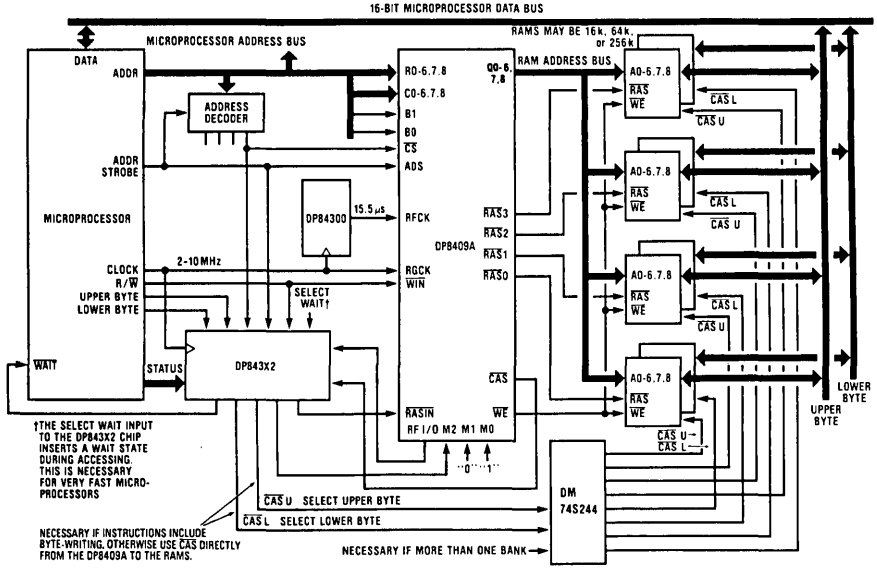

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FIGURE 13a. Connecting the DP8409A Between the 16-Bit Microprocessor and Memory

Applications (Continued)

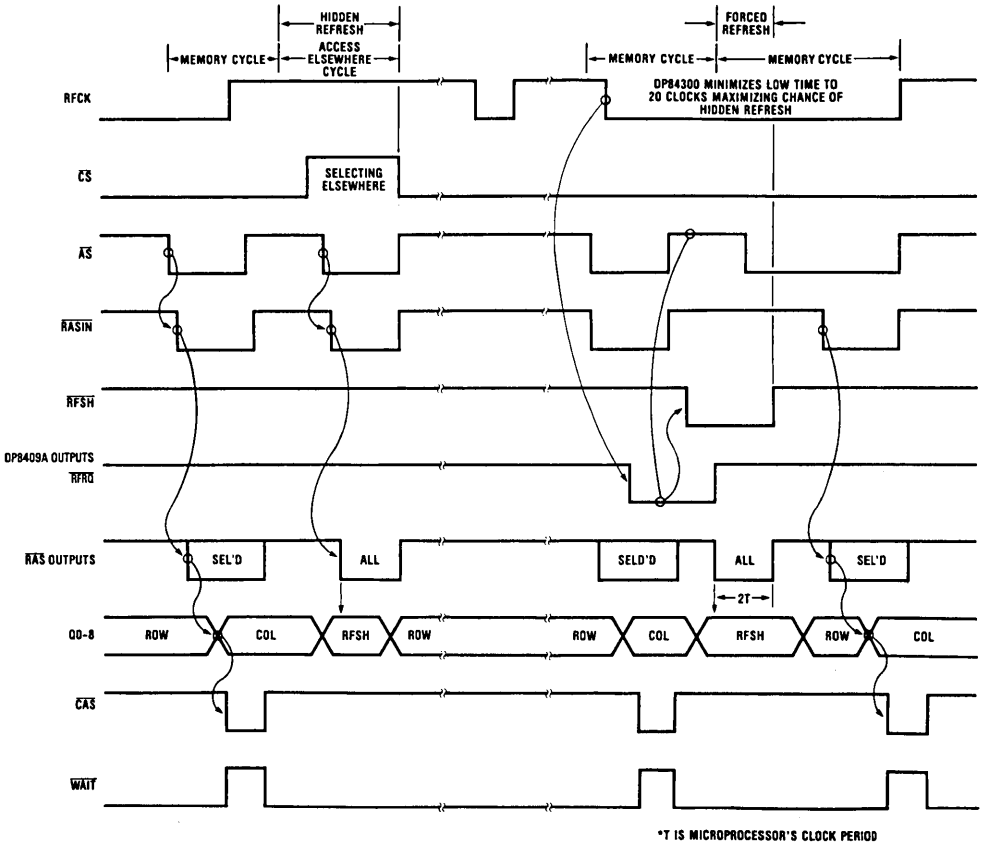

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FIGURE 13b. DP8409A Auto Refresh

National Semiconductor Corporation

PRELIMINARY

DP8417/NS32817, 8418/32818, 8419/32819, 8419X/ 32819X 64k, 256k Dynamic RAM Controller/Drivers

General Description

The DP8417/8418/8419/8419X represent a family of 256k DRAM Controller/Drivers which are designed to provide "No-Waitstate" CPU interface to Dynamic RAM arrays of up to 2 Mbytes and larger. Each device offers slight functional variations of the DP8419 design which are tailored for different system requirements. All family members are fabricated using National's new oxide isolated Advanced Low power Schottky (ALS) process and use design techniques which enable them to significantly out-perform all other LSI or discrete alternatives in speed, level of integration, and power consumption.

Each device integrates the following critical 256k DRAM controller functions on a single monolithic device: ultra precise delay line; 9-bit refresh counter; fall-through row, column, and bank select input latches; Row/Column address muxing logic; on-board high capacitive-load $\overline{RAS}$, $\overline{CAS}$, and Write Enable & Address output drivers; and, precise control signal timing for all the above.

There are four device options of the basic DP8419 Controller. The DP8417 is pin and function compatible with the DP8419 except that its outputs are TRI-STATE®. The DP8418 changes one pin and is specifically designed to offer an optimum interface to 32 bit microprocessors. The DP8419X is functionally identical to the DP8419, but is available in a 52-pin DIP package which is upward pin compatible with National's new DP8429D 1 Mbit DRAM Controller/ Driver.

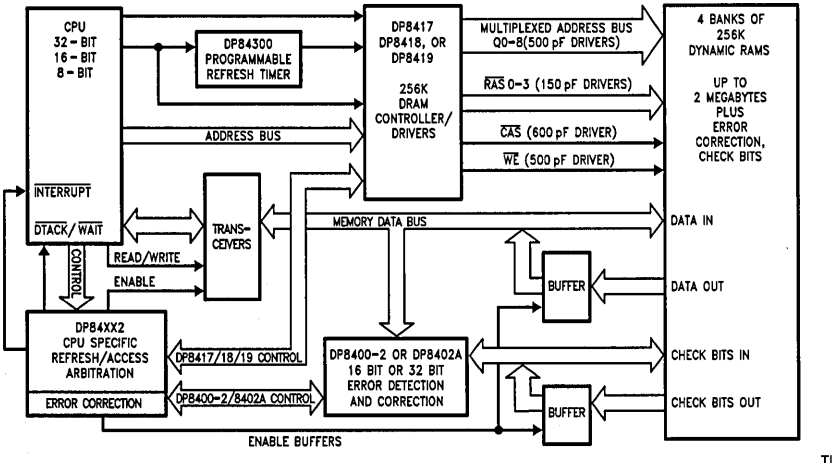
Each device is available in plastic DIP, Ceramic DIP, and Plastic Chip Carrier (PCC) packaging. (Continued)

Operational Features

- Makes DRAM Interface and refresh tasks appear virtually transparent to the CPU, making DRAMs as easy to use as static RAMs
- Specifically designed to eliminate CPU wait states up to 10 MHz or beyond
- Eliminates 15 to 20 SSI/MSI components for significant board real estate reduction, system power savings and the elimination of chip-to-chip AC skewing
- On-board ultra precise delay line
- On-board high capacitive $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and address drivers (specified driving 88 DRAMs directly)
- AC specified for directly addressing up to 8 Megabytes
- Low power/high speed bipolar oxide isolated process
- Upward pin and function compatible with new DP8428/ DP8429 1 Mbit DRAM controller drivers
- Downward pin and function compatible with DP8408A/ DP8409A 64k/256k DRAM controller/drivers
- 4 user selectable modes of operation for Access and Refresh (2 automatic, 2 external)

Contents

System Diagram



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General Description (Continued)

In order to specify each device for "true" worst case operating conditions, all timing parameters are guaranteed while the chip is driving the capacitive load of 88 DRAMs including trace capacitance. The chip's delay timing logic makes use of a patented new delay line technique which keeps A.C. skew to ±3 ns over the full V_{CC} range of ±10% and temperature range of −55°C to +125°C. The DP8417, DP8418, DP8419, and DP8419X guarantee a maximum $\overline{\text{RASIN}}$ to CASOUT delay of 80 ns or 70 ns even while driving a 2 Mbyte memory array with error correction check bits included. Speed selected options of these devices are shown in the switching characteristics section of this document.

With its four independent $\overline{\text{RAS}}$ outputs and nine multiplexed address outputs, the DP8419 can support up to four banks of 16k, 64k or 256k DRAMs. Two bank select pins, B1 and B0, are decoded to activate one of the $\overline{\text{RAS}}$ signals during an access, leaving the three non-selected banks in the standby mode (less than one tenth of the operating power) with data outputs in TRI-STATE.

The DP8419 has two mode-select pins, allowing for two refresh modes and two access modes. Refresh and access timing may be controlled either externally or automatically. The automatic modes require a minimum of input control signals.

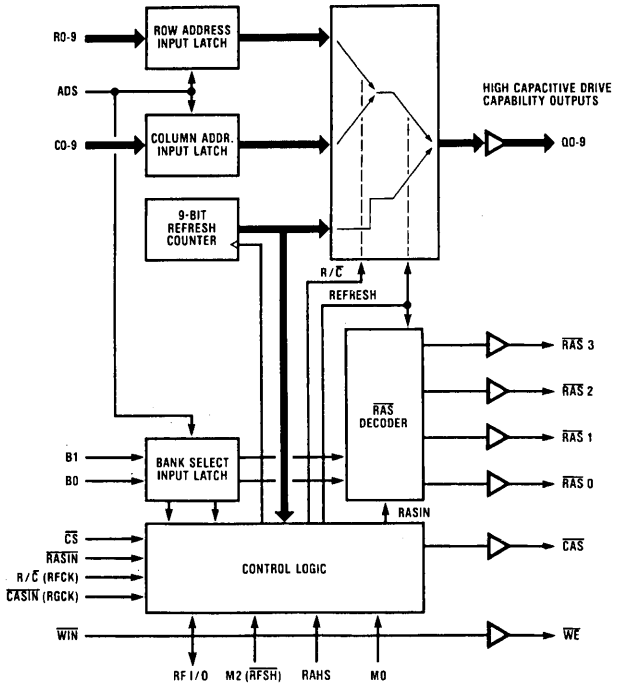
A refresh counter is on-chip and is multiplexed with the row and column inputs. Its contents appear at the address outputs of the DP8419 during any refresh, and are incremented at the completion of the refresh. Row/Column and bank address latches are also on-chip. However, if the address inputs to the DP8419 are valid throughout the duration of the access, these latches may be operated in the fall-through mode.

System Companion Components

Device #	Function
DP84300	Programmable Refresh Timer for DP84xx DRAM Controller
DP84412	NS32008/16/32 to DP8409A/17/18/19/28/29 Interface
DP84512	NS32332 to DP8417/18/19/28/29 Interface
DP84322	68000/08/10 to DP8409A/17/18/19/28/29 Interface (up to 8 MHz)
DP84422	68000/08/10 to DP8409A/17/18/19/28/29 Interface (up to 12.5 MHz)
DP84522	68020 to DP8417/18/19/28/29 Interface
DP84432	8086/88/186/188 to DP8409A/17/18/19/28/29 Interface
DP84532	80286 to DP8409A/17/18/19/28/29 Interface
DP8400-2	16-bit Expandable Error Checker/Corrector
DP8400-4	16-bit Expandable Error Checker/Corrector
DP8402A	32-bit Error Detector and Corrector (EDAC)

Block Diagrams

DP8417, 8419 and 8419X



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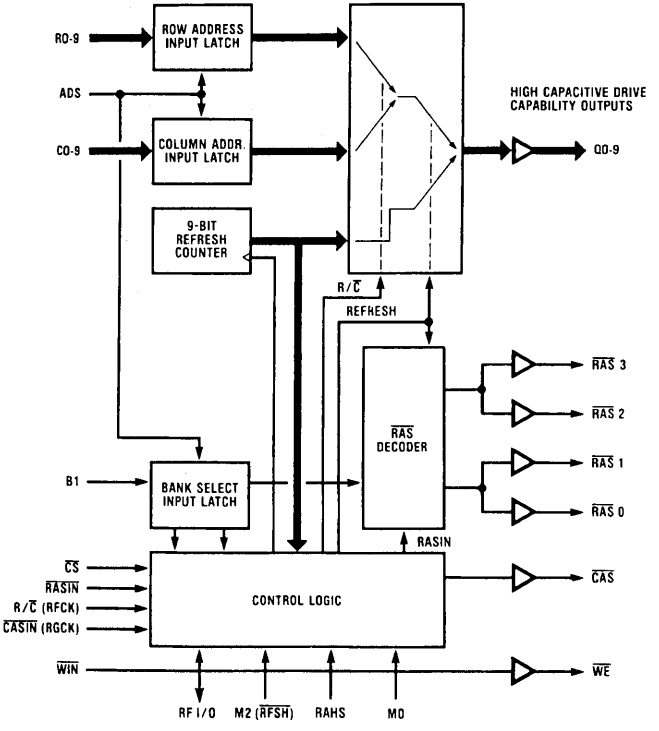
DP8418



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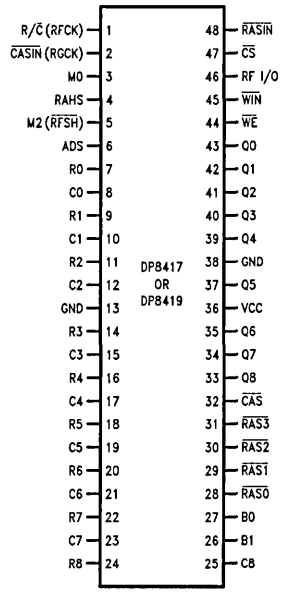
Connection Diagrams (Dual-In-Line Package)



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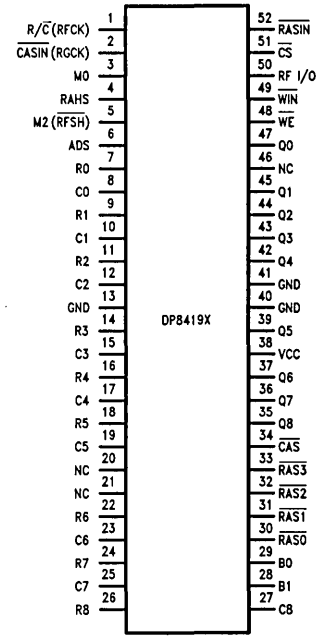

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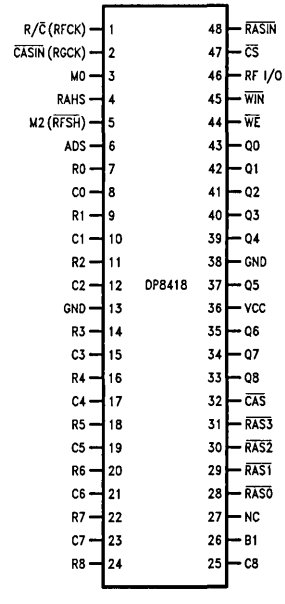

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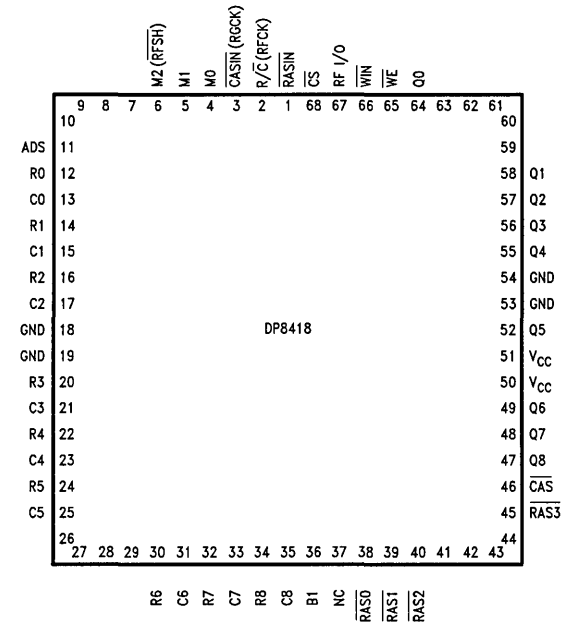
Order Number DP8417D-70, DP8417D-80, DP8417N-70, DP8417N-80, DP8418D-70, DP8418D-80, DP8418N-70, DP8418N-80, DP8419D-70, DP8419D-80, DP8419N-70, DP8419N-80, DP8419XD-70 or DP8419XD-80.

See NS Package Number D48A, D52A, or N48A

Connection Diagrams (Continued)

Plastic Chip Carrier Package



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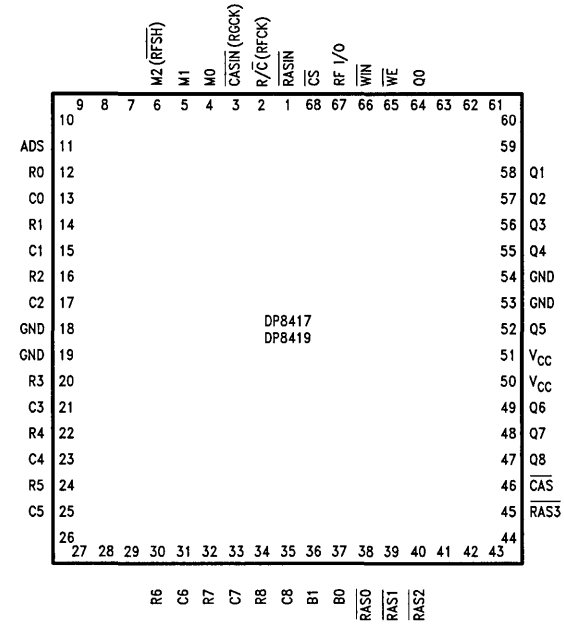
Plastic Chip Carrier Package



TL/F/8396–32

Order Number DP8417V-70, DP8417V-80, DP8418V-70, DP8418V-80, DP8419V-70 or DP8419V-80
See NS Package Number V68A

Family Device Differences

DP8417 vs DP8419

The DP8417 is identical to the DP8419 with the exception that its $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Q (Multiplexed Address) outputs are TRI-STATE when $\overline{CS}$ (Chip Select) is high and the chip is not in a refresh mode. This feature allows access to the same DRAM array through multiple DRAM Controller/Driver DP8417s. All AC specifications are the same as the DP8419 except t_{CSRLO} which is 34 ns for the DP8417 versus 5 ns for the DP8419. Separate delay specifications for the TRI-STATE timing paths are provided in the AC tables of this data sheet.

DP8418 vs DP8419

The DP8418 DYNAMIC RAM CONTROLLER/DRIVER is identical to the DP8419 with the exception of two functional differences incorporated to improve performance with 32-bit microprocessors.

1) Pin 26 (B1) is used to enable/disable a pair of $\overline{RAS}$ outputs, and pin 27 (B0 on the DP8419) is a no connect. When B1 is low, $\overline{RAS}$0 and $\overline{RAS}$1 are enabled such that they both go low during an access. When B1 is high, $\overline{RAS}$2 and $\overline{RAS}$3 are enabled. This feature is useful when driving words to 32 bits or more since each $\overline{RAS}$ would be driving only one half of the word. By distributing the load on each $\overline{RAS}$ line in this way, the DP8418 will meet the same AC specifications driving 2 banks of 32 DRAMs each as the DP8419 does driving 4 banks of 16 bits each.
2) The hidden refresh function available on the DP8419 has been disabled in order to reduce the amount of setup time necessary from $\overline{CS}$ going low to $\overline{RASIN}$ going low during an access of DRAM. This parameter, called t_{CSRL1}, is 5 ns for the DP8418 whereas it is 34 ns for the DP8419. The hidden refresh function only allows a very small increase in system performance, at best, at microprocessor frequencies of 10 MHz and above.

DP8419 vs DP8409A

The DP8419 High Speed DRAM Controller/Driver combines the most popular memory control features of the DP8408A/9A DRAM Controller/Driver with the high speed of bipolar oxide isolation processing.

The DP8419 retains the high capacitive-load drive capability of the DP8408A/9A as well as its most frequently used access and refresh modes, allowing it to directly replace the DP8408A/9A in applications using only modes 0, 1, 4 and 5. Thus, the DP8419 will allow most DP8408A/9A users to directly upgrade their system by replacing their old controller chip with the DP8419.

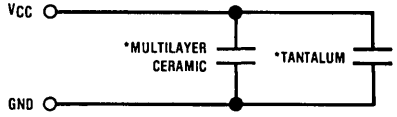
The highest priority of the DP8419 is speed. By peforming the DRAM address multiplexing, control signal timing and high-capacitive drive capability on a single chip, propagation delay skews are minimized. Emphasis has been placed on reducing delay variation over the specified supply and temperature ranges.

Except for the following, a DP8419 will operate essentially the same as a DP8409A.

1) The DP8419 has significantly faster AC performance.
2) The DP8419 can replace the DP8409A in applications which use modes 0, 1, 4, and 5. Modes 2, 3, 6, and 7 of the DP8409A are not available on the DP8419.
3) Pin 4 on the DP8419 is RAHS instead of M1, as on the DP8409A, and allows for two choices of t_{RAH} in mode 5.
4) RFI/O does not function as an end-of-count signal in Mode 0 on the DP8419 as it does on the DP8409A.
5) DP8419 address and control outputs do not TRI-STATE when $\overline{CS}$ is high as on the DP8409A. DP8419 control outputs are active high when $\overline{CS}$ is high (unless refreshing).

Pin Definitions

V_{CC}, GND, GND – V_{CC} = 5V ±10%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to V_{CC} and GND to reduce lead inductance. See Figure below.



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*Capacitor values should be chosen depending on the particular application.

R0–R8: Row Address Inputs.

C0–C8: Column Address Inputs.

Q0–Q8: Multiplexed Address Outputs - This address is selected from the Row Address Input Latch, the Column Address Input Latch or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input - $\overline{RASIN}$ directly controls the selected $\overline{RAS}$ output when in an access mode and all $\overline{RAS}$ outputs during hidden or external refresh.

R/$\overline{C}$ (RFCK) - In the auto-modes this pin is the external refresh clock input; one refresh cycle should be performed each clock period. In the external access mode it is Row/Column Select Input which enables either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK) - In the auto-modes this pin is the $\overline{RAS}$ Generator Clock input. In external access mode it is the Column Address Strobe input which controls $\overline{CAS}$ directly once columns are enabled on the address outputs.

ADS: Address (Latch) Strobe Input - Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; latching occurs on high-to-low transition of ADS.

$\overline{CS}$: Chip Select Input - When high, $\overline{CS}$ disables all accesses. Refreshing, however, in both modes 0 and 1 is not affected by this pin.

M0, M2 ($\overline{RFSH}$): Mode Control Inputs - These pins select one of the four available operational modes of the DP8419 (see Table III).

RFI/O: Refresh Input/Output - In the auto-modes this pin is the Refresh Request Output. It goes low following RFCK

Pin Definitions (Continued)

indicating that no hidden refresh was performed while RFCK was high. When this pin is set low by an external gate the on-chip refresh counter is reset to all zeroes.

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output - $\overline{WE}$ follows $\overline{WIN}$ unconditionally.

RAHS: Row Address Hold Time Select - Selects the t_{RAH} to be generated by the DP8419 delay line to allow use with fast or slow DRAMs.

$\overline{CAS}$: Column Address Strobe Output - In mode 5 and in mode 4 with $\overline{CASIN}$ low before R/$\overline{C}$ goes low, $\overline{CAS}$ goes low automatically after the column address is valid on the address outputs. In mode 4 $\overline{CAS}$ follows $\overline{CASIN}$ directly after R/$\overline{C}$ goes low, allowing for nibble accessing. $\overline{CAS}$ is always high during refresh.

$\overline{RAS}$ 0–3: Row Address Strobe Outputs - The enabled $\overline{RAS}$ output (see Table II) follows $\overline{RASIN}$ directly during an access. During refresh, all $\overline{RAS}$ outputs are enabled.

B0, B1: Bank Select Inputs - These pins are decoded to enable one of the four $\overline{RAS}$ outputs during an access (see Table I and Table II).

TABLE I. DP8417, DP8419, DP8419X Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

TABLE II. DP8418 Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	NC	
0	X	$\overline{RAS}_0$ and $\overline{RAS}_1$
1	X	$\overline{RAS}_2$ and $\overline{RAS}_3$

Conditions for All Modes

INPUT ADDRESSING

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after $\overline{CAS}$ goes low at the end of the memory cycle, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

DRIVE CAPABILITY

The DP8419 has timing parameters that are specified driving the typical capacitance (including traces) of 88, 5V-only DRAMs. Since there are 4 $\overline{RAS}$ outputs, each is specified driving one-fourth of the total memory. $\overline{CAS}$, $\overline{WE}$ and the address outputs are specified driving all 88 DRAMs.

The graph in *Figure 10* may be used to determine the slight variations in timing parameters, due to loading conditions other than 88 DRAMs.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To reduce these spikes, a damping resistor (low inductance, carbon) should be inserted between the DP8419 outputs and the DRAMs, as close as possible to the DP8419. The damping resistor values may differ depending on how heavily an output is loaded. These resistors should be determined by the first prototypes (not wire-wrapped due to the larger distributed capacitance and inductance). Resistors should be chosen such that the transition on the control outputs is critically damped. Typical values will be from 15Ω to 100Ω, with the lower values being used with the larger memory arrays. Note that AC parameters are specified with 15Ω damping resistors. For more information see AN-305 "Precautions to Take When Driving Memories".

DP8419 DRIVING ANY 16k, 64k or 256k DRAMs

The DP8419 can drive any 16k, 64k or 256k DRAMs. All 16k DRAMs use basically the same configuration, including the 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8419 can drive them all (see *Figure 1a*).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8419 can drive all three configurations, and allows them all to be interchangeable (as shown in *Figures 1b* and *1c*), providing maximum flexibility in the choice of DRAMs. Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter, if present, is never used.

256k DRAMs require all 18 of the DP8419's address inputs to select one memory location within the DRAM. $\overline{RAS}$-only refreshing with the nine-bit refresh-counter on the DP8419 makes $\overline{CAS}$ before $\overline{RAS}$ refreshing, available on 256k DRAMs, unnecessary.

READ, WRITE AND READ-MODIFY-WRITE CYCLES

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid, then data DI is written into the same address in the DRAM as $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. $\overline{WE}$ always follows $\overline{WIN}$ directly to determine the type of access to be performed.

POWER-UP INITIALIZE

When V_{CC} is first applied to the DP8419, an initialize pulse clears the refresh counter and the internal control flip-flops.

Mode Features Summary

- 4 modes of operation: 2 access and 2 refresh
- Automatic or external control selected by the user
- Auto access mode provides $\overline{RAS}$, row to column change, and then $\overline{CAS}$ automatically
- Choice between two different values of t_{RAH} in auto-access mode
- $\overline{CAS}$ controlled independently in external control mode, allowing for nibble mode accessing
- Automatic refreshing can make refreshes transparent to the system
- $\overline{CAS}$ is inhibited during refresh cycles

DP8419 Mode Descriptions

MODE 0–EXTERNALLY CONTROLLED REFRESH

Figure 2 shows the Externally Controlled Refresh timing. In this mode the refresh counter contents are multiplexed to the address outputs. All $\overline{RAS}$ outputs are enabled to follow $\overline{RASIN}$ so that the row address indicated by the refresh counter is refreshed in all DRAM banks when $\overline{RASIN}$ goes low. The refresh counter increments when $\overline{RASIN}$ goes high. $\overline{RFSH}$ should be held low at least until $\overline{RASIN}$ goes high (they may go high simultaneously) so that the refresh address remains valid and all $\overline{RAS}$ outputs remain enabled throughout the refresh.

A burst refresh may be performed by holding $\overline{RFSH}$ low and toggling $\overline{RASIN}$ until all rows are refreshed. It may be useful in this case to reset the refresh counter just prior to beginning the refresh. The refresh counter resets to all zeroes when RFI/O is pulled low by an external gate. The refresh counter always counts to 511 before rolling over to zero. If there are 128 or 256 rows being refreshed then Q7 or Q8, respectively, going high may be used as an end-of-burst indicator.

In order that the refresh address is valid on the address outputs prior to the $\overline{RAS}$ lines going low, $\overline{RFSH}$ must go low before $\overline{RASIN}$. The setup time required is given by t_{RFLRL} in the Switching Characteristics. This parameter may be adjusted using *Figure 10* for loading conditions other than those specified.

TABLE III. DP8419 Mode Select Options

Mode	($\overline{RFSH}$) M2	M0	Mode of Operation
0	0	0	Externally Controlled Refresh
1	0	1	Auto Refresh–Forced
4	1	0	Externally Controlled Access
5	1	1	Auto Access (Hidden Refresh)

DP8419 Mode Descriptions (Continued)

DP8419 Interface Between System & DRAM Banks

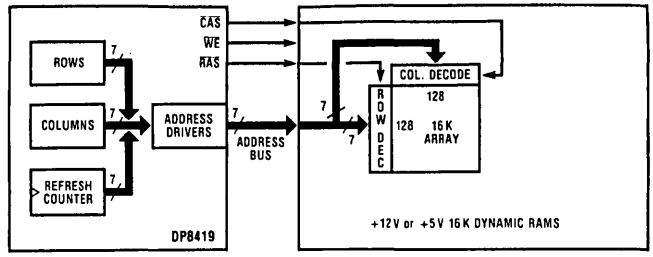

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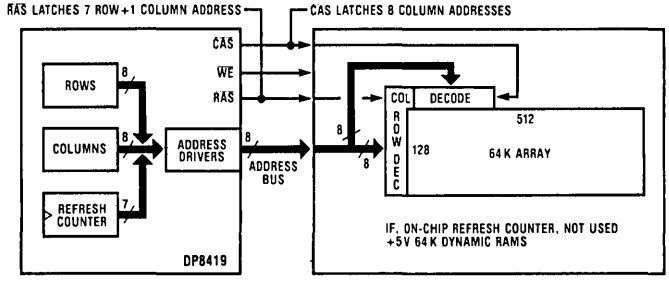
FIGURE 1a. DP8419 with any 16k DRAMS



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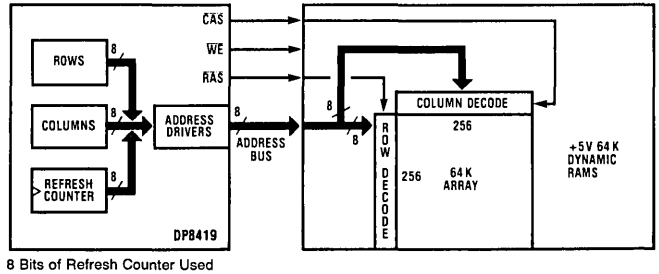
Only LS 7 Bits of Refresh Counter used for the 7 Row Addresses.
MSB not used but can toggle.

FIGURE 1b. DP8419 with 128 Row x 512 Column 64k DRAM



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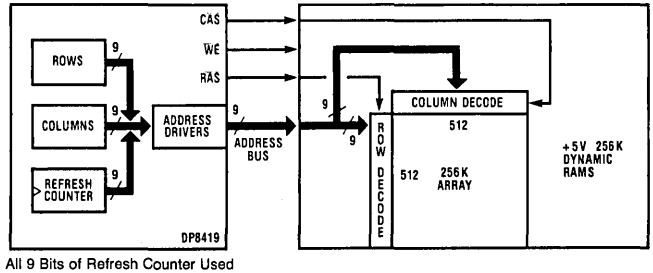
8 Bits of Refresh Counter Used

FIGURE 1c. DP8419 with 256 Row x 256 Column 64k DRAM



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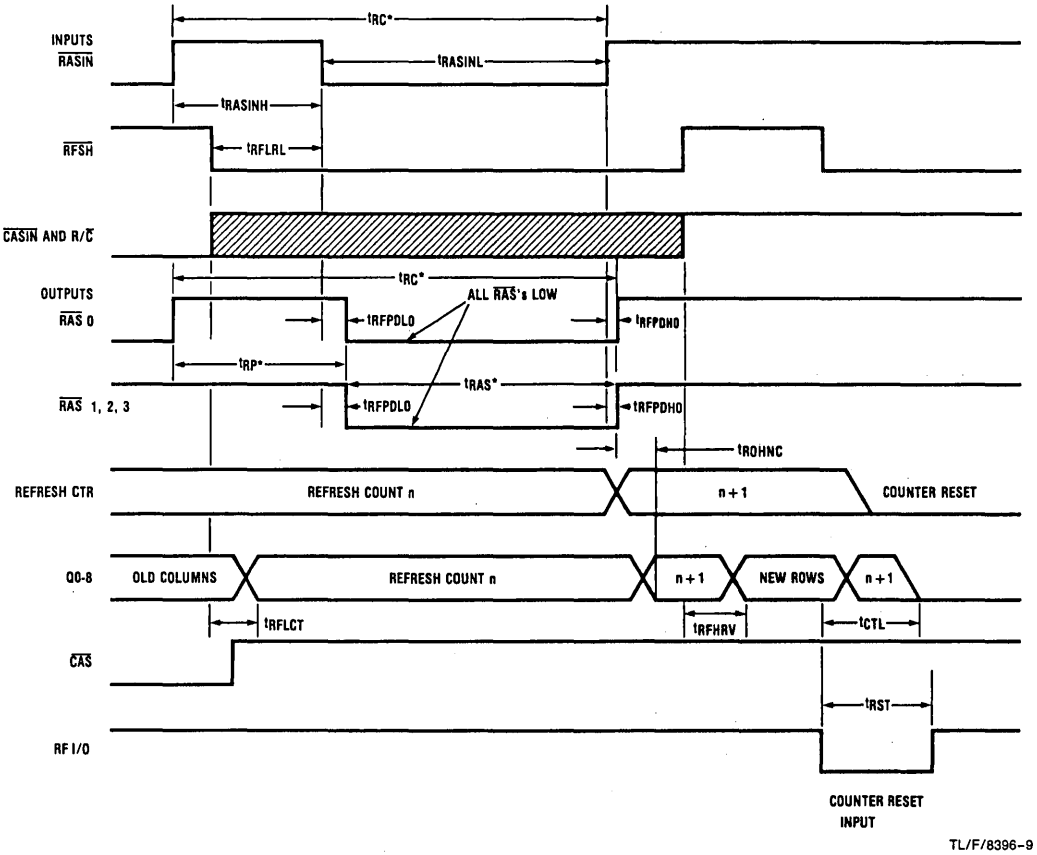
All 9 Bits of Refresh Counter Used

FIGURE 1d. DP8419 with 256k DRAMs

DP8419 Mode Descriptions (Continued)



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*Indicates Dynamic RAM Parameters

FIGURE 2a. External Control Refresh Cycle (Mode 0)

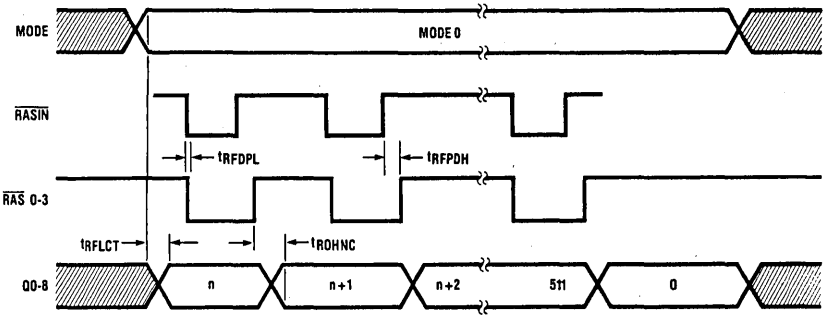

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FIGURE 2b. Burst Refresh Mode 0

DP8419 Mode Descriptions (Continued)

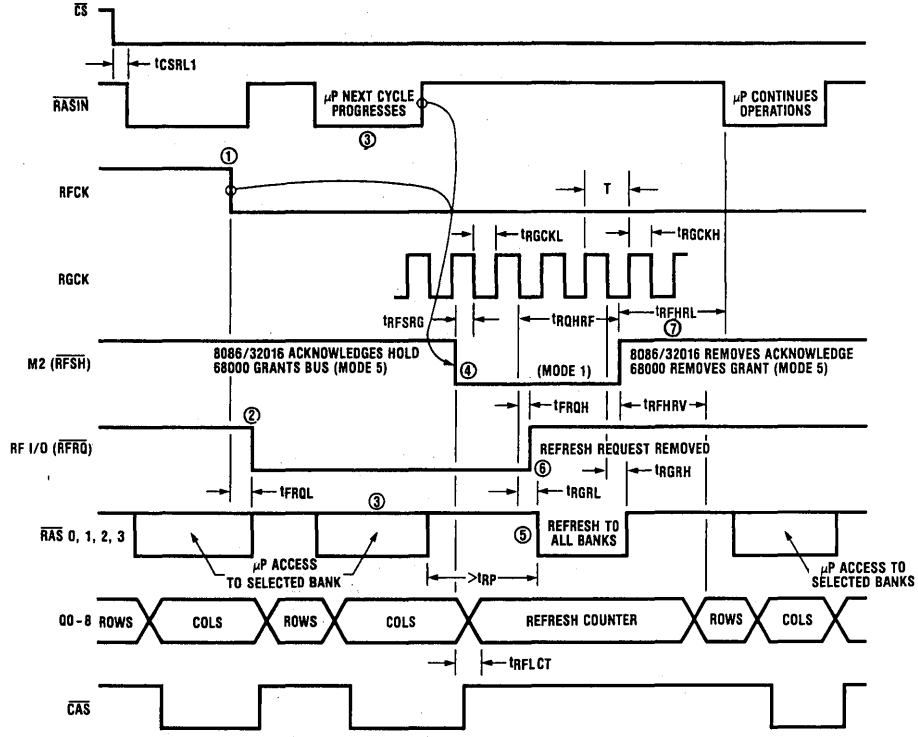
MODE 1–AUTOMATIC FORCED REFRESH

In Mode 1 the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock) and the $\overline{CASIN}$ (RGCK) pin becomes RGCK ($\overline{RAS}$ generator clock). If RFCK is high and Mode 1 is entered then the chip operates as if in MODE 0 (externally controlled refresh), with all $\overline{RAS}$ outputs following $\overline{RASIN}$. This feature of Mode 1 may be useful for those who want to use Mode 5 (automatic access) with externally controlled refresh. By holding RFCK permanently high one need only toggle M2 ($\overline{RFSH}$) to switch from Mode 5 to external refresh. As with Mode 0, RFI/O may be pulled low by an external gate to reset the refresh counter.

When using Mode 1 as automatic refresh, RFCK must be an input clock signal. One refresh should occur each period of RFCK. If no refresh is performed while RFCK is high, then when RFCK goes low RFI/O immediately goes low to indicate that a refresh is requested. (RFI/O may still be used to reset the refresh counter even though it is also used as a refresh request pin, however, an open-collector gate should be used to reset the counter in this case since RFI/O is forced low internally for a request).

After receiving the refresh request the system must allow a forced refresh to take place while RFCK is low. External logic can monitor $\overline{RFRQ}$ (RFI/O) so that when $\overline{RFRQ}$ goes low this logic will wait for the access currently in progress to be completed before pulling M2 ($\overline{RFSH}$) low to put the DP8419 in mode 1. If no access is taking place when $\overline{RFRQ}$ occurs, then M2 may immediately go low. Once M2 is low, the refresh counter contents appear at the address outputs and $\overline{RAS}$ is generated to perform the refresh.

An external clock on RGCK is required to derive the refresh $\overline{RAS}$ signals. On the second falling edge of RGCK after M2 is low, all $\overline{RAS}$ lines go low. They remain low until two more falling edges of RGCK. Thus $\overline{RAS}$ remains high for one to two periods of RGCK after M2 goes low, and stays low for two periods. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the falling edge of RGCK.



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① RFCK goes low
② $\overline{RFRQ}$ goes low if no hidden refresh occurred while RFCK was high
③ Next $\overline{RASIN}$ starts next access
④ μP acknowledges refresh request
⑤ Forced refresh $\overline{RAS}$ starts after > T (> t_{RP})
⑥ Forced refresh $\overline{RAS}$ ends $\overline{RFRQ}$
⑦ μP removes refresh acknowledge

FIGURE 3. DP8419 Performing a Forced Refresh (Mode 5 → 1 → 5) with Various Microprocessors

DP8419 Mode Descriptions (Continued)

The Refresh Request on RFI/O is terminated as $\overline{RAS}$ goes low. This signal may be used to end the refresh earlier than it normally would as described above. If M2 is pulled high while the $\overline{RAS}$ lines are low, then the $\overline{RAS}$s go high t_{RFRH} later. The designer must be careful, however, not to violate the minimum $\overline{RAS}$ low time of the DRAMs. He must also guarantee that the minimum $\overline{RAS}$ precharge time is not violated during a transition from mode 1 to mode 5 when an access is desired immediately following a refresh.

If the processor tries to access memory while the DP8419 is in mode 1, WAIT states should be inserted into the processor cycles until the DP8419 is back in mode 5 and the desired access has been accomplished (see *Figure 9*).

Instead of using WAIT states to delay accesses when refreshing, HOLD states could be used as follows. $\overline{RFRQ}$ could be connected to a HOLD or Bus Request input to the system. When convenient, the system acknowledges the $\overline{HOLD}$ or $\overline{Bus\ Request}$ by pulling M2 low. Using this scheme, $\overline{HOLD}$ will end as the $\overline{RAS}$ lines go low (RFI/O goes high). Thus, there must be sufficient delay from the time $\overline{HOLD}$ goes high to the DP8419 returning to mode 5, so that the $\overline{RAS}$ low time of the DRAMs isn't violated as described earlier (see *Figure 3* for mode 1 refresh with Hold states).

To perform a forced refresh the system will be inactive for about four periods of RGCK. For a frequency of 10 MHz, this is 400 ns. To refresh 128 rows every 2 ms an average of about one refresh per 16 μs is required. With a RFCK period of 16 μs and RGCK period of 100 ns, DRAM accesses are delayed due to refresh only 2.5% of the time. If using the Hidden Refresh available in mode 5 (refreshing with RFCK high) this percentage will be even lower.

MODE 4 - EXTERNALLY CONTROLLED ACCESS

In this mode all control signal outputs can be controlled directly by the corresponding control input. The enabled $\overline{RAS}$ output follows $\overline{RASIN}$, $\overline{CAS}$ follows $\overline{CASIN}$ (with R/$\overline{C}$ low), $\overline{WE}$ follows $\overline{WIN}$ and R/$\overline{C}$ determines whether the row or the column inputs are enabled to the address outputs (see *Figure 4*).

With R/$\overline{C}$ high, the row address latch contents are enabled onto the address bus. $\overline{RAS}$ going low strobes the row address into the DRAMs. After waiting to allow for sufficient row-address hold time (t_{RAH}) after $\overline{RAS}$ goes low, R/$\overline{C}$ can go low to enable the column address latch contents onto the address bus. When the column address is valid, $\overline{CAS}$ going low will strobe it into the DRAMs. $\overline{WIN}$ determines whether the cycle is a read, write or read-modify-write access. Refer to *Figures 5a* and *5b* for typical Read and Write timing using mode 4.

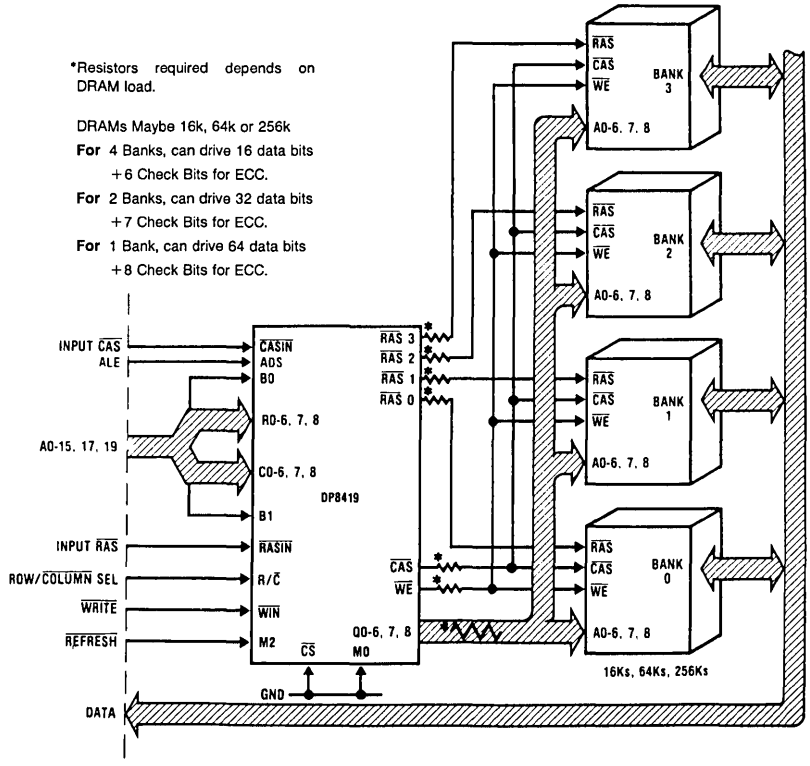

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FIGURE 4. Typical Application of DP8419 Using External Control Access and Refresh in Modes 0 and 4

DP8419 Mode Descriptions (Continued)

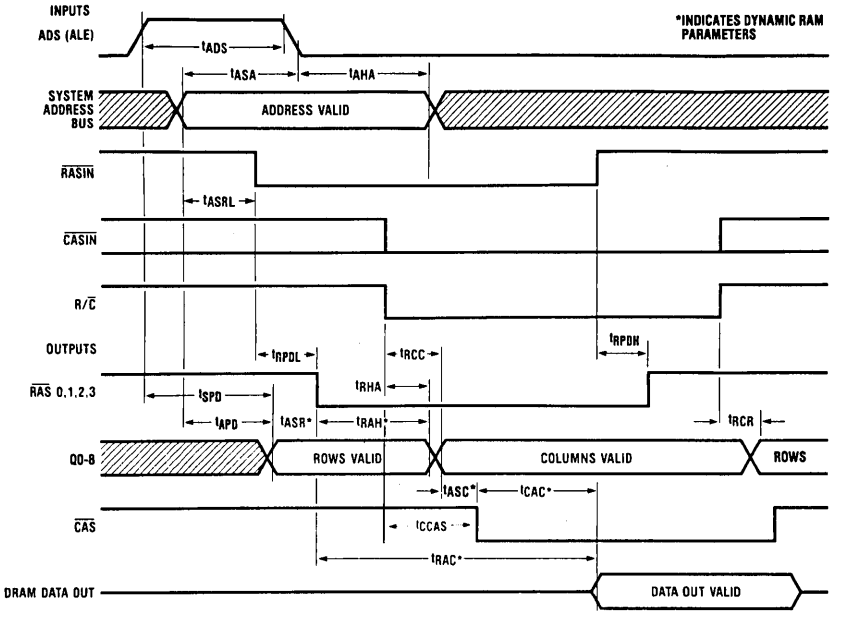

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FIGURE 5a. Read Cycle Timing (Mode 4)

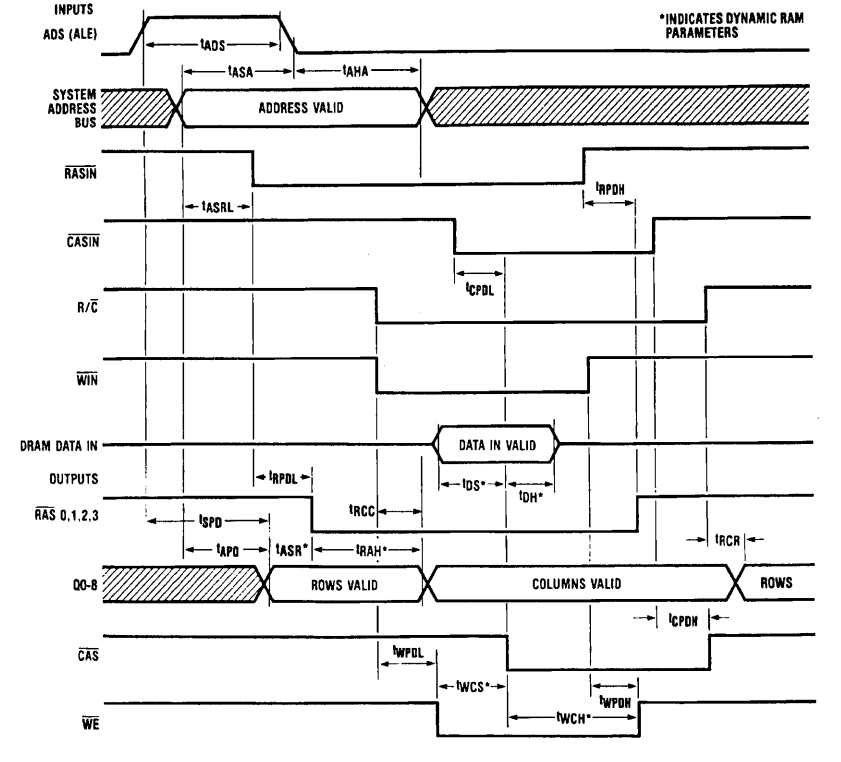

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FIGURE 5b. Write Cycle Timing (Mode 4)

DP8419 Mode Descriptions (Continued)

Page or Nibble mode may be performed by toggling $\overline{CASIN}$ once the initial access has been completed. In the case of page mode the column address must be changed before $\overline{CASIN}$ goes low to access a new memory location (see *Figure 5c*). Parameter t_{CPdif} has been specified in order that users may easily determine minimum $\overline{CAS}$ pulse widths when $\overline{CASIN}$ is toggling.

AUTOMATIC $\overline{CAS}$ GENERATION

$\overline{CAS}$ is held high when R/$\overline{C}$ is high even if $\overline{CASIN}$ is low. If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ goes low automatically, t_{ASC} after the column address is valid. This feature eliminates the need for an externally derived $\overline{CASIN}$ signal to control $\overline{CAS}$ when performing a simple access (*Figure 5a* demonstrates Auto-$\overline{CAS}$ generation in mode 4). Page or nibble accessing may be performed as shown in *Figure 5c* even if $\overline{CAS}$ is generated automatically for the initial access.

FASTEST MEMORY ACCESS

The fastest mode 4 access is achieved by using the automatic $\overline{CAS}$ feature and external delay line to generate the required delay between $\overline{RASIN}$ and R/$\overline{C}$. The amount of delay required depends on the minimum t_{RAH} of the DRAMs being used. The DP8419 parameter t_{DIF1} has been specified in order that the delay between $\overline{RASIN}$ and R/$\overline{C}$ may be minimized.

$$t_{DIF1} = \text{MAXIMUM } (t_{RPDL} - t_{RHA})$$

where t_{RPDL} = $\overline{RASIN}$ to $\overline{RAS}$ delay

and t_{RHA} = row address held from R/$\overline{C}$ going low.

The delay between $\overline{RASIN}$ and R/$\overline{C}$ that guarantees the specified DRAM t_{RAH} is given by

$$\text{MINIMUM } \overline{RASIN} \text{ to R/}\overline{C} = t_{DIF1} + t_{RAH}.$$

Example

In an application using DRAMs that require a minimum t_{RAH} of 15 ns, the following demonstrates how the maximum $\overline{RASIN}$ to $\overline{CAS}$ time is determined.

With t_{DIF1} (from Switching Characteristics) = 7 ns,

$\overline{RASIN}$ to R/$\overline{C}$ delay = 7 ns + 15 ns = 22 ns.

A delay line of 25 ns will be sufficient.

With Auto-$\overline{CAS}$ generation, the maximum delay from R/$\overline{C}$ to $\overline{CAS}$ (loaded with 600 pF) is 46 ns. Thus the maximum $\overline{RASIN}$ to $\overline{CAS}$ time is 71 ns, under the given conditions.

With a maximum $\overline{RASIN}$ to $\overline{RAS}$ time (t_{RPDL}) of 20 ns, the maximum $\overline{RAS}$ to $\overline{CAS}$ time is about 51 ns. Most DRAMs with a 15 ns minimum t_{RAH} have a maximum t_{RCD} of about 60 ns. Thus, memory accesses are likely to be $\overline{RAS}$ limited instead of $\overline{CAS}$ limited. In other words, memory access time is limited by DRAM performance, not controller performance.

REFRESHING IN CONJUNCTION WITH MODE 4

If using mode 4 to access memory, mode 0 (externally controlled refresh) must be used for all refreshing.

MODE 5 – AUTOMATIC ACCESS WITH HIDDEN REFRESHING CAPABILITY

Automatic-Access has two advantages over the externally controlled access (mode 4). First, $\overline{RAS}$, $\overline{CAS}$ and the row to column change are all derived internally from one input signal, $\overline{RASIN}$. Thus the need for an external delay line (see mode 4) is eliminated.

Secondly, since R/$\overline{C}$ and $\overline{CASIN}$ are not needed to generate the row to column change and $\overline{CAS}$, these pins can be used for the automatic refreshing function.

AUTOMATIC ACCESS CONTROL

Mode 5 of the DP8419 makes accessing Dynamic RAM nearly as easy as accessing static RAM. Once row and column addresses are valid (latched on the DP8419 if necessary), $\overline{RASIN}$ going low is all that is required to perform the memory access.

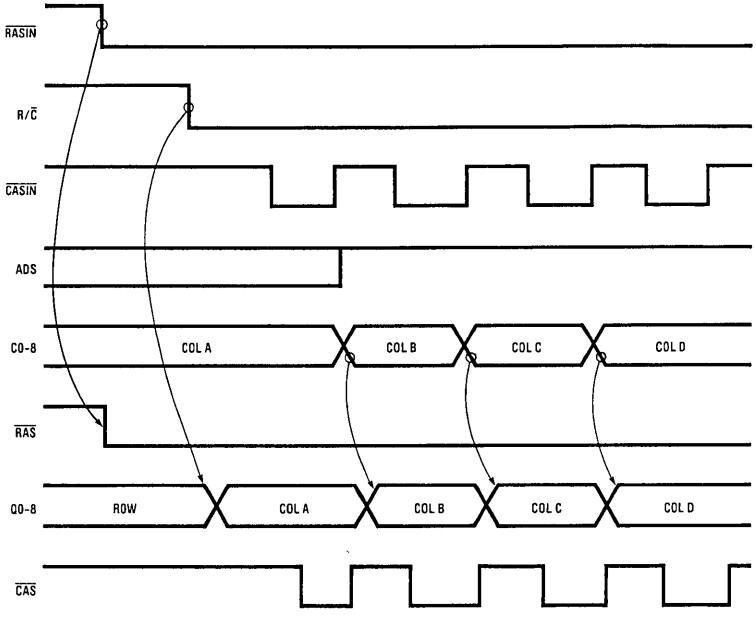

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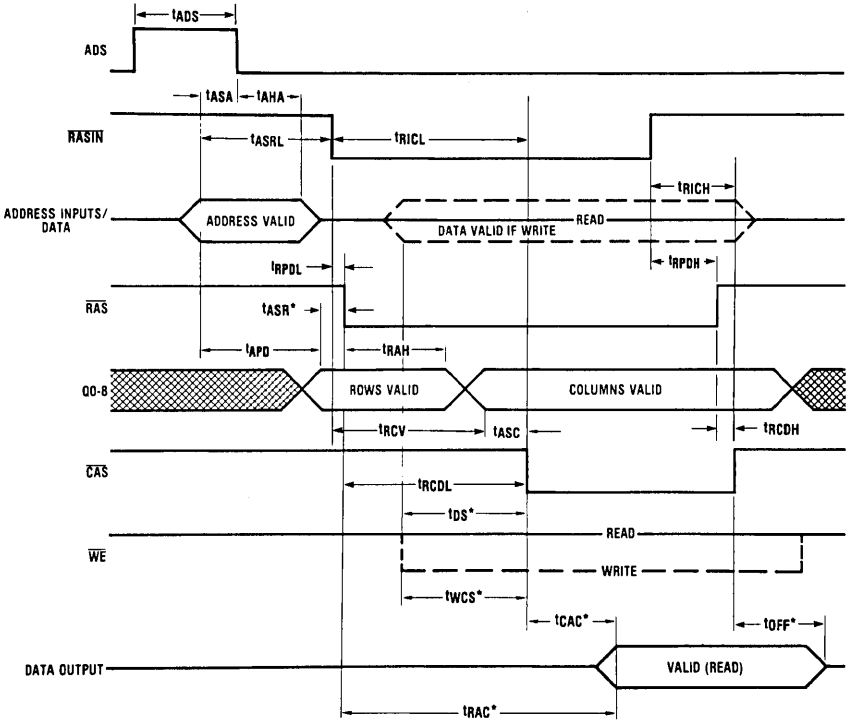
FIGURE 5c. Page or Nibble Access in Mode 4

DP8419 Mode Descriptions (Continued)



*Indicates Dynamic RAM Parameters

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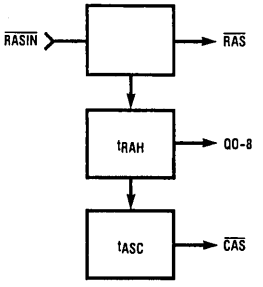
FIGURE 6. Mode 5 Timing

(Refer to *Figure 6*) In mode 5 the selected $\overline{RAS}$ follows $\overline{RASIN}$ immediately, as in mode 4, to strobe the row address into the DRAMs. The row address remains valid on the DP8419 address outputs long enough to meet the t_{RAH} requirement of the DRAMs (pin 4, RAHS, of the DP8419 allows the user two choices of t_{RAH}). Next, the column address replaces the row address on the address outputs and $\overline{CAS}$ goes low to strobe the columns into the DRAMs. $\overline{WIN}$ determines whether a read, write or read-modify-write is done.

The diagram below illustrates mode 5 automatic control signal generation.



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REFRESHING IN CONJUNCTION WITH MODE 5

When using mode 5 to perform memory accesses, refreshing may be accomplished:

(a) externally (in mode 0 or mode 1)

(b) by a combination of mode 5 (hidden refresh) and mode 1 (auto-refresh)

or (c) by a combination of mode 5 and mode 0

(a) Externally Controlled Refreshing in Mode 0 or Mode 1

All refreshing may be accomplished using external refreshes in either mode 0 or mode 1 with R/$\overline{C}$ (RFCK) tied high (see mode 0 and mode 1 descriptions). If this is desired, the system determines when a refresh will be performed, puts the DP8419 in the appropriate mode, and controls the $\overline{RAS}$ signals directly with $\overline{RASIN}$. The on-chip refresh counter is enabled to the address outputs of the DP8419 when the refresh mode is entered, and increments when $\overline{RASIN}$ goes high at the completion of the refresh.

(b) Mode 5 Refreshing (hidden) with Mode 1 refreshing (auto)

(Refer to *Figure 7a*) If RFCK is tied to a clock (see mode 1 description), RFI/O becomes a refresh request output and goes low following RFCK going low if no refresh occurred while RFCK was high. Refreshes may be performed in mode 5 when the DP8419 is not selected for access ($\overline{CS}$ is high) and RFCK is high. If these conditions exist the refresh counter contents appear on the DP8419 address outputs and all $\overline{RAS}$ lines follow $\overline{RASIN}$ so that if $\overline{RASIN}$ goes low (an access other than through the DP8419 occurs), all $\overline{RAS}$ lines go low to perform the refresh. The DP8419 allows only one refresh of this type for each period of RFCK, since RFCK should be fast enough such that one refresh per period is sufficient to meet the DRAM refresh requirement.

DP8419 Mode Descriptions (Continued)

Once it is started, a hidden refresh will continue even if RFCK goes low. However, $\overline{CS}$ must be high throughout the refresh (until $\overline{RASIN}$ goes high).

These hidden refreshes are valuable in that they do not delay accesses. When determining the duty cycle of RFCK, the high time should be maximized in order to maximize the probability of hidden refreshes. If a hidden refresh doesn't happen, then a refresh request will occur on RFI/O when RFCK goes low. After receiving the request, the system must perform a refresh while RFCK is low. This may be done by going to mode 1 and allowing an automatic refresh (see mode 1 description). This refresh must be completed while RFCK is low, thus the RFCK low time is determined by the worst-case time required by the system to respond to a refresh request.

(c) Mode 5 Refresh (Hidden Refresh) with mode 0 Refresh (External Refresh)

This refresh scheme is identical to that in (b) except that after receiving a refresh request, mode 0 is entered to do the refresh (see mode 0 description). The refresh request is terminated (RFI/O goes high) as soon as mode 0 is entered. This method requires more control than using mode 1 (auto-refresh), however, it may be desirable if the mode 1 refresh time is considered to be excessive.

Example

Figure 7b demonstrates how a system designer would use the DP8419 in mode 5 based on certain characteristics of his system.

System Characteristics:

1) DRAM used has min t_{RAH} requirement of 15 ns and min t_{ASR} of 0 ns
2) DRAM address is valid from time T_V to the end of the memory cycle
3) four banks of twenty-two 256K memory chips each are being driven

Using the DP8419 (see *Figure 7b*):

1) Tie pin 4 (RAHS) high to guarantee a 15 ns minimum t_{RAH} which is sufficient for the DRAMs being used
2) Generate $\overline{RASIN}$ no earlier than time $T_V + t_{ASRL}$ (see switching characteristics), so that the row address is valid on the DRAM address inputs before $\overline{RAS}$ occurs
3) Tie ADS high since latching the DRAM address on the DP8419 is not necessary
4) Connect the first 18 system address bits to R0-R8 and C0-C8, and bits 19 and 20 to B0 and B1
5) Connect each $\overline{RAS}$ output of the DP8419 to the $\overline{RAS}$ inputs of the DRAMs of one bank of the memory array; connect Q0-Q8 of the DP8419 to A0-A8 of all DRAMs; connect $\overline{CAS}$ of the DP8419 to $\overline{CAS}$ of all the DRAMs

Figure 7c illustrates a similar example using the DP8418 to drive two 32-bit banks.

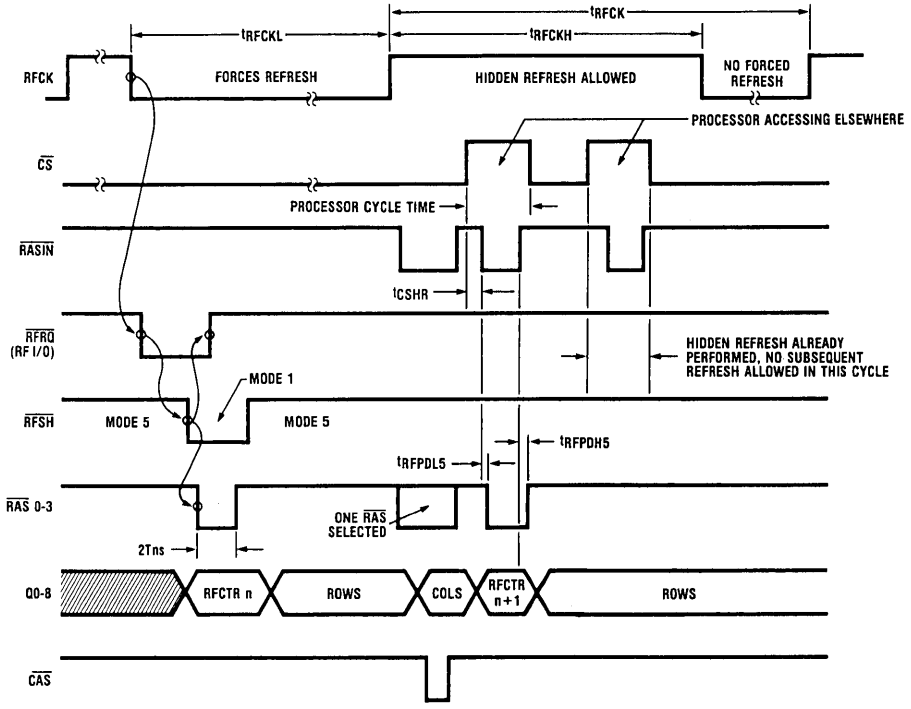

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FIGURE 7a. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

DP8419 Mode Descriptions (Continued)

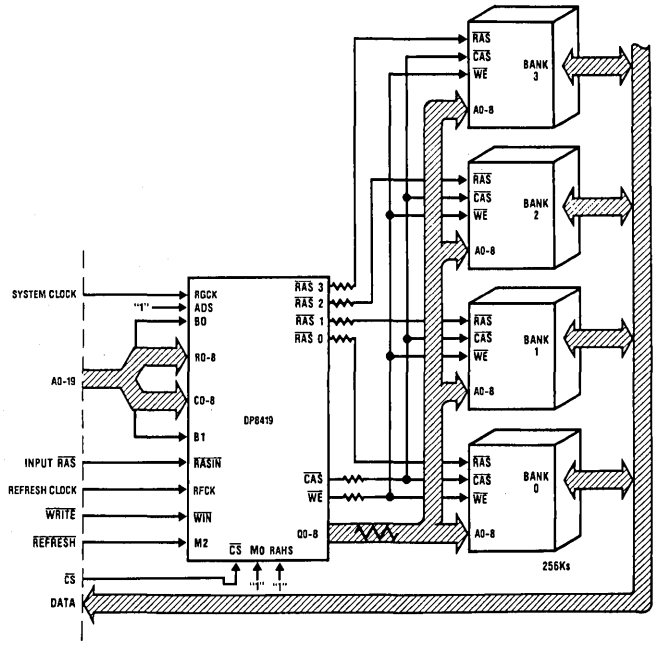

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FIGURE 7b. Typical Application of DP8419 Using Modes 5 and 1

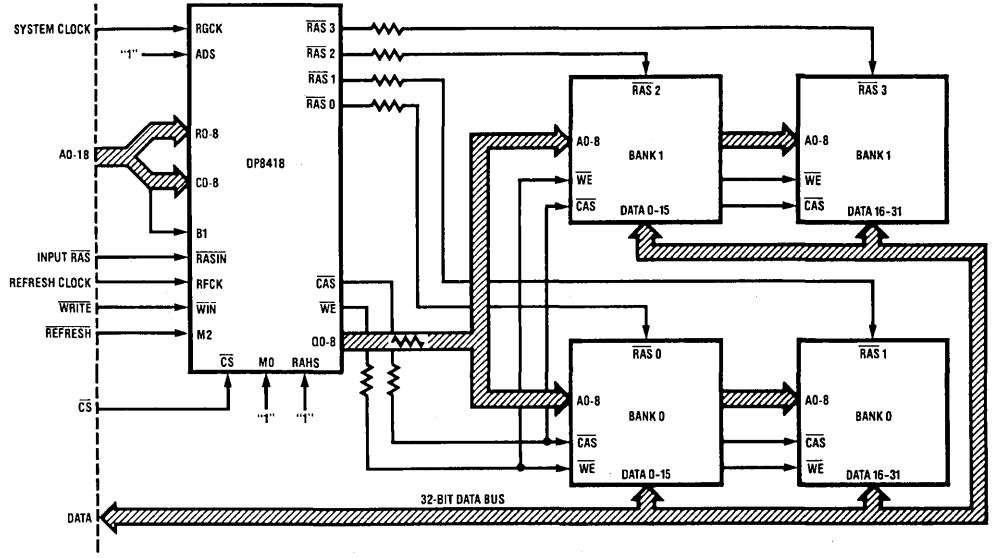

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FIGURE 7c. Typical Application of DP8418 Using Modes 5 and 1

Applications

If one desires a memory interface containing the DP8419 that minimizes the number of external components required, modes 5 and 1 should be used. These two modes provide:

1) Automatic access to memory (in mode 5 only one signal, $\overline{\text{RASIN}}$, is required in order to access memory)
2) Hidden refresh capability (refreshes are performed automatically while in mode 5 when non-local accesses are taking place, as determined by $\overline{\text{CS}}$)
3) Refresh request capability (if no hidden refresh took place while RFCK was high, a refresh request is generated at the RFI/O pin when RFCK goes high)
4) Automatic forced refresh (If a refresh request is generated while in mode 5, as described above, external logic should switch the DP8419 into mode 1 to do an automatic forced refresh. No other external control signals need be issued. WAIT states can be inserted into the processor machine cycles if the system tries to access memory while the DP8419 is in mode 1 doing a forced refresh).

Some items to be considered when integrating the DP8419 into a system design are:

1) The system designer should ensure that a DRAM access not be in progress when a refresh mode is entered. Similarly, one should not attempt to start an access while a refresh is in progress. The parameter t_{RFHRL} specifies the minimum time from $\overline{\text{RFSH}}$ high to $\overline{\text{RASIN}}$ going low to initiate an access.
2) One should always guarantee that the DP8419 is enabled for access prior to initiating the access (see t_{CSRL1}).
3) One should bring $\overline{\text{RASIN}}$ low even during non-local access cycles when in mode 5 in order to maximize the chance of a hidden refresh occurring.
4) At lower frequencies (under 10 Mhz), it becomes increasingly important to differentiate between READ and WRITE cycles. $\overline{\text{RASIN}}$ generation during READ cycles can take place as soon as one knows that a processor READ access cycle has started. WRITE cycles, on the other hand, cannot start until one knows that the data to be written at the DRAM inputs will be valid a setup time before $\overline{\text{CAS}}$ (column address strobe) goes true at the DRAM inputs. Therefore, in general, READ cycles can be initiated earlier than WRITE cycles.
5) Many times it is possible to only add WAIT states during READ cycles and have no WAIT states during WRITE cycles. This is because it generally takes less time to write data into memory than to read data from memory.

The DP84XX2 family of inexpensive preprogrammed medium Programmable Array Logic devices (PALs) have been developed to provide an easy interface between various microprocessors and the DP84XX family of DRAM controller/drivers. These PALs interface to all the necessary control signals of the particular processor and the DP8419. The PAL controls the operation of the DP8419 in modes 5 and 1, while meeting all the critical timing considerations discussed above. The refresh clock, RFCK, may be divided down from the processor clock using an IC counter such as the DM74LS393 or the DP84300 programmable refresh timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on an input clock of 2 to 10 MHz. *Figure 8* shows a general block diagram for a system using the DP8419 in modes 1 and 5. *Figure 9* shows possible timing diagrams for such a system (using $\overline{\text{WAIT}}$ to prohibit access when refreshing). Although the DP84XX2 PALs are offered as standard peripheral devices for the DP84XX DRAM controller/drivers, the programming equations for these devices are provided so the user may make minor modification, for unique system requirements.

ADVANTAGES OF DP8419 OVER A DISCRETE DYNAMIC RAM CONTROLLER

1) The DP8419 system solution takes up much less board space because everything is on one chip (latches, refresh counter, control logic, multiplexers, drivers, and internal delay lines).
2) Less effort is needed to design a memory system. The DP8419 has automatic modes (1 and 5) which require a minimum of external control logic. Also programmable array logic devices (PALs) have been designed which allow an easy interface to most popular microprocessors (Motorola 68000 family, National Semiconductor 32032 family, Intel 8086 family, and the Zilog Z8000 family).
3) Less skew in memory timing parameters because all critical components are on one chip (many discrete drivers specify a minimum on-chip skew under worst-case conditions, but this cannot be used if more then one driver is needed, such as would be the case in driving a large dynamic RAM array).
4) Our switching characteristics give the designer the critical timing specifications based on TTL output levels (low = 0.8V, high = 2.4V) at a specified load capacitance. All timing parameters are specified on the DP8419:
   A) driving 88 DRAM's over a temperature range of 0–70 degrees centigrade (no extra drivers are needed).
   B) under worst-case driving conditions with all outputs switching simultaneously (most discrete drivers on the market specify worst-case conditions with only one output switching at a time; this is not a true worst-case condition!).

Applications (Continued)

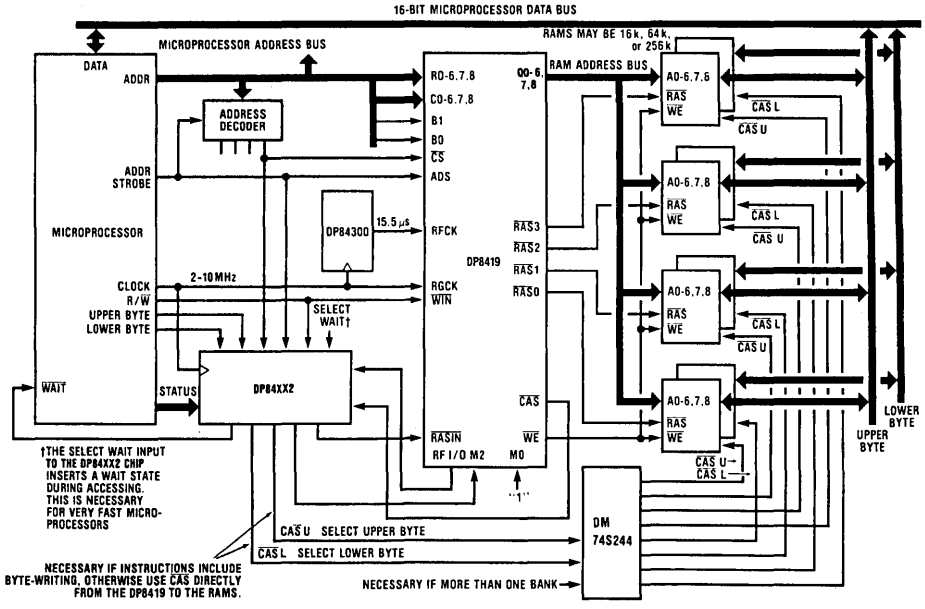

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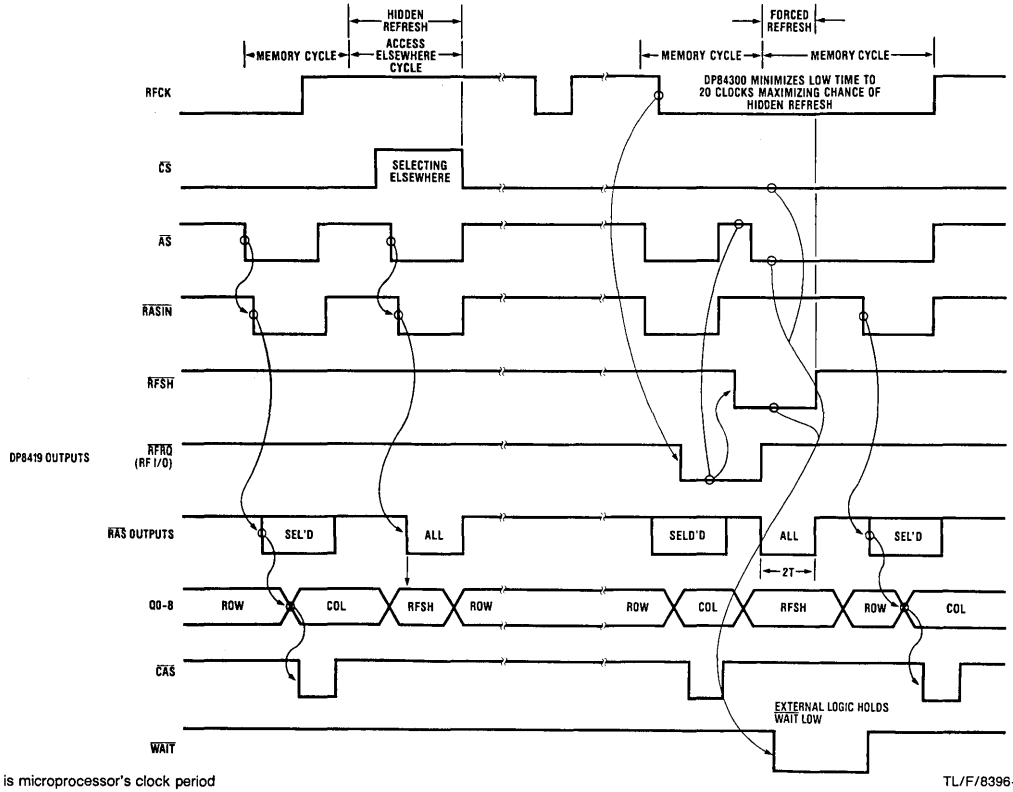
FIGURE 8. Connecting the DP8419 Between the 16-bit Microprocessor and Memory



*T is microprocessor's clock period

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FIGURE 9. DP8419 Auto Refresh, Access with $\overline{\text{WAIT}}$ States

Switching Characteristics

All AC parameters are specified with the equivalent load capacitances, including traces, of 88 DRAMs organized as 4 banks of 22 DRAMs each. Maximums are based on worst-case conditions including all outputs switching simultaneously. This, in many cases, results in the AC values shown in the DP84XX DRAM controller data sheet being much looser than true worst case (maximum) AC delays. The system designer should estimate the DP8419 load in his/her application, and modify the appropriate AC parameters using the graph in *Figure 10*. Two example calculations are provided below.

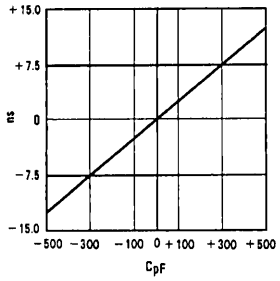

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FIGURE 10. Change in Propagation Delay Relative to "True" (Application) Load Minus AC Specified Data Sheet Load

2 Examples

#1) A mode 4 user driving 2 16-bit banks of DRAM has the following approximate "true" loading conditions:

$\overline{CAS}$ - 300 pF

Q0-Q8 - 250 pF

$\overline{RAS}$ - 150 pF

max t_{RPDL} = 20 ns − 0 ns = 20 ns (since $\overline{RAS}$ loading is the same as that which is spec'ed)

max t_{CPDL} = 32 ns − 7 ns = 25 ns

max t_{CCAS} = 46 ns − 7 ns = 39 ns

max t_{RCC} = 41 ns − 6 ns = 35 ns

min t_{RHA} is not significantly effected since it does not involve an output transition

Other parameters are adjusted in a similar manner.

#2) A mode 5 user driving one 16-bit bank of DRAM has the following approximate "true" loading conditions:

$\overline{CAS}$ - 120 pF

Q0-Q8 - 100 pF

$\overline{RAS}$ - 120 pF

A. C. parameters should be adjusted as follows:

with RAHS = "1",

max t_{RICL} = 70 ns − 11 ns = 59 ns

max t_{RCDL} = 55 ns + 1 ns − 11 ns = 45 ns

(the + 1 ns is due to lighter $\overline{RAS}$ loading; the − 11 ns is due to lighter $\overline{CAS}$ loading)

min t_{RAH} = 15 ns + 1 ns = 16 ns

The additional 1 ns is due to the fact that the $\overline{RAS}$ line is driving less (switching faster) than the load to which the 15 ns spec applies. The row address will remain valid for about the same time irregardless of address loading since it is considered to be not valid at the beginning of its transition.

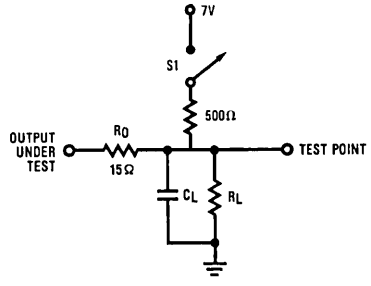

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FIGURE 11a. Output Load Circuit

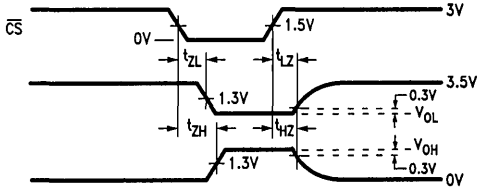

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FIGURE 11b. DP8417 TRI-STATE Waveforms

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150 mA
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

		Min	Max	Units
V_{CC}	Supply Voltage	4.50	5.50	V
T_A	Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min, I_C = − 12 mA		− 0.8	− 1.2	V
I_{IH}	Input High Current for all Inputs	V_{IN} = 2.5V		2.0	100	μA
I_I RSI	Output Load Current for RFI/O	V_{IN} = 0.5V, Output high		−0.7	−1.5	mA
I_{IL1}	Input Low Current for all Inputs**	V_{IN} = 0.5V		−0.02	−0.25	mA
I_{IL2}	ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	I_{OL} = 20 mA		0.3	0.5	V
V_{OL2}	Output Low Voltage for RFI/O	I_{OL} = 8 mA		0.3	0.5	V
V_{OH1}	Output High Voltage*	I_{OH} = − 1 mA	2.4	3.5		V
V_{OH2}	Output High Voltage for RFI/O	I_{OH} = − 100 μA	2.4	3.5		V
I_{1D}	Output High Drive Current*	V_{OUT} = 0.8V (Note 3)	−50	− 200		mA
I_{0D}	Output Low Drive Current*	V_{OUT} = 2.4V (Note 3)	50	200		mA
I_{CC}	Supply Current	V_{CC} = Max		150	240	mA

*Except RFI/O

**Except RFI/O, ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5), the output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise noted. Maximum propagation delays are specified with all outputs switching.**

**** Preliminary**

Symbol	Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
ACCESS							
t_{RICL0}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-80	57	97	42	85	ns
t_{RICL0}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-70	57	87	42	75	ns
t_{RICL1}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-80	48	80	35	68	ns
t_{RICL1}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-70	48	70	35	58	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ High Delay	*Figure 6*		37			ns
t_{RCDL0}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-80	43	80			ns
t_{RCDL0}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8417, 18, 19-70	43	72			ns
t_{RCDL1}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-80	34	63			ns
t_{RCDL1}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8417, 18, 19-70	34	55			ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ High Delay	*Figure 6*		22			ns
t_{RAH0}	Row Address Hold Time (RAHS = 0, Mode 5)	*Figure 6*	25		25		ns
t_{RAH1}	Row Address Hold Time (RAHS = 1, Mode 5)	*Figure 6*	15		15		ns
t_{ASC}	Column Address Set-up Time (Mode 5)	*Figure 6*	0		0		ns

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X (Continued)

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS0}$-$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise specified. Maximum propagation delays are specified with all outputs switching.**

**** Preliminary**

Symbol	Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
ACCESS (Continued)							
t_{RCV0}	$\overline{RASIN}$ to Column Address Valid (RAHS = 0, Mode 5)	*Figure 6* DP8417, 18, 19-80		94			ns
t_{RCV0}	$\overline{RASIN}$ to Column Address Valid (RAHS = 0, Mode 5)	*Figure 6* DP8417, 18, 19-70		85			ns
t_{RCV1}	$\overline{RASIN}$ to Column Address Valid (RAHS = 1, Mode 5)	*Figure 6* DP8417, 18, 19-80		76			ns
t_{RCV1}	$\overline{RASIN}$ to Column Address Valid (RAHS = 1, Mode 5)	*Figure 6* DP8417, 18, 19-70		68			ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay	*Figures 5a, 5b, 6*		21		18	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay	*Figures 5a, 5b, 6*		20		17	ns
t_{ASRL}	Address Set-up to $\overline{RASIN}$ low	*Figures 5a, 5b, 6*	13				ns
t_{APD}	Address Input to Output Delay	*Figures 5a, 5b, 6*		36		25	ns
t_{SPD}	Address Strobe High to Address Output Valid	*Figures 5a, 5b*		48			ns
t_{ASA}	Address Set-up Time to ADS	*Figures 5a, 5b, 6*	5				ns
t_{AHA}	Address Hold Time from ADS	*Figures 5a, 5b, 6*	10				ns
t_{ADS}	Address Strobe Pulse Width	*Figures 5a, 5b, 6*	26				ns
t_{WPD}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 5b*		28			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Low Delay (R/$\overline{C}$ low, Mode 4)	*Figure 5b*	21	32			ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ High Delay (R/$\overline{C}$ low, Mode 4)	*Figure 5b*	16	33			ns
t_{CPdif}	t_{CPDL} - t_{CPDH}	See Mode 4 Description		11			ns
t_{RCC}	Column Select to Column Address Valid	*Figure 5a*		41			ns
t_{RCR}	Row Select to Row Address Valid	*Figures 5a, 5b*		45			ns
t_{RHA}	Row Address Held from Column Select	*Figure 5a*	7				ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low Delay ($\overline{CASIN}$ Low, Mode 4)	*Figure 5a* DP8417, 18, 19-80		50			ns
t	R/$\overline{C}$ Low to $\overline{CAS}$ Low Delay ($\overline{CASIN}$ Low, Mode 4)	*Figure 5a* DP8417, 18, 19-70		46			ns
t_{DIF1}	Maximum (t_{RPDL} - t_{RHA})	See Mode 4 Description		7			ns
t_{DIF2}	Maximum (t_{RCC} - t_{CPDL})			13			ns
REFRESH							
t_{RC}	Refresh Cycle Period	*Figure 2a*	100				ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2a*	50				ns
t_{RFPDL0}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay during Refresh (Mode 0)	*Figure 2a*		28			ns

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X (Continued)

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS}$0–$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise specified. Maximum propagation delays are specified with all outputs switching.**

Symbol	Parameter	Condition	*CL		All C_L = 50 pF		Units
			Min	Max	Min	Max	
REFRESH (Continued)							
t_{RFPDL5}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay during Hidden Refresh	*Figure 7*		38			ns
t_{RFPDH0}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay during Refresh (Mode 0)	*Figure 2a*		35			ns
t_{RFPDH5}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay during Hidden Refresh	*Figure 7*		44			ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	*Figures 2a, 3* $\overline{CS}$ = X		38			ns
t_{RFLRL}	$\overline{RFSH}$ Low Set-up to $\overline{RASIN}$ Low (Mode 0), to get Minimum t_{ASR} = 0	*Figure 2a*	12				ns
t_{RFHRL}	$\overline{RFSH}$ High Setup to Access $\overline{RASIN}$ Low	*Figure 3*	25				ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figure 3*		43			ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figure 2a*		42			ns
t_{RST}	Counter Reset Pulse Width	*Figure 2a*	46				ns
t_{CTL}	RFI/O Low to Counter Outputs All Low	*Figure 2a*		80			ns
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	*Figure 7*	100				ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	30				ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	15				ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	15				ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ (RFI/O) Low	*Figure 3* C_L = 50 pF RL = 35k		66			ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	*Figure 3* C_L = 50 pF RL = 35k		55			ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	21	41			ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	23	48			ns

Switching Characteristics: DP8417, DP8418, DP8419, DP8419X (Continued)

V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11a* for test load. S1 is open unless otherwise specified. Maximum propagation delays are specified with all outputs switching.**

Symbol	Parameter	Condition	*CL		All C_L = 50 pF		Units
			Min	Max	Min	Max	
REFRESH (Continued)							
t_{RQHRF}	$\overline{RFSH}$ Hold Time from RGCK	*Figure 3*	2T				ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (Ending Forced Refresh early)	(See Mode 1 Description)		42			ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	(See Mode 1 Description) *Figure 3*	12				ns
t_{CSHR}	$\overline{CS}$ High to $\overline{RASIN}$ Low for Hidden Refresh	*Figure 7*	10				ns
t_{RKRL}	RFCK High to $\overline{RASIN}$ low for hidden Refresh		50				ns
DP8419, DP8419X ONLY							
t_{CSRL1}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	34				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	5				ns
DP8418 ONLY							
t_{CSRL1}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	5				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	5				ns
DP8417 ONLY — PRELIMINARY							
t_{CSRL1}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	34				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	34				ns
TRI-STATE							
t_{ZH}	$\overline{CS}$ Low to Output High from Hi-Z	S1 Open *Figure 11G*		50			ns
t_{HZ}	$\overline{CS}$ High to Output Hi-Z from High	S1 Open *Figure 11G*				50	ns
t_{ZL}	$\overline{CS}$ Low to Output Low from Hi-Z	S1 Closed *Figure 11G*		50			ns
t_{HZ}	$\overline{CS}$ High to Output Hi-Z from Low	S1 Closed *Figure 11G*				50	ns

Input Capacitance T_A = 25°C (Note 2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F = 2.5$ ns, $f = 2.5$ MHz, $t_{PW} = 200$ ns. Input reference point on AC measurements is 1.5V Output reference points are 2.4V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

National Semiconductor Corporation

DP8428/NS32828, DP8429/NS32829
1 Megabit High Speed Dynamic RAM Controller/Drivers

General Description

The DP8428 and DP8429 1M DRAM Controller/Drivers are designed to provide "No-Waitstate" CPU interface to Dynamic RAM arrays of up to 8 Mbytes and larger. The DP8428 and DP8429 are tailored for 32-bit and 16-bit system requirements, respectively. Both devices are fabricated using National's new oxide isolated Advanced Low power Schottky (ALS) process and use design techniques which enable them to significantly out-perform all other LSI or discrete alternatives in speed, level of integration, and power consumption.

Each device integrates the following critical 1M DRAM controller functions on a single monolithic device: ultra precise delay line; 9 bit refresh counter; fall-through row, column, and bank select input latches; Row/Column address muxing logic; on-board high capacitive-load $\overline{RAS}$, $\overline{CAS}$, Write Enable and Address output drivers; and, precise control signal timing for all the above.

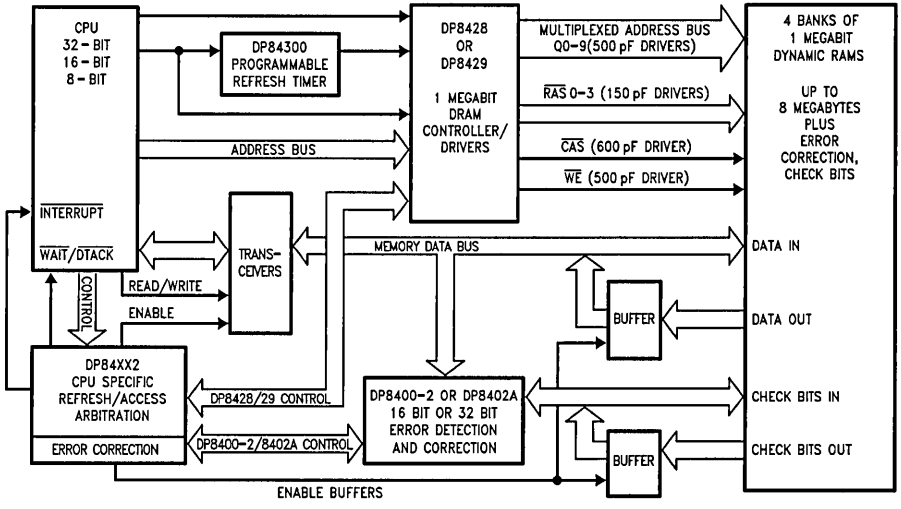
In order to specify each device for "true" worst case operating conditions, all timing parameters are guaranteed while the chip is driving the capacitive load of 88 DRAMs including trace capacitance. The chip's delay timing logic makes use of a patented new delay line technique which keeps AC skew to ± 3 ns over the full V_{CC} range of $\pm 10\%$ and temperature range of $-55°C$ to $+125°C$. The DP8428 and DP8429 guarantee a maximum RASIN to CASOUT delay of 80 ns or 70 ns even while driving an 8 Mbyte memory array with error correction check bits included. Two speed selected options of these devices are shown in the switching characteristics section of this document. (Continued)

Features

- Makes DRAM interface and refresh tasks appear virtually transparent to the CPU making DRAMs as easy to use as static RAMs
- Specifically designed to eliminate CPU wait states up to 10 MHz or beyond
- Eliminates 20 discrete components for significant board real estate reduction, system power savings and the elimination of chip-to-chip AC skewing
- On-board ultra precise delay line
- On-board high capacitive $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address drivers (specified driving 88 DRAMs directly)
- AC specified for directly addressing up to 8 Mbytes
- Low power/high speed bipolar oxide isolated process
- Downward pin and function compatible with 256k DRAM Controller/Drivers DP8409A, DP8417, DP8418, and DP8419

Contents

System Diagram



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1

General Description (Continued)

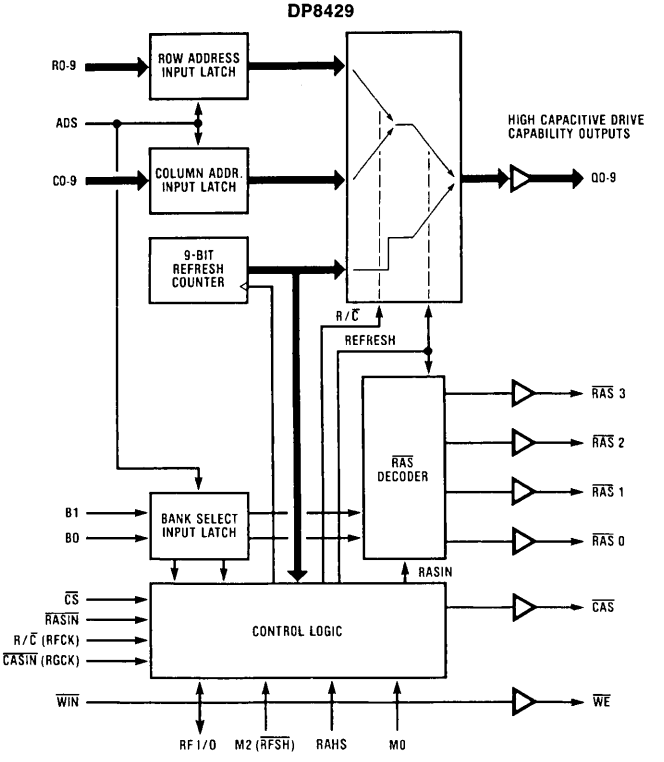
With its four independent $\overline{RAS}$ outputs and ten multiplexed address outputs, the DP8429 can support up to four banks of 64k, 256k or 1M DRAMs. Two bank select pins, B1 and B0, are decoded to activate one of the $\overline{RAS}$ signals during an access, leaving the three non-selected banks in the standby mode (less than one tenth of the operating power) with data outputs in TRI-STATE®. The DP8428's one Bank Select pin, B1, enables 2 banks automatically during an access in order to provide an optimum interface for 32-bit microprocessors.

The DP8428 and DP8429 each have two mode-select pins, allowing for two refresh modes and two access modes. Refresh and access timing may be controlled either externally or automatically. The automatic modes require a minimum of input control signals.

A refresh counter is on-chip and is multiplexed with the row and column inputs. Its contents appear at the address outputs of the DP8428 or DP8429 during any refresh, and are incremented at the completion of the refresh. Row, Column and bank address latches are also on-chip. However, if the address inputs to the DP8428 or DP8429 are valid throughout the duration of the access, these latches may be operated in the fall-through mode.

Each device is available in either the 52 pin Ceramic DIP, or the low cost JEDEC standard 68 pin Plastic Chip Carrier (PCC) package.

Functional Block Diagrams



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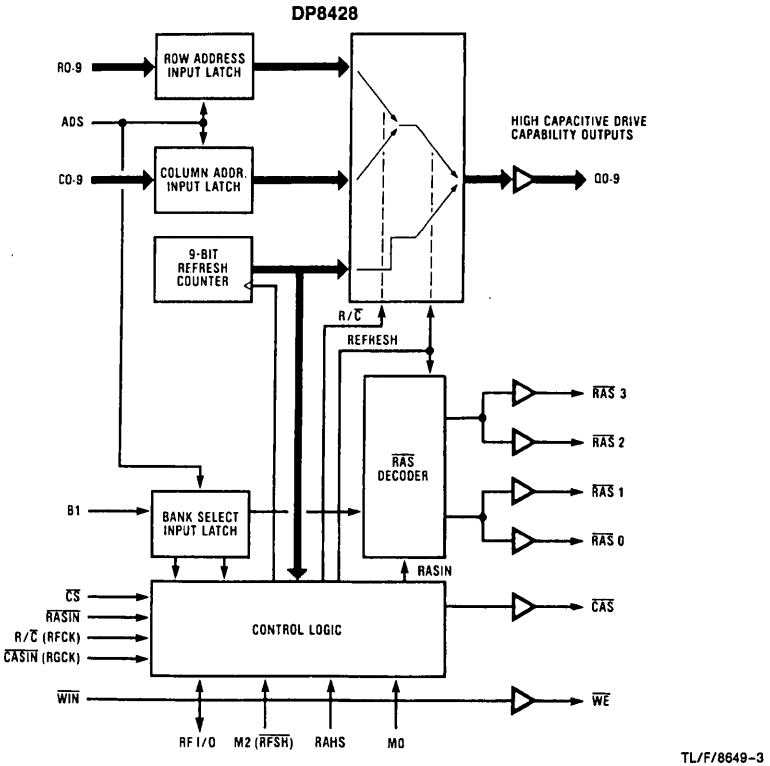
Functional Block Diagrams (Continued)



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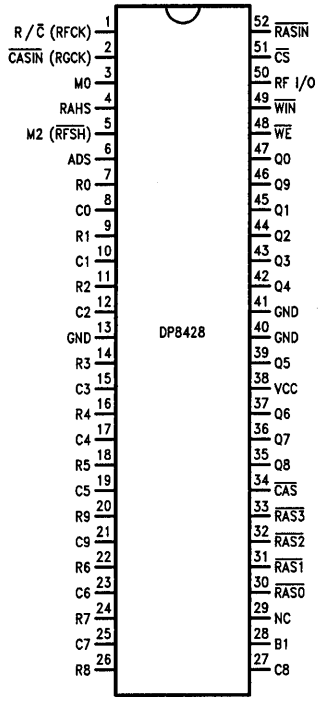
System Companion Components

Device #	Function
DP84300	Programmable Refresh Timer for DP84xx DRAM Controller
DP84412	NS32008/16/32 to DP8409A/17/18/19/28/29 Interface
DP84512	NS32332 to DP8417/18/19/28/29 Interface
DP84322	68000/08/10 to DP8409A/17/18/19/28/29 Interface (up to 8 MHz)
DP84422	68000/08/10 to DP8409A/17/18/19/28/29 Interface (up to 12.5 MHz)
DP84522	68020 to DP8417/18/19/28/29 Interface
DP84432	8086/88/186/188 to DP8409A/17/18/19/28/29 Interface
DP84532	80286 to DP8409A/17/18/19/28/29 Interface
DP8400-2	16-Bit Expandable Error Checker/Corrector (E2C2)
DP8402A	32-Bit Error Detector And Corrector (EDAC)

Connection Diagrams

Dual-In-Line Package



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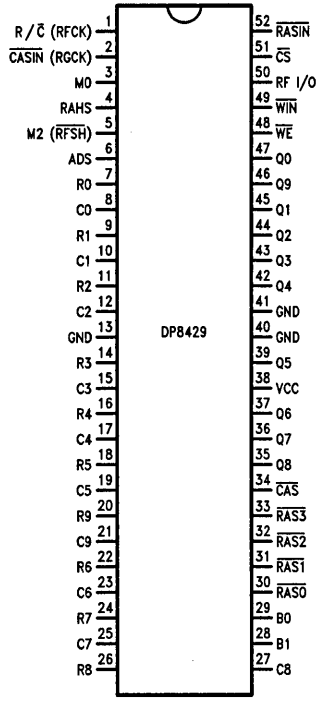
Dual-In-Line Package



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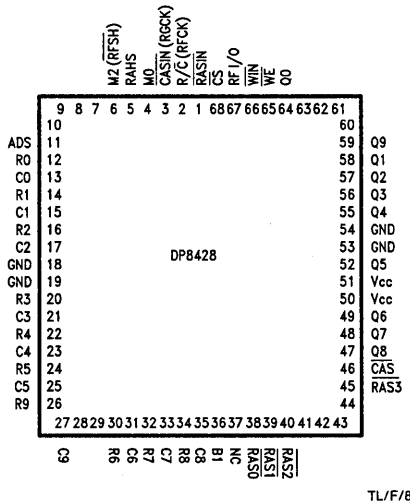
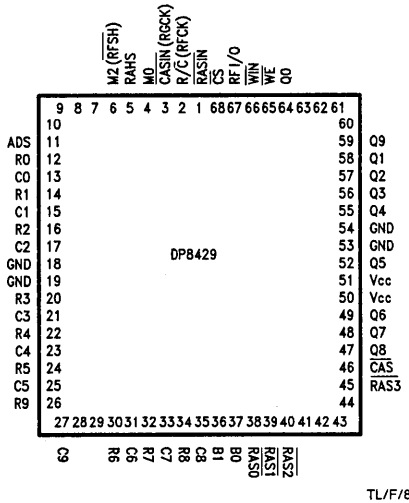
Order Number DP8428D-70, DP8428D-80 or DP8429D-70, DP8429D-80
See NS Package Number D52A

Plastic Chip Carrier Package



Plastic Chip Carrier Package



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TL/F/8649–7

Order Number DP8428V-70, DP8428V-80 or DP8429V-70, DP8429V-80
See NS Package Number V68A

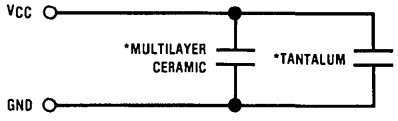
DP8428 vs DP8429

The DP8428 DYNAMIC RAM CONTROLLER/DRIVER is identical to the DP8429 with the exception of two functional differences incorporated to improve performance with 32-bit microprocessors.

1) Pin 28 (B1) is used to enable/disable a pair of $\overline{RAS}$ outputs, and pin 29 (B0 on the DP8429) is a no connect. When B1 is low, $\overline{RAS0}$ and $\overline{RAS1}$ are enabled such that they both go low during an access. When B1 is high, $\overline{RAS2}$ and $\overline{RAS3}$ are enabled. This feature is useful when driving words of 32 bits or more since each $\overline{RAS}$ would be driving only one half of the word. By distributing the load on each $\overline{RAS}$ line in this way, the DP8428 will meet the same AC specifications driving 2 banks of 32 DRAMs each as the DP8429 does driving 4 banks of 16 bits each.
2) The hidden refresh function available on the DP8429 has been disabled on the DP8428 in order to reduce the amount of setup time necessary from $\overline{CS}$ going low to $\overline{RASIN}$ going low during an access of DRAM. This parameter, called t_{CSRL1}, is 5 ns for the DP8428 whereas it is 34 ns for the DP8429. The hidden refresh function allowed only a very small increase in system performance, at microprocessor frequencies of 10 MHz and above.

Pin Definitions

V_{CC}, GND, GND – V_{CC} = 5V ±10%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 10 address bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to GND and V_{CC} to reduce lead inductance. See Figure below.



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*Capacitor values should be chosen depending on the particular application.

R0–R9: Row Address Inputs.

C0–C9: Column Address Inputs.

Q0–Q9: Multiplexed Address Outputs – This address is selected from the Row Address Input Latch, the Column Address Input Latch or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input – $\overline{RASIN}$ directly controls the selected $\overline{RAS}$ output when in an access mode and all $\overline{RAS}$ outputs during hidden or external refresh.

R/$\overline{C}$ (RFCK) – In the auto-modes this pin is the external refresh clock input; one refresh cycle should be performed each clock period. In the external access mode it is Row/Column Select Input which enables either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK) – In the auto-modes this pin is the $\overline{RAS}$ Generator Clock input. In external access mode it is the Column Address Strobe input which controls $\overline{CAS}$ directly once columns are enabled on the address outputs.

ADS: Address (Latch) Strobe Input – Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; latching occurs on high-to-low transition of ADS.

$\overline{CS}$: Chip Select Input – When high, $\overline{CS}$ disables all accesses. Refreshing, however, in both modes 0 and 1 is not affected by this pin.

M0, M2 ($\overline{RFSH}$): Mode Control Inputs – These pins select one of the four available operational modes of the DP8429 (see Table III).

RFI/0: Refresh Input/Output – In the auto-modes this pin is the Refresh Request Output. It goes low following RFCK indicating that no hidden refresh was performed while RFCK was high. When this pin is set low by an external gate the on-chip refresh counter is reset to all zeroes.

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output – $\overline{WE}$ follows $\overline{WIN}$ unconditionally.

RAHS: Row Address Hold Time Select – Selects the t_{RAH} to be guaranteed by the DP8428 or DP8429 delay line to allow for the use of fast or slow DRAMs.

$\overline{CAS}$: Column Address Strobe Output – In mode 5 and in mode 4 with $\overline{CASIN}$ low before R/$\overline{C}$ goes low, $\overline{CAS}$ goes low automatically after the column address is valid on the address outputs. In mode 4 $\overline{CAS}$ follows $\overline{CASIN}$ directly after R/$\overline{C}$ goes low, allowing for nibble accessing. $\overline{CAS}$ is always high during refresh.

$\overline{RAS}$ 0–3: Row Address Strobe Outputs – The enabled $\overline{RAS}$ output (see Table II) follows $\overline{RASIN}$ directly during an access. During refresh, all $\overline{RAS}$ outputs are enabled.

Pin Definitions (Continued)

B0, B1: Bank Select Inputs – These pins are decoded to enable one or two of the four $\overline{RAS}$ outputs during an access (see Table I and Table II).

TABLE I. DP8429 Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

TABLE II. DP8428 Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	NC	
0	X	$\overline{RAS}_0$ & $\overline{RAS}_1$
1	X	$\overline{RAS}_2$ & $\overline{RAS}_3$

Conditions for All Modes

INPUT ADDRESSING

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after $\overline{CAS}$ goes low at the end of the memory cycle, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

DRIVE CAPABILITY

The DP8429 has timing parameters that are specified driving the typical capacitance (including traces) of 88, 5V-only DRAMs. Since there are 4 $\overline{RAS}$ outputs, each is specified driving one-fourth of the total memory. $\overline{CAS}$, $\overline{WE}$ and the address outputs are specified driving all 88 DRAMs.

The graph in *Figure 10* may be used to determine the slight variations in timing parameters, due to loading conditions other than 88 DRAMs.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To reduce these spikes, a damping resistor (low inductance, carbon) should be inserted between the DP8429 outputs and the DRAMs, as close as possible to the DP8429. The damping resistor values may differ depending on how heavily an output is loaded. These resistors should be determined by the first prototypes (not wire-wrapped due to the larger distributed capacitance and inductance). Resistors should be chosen such that the transition on the control outputs is critically damped. Typical values will be from 15Ω to 100Ω, with the lower values being used with the larger memory arrays. Note that AC parameters are specified with 15Ω damping resistors. For more information see AN-305 "Precautions to Take When Driving Memories".

DP8429 DRIVING ANY 256k or 1M DRAMS

The DP8429 can drive any 256k or 1M DRAMs. 256k DRAMs require 18 of the DP8429's address inputs to select one memory location within the DRAM. $\overline{RAS}$-only refreshing with the nine-bit refresh-counter on the DP8429 makes $\overline{CAS}$ before $\overline{RAS}$ refreshing, available on 256k DRAMs, unnecessary (see *Figure 1a*).

1 Mbit DRAMs require the use of all 10 of the DP8429 Address Outputs (see *Figure 1b*).

READ, WRITE AND READ-MODIFY-WRITE CYCLES

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid, then data DI is written into the same address in the DRAM as $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. $\overline{WE}$ always follows $\overline{WIN}$ directly to determine the type of access to be performed.

POWER-UP INITIALIZE

When V_{CC} is first applied to the DP8429, an initialize pulse clears the refresh counter and the internal control flip-flops.

Mode Features Summary

- 4 modes of operation: 2 access and 2 refresh
- Automatic or external selected by the user
- Auto access mode provides $\overline{RAS}$, row to column change, and then $\overline{CAS}$ automatically.
- Choice between two different values of t_{RAH} in auto-access mode
- $\overline{CAS}$ controlled independently in external control mode, allowing for nibble mode accessing
- Automatic refreshing can make refreshes transparent to the system
- $\overline{CAS}$ is inhibited during refresh cycles

DP8428/DP8429 Mode Descriptions

MODE 0–EXTERNALLY CONTROLLED REFRESH

Figure 2 shows the Externally Controlled Refresh timing. In this mode the refresh counter contents are multiplexed to the address outputs. All $\overline{RAS}$ outputs are enabled to follow $\overline{RASIN}$ so that the row address indicated by the refresh counter is refreshed in all DRAM banks when $\overline{RASIN}$ goes low. The refresh counter increments when $\overline{RASIN}$ goes high. $\overline{RFSH}$ should be held low at least until $\overline{RASIN}$ goes high (they may go high simultaneously) so that the refresh address remains valid and all $\overline{RAS}$ outputs remain enabled throughout the refresh.

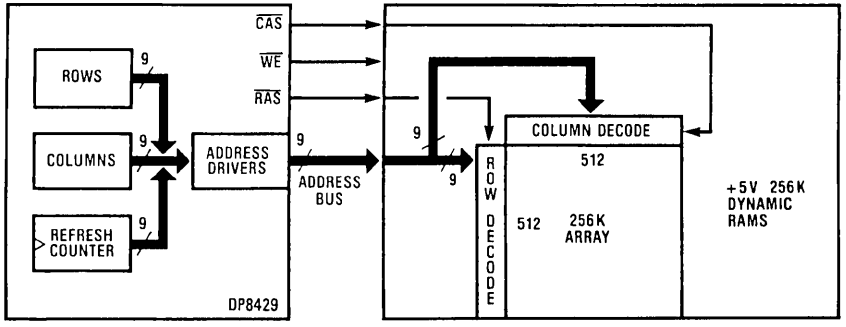
A burst refresh may be performed by holding $\overline{RFSH}$ low and toggling $\overline{RASIN}$ until all rows are refreshed. It may be useful in this case to reset the refresh counter just prior to beginning the refresh. The refresh counter resets to all zeroes when RFI/O is pulled low by an external gate. The refresh counter always counts to 511 before rolling over to zero. If there are 128 or 256 rows being refreshed then Q7 or Q8, respectively, going high may be used as an end-of-burst indicator.

In order that the refresh address is valid on the address outputs prior to the $\overline{RAS}$ lines going low, $\overline{RFSH}$ must go low before $\overline{RASIN}$. The setup time required is given by t_{RFLRL} in the Switching Characteristics. This parameter may be adjusted using *Figure 10* for loading conditions other than those specified.

TABLE III. DP8428/DP8429 Mode Select Options

Mode	($\overline{RFSH}$) M2	M0	Mode of Operation
0	0	0	Externally Controlled Refresh
1	0	1	Auto Refresh–Forced
4	1	0	Externally Controlled Access
5	1	1	Auto Access (Hidden Refresh)

DP8428/DP8429 Interface Between System and DRAM Banks



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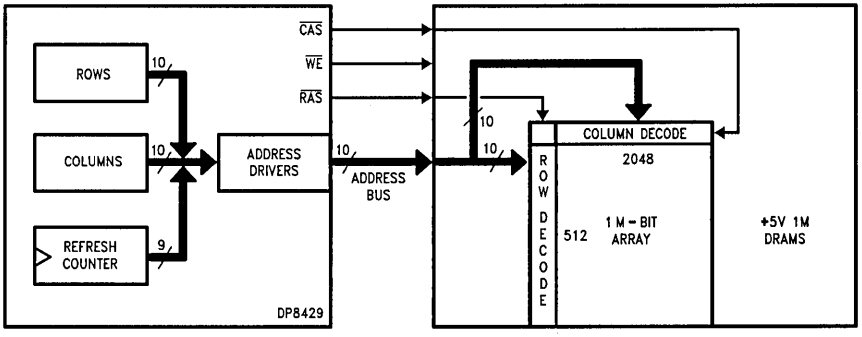
All 9 Bits of Refresh Counter Used

FIGURE 1a. DP8428/DP8429 with 256k DRAMs



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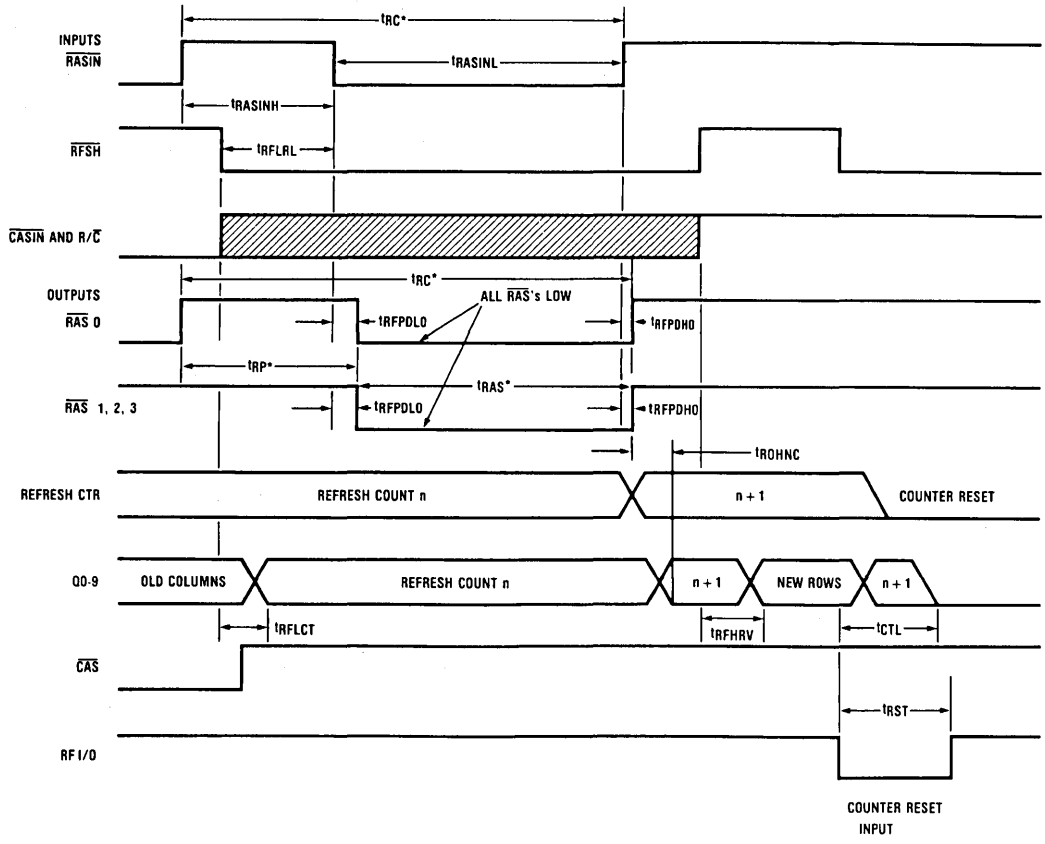
All 9 Bits of Refresh Counter Used

FIGURE 1b. DP8428/DP8429 with 1M DRAMs

DP8428/DP8429 Mode Descriptions (Continued)



*Indicates Dynamic RAM Parameters

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FIGURE 2a. External Control Refresh Cycle (Mode 0)

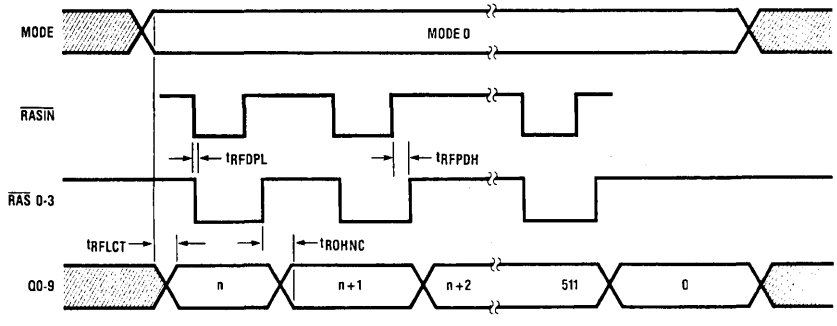

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FIGURE 2b. Burst Refresh Mode 0

DP8428/DP8429 Mode Descriptions (Continued)

MODE 1–AUTOMATIC FORCED REFRESH

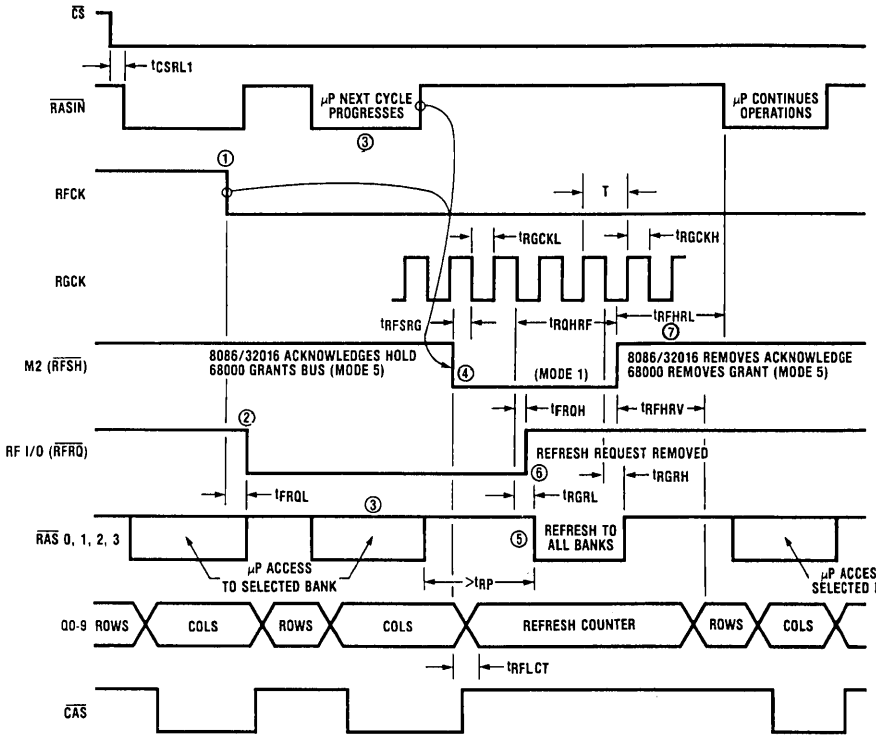
In Mode 1 the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock) and the $\overline{CASIN}$ (RGCK) pin becomes RGCK ($\overline{RAS}$ generator clock). If RFCK is high and Mode 1 is entered then the chip operates as if in MODE 0 (externally controlled refresh), with all $\overline{RAS}$ outputs following $\overline{RASIN}$. This feature of Mode 1 may be useful for those who want to use Mode 5 (automatic access) with externally controlled refresh. By holding RFCK permanently high one need only toggle M2 ($\overline{RFSH}$) to switch from Mode 5 to external refresh. As with Mode 0, RFI/O may be pulled low by an external gate to reset the refresh counter.

When using Mode 1 as automatic refresh, RFCK must be an input clock signal. One refresh should occur each period of RFCK. If no refresh is performed while RFCK is high, then when RFCK goes low RFI/O immediately goes low to indicate that a refresh is requested. (RFI/O may still be used to reset the refresh counter even though it is also used as a refresh request pin, however, an open-collector gate should be used to reset the counter in this case since RFI/O is forced low internally for a request).

After receiving the refresh request the system must allow a forced refresh to take place while RFCK is low. External logic can monitor $\overline{RFRQ}$ (RFI/O) so that when $\overline{RFRQ}$ goes low this logic will wait for the access currently in progress to be completed before pulling M2 ($\overline{RFSH}$) low to put the DP8429 in mode 1. If no access is taking place when $\overline{RFRQ}$ occurs, then M2 may immediately go low. Once M2 is low, the refresh counter contents appear at the address outputs and $\overline{RAS}$ is generated to perform the refresh.

An external clock on RGCK is required to derive the refresh $\overline{RAS}$ signals. On the second falling edge of RGCK after M2 is low, all $\overline{RAS}$ lines go low. They remain low until two more falling edges of RGCK. Thus $\overline{RAS}$ remains high for one to two periods of RGCK after M2 goes low, and stays low for two periods. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the falling edge of RGCK.

The Refresh Request on RFI/O is terminated as $\overline{RAS}$ goes low. This signal may be used to end the refresh earlier than it normally would as described above. If M2 is pulled high



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① RFCK goes low
② $\overline{RFRQ}$ goes low if no hidden refresh occurred while RFCK was high
③ Next $\overline{RASIN}$ starts next access
④ μP acknowledges refresh request
⑤ Forced refresh $\overline{RAS}$ starts after > T (> t_{RP})
⑥ Forced refresh $\overline{RAS}$ ends $\overline{RFRQ}$
⑦ μP removes refresh acknowledge

FIGURE 3. DP8428/DP8429 Performing a Forced Refresh (Mode 5 → 1 → 5) with Various Microprocessors

DP8428/DP8429 Mode Descriptions (Continued)

while the $\overline{RAS}$ lines are low, then the $\overline{RAS}$s go high t_{RFRH} later. The designer must be careful, however, not to violate the minimum $\overline{RAS}$ low time of the DRAMs. He must also guarantee that the minimum $\overline{RAS}$ precharge time is not violated during a transition from mode 1 to mode 5 when an access is desired immediately following a refresh.

If the processor tries to access memory while the DP8429 is in mode 1, WAIT states should be inserted into the processor cycles until the DP8429 is back in mode 5 and the desired access has been accomplished (see *Figure 9*).

Instead of using WAIT states to delay accesses when refreshing, HOLD states could be used as follows. $\overline{RFRQ}$ could be connected to a HOLD or Bus Request input to the system. When convenient, the system acknowledges the $\overline{HOLD}$ or $\overline{Bus\ Request}$ by pulling M2 low. Using this scheme, $\overline{HOLD}$ will end as the $\overline{RAS}$ lines go low (RFI/O goes high). Thus, there must be sufficient delay from the time $\overline{HOLD}$ goes high to the DP8429 returning to mode 5, so that the $\overline{RAS}$ low time of the DRAMs isn't violated as described earlier (see *Figure 3* for mode 1 refresh with Hold states).

To perform a forced refresh the system will be inactive for about four periods of RGCK. For a frequency of 10 MHz, this is 400 ns. To refresh 128 rows every 2 ms an average of about one refresh per 16 μs is required. With a RFCK period of 16 μs and RGCK period of 100 ns, DRAM accesses are delayed due to refresh only 2.5% of the time. If using the Hidden Refresh available in mode 5 (refreshing with RFCK high) this percentage will be even lower.

MODE 4 - EXTERNALLY CONTROLLED ACCESS

In this mode all control signal outputs can be controlled directly by the corresponding control input. The enabled $\overline{RAS}$ output follows $\overline{RASIN}$, $\overline{CAS}$ follows $\overline{CASIN}$ (with R/$\overline{C}$ low), $\overline{WE}$ follows $\overline{WIN}$ and R/$\overline{C}$ determines whether the row or the column inputs are enabled to the address outputs (see *Figure 4*).

With R/$\overline{C}$ high, the row address latch contents are enabled onto the address bus. $\overline{RAS}$ going low strobes the row address into the DRAMs. After waiting to allow for sufficient row-address hold time (t_{RAH}) after $\overline{RAS}$ goes low, R/$\overline{C}$ can go low to enable the column address latch contents onto the address bus. When the column address is valid, $\overline{CAS}$ going low will strobe it into the DRAMs. $\overline{WIN}$ determines whether the cycle is a read, write or read-modify-write access. Refer to *Figures 5a* and *5b* for typical Read and Write timing using mode 4.

Page or Nibble mode may be performed by toggling $\overline{CASIN}$ once the initial access has been completed. In the case of page mode the column address must be changed before

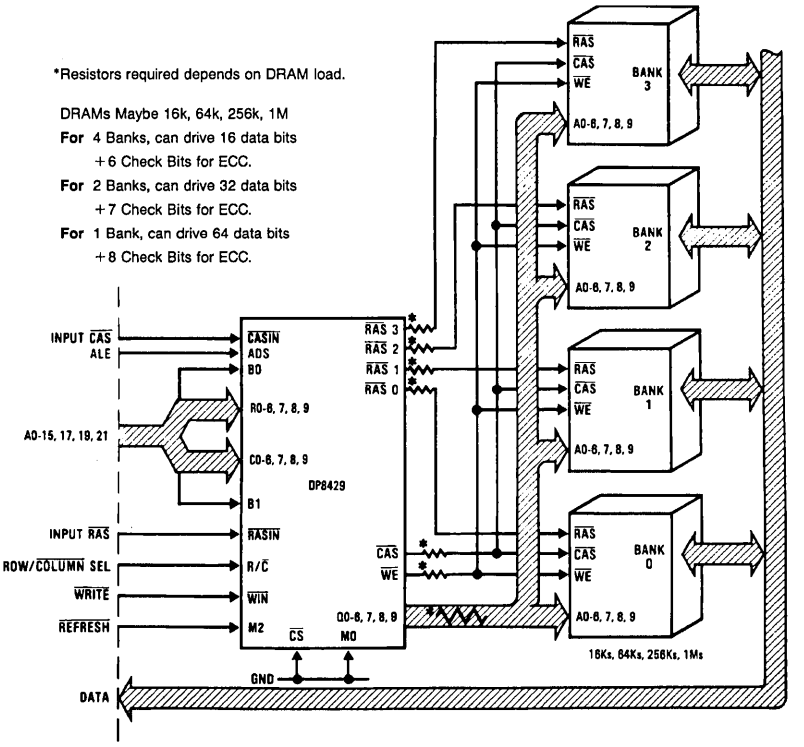

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FIGURE 4. Typical Application of DP8429 Using External Control Access and Refresh in Modes 0 and 4

DP8428/DP8429 Mode Descriptions (Continued)

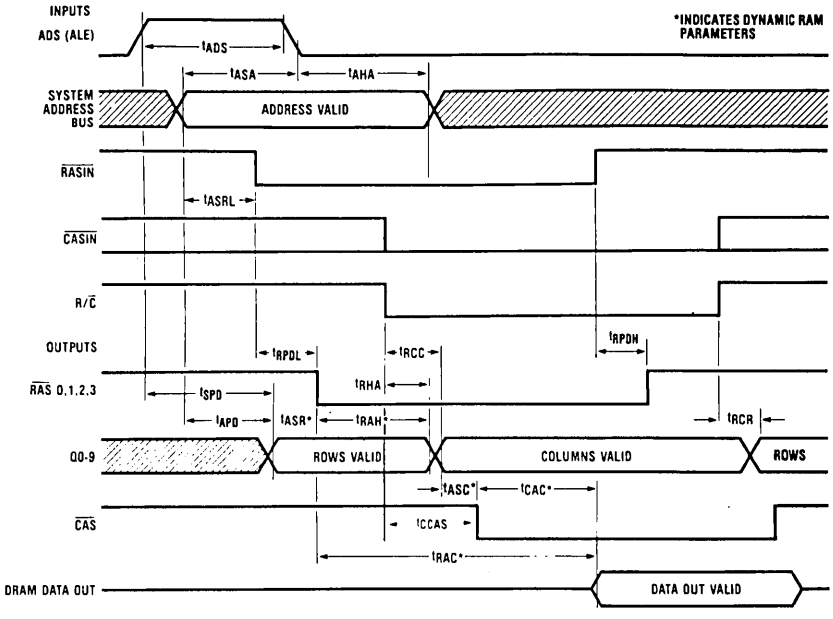

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FIGURE 5a. Read Cycle Timing (Mode 4)

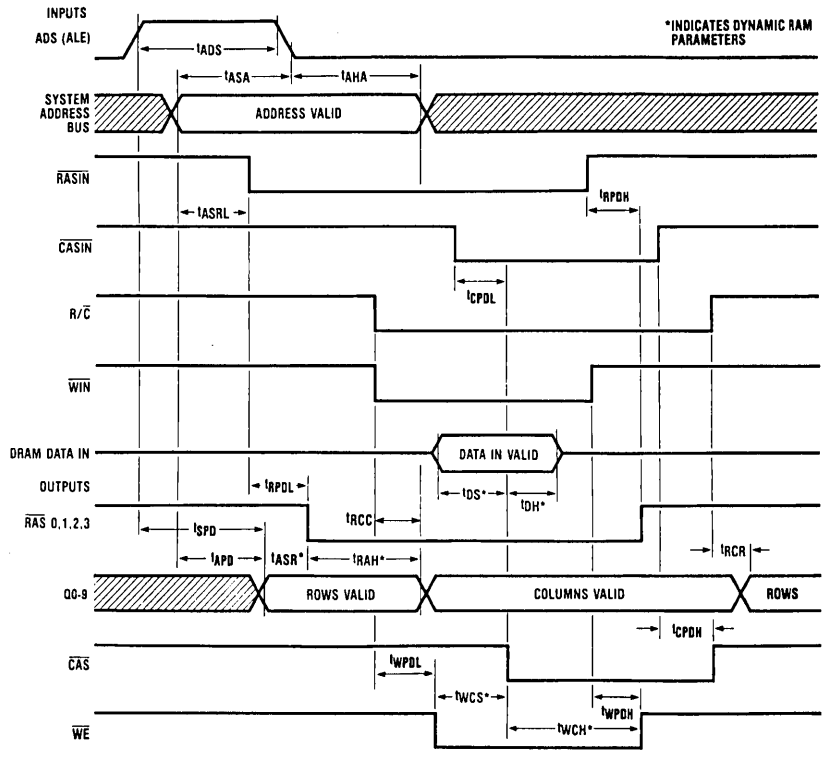

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FIGURE 5b. Write Cycle Timing (Mode 4)

DP8428/DP8429 Mode Descriptions (Continued)

$\overline{CASIN}$ goes low to access a new memory location (see *Figure 5c*). Parameter t_{CPdif} has been specified in order that users may easily determine minimum $\overline{CAS}$ pulse widths when $\overline{CASIN}$ is toggling.

AUTOMATIC $\overline{CAS}$ GENERATION

$\overline{CAS}$ is held high when R/$\overline{C}$ is high even if $\overline{CASIN}$ is low. If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ goes low automatically, t_{ASC} after the column address is valid. This feature eliminates the need for an externally derived $\overline{CASIN}$ signal to control $\overline{CAS}$ when performing a simple access (*Figure 5a* demonstrates Auto-$\overline{CAS}$ generation in mode 4). Page or nibble accessing may be performed as shown in *Figure 5c* even if $\overline{CAS}$ is generated automatically for the initial access.

FASTEST MEMORY ACCESS

The fastest Mode 4 access is achieved by using the automatic $\overline{CAS}$ feature and external delay line to generate the required delay between $\overline{RASIN}$ and R/$\overline{C}$. The amount of delay required depends on the minimum t_{RAH} of the DRAMs being used. The DP8429 parameter t_{DIF1} has been specified in order that the delay between $\overline{RASIN}$ and R/$\overline{C}$ may be minimized.

$$t_{DIF1} = \text{MAXIMUM } (t_{RPDL} - t_{RHA})$$

where t_{RPDL} = $\overline{RASIN}$ to $\overline{RAS}$ delay

and t_{RHA} = row address held from R/$\overline{C}$ going low.

The delay between $\overline{RASIN}$ and R/$\overline{C}$ that guarantees the specified DRAM t_{RAH} is given by

$$\text{MINIMUM } \overline{RASIN} \text{ to R/}\overline{C} = t_{DIF1} + t_{RAH}.$$

Example

In an application using DRAMs that require a minimum t_{RAH} of 15 ns, the following demonstrates how the maximum $\overline{RASIN}$ to $\overline{CAS}$ time is determined.

With t_{DIF1} (from Switching Characteristics) = 7 ns,

$\overline{RASIN}$ to R/$\overline{C}$ delay = 7 ns + 15 ns = 22 ns.

A delay line of 25 ns will be sufficient.

With Auto-$\overline{CAS}$ generation, the maximum delay from R/$\overline{C}$ to $\overline{CAS}$ (loaded with 600 pF) is 46 ns. Thus the maximum $\overline{RASIN}$ to $\overline{CAS}$ time is 71 ns, under the given conditions.

With a maximum $\overline{RASIN}$ to $\overline{RAS}$ time (t_{RPDL}) of 20 ns, the maximum $\overline{RAS}$ to $\overline{CAS}$ time is about 51 ns. Most DRAMs with a 15 ns minimum t_{RAH} have a maximum t_{RCD} of about 60 ns. Thus memory accesses are likely to be $\overline{RAS}$ limited instead of $\overline{CAS}$ limited. In other words, memory access time is limited by DRAM performance, not controller performance.

REFRESHING IN CONJUNCTION WITH MODE 4

If using mode 4 to access memory, mode 0 (externally controlled refresh) must be used for all refreshing.

MODE 5 – AUTOMATIC ACCESS WITH HIDDEN REFRESHING CAPABILITY

Automatic-Access has two advantages over the externally controlled access (mode 4). First, $\overline{RAS}$, $\overline{CAS}$ and the row to column change are all derived internally from one input signal, $\overline{RASIN}$. Thus the need for an external delay line (see mode 4) is eliminated.

Secondly, since R/$\overline{C}$ and $\overline{CASIN}$ are not needed to generate the row to column change and $\overline{CAS}$, these pins can be used for the automatic refreshing function.

AUTOMATIC ACCESS CONTROL

Mode 5 of the DP8429 makes accessing Dynamic RAM nearly as easy as accessing static RAM. Once row and column addresses are valid (latched on the DP8429 if necessary), $\overline{RASIN}$ going low is all that is required to perform the memory access.

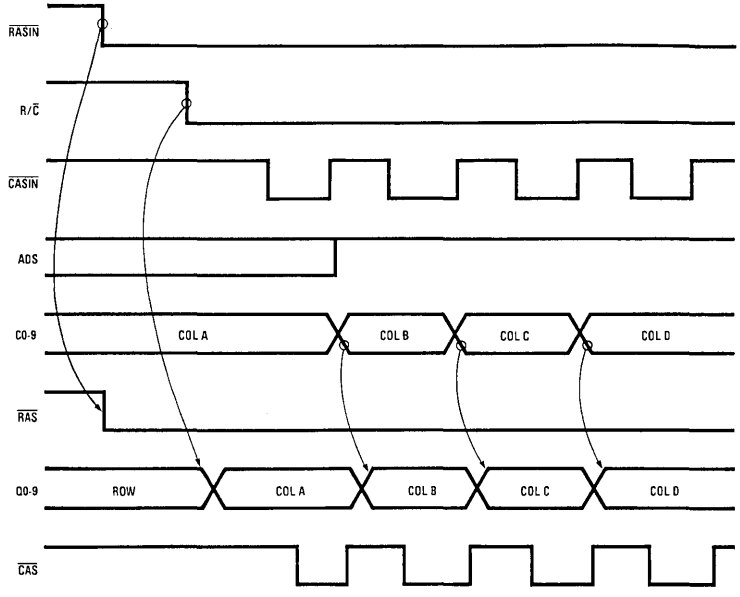

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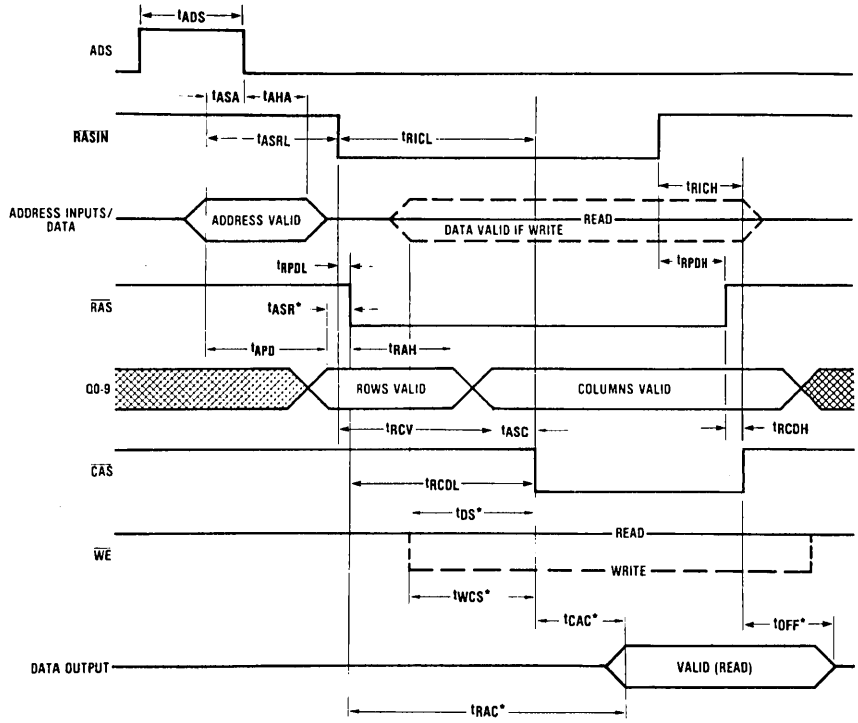
FIGURE 5c. Page or Nibble Access in Mode 4

DP8428/DP8429 Mode Descriptions (Continued)



*Indicates Dynamic RAM Parameters

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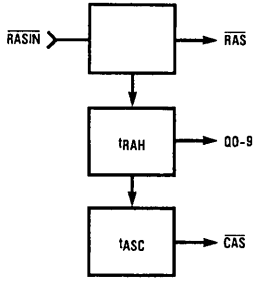
FIGURE 6. Mode 5 Timing

(Refer to *Figure 6*) In mode 5 the selected $\overline{RAS}$ follows $\overline{RASIN}$ immediately, as in mode 4, to strobe the row address into the DRAMs. The row address remains valid on the DP8429 address outputs long enough to meet the t_{RAH} requirement of the DRAMs (pin 4, RAHS, of the DP8429 allows the user two choices of t_{RAH}). Next, the column address replaces the row address on the address outputs and $\overline{CAS}$ goes low to strobe the columns into the DRAMs. $\overline{WIN}$ determines whether a read, write or read-modify-write is done.

The diagram below illustrates mode 5 automatic control signal generation.



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REFRESHING IN CONJUNCTION WITH MODE 5

When using mode 5 to perform memory accesses, refreshing may be accomplished:

(a) externally (in mode 0 or mode 1)

(b) by a combination of mode 5 (hidden refresh) and mode 1 (auto-refresh)

or (c) by a combination of mode 5 and mode 0

(a) Externally Controlled Refreshing in Mode 0 or Mode 1

All refreshing may be accomplished using external refreshes in either mode 0 or mode 1 with R/$\overline{C}$ (RFCK) tied high (see mode 0 and mode 1 descriptions). If this is desired, the system determines when a refresh will be performed, puts the DP8429 in the appropriate mode, and controls the $\overline{RAS}$ signals directly with $\overline{RASIN}$. The on-chip refresh counter is enabled to the address outputs of the DP8429 when the refresh mode is entered, and increments when $\overline{RASIN}$ goes high at the completion of the refresh.

(b) Mode 5 Refreshing (hidden) with Mode 1 refreshing (auto)

(Refer to *Figure 7a*) If RFCK is tied to a clock (see mode 1 description), RFI/O becomes a refresh request output and goes low following RFCK going low if no refresh occurred while RFCK was high. Refreshes may be performed in mode 5 when the DP8429 is not selected for access ($\overline{CS}$ is high) and RFCK is high. If these conditions exist the refresh counter contents appear on the DP8429 address outputs and all $\overline{RAS}$ lines follow $\overline{RASIN}$ so that if $\overline{RASIN}$ goes low (an access other than through the DP8429 occurs), all $\overline{RAS}$ lines go low to perform the refresh. The DP8429 allows only one refresh of this type for each period of RFCK, since RFCK should be fast enough such that one refresh per period is sufficient to meet the DRAM refresh requirement.

DP8428/DP8429 Mode Descriptions (Continued)

Once it is started, a hidden refresh will continue even if RFCK goes low. However, $\overline{CS}$ must be high throughout the refresh (until $\overline{RASIN}$ goes high).

These hidden refreshes are valuable in that they do not delay accesses. When determining the duty cycle of RFCK, the high time should be maximized in order to maximize the probability of hidden refreshes. If a hidden refresh doesn't happen, then a refresh request will occur on RFI/O when RFCK goes low. After receiving the request, the system must perform a refresh while RFCK is low. This may be done by going to mode 1 and allowing an automatic refresh (see mode 1 description). This refresh must be completed while RFCK is low, thus the RFCK low time is determined by the worst-case time required by the system to respond to a refresh request.

(c) Mode 5 Refresh (Hidden Refresh) with mode 0 Refresh (External Refresh)

This refresh scheme is identical to that in (b) except that after receiving a refresh request, mode 0 is entered to do the refresh (see mode 0 description). The refresh request is terminated (RFI/O goes high) as soon as mode 0 is entered. This method requires more control than using mode 1 (auto-refresh), however, it may be desirable if the mode 1 refresh time is considered to be excessive.

Example

Figure 7b demonstrates how a system designer would use the DP8429 in mode 5 based on certain characteristics of his system.

System Characteristics:

1) DRAM used has min t_{RAH} requirement of 15 ns and min t_{ASR} of 0 ns
2) DRAM address is valid from time T_V to the end of the memory cycle
3) four banks of twenty-two 256k memory chips each are being driven

Using the DP8429 (see *Figure 7b*):

1) Tie pin 4 (RAHS) high to guarantee a 15 ns minimum t_{RAH} which is sufficient for the DRAMs being used
2) Generate $\overline{RASIN}$ no earlier than time $T_V + t_{ASRL}$ (see switching characteristics), so that the row address is valid on the DRAM address inputs before $\overline{RAS}$ occurs
3) Tie ADS high since latching the DRAM address on the DP8429 is not necessary
4) Connect the first 20 system address bits to R0-R9 and C0-C9, and bits 21 and 22 to B0 and B1
5) Connect each $\overline{RAS}$ output of the DP8429 to the $\overline{RAS}$ inputs of the DRAMs of one bank of the memory array; connect Q0-Q9 of the DP8429 to A0-A9 of all DRAMs; connect $\overline{CAS}$ of the DP8429 to $\overline{CAS}$ of all the DRAMs

Figure 7c illustrates a similar example using the DP8428 to drive two 32-bit banks.

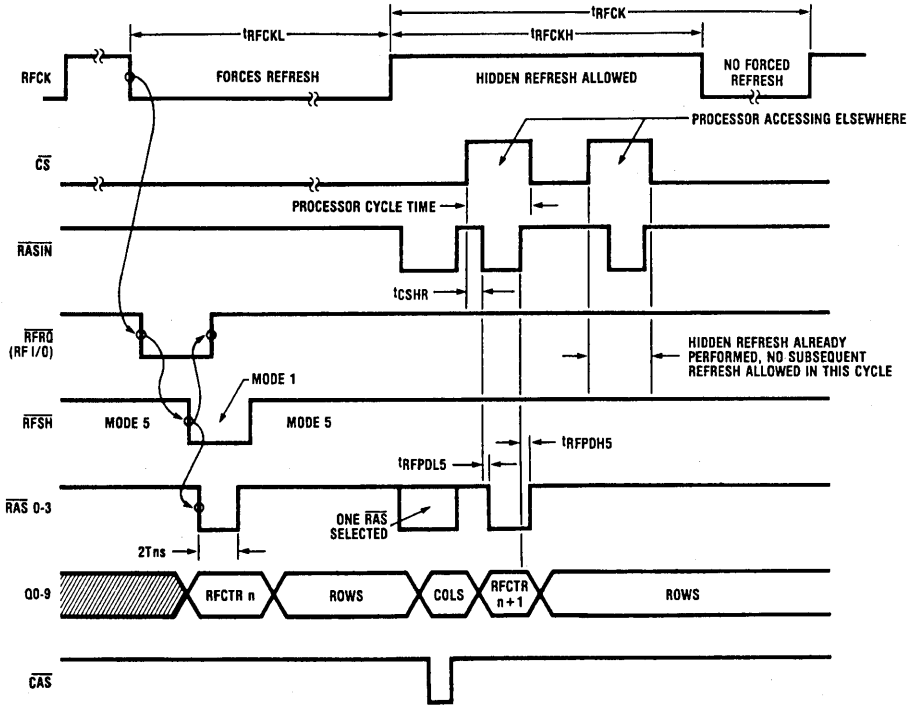

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FIGURE 7a. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

DP8428/DP8429 Mode Descriptions (Continued)

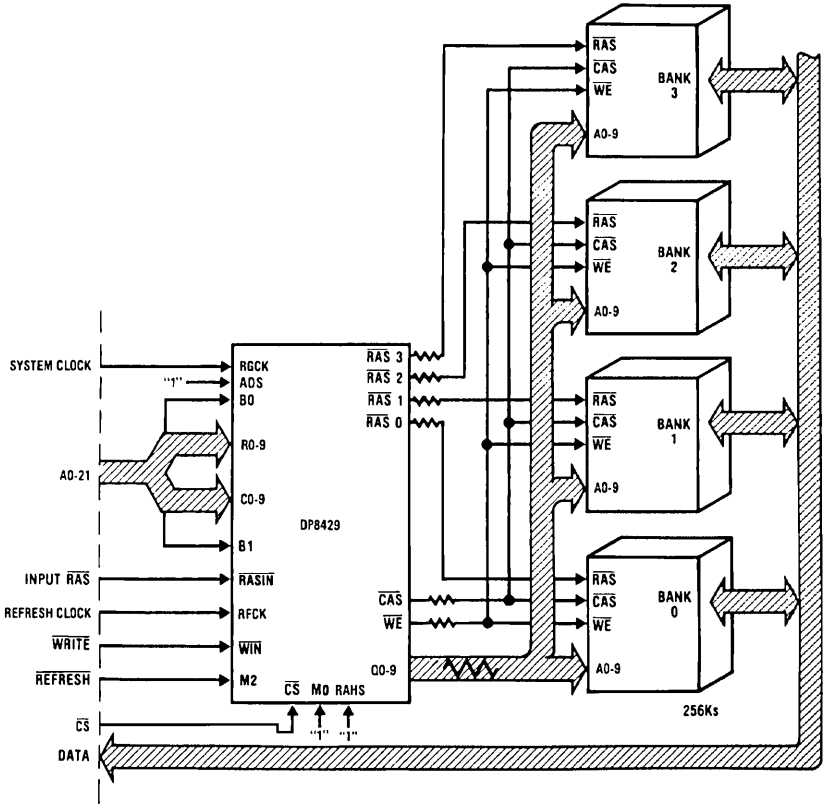

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FIGURE 7b. Typical Application of DP8429 Using Modes 5 and 1

Applications

If one desires a memory interface containing the DP8429 that minimizes the number of external components required, modes 5 and 1 should be used. These two modes provide:

1) Automatic access to memory (in mode 5 only one signal, $\overline{\text{RASIN}}$, is required in order to access memory)
2) Hidden refresh capability (refreshes are performed automatically while in mode 5 when non-local accesses are taking place, as determined by $\overline{\text{CS}}$)
3) Refresh request capability (if no hidden refresh took place while RFCK was high, a refresh request is generated at the RFI/O pin when RFCK goes high)
4) Automatic forced refresh (If a refresh request is generated while in mode 5, as described above, external logic should switch the DP8429 into mode 1 to do an automatic forced refresh. No other external control signals need be issued. WAIT states can be inserted into the processor machine cycles if the system tries to access memory while the DP8429 is in mode 1 doing a forced refresh).

Some items to be considered when integrating the DP8429 into a system design are:

1) The system designer should ensure that a DRAM access not be in progress when a refresh mode is entered. Similarly, one should not attempt to start an access while a refresh is in progress. The parameter t_{RFHRL} specifies the minimum time from $\overline{\text{RFSH}}$ high to $\overline{\text{RASIN}}$ going low to initiate an access.
2) One should always guarantee that the DP8429 is enabled for access prior to initiating the access (see t_{CSRL1}).
3) One should bring $\overline{\text{RASIN}}$ low even during non-local access cycles when in mode 5 in order to maximize the chance of a hidden refresh occurring.
4) At lower frequencies (under 10 Mhz), it becomes increasingly important to differentiate between READ and WRITE cycles. $\overline{\text{RASIN}}$ generation during READ cycles can take place as soon as one knows that a processor READ access cycle has started. WRITE cycles, on the other hand, cannot start until one knows that the data to be written at the DRAM inputs will be valid a setup time before $\overline{\text{CAS}}$ (column address strobe) goes true at the DRAM inputs. Therefore, in general, READ cycles can be initiated earlier than WRITE cycles.
5) Many times it is possible to only add WAIT states during READ cycles and have no WAIT states during WRITE cycles. This is because it generally takes less time to write data into memory than to read data from memory.

Applications (Continued)

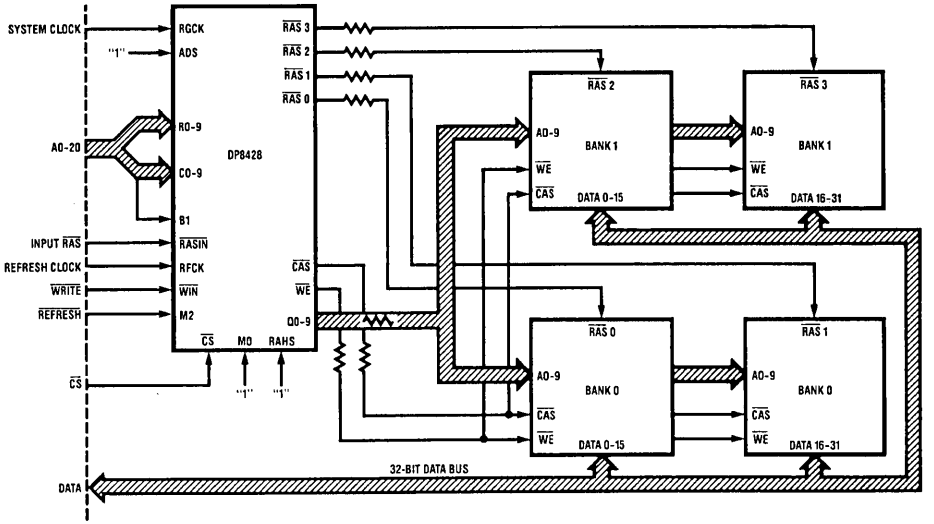

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FIGURE 7c. Typical Application of DP8428 Using Modes 5 and 1

The DP84XX2 family of inexpensive preprogrammed medium Programmable Array Logic devices (PALs) have been developed to provide an easy interface between various microprocessors and the DP84XX family of DRAM controller/drivers. These PALs interface to all the necessary control signals of the particular processor and the DP8429. The PAL controls the operation of the DP8429 in modes 5 and 1, while meeting all the critical timing considerations discussed above. The refresh clock, RFCK, may be divided down from the processor clock using an IC counter such as the DM74LS393 or the DP84300 programmable refresh timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on an input clock of 2 to 10 MHz. *Figure 8* shows a general block diagram for a system using the DP8429 in modes 1 and 5. *Figure 9* shows possible timing diagrams for such a system (using $\overline{\text{WAIT}}$ to prohibit access when refreshing). Although the DP84XX2 PALs are offered as standard peripheral devices for the DP84XX DRAM controller/drivers, the programming equations for these devices are provided so the user may make minor modifications for unique system requirements.

ADVANTAGES OF DP8429 OVER A DISCRETE DYNAMIC RAM CONTROLLER

1) The DP8429 system solution takes up much less board space because everything is on one chip (latches, refresh counter, control logic, multiplexers, drivers, and internal delay lines).
2) Less effort is needed to design a memory system. The DP8429 has automatic modes (1 and 5) which require a minimum of external control logic. Also programmable array logic devices (PALs) have been designed which allow an easy interface to most popular microprocessors (Motorola 68000 family, National Semiconductor 32032 family, Intel 8086 family, and the Zilog Z8000 family).
3) Less skew in memory timing parameters because all critical components are on one chip (many discrete drivers specify a minimum on-chip skew under worst-case conditions, but this cannot be used if more then one driver is needed, such as would be the case in driving a large dynamic RAM array).
4) Our switching characteristics give the designer the critical timing specifications based on TTL output levels (low = 0.8V, high = 2.4V) at a specified load capacitance. All timing parameters are specified on the DP8429:
   A) driving 88 DRAM's over a temperature range of 0–70 degrees centigrade (no extra drivers are needed).
   B) under worst-case driving conditions with all outputs switching simultaneously (most discrete drivers on the market specify worst-case conditions with only one output switching at a time; this is not a true worst-case condition!).

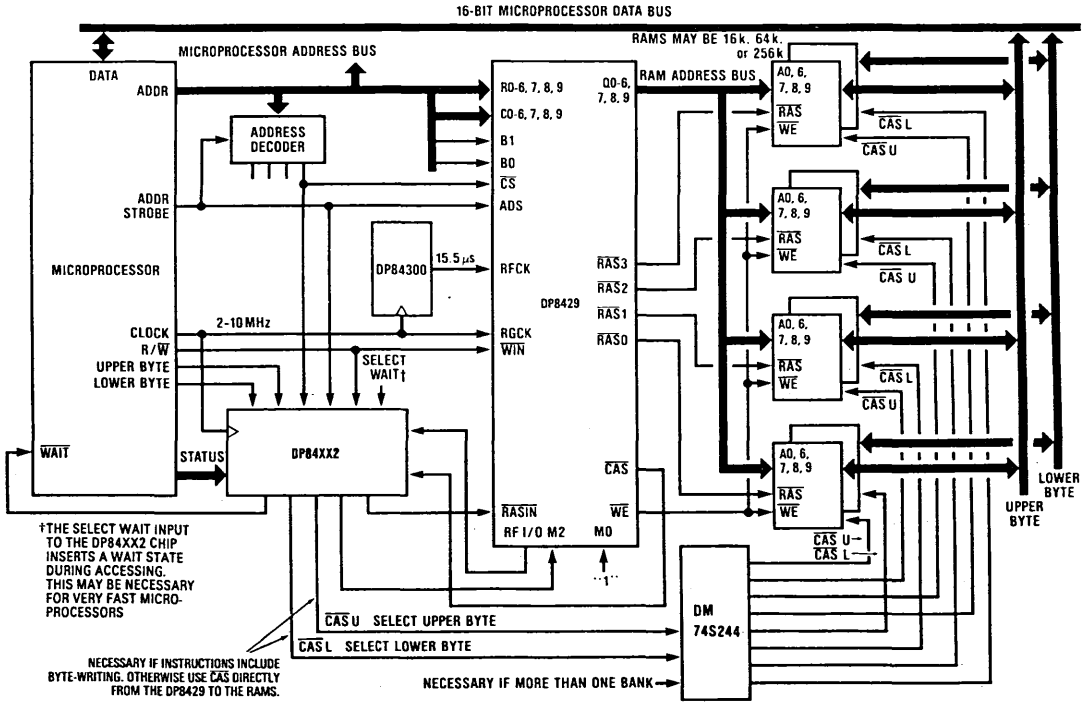

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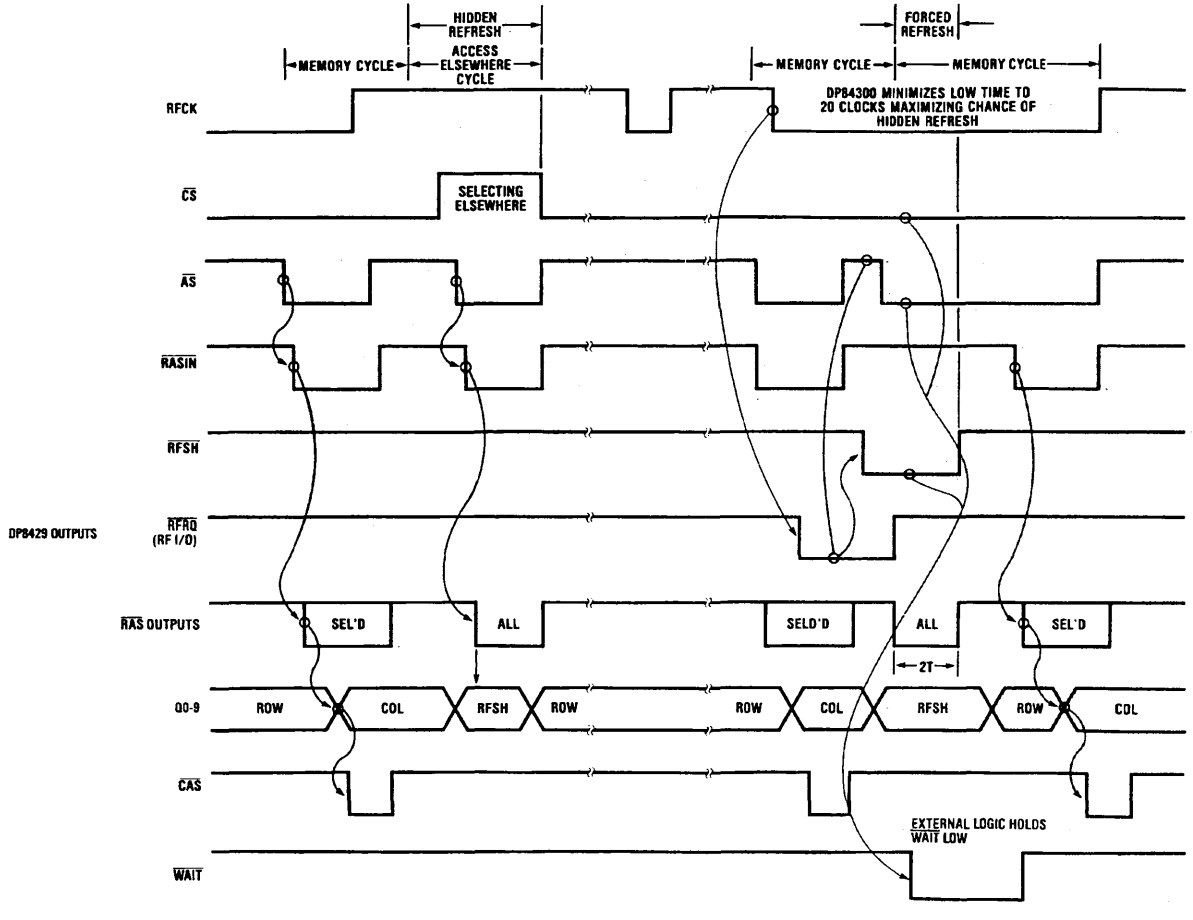
FIGURE 8. Connecting the DP8429 Between the 16-bit Microprocessor and Memory



*T is microprocessor's clock period

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FIGURE 9. DP8429 Auto Refresh, Access with $\overline{\text{WAIT}}$ States

Switching Characteristics

All A. C. parameters are specified with the equivalent load capacitances, including traces, of 88 DRAMs organized as 4 banks of 22 DRAMs each. Maximums are based on worst-case conditions including all outputs switching simultaneously. This, in many cases, results in the AC valves shown in the DP84XX DRAM controller data sheet being much looser than true worst case maximum AC delays. The system designer should estimate the DP8429 load in his/her application, and modify the appropriate A. C. parameters using the graph in *Figure 10*. Two example calculations are provided below.

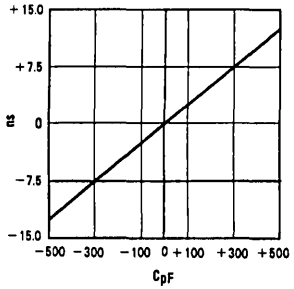

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FIGURE 10. Change in Propagation Delay relative to "true" (application) load minus AC specified data sheet load

Examples

1) A mode 4 user driving 2 banks of DRAM has the following loading conditions:

   $\overline{CAS}$ - 300 pF

   Q0–Q9 - 250 pF

   $\overline{RAS}$ - 150 pF

A.C. parameters should be adjusted in accordance with *Figure 10* and the specifications given for the 88 DRAM load as follows:

max t_{RPDL} = 20 ns − 0 ns = 20 ns (since $\overline{RAS}$ loading is the same as that which is spec'ed)

max t_{CPDL} = 32 ns − 7 ns = 25 ns

max t_{CCAS} = 46 ns − 7 ns = 39 ns

max t_{RCC} = 41 ns − 6 ns = 35 ns

min t_{RHA} is not significantly effected since it does not involve an output transition

Other parameters are adjusted in a similar manner.

2) A mode 5 user driving one bank of DRAM has the following loading conditions:

   $\overline{CAS}$ - 120 pF

   Q0–Q9 - 100 pF

   $\overline{RAS}$ - 120 pF

A. C. parameters should be adjusted as follows:

with RAHS = "1",

max t_{RICL} = 70 ns − 11 ns = 59 ns

max t_{RCDL} = 55 ns + 1 ns − 11 ns = 45 ns

(the + 1 ns is due to lighter $\overline{RAS}$ loading; the − 11 ns is due to lighter $\overline{CAS}$ loading)

min t_{RAH} = 15 ns + 1 ns = 16 ns

The additional 1 ns is due to the fact that the $\overline{RAS}$ line is driving less (switching faster) than the load to which the 15 ns spec applies. The row address will remain valid for about the same time irregardless of address loading since it is considered to be not valid at the beginning of its transition.

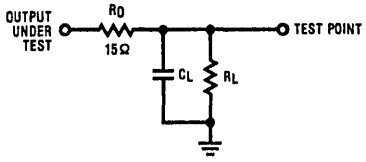

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FIGURE 11. Output Load Circuit

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150 mA
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

		Min	Max	Units
V_{CC}	Supply Voltage	4.50	5.50	V
T_A	Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min, I_C = − 12 mA		− 0.8	− 1.2	V
I_{IH}	Input High Current for all Inputs	V_{IN} = 2.5V		2.0	100	μA
I_I RSI	Output Load Current for RFI/O	V_{IN} = 0.5V, Output high		−0.7	−1.5	mA
I_{IL1}	Input Low Current for all Inputs**	V_{IN} = 0.5V		−0.02	−0.25	mA
I_{IL2}	ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	I_{OL} = 20 mA		0.3	0.5	V
V_{OL2}	Output Low Voltage for RFI/O	I_{OL} = 8 mA		0.3	0.5	V
V_{OH1}	Output High Voltage*	I_{OH} = − 1 mA	2.4	3.5		V
V_{OH2}	Output High Voltage for RFI/O	I_{OH} = − 100 μA	2.4	3.5		V
I_{1D}	Output High Drive Current*	V_{OUT} = 0.8V (Note 3)	−50	− 200		mA
I_{0D}	Output Low Drive Current*	V_{OUT} = 2.4V (Note 3)	50	200		mA
I_{CC}	Supply Current	V_{CC} = Max		150	240	mA

*Except RFI/O

**Except RFI/O, ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$

Switching Characteristics: DP8428 and DP8429

V_{CC} = 5.0V ± 10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5), the output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q9, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11* for test load. Maximum propagation delays are specified with all outputs switching.**

**** Preliminary**

Symbol	Access Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
t_{RICL0}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8428-80/29-80	57	97	42	85	ns
t_{RICL0}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8428-70/29-70	57	87	42	75	ns
t_{RICL1}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8428-80/29-80	48	80	35	68	ns
t_{RICL1}	$\overline{RASIN}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8428-70/29-70	48	70	35	58	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ High Delay	*Figure 6*		37			ns
t_{RCDL0}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8428-80/29-80	43	80			ns
t_{RCDL0}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 0)	*Figure 6* DP8428-70/29-70	43	72			ns

Switching Characteristics: DP8428 and DP8429 (Continued)

V_{CC} = 5.0V ± 10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5), the output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q9, C_L = 500 pF; $\overline{RAS}$0-$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11* for test load. Maximum propagation delays are specified with all outputs switching.**

**** Preliminary**

Symbol	Access Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
t_{RCDL1}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8428-80/29-80	34	63			ns
t_{RCDL1}	$\overline{RAS}$ to $\overline{CAS}$ Low Delay (RAHS = 1)	*Figure 6* DP8428-70/29-70	34	55			ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ High Delay	*Figure 6*		22			ns
t_{RAH0}	Row Address Hold Time (RAHS = 0, Mode 5)	*Figure 6*	25		25		ns
t_{RAH1}	Row Address Hold Time (RAHS = 1, Mode 5)	*Figure 6*	15		15		ns
t_{ASC}	Column Address Set-up Time (Mode 5)	*Figure 6*	0		0		ns
t_{RCV0}	$\overline{RASIN}$ to Column Address Valid (RAHS = 0, Mode 5)	*Figure 6* DP8428-80/29-80		94			ns
t_{RCV0}	$\overline{RASIN}$ to Column Address Valid (RAHS = 0, Mode 5)	*Figure 6* DP8428-70/29-70		85			ns
t_{RCV1}	$\overline{RASIN}$ to Column Address Valid (RAHS = 1, Mode 5)	*Figure 6* DP8428-80/29-80		76			ns
t_{RCV1}	$\overline{RASIN}$ to Column Address Valid (RAHS = 1, Mode 5)	*Figure 6* DP8428-70/29-70		68			ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay	*Figures 5a, 5b, 6*		21		18	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay	*Figures 5a, 5b, 6*		20		17	ns
t_{ASRL}	Address Set-up to $\overline{RASIN}$ low	*Figures 5a, 5b, 6*	13				ns
t_{APD}	Address Input to Output Delay	*Figures 5a, 5b, 6*		36		25	ns
t_{SPD}	Address Strobe High to Address Output Valid	*Figures 5a, 5b*		48			ns
t_{ASA}	Address Set-up Time to ADS	*Figures 5a, 5b, 6*	5				ns
t_{AHA}	Address Hold Time from ADS	*Figures 5a, 5b, 6*	10				ns
t_{ADS}	Address Strobe Pulse Width	*Figures 5a, 5b, 6*	26				ns
t_{WPD}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 5b*		28			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Low Delay (R/$\overline{C}$ low, Mode 4)	*Figure 5b*	21	32			ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ High Delay (R/$\overline{C}$ low, Mode 4)	*Figure 5b*	16	33			ns
t_{CPdif}	t_{CPDL} - t_{CPDH}	See Mode 4 Description		11			ns
t_{RCC}	Column Select to Column Address Valid	*Figure 5a*		41			ns
t_{RCR}	Row Select to Row Address Valid	*Figures 5a, 5b*		45			ns
t_{RHA}	Row Address Held from Column Select	*Figure 5a*	7				ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low Delay ($\overline{CASIN}$ Low, Mode 4)	*Figure 5a* DP8428-80/29-80		50			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low Delay ($\overline{CASIN}$ Low, Mode 4)	*Figure 5a* DP8428-70/29-70		46			ns
t_{DIF1}	Maximum (t_{RPDL} - t_{RHA})	See Mode 4 Description		7			ns
t_{DIF2}	Maximum (t_{RCC} - t_{CPDL})			13			ns

Switching Characteristics: DP8428 and DP8429 (Continued)

V_{CC} = 5.0V ± 10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q9, C_L = 500 pF; $\overline{RAS}$0-$\overline{RAS}$3, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11* for test load. Maximum propagation delays are specified with all outputs switching.**

****Preliminary**

Symbol	Refresh Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
t_{RC}	Refresh Cycle Period	*Figure 2a*	100				ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2a*	50				ns
t_{RFPDL0}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay during Refresh (Mode 0)	*Figure 2a*		28			ns
t_{RFPDL5}	$\overline{RASIN}$ to $\overline{RAS}$ Low Delay during Hidden Refresh	*Figure 7*		38			ns
t_{RFPDH0}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay during Refresh (Mode 0)	*Figure 2a*		35			ns
t_{RFPDH5}	$\overline{RASIN}$ to $\overline{RAS}$ High Delay during Hidden Refresh	*Figure 7*		44			ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	*Figures 2a, 3* $\overline{CS}$ = X		38			ns
t_{RFLRL}	$\overline{RFSH}$ Low Set-up to $\overline{RASIN}$ Low (Mode 0), to get Minimum t_{ASR} = 0	*Figure 2a*	12				ns
t_{RFHRL}	$\overline{RFSH}$ High Setup to Access $\overline{RASIN}$ Low	*Figure 3*	25				ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figure 3*		43			ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figure 2a*		42			ns
t_{RST}	Counter Reset Pulse Width	*Figure 2a*	46				ns
t_{CTL}	RFI/O Low to Counter Outputs All Low	*Figure 2a*		80			ns
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	*Figure 7*	100				ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	30				ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	15				ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	15				ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ (RFI/O) Low	*Figure 3* C_L = 50 pF RL = 35k		66			ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	*Figure 3* C_L = 50 pF RL = 35k		55			ns

Switching Characteristics: DP8428 and DP8429 (Continued)

V_{CC} = 5.0V ± 10%, 0°C ≤ T_A ≤ 70°C unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs, including trace capacitance.

*** These values are Q0-Q9, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF; RL = 500Ω unless otherwise noted. See *Figure 11* for test load. Maximum propagation delays are specified with all outputs switching.**

****Preliminary**

Symbol	Refresh Parameter	Condition	*CL		**All C_L = 50 pF		Units
			Min	Max	Min	Max	
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	21	41			ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	23	48			ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from RGCK	*Figure 3*	2T				ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (Ending Forced Refresh early)	(See Mode 1 Description)		42			ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	(See Mode 1 Description) *Figure 3*	12				ns
t_{CSHR}	$\overline{CS}$ High to $\overline{RASIN}$ Low for Hidden Refresh	*Figure 7*	10				ns
t_{CSRL1} for DP8429	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	34				ns
t_{CSRL1} for DP8428	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Mode 5 with Auto Refresh Mode)	*Figure 3*	5				ns
t_{CSRL0}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low (Using Modes 4 or 5 with externally controlled Refresh)	(See Mode 5 Description)	5				ns
t_{RKRL}	RFCK High to $\overline{RASIN}$ low for hidden Refresh		50				ns

Input Capacitance T_A = 25°C (Note 2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$, $\overline{CS}$, M2, $\overline{RASIN}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V Output reference points are 2.4V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.

National Semiconductor Corporation

FUTURE PRODUCT

DP8420/DP8422 Programmable 1 and 4 Megabit Dynamic RAM Controller/Driver(s)

General Description

The DP8420/22 DRAM Controller(s) provide single-chip interfaces between Dynamic RAM and all popular 8-, 16-, and 32-bit microprocessors. Each device is easily programmmed so that its control logic configuration(s) may be optimized for use with virtually any manufacturer's microprocessors, eliminating the need for any external support circuits.

The DP8420/22 generate all required access control signal timing and automatically refresh all DRAMs as required. Furthermore, each device performs all access/refresh arbitration. Control signal pulse widths are adjustable so that system timing may be optimized for any operating frequency.

The DP8420 is packaged in a 68-pin Plastic Chip Carrier (PCC). The DP8422 has most of the features of the DP8420 plus the additional control signals necessary to perform dual-porting and 4 megabit DRAM addressing.

Features

- Controls all Dynamic RAMs including 4 Mbit DRAMs
- Allows no-wait state operation at processor clock frequencies of 10 MHz and above
- Supports clock frequencies above 20 MHz
- Can directly address up to 32 Mbytes of Dynamic RAM
- On board access/refresh arbitration logic
- Direct interface to all major microprocessors
- CMOS process for low power consumption
- Programmable WAIT/DATA ACKNOWLEDGE output
- Adjustable RAS and CAS pulse widths
- Byte write capability up to 32 bits
- Programmable DRAM row address hold time and column address setup time
- Programmable RAS low time during refresh
- Programmable RAS precharge time
- Precise on-board delay line
- Programmable refresh period
- Burst refresh available
- Support for error detection and correction including scrubbing during refresh cycles
- 4 RAS and 4 CAS drivers
- Programmable RAS/CAS configuration
- Allows synchronous or asynchronous operation
- Supports all nibble and page modes of operation
- Support for memory interleaving
- Automatic column generation on-chip allows multiple word accesses within a page after the initial address is specified
- Support for staggered refresh

Precautions to Take When Driving Memories

National Semiconductor
Application Note 305
Mike Evans

As memory prices continue their relentless reduction of cost per bit, more and more systems designers are incorporating memories into their designs. In general these memories comprise a number of dynamic RAMs, such as the 64k x 1. In this x 1 configuration, the number of RAMs required is a multiple of the bus width. Most new system designs use 16-bit microprocessors, so that a typical memory will comprise from 16 to 64 DRAMs, thus providing from 64k to 256k addressing capability. This means the memory drivers have to drive upwards of 16 RAMs. The drivers may be part of an integrated circuit dynamic RAM controller such as the DP8408A/DP8409A, or they may be on a separate chip such as the DP84240/DP84244 octal memory drivers. The recommendations in this article are valid for any type of memory driver. The purpose of the article is to forewarn new designers using memories of problems they will encounter if adequate precautions are not taken.

A typical configuration of a 16-bit wide memory is shown in *Figure 1*. Each driver address output goes to every dynamic RAM, as does $\overline{WE}$. $\overline{CAS}$ outputs go to half the number of RAMs assuming byte writing is required. $\overline{RAS}$ outputs each go only to one bank. Note that these loads are not true for the data inputs and outputs. Each data I/O only connects to its respective bit, so the loading is only one RAM per bank for data. In general, this is why buffers are not required on the data bus when interfacing to memory. Data In of the RAMs can be linked directly to Data Out for any one bit, and also to the corresponding bit on the data bus. This is true for normal read and write operations, but if read-modify-write cycles are employed, the Data Out signals must be buffered from the data bus.

Using this typical memory configuration may not be as simple as it seems. Without care and attention, problems can arise for the unprepared, and there are two areas in particular which may cause memory errors or memory damage: one is voltage overshoot caused by inductive traces and high capacitive loads, the other is switching spikes caused by switching high capacitive loads.

OVERSHOOT AND UNDERSHOOT

(Undershoot is Negative Overshoot)

When a system requires a number of dynamic RAMs, the result is high capacitance loads, caused by a combination of RAM input capacitance and trace capacitance. Each dynamic RAM has a specified input capacitance of 10 pF maximum, but most dynamic RAMs are closer to 2 to 3 pF. Very few actually get close to 10 pF, even under worst case conditions of high temperature and V_{CC}. It is safe, therefore, to assume a much lower average input capacitance when using 16 or more RAMs.

In fact, the input capacitance of most inputs is due more to the package than the input gating, because the silicon gate inputs of the transistors in today's market have such high impedance. A typical maximum would be 2.5 pF. Control inputs such as $\overline{RAS}$ and $\overline{CAS}$ connect to more than one transistor input. For example, on the National Semiconductor 64k x 1 dynamic RAM, the NMC4164, $\overline{RAS}$ goes to two transistors and $\overline{CAS}$ to four. In general, this is true for most manufacturers' RAMs, so a more typical maximum input capacitance would be 3 pF for $\overline{RAS}$ and 3.5 pF for $\overline{CAS}$. RAM input currents are so small as to be negligible. The input current is quoted as 10 μA maximum, but again most RAMs are much less than this in a typical memory. Driving DRAMs, therefore, is not a problem of DC drive capability, but rather a problem of capacitance drive capability.

Driving DRAM input capacitance is further compounded by printed circuit traces, and even more so by wire-wrapping. Both can be represented by a transmission line with distributed capacitance and inductance. Thus, the total load is equivalent to a complex impedance comprising the distributed trace inductance, and a capacitance comprising distributed trace capacitance and RAM input capacitance as shown in *Figure 2a*.

The effect is an overshoot or undershoot at the dynamic RAM inputs that occurs each time a memory driver changes state, as shown in *Figure 2b*. As the driver output changes state, the load capacitance cannot be instantaneously charged or discharged because the current available is limited both by the driver transistor impedance, and the equivalent series resistance from the supply rail through the chip to the trace resistance. This current will be similar in value to the quoted short circuit current of the driver stage; therefore there is a spike of current that lasts as long as it takes to change the voltage of all the capacitances. For the driver stages of the DP8408A/DP8409A, or the DP84240/DP84244, the typical short circuit current is 100 mA per stage. This is true for either direction, so that the high-to-low transition takes roughly the same time as the low-to-high transition, minimizing skew times on all the driver outputs, as they transition in either direction. Assuming the output low voltage, V_{OL}, is 0.2V and the output high voltage, V_{OH}, is 3.2V, and that the charge/discharge current is constant at I_{SC}, then the current spike will exist for a time, T, where,

$$T = C_{IL} \times (V_{OH} - V_{OL})/I_{SC}$$
$$= 500\ pF \times 3.0V/100\ mA = 15\ ns$$

C_L (500 pF) is the load capacitance of typically 64 to 88 dynamic RAMs, in other words, four banks comprising 16 data bits and possibly six check bits if error correction is required.

In fact, due to the trace inductance, the rate of change of current will not be a step function, so that the current waveform looks like a spike. Even so, the rapid rate of change of current, di/dt, into the trace inductance L, will create a potentially excessive voltage "e" across this inductance. As an example, if the current changes from 0 to 100 mA in 6 ns, and the composite trace inductance is 0.3 μH, then the voltage across this inductance is "e,"where,

$$e = L\ di/dt$$
$$= 0.3\ \mu H \times 100\ mA/6\ ns = 5V$$

In other words, at this rate of change in current, even a small inductance can be dangerous for two reasons. First, the dynamic RAMs at the far end of the trace could be destroyed, unless they have clamping diodes to V_{CC} and GND (most do not), or second, the returning voltage may exceed the threshold it has just passed causing a second

and then third change of state. If this sudden glitch occurs on a control signal input such as $\overline{RAS}$, the memory contents may be inadvertently changed.

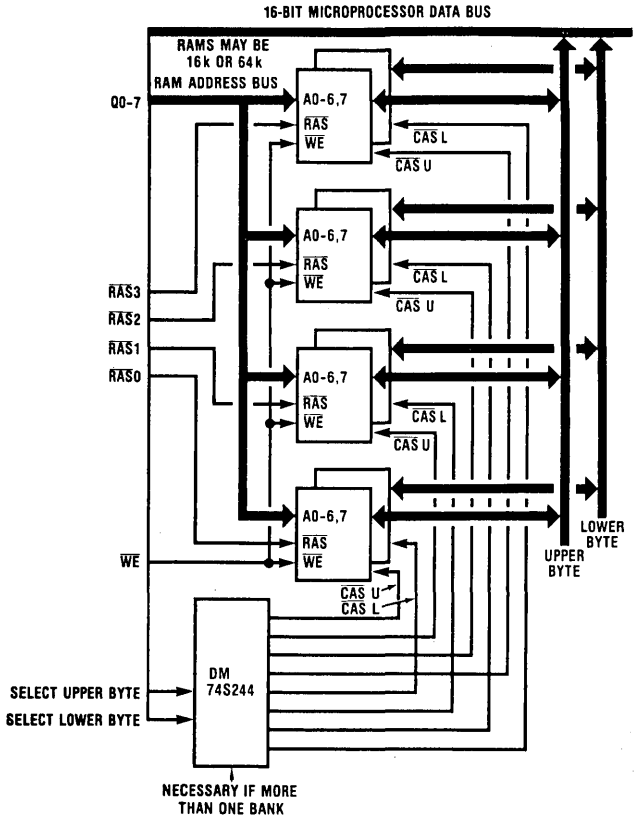
It is therefore necessary to remove the spike. The most common approach is to insert a damping resistor in the path between the driver and the RAMs, fairly close to the driver, as shown by R_D in *Figure 2a*. The best value for the resistor is the critical value giving a critically damped transition. Too high a value will cause overdamping which results in a slow transition. This slow edge may create excessive skew problems and slow down the memory cycle, or even worse, the edge may be slow enough that the RAM cycle never begins internally. If the damping resistor value is too low, the undershoot or overshoot may not be removed. It is therefore recommended that the resistor be determined on the first prototypes (not wire-wrapped prototypes because the value will be different due to the larger distributed inductance and capacitance). Also, the values may be different for the control lines, particularly $\overline{CAS}$. If there are a number of banks, and a $\overline{RAS}$ is used to select each bank, then the damping resistor in this line will be higher.

Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading, the higher the values.

Some IC manufacturers offer octal memory drivers with on-chip series resistors fixed at ≈25Ω. Unless this is the critical value required for all the lines, problems will arise. The DP8400 family has been designed with equivalent internal values of approximately 10Ω, allowing for any external value of damping resistor.

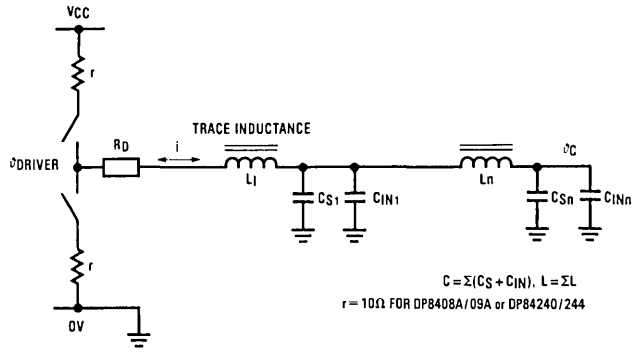
SWITCHING CURRENT SPIKES

Another major undesirable effect of the fast current spikes is the effect on the V_{CC} and GND pins. The worst case is when all eight or nine address outputs switch in the same direction at the same time, as shown in *Figure 3a*. If each driver can source or sink 100 mA, then a current of approximately 1A could enter or exit the driver chip in a period of 20 ns. The resistance and inductance of the V_{CC} and GND lines to the chip can cause excessive drops during this switching time (see waveforms in *Figure 3a*), which may, in turn, upset latches either in the DP8408A/DP8409A, or externally. A ceramic capacitor connected across V_{CC} and GND pins will largely remove the spike. A 1 μF multilayer ceramic is recommended. This should be fitted as close as possible to the pins in order to reduce lead inductance. The DP8408A/DP8409A pin configuration facilitates this with



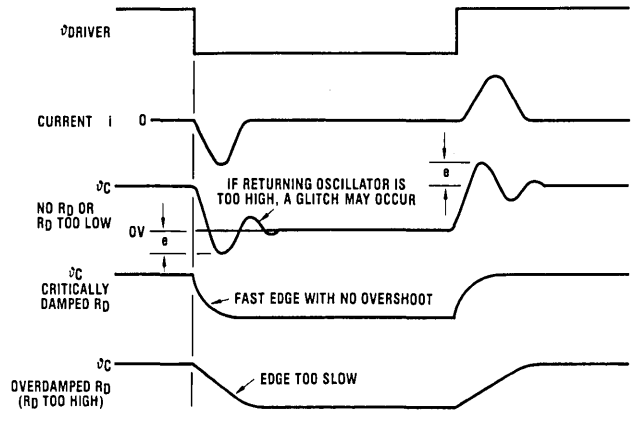
TL/F/5031–1

FIGURE 1. Typical 16-Bit Memory with Byte Write Address



TL/F/5031-2

FIGURE 2a. Complex Load Impedance Caused by Distributed Trace Inductance L and Capacitance C_S, and RAM Input Capacitance C_{IN}



TL/F/5031-3

FIGURE 2b. Timing Waveforms Showing the Effect of Variations of R_D on Signals Appearing at the RAM

GND and V_{CC} pins 0.2" apart so that the ceramic capacitor can be fitted as close to the chip as possible. The second GND pin should also be decoupled. These GND and V_{CC} pins are located in the center of the package to reduce bonding lead lengths. In fact, the lead resistance is five times lower than if the supply pins were in the corners. An example of how this spike can be reduced would be the previous example of a 1A change in supply current switching in 20 ns with a 1 μF ceramic capacitor decoupling GND and V_{CC}. The voltage drop "v" is 1A$\times$20 ns/1 μF, or 20 mV.

If the decoupling capacitor was 0.01 μF, the drop would be 2V. Tantalum or other types of capacitors are lower frequency capacitors and have only a small effect in reducing the voltage spike. Ceramic capacitors are high frequency, and multilayer capacitors with lower inductance have a greater effect in reducing the voltage spike and are therefore recommended. As a further recommendation, the dynamic RAMs should be similarly decoupled with approximately a 0.1 μF ceramic capacitor on each RAM. Wire-wrapped boards, in particular, need special attention.

There are some other precautions that may be considered when driving memories. First, be aware that IC sockets increase load capacitance and inductance, so it becomes a matter of the importance of removability of chips, and maintainability. Also, shorter, thicker trace lengths will reduce the load, and good GND and V_{CC} connections will help reduce the voltage spikes around the memory board. For wire-wrapped designs, GND and V_{CC} should be multiwired.

With proper decoupling and correct selection of damping resistors, integrated circuit dynamic RAM controllers will function as expected to ease the burden of the system designer.

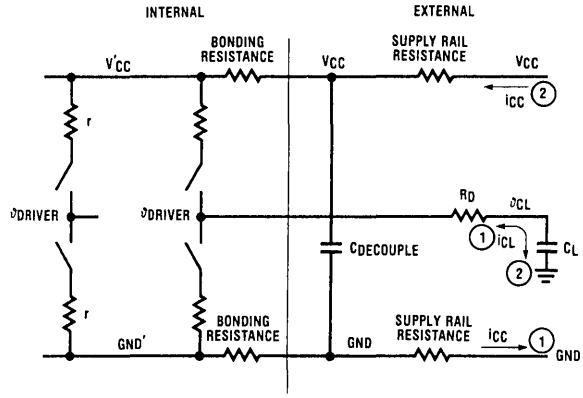


FIGURE 3a. Effect of Switching All Outputs Simultaneously in the Same Direction

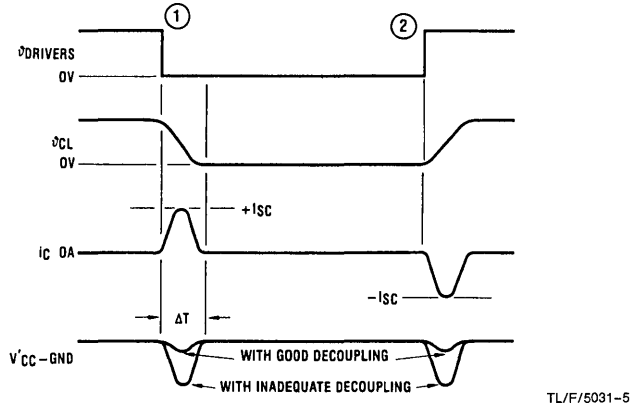


FIGURE 3b. Timing Waveforms Showing Internal Supply Rail Drops During Output Switching

Determining the Speed of the Dynamic RAM Needed When Interfacing the DP8419-80 to Most Major Microprocessors

National Semiconductor
Application Note 411
Webster (Rusty) Meier Jr.

INTRODUCTION

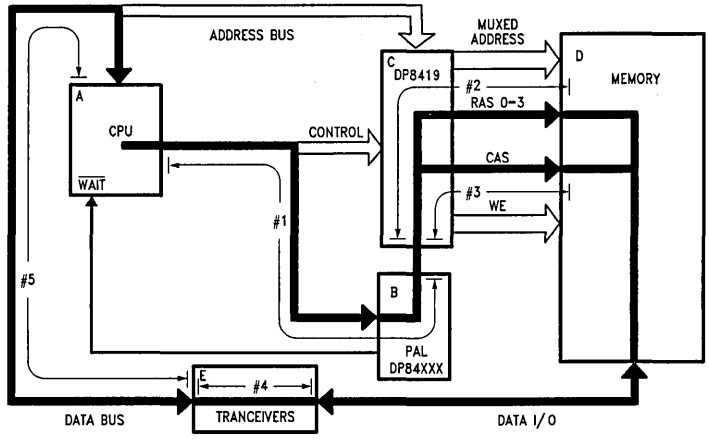
This application note looks at the individual delay elements of a CPU to memory access path for a typical memory system utilizing the DP8419-80 DRAM controller. In the final analysis the reader should be equipped with all the necessary equations to easily calculate the slowest/cheapest allowable DRAMS for no wait state CPU operation when using the DP8419-80 in his/her system.

Equations for calculating the maximum allowable DRAM "tRAC" ($\overline{RAS}$ access time) and "tCAC" ($\overline{CAS}$ access time) specifications for a particular microprocessor to operate at its maximum clock frequency without wait states are provided. Table I and *Figure 3* at the end of this application note give potential DP8419-80 users an illustration of what speed DRAM they may typically need to use in order to achieve no wait state operation with a particular microprocessor. It is important to note that even better performance can be achieved by using the faster DP8419-70.

THE 5 FUNCTIONAL BLOCKS

**Figure 1* illustrates the five functional blocks and the five main delay segments of our DP8419-80 based system example. For this particular example, the following functional block descriptions apply:

Functional Block	Functional Block Description
A)	The CPU issues an access request to the PAL then reads or writes data to or from the DRAMs;
B)	The PAL provides the refresh access arbitration logic which holds off a CPU access during a DRAM refresh and DRAM refresh during a CPU access. The PAL also provides the $\overline{RASIN}$ signal to the DP8419-80;
C)	The DP8419-80 generates the control signal timing required by the DRAMs. It also automatically multiplexes the row and column addresses during access, provides the refresh address during refresh and provides the on board capacitive drive for the direct interface with the DRAM array;
D)	The DRAM provides or stores data in response to the DP8419-80's control signal; and,
E)	The tranceivers isolate the DRAMs from the data bus when they are not being accessed in addition to passing data between the CPU and memory during read and write cycles.



TL/F/8595-1

DP84412: 32008/016/032 - DP8409A/18/19/28/29 Interface PAL
DP84512: NS32332 - DP8417/18/19/28/29 Interface PAL
DP84322/422: 68000/008/010 - DP8409A/18/19/28/29 Interface PALS
DP84522: 68020 - DP8418/19/28/29 Interface PAL
DP84432: 8086/88/186/188 - DP8409A/18/19/28/29 Interface PAL
DP84532: 80286 - DP8418/19/28/29 Interface PALS

FIGURE 1. Delay Elements of the CPU to Memory Data Access Path (DP8409A or DP8417/18/19/28/29 System)

Figure 2 may prove to be a helpful reference. It illustrates a hypothetical system timing pattern for memory accessing for a 4T state microprocessor.

DELAY SEGMENTS

Delay segments #1 through #5 are also shown in *Figure 1*. Delay segment #1 represents the timing delay from when the CPU initiates an access to the point where $\overline{RASIN}$ is issued by the PAL to the DP8419-80;

Delay segment #2 represents the $\overline{RASIN}$ to $\overline{RAS}$ out delay of the DP8419-80 DRAM controller;

Delay segment #3 represents the $\overline{RASIN}$ to $\overline{CAS}$ out delay of the DP8419-80 DRAM controller;

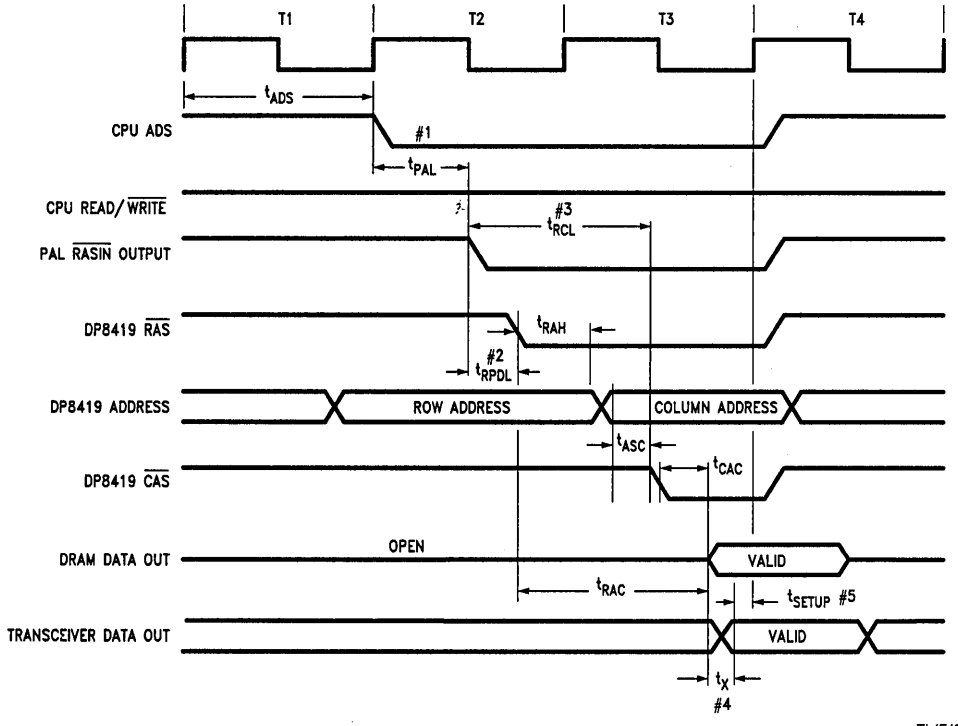
Delay segment #4 represents the inherent delay of the CPU/memory bus transceivers;

Delay segment #5 represents the required CPU data setup time.

The unique equations for determining the values of delay segments #1 through #5 for each of the major microprocessors are provided as the primary content of this application note.

Both "tRAC" and "tCAC" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "tRAC" and "tCAC" parameters calculated. If more information is desired on how "tRAC" and "tCAC" were calculated for a particular microprocessor, the reader should consult the microprocessor data sheet and the PAL data sheet for the particular microprocessor (ie. DP84412 Series 32000 processors, DP84422 68000 family processors. DP84522 68020 family processors, DP84432 iAPX88/86/188/186 processor, DP84532 iAPX286).

Most of the calculations contained in this application note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from $\overline{RAS}$ equaled or exceeded 200 ns. This is because DRAMs can be found with $\overline{RAS}$ access times up to 150 ns that require only 15 ns row address hold times.



TL/F/8595-2

FIGURE 2. System Access Timing (4T State Microprocessor Example)

tRAC/tCAC CALCULATIONS FOR THE MAJOR MICROPROCESSORS

I) Series 32000 "tRAC" and "tCAC" Calculations

Series 32000 8 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = T1 − 2 ns (FCLK − PHI1 skew) + 12 ns ("B" PAL clocked output) = 125 − 2 + 12 = 135 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 25 + 125 + 125 − 135 − 20 − 7 − 20
= 193 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 135 − 77 − 7 − 20
= 136 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 193 ns and a "tCAC" less than or equal to 136 ns. Standard 150 ns DRAMs meet this criteria.

Series 32000 10 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = T1 − 2 ns (FCLK − PHI1 skew) + 12 ns ("B" PAL clocked (output) = 100 − 2 + 12 = 110 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 15 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 100 + 100 + 100 − 110 − 20 − 7 − 15
= 148 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 100 + 100 + 100 − 100 − 77 − 7 − 15
= 91 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 148 ns and a "tCAC" less than or equal to 91 ns. Standard 120 ns DRAMs meet this criteria.

II) 68000 Family "tRAC" and "tCAC" Calculations

68000 Family 8 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 125 + 60 + 15 = 200 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 15 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 125 + 125 + 125 + 55 − 200 − 20 − 7 − 15
= 188 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 125 + 125 + 125 + 55 − 200 − 77 − 7 − 15
= 131 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 188 ns and a "tCAC" less than or equal to 131 ns. Standard 150 ns DRAMs meet this critieria.

68000 Family 9 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 111 + 55 + 15 = 181 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 111 + 111 + 111 + 45 − 181 − 20 − 7 − 10
= 160 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 111 + 111 + 111 + 45 − 181 − 77 − 7 − 10
= 103 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 160 ns and a "tCAC" less than or equal to 103 ns. Standard 150 ns DRAMs meet this criteria.

68000 Family 10 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay = 100 + 55 + 15 = 170 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 100 + 100 + 100 + 45 − 170 − 20 − 7 − 10
= 138 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 100 + 100 + 100 + 45 − 170 − 77 − 7 − 10
= 81 ns

Therefore the DRAM chosen have a "tRAC" less than or equal to 138 ns and a "tCAC" less than or equal to 81 ns. Standard 120 ns DRAMs meet this criteria.

68000 Family 11 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 91 + 55 + 15 = 161 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 91 + 91 + 91 + 35 − 161 − 20 − 7 − 10
= 110 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 91 + 91 + 91 + 35 − 161 − 77 − 7 − 10
= 53 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 110 ns and a "tCAC" less than or equal to 53 ns. Standard 100 ns DRAMs meet this criteria.

68000 Family 12 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 83 + 55 + 15 = 153 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #2 − #4 − #5
= 83.3 + 83.3 + 83.3 + 35 − 153 − 20 − 7 − 10 = 95 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (minimum) − #1 − #3 − #4 − #5
= 83.3 + 83.3 + 83.3 + 35 − 153 − 77 − 7 − 10 = 38 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 95 ns and a "tCAC" less than or equal to 38 ns.

III) 68020 "TRAC" AND "TCAC" Calculations

68020 6 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 167 + 15 = 182 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5
= 167 + 167 + 75 − 182 − 20 − 7 − 10 = 190 ns

"tCAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5
= 167 + 167 + 75 − 182 − 77 − 7 − 10 = 133 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 190 ns and a "tCAC" less than or equal to 133 ns. Standard 150 ns DRAMs meet this criteria.

68020 7 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 143 + 15 = 158 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5
= 143 + 143 + 60 − 158 − 20 − 7 − 10 = 151 ns

"tCAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5
= 143 + 143 + 60 − 158 − 77 − 7 − 10 = 94 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 151 ns and a "tCAC" less than or equal to 94 ns. Standard 150 ns DRAMs meet this criteria.

68020 8 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 125 + 15 = 140 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5
= 125 + 125 + 55 − 140 − 20 − 7 − 10 = 128 ns

"tCAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5

= 125 + 125 + 55 − 140 − 77 − 7 − 10 = 71 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 128 ns and a "tCAC" less than or equal to 71 ns. Standard 120 ns DRAMs meet this criteria.

68020 9 MHz No Wait State Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 111 + 15 = 131 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to CAS low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #2 − #4 − #5

= 111 + 111 + 50 − 131 − 20 − 7 − 10

= 104 ns

"tCAC" = (S0 + S1) + (S2 + S3) + S4 (minimum) − #1 − #3 − #4 − #5

= 111 + 111 + 50 − 131 − 77 − 7 − 10

= 47 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 104 ns and a "tCAC" less than or equal to 47 ns.

IV) 68020 with 1 Wait State Inserted "tRAC" and "tCAC" Calculations

68020 10 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 100 + 15 = 115 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to CAS low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 100 + 100 + 100 + 45 − 115 − 20 − 7 − 10

= 193 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 100 + 100 + 100 + 45 − 115 − 77 − 7 − 10

= 136 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 193 ns and a "tCAC" less than or equal to 136 ns. Standard 150 ns DRAMs meet this criteria.

68020 12 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 80 + 15 = 95 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 83.3 + 83.3 + 83.3 + 35 − 95 − 20 − 7 − 10

= 153 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 83.3 + 83.3 + 83.3 + 35 − 95 − 77 − 7 − 10

= 96 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 153 ns and a "tCAC" less than or equal to 96 ns. Standard 150 ns DRAMs meet this criteria.

68020 14 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 72 + 15 = 87 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 5 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 72 + 72 + 72 + 30 − 87 − 20 − 7 − 5

= 127 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5

= 72 + 72 + 72 + 30 − 87 − 77 − 7 − 5

= 70 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 127 ns and a "tCAC" less than or equal to 70 ns. Standard 120 ns DRAMs meet this criteria.

68020 16 MHz (1 Wait State) Calculations

#1) $\overline{\text{RASIN}}$ low = S0 + S1 + "B" PAL combinational output delay maximum = 62.5 + 15 = 77.5 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419-80 $\overline{\text{RASIN}}$ − $\overline{\text{CAS}}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMS speced in data sheet) = 77 ns

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time = 5 ns minimum

"tRAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #2 − #4 − #5

= 62.5 + 62.5 + 62.5 + 25 − 77.5 − 20 − 7 − 5

= 103 ns

"tCAC" = (S0 + S1) + (S2 + S3) + (SW + SW) + S4 (minimum) − #1 − #3 − #4 − #5
= 62.5 + 62.5 + 62.5 + 25 − 77.5 − 77 − 7 − 5
= 46 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 103 ns and a "tCAC" less than or equal to 46 ns.

V) iAPX 86/88/186/188 Family "tRAC" and "tCAC" Calculations

iAPX 86/88 8 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 82 + 15 = 97 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 97 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 125 + 125 + 125 − 97 − 20 − 7 − 20
= 231 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 97 − 94 − 7 − 20
= 157 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 231 ns and a "tCAC" less than or equal to 157 ns. Standard 200 ns DRAMs meet this criteria.

iPX 186/188 8 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 70 + 15 = 85 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 97 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 125 + 125 + 125 − 85 − 20 − 7 − 20
= 243 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 85 − 94 − 7 − 20
= 169 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 243 ns and a "tCAC" less than or equal to 169 ns. Standard 200 ns DRAMs meet this criteria.

iAPX 86/88 10 MHz No Wait State Calculations

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 61 + 15 = 76 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 5 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 100 + 100 + 100 − 76 − 20 − 7 − 5
= 192 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 100 + 100 + 100 − 76 − 77 − 7 − 5
= 135 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 192 ns and a "tCAC" less than or equal to 135 ns. Standard 150 ns DRAMs meet this criteria.

VI) iAPX 286 "tRAC" and "tCAC" Calculations

6 MHz iAPX 286, 12 MHz Clock, No Wait State Calculations

#1) $\overline{RASIN}$ low = T1 + 74AS04 gate delay + "B" PAL clocked output delay = 83.3 + 4.5 + 12 = 100 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"tRAC" = T1 + T2 + T3 + T4 − #1 − #2 − #4 − #5
= 83.3 + 83.3 + 83.3 + 83.3 − 100 − 20 − 7 − 20 = 186 ns

"tCAC" = T1 + T2 + T3 + T4 − #1 − #3 − #4 − #5
= 83.3 + 83.3 + 83.3 + 83.3 − 100 − 77 − 7 − 20 = 129 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 186 ns and a "tCAC" less than or equal to 129 ns. Standard 150 ns DRAMs meet this criteria.

7 MHz iAPX 286, 14 MHz Clock, No Wait State Calculations

#1) $\overline{RASIN}$ low = T1 + 74AS04 gate delay + "B" PAL clocked output delay = 71.4 + 4.5 + 12 = 88 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 10 ns minimum

"tRAC" = T1 + T2 + T3 + T4 − #1 − #2 − #4 − #5
= 71.4 + 71.4 + 71.4 + 71.4 − 88 − 20 − 7 − 10 = 160 ns

"tCAC" = T1 + T2 + T3 + T4 − #1 − #3 − #4 − #5
= 71.4 + 71.4 + 71.4 + 71.4 − 88 − 77 − 7 − 10 = 103 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 160 ns and a "tCAC" less than or equal to 103 ns. Standard 150 ns DRAMs meet this criteria.

8 MHz IAPX 286, 16 MHz Clock, No Wait State Calculations

#1) $\overline{RASIN}$ low = T1 + 74AS04 gate delay + "B" PAL clocked output delay = 62.5 + 4.5 + 12 = 79 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419-80 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

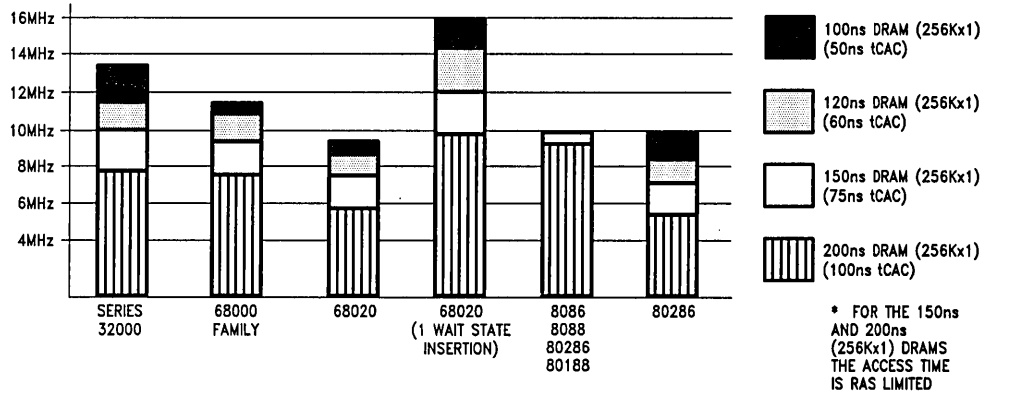
#4) 74F244 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 10 ns minimum

"tRAC" = T1 + T2 + T3 + T4 − #1 − #2 − #4 − #5
= 62.5 + 62.5 + 62.5 + 62.5 − 79 − 20 − 7 − 10 = 134 ns

"tCAC" = T1 + T2 + T3 + T4 − #1 − #3 − #4 − #5
= 62.5 + 62.5 + 62.5 + 62.5 − 79 − 77 − 7 − 10 = 77 ns

Therefore the DRAM chosen should have a "tRAC" less than or equal to 134 ns and a "tCAC" less than or equal to 77 ns. Standard 120 ns DRAMs meet this criteria.



TL/F/8595–3

FIGURE 3

Note 1: The data presented in this figure is based on typical examples. Faster "no wait state" CPU performance is possible with several of the microprocessors shown above via the use of the DP8419-70 instead of the DP8419-80; the elimination of Data Bus Transceivers; a more tailored PAL (Refresh Access Arbitrator) approach; faster support logic; lower than the 15Ω damping resistor specified in the DP8419-80 data sheet; or, less than the specified capacitive load driven directly by the DP8419 (88 DRAMs).

DP8408A/09A/17/18/19/ 28/29 Application Hints

National Semiconductor
Application Brief # 1
Tim Garverick
Webster Meier

The DP8408A, DP8409A dynamic RAM controllers have been well received by dynamic memory users because they perform functions formerly requiring multiple integrated circuit chips. These controllers are designed to be suitable for a variety of DRAM control methods. As a result of the many combinations of ways in which inputs to these chips may be varied, it was inevitable that certain conditions exist that would cause the DP8408A, DP8409A to respond in an undesirable way. Feedback from customers using these chips has resulted in thorough investigations of such conditions. The following are constraints on the use of the DRAM controllers which are not addressed in their data sheets. The majority of customers will find that most of the items on this list are not pertinent to their particular application, and those that are impose minimal restrictions.

1) The on-chip refresh counter resets when the RFI/O pin goes low for a refresh request in mode 5 if this pin is excessively loaded with capacitance. The data sheet suggests that this pin not be loaded with greater than 50 pF. Since RFI/O, in most cases, needs only to drive a low capacitance in a refresh control circuit, this limit is not unreasonable.

2) When the DP8408A, DP8409A is in a refresh mode, the RFI/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 511 (511 is available only on the DP8409A) to accommodate 16k, 64k or 256k DRAMS, respectively. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 (255 for the DP8408A) before rolling over to zero.

3) When going from mode 0, 1 or 2 (refresh) to mode 5 of the DP8408A, if $\overline{\text{CASIN}}$ and R/$\overline{\text{C}}$ are both low, a glitch occurs on the $\overline{\text{CAS}}$ output. Since neither of these inputs is used in these modes, one or both should be held high.

4) Most DRAMs specify 0 ns row address set-up time to $\overline{\text{RAS}}$. In order to guarantee this, the row address to the DP8408A, DP8409A must be valid 10 ns before $\overline{\text{RASIN}}$ transitions low to initiate an access. In terms of the data sheet parameters, maximum ($t_{APD} - t_{RPDL}$) = 10 ns.

5) When changing modes from refresh to access, again sufficient time must be allowed for the row address to be valid before $\overline{\text{RAS}}$ occurs. In this case, the address outputs of the DP8408A, DP8409A are changing from the refresh counter to the row address inputs. In order for the row address to be set up a minimum of 0 ns before $\overline{\text{RAS}}$ goes low, $\overline{\text{RASIN}}$ should not go low until 30 ns after the change from refresh to access mode.

6) Both the low and high pulse widths of $\overline{\text{RAS}}$ have minimum requirements during refresh. When in mode 0, the $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low delay is longer than the $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ high delay. In terms of the data sheet parameters, maximum ($t_{RFPDL} - t_{RFPDH}$) = 25 ns. Thus, the minimum low pulse width of $\overline{\text{RAS}}$ in mode 0 equals the $\overline{\text{RASIN}}$ low pulse width minus 25 ns. The minimum high pulse width of $\overline{\text{RAS}}$ in mode 0 equals the $\overline{\text{RASIN}}$ high pulse width.

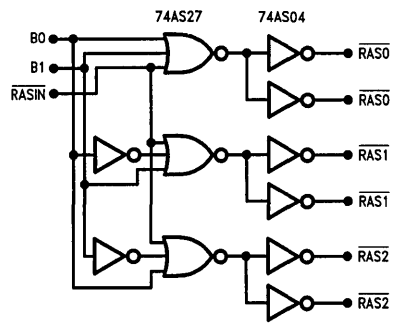
7) The fastest memory access may be accomplished using mode 4 and external delay lines (see App. Brief #9).

8) In the data sheet, it is specified that $\overline{\text{CS}}$ should go low 30 ns (t_{CSLR}) before $\overline{\text{RASIN}}$ goes low to initiate an access in mode 5. This is to prevent the possibility of a glitch on the $\overline{\text{RAS}}$ outputs, resulting from the DP8409A interpreting the $\overline{\text{RASIN}}$ as a hidden refresh. For the same reason, $\overline{\text{CS}}$ should be held low for a minimum of 15 ns after $\overline{\text{RASIN}}$ returns high, ending the access in mode 5.

9) If the DP8409A is being used in mode 5 and $\overline{\text{CS}}$ = 1, and if $\overline{\text{RASIN}}$ goes low within 15 ns before RFCK (R/$\overline{\text{C}}$) goes low, up to a 15 ns glitch may occur on the refresh request pin, RFI/O. However, since $\overline{\text{CS}}$ is high, a hidden refresh will occur as it normally would with RFCK high. If the glitch on RFI/O were detected and interpreted as a forced refresh request, no forced refresh would be allowed by the DP8409A since a hidden refresh was allowed. This would not cause any problem, however, since the hidden refresh has taken care of the refresh requirement for that period of RFCK. Also, this forced refresh request could not be detected if the system does not check RFI/O for a low state while $\overline{\text{RASIN}}$ is low (i.e., an access is taking place).

10) At CPU clock frequencies of 10 MHz and above it is suggested that the hidden refresh capability of the DRAM controller (DP8409/17/19/29) be disabled. The main reason for this suggestion is to satisfy the parameter "t_{RKRL}" (RFCK high to $\overline{\text{RASIN}}$ low for hidden refresh) which is given as a minimum of 50 ns in the DP8417/19/29 data sheets. Disabling hidden refresh also eliminates the need of meeting the parameter of "t_{CSRL1}" ($\overline{\text{CS}}$ low to access $\overline{\text{RASIN}}$ low using Mode 5 with hidden refresh capability) which is given as a minimum of 34 ns in the DP8417/19/29 data sheets. In order to eliminate hidden refresh the "$\overline{\text{CS}}$" pin of the DRAM controller should be permanently grounded on the DRAM controller, and the "$\overline{\text{CS}}$" that previously went to the DRAM controller should be "ORed" with "$\overline{\text{RASIN}}$" (the "OR" gate's output becoming the new "$\overline{\text{RASIN}}$" input to the DRAM controller).

11) If the user desires to improve the DRAM controller "$\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ out" time ("tRPDL") external logic may be used to create multiple "$\overline{\text{RAS}}$s". The circuit shown below requires only several 74XX oxide isolated type IC's (74AS27 and 74AS04) to accomplish this aim.



TL/F/5033–1

DP8408A/9A Fastest DRAM Access Mode

National Semiconductor
Application Brief 9
Tim Garverick
Rusty Meier

If one desires the fastest possible operation of the DP8408A/9A multi-mode dynamic RAM controller/driver in accessing DRAMs, mode 4, externally controlled access mode should be considered.

In using mode 4 there are three input signals which must be considered:

1) $\overline{\text{RASIN}}$—generates $\overline{\text{RAS}}$
2) R/$\overline{\text{C}}$—switches between rows and columns on the address outputs
3) $\overline{\text{CASIN}}$—generates $\overline{\text{CAS}}$

In producing these signals a delay will be needed between $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ and between R/$\overline{\text{C}}$ and $\overline{\text{CASIN}}$. **(Note:** In mode 4 external generation of $\overline{\text{CASIN}}$ can produce $\overline{\text{CAS}}$ faster than automatic generation of $\overline{\text{CAS}}$.)

Two important parameters have been added to the DP8408A/9A data sheets that help one compute the minimum acceptable delays between the above-mentioned signals. These parameters are:

1) t_{DIF1} = MAXIMUM ($t_{RPDL} - t_{RHA}$) = 13 ns
   where t_{RPDL} = $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ delay
   t_{RHA} = row address held from column select
2) t_{DIF2} = MAXIMUM ($t_{RCC} - t_{CPDL}$) = 13 ns
   where t_{RCC} = column select to column address valid
   t_{CPDL} = $\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ delay

These parameters are specified as being less than what would be calculated using the min/max values given for t_{RCC}, t_{CPDL}, t_{RPDL} and t_{RHA} in the DP8408A/9A specification sheets, because on-chip delays track over temperature and supply variations.

The equation for the delay between $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ that guarantees the specified DRAM t_{RAH} is:

$$\text{min delay required} = t_{DIF1} + t_{RAH}$$
$$= 13\text{ ns} + t_{RAH}$$

where t_{RAH} = DRAM minimum row address hold time from $\overline{\text{RAS}}$

The equation for the delay between R/$\overline{\text{C}}$ and $\overline{\text{CASIN}}$ that guarantees the specified DRAM t_{ASC} is:

$$\text{min delay required} = t_{DIF2} + t_{ASC}$$
$$= 13\text{ ns} + t_{ASC}$$

where t_{ASC} = DRAM minimum column address set-up time to $\overline{\text{CAS}}$

To produce the above-mentioned delays between signals, a ±2 ns resolution delay line can be used as follows:

(assuming t_{RAH} = 20 ns, t_{ASC} = 0 ns)

$\overline{\text{RASIN}}$ to R/$\overline{\text{C}}$ delay = 13 ns + 20 ns
= 33 ns

R/$\overline{\text{C}}$ to $\overline{\text{CASIN}}$ delay = 13 ns + 0 ns
= 13 ns

Thus, R/$\overline{\text{C}}$ must follow $\overline{\text{RASIN}}$ by a minimum of 33 ns and $\overline{\text{CASIN}}$ must follow R/$\overline{\text{C}}$ by a minimum of 13 ns. With a delay line of ± 2 ns resolution, the $\overline{\text{RASIN}}$ to R/$\overline{\text{C}}$ and R/$\overline{\text{C}}$ to $\overline{\text{CASIN}}$ delays can be typicals of 35 ns and 15 ns, respectively. (See *Figures 1* and *2*.)

This scheme will provide a maximum $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ delay of:

35 ns + 15 ns + 2 ns (resolution uncertainty)
+ MAXIMUM (t_{CPDL}) = 52 ns + MAXIMUM (t_{CPDL})

For the DP8408/9-2, MAXIMUM (t_{CPDL}) = 58 ns.

For the DP8408A/9A (no dash), MAXIMUM (t_{CPDL}) = 68 ns (not 58 ns as indicated in data sheets up to November 1982).

The fastest mode 4 accesses (with the assumed delay line and DRAM parameters) are therefore, 110 ns and 120 ns, respectively, for the -2 and non-dash parts.

The maximum $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ delay (t_{RICL}) in mode 5 (auto mode) for the DP8408/9-2 (which guarantees a min t_{RAH} of 20 ns) is 130 ns. The maximum t_{RICL} in mode 5 for the DP8408A/9A (no dash) is 160 ns.

Thus, it is shown that if the features offered by the DP8408A/9A automatic modes can be sacrificed, mode 4 (externally controlled access) may be used to obtain the fastest memory access.

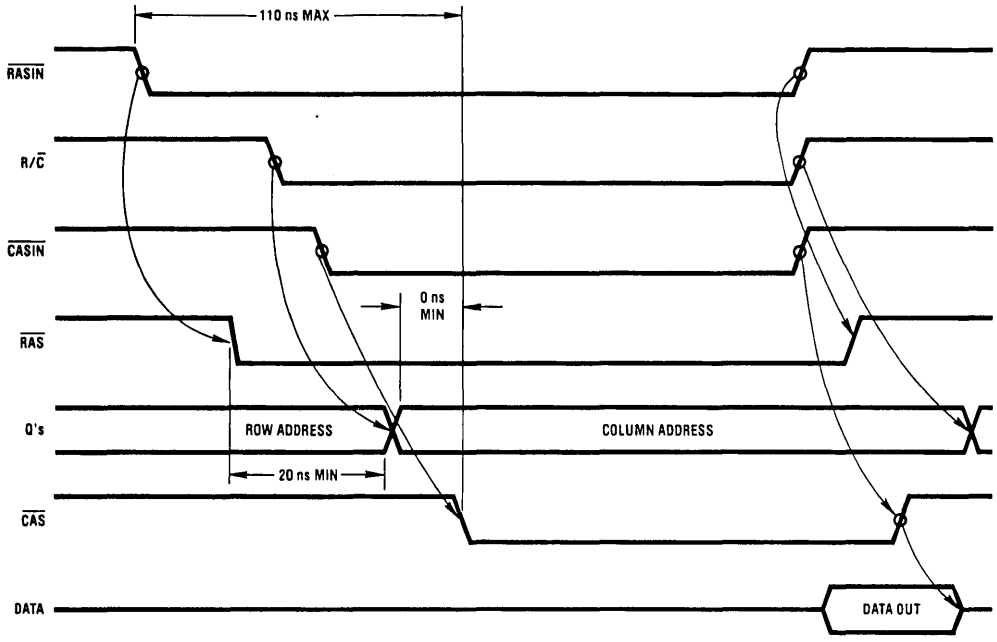


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FIGURE 1. Mode 4 Timing Relationships

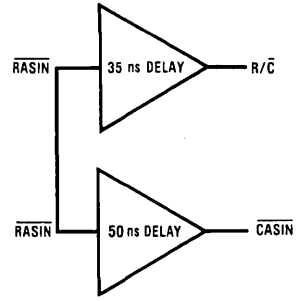

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FIGURE 2. Mode 4 Externally Generated Signals

A family of single-chip dynamic RAM controllers provides the access-timing and refreshing capability for any chip made, or projected.

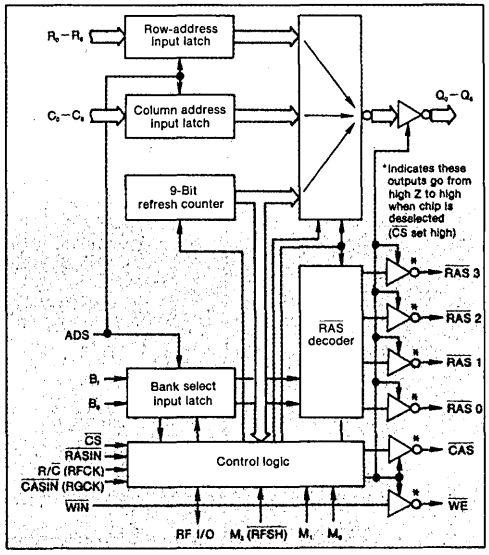
Single-chip controllers cover all RAMs from 16-k to 256-k

While the high performance and low cost of MOS dynamic RAMs make them the most widely used digital semiconductor devices, operating them is more difficult than most other memory chips. Demands are growing for both the automatic sequencing of RAM-access timing and the automatic control of refreshing. National Semiconductor's response is the DP8400 family of memory-interface circuits. The first two members, the DP8408 and the DP8409, are powerful single-chip dynamic-RAM controllers housed in 48-pin dual-in-line packages and, more important, designed to drive the entire range of dynamic RAMs.

The DP8408's eight address outputs drive all current 16-k and 64-k dynamic RAMs. The DP8409, with nine address outputs, not only handles the same RAMs as the 8408, but can control the coming generation of 256-k memory chips. Both devices are pin-compatible, which means a system designed with the DP8408 to control 64-k chips can be directly upgraded to the DP8409 when 256-k RAMs appear on the market. Another benefit for designers is alternate-sourcing—the first DP8400 devices are available from Monolithic Memories (Sunnyvale, CA).

The DP8408, a subset of the DP8409, fits into applications that do not require automatic refreshing. But it does have automatic access modes. The DP8409 is designed for any type of dynamic RAM system, from small microprocessor-based systems to large memory boards. An automatic-accessing mode makes it desirable in mainframes, since it reduces skew time to that of just one chip, while offering tracking of the RAM input controls. This faster accessing permits the use of slower RAMs. With 64-k RAMs, for example, the cost savings between 200-ns and 150-ns devices is significant when large quantities are involved.

Microprocessor users will prefer the DP8409 to other controllers because a single chip performs all the basic automatic access sequencing and automatic refreshing control. (If desired, external refreshing can be used with either controller.) Fast automatic accessing eliminates the need for the wait states that are normally required in faster microprocessors. Automatic refreshing eliminates complicated refresh-arbitration control circuitry while offering a



1. With a 9-bit output bus suitable for interfacing with the largest dynamic RAMs (256 k), National Semiconductor's DP8409 RAM controller drives every RAM available. Features include automatic accessing, automatic refreshing, and high-impedance outputs when not selected. An 8-bit version, the DP8408, operates with RAMs up to 64 kbits, and is used in applications that do not require automatic refreshing.

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Charles Carinalli, Design Manager, Interface Circuits

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hidden refresh feature to increase the system throughput. The DP8409 offers full control, including byte writing, of the 68000, 8086, and Z8000 microprocessors, and National Semiconductor's new 16032 16-bit microprocessor.

Controlling a dynamic RAM is no simple task (see "Dynamic RAM Operation—from $\overline{RAS}$ to $\overline{CAS}$"). Three timing delays are required for an access, and refreshing must be performed continually. With the arrival of powerful 16-bit processors and their large, direct memories, a single-chip controller becomes necessary for efficient system design. Propagation timing delays through the controller must be in the tens of nanoseconds to minimize total access time. Moreover, to eliminate the propagation delays caused by additional memory drivers, a controller should be capable of directly driving a large number of RAMs. The controller must also reduce component cost and conserve PC-board area.

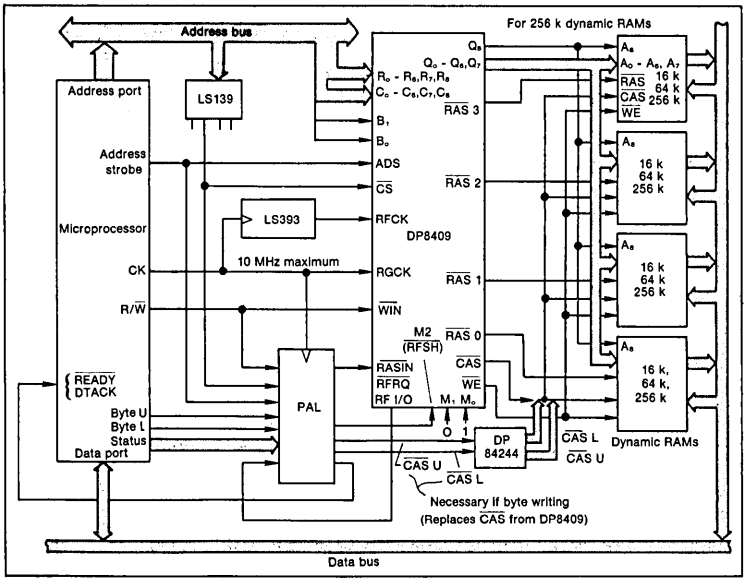
To fulfill these requirements, the DP8408 and 8409 are fabricated in bipolar technology rather than MOS. LSI capability exists in bipolar technology, and bipolar dynamic-RAM controllers are already available. Two such controllers, Intel's 8202 and AMD's 2964 (AMZ8164), represented early attempts to bring timing delays under system control.

In the Intel device, the clock is independent of the access-request signal, causing excessive synchronizing delays before the appearance of the output signals. This leads to long system access times, and for most 16-bit microprocessors requires the insertion of wait states. The AMD controller is an address multiplexer with an on-board refresh counter and bank selection for up to four banks of RAMs. While this device drives a small number of RAMs, AMD offers octal memory drivers that can be placed between the 2964 and the RAMs. Delays become progressively longer as timing signals proceed through the delay timer, the 2964, and the additional drivers. And external components are needed to initiate timing delays. Quite simply, the DP8408 and DP8409 go well beyond the access-time and functional capabilities of the 8202 and 2964.

On board the RAM controllers

A functional block diagram of the DP8409 is shown in Fig. 1. The DP8408 is similar, except for its 8-bit-wide multiplexed address-bus and the fact that its R/C and $\overline{CASIN}$ inputs do not provide dual functions as RFCK and RGCK inputs, as they do in the 8409.

The multiplexed address outputs of both controllers can be selected from the row or column input latches, or from the refresh counter. A high level on input signal ADS enables input row-addresses, R_0



2. The interface of the DP8409 RAM controller to a 16-bit microprocessor looks ahead to the day when 256-kbit dynamic RAMs are available. By designing-in the controller now, no modifications to printed-circuit boards will be necessary when 256-k devices are developed. Simply exchanging controller chips will allow the memory-control capability of a microprocessor to increase by four times.

through R_8, input column-addresses C_0 through C_8, and bank-select inputs B_0 and B_1 into their respective input latches. ADS also latches these signals on its low-going edge. In a normal RAM access, B_0 and B_1 are decoded to determine which bank is selected. By enabling one of the four RAS outputs (when $\overline{\text{RASIN}}$ goes low), the contents of the row-address latch are strobed into the selected RAMs.

Now the control logic causes the row addresses to be replaced with the column addresses, and CAS goes low as determined by the control logic. This causes the contents of the column-address latch to be strobed into the selected RAMs.

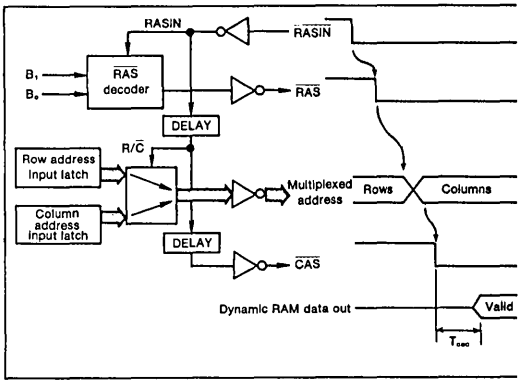
On a write cycle, $\overline{\text{WE}}$ must be low as $\overline{\text{CAS}}$ goes low; on a read cycle, $\overline{\text{WE}}$ must be high. For a read-modify-write cycle, $\overline{\text{WE}}$ must go low some time after $\overline{\text{CAS}}$—this is specified in RAM data sheets. To simplify control, $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally 20 ns later, typically. Three mode pins—M_0, M_1, and M_2 (M_2 is refresh mode)—offer externally selected operating modes. For example, mode 5—automatic access—identified by code 101, can be changed to mode 1—forced refresh—identified by code 100, when M_2 is driven low. These modes include automatic and external control of accesses, and various refreshing modes.

Input pin $\overline{\text{CS}}$ selects or deselects the controller to allow for multiaddressing of memory. For accesses, $\overline{\text{CS}}$ is normally low, but to access a second DP8409 sharing the same memory, $\overline{\text{CS}}$ of the first 8409 must go high. This puts the three-state address outputs in a high-impedance high-state through an external 5-kΩ pull-up resistor, and sets the control signals to a high impedance to prevent them from drifting low; a low level can result in a false access. Switching between chips takes about 30 ns, providing fast multiaddressing. Refreshing must be performed using only one chip. As $\overline{\text{CS}}$ goes high in mode 5, deselection is overridden and, provided RFCK is already high, hidden refreshing can occur.

Input/output pin RF I/O can be used to clear the refresh counter when it has been set low by an external open-collector gate. It also sends out an end-of-count signal—a low level—when the refresh counter has filled (counts are selectable to 127, 255, or 511). This is a useful feature for burst refreshing. In the automatic-refresh mode, RF I/O becomes the signal Refresh Request.

No problems with capacitive loads

One important asset of the DP8408 and 8409 is their ability to drive high-capacitance loads. RAM inputs are generally specified as having a maximum input capacitance of 10 pF/pin, but in large RAM systems, the worst-case input capacitance is usually on the order of 2.5 pF per input. However, one or two devices



3. The DP8408/8409's automatic-accessing capability uses on-chip delay paths to provide faster access while saving on external delay-timing circuitry. On-chip Schottky inverters track extremely well with temperature and voltage, keeping access-times stable.

in a system can go up to 10 pF, especially at high temperature. On the other hand, RAM input currents carry specifications of around 10 μA maximum, but actual input currents seldom exceed 3 μA per input in large systems. Of the two parameters—capacitance and input current—high capacitance always causes more system problems.

In addition to a RAM's input capacitance, designers must consider the capacitance of the PC-board traces. The value of capacitance depends on trace length, nearness to other traces, board thickness, etc. Generally, this amounts to about 3.2 pF per input, giving a total worst-case input capacitance of 5.7 pF/input.

The output stages of the DP8408/8409 can drive up to 88 RAMs, or 500 pF of capacitive loading. Looking at it another way, the controllers can drive four banks each of 16-data bits plus 6 associated check bits for error correction; two banks of 32 data bits with 7 check bits; one bank of 64 data bits with 8 check bits; or any smaller combination. Output rise and fall times are proportional to the capacitive loading, and more than 500 pF increases transition time. Similarly, less than 500 pF decreases propagation delays.

The output-driver stages of the DP8409/8409 are matched. Each stage has symmetrical high and low drive capability, which require that the high and low on-resistances be the same. High output currents are needed to quickly charge or discharge the effective RAM load capacitance on each output. In most applications, a series damping resistor is required between each output and the RAM to minimize undershoot. Undershoot occurs at RAM inputs having both inductive board traces and high capacitive loads on high-to-low transitions.

The value of the series damping resistor depends heavily on the board layout. Address lines usually use a value different from control lines, but both are functions of layout and input loading. The resistor is almost tuned to a specific board since too high a value yields an excessively slow edge, while too low a value does not remove the undershoot. In any case, damping-resistor values vary from 15 to 100 Ω.

Control over all RAMs

The DP8408 and 8409 are designed to control all multiplexed-address dynamic RAMs. The DP8408, with eight multiplexed address outputs and an 8-bit refresh counter, controls 16-k dynamic RAMs (+5 V or three-power-supply types) and both configurations of 64-k RAMs (128 rows by 512 columns or 256 rows by 256 columns). Memory users can specify either of the two 64-k RAM configurations provided the refresh counter on the DP8408 is used. This replaces on-the-RAM refresh counters offered by some RAM manufacturers.

The DP8409's nine address pins and 9-bit refresh counter allow it to control 16-k, 64-k, and 256-k RAMs. Designers can take advantage of the 8409's 256-k capability by building current memory boards using the device. No modifications will be needed when the 256-k RAMs are available. By simply providing for two new input address lines and connecting Q_8 (the ninth multiplexed address output) to A_8 (pin 1) of the RAMs, the memory size can be increased instantly by a factor of four. Figure 2 shows how the connections are made.

Automatic accessing capability is provided by the 8408 and 8409 using on-chip delay paths to generate the correct timing sequence (Fig. 3). These delays are initiated from only one input signal, $\overline{\text{RASIN}}$. This generates all the access-sequencing required by most RAMs. Automatic accessing operates in the following manner: First, $\overline{\text{RASIN}}$ is used to generate the selected $\overline{\text{RAS}}$ output as decoded from bank-select signals B_1 and B_0. $\overline{\text{RASIN}}$ is also fed to the first series of Schottky inverters to produce the necessary delay before rows can be switched to columns. This guarantees exceeding the row-address hold time (t_{RAH}) of most RAMs. For 64-k RAMs, t_{RAH} varies from 20 to 25 ns, so the minimum specification for the 8408 and 8409, 30 ns, is on the safe side. If the address outputs are driving 500-pF loads, switching from row addresses to valid column addresses takes 10 ns. The second series of inverters set $\overline{\text{CAS}}$ low 12 ns (typically) after the columns are valid.

The inverters track with temperature and V_{CC}, as do the output driver stages. Tracking of the output paths holds over the specified temperature and V_{CC} ranges. Since Schottky-logic parameters do not vary significantly with temperature or V_{CC}, the absolute times are not affected by more than 25% over the 0 to 70°C range. At the end of an access-cycle, $\overline{\text{RASIN}}$ goes high and the sequence repeats at a higher speed to terminate the cycle.

An automatic-access mode offers two important advantages: First, there is no need for external timing delay circuitry—this saves cost, memory-board area, and the timing skews that external circuitry introduces. Second, this sequence is much faster than a clocked sequencing approach—that is, the delay from $\overline{\text{RASIN}}$ input to $\overline{\text{CAS}}$ output is much shorter. Benefits include a faster system access time, the possibility of eliminating a wait state in a microprocessor memory-access cycle, or the ability to choose slower RAMs (a lower-cost solution) without affecting access time. And since both chips need no external memory drivers, the timing skews are confined to just one chip.

If automatic timing is not desired, another mode allows all timing to be under the control of the relevant external control signals. $\overline{\text{RASIN}}$ initiates the selected $\overline{\text{RAS}}$ output, R/$\overline{\text{C}}$ selects either the row or column address, and $\overline{\text{CASIN}}$ controls $\overline{\text{CAS}}$.

Refreshing comes in many forms

The DP8408 performs refresh operations only under external control. The microprocessor system decides when a refresh is needed by setting M_2 ($\overline{\text{REFRESH}}$) low to place the refresh counter contents on the address outputs. Then the system sets $\overline{\text{RASIN}}$ low to allow all four RAS outputs to low-stroke the refresh address into the rows of all four banks of RAMs. $\overline{\text{CAS}}$ is inhibited, preventing a false write, and the RAM data outputs remain in a high-impedance state.

A refresh cycle ends when $\overline{\text{RASIN}}$ goes high and the refresh counter increments, ready for the next refresh cycle. Most RAMs require that all 128 rows be refreshed in 2 ms, or 256 rows in 4 ms. This can be accomplished by either guaranteeing a refresh on one row every 16 μs, or performing a burst refresh of 128 rows at the start of each 2-ms period, until RF I/O indicates end-of-count. Most system designers prefer one refresh every 16 μs. But this can involve inhibiting normal memory accessing, and requires refresh arbitration.

The end-of-count indication on RF I/O can be set under external system control to either 127 or 255 for burst-refresh applications. Actually, the internal address counter still counts to its maximum value, independent of the end-of-count value—the RF I/O value is a result of counter decode and does not reset the counter. This simplifies the RAM interface since the higher-order address bit-count is ignored by RAMs with 128 rows.

In addition to providing the external-control

refresh mode of the 8408, the 8409 performs hidden refreshing in one of the automatic-access modes. To attain maximum throughput, it is obviously advantageous to perform refreshes without interrupting the system. The DP8409 can do this by monitoring the $\overline{CS}$ input to see if it is high. If $\overline{CS}$ is high, the RAMs are not being accessed. If $\overline{CS}$ is high for one cycle, the 8409 performs a hidden refresh during this cycle, and stops in time for the system to start another access. But if a hidden refresh does not occur in a specific 16-μs time slot, a refresh must be forced, possibly by stopping the system.

To perform auto-refreshing, the DP8409 must receive two clock signals: the 16-μs refresh-period clock, RFCK, and RGCK, the RAS-generator clock; RGCK can be the microprocessor clock. To keep the number of pins at 48, RFCK and RGCK share pins with other signals. In the automatic-access mode (mode 5), neither R/$\overline{C}$ nor $\overline{CASIN}$ are used, so these duplicate as RFCK and RGCK in modes 1 and 5. To stop the

Dynamic RAM operation—from $\overline{RAS}$ to $\overline{CAS}$

The operation of a dynamic RAM (see figure) is, in a word, complex: Not only do its multiplexed address inputs require delayed timing signals, but it must be refreshed continually.

During an access to a RAM, the first step requires that a row address be presented to the multiplexed address inputs. As the row-address signal ($\overline{RAS}$) goes low, the address is latched into the row latch, and decoded to the memory array. There, the outputs from the selected row are presented to the sense amplifiers. Row addresses must be held on the address inputs for a predetermined time—t_{RAIL}, or row-address hold-time—after $\overline{RAS}$ switches low.

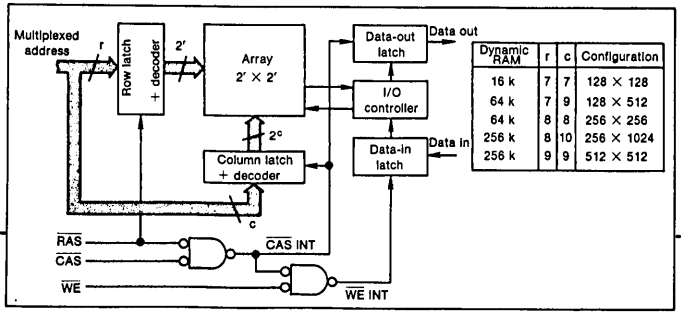
At this time, the row address can be replaced by a column-address. When a column address is valid, the column-address strobe ($\overline{CAS}$) goes low to latch the address into the column latch. Column-addresses are decoded to allow a selected sense amplifier to send data to the output data-latch (during a read cycle). In a write cycle, with the Write Enable signal ($\overline{WE}$) already low, a low-going $\overline{CAS}$ signal causes the selected cell to be set to the value at the data input.

The RAM block diagram shows the chip's operation, including the internal gating of the control signals. One key feature is that $\overline{RAS}$ internally controls $\overline{CAS}$. Thus, if $\overline{RAS}$ is already low when $\overline{CAS}$ goes low, a normal read or write cycle follows, and the chip consumes its full operating current. On the other hand, if $\overline{CAS}$ goes low while $\overline{RAS}$ is high, $\overline{CAS}$ $\overline{INT}$ is inhibited along with $\overline{RAS}$, and the RAM consumes only the current required for standby. In this case, the chip is deactivated. Similarly, $\overline{WE}$ $\overline{INT}$ is controlled by both $\overline{RAS}$ and $\overline{CAS}$.

This simplifies bank selection by using different $\overline{RAS}$ outputs to select the banks. $\overline{CAS}$ and $\overline{WE}$ can be common to all the RAM-banks, along with the multiplexed addressing. For example, in a four-bank system, only one $\overline{RAS}$ goes low in any access-cycle. This activates all the RAMs in a selected bank, but does not activate RAMs in the other three banks. These latter RAMs remain in the standby mode. The common data bus accesses only the selected bank, whether reading or writing.

Besides a complex sequencing arrangement, dynamic RAMs must be refreshed to prevent the capacitor in each cell from losing its charge, which represents information. If any row is not accessed for too long a period of time—the refresh period—capacitors will discharge, causing the voltage to drop below the sense-amplifier threshold. Then, when the row is finally accessed, its outputs will appear as all zeros or all ones, depending on which side of the sense amplifier is accessed.

Most RAMs have 2-ms minimum refresh times, but 64-k dynamic RAMs are typically much higher. When accessing a row for refresh, $\overline{RAS}$ is needed for a strobe, but $\overline{CAS}$ is not necessary. The simplest approach to refreshing is to access a refresh counter that increments at the end of each refresh $\overline{RAS}$. For some RAMs, 128 rows must be refreshed in 2 ms, while others require refreshing 256 rows in 4 ms. With distributed refreshing, one row must be refreshed every 16 μs for proper operation.



Dynamic RAM	r	c	Configuration
16 k	7	7	128 × 128
64 k	7	9	128 × 512
64 k	8	8	256 × 256
256 k	8	10	256 × 1024
256 k	9	9	512 × 512

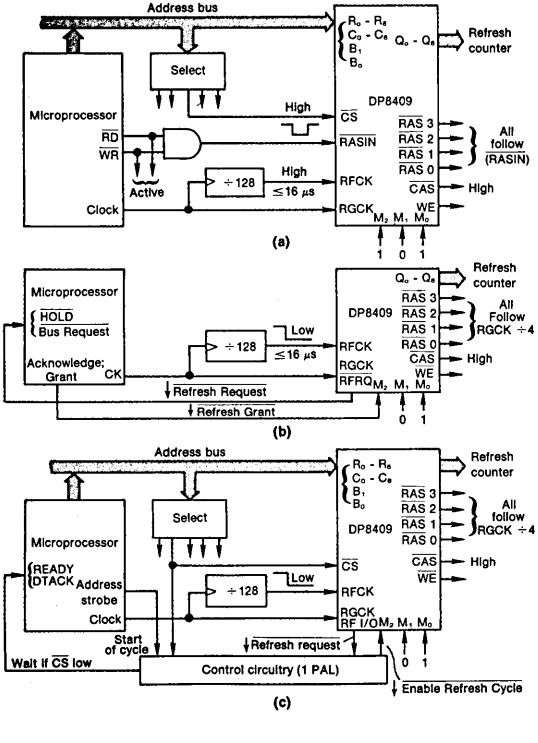
system, the DP8409 gives preference to hidden refreshing using RFCK as a level reference. The 16-μs cycle commences as RFCK goes high; if CS goes high while RFCK is high, the refresh counter is enabled on the address outputs, overriding the internal three-state signals (Fig. 4a). All four RAS outputs follow $\overline{\text{RASIN}}$, so to perform a refresh, $\overline{\text{RASIN}}$ must be set low. In smaller systems, $\overline{\text{RASIN}}$ is set low every time a microprocessor performs a read or write cycle. Each time the processor accesses something other than RAM—a peripheral or ROM or another memory segment—a hidden refresh is performed.

The DP8409 detects that $\overline{\text{CS}}$ is high when the processor accesses another section of the system and places the present state of the refresh counter outputs on the multiplexed address bus to memory. When the Read or Write output of the microprocessor is activated, $\overline{\text{RASIN}}$ follows. This causes all four RAS outputs to low-strobe the refresh address into the RAMs. When the cycle ends, $\overline{\text{RASIN}}$ ends, forcing the four $\overline{\text{RAS}}$ outputs back to their inactive states. This ends the hidden refresh.

At this time, the refresh counter increments, and another microprocessor cycle can begin immediately. This cycle can be a memory access; therefore, the previous refresh cycle has been completely hidden from the microprocessor. The DP8409 allows only one such hidden refresh cycle to occur within a clock cycle of RFCK to minimize power dissipation.

If a hidden refresh does not occur, the DP8409 must force a refresh before RFCK begins a new cycle on a low-to-high transition. Therefore, as RFCK goes low (and a hidden refresh has not occurred), RF I/O (Refresh Request) goes low requesting that a refresh be performed. When the system acknowledges the request, it sets M_2 (refresh) low, and prevents further accesses to the DP8409. The 8409 then sends out the refresh-counter contents and interrogates RGCK—in most applications, RGCK is 100 to 150 ns. The 8409 waits one full cycle of RGCK before setting all four RAS outputs low. This guarantees that the minimum RAS precharge time of the RAMs is exceeded. Then RF I/O goes high, allowing the system to recognize that holding is about to end. Most microprocessors allow enough time so that as refresh finishes, they are almost ready to begin again. The $\overline{\text{RAS}}$ outputs remain low for the next two clock periods to exceed the minimum t_{RAS} time for refreshing—200 ns is about the right time. When all $\overline{\text{RAS}}$ outputs go high, the refresh counter increments.

A minimum component-count solution to forced refreshing is to connect RF I/O to the Hold or Bus-Request input of a microprocessor, and the Hold Acknowledge or Bus Grant output to M_2 (Fig. 4b). For some microprocessors, it may be preferable to continue operation without going into hold, and with additional circuitry, the approach can be easily implemented as shown in Fig. 4c. Using this technique of forced refreshing, the control circuit monitors the refresh-request output. When this output switches low, the control circuit waits for a new microprocessor cycle to begin. If the next cycle is for the segment of memory controlled by the DP8409, $\overline{\text{CS}}$ and the control circuitry will be set low. The control circuitry issues a Wait signal to the microprocessor, which is removed when refreshing has ended. If $\overline{\text{CS}}$ is set high, the refresh cycle begins and ends without affecting other system cycles. In effect, this is still a hidden refresh.□



4. Automatic refreshing can be performed in three different ways with the DP8409 controller. A hidden refresh (a) occurs while the microprocessor is reading or writing elsewhere in the system. Although undesirable, forced refreshing (b) can be performed by stopping the microprocessor. A better technique for forced refreshing (c) is to insert wait states into the processor timing cycle.

Dynamic RAM controller pushes system speed to 10 MHz—and beyond

A highly integrated controller chip makes an ideal replacement for discrete equivalents, sacrificing neither system speed nor dynamic RAM access time.

Few system designers would deny that the integration level of today's controller chips greatly simplifies their jobs. Take dynamic RAM controllers, which now incorporate refresh counters, output buffers, and row and column multiplexing circuitry. Today's high-performance microprocessor-based systems, however, exceed the 8-MHz maximum operating rate of present controllers. So a new controller chip surmounts that, running at 10 MHz or more without imposing wait states. Cost-conscious system designers can take advantage of the improved RAM controller by using slower, cheaper dynamic RAMs in their systems without sacrificing performance.

A second-generation dynamic RAM controller, the DP8419 can directly replace its predecessor, the DP8409, in most systems. Its higher speed is due to unusual delay line circuitry and to the bipolar oxide isolation process called advanced low-power Schottky. Moreover, its on-chip circuitry multiplexes addresses, generates control signal timing, and directly accesses up to 2 Mbytes of RAM. An extremely versatile chip, it interfaces with most popular microprocessors, and the addition of an error detection and correction chip (the DP8400-2) enhances the RAM system's data integrity.

Like the earlier chip, the controller has all the dynamic RAM functions necessary to minimize skewing on its outputs. Built-in drivers are specified at 500 pF when driving 88 dynamic RAMs, and all ac and dc characteristics are guaranteed over the full range of operating temperature and supply voltage.

The chip's nine address drivers enable it to directly drive 16-kbit, 64-kbit, and the newer 256-kbit dynamic RAMs (Fig. 1). Its address, Row and Column Address Strobe, and Write Enable lines all are specified for driving the equivalent capacitance of 88 dynamic RAMs, including pc board traces. With 256-kbit memories, that translates into 2 Mbytes of addressable data, plus the check bits for error correction.

Row and column address latches prove valuable for microprocessor systems that multiplex their address and data lines. They may operate in a fall-through mode when the address information remains valid throughout the memory access cycle. The chip's refresh counter, which

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Timothy Garverick is a senior design engineer for National Semiconductor's LSI Interface Circuit Development group. He designed the dynamic RAM controller, as well as the industry's fastest TTL-to-ECL voltage-level translator. He holds a BSEE from MIT.

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Dynamic RAM controller chip

keeps track of the next row to be refreshed, is multiplexed with the row and column address latches, feeding input to the address drivers.

The internal delay line generates the critical access timing signals required by dynamic RAMs. By adjusting one pin, it is possible to optimize timing for the speed of the memory.

Functionally, the controller chip is a subset of the DP8409, giving up half the latter's operating modes in favor of greater speed. Nevertheless, the four remaining modes are the most common, allowing the chip to replace the earlier one in most applications. Only two pins now select the controller's operating modes; the extra pin sets the system for fast or slow RAMs. Otherwise, the pinouts of the two chips are compatible.

The controller has two memory access modes, automatic or external. In the first case, its own delay line generates all control timing. In the latter, an external delay line is required, but allows the Column Address Strobe signal ($\overline{CAS}$) to be toggled without affecting the Row Address Strobe ($\overline{RAS}$). The external mode is important for high-speed nibble and page accessing schemes, in which multiple columns can be accessed within the enabled row without generating $\overline{RAS}$ signals between accesses.

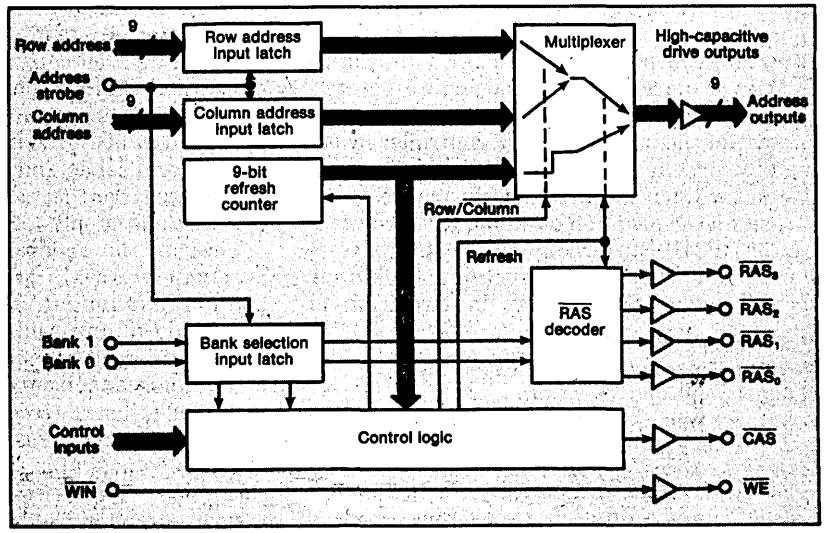
The controller also has two refresh modes. When it is in the external mode, the user determines when refreshing is necessary and sets up burst refreshes as desired. In the automatic mode, the chip requests refreshing and also performs "hidden" refreshing—that is, refreshing that is transparent to the microprocessor.

Minimizing delay variations

The time it takes to get data from dynamic RAM depends not only on the memory's access time but also on the control function. Often that function accounts for more of the total memory access time than the memory itself.

In the case of the DP8419 controller, its $\overline{RAS}$IN input initiates a memory access; the chip responds with its $\overline{RAS}$, $\overline{CAS}$, and row and column addresses. $\overline{RAS}$ latches the row address, $\overline{CAS}$ the column one. During a read access, data from RAM is valid some time after $\overline{CAS}$.

The timing has several components (Fig. 2): t_{RAH}, representing the time that the row address must remain valid on the memory address inputs after $\overline{RAS}$ has been issued; t_{ASC}, the time that the column address must be set up (valid)



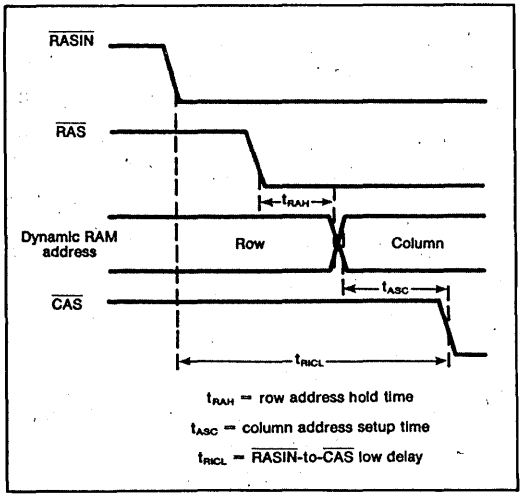
1. Row and column address latches are built into the DP8419 dynamic RAM controller, to meet the needs of microprocessor-based systems that multiplex their data and address lines. The refresh counter keeps track of the next row being refreshed, and a novel addition to any RAM controller, an internal delay line (not shown here), generates the critical access timing on chip.

on the inputs before $\overline{CAS}$ occurs; and t_{RICL}, the total delay between when the controller receives RASIN and the time it issues $\overline{CAS}$.

A dynamic RAM controller's worst-case t_{RICL} depends on how well the delay elements—typically a string of inverters or a resistor and a capacitor—control t_{RAH} and t_{ASC}. The delay varies according to voltage supply, temperature, and process variations. But in the DP8419, the novel delay circuit nearly eliminates voltage supply and temperature dependencies and significantly reduces process variation effects. The result is an extremely tight $\overline{RAS}$-to-$\overline{CAS}$ delay specification. Tests indicate a typical variation of only ±3 ns over a ±10% supply voltage range and operating temperature range of 0° to 70°C.

Besides the delay line, the chip features fast propagation times in all of its critical delay paths, thanks largely to the ALS fabrication process. Compared with conventional junction-isolated processes, this oxide-isolated process produces much lower parasitic capacitances. Gates, therefore, inherently switch much faster.

With its built-in delay line and address and control drivers, the chip reaches a performance level previously attained only with discrete solutions. Moreover, the access-refresh arbiter has purposely not been incorporated in the chip, making it a prime candidate for optimization by the system designer for any microprocessor.



2. In building a system around dynamic RAMs, designers must focus on the times that the row and column addresses must remain valid, t_{RAH} and t_{ASC}, respectively. The total delay of the memory controller chip can be defined as t_{RICL}, the delay from RASIN to CAS.

The chip's advantages over a discrete design are dramatically demonstrated when calculating the worst-case t_{RICL} for a discrete system that controls 72 dynamic RAMs. Typically, taps on the discrete controller's delay lines control and adjust the delay in 10-ns increments. But choosing the optimum delay tap with confidence is a difficult task, and designers should prepare themselves by developing a table of the worst-case conditions for several critical delay paths and then checking to make sure that the RAMs' minimum t_{RAN} and t_{ASC} specifications are met.

Discrete versus chip

For the discrete system, the third tap on the delay line should guarantee an acceptable t_{ASC}, while the fifth tap usually satisfies the minimum t_{RAH} requirement. Using exactly those taps on a ±3-ns delay line with octal high-capacitive drives, the maximum t_{RICL} comes out as 53 ns for the delay line plus 35 ns for the drives, for a total of 88 ns.

The controller chip meets exactly the same timing requirements, but with a maximum t_{RICL} of only 77 ns. In addition, it dissipates less than a quarter the power of the equivalent discrete controller (1.1 W maximum vs 4.7 W maximum).

The system benefits of the controller chip stretch beyond the delay timing. In one application, the chip, operating in its automatic memory and refresh modes, teams up with a PAL device (Fig. 3). Transceivers are part of the system, isolating the data pins of the dynamic RAM from the CPU data bus. Divider circuitry supplies the controller with one refresh clock signal (RFSH CLK) per period, enough to refresh the RAM properly.

The logic array primarily arbitrates between the refresh and access cycles. It initiates read or write access cycles by monitoring the Address Strobe signal ($\overline{ADS}$) and the R/$\overline{W}$ input from the CPU (Fig. 4). When it determines that an access is beginning, it produces $\overline{RASIN}$, initiating the RAM access. In a write cycle, the logic device generates that signal later than it does in a read cycle, guaranteeing that data is valid before $\overline{CAS}$ goes low.

Through the $\overline{Wait}$ input to the CPU, wait

Dynamic RAM controller chip

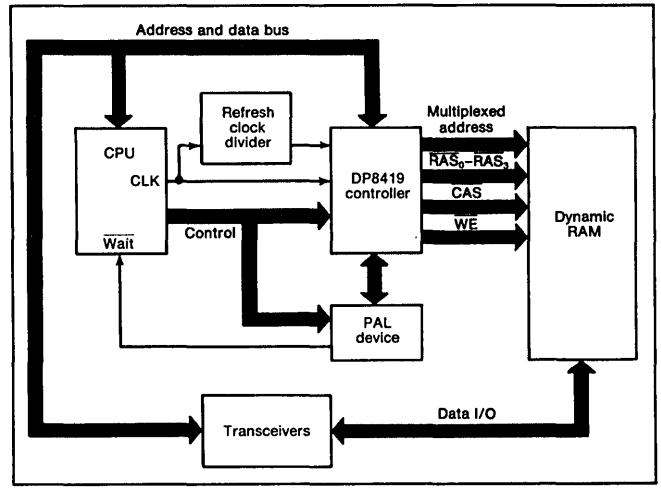
states can be inserted into the access cycles, allowing the CPU to access the memory over more than the minimum number of system clock periods (T states) per cycle. For example, if the CPU samples its $\overline{\text{Wait}}$ input during T_2 and $\overline{\text{Wait}}$ is low, then extra clock periods are added to the access cycle until the sampled signal goes high.

The controller produces the Refresh Request signal ($\overline{\text{RFRQ}}$) when the divider's RFSH CLK signal goes low and no hidden refreshing has taken place while RFSH CLK was high (Fig. 5). The logic device responds to $\overline{\text{RFRQ}}$ by immediately forcing the controller into its automatic refresh mode, unless, of course, the RAM is being accessed at the time. In that case, the PAL waits for the access to end before putting the controller into its refresh mode. Similarly, when the CPU requests a memory read cycle during a forced refresh cycle, the logic array senses the access request. In response, it inserts wait states until the refresh has ended and the RAM's $\overline{\text{RAS}}$ precharge specification has been met.

The performance of the system depends not only on the logic array and the controller chip but also on the speed of the dynamic RAMs. The memories' access time from $\overline{\text{CAS}}$ (t_{CAC}) and access time from $\overline{\text{RAS}}$ (t_{RAC}) indicate how quickly the memory can be accessed. Unfortunately, dynamic RAMs are commonly classified only by t_{RAC}, even though t_{CAC} is often the more critical parameter. To further complicate matters, both types of access times vary from supplier to supplier. For instance, a memory with a t_{RAC} of 150 ns may have a t_{CAC} ranging from 75 to 100 ns.

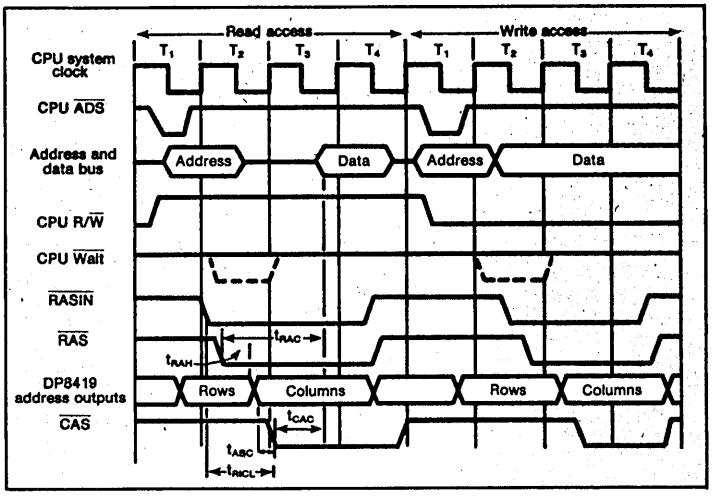
The controller chip determines which of these two items is relevant in determining the actual access time in a system. If the controller's $\overline{\text{RAS}}$-to-$\overline{\text{CAS}}$ delay renders t_{RAC} greater than the $\overline{\text{RAS}}$-to-$\overline{\text{CAS}}$ delay plus t_{CAC}, then t_{RAC} determines access time. Otherwise, t_{CAC} is used. For 150-ns dynamic RAMs with a t_{CAC} of 100 ns, the $\overline{\text{RAS}}$-to-$\overline{\text{CAS}}$ delay must be less than 50 ns in order for t_{RAC} to be relevant.

The table on page 212 shows the maximum t_{CAC} allowable for the dynamic RAM if it is to work with the controller chip without inflicting wait states on various microprocessors. It can be seen that the DP8419 does not require a fast,

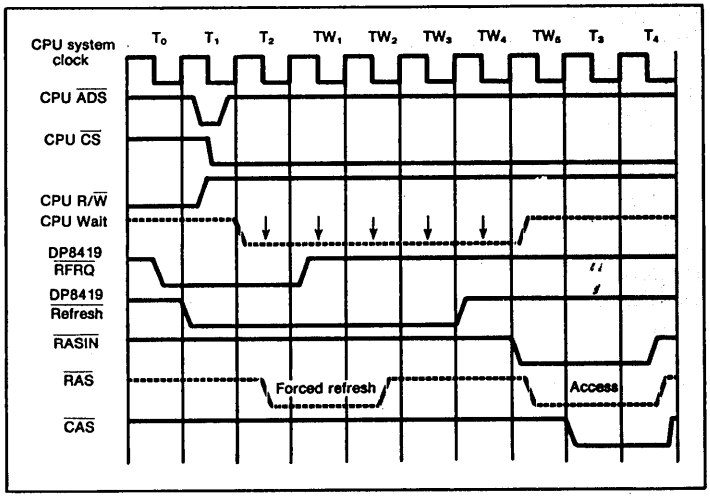


3. In a typical system based on the controller chip, transceivers isolate the dynamic RAM data pins from the CPU data bus. The chief job of the PAL device is to strike a balance between memory refresh and access cycles, and a special divider circuit supplies the controller with one refresh signal per clock period—enough to keep the memory refreshed.

expensive dynamic RAM in order to achieve high system performance. Most popular microprocessors require at least four system clock periods to access a dynamic RAM. The 68020, however, takes only three periods. To reconcile its t_{CAC} needs with those of other processors, its



4. The interface between the CPU and the DP8419 controller chip, as shown in Fig. 3, underscores the importance of access timing. Most dynamic RAMs are characterized by t_{RAC}, their access time from RAS, but in reality t_{CAC}, the access time from CAS, is often more critical. The memory controller in fact determines which of those parameters will govern the actual access time in a system.



5. If the CPU in Fig. 3 requests a memory read cycle during a forced refresh cycle, the PAL senses the access request. It then adds wait states (TW_X) to the CPU access cycle (upper dotted line) until the forced refresh has ended and the RAM's RAS precharge specification has been met (lower dotted line).

Dynamic RAM controller chip

Maximum dynamic RAM t_{CAC} allowable for no wait states with the DP8419

Microprocessor	t_{CAC} (ns)			
	8 MHz	10 MHz	12 MHz	16 MHz
Series 32000	126	86	N.a.	N.a
68000, 68010, or 68008	121	81	38	N.a.
68020	N.a.	121	88	41
8086/8088	164	108	N.a.	N.a.
80186/80188	176	N.a.	N.a.	N.a.
80286*	234	N.a.	119	77

N.a. = not applicable
* Operating frequency refers to CLK of 82284 clock generator.

t_{CAC} calculation is based instead on four clock periods, with one wait state inserted.

Overall, the information in the table is valid for arrays of 72 dynamic RAMs. The maximum allowable t_{CAC} of the dynamic RAM will be greater by about 1 ns for every five fewer RAMs.

Complementing the dynamic RAM controller is the DP8400-2 error checking and correction chip, which exploits several novel circuit techniques—along with the ALS process—to achieve a 20% to 40% improvement in both power consumption and speed over the earlier DP8400-4. It needs a maximum supply current of 300 mA, and it takes a maximum of 40 ns from valid data input to valid check bit output, 31 ns to valid error, and 61 ns to corrected data.

As a member of the DP8400 series of ECC chips, the DP8400-2 boosts the reliability of a dynamic RAM system by using a modified Hamming code that allows all single-bit errors to be detected and corrected and all double-bit errors to be detected. Then it goes the rest one better, using a double-complement method that allows all double-bit errors also to be corrected, so long as one of the errors is a hard error.

-Also unique to the error-correcting device is its on-chip circuitry for byte parity, which detects all single-bit errors. This feature may be useful in systems where the CPU card and the memory card are separate and the user requires data integrity between the two. □

Section 2

Error Checking and Correction

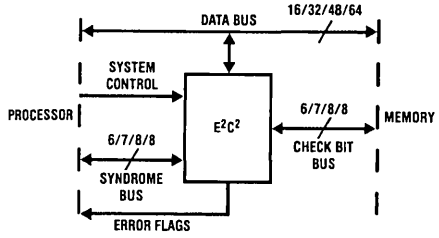
Section Contents

National Semiconductor Corporation

DP8400-2—E²C² Expandable Error Checker/Corrector

General Description

The DP8400-2 Expandable Error Checker and Corrector (E^2C^2) aids system reliability and integrity by detecting errors in memory data and correcting single or double-bit errors. The E^2C^2 data I/O port sits across the processor-memory data bus as shown, and the check bit I/O port connects to the memory check bits. Error flags are provided, and a syndrome I/O port is available. Fabricated using high speed Schottky technology in a 48-pin dual-in-line package, the DP8400-2 has been designed such that its internal delay times are minimal, maintaining maximum memory performance.



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For a 16-bit word, the DP8400-2 monitors data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400-2 uses an encoding matrix to generate 6 check bits from the 16 bits of data. In a WRITE cycle, the data word and the corresponding check bits are written into memory. When the same location of memory is subsequently read, the E^2C^2 generates 6 new check bits from the memory data and compares them with the 6 check bits read from memory to create 6 syndrome bits. If there is a difference (causing some syndrome bits to go high), then that memory location contains an error and the DP8400-2 indicates the type of error with 3 error flags. If the error is a single data-bit error, the DP8400-2 will automatically correct it.

The DP8400-2 is easily expandable to other data configurations. For a 32-bit data bus with 7 check bits, two DP8400-2s can be used in cascade with no other ICs. Three DP8400-2s can be used for 48 bits, and four DP8400-2s for 64 data bits, both with 8 check bits. In all these configurations, single and double-error detection and single-error correction are easy to implement.

When the memory is more unreliable, or better system integrity is preferred, then in any of these configurations, double-error correction can be performed. One approach requires a further memory WRITE-READ cycle using complemented data and check bits from the DP8400-2. If at least one of the two errors is a hard error, the DP8400-2 will correct both errors. This implementation requires no more memory check bits or DP8400-2s than the single-error correct configurations.

The DP8400-2 has a separate syndrome I/O bus which can be used for error logging or error management. In addition, the DP8400-2 can be used in BYTE-WRITE applications (for up to 72 data bits) because it has separate byte controls for the data buffers. In 16 or 32-bit systems, the DP8400-2 will generate and check system byte parity, if required, for integrity of the data supplied from or to the processor. There are three latch controls to enable latching of data in various modes and configurations.

Operational Features

- Fast single and double-error detection
- Fast single-error correction
- Double-error correction after catastrophic failure with no additional ICs or check bits
- Functionally expandable to 100% double-error correct capability
- Functionally expandable to triple-error detect
- Directly expandable to 32 bits using 2 DP8400-2s only
- Directly expandable to 48 bits using 3 DP8400-2s only
- Directly expandable to 64 bits using 4 DP8400-2s only
- Expandable to and beyond 64 bits in fast configuration with extra ICs
- 3 error flags for complete error recording
- 3 latch enable inputs for versatile control
- Byte parity generating and checking
- Separate byte controls for outputting data in BYTE-WRITE operation
- Separate syndrome I/O port accessible for error logging and management
- On-chip input and output latches for data bus, check bit bus and syndrome bus
- Diagnostic capability for simulating check bits
- Memory check bit bus, syndrome bus, error flags and internally generated syndromes available on the data bus
- Self-test of E^2C^2 on the memory card under processor control
- Full diagnostic check of memory with the E^2C^2
- Complete memory failure detectable
- Power-on clears data and syndrome input latches

Timing Features

16-BIT CONFIGURATION

WRITE Time: 29 ns from data-in to check bits valid

DETECT Time: 21 ns from data-in to Any Error (AE) flag set

CORRECT Time: 44 ns from data-in to correct data out

Timing Features (Continued)

32-BIT CONFIGURATION

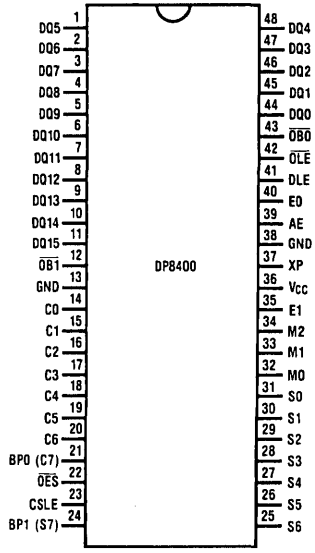
WRITE Time: 49 ns from data-in to check bits valid

DETECT Time: 46 ns from data-in to Any Error (AE) flag set

CORRECT Time: 84 ns from data-in to correct data out

DP8400-2 Connection Diagram

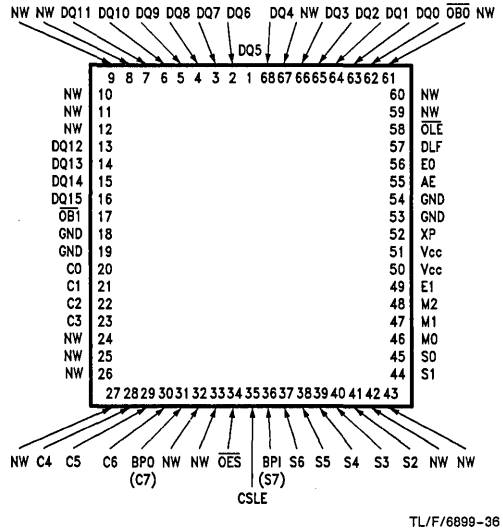
Dual-In-Line Package



Top View TL/F/6899–2

Order Number DP8400V-2, DP8400N-2, or DP8400D-2
See NS Package V68, N48A or D48A

Chip Carrier Package



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Top View

Pin Descriptions

Pin #	Description
1	DQ5
2	DQ6
3	DQ7
4	DQ8
5	DQ9
6	DQ10
7	DQ11
13	DQ12
14	DQ13
15	DQ14
16	DQ15
17	$\overline{OB1}$
18	GND
19	GND
20	C0
21	C1
22	C2
23	C3
28	C4
29	C5
30	C6
31	BP0 (C7)
34	$\overline{OES}$
35	CSLE
36	BP1 (S7)
37	S6
38	S5
39	S4
40	S3
41	S2
44	S1
45	S0
46	M0
47	M1
48	M2
49	E1
50	V_{CC}
51	V_{CC}
52	XP
53	GND
54	GND
55	AE
56	E0
57	DLF
58	$\overline{OLE}$
62	$\overline{OB0}$
63	DQ0
64	DQ1
65	DQ2
66	DQ3
68	DQ4

Note: Pins 8, 9, 10, 11, 12, 24, 25, 26, 27, 32, 33, 42, 43, 59, 60, 61, and 67 are all **NW**.

Pin Definitions See *Figure 1* for abbreviations

V_{CC}, GND, GND: 5.0V ±5%. The 3 supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. Also there are two ground pins to reduce the low-level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 16 data bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

DQ0–DQ15: Data I/O port. 16-bit bidirectional data bus which is connected to the input of DIL0 and DIL1 and the output of DOB0 and DOB1, with DQ8–DQ15 also to CIL.

C0–C6: Check-bit I/O port. 7-bit bidirectional bus which is connected to the input of the CIL and the output of the COB. COB is enabled whenever M2 is low.

S0–S6: Syndrome I/O port. 7-bit bidirectional bus which is connected to the input of the SIL and the output of the SOB.

DLE: Input data latch enable. When high, DIL0 and DIL1 outputs follow the input data bus. When low, DIL0 and DIL1 latch the input data.

CSLE: Input check bit and syndrome latch enable. When high, CIL and SIL follow the input check and syndrome bits. When low, CIL and SIL latch the input check and syndrome bits. If $\overline{OES}$ is low, SIL remains latched.

$\overline{OLE}$: Output latch enable. $\overline{OLE}$ enables the internally generated data to DOL0, and DOL1, COL and SOL when low, and latches when high.

XP: Multi-expansion, which feeds into a three-level comparator. With XP at 0V, only 6 or 7 check bits are available for expansion up to 40 bits, allowing byte parity capability. With XP open or at V_{CC}, expansion beyond 40 bits is possible, but byte parity capability is no longer available. When XP is at V_{CC}, CG6 and CG7, the internally generated upper two check bits, are set low. When XP is open, CG6 and CG7 are set to word parity.

BP0 (C7): When XP is at 0V, this pin is byte-0 parity I/O. In the Normal WRITE mode, BP0 receives system byte-0 parity, and in the Normal READ mode outputs system byte-0 parity. When XP is open or at V_{CC}, this pin becomes C7 I/O, the eighth check bit for the memory check bits, for 48-bit expansion and beyond.

BP1 (S7): When XP is at 0V, this pin is byte-1 parity I/O. In the Normal WRITE mode, BP1 receives system byte-1 parity, and in the Normal READ mode outputs system byte-1 parity. When XP is open or at V_{CC}, this pin becomes S7 I/O, the eight syndrome bit for 48-bit expansion and beyond.

AE: Any error. In the Normal READ mode, when low, AE indicates no error and when high, indicates that an error has occurred. In any WRITE mode, AE is permanently low.

E0: In the Normal READ mode, E0 is high for a single-data error, and low for other conditions. In the Normal WRITE mode, E0 becomes $\overline{PE0}$ and is low if a parity error exists in byte-0 as transmitted from the processor.

E1: In the Normal READ mode, E1 is high for a single-data error or a single check bit error, and low for no error and double-error. In the Normal WRITE mode, E1 becomes $\overline{PE1}$ and is low if a parity error exists in byte-1 as transmitted from the processor.

$\overline{OB0}$, $\overline{OB1}$: Output byte-0 and output byte-1 enables. These inputs, when low, enable DOL0 and DOL1 through DOB0 and DOB1 onto the data bus pins DQ0–DQ7 and DQ8–DQ15. When $\overline{OB0}$ and $\overline{OB1}$ are high the DOB0, DOB1 outputs are TRI-STATE®.

$\overline{OES}$: Output enables syndromes. I/O control of the syndrome latches. When high, SOB is TRI-STATE and external syndromes pass through the syndrome input latch with CSLE high. When $\overline{OES}$ is low, SOB is enabled and the generated syndromes appear on the syndrome bus, also CSLE is inhibited internally to SIL.

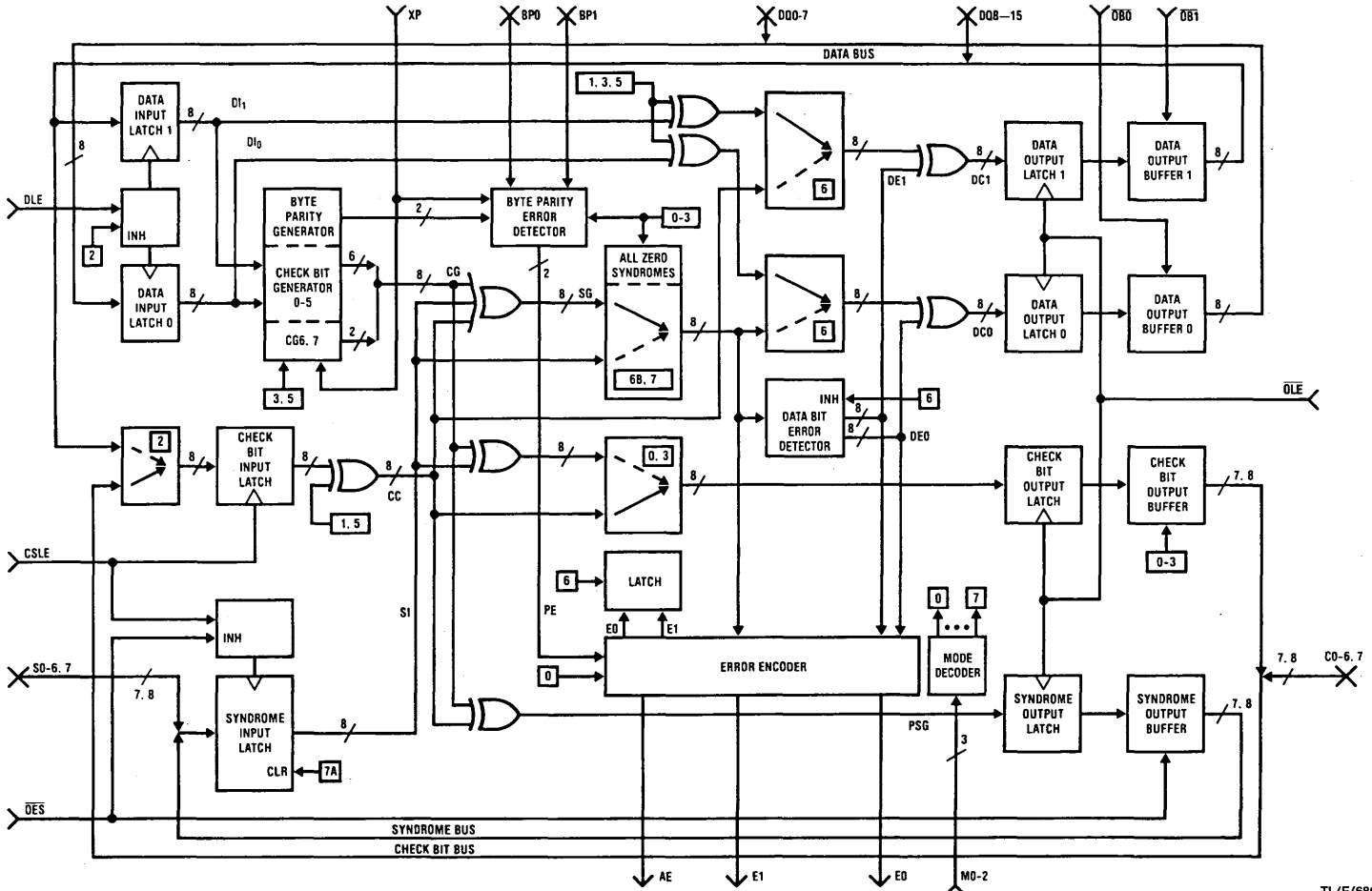
M0, M1, M2: Mode control inputs. These three controls define the eight major operational modes of the DP8400-2. Table III depicts the modes.

System Write (*Figure 2a*)

The Normal WRITE mode is mode 0 of Table III. Referring to the block diagram in *Figure 9a* and the timing diagram of *Figure 9b*, the 16 bits of data from the processor are enabled into the data input latches, DIL0 and DIL1, when the input data latch enable (DLE) is high. When this goes low, the input data is latched. The check bit generator (CG) then produces 6 parity bits, called check bits. Each parity bit monitors different combinations of the input data-bits. In the 16-bit configuration, assuming no syndrome bits are being fed in from the syndrome bus into the syndrome input latch, the 6 check bits enter the check bit output latch (COL), when the output latch enable $\overline{OLE}$ is low, and are latched in when $\overline{OLE}$ goes high. Whenever M2 (READ/$\overline{WRITE}$) is low, the check bit output buffer COB always enables the COL contents onto the external check bit bus. Also the data error decoder (DED) is inhibited during $\overline{WRITE}$ so no correction can take place. Data output latches DOL0 and DOL1, when enabled with $\overline{OLE}$, will therefore see the contents of DIL0 and DIL1. If valid system data is still on the data bus, a memory WRITE will write to memory the data on the data bus and the check bits output from COB. If the system has vacated the data bus, output enables ($\overline{OB0}$ and $\overline{OB1}$) must be set low so that the original data word with its 6 check bits can be written to memory.

System Read

There are two methods of reading data: the error monitoring method (*Figure 2b*), and the always correct method (*Figure 2c*). Both require fast error detection, and the second, fast correction. With the first method, the memory data is only monitored by the E^2C^2, and is assumed to be correct. If there is an error, the Any Error flag (AE) goes high, requiring further action from the system to correct the data. With the always correct method, the memory data is assumed to be possibly in error. Memory data is removed and the corrected, or already correct, data is output from the E^2C^2 by enabling $\overline{OB1}$ and $\overline{OB0}$. To detect an error (referring to *Figures 10a* and *10b*) first DLE and CSLE go high to enter data bits and check bits from memory into DIL0, DOL1 and CIL. The 6 check bits generated in CG from DIL0 and DOL1 are then compared with CIL to generate syndromes on the internal syndrome bus (SG). Any bit or bits of SG that go high indicate an error to the error encoder (EE).



DIL	Data Input Latch	SG	Syndrome Generator	SOL	Syndrome Output Latch
CG	Check Bit Generator	DED	Data Error Detector	DOB0, 1	Data Output Buffer Bytes 0, 1
CIL	Check Bit Input Latch	DE0, 1	Data Error Bytes 0, 1	COB	Check Bit Output Buffer
CC	Check Bit Complementor	PE	Parity Error	SOB	Syndrome Output Buffer
SIL	Syndrome Input Latch	DOL0, 1	Data Output Latch Bytes 0, 1	EE	Error Encoder
PSG	Partial Syndrome Generator	COL	Check Bit Output Latch	DC0, 1	Data Corrector Bytes 0, 1

[n] mode of operation signifies active signal

FIGURE 1. DP8400-2 Block Diagram

System Diagrams—Modes of Operation

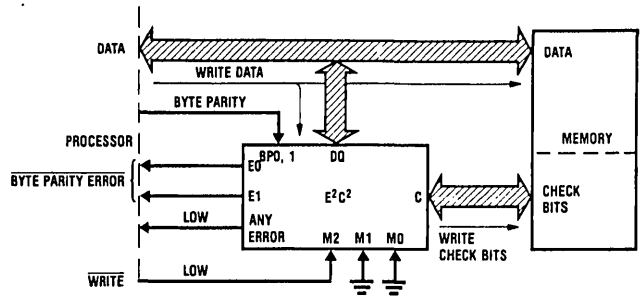


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FIGURE 2a. Normal WRITE Mode with E^2C^2

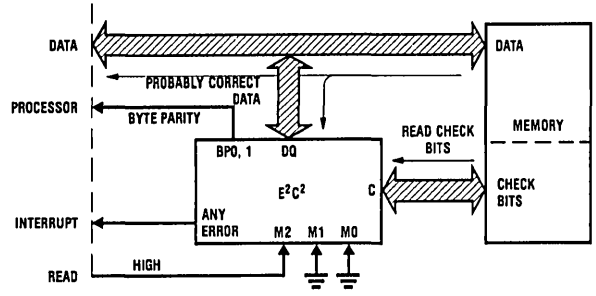

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FIGURE 2b. Normal READ Mode, Error Monitoring Method with E^2C^2

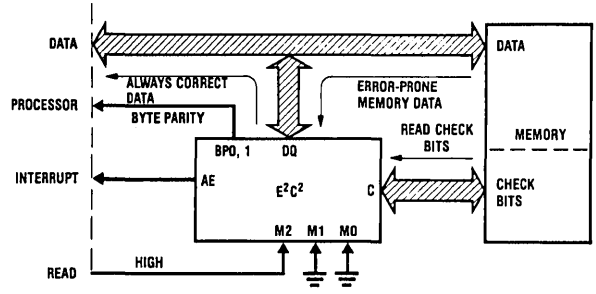

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FIGURE 2c. Normal READ Mode, Always Correct Method with E^2C^2

System Read (Continued)

If data correction is required $\overline{OB0}$ and $\overline{OB1}$ must be set low (after memory data has been disabled) to enable data output buffers DOB0 and DOB1. The location of any data bit error is determined by the data error decoder (DED), from the syndrome bits. The bit in error is complemented in the DOL for correction. The other 15 bits from DED pass the DIL contents directly to the DOL, so that DOL now contains corrected data.

Error Determination

The three error flags, for a 16-bit example, are decoded from the internally generated syndromes as shown in *Figure 3*. First, if any error has occurred, the generated check bits will be different from the memory check bits, causing some of the syndrome bits to go high. By OR-ing the syndrome bits, the output will be an indication of any error.

If there is a single-data error, then (from the matrix in Table IV) it can be seen that any data error causes either 3 or 5 syndrome bits to go high. 16 AND gates decode which bit is in error and the bit in error is XOR-ed with the corresponding bit of the DIL to correct it, whereas the other 15 decoder outputs are low, causing the corresponding 15 bits in DIL to transfer to DOL directly. DOL now contains corrected data. The 16 AND gate outputs are OR-ed together causing E0 to go high, so that E0 is the single-data-error indication. If the error is a double-error, then either 2, 4 or 6 of the syndrome bits will be high. The syndromes for two errors (including one or two check bit errors) are the two sets of syndromes for each individual error bit, XOR-ed together. By performing a parity check on the syndrome bits, flag E1 will indicate even/odd parity. If there is still an error, but it is not one of these errors, then it is a detectable triple-bit error. Some triple-bit errors are not detectable as such and may be interpreted as single-bit errors and falsely corrected as single-data errors. This is true for all standard ECC circuits using a Modified Hamming-code matrix. The DP8400-2 is capable, with its Rotational Syndrome Word Generator matrix, of determining all triple-bit errors using twice as many DP8400-2s and twice as many check bits.

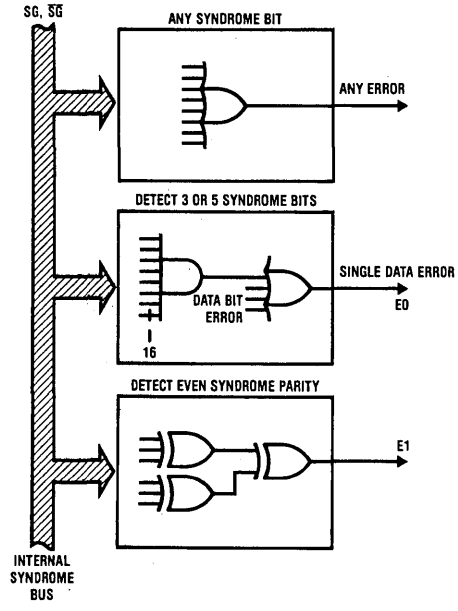

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FIGURE 3. Error Encoder

Error Flags

Three error flags are provided to allow full error determination. Table I shows the error flag outputs for the different error types in Normal READ mode. If there is an error, then ANY ERROR will go high, at a time t_{DEV} (*Figure 10b*) after data and check bits are presented to the DP8400-2. The other two error flags E0 and E1 become valid t_{DE0} and t_{DE1} later.

The error flags differentiate between no error, single check bit error, single data-bit error, double-bit error. Because the DP8400-2 can correct double errors, it is important to know that two errors have occurred, and not just a multiple-error indication. The error flags will remain valid as long as DLE and CSLE are low, or if DLE is high, and data and check bits remain valid.

Byte Parity Support

Some systems require extra integrity for transmission of data between the different cards. To achieve this, individual byte parity bits are transmitted with the data bits in both directions. The DP8400-2 offers byte parity support for up to 40 data bits. If the processor generates byte parity when transferring information to the memory, during the WRITE cycle, then each byte parity bit can be connected to the corresponding byte parity I/O pin on the DP8400-2, either BP0 or BP1. The DP8400-2 develops its own internal byte parity bits from the two bytes of data from the processor, and compares them with BP0 and BP1 using an exclusive-OR for both parities. The output of each exclusive-OR is fed to the error flags E0 and E1 as $\overline{PE0}$ and $\overline{PE1}$, so that a byte parity error forces its respective error flag low, as in Table II. These flags are only valid for the Normal WRITE (mode 0) and XP at 0V. The DP8400-2 checks and generates even byte parity.

When transferring information from the memory to the processor, the DP8400-2 receives the memory data, and outputs the corresponding byte parity bits on BP0 and BP1 to the processor. The processor block can then check data integrity with its own byte parity generator. If in fact memory data was in error, the DP8400-2 derives BP0 and BP1 from the memory input data, and not the corrected data, so when corrected data is output from the DP8400-2, the processor will detect a byte parity error.

During the read mode, DP8400-2 corrects single data bit error and also its parity.

TABLE I. Error Flags After Normal Read (Mode 4)

AE	E1	E0	Error Type
0	0	0	No error
1	1	0	Single check bit error
1	1	1	Single-data error
1	0	0	Double-bit error
All Others			Invalid conditions

TABLE II. Error Flags after Normal Write (Mode 0)

AE	E1 ($\overline{PE1}$)	E0 ($\overline{PE0}$)	Error Type
0	1	1	No parity error
0	1	0	Parity error, byte 0
0	0	1	Parity error, byte 1
0	0	0	Parity error, bytes 0, 1

TABLE III. DP8400-2 Modes of Operation

Mode	M2 (R/W)	M1	M0	$\overline{OES}$	Operation
0	0	0	0	X	Normal WRITE DIL → DOL, CG → COL → COB
1	0	0	1	X	Complement WRITE $\overline{DIL}$ → DOL, $\overline{CIL}$ → COL → COB
2	0	1	0	X	Diagnostic WRITE, DLE inhibited DQ8–DQ15 ⊕ CG → SOL → SOB DQ8–DQ15 → CIL → COL → COB
3	0	1	1	X	Complement data-only WRITE $\overline{DIL}$ → DOL, (CG0, 1, 4, 5, $\overline{CG2}$, $\overline{CG3}$) → COL → COB
4	1	0	0	X	Normal READ DIL ⊕ DE → DOL, CIL → COL
5	1	0	1	X	Complement READ $\overline{DIL}$ ⊕ DE → DOL, $\overline{CIL}$ → COL
6A	1	1	0	0	READ generated syndromes, check bit bus, error flags, SG0–SG6 → DQ0–DQ6, CIL0–CIL6 → DQ8–DQ14, E1 → DQ7, E0 → DQ15
6B	1	1	0	1	READ syndrome bus, check bit bus, error flags, SIL0–SIL6 → DQ0–DQ6, CIL0–CIL6 → DQ8–DQ14, E1 → DQ7, E0 → DQ15
7A	1	1	1	0	Generated syndromes replace with zero 0 → SIL → SG, CIL → COL, DIL ⊕ DE → DOL
7B	1	1	1	1	Generated syndromes replace SIL → SG, CIL → COL, DIL ⊕ DE → DOL

TABLE IV. Data-In To Check Bit Generate, Or Data Bit Error To Syndrome-Generate Matrix (16-Bit Configuration)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	GENERATE CHECK BITS →																DQ0–15
0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1
2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2*
3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3*
4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
GENERATED SYNDROMES																	GENERATED CHECK BITS
	4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	0
	3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	1
	HEXADECIMAL EQUIVALENT OF SYNDROME BITS																

*C2, C3 generate odd parity

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Modes of Operation

There are three mode-control pins, M2, M1 and M0, offering 8 major modes of operation, according to Table III.

M2 is the READ/$\overline{\text{WRITE}}$ control. In normal operation, mode 0 is Normal WRITE and mode 4 is Normal READ. By clamping M0 and M1 low, and setting M2 low during WRITE and high during READ, the DP8400-2 is very easy to use for normal operation. The other modes will be covered in later sections.

16-BIT CONFIGURATION

The first two rows on top of the check bit generate matrix (Table IV) indicate the data position of DQ0 to DQ15. The left side of the matrix, listed 0 to 5, corresponds to syndromes S0 to S5. S0 is the least significant syndrome bit. There are two rows of hexadecimal numbers below the matrix. They are the hex equivalent of the syndrome patterns. For example, syndrome pattern in the first column of the matrix is 001011. Its least significant four bits (0010) equal hexadecimal 4, and the remaining two bits (11) equal hexadecimal 3.

Check bit generation is done by selecting different combinations of data bits and generating parities from them. Each row of the check bit generate matrix corresponds to the generation of a check bit numbered on the right hand side of the matrix, and the ones in that row indicate the selection of data bits.

The following are the check bit generate equations for 16-bit wide data words:

$$CG0 = DQ2 \oplus DQ3 \oplus DQ4 \oplus DQ5 \oplus DQ6 \oplus DQ7 \oplus DQ9 \oplus DQ10 \oplus DQ11 \oplus DQ13 \oplus DQ14 \oplus DQ15$$

$$CG1 = DQ3 \oplus DQ6 \oplus DQ8 \oplus DQ9 \oplus DQ11 \oplus DQ13 \oplus DQ14 \oplus DQ15$$

$$*CG2 = DQ0 \oplus DQ3 \oplus DQ4 \oplus DQ8 \oplus DQ10 \oplus DQ12 \oplus DQ13 \oplus DQ14 \oplus DQ15 \oplus 1$$

$$*CG3 = DQ1 \oplus DQ2 \oplus DQ7 \oplus DQ8 \oplus DQ9 \oplus DQ10 \oplus DQ12 \oplus DQ14 \oplus DQ15 \oplus 1$$

$$CG4 = DQ0 \oplus DQ1 \oplus DQ5 \oplus DQ7 \oplus DQ8 \oplus DQ11 \oplus DQ13 \oplus DQ15$$

$$CG5 = DQ0 \oplus DQ1 \oplus DQ2 \oplus DQ4 \oplus DQ5 \oplus DQ6 \oplus DQ8 \oplus DQ12 \oplus DQ13 \oplus DQ14$$

*CG2 and CG3 are odd parities.

The following error map (Table V) depicts the relationship between all possible error conditions and their associated syndrome patterns. For example, if a syndrome pattern is S0–5 = 111101, data bit 14 is in error.

Figure 4 shows how to connect one DP8400-2 in a 16-bit configuration, in order to detect and correct single or double-bit errors. For a Normal WRITE, processor data is presented to the DP8400-2, where it is fed through DIL0 and DIL1 to the check bit generator. This generates 6 parity bits from different combinations of data bits, according to Table IV. The numbers in the row below the table are the hexadecimal equivalent of the column bits (with bits 6, 7 low). A "1" in any row indicates that the data bit in that column is connected to the parity generator for that row. For example, check bit 1 generates parity from data bits 3, 6, 8, 9, 11, 13, 14, and 15.

Check bits 0, 1, 4, 5, and 6 generate even parity, and check bits 2 and 3 generate odd parity. This is done to insure that a total memory failure is detected. If all check bits were even parity, then all zeroes in the data word would generate all check bits zero and a total memory failure would not be detected when a memory READ was performed. Now all-zero-data bits produce C2 and C3 high and a total memory failure will be detected. When reading back from the same location, the memory data bits (possibly in error) are fed to the same check bit generator, where they are compared to the memory check bits (also possibly in error) using 6 exclusive-OR gates. The outputs of the XORs are the syndrome bits, and these can be determined according to Table IV for one data bit error. For example, an error in bit 2 will produce the syndrome word 101001 (for S5 to S0 respectively). The syndrome word is decoded by the error encoder to the error flags, and the data-error decoder to correct a single data bit error. Assuming the memory data has been latched in the DIL, by making DLE go low, memory data can be disabled. Then by setting $\overline{\text{OB0}}$ and $\overline{\text{OB1}}$ low, corrected data will appear on the data bus. The syndromes are available as outputs on pins S0–5 when $\overline{\text{OES}}$ is low. It is also possible to feed in syndromes to SIL when $\overline{\text{OES}}$ is high and CSLE goes high. This can be useful when using the Error Management Unit shown in *Figure 4*. C6 and S6 are not used for 16 bits. It is safe therefore to make C6 appear low, through a 2.7 kΩ resistor to ground. The same applies for S6 if syndromes are input to the DP8400-2. If $\overline{\text{OES}}$ is permanently low, S6 may be left open.

Any 16-bit memory correct system using the DP8400-2 without syndrome inputs must keep the $\overline{\text{OES}}$ pin grounded, then all the syndrome I/O pins may be left open. The reason for this is that the DP8400-2 resets the syndrome input latch at power up. If the $\overline{\text{OES}}$ pin is grounded, the syndrome input latch will remain reset for normal operations.

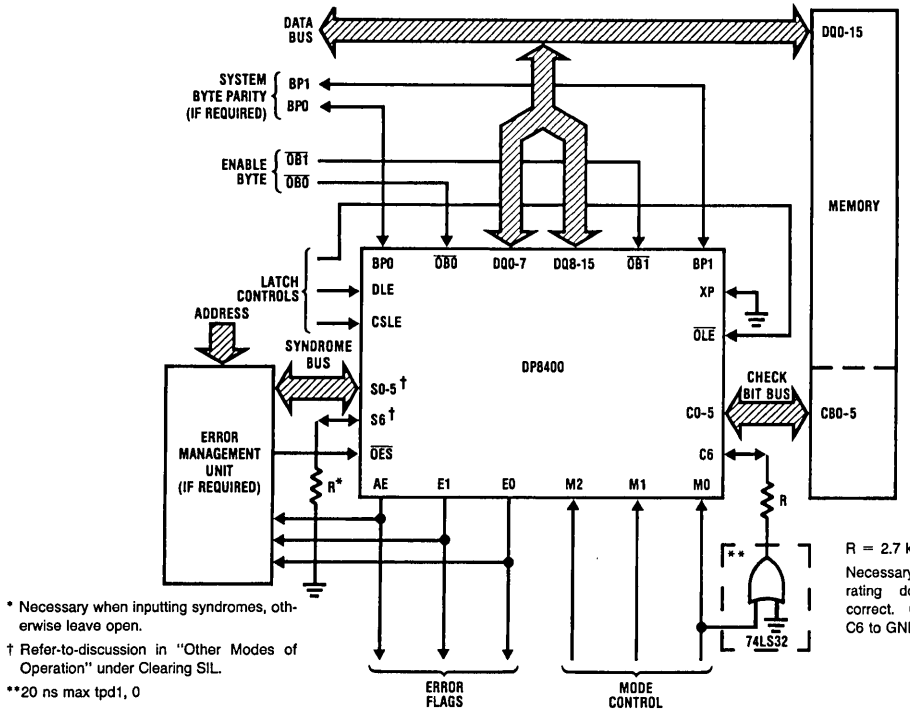
The parameter t_{NMR} (see *Figure 10b*), new mode recognized time, is measured from M2 (changing from READ to WRITE) to the valid check bits appearing on the check bit bus, provided the $\overline{\text{OLE}}$ was held low.

The parameter t_{MCR} (see *Figure 10b*), mode change recognized time, is measured from M2 (changing from WRITE to

TABLE V. Syndrome Decode To Bit In Error For 16-Bit Data Word

		S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Syndrome		**S1**	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Bits		**S2**	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S5	**S4**																	
0	0		NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	1		C4	D	D	11	D	T	T	D	D	7	T	D	T	D	D	15
1	0		C5	D	D	6	D	4	T	D	D	2	T	D	12	D	D	14
1	1		D	5	T	D	0	D	D	13	1	D	D	T	D	T	8	D

NE = no error Cn = check bit n in error T = three errors detected Number = single data bit in error D = two bits in error



* Necessary when inputting syndromes, otherwise leave open.

† Refer-to-discussion in "Other Modes of Operation" under Clearing SIL.

**20 ns max tpd1, 0

R = 2.7 kΩ

Necessary only when incorporating double complement correct. Otherwise connect C6 to GND through R.

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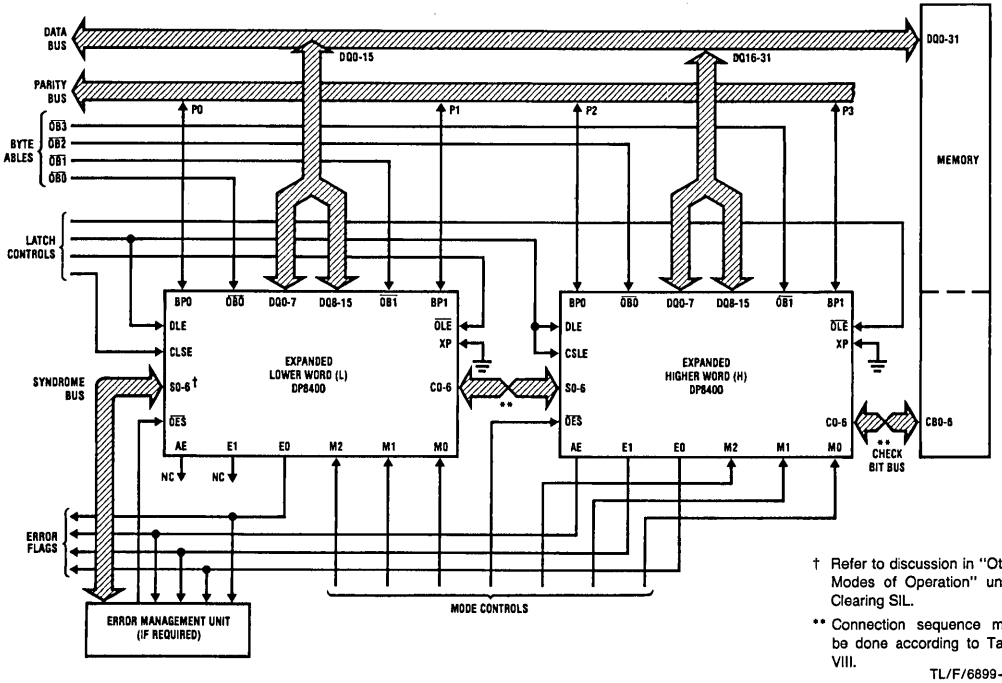
FIGURE 4. 16-Bit Configuration Using One DP8400-2



† Refer to discussion in "Other Modes of Operation" under Clearing SIL.

** Connection sequence must be done according to Table VIII.

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FIGURE 5. 32-Bit Error Detection and Correction

Modes of Operation (Continued)

READ) when both E1 and E2 become invalid. This is required when a memory correcting system employs the DP8400-2 with byte parity checking. The E1 and E2 pins flag the byte parity error in a memory WRITE cycle. When the DP8400-2 switches to a subsequent memory READ cycle, it requires t_{MCR} for E1 and E2 to be switched to flag any READ error(s).

Expanded Operation

32-BIT CONFIGURATION

Figure 5 shows how to connect two DP8400-2s in cascade to detect single and double-bit errors, and to correct single-data errors. The same circuit will also correct double-bit errors once a double-error has been detected, provided at least one error is a hard error. The lower chip L is in effect a slave to the higher chip H, which controls the memory check bits and error reporting. The check bit bus of L is reordered and connected to the syndrome bus of H, as shown in *Figure 5*.

In a Normal WRITE mode, referring to *Figures 13a, 13b,* and *13c*, the 7 check bits generated from the lower 16 bits (CGL) are transferred via the COL to the COB of L, provided $\overline{OLE}$ is high and M2 (R/$\overline{W}$) of L is low. These partial check bits from L then appear at SIL of H, so that with CSLE high, they combine with the 6 check bits generated in H with an overlap of one bit, to produce 7 check bits. With M2 (R/$\overline{W}$) of H low, these 7 check bits are output from COB to memory.

A READ cycle may consist of DETECT ONLY or DETECT THEN CORRECT, depending on the system approach. In both approaches, L writes its partial check bits, CGL, to H as in WRITE mode. H develops the syndrome bits from CGL, CGH and the 7 check bits read from memory in CIL. H then outputs from its error encoder (EE) if there is an error. If corrected data is required, H already knows if it has a single-data error from its syndrome bits, but if not, it must transfer partial syndromes back to L. These partial syndromes PSH, (CGH XOR-ed with CIL), are stored in SOL of H. L must therefore change modes from WRITE to READ, while H outputs the partial syndromes from its SOB by setting $\overline{OES}$ low. The partial syndromes are fed into CIL of L and XOR-ed with CGL to produce syndrome bits at SGL. The data error decoder, DED, then corrects the error in L. The DED of H will already have corrected an error in the higher 16 bits. Only one error in 32 bits can be corrected as a single-data error, the chip with no error does not change the contents of its DIL when it is enabled in DOL. Table VI shows the 3 error flags of H, which become valid during the DETECT cycle. E0 of L becomes valid during the CORRECT cycle, so that the 4 flags provide complete error reporting.

TABLE VI. Error Flags After Normal READ (32-Bit Configuration)

AE (H)	E1 (H)	E0 (H)	E0 (L)*	Error Type
0	0	0	0	No error
1	1	0	0	Single-check bit error
1	1	1	0	Single-data bit error (H)
1	1	0	1	Single-data bit error (L)
1	0	0	0	Double-bit error
All Others				Invalid conditions

*E0 (L) is valid after transfer of partial syndromes from higher to lower

Equations for 32-bit expansion:

$$t_{DCB32} = t_{DCB16} + t_{SCB16}$$

$$t_{DEV32} = t_{DCB16} + t_{SEV16}$$

$$t_{DCD32}\ (\text{High Chip}) = t_{DCB16} + t_{SCD16}$$

$$t_{DCD32}\ (\text{Low Chip}) = t_{DCB16} + t_{BR}{}^{*} + t_{CCD16}$$

*t_{BR}: Bus reversing time (25 ns)

32-BIT MATRIX

Table VII shows a 32-bit matrix using two DP8400-2s in cascade as in *Figure 5*. This is one of 12 matrices that work for 32 bits. The matrix for bits 0 to 15 (lower chip) is the matrix of Table IV for 16-bit configuration, with row 6 always "0". The matrix for bits 16 to 31 (higher chip) uses the same row combinations but interchanged, for example, the 3rd row (row 2) of L matrix is the same as the 6th row (row 5) of the H matrix. This means row 5 of H is in fact check bit 2 of H. Thus, the 6th row (row 5) combines generated check bit 5 (CG5) of L and generated check bit 2 of H. Check bit 5 of L therefore connects to the syndrome bit 2 (CG2) of H, and the composite generated check bit is written to check bit 2 of memory. Thus C2 performs a parity check on bits 0, 1, 2, 4, 5, 6, 8, 12, 13, 14, of L, and bits 16, 19, 20, 24, 26, 28, 29, 30, 31, of H. CG2 and CG3 generate odd parity, so that CG5 of L generates even parity which combines with CG2 of H generating odd parity. CG3 of L and CG3 of H both generate odd parity causing C3 to memory to represent even parity. Only 6 check bits are generated in each chip, the 7th (CG6) is always zero with XP grounded. Thus CG6 of L combines with CG0 of H so that C0 to memory is the parity of bits 18, 19, 20, 21, 22, 23, 25, 26, 27, 29, 30, 31. Similarly C6 to memory is only CG2 of L. The 7 composite generated check bits of H can now be written to memory.

When reading data and check bits from memory, CG6–CG0 of L are combined with CG6–CG0 of H in the same combination as WRITE. Memory check bits are fed into C6–C0 of H and compared with the 7 combined parity bits in H, to

TABLE VII. Data Bit Error To Syndrome-Generate Matrix (32-Bit Configuration)

	L																H																
											1	1	1	1	1	1																		
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	DQ0-31
0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1
1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
*2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
*3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3
4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	2	A	A	1	2	2	3	8	B	9	8	1	A	3	B	9	0	HEX
	3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	3	1	4	6	6	5	4	5	3	4	6	5	2	7	6	7	1	

SYNDROMES

GENERATED CHECK BITS

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*CG2, CG3 generate odd parity

Expanded Operation (Continued)

TABLE VIII. Check Bit Port To Syndrome Port Interconnections For Expansion To 32 Bits

		LS		LC	HS		HC		
Syndrome I/O to Management	S0	0		0	1		1	C0	Check Bit I/O to Memory
	S1	1		1	5		5	C1	
	S2	2		2	6		6	C2	
	S3	3		3	3		3	C3	
	S4	4		4	4		4	C4	
	S5	5		5	2		2	C5	
	S6	6		6	0		0	C6	

TABLE IX. Syndrome Decode To Bit In Error For 32-Bit Data Word

Syndrome Bits			S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S6	S5	S4																	
0	0	0		NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	0	1		C4	D	D	11	D	T	T	D	D	7	17	D	T	D	D	15
0	1	0		C5	D	D	6	D	4	T	D	D	2	28	D	12	D	D	14
0	1	1		D	5	16	D	0	D	D	13	1	D	D	24	D	T	8	D
1	0	0		C6	D	D	22	D	T	T	D	D	25	18	D	T	D	D	T
1	0	1		D	27	21	D	T	D	D	T	23	D	D	T	D	T	T	D
1	1	0		D	19	20	D	T	D	D	T	26	D	D	30	D	T	T	D
1	1	1		T	D	D	29	D	T	T	D	D	31	T	D	T	D	D	T

NE = no error Cn = check bit n in error T = three errors detected
Number = single data bit in error D = two bits in error

produce 7 syndrome bits S6–S0. H can now determine if there is any error, and if it has a single-data error, it can locate it and correct it without transferring partial syndromes to L. As an example of a DETECT cycle, CG5 of L combines with CG2 of H and is compared in H with memory check bit 2.

If L is now set to mode 4, Normal READ, and $\overline{OES}$ of H is set low, the partial syndromes of H (CG6–CG0 of H XOR-ed with C6–C0 of H) are transferred and shifted to L. L receives these partial syndromes (S6–S0 of H) as check bit inputs C2, C1, C4, C3, C5, C0, C6 respectively, and compares them with CG6–CG0 respectively, to produce syndrome bits S6–S0. L now decodes these syndromes to correct any single-data error in data bits 0 to 15. For example, partial syndrome bit 2 of H combines with generated check bit 5 of L to produce syndrome bit 5 in L. An error in data bit 10 will create syndrome bits in L as 0001101 from S6–S0, and these will appear on S6–S0 of L with $\overline{OES}$ low. An error in H will appear as per the H matrix. For example, an error in bit 16 will cause S6–S0 of L to be 0110010.

If $\overline{OES}$ of L is set low, this syndrome combination appears on pins S6 to S0. For errors in bits 0 to 15, the syndrome outputs will be according to Table VII. For errors in bits 16 to 31, the syndrome outputs from L will still be according to Table VII due to the shifting of partial syndrome bits from H to L. The syndrome outputs from L are unique for each of the possible 32 bits in error.

If there is a check bit error, only one syndrome bit will be high. For example, if C5 is in error, then S1 of L will be high. For double-errors, an even number of syndrome bits will be high, derived from XOR-ing the two single-bit error syndromes. As mentioned previously, this is only one of the 12 approaches to connecting two chips for 32 bits, 6 of which are mirror images.

Table VIII depicts the exact connection for 32-bit expansion. LS equals syndrome bits of L. LC equals check bits of L. HS equals syndrome bits of H. HC equals check bits of H. Syndrome bits S0 to S6 of L are connected to system syndrome bits S0 to S6. LC and HS columns are lined together showing the check bit port of L connected to the syndrome port of H in the exact sequence as shown in Table VIII. For example, check bit C0 of L is connected to the syndrome bit S1 of H, and check bit C6 of L is connected to the syndrome bit S0 of H. Check bits of H are connected to the system check bits in the order shown. Check bit C1 of H is connected to the system check bit C0.

EXPANSION FOR DATA WORDS REQUIRING 8 CHECK BITS

For 16-bit and 32-bit configurations, XP is set permanently low. In 48-bit or 64-bit configurations, XP is either set permanently to V_{CC} or left open, according to Table X, to provide 8 check bits and syndrome bits.

TABLE X. XP: Expansion Status

XP	Status	Data Bus
0V	BP0 and BP1 are byte parity I/O CG6 = 0	< 40 Bits
Open	No byte parity I/O, CG6 and CG7 = word parity	≥ 40 Bits
V_{CC}	No byte parity I/O, CG6 and CG7 = 0	≥ 40 Bits

48-BIT EXPANSION

Three DP8400-2s are required for 48 bits, with the higher chip using all 8 of its check bits to the memory. No byte parity is available for 48 to 64 bits. XP of all three chips must be at V_{CC}. The three chips are connected in cascade as in

Expanded Operation (Continued)

TABLE XI. Check Bit Port To Syndrome Port Interconnections For Expansion To 48 Bits

		LL S		LL C	LH S		LH C	HL S		HL C		
Syndrome I/O to Management	S0	0		0	1		1	6		6	C0	Check Bit I/O to Memory
	S1	1		1	5		5	1		1	C1	
	S2	2		2	6		6	4		4	C2	
	S3	3		3	3		3	7		7	C3	
	S4	4		4	4		4	2		2	C4	
	S5	5		5	2		2	3		3	C5	
	S6	6		6	0		0	5		5	C6	
	S7	7		7	7		7	0		0	C7	

For example: S0 of LL is connected to system syndrome S0. C0 of LL is connected to S1 of LH. C1 of LH is connected to S6 of HL. C6 of HL is connected to system check bit C0.

TABLE XII. Syndrome Decode To Bit In Error For 48-Bit Data Word

Syndrome Bits S7	S6	S5	S0 S1 S2 S3 S4																
			S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	0	0	1	C4	D	D	11	D	T	T	D	D	7	17	D	T	D	D	15
0	0	1	0	C5	D	D	6	D	4	T	D	D	2	28	D	12	D	D	14
0	0	1	1	D	5	16	D	0	D	D	13	1	D	D	24	D	T	8	D
0	1	0	0	C6	D	D	22	D	T	T	D	D	25	18	D	T	D	D	T
0	1	0	1	D	27	21	D	32	D	D	T	23	D	D	T	D	T	T	D
0	1	1	0	D	19	20	D	33	D	D	T	26	D	D	30	D	T	T	D
0	1	1	1	44	D	D	29	D	T	40	D	D	31	T	D	T	D	D	T
1	0	0	0	C7	D	D	T	D	T	43	D	D	T	T	D	T	D	D	T
1	0	0	1	D	T	35	D	T	D	D	T	T	D	D	T	D	T	T	D
1	0	1	0	D	T	41	D	39	D	D	T	T	D	D	T	D	T	T	D
1	0	1	1	42	D	D	T	D	T	47	D	D	T	T	D	T	D	D	T
1	1	0	0	D	T	38	D	37	D	D	T	T	D	D	T	D	T	T	D
1	1	0	1	36	D	D	T	D	T	45	D	D	T	T	D	T	D	D	T
1	1	1	0	34	D	D	T	D	T	T	D	D	T	T	D	T	D	D	T
1	1	1	1	D	T	46	D	T	D	D	T	T	D	D	T	D	T	T	D

NE = no error Cn = check bit n in error T = three errors detected
Number = single data bit in error D = two bits in error

Figure 6, but with the HH chip removed. The error flags are as Table XV, but with AE (HH) and E1 (HH) becoming AE (HL) and E1 (HL), and E0 (HH) removed.

48-BIT MATRIX

The matrix for 48 bits is that for 64 bits shown (in Table XVI) but only using bits 0 to 47. This is one of many matrices for 48-bit expansion using the basic 16-bit matrix. The matrix shown uses 2 zeroes for CG6 and CG7, for all three chips, with XP set to V_{CC}. Other matrices may use CG6 and CG7 as word parity with XP open.

64-BIT EXPANSION

There are two basic methods of expansion to 64 bits, both requiring 8 check bits to memory, and four DP8400-2s. One is the cascade method of *Figure 6*, requiring no extra ICs. With this method partial check bits have to be transferred through three chips in the WRITE or DETECT mode, and partial syndrome bits transferred back through three chips in CORRECT mode. This method is similar to *Figure 5*, 32-bit approach. The connections between the check bit bus and syndrome bus for each of the chip pairs are shown in Table XIII.

The error flags of HH are valid during the DETECT cycle as in Table XV, and the other error flags are valid during the CORRECT cycle.

A faster method of 64-bit expansion shown in *Figure 7* requires a few extra ICs, but can WRITE in 50 ns, DETECT in 42 ns or DETECT THEN CORRECT in 90 ns. In the WRITE mode, all four sets of check bits are combined externally in the 8 74S280 parity generators. These generate 8 composite check bits from the system data, which are then enabled to memory. In the DETECT mode, again 8 composite check bits are generated, from the memory data this time, and compared with the memory check bits to produce 8 external syndrome bits. These syndrome bits may be OR-ed to determine if there is any error. By making the 74S280 outputs $\overline{\text{SYNDROMES}}$, then any bit low causes the 74S30 NAND gate to go high, giving any error indication. To correct the error, these syndrome bits are fed re-ordered into SIL of each DP8400-2 now set to mode 7B. This enables the syndromes directly to SG and then DED of each chip. One chip

Expanded Operation (Continued)

will output corrected data, while the other three output non-modified data (but still correct).

Equations for fast 64-bit expansion:

$t_{DCB64} = t_{DCB16} + t_{pd}$ (74S280) + t_{pd} (74S240)

$t_{DEV64} = t_{DCB16} + t_{pd}$ (74S280) + t_{pd} (74S30)

$t_{DCB64} = t_{DCB16} + t_{pd}$ (74S280) + t_{pd} (74ALS533) + t_{SCD16}

64-BIT MATRIX

With the 64-bit matrix shown in Table XVI, it is necessary to set at least one chip with CG6, CG7 non-zero. The highest chip, connected to data bits 48 to 63, has XP set open, so that its CG6 and CG7 are word parity. The syndrome word of the highest chip will now have either 5 or 7 syndrome bits high, but inside the chip CG6 and CG7 remove two of these in a READ so that the chip sees the normal 3 or 5 syndrome bits.

TABLE XIII. Check Bit Port To Syndrome Port Interconnections For Expansion To 64 Bits

		LL S		LL C	LH S		LH C	HL S		HL C	HH S		HH C		
Syndrome I/O to Management	S0	0		0	1		1	6		6	7		7	C0	Check Bit I/O to Memory
	S1	1		1	5		5	1		1	0		0	C1	
	S2	2		2	6		6	4		4	1		1	C2	
	S3	3		3	3		3	7		7	2		2	C3	
	S4	4		4	4		4	2		2	3		3	C4	
	S5	5		5	2		2	3		3	4		4	C5	
	S6	6		6	0		0	5		5	5		5	C6	
	S7	7		7	7		7	0		0	6		6	C7	

For example: S0 of LL is connected to system syndrome S0. C0 of LL is connected to S1 of LH. C1 of LH is connected to S6 of HL. C6 of HL is connected to S7 of HH. C7 of HH is connected to system check bit C0.

TABLE XIV. Syndrome Decode To Bit In Error For 64-Bit Data Word

Syndrome Bits				S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S7	S6	S5	S4																	
0	0	0	0	NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	0	0	1	C4	D	D	11	D	T	T	D	D	7	17	D	T	D	D	15
0	0	1	0	C5	D	D	6	D	4	T	D	D	2	28	D	12	D	D	14
0	0	1	1	D	5	16	D	0	D	D	13	1	D	D	24	D	T	8	D
0	1	0	0	C6	D	D	22	D	T	T	D	D	25	18	D	T	D	D	T
0	1	0	1	D	27	21	D	32	D	D	T	23	D	D	T	D	T	T	D
0	1	1	0	D	19	20	D	33	D	D	T	26	D	D	30	D	T	T	D
0	1	1	1	44	D	D	29	D	T	40	D	D	31	T	D	T	D	D	T
1	0	0	0	C7	D	D	T	D	T	43	D	D	T	T	D	T	D	D	51
1	0	0	1	D	T	35	D	T	D	D	57	T	D	D	58	D	T	T	D
1	0	1	0	D	T	41	D	39	D	D	59	T	D	D	T	D	T	T	D
1	0	1	1	42	D	D	55	D	T	47	D	D	T	T	D	T	D	D	63
1	1	0	0	D	T	38	D	37	D	D	54	T	D	D	52	D	T	T	D
1	1	0	1	36	D	D	50	D	T	45	D	D	60	T	D	T	D	D	62
1	1	1	0	34	D	D	53	D	T	T	D	D	48	T	D	T	D	D	61
1	1	1	1	D	49	46	D	T	D	D	T	T	D	D	T	D	56	T	D

NE = no error
Cn = check bit n in error
T = three errors detected
Number = single data bit in error
D = two bits in error

TABLE XV. Error Flags After Normal READ (Any 64-Bit Configuration)

AE (HH)	E1 (HH)	E0 (HH)	E0 (HL)	E0 (LH)	E0 (LL)	Error Type
0	0	0	0	0	0	No error
1	1	0	0	0	0	Single-check bit error
1	1	1	0	0	0	Single-data bit error in HH
1	1	0	1	0	0	Single-data bit error in HL
1	1	0	0	1	0	Single-data bit error in LH
1	1	0	0	0	1	Single-data bit error in LL
1	0	0	0	0	0	Double-error

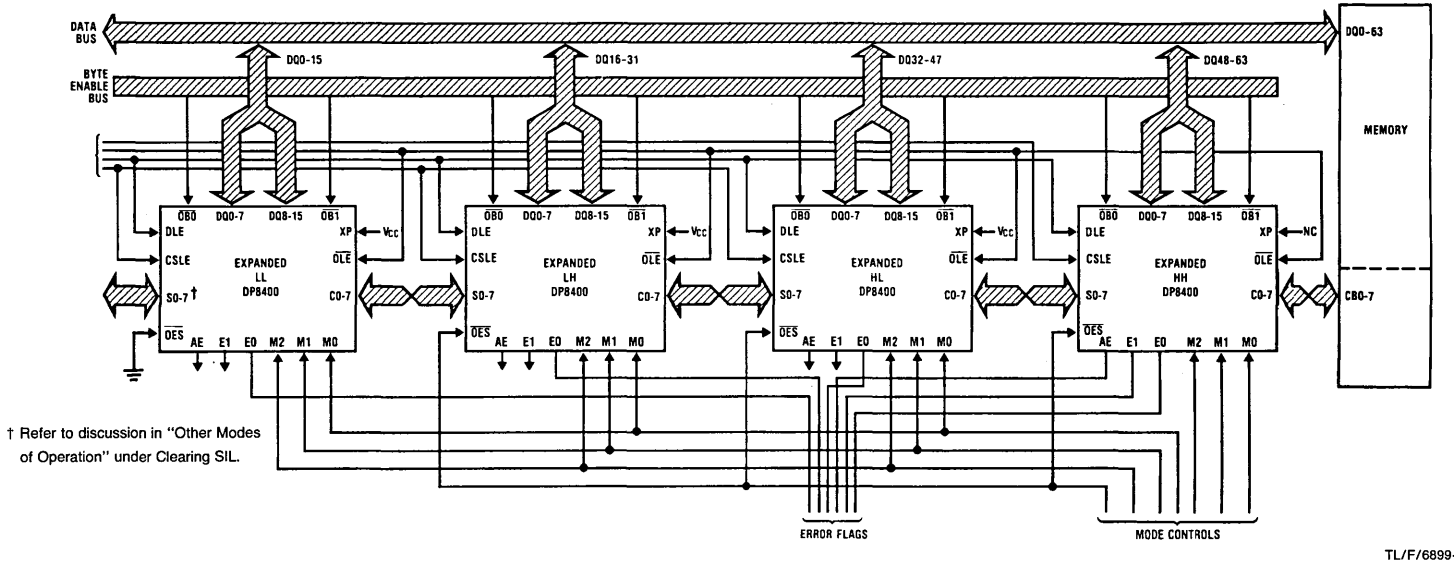

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FIGURE 6. Cascade Expansion Using No Extra ICs (64-Bit Configuration)

TABLE XVI. Data Bit Error To Syndrome-Generate Matrix (64-Bit Configuration)

SYNDROMES	LL	LH	HL	HH	GENERATED CHECK BITS
	0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5	6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1	2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7	8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3	DQ0-63
0	0 0 1 1 1 1 1 1 0 1 1 1 0 1 1 1	0 0 0 1 0 0 1 0 1 1 0 1 0 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	7
1	0 0 0 1 0 0 1 0 1 1 1 0 1 0 1 1 1	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	0 0 0 1 0 0 1 0 1 1 1 0 1 0 1 1 1	0 0 1 1 1 1 1 1 0 1 1 1 0 1 1 1	0
2	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	0 0 0 1 0 0 1 0 1 1 1 0 1 0 1 1 1	1
3	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	2
4	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	3
5	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	4
6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 0 1 1 1 0 1 1 1	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	5
7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6
	4 8 9 7 5 1 3 9 E B D 3 C 7 F F	2 A A 1 2 2 3 8 B 9 8 1 A 3 B 9	4 4 0 2 0 4 2 4 6 2 0 6 0 6 2 6	9 1 3 F B 3 7 3 D 7 B 7 9 F F F	0 HEX
	3 3 2 0 2 3 2 1 3 0 0 1 2 3 2 1	3 1 4 6 6 5 4 5 3 4 6 5 2 7 6 7	5 6 E 9 D C C A 7 A B 8 7 D F B	E F D 8 C E C B F 9 9 A D E D B	1

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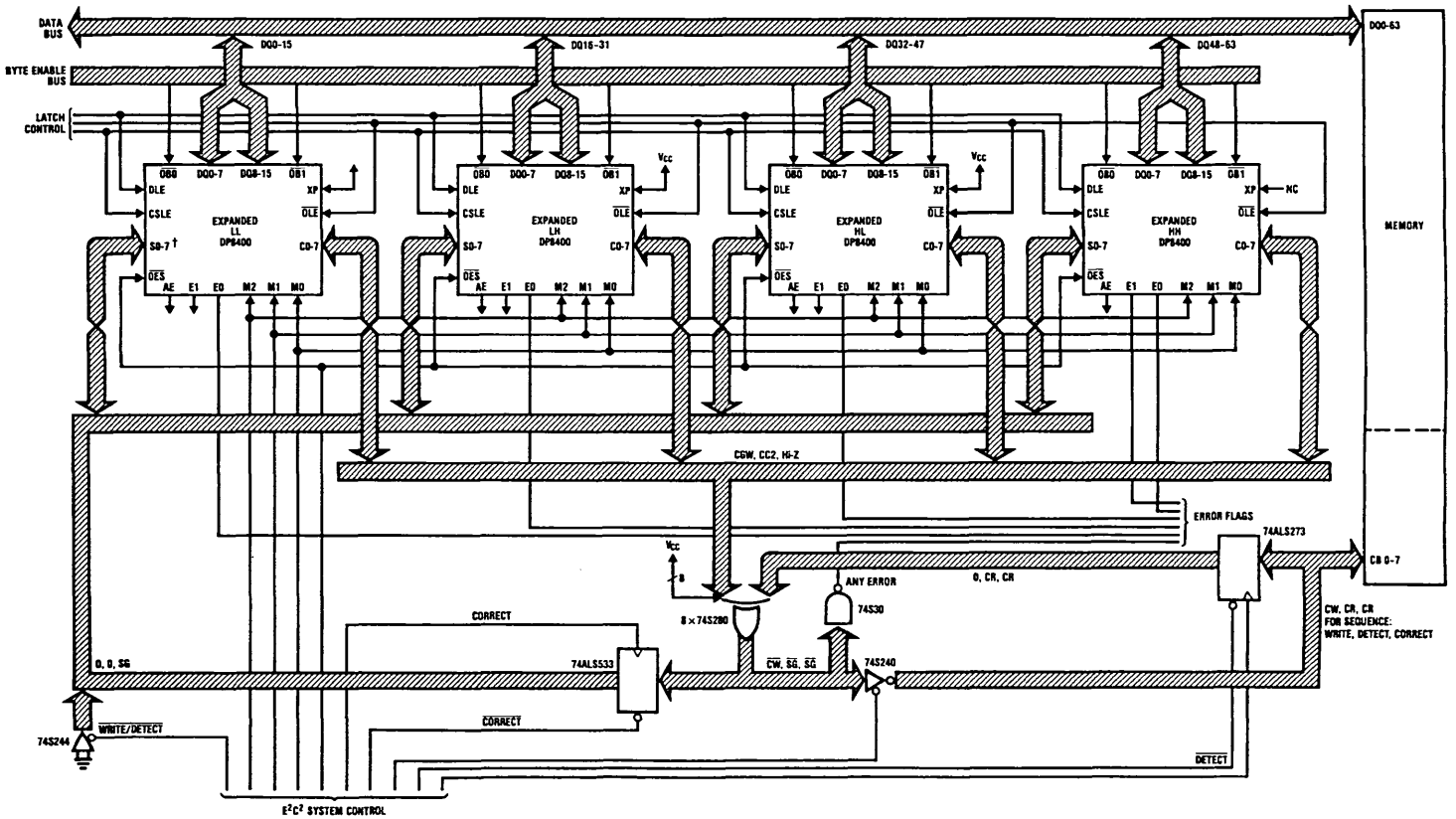

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FIGURE 7. Parallel Expansion (Fast 64-Bit Configuration)

Other Modes Of Operation

DOUBLE ERROR CORRECTION, USING THE DOUBLE-COMPLEMENT APPROACH

The DP8400-2 can be made to correct two errors, using no extra ICs or check bits, if at least one of the two errors detected is a hard error. This does require an extra memory WRITE and READ. Nevertheless, if a permanent failure exists, and an additional error occurs (creating two errors), both errors can be corrected, thereby saving a system crash.

Once a double error has been detected, the system puts the DP8400-2 in COMPLEMENT mode by setting M0 high. First a WRITE cycle is required and M2 is set low, putting the chip in mode 1, Table III, (COMPLEMENT WRITE), so that the contents of DIL are complemented into DOL, and the contents of CIL complemented into COL. $\overline{OB0}$ and $\overline{OB1}$ are set low so that complemented data and check bits can be written back to the same location of memory. Writing back complemented data to a location with a hard error forces the error to repeat itself. For example, if cell N of a particular location is jammed permanently high, and a low is written to it, a high will be read. However, when the data is complemented a low is again written, so that a high is read back for the second time. After a second READ (this second READ is a COMPLEMENT READ) of the location, data and check bits from the memory are recomplemented, so that bit N now contains a low. In other words, the error in bit N has corrected itself, while the other bits are true again. If there are two hard errors in a location, both are automatically corrected and the DP8400-2 detects no error on COMPLEMENT READ, as in *Figure 8a*. *Figure 8b* also shows that if one error is soft, the hard error will disappear on the second READ and the DP8400-2 corrects the soft error as a single-error. Therefore, in both cases, the DOL contains corrected data, ready to be enabled by $\overline{OB0}$ and $\overline{OB1}$. A WRITE to memory at this stage removes the complemented data written at the start of the sequence.

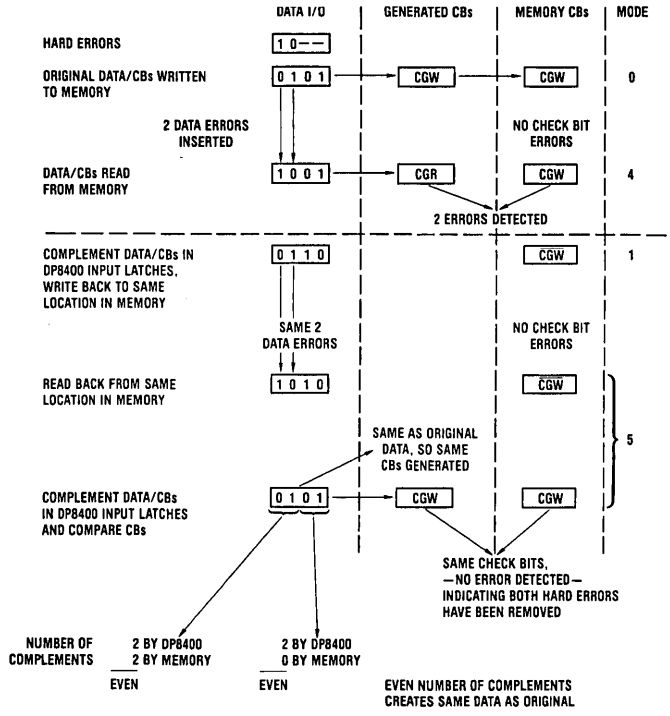

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FIGURE 8a. Double Error Correct Complement Hard Error Method — 2 Hard Errors In Data Bits

Other Modes of Operation (Continued)

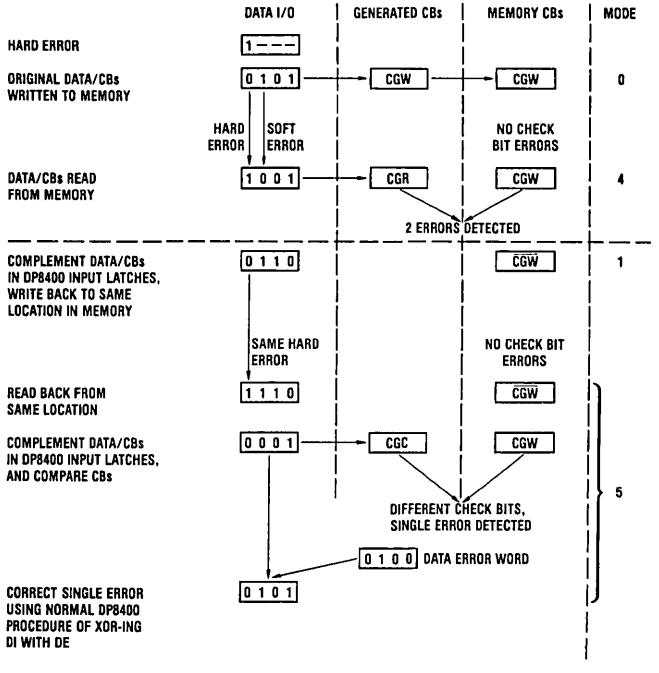

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FIGURE 8b. Double Error Correct Complement Hard Error Method — 1 Hard Error, 1 Soft Error In Data Bits

The examples shown in *Figures 8a* and *8b* are for 4 data bits. This approach will work for any number of data bits, but for simplicity these examples show how complementing twice corrects two errors in the data bits. The double COMPLEMENT approach also works for any two errors providing at least one is hard. In other words, one data-bit error and one check bit error, or two check bit errors are also corrected if one or both are hard. At the end of the COMPLEMENT READ cycle, the error flags indicate whether the data was correctable or not, as shown in Table XVII. If both the errors were soft, then the data was not correctable and the error flags indicate this.

This approach is ideal where double errors are rare but may occur. To avoid a system crash, a double-error detect now causes the system to enter a subroutine to set the DP8400-2 in COMPLEMENT mode. This method is also useful in bulk-memory applications, where RAMs are used with known cell failures, and is applicable in 16, 32, 48 or 64-bit configuration. In the 16-bit configuration, modes 1 and 5 of Table III are used. In the 32-bit expanded configuration, modes 1, 5 and 5 are used for the highest chip, and modes 3, 3 and 4 for the lower chip for WRITE, DETECT, and CORRECT. With the lower chip it is necessary to wrap around DOL (after latching its contents in mode 3), back to DIL and perform a Normal READ in mode 4 in the lower chip.

TABLE XVII. ERROR FLAGS AFTER COMPLEMENT READ (MODE 5)

AE	E1	E0	Error Type
0	0	0	Two hard errors
1	1	0	One hard error, one soft check bit error
1	1	1	One hard error, one soft data bit error
1	0	0	Two soft errors, not corrected

Other Modes of Operation (Continued)

DOUBLE-ERROR CORRECT WITH ERROR LOGGING

Figures 4 and *5* show the E²C² syndrome port connected to an error management unit (EMU). This scheme stores syndromes and the address of locations that fail, thereby logging the errors. Subsequent errors in a memory location that has already stored syndromes in the EMU, can then be removed by injecting the stored syndromes of the first error. To save the addresses and syndromes when power to the EMU is removed, it is necessary to be able to transfer information via the E²C² syndrome port to the processor data bus. This is also useful for logging the errors in the processor. Transfer in the opposite direction is also necessary.

DATA BUS TO SYNDROME BUS TRANSFER

This is necessary when transferring syndrome information to the error management unit, which is connected to the external syndrome bus. First, data to make CG = 0 (all data bits high) must be latched in DIL. Then in mode 2, data is fed to CIL, XOR-ed with 0, and output via SOL with $\overline{OES}$ low to the syndrome bus. Data is therefore fed directly from the system to the syndrome bus, and this cycle may be repeated as long as DLE is kept low, forcing CG to remain zero.

SYNDROME BUS TO DATA BUS TRANSFER

This is important when information in the error logger or error management unit has to be read. The DP8400-2 is set to mode 6B with $\overline{OES}$ high, and with $\overline{OB0}$, $\overline{OB1}$ and $\overline{OLE}$ low. If CSLE is high, the syndrome bus and check bit bus data appear on the lower and upper bytes of the data bus to be read by the system. Also E1 and E0 values that were valid when mode 6 was entered, appear on DQ7 and DQ15.

FULL DIAGNOSTIC CHECK OF MEMORY

Using mode 2, it is possible to transfer the upper byte of the data bus directly to the CIL, with CSLE high, without affecting DIL. These simulated check bits then appear on the check bit bus with $\overline{OLE}$ low, which also causes the previously latched contents of DIL to transfer to DOL. By enabling $\overline{OB0}$ and $\overline{OB1}$ data can be written to memory with the simulated check bits. A Normal READ cycle can then aid the system in determining that the memory bits are functioning correctly, since the processor knows the check bits and data it sent to the E²C². Another solution is to put the E²C² in mode 6 and read the memory check bits directly back to the processor.

SELF-TEST OF THE E²C² ON-CARD

Again using mode 2, data written from the processor data bus upper byte to CIL may be stored in CIL, by taking CSLE low. Next, a mode 0 WRITE can be performed and the user generated data can be latched in the DP8400-2 input latches (DLE held low). Now the user may perform a normal mode 4 READ. This will in effect be a Diagnostic READ of the user generated data and check bits without using the external memory. Thus by reading corrected data in mode 4, and by reading the generated syndromes, and error flags E0 and E1, the DP8400-2 can be tested completely on-card without involving memory.

MONITORING GENERATED SYNDROMES AND MEMORY CHECK BITS

Mode 6A enables SG0–SG6 onto DQ0–DQ6, and CIL0–CIL6 onto DQ8–DQ14, provided $\overline{OLE}$, $\overline{OB0}$ and $\overline{OB1}$ are low. Also the two error flags, E1 and E0 (latched from the previous READ mode), appear on DQ7 and DQ15. This may be used for checking the internal syndromes, for reading the memory check bits, or for diagnostics by checking the latched error flags.

CLEARING SIL

In the 16-bit only configuration, or the lower chip of expanded configurations, and in various modes of operation in the higher expanded chips, it is required that SIL be maintained at zero. At power-up initialization, both SIL and DIL are reset to all low. If $\overline{OES}$ is kept low, SIL will remain reset because CSLE is inhibited to SIL. Another method is to keep $\overline{OES}$ always high and the syndrome bus externally set low, or set low whenever CSLE can be used to clear SIL.

Mode 7A also forces the SIL to be cleared whenever CSLE occurs, and also these zero syndromes go to the internal syndrome bus SG. This puts the DP8400-2 in a PASS-THROUGH mode where the DIL contents pass to DOL and CIL contents to COL, if $\overline{OLE}$ is low.

POWER-UP INITIALIZATION OF MEMORY

Both SIL and DIL are reset low at power-up initialization. This facilitates writing all zeroes to the memory data bits to set up the memory. The check bits corresponding to all-zero data will appear on the check bit bus if the DP8400-2 is set to mode 0 and $\overline{OLE}$ is set low. All-zero data appears on the data bus when $\overline{OB0}$ and $\overline{OB1}$ are also set low. The system can now write zero-data and corresponding check bits to every memory location.

BYTE WRITING

Figure 14a shows the block diagram of a 16-bit memory correction system consisting of a DP8400-2 error correction chip and a DP8409A DRAM controller chip. There are 12 control signals associated with the interface. Six of the signals are standard DP8400-2 input signals, three are standard DP8409A input signals, and three are buffer control signals. The buffer control signals, $\overline{PBUF0}$ and $\overline{PBUF1}$, control when data words or bytes from the DP8400-2/memory data bus are gated to the processor bus and when data words or bytes from the processor are gated to the DP8400-2/memory data bus.

When the processor is reading or writing bytes to memory, words will always be read or written by the DP8400-2 and DP8409A error correction and DRAM controller section. The High Byte Enable and Address Data Bit Zero signals from the processor should control the byte transfers via the ocal bus transceiver signals $\overline{PBUF0}$ and $\overline{PBUF1}$. The buffer control signal, $\overline{DOUTB}$, controls when data from memory is gated onto the DP8400-2/memory data bus.

Figure 14b shows the timing relationships of the 12 control signals, along with the DP8400-2/memory data bus and some of the DRAM control signals ($\overline{RAS}$ and $\overline{CAS}$). RGCK is the $\overline{RAS}$ generator clock of the DP8409A which is used in Mode 1 (Auto Refresh mode), along with being the system clock.

Other Modes of Operation (Continued)

Having two separate byte enable pins, $\overline{OB0}$ and $\overline{OB1}$, it is easy to implement byte writing using the DP8400-2. First it is necessary to read from the location to which the byte is to be written. To do this the DP8400-2 is put in normal Read mode (Mode 4), which will detect and correct a single bit error. $\overline{WIN}$ is kept high and $\overline{RASIN}$ is pulled low, causing the DP8409A, now in Mode 5 (Auto Access mode), to start a read memory cycle. The data word and check bits from memory are then enabled onto the DP8400-2/memory data bus by pulling $\overline{DOUTB}$ low. The data and check bits are valid on the bus after the $\overline{RASIN}$ to $\overline{CAS}$ time (t_{RAC}) plus the column access time (t_{CAC}) of the particular memories used. DLE, CSLE can then be pulled low in order to latch the memory data into the input latches of the DP8400-2. $\overline{OLE}$ can be pulled low to enable the corrected memory word, or the original memory word if no error was present, into the data output latches. Following this, $\overline{DOUTB}$ can be pulled high to disable the memory data from the DP8400-2/memory data bus. The corrected memory word will be available at the data output latches "t_{DCD16}" after the memory word was available at the data input latches. Once the corrected data is available at the output latches $\overline{OLE}$ can be pulled high to latch the corrected data. Also DLE and CSLE can be pulled high in order to enable the input data latches again.

Now the DP8400-2 can be put into a write cycle (Mode 0 = M2 = Low). At this time the byte to be written to memory and the other byte from memory can be enabled onto the DP8400-2/memory data bus ($\overline{OB0}$, $\overline{PBUF1}$ or $\overline{OB1}$, $\overline{PBUF0}$ go low). DLE, CSLE can now transition low to latch the new memory word into the data input latch. $\overline{OLE}$ is pulled low to enable the output latches. When the new checkbits are valid, t_{DCB16} after the data word is valid on the DP8400-2/memory data bus, $\overline{OLE}$ and $\overline{DLE}$ can be pulled high to latch the new memory word into the output latches, and then $\overline{WIN}$ can be pulled low to write the data into memory. $\overline{RASIN}$ should be held low long enough to cause the new data and check bits to be stored into memory ($\overline{WIN}$ data hold time).

Also a READ-MODIFY-WRITE cycle was performed, taking approximately 40% longer than a normal memory WRITE cycle. A READ and then a WRITE memory cycle could have been used in the above example but it would have taken longer.

Buffers are used in this system (74ALS244) to keep the Data Out and Data In of the memory IC's from conflicting with each other during Read-Modify-Write cycles.

A byte READ from memory is no different from a normal READ. This approach may be used for a 16-bit processor using byte writing, or an 8-bit processor using a 16-bit memory to reduce the memory percentage of check bits, or with memory word sizes greater than two bytes.

An APP NOTE (App Note 387) has been written detailing an Error Correcting Memory System using the DP8409A or DP8419 (Dynamic RAM Controller) and the DP8400-2 interfaced to a National Semiconductor Series 32000 CPU. See this App Note for further system details and considerations.

BEYOND SINGLE-ERROR CORRECT

With the advent of larger semiconductor memories, the frequency of the soft errors will increase. Also some memory system designers may prefer to buy less expensive memories with known cell, row or column failures, thus, more hard errors. All this means that double-error correct, triple-error detect capability, and beyond will become increasingly important. The DP8400-2 can correct two errors, provided one or both are hard errors, with no extra components, using the double complement approach. There are two other approaches to enhance reliability and integrity. One is to use the error management unit to log errors using the syndrome bus, and then to output these syndromes, when required, back to the DP8400-2.

DOUBLE SYNDROME DECODING

The other approach takes advantage of the Rotational Syndrome Word Generator matrix. This matrix is an improvement of the Modified Hamming-code, so that if, on a second DP8400-2, the data bus is shifted or rotated by one bit, and 2 errors occur, the syndromes for this second chip will be different from the first for any 2 bits in error. Both chips together output a unique set of syndromes for any 2 bits in error. This can be decoded to correct any 2-bit error. This is not possible with other Modified Hamming-code matrices.

Absolute Maximum Ratings (Note 1)

Storage Temperature Range	−65°C to +150°C
Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Sink Current	50 mA
Maximum Power Dissipation at 25°C	
Molded Package	3269 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 26.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C

Electrical Characteristics (Note 2) V_{CC} = 5V ±5%, T_A = 0°C to 70°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_C = −18 mA		−0.8	−1.5	V
I_{IH}	Input High Current	V_{IN} = 2.7V		1	160	μA
I_{IH} (XP)	Input High Current	V_{CC} = Max, XP = 5.25V		2.5	4.5	mA
I_{IL} (XP)	Input Low Current	V_{CC} = Max, XP = 0V		−2.5	−4.5	mA
I_{IL} (BP0/C7)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−100.0	−500	μA
I_{IL} (BP1/S7)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−100.0	−500	μA
I_{IL} (CSLE)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−150.0	−750	μA
I_{IL} (DLE)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−200.0	−1000	μA
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−50.0	−250	μA
I_I	Input High Current (Max)	V_{IN} = 5.5V (Except XP Pin)			1.0	mA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA (Except BP0, BP1) I_{OL} = 4 mA (BP0, BP1 Only)		0.3 0.3	0.5 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = −100 μA I_{OH} = −1 mA	2.7 2.4	3.2 3.0		V V
I_{OS}	Output Short Current (Note 3)	V_{CC} = Max		−150	−250	mA
I_{CC}	Supply Current	V_{CC} = Max		220	300	mA
C_{IN} (I/O)	Input Capacitance All Bidirectional Pins	Note 4		8.0		pF
C_{IN}	Input Capacitance All Unidirectional Input Pins	Note 4		5.0		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V

Note 3: Only one output at a time should be shorted.

Note 4: Input capacitance is guaranteed by periodic testing. F test = 10 kHz at 300 mV, T_A = 25°C.

Note 5: All switching parameters measured from 1.5V of input to 1.5V of output. Input pulse amplitude 0V to 3V, $t_r = t_f$ = 2.5 ns.

DP8400-2 Switching Characteristics (Note 5)

V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C, C_L = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DCB16}	Data Input Valid to Check Bit Valid	*Figure 9b*		29	40	ns
t_{DEV16}	Data Input to Any Error Valid	*Figures 10b, 11b*		21	31	ns
t_{DCD16}	Data Input Valid to Corrected Data Valid	*Figure 10b*, $\overline{OB0}$, $\overline{OB1}$ Low		44	61	ns
t_{DSI}	Data Input Set-Up Time Before DLE, CSLE H to L	*Figures 10b, 13d*	10	5		ns
t_{DHI}	Data Input Hold Time After DLE, CSLE H to L	*Figures 10b, 13d*	10	5		ns
t_{DSO}	Data Input Set-Up Time Before $\overline{OLE}$ L to H	*Figure 10b*	10	5		ns
t_{DHO}	Data Input Hold Time After $\overline{OLE}$ L to H	*Figure 10b*	10	5		ns
t_{DE0}	Data in Valid to E0 Valid	*Figures 9b, 10b, 13d*		36	55	ns
t_{DE1}	Data in Valid to E1 Valid	*Figures 9b, 10b, 13d*		43	55	ns
t_{IEV}	DLE, CSLE High to Any Error Flag Valid (Input Data Previously Valid)	*Figure 10b*		28	45	ns
t_{IEX}	DLE, CSLE High to Any Error Flag Invalid	*Figures 9b, 10b*		38	60	ns
t_{ILE}	DLE, CSLE High Width to Guarantee Valid Data Latched	*Figures 10b, 13d*	20			ns
t_{OLE}	$\overline{OLE}$ Low Width to Guarantee Valid Data Latched	*Figure 13d*	20			ns
t_{ZH}	High Impedance to Logic 1 from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$ M2 H to L	*Figures 9b, 10b, 13d*		22	36	ns
t_{HZ}	Logic 1 to High Impedance from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$, M2 L to H	*Figures 9b, 10b, 13d,*		38	55	ns
t_{ZL}	High Impedance to Logic 0 from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$ M2 H to L	*Figures 9b, 10b, 13d*		19	35	ns
t_{LZ}	Logic 0 to High Impedance from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$, M2 H to L	*Figures 9b, 10b, 13d*		15	25	ns
t_{PPE}	Byte Parity Input Valid to Parity Error Flags Valid	*Figure 9b*		16	27	ns
t_{DPE}	Data In Valid to Parity Error Flags Valid	*Figures 9b, 13d*		27	55	ns
t_{DCP}	Data in Valid to Corrected Byte Parity Output Valid	*Figure 9b*		44	61	ns

DP8400-2 Switching Characteristics (Continued) (Note 5)

V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C, C_L = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{NMR}	New Mode Recognize Time	*Figure 10b*		22	35	ns
t_{CDV}	Mode Valid to Complement Data Valid	*Figure 11b*		34	50	ns
t_{CCV}	Mode Valid to Complement Check Bit Valid	*Figure 11b*		30	45	ns
t_{SCB}	Syndrome Input Valid to Check Bit Valid	*Figure 13d*		20	35	ns
t_{SEV}	Syndrome Input Valid (CGL) to Any Error Valid	*Figure 13d*		17	27	ns
t_{SCD}	Syndrome Inputs Valid to Corrected Data Valid	*Figure 13d*		35	50	ns
t_{DSB}	Data Input Valid to Syndrome Bus Valid	*Figure 13d*, $\overline{OES}$ Low		28	46	ns
t_{CSB}	Check Bit Inputs Valid to Syndrome Bus Valid	*Figure 13d*, $\overline{OES}$ Low		19	32	ns
t_{CEV}	Check Bit Inputs Valid (PSH) to Any Error Valid	*Figure 13d*		17	30	ns
t_{CCD}	Check Bit Input Valid (PSH) to Corrected Data Valid	*Figure 13d*		30	45	ns
t_{DCB32}	Data Input Valid to Check Bit Valid	*Figure 13d*		49	75	ns
t_{DEV32}	Data Input Valid to Any Error Valid	*Figure 13d*		46	67	ns
t_{DCD32}	Data Input Valid to Corrected Data Out	*Figure 13d*, $\overline{OB0}$, $\overline{OB1}$ Low		84	110	ns

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

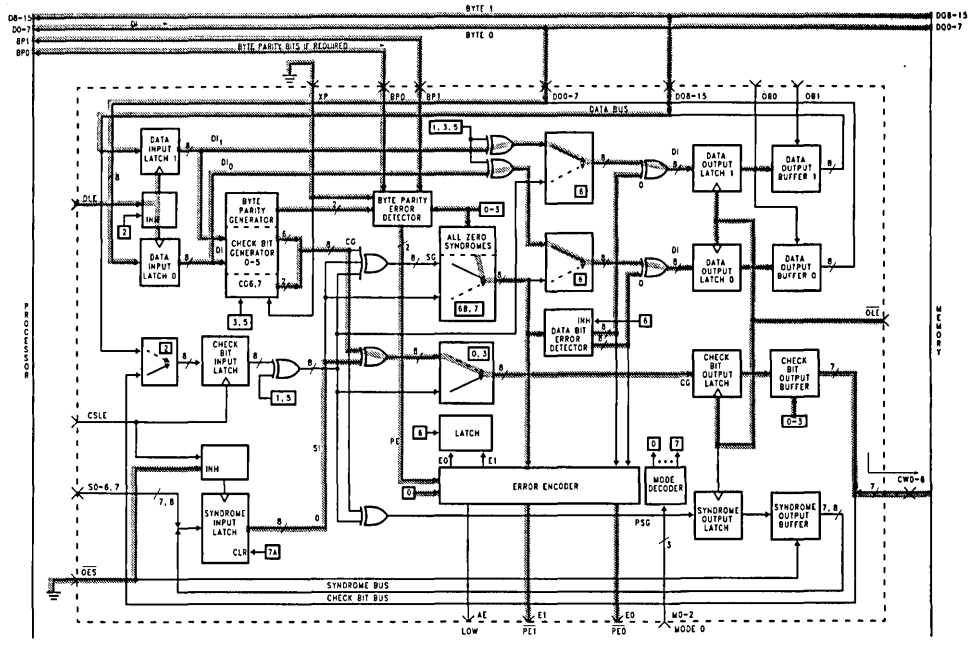
Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: Only one output at a time should be shorted.

Note 4: Input capacitance is guaranteed by periodic testing. F test = 10 kHz at 300 mV, $T_A = 25°C$.

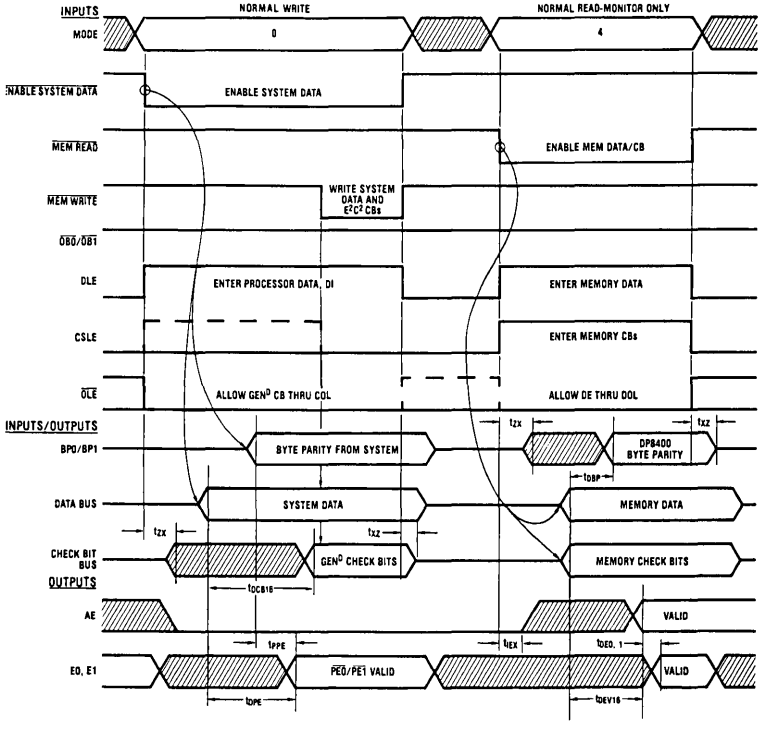
Note 5: All switching parameters measured from 1.5V of input to 1.5V of output. Input pulse amplitude 0V to 3V, $t_r = t_f = 2.5$ ns.

Typical Applications



TL/F/6899–17

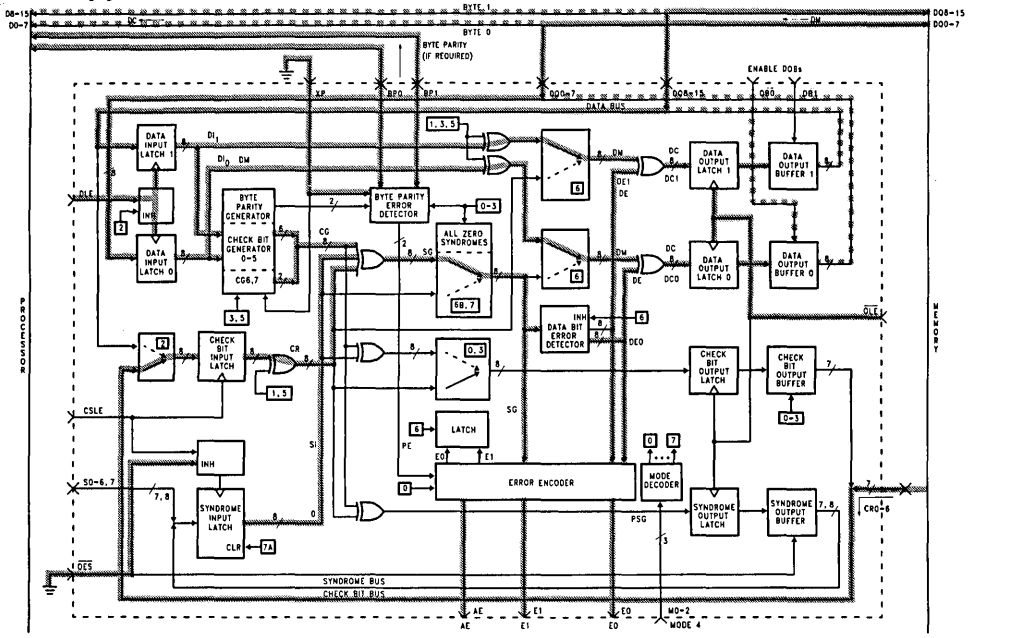
FIGURE 9a. DP8400-2 16-Bit Configuration, Normal WRITE with Byte Parity Error Detect If Required



TL/F/6899–18

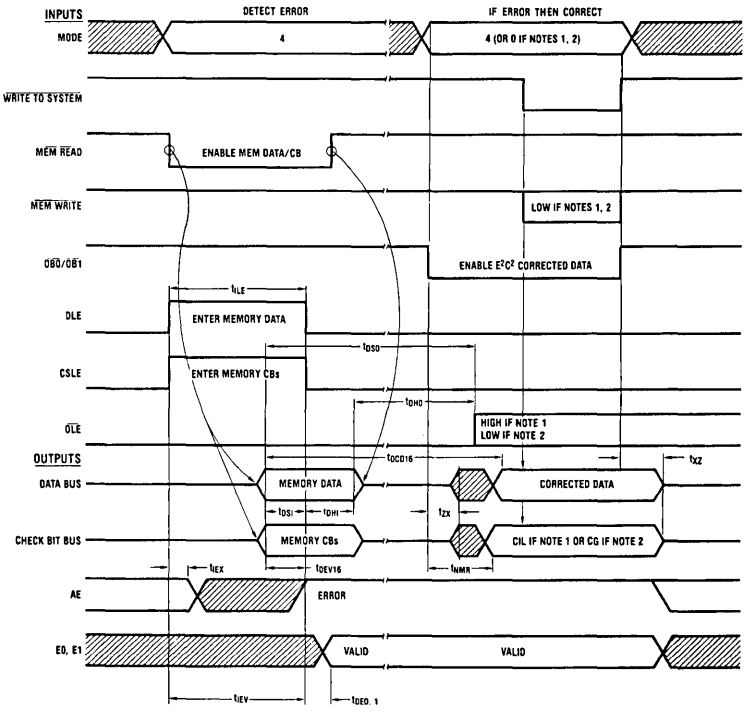
FIGURE 9b. DP8400-2 16-Bit Configuration, Normal WRITE and Normal READ Timing Diagram

Typical Applications (Continued)



TL/F/6899-19

FIGURE 10a. DP8400-2 16-Bit Configuration, Normal READ — Detect Error (And Correct if Required---)



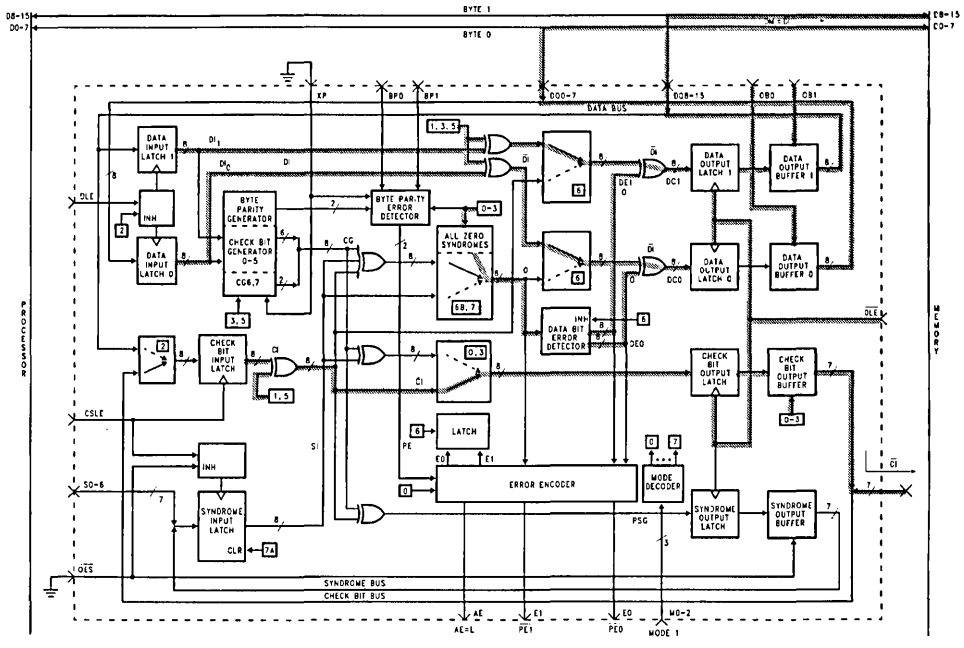
TL/F/6899-20

Note 1: If rewriting correct data and CBs to same location and single data error was detected.

Note 2: If rewriting correct data and CBs to same location and single check bit was detected.

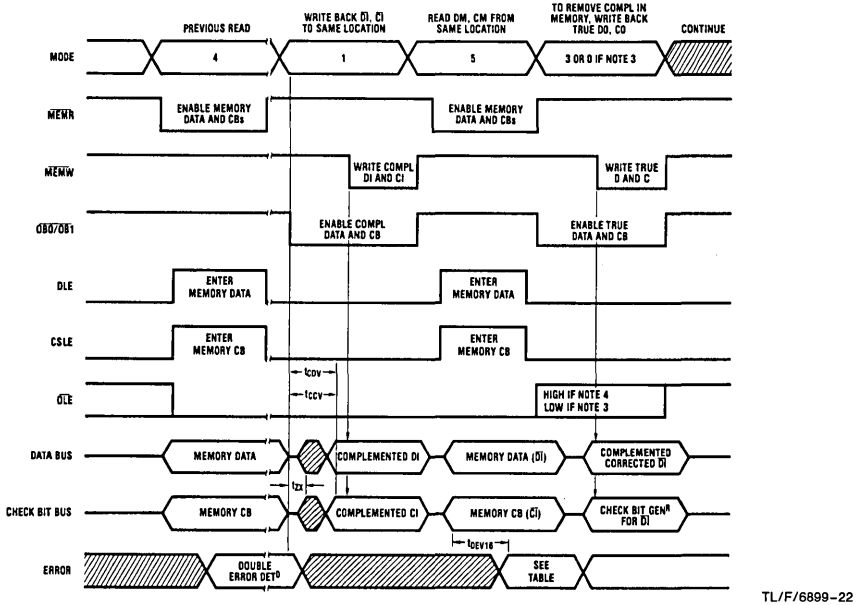
FIGURE 10b. DP8400-2 16-Bit Configuration, DETECT THEN CORRECT Timing Diagram

Typical Applications (Continued)



TL/F/6899-21

FIGURE 11a. DP8400-2 16-Bit Configuration, COMPLEMENT WRITE



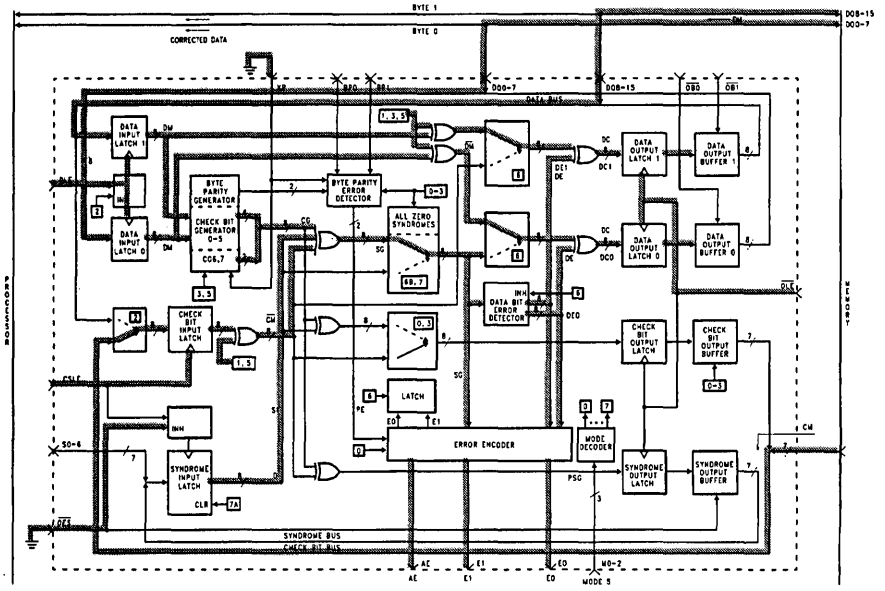
TL/F/6899-22

Note 3: If rewriting corrected data and CBs back to same location and 1 soft data bit error was detected.

Note 4: If rewriting corrected data and CBs back to same location and 2 hard errors or 1 soft check bit was detected.

FIGURE 11b. DP8400-2 16-Bit Configuration, Detect 2 Errors, COMPLEMENT WRITE, COMPLEMENT READ, Output Corrected Data Timing Diagram

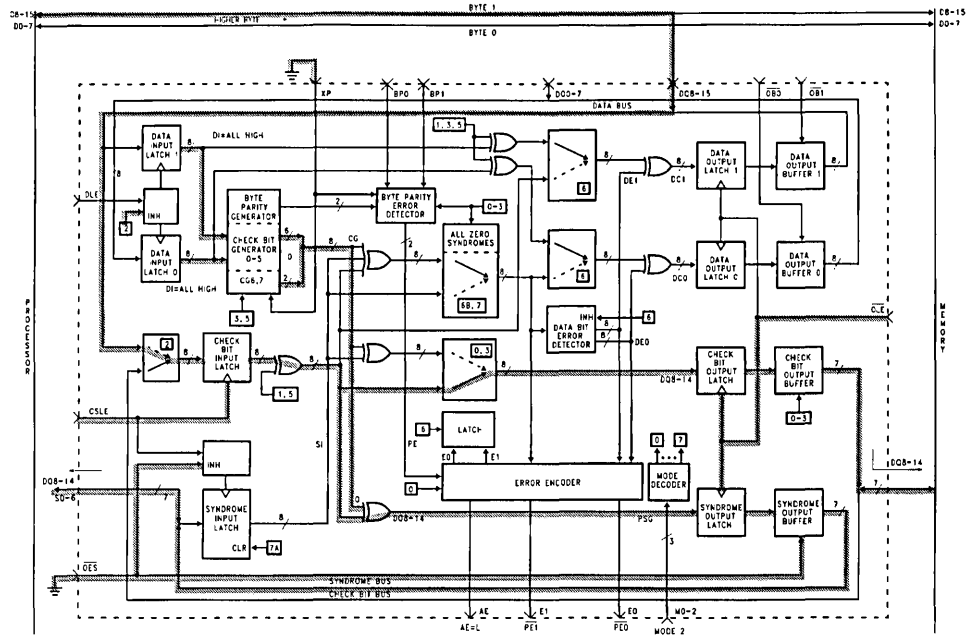
Typical Applications (Continued)



TL/F/6899–23

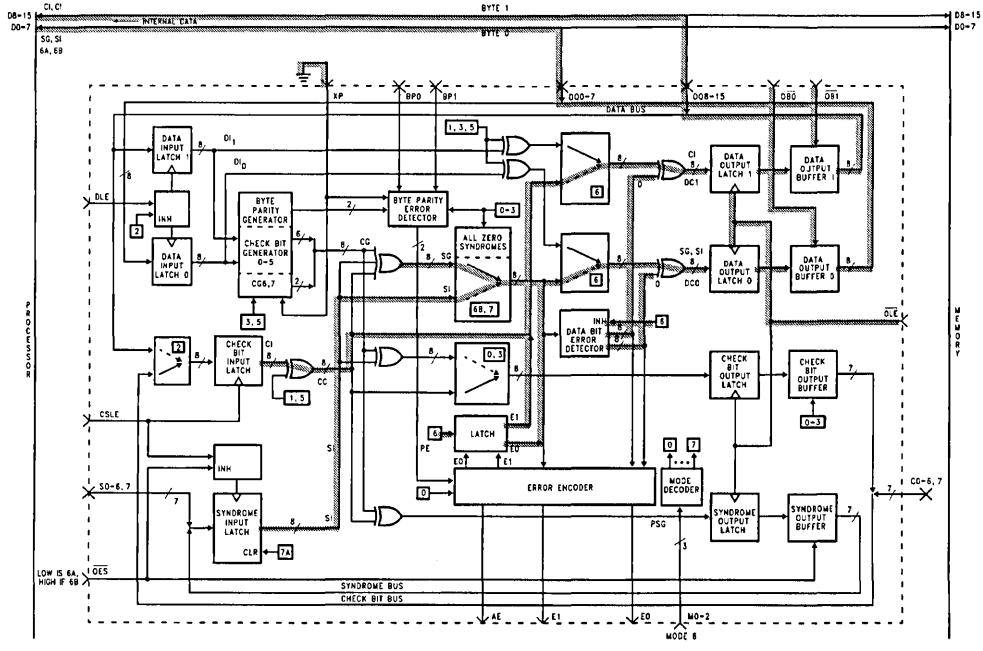
FIGURE 11c. DP8400-2 16-Bit Configuration, COMPLEMENT READ and Output Corrected if One or Two Hard Errors

Typical Applications (Continued)



TL/F/6899–24

FIGURE 12a. DP8400-2 16-Bit Configuration, Diagnostic WRITE, READ. Data Bus to Check Bit Bus or Syndrome Bus (Providing DI = HIGH in Previous Cycle to Set CG = All Zero For Transfer to S)



TL/F/6899–25

FIGURE 12b. DP8400-2 16-Bit Configuration, Monitor on Data Bus — Memory Check Bits

Typical Applications (Continued)

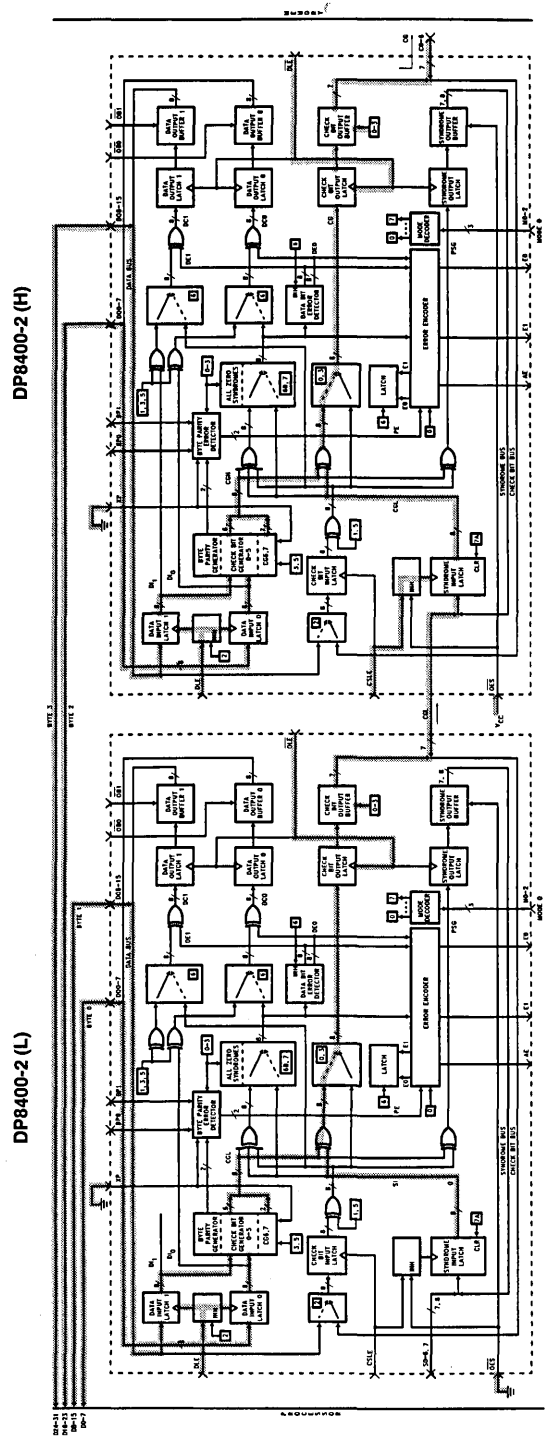


FIGURE 13a. DP8400-2 32-Bit Configuration, WRITE

TL/F/6899–26

Typical Applications (Continued)

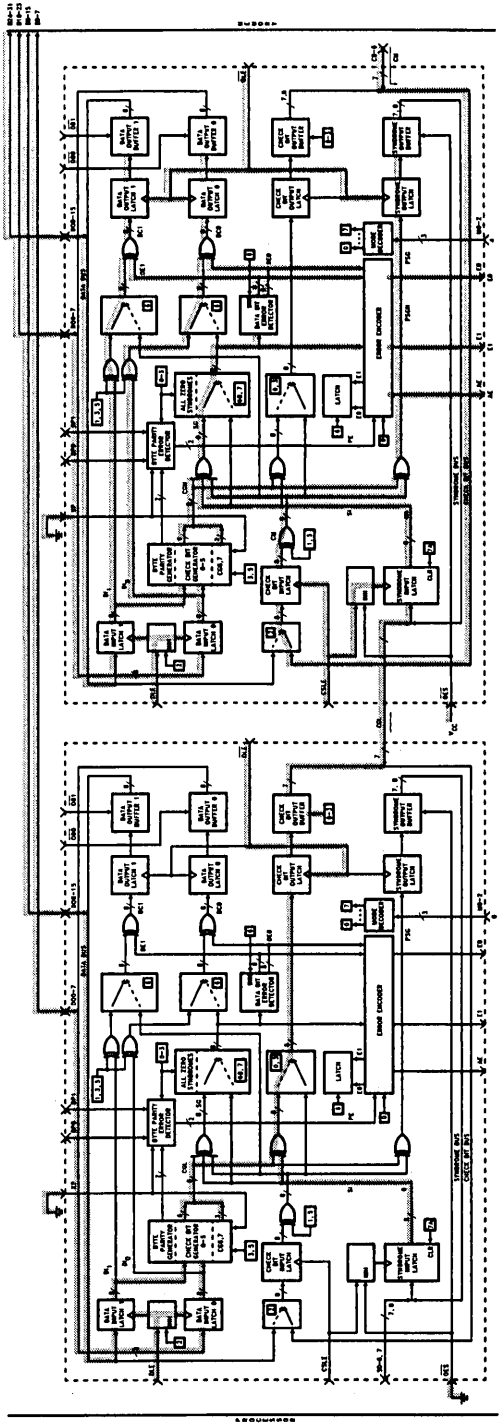


FIGURE 13b. DP8400-2 32-Bit Configuration, READ Detect Error Only

TL/F/6899–27

Typical Applications (Continued)

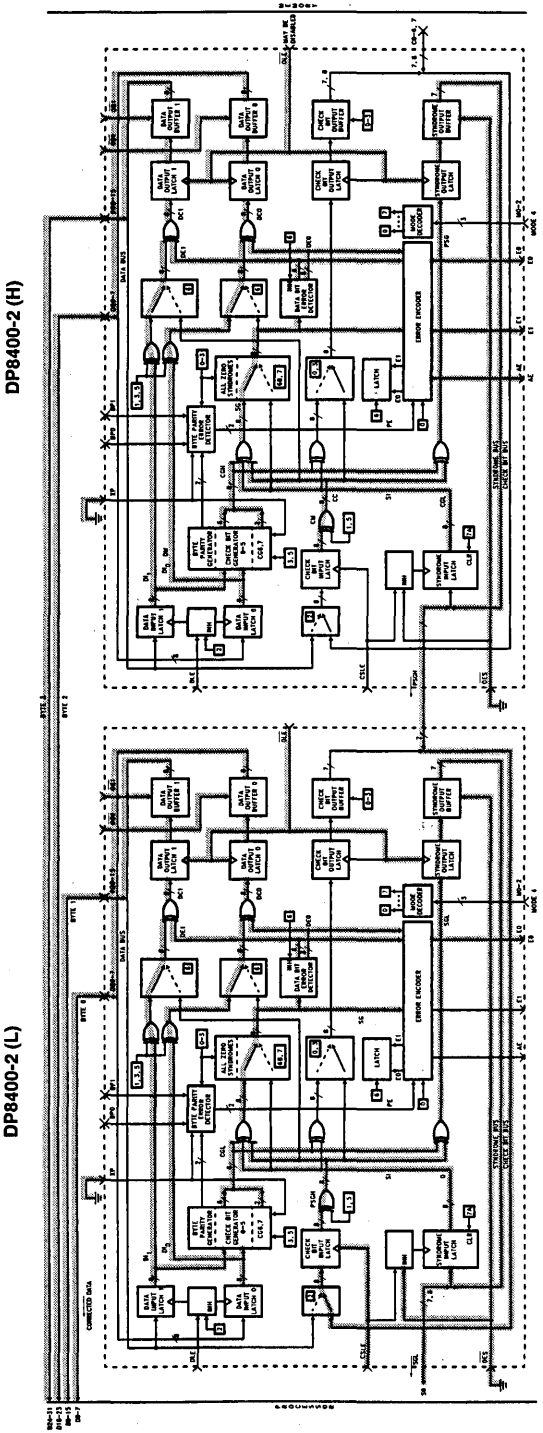
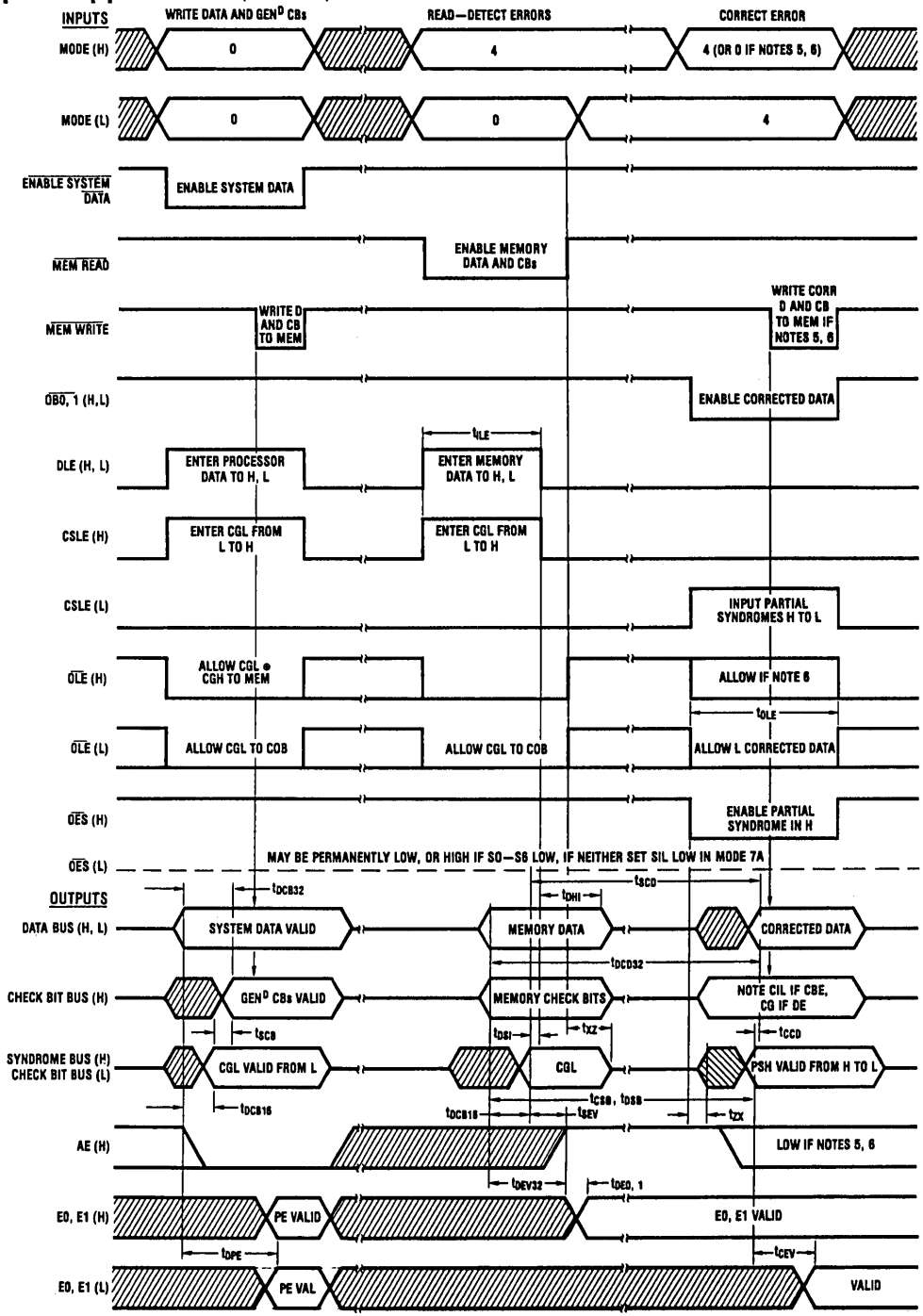


FIGURE 13c. DP8400-2 32-Bit Configuration, READ Correct Data

TL/F/6899–28

Typical Applications (Continued)

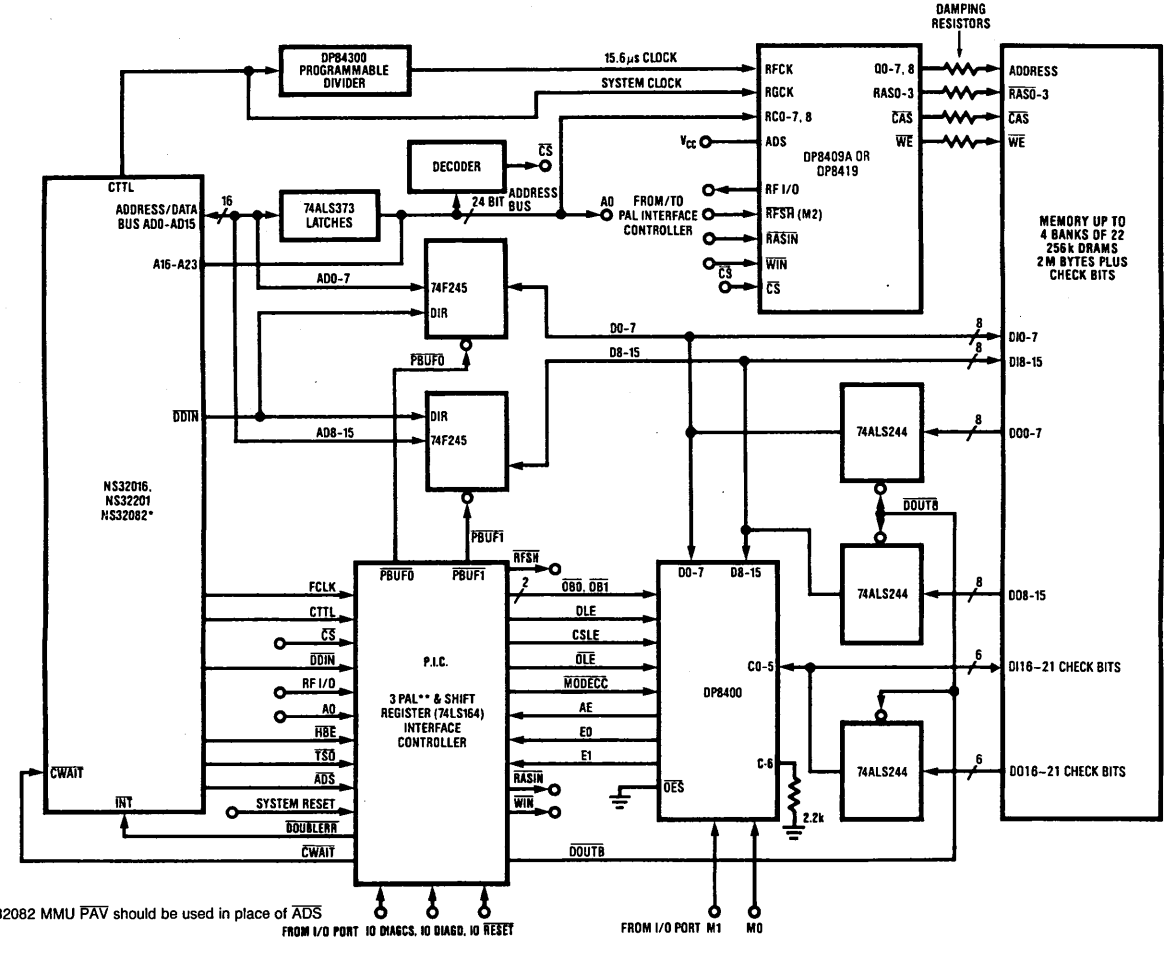


Note 5: If rewriting corrected data and CBs back to same location and single data error was detected. TL/F/6899–29

Note 6: If rewriting corrected data and CBs back to same location and single check bit error was detected.

FIGURE 13d. DP8400-2 32-Bit Configuration, WRITE, DETECT and CORRECT Timing Diagram

NS32016, DP8400-2, DP8409A or DP8419 Error Correcting Memory System

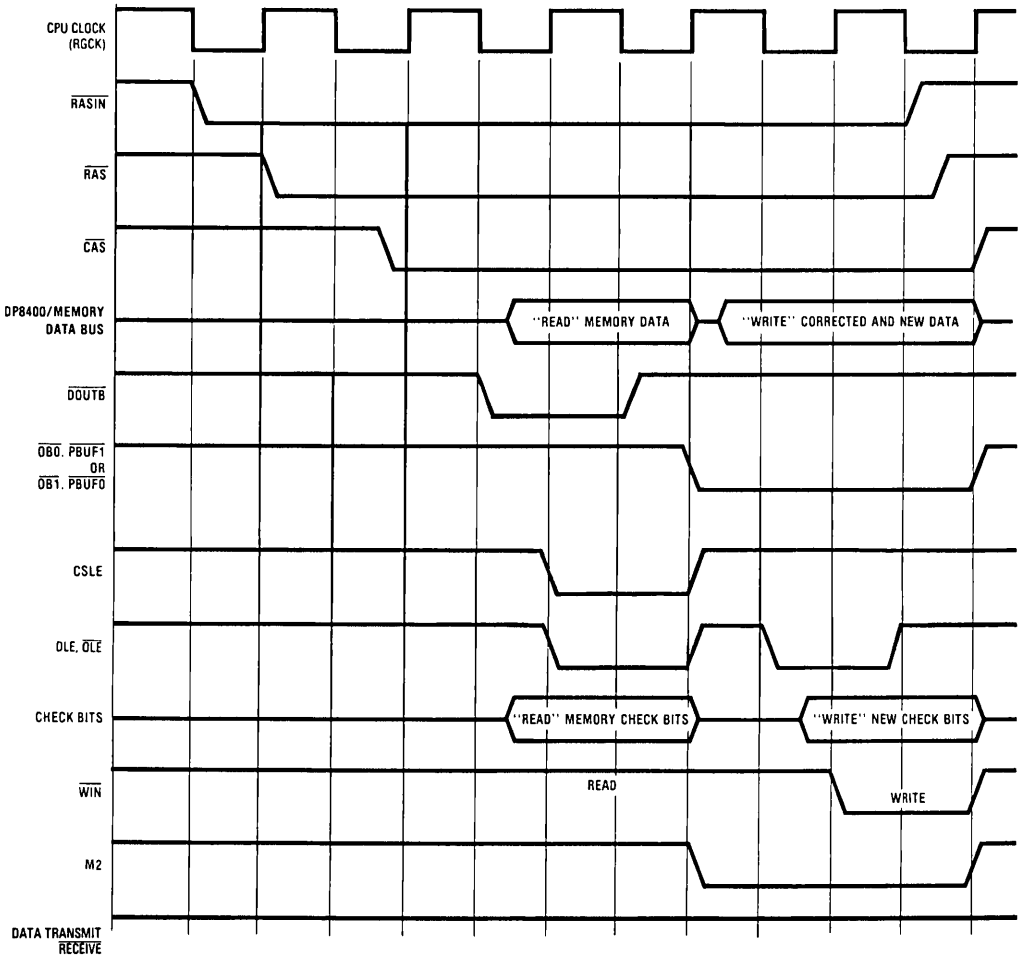


IF system contains NS32082 MMU $\overline{PAV}$ should be used in place of $\overline{ADS}$

TL/F/6899–30

FIGURE 14a. DP8400-2/8409A System Interface Block Diagram (See Figure 14b for Byte Write Control Timing)

Typical Applications (Continued)



TL/F/6899–31

FIGURE 14b. DP8400-2 16-Bit Configuration, Byte Write Timing

Typical Applications (Continued)

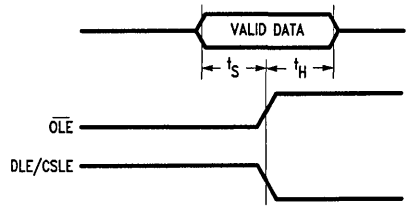


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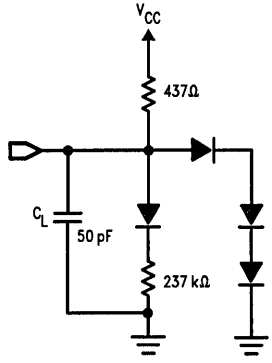
FIGURE 15. Timing Waveform for Set-Up and Hold Time



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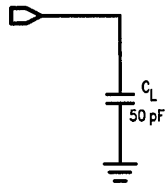
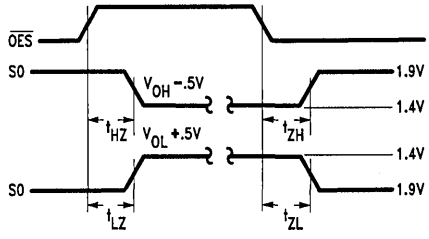
(a) TRI-STATE LOAD



TL/F/6899–34

(b) TEST LOAD

FIGURE 16. Loading Circuit



TL/F/6899–35

FIGURE 17. TRI-STATE Measurement

National Semiconductor Corporation

PRELIMINARY

DP8402A/DP8403/DP8404/DP8405 32-Bit Parallel Error Detection and Correction Circuits (EDAC's)

General Description

The DP8402A, DP8403, DP8404 and DP8405 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin DP8402A and DP8403 or 48-pin DP8404 and DP8405 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Double bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

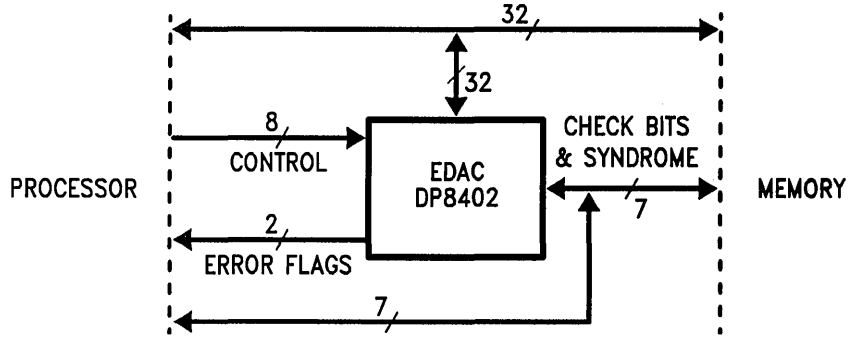
Read-modify-write (byte-control) operations can be performed with the DP8402A and DP8403 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

Features

- Detects and corrects single-bit errors
- Detects and flags double-bit errors
- Built-in diagnostic capability
- Fast write and read cycle processing times
- Byte-write capability . . . DP8402A and DP8403
- Fully pin and function compatible with TI's SN74ALS632A thru SN74ALS635 series

System Environment



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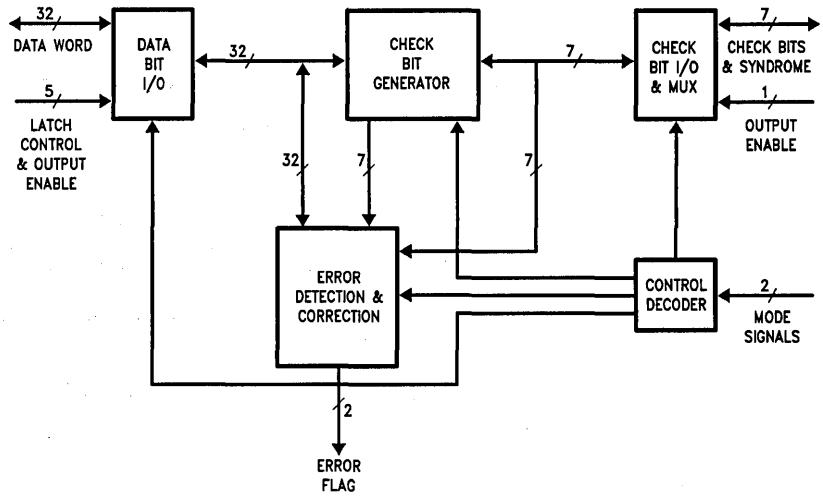
2

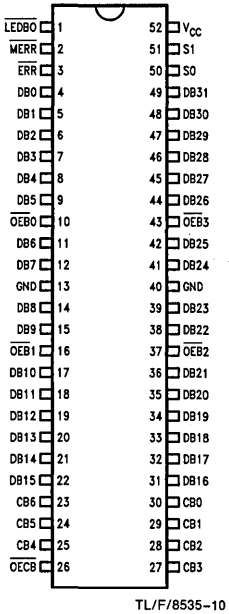
Simplified Functional Block and Connection Diagrams



TL/F/8535–2

Device	Package	Byte-Write	Output
DP8402A	52-pin	yes	TRI-STATE®
DP8403	52-pin	yes	Open-Collector
DP8404	48-pin	no	TRI-STATE
DP8405	48-pin	no	Open-Collector

Dual-In-Line Packages



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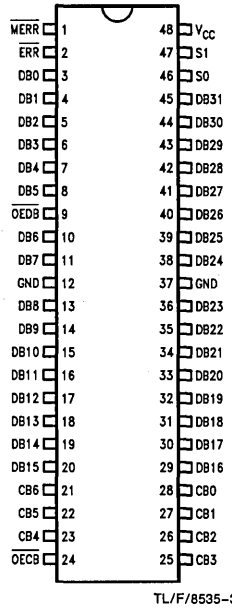
Top View

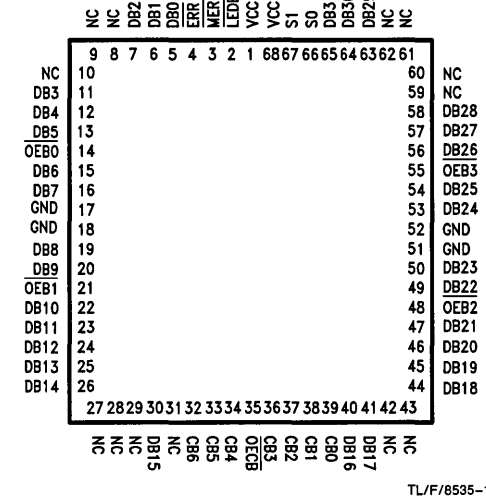


TL/F/8535–3

Top View

Order Number DP8402AD, DP8403D, DP8404D or DP8405D
See NS Package Number D48A or D52A

Plastic Chip Carrier



TL/F/8535–11

Top View

Order Number DP8402AV
See NS Package Number V68A

Mode Definitions

MODE	PIN NAME S1	S0	DESCRIPTION MODE	OPERATION
0	L	L	WRITE	Input dataword and output checkword
1	L	H	DIAGNOSTICS	Input various data words against latched checkword/output valid error flags.
2	H	L	READ & FLAG	Input dataword and output error flags
3	H	H	CORRECT	Latched input data and checkword/output corrected data and syndrome code

Pin Definitions

S0, S1	Control of EDAC mode, see preceding Mode Definitions
DB0 thru DB31	I/O port for 32 bit dataword.
CB0 thru CB6	I/O port for 7 bit checkword. Also output port for the syndrome error code during error correction mode.
$\overline{OEB0}$ thru $\overline{OEB3}$ (DP8402A, DP8403)	Dataword output buffer enable. When high, output buffers are at TRI-STATE. Each pin controls 8 I/O ports. $\overline{OEB0}$ controls DB0 thru DB7, $\overline{OEB1}$ controls DB8 thru DB15, $\overline{OEB2}$ controls DB16 thru DB23 and $\overline{OEB3}$ controls DB24 thru DB31.
$\overline{LEDBO}$ (DP8402A, DP8403)	Data word output Latch enable. When high it inhibits input to the Latch. Operates on all 32 bits of the dataword.
$\overline{OEDB}$ (DP8404, DP8405)	TRI-STATE control for the data I/O port. When high output buffers are at TRI-STATE.
$\overline{OECB}$	Checkword output buffer enable. When high the output buffers are in TRI-STATE mode.
$\overline{ERR}$	Single error output flag, a low indicates at least a single bit error.
$\overline{MERR}$	Multiple error output flag, a low indicates two or more errors present.

PCC Pin Definitions DP8402A

pin		pin	
1	V_{CC}	35	$\overline{OECB}$
2	$\overline{LEDBO}$	36	CB3
3	$\overline{MERR}$	37	CB2
4	$\overline{ERR}$	38	CB1
5	DB0	39	CB0
6	DB1	40	DB16
7	DB2	41	DB17
8	NC	42	NC
9	NC	43	NC
10	NC	44	DB18
11	DB3	45	DB19
12	DB4	46	DB20
13	DB5	47	DB21
14	$\overline{OEBO}$	48	$\overline{OEB2}$
15	DB6	49	DB22
16	DB7	50	DB23
17	GND	51	GND
18	GND	52	GND
19	DB8	53	DB24
20	DB9	54	DB25
21	$\overline{OEB1}$	55	$\overline{OEB3}$
22	DB10	56	DB26
23	DB11	57	DB27
24	DB12	58	DB28
25	DB13	59	NC
26	DB14	60	NC
27	NC	61	NC
28	NC	62	NC
29	NC	63	DB29
30	DB15	64	DB30
31	NC	65	DB31
32	CB6	66	S0
33	CB5	67	S1
34	CB4	68	V_{CC}

TABLE I. Write Control Function

Memory Cycle	EDAC Function	Control S1	S0	Data I/O	DB Control $\overline{OEBn}$ or $\overline{OEDB}$	DB Output Latch DP8402A, DP8403 $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	$\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table II for details on check bit generation.

Memory Write Cycle Details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.

2

TABLE II. Parity Algorithm

Check Word Bit	32-Bit Data Word																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X			X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X		X	X	X		X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X			X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

Memory Read Cycle (Error Detection & Correction Details)

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from the memory is acceptable to use as presented on the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table III represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

TABLE III. Error Function

Total Number of Errors		Error Flags		Data Correction
32-Bit Data Word	7-Bit Check Word	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

The DP8402 check bit syndrome matrix can be seen in TABLE II. The horizontal rows of this matrix generate the check bits by selecting different combinations of data bits, indicated by "X"s in the matrix, and generating parity from them. For instance, parity check bit "0" is generated by EXCLUSIVE NORing the following data bits together; 31, 29, 28, 26, 21, 19, 18, 17, 14, 11, 9, 8, 7, 6, 4, and 0.

During a WRITE operation (mode 0) the data enters the DP8402 and check bits are generated at the check bit input/output port. Both the data word and the check bits are then written to memory.

During a READ operation (mode 2, error detection) the data and check bits that were stored in memory, now possibly in error, are input through the data and check bit I/O ports. New check bits are internally generated from the data word. These new check bits are then compared, by an EXCLUSIVE NOR operation, with the original check bits that were stored in memory. The EXCLUSIVE NOR of the original check bits, that were stored in memory, with the new check bits is called the syndrome word. If the original check bits are the same as the new check bits, a no error condition, then a syndrome word of all ones is produced and both error flags ($\overline{ERR}$ and $\overline{MERR}$) will be high. The DP8402 matrix encodes errors as follows:

TABLE IV. Read, Flag, and Correct Function

Memory Cycle	EDAC Function	Control S1	Control S0	Data I/O	DB Control $\overline{OEBn}$ or $\overline{OEDB}$	DB Output Latch DP8402A, DP8403 $\overline{LEDBO}$	Check I/O	CB Control $\overline{OECB}$	Error Flags $\overline{ERR}$	Error Flags $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†	
Read	Latch input data and check bits	H	H	Input data latched	H	L	Input check word latched	H	Enabled†	
Read	Output corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†	

†See Table III for error description.

‡See Table V for error location.

Memory Read Cycle (Error Detection & Correction Details) (Continued)

1) Single data bit errors cause 3 or 5 bits in the syndrome word to go low. The columns of the check bit syndrome matrix (TABLE II) are the syndrome words for all single bit data errors in the 32 bit word (also see TABLE V). The data bit in error corresponds to the column in the check bit syndrome matrix that matches the syndrome word. For instance, the syndrome word indicating that data bit 31 is in error would be (CB6-CB0) = "0001010", see the column for data bit 31 in TABLE II, or see TABLE V. During mode 3 (S0 = S1 = 1) the syndrome word is decoded, during single data bit errors, and used to invert the bit in error thus correcting the data word. The corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents the 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip.

2) A single check bit error will cause that particular check bit to go low in the syndrome word.

3) A double bit error will cause an even number of bits in the syndrome word to go low. The syndrome word will then be the EXCLUSIVE NOR of the two individual syndrome words corresponding to the 2 bits in error. The two-bit error is not correctable since the parity tree can only identify single bit errors.

If any of the bits in the syndrome word are low the "$\overline{ERR}$" flag goes low. The "$\overline{MERR}$" (dual error) flag goes low during any double bit error conditions. (See Table III).

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE V. Syndrome Decoding

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

Syndrome Bits							Error
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	2-bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB15
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

Syndrome Bits							Error
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X = error in check bit X

DB Y = error in data bit Y

2-bit = double-bit error

unc = uncorrectable multibit error

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TABLE VI. Read-Modify-Write Function

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S0	BYTEn†	$\overline{OEB}$n†	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL	ERROR FLAG $\overline{ERR}$ $\overline{MERR}$
Read	Read & Flag	H	L	Input	H	X	Input	H	Enabled
Read	Latch input data & check bits	H	H	Input data latched	H	L	Input check word latched	H	Enabled
Read	Latch corrected data word into output latch	H	H	Output data word latched	H	H	Hi-Z	H	Enabled
							Output Syndrome bits	L	
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H H
				Ouput unchanged BYTE0	L				

†$\overline{OEB}$0 controls DB_0–DB_7 (BYTE0), $\overline{OEB}$1 controls DB_8–DB_{15} (BYTE1), $\overline{OEB}$2 controls DB16–DB23 (BYTE2), $\overline{OEB}$3 controls DB24–DB31 (BYTE3).

Read-Modify-Write (Byte Control) Operations

The DP8402A and DP8403 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, SO = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{LEDBO}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{OEB}$0 through $\overline{OEB}$3 controls. $\overline{OEB}$0 controls DB0–DB7 (byte 0), $\overline{OEB}$1 controls DB8–DB15 (byte 1), $\overline{OEB}$2 controls DB16–DB23 (byte 2), and $\overline{OEB}$3 controls DB24–DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table VI lists the read-modify-write functions.

Diagnostic Operations

The DP8402A thru DP8405 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{MERR}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{OECB}$ low. This outputs the latched checkword. With the DP8402A and DP8403, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the DP8404 and DP8405 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table VII DP8402A and DP8403 and Table VIII DP8404 and DP8405 list the diagnostic functions.

TABLE VII. DP8402A, DP8403 Diagnostic Function

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEBn}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains transparent	L	H	Input diagnostic data word†	H	L	Input check bits latched	H	Enabled	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bits	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Input diagnostic data word latched	H	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome bits	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

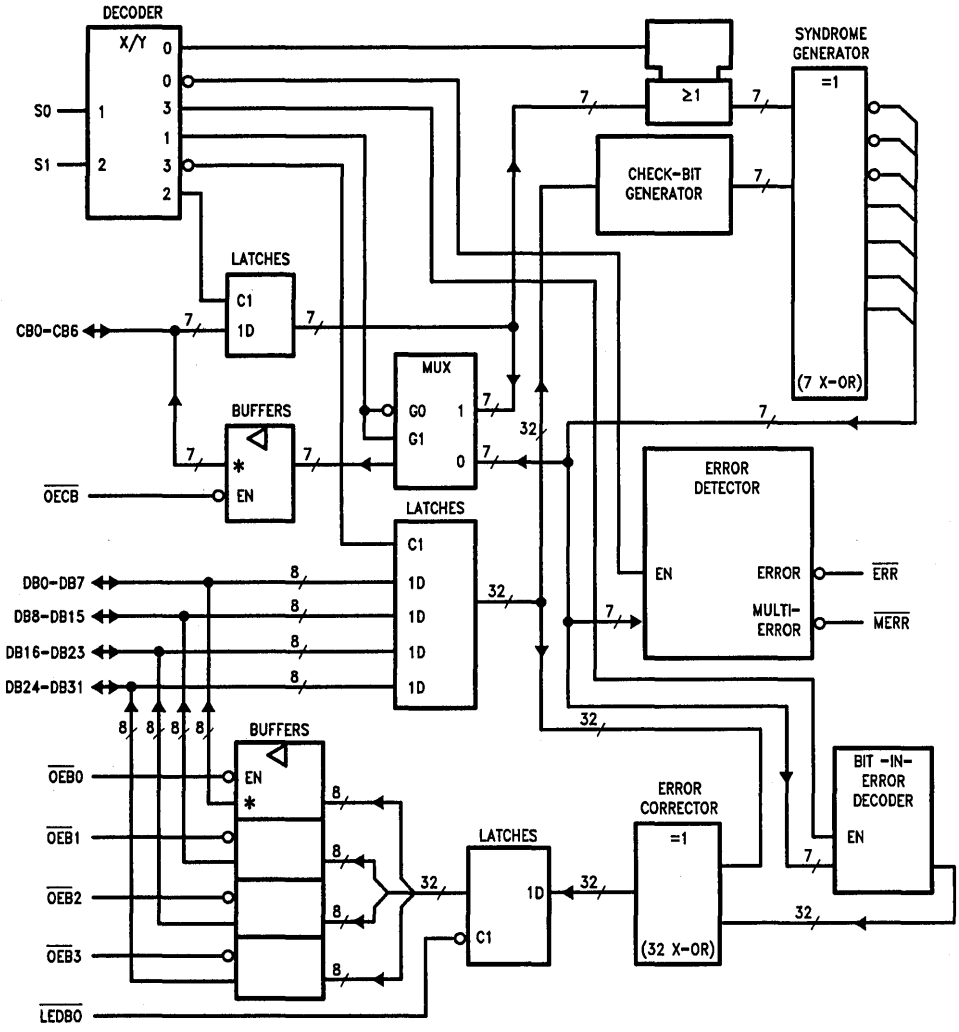
†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

TABLE VIII. DP8404, DP8405 Diagnostic Function

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB CONTROL $\overline{OEDB}$	CHECK I/O	DB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	Input correct check bits	H	H	H
Latch input check bits while data input latch remains transparent	L	H	Input diagnostic data word†	H	Input check bits latched	H	Enabled	
Output input check bits	L	H	Input diagnostic data word†	H	Output input check bits	L	Enabled	
Latch diagnostic data into input latch	H	H	Input diagnostic data word latched	H	Output syndrome bits	L	Enabled	
					Hi-Z	H		
Output corrected diagnostic data word	H	H	Output corrected diagnostic data word	L	Output syndrome bits	L	Enabled	
					Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

DP8402A, DP8403 Logic Diagram (Positive Logic)



DP8402A HAS TRI-STATE (▽) CHECK-BIT AND DATA OUTPUTS.
DP8403 HAS OPEN-COLLECTOR (◇) CHECK-BIT AND DATA OUTPUTS.

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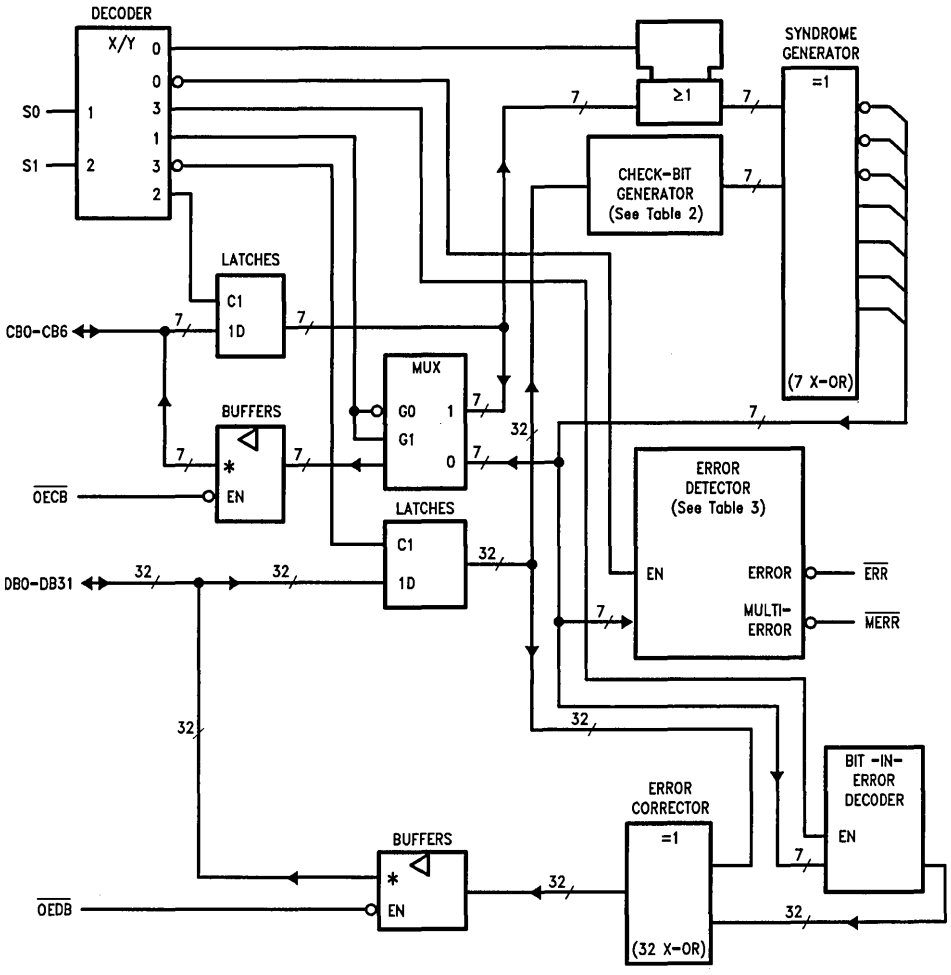
DP8404, DP8405 Logic Diagram (Positive Logic)



DP8404 HAS TRI-STATE (▽) CHECK-BIT AND DATA OUTPUTS.
DP8405 HAS OPEN-COLLECTOR (◇) CHECK-BIT AND DATA OUTPUTS.

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Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Over Operating Free-Air Temperature Range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) 7V

Input Voltage: CB and DB 5.5V

All Others 7V

Operating Free-Air Temperature: Military −55°C to +125°C

Commercial 0° to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-Level Input Voltage		2			2			V
V_{IL}	Low-Level Input Voltage				0.8			0.8	V
I_{OH}	High-Level Output Current	$\overline{ERR}$ Or $\overline{MERR}$			−0.4			−0.4	mA
		DB Or CB DP8402A, DP8404			−1			−2.6	
I_{OL}	Low-Level Output Current	$\overline{ERR}$ Or $\overline{MERR}$			4			8	mA
		DB or CB			12			24	
t_w	Pulse Duration	$\overline{LEDBO}$ Low	25			25			ns
t_{su}	Setup Time	(1) Data And Check Word Before S0 ↑ (S1 = H)	15			10			ns
		(2) SO High Before $\overline{LEDBO}$ ↑ (S1 = H)†	45			45			
		(3) $\overline{LEDBO}$ High Before The Earlier of S0 ↓ or S1 ↓ †	0			0			
		(4) $\overline{LEDBO}$ High Before S1 ↑ (S0 = H)	0			0			
		(5) Diagnostic Data Word Before S1 ↑ (S0 = H)	15			10			
		(6) Diagnostic Check Word Before The Later Of S1 ↓ or S0 ↑	15			10			
		(7) Diagnostic Data Word Before $\overline{LEDBO}$ ↑ (S1 = L and S0 = H)‡	25			20			
t_h	Hold Time	(8) Read-Mode, S0 Low And S1 High	35			30			ns
		(9) Data And Check Word After S0 ↑ (S1 = H)	20			15			
		(10) Data Word After S1 ↑ (S0 = H)	20			15			
		(11) Check Word After The Later of S1 ↓ or S0 ↑	20			15			
		(12) Diagnostic Data Word After $\overline{LEDBO}$ ↑ (S1 = L And S0 = H)‡	0			0			
t_{corr}	Correction Time (see *Figure 1*)*		65			58			ns
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

*This specification may be interpreted as the maximum delay to guarantee valid corrected data at the output and includes the t_{su} setup delay.

†These times ensure that corrected data is saved in the output data latch.

‡These times ensure that the diagnostic data word is saved in the output data latch.

DP8402A, DP8404 Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ†	Max	Min	Typ†	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	All outputs	V_{CC} = 4.5V to 5.5V, I_{OH} = − 0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5V, I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5V, I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5V, I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5V, I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
	All others	V_{CC} = 5.5V, V_I = 5.5V			0.1			0.1	
I_{IH}	S0 or S1	V_{CC} = 5.5V, V_I = 2.7V			20			20	µA
	All others‡				20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5V, V_I = 0.4V			−0.4			−0.4	mA
	All others‡				−0.1			−0.1	
I_O§		V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5V, (See Note 1)		150	250		150	250	mA

DP8403, DP8405 Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ†	Max	Min	Typ†	Max	
V_{IK}		V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
I_{OH}	DB or CB	V_{CC} = 4.5V, V_{OH} = 5.5V			0.1			0.1	mA
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8 mA					0.35	0.5	
	DB or CB	V_{CC} = 4.5V, I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5V, I_{OL} = 24 mA					0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5V, V_I = 7V							mA
	All others	V_{CC} = 5.5V, V_I = 5.5V							
I_{IH}	S0 or S1	V_{CC} = 5.5V, V_I = 2.7V							µA
	All others‡								
I_{IL}	S0 or S1	V_{CC} = 5.5V, V_I = 0.4V							mA
	All others‡								
I_O§	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5V, (See Note 1)		150			150		mA

†All typical values are at V_{CC} = 5V, T_A = +25°C.

‡For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Note 1: I_{CC} is measured with S0 and S1 at 4.5V and all CB and DB pins grounded.

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DP8402A Switching Characteristics

V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max (unless otherwise noted)

Symbol	From (Input)	To (Output)	Test Conditions	Military		Commercial		Units
				Min	Max	Min	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω	10	43	10	40	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω	10	43	10	40	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω	15	67	15	55	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500Ω	15	67	15	55	
t_{pd}	S0 ↓ and S1 ↓	CB	R1 = R2 = 500Ω	10	60	10	48	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500Ω	10	60	10	48	ns
t_{pd}	$\overline{LEDB0}$ ↓	DB	S1 = X, S0 = H, R1 = R2 = 500Ω	7	35	7	30	ns
t_{pd}	S1 ↑	CB	S0 = H, R1 = R2 = 500Ω	10	60	10	50	ns
t_{en}	$\overline{OECB}$ ↓	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns
t_{dis}	$\overline{OECB}$ ↑	CB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↓	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↑	DB	S0 = H, S1 = X, R1 = R2 = 500Ω	2	30	2	25	ns

DP8403 Switching Characteristics

V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max (unless otherwise noted)

Symbol	From (Input)	To (Output)	Test Conditions	Military			Commercial			Units
				Min	Typ†	Max	Min	Typ†	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500Ω		40			40		
t_{pd}	S0 ↓ and S1 ↓	CB	R_L = 680Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680Ω		40			40		ns
t_{pd}	$\overline{LEDB0}$ ↓	DB	S1 = X, S0 = H, R_L = 680Ω		26			26		ns
t_{pd}	S1 ↑	CB	S0 = H, R_L = 680Ω		40			40		ns
t_{PLH}	$\overline{OECB}$ ↑	CB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PHL}	$\overline{OECB}$ ↓	CB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PLH}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↑	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PHL}	$\overline{OEB0}$ thru $\overline{OEB3}$ ↓	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns

†All typical values are at V_{CC} = 5V, T_A = +25°C.

DP8404 Switching Characteristics, V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max

Symbol	From (Input)	To (Output)	Test Conditions	Military			Commercial			Units
				Min	Typ†	Max	Min	Typ†	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω		26			26		ns
			S1 = L, S0 = H, R_L = 500Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500Ω		40			40		
t_{pd}	S0 ↓ and S1 ↓	CB	R1 = R2 = 500Ω		35			35		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500Ω		35			35		ns
t_{pd}	S1 ↑	CB	S0 = H, R1 = R2 = 500Ω		35			35		ns
t_{en}	$\overline{OECB}$ ↓	CB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns
t_{dis}	$\overline{OECB}$ ↑	CB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns
t_{en}	$\overline{OECB}$ ↓	DB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns
t_{dis}	$\overline{OECB}$ ↑	DB	S1 = X, S0 = H, R1 = R2 = 500Ω		18			18		ns

DP8405 Switching Characteristics, V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max

Symbol	From (Input)	To (Output)	Test Conditions	Military			Commercial			Units
				Min	Typ†	Max	Min	Typ†	Max	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500Ω		26			26		ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500Ω		26			26		
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500Ω		40			40		ns
			S1 = L, S0 = H, R_L = 500Ω		40			40		
t_{pd}	S0 ↓ and S1 ↓	CB	R_L = 680Ω		40			40		ns
t_{pd}	DB	CB	S1 = L, S0 = L, R_L = 680Ω		40			40		ns
t_{pd}	S1 ↑	DB	S0 = H, R_L = 680Ω		40			40		ns
t_{PLH}	$\overline{OECB}$ ↑	CB	S1 = X, S0 = H, R_L = 500Ω		24			24		ns
t_{PHL}	$\overline{OECB}$ ↓	CB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PLH}	$\overline{OEDB}$ ↑	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns
t_{PHL}	$\overline{OEDB}$ ↓	DB	S1 = X, S0 = H, R_L = 680Ω		24			24		ns

†All typical values are at V_{CC} = 5V, T_A = +25°C.

Switching Waveforms

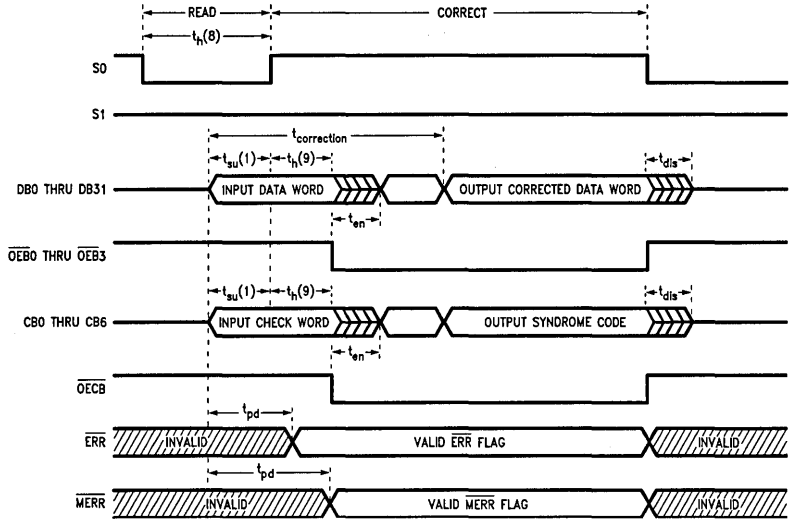

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FIGURE 1. Read, Flag, and Correct Mode

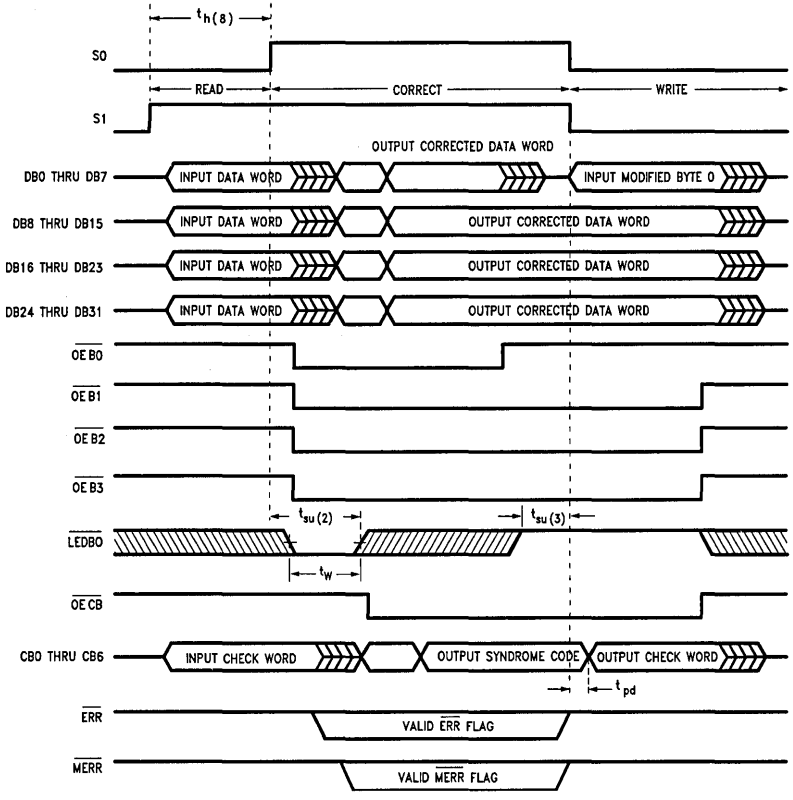

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FIGURE 2. Read, Correct Modify Mode

Switching Waveforms (Continued)

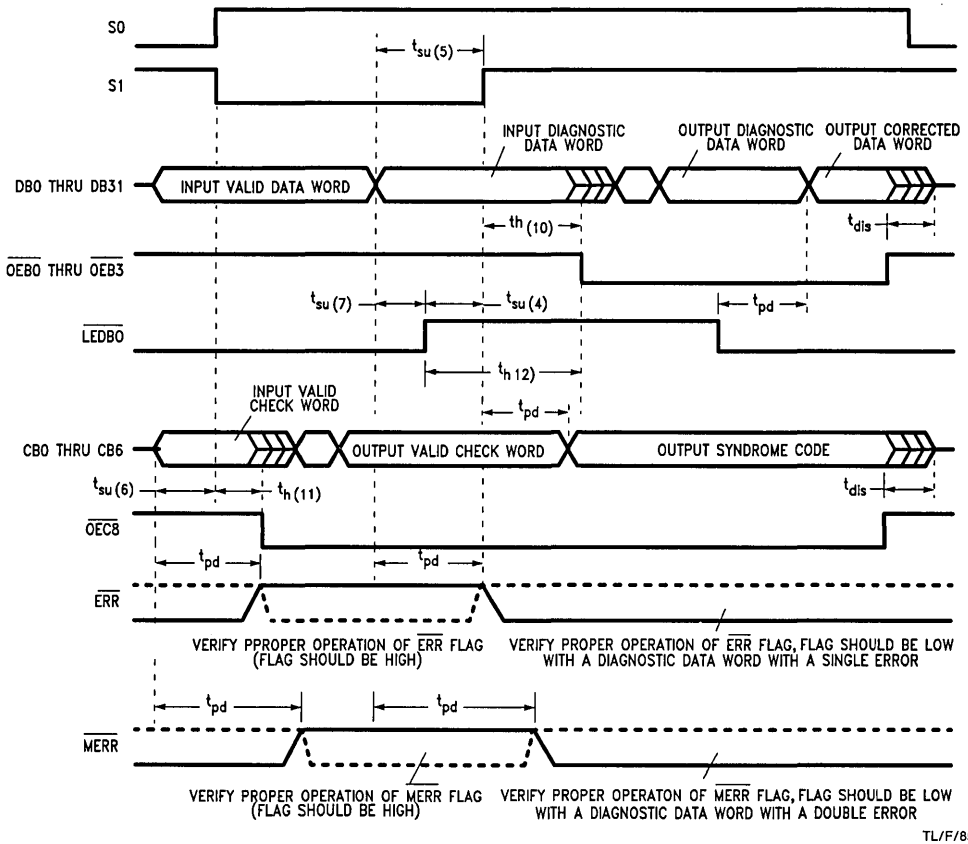

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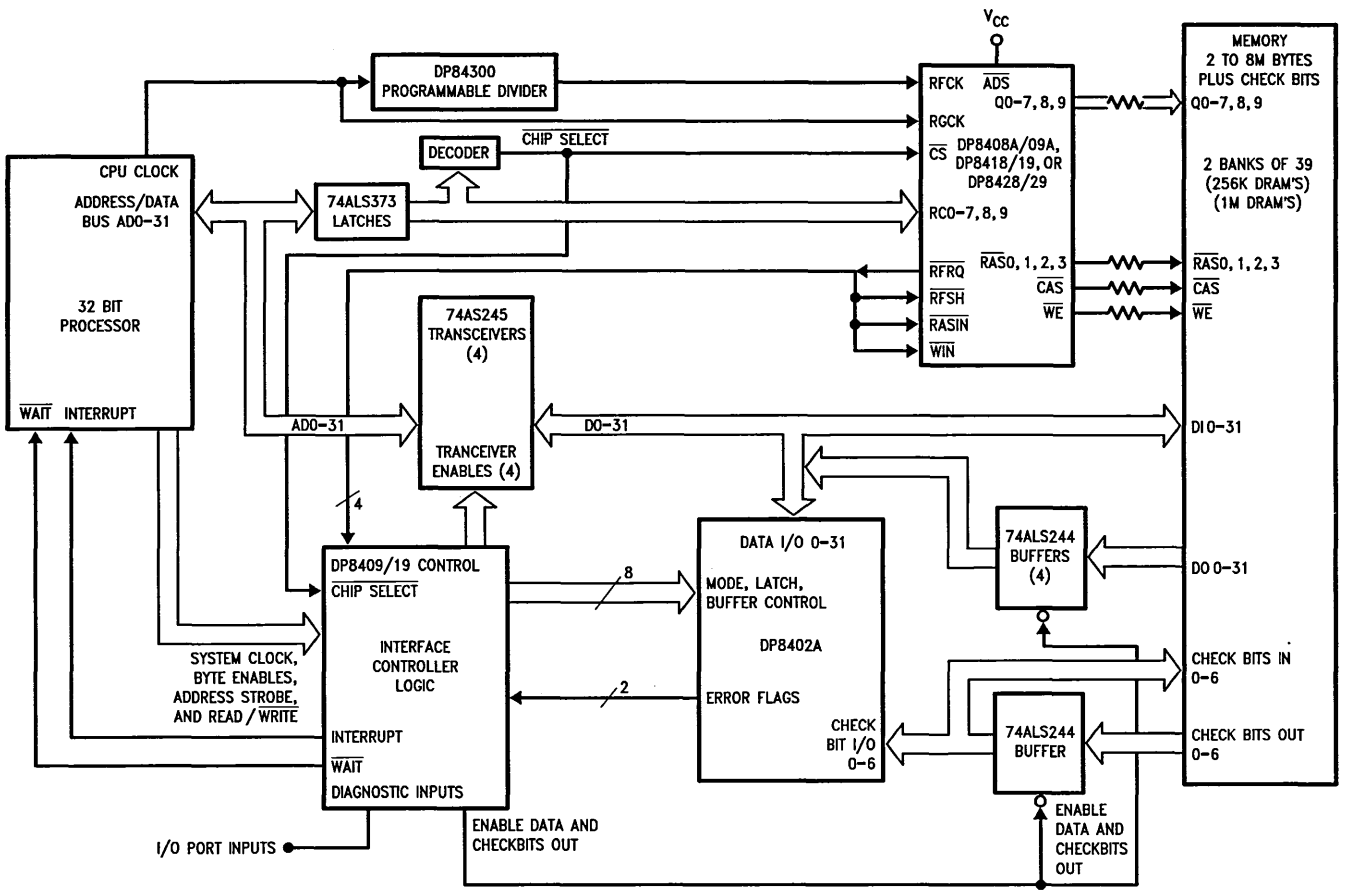
FIGURE 3. Diagnostic Mode

2

DP8402A System Diagram



TL/F/8535-9

Expanding the Versatility of the DP8400

National Semiconductor
Application Note 306
Mike Evans

BASIC OPERATION OF THE DP8400

Introducing error correction capabilities to a memory incurs some penalties–extra memory, additional access times, and extra control circuitry. The DP8400 has been designed to minimize the last two, and for some data word widths, less extra memory is required than for other error correction circuits.

In systems using error correction, extra memory is needed for check bits, which are merely parity bits, each derived from different combinations of the data bits. If a single error does occur, the error correction circuit can determine which bit is in error and then complement that bit, to re-create the original data word. As the memory data word widens, the ratio of check bits to memory data bits is reduced. As a rough guide, starting with four data bits and four check bits, one additional check bit is required each time the data word doubles.

A circuit diagram of how the DP8400 generates the check bits in a write cycle and corrects errors in a read cycle is shown in *Figure 1a*, which uses four data bits and four check bits. A 4-bit example is shown in *Figure 1b*. In a write cycle, the data input latch, DIL, receives the system data and generates four parity bits or check bits, which pass through the check bit output latch, COL, and buffer, to be written to the selected memory location with the system data. This delays every write cycle, but fortunately the DP8400 takes only 30 ns extra to generate the (six) check bits. When this location is subsequently read, the four memory data bits pass through DIL to generate four new check bits. The four memory check bits pass through the check bit input latch, CIL, and are fed into four Exclusive-OR gates with the four generated check bits. The outputs of these gates are called syndrome bits, and obviously, if there are no errors, the two sets of check bits will be the same and no syndrome bits will go high. If there is an error in the check bits, only the corresponding syndrome bit will go high; in this case the data bits are still correct. If one of the data bits is in error, three syndrome bits will go high (in the case of DP8400, three or five will go high), and the syndrome word is unique for any of the bits in error. The four AND-gates decode which bit is in error and complement it out of the second set of Exclusive-OR gates. The other three output bits remain the same as the input bits, so the corrected word is now available to the system.

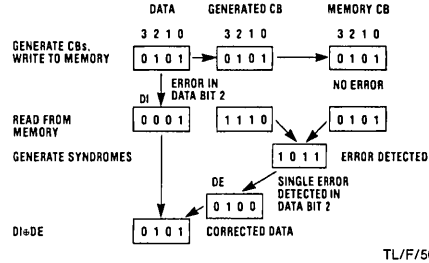


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FIGURE 1b. Example of Single Error Correction

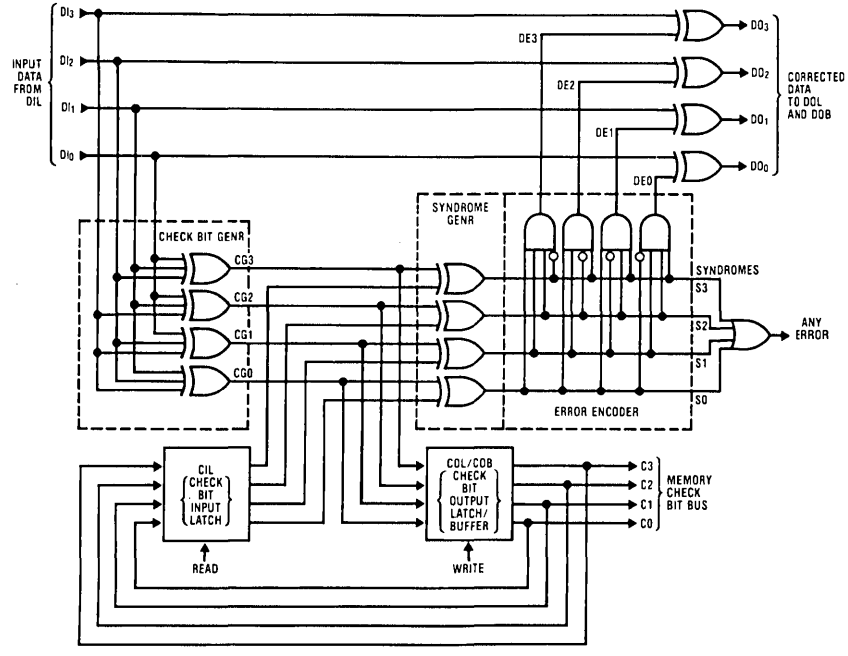

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FIGURE 1a. Error Correction 4-Bit Functional Diagram

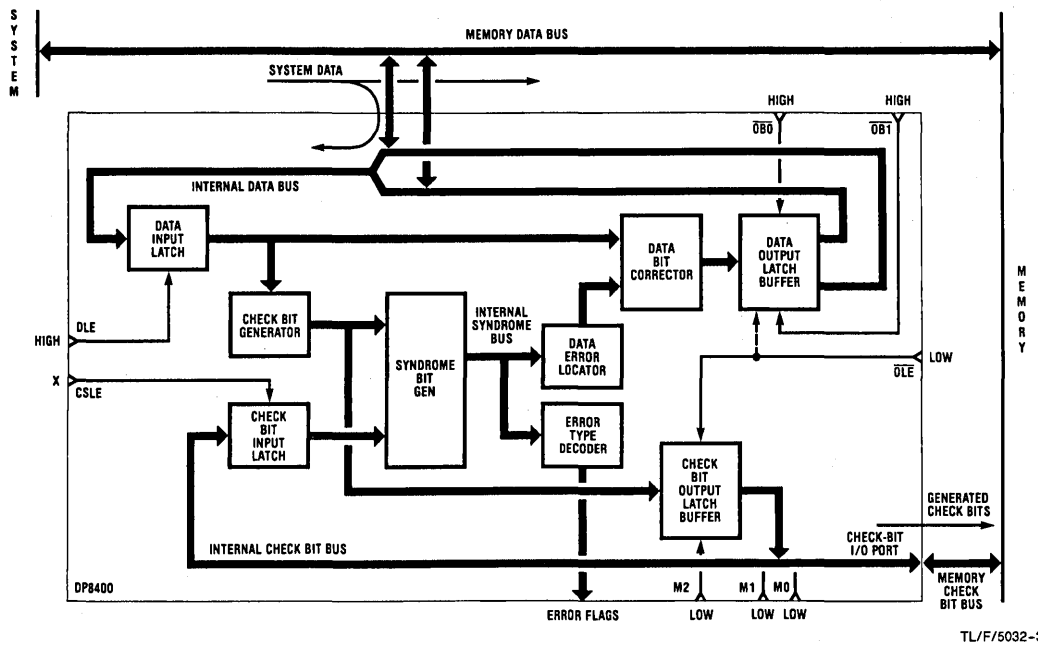

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FIGURE 2a. DP8400 Write To Memory Cycle

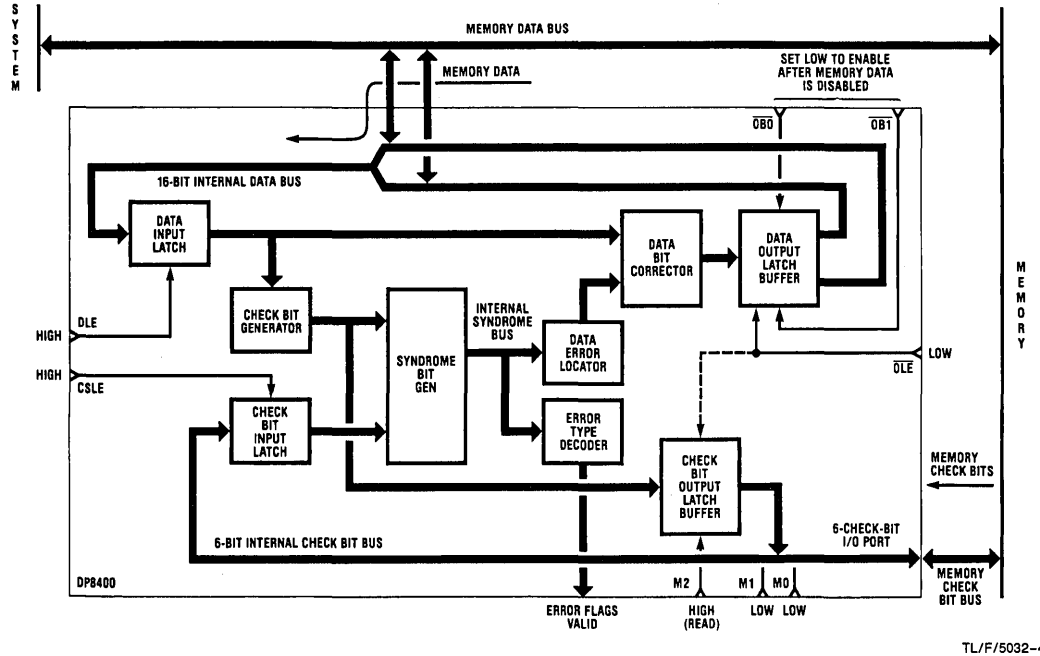

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FIGURE 2b. DP8400 Read From Memory Cycle

In the case of the DP8400 with 16 data bits and 6 check bits, there are 16 AND-gates to decode the 6 syndrome bits to determine the data bit in error. Table I shows the DP8400 matrix, called a Nelson Code, which has some unique features concerned with double soft error correction. For the purposes of this description, the matrix may be considered to be a form of Modified Hamming Code. The matrix has two functions: horizontally it tells us the value of the generated check bits for any data word when writing to memory, and vertically it tells us the syndrome word for any data bit in error. In a write cycle to memory, a '1' in any row indicates that the data bit in that column helps generate the parity bit in that row. For example, check bit 1 checks the parity of data bits 3, 6, 8, 9, 11, 13, 14 and 15, and generates even parity for those data bits. In a read cycle from memory, three or five of the six syndrome bits will go high for a single data bit error, and the columns represent the syndrome word, so the data bit in error is the number at the top of the column for that syndrome word. The 16 AND-gates each decode one of the 16 syndrome words shown in the columns of Table I, to locate the error. If there is a data bit error, one of the outputs of the 16 AND-gates will go high, to complement the data bit in error.

If two errors have occurred, the syndrome word is simply the Exclusive-OR of the syndrome words of the two individual bits in error, whether data or check bits, and is always even parity. First, if two check bits are in error, the corresponding two syndrome bits will go high. Second, for one data bit and one check bit error, then either two, four or six syndrome bits will go high. Finally, if two data bits are in error, again two, four or six syndrome bits go high. Thus a parity on the syndromes will indicate any two errors. This is important because if we know there are two errors, the DP8400 can attempt to correct them. The third error flag, E1, is the parity of the syndrome bus and check bit error. The DP8400 provides three error flags AE (Any error), E0 and E1, as shown in Table II, so that the exact nature of the error can be determined.

CONFIGURATION AND CONTROL OF THE DP8400

The DP8400 has a 16-bit data I/O port and an 8-bit check bit I/O port (6 bits used with 16 data bits) for applications with memories used with 16-bit microprocessors. The 16-bit data I/O port sits on the memory data bus, and the 6 check bit I/O port connects directly to the check bit section of memory. In other words, each memory location now contains 16 data bits with 6 check bits. The DP8400 is expandable to beyond 80 data bits, each additional 16 data bits requiring an additional DP8400 without the need for extra logic circuitry. 32-bit wide memory busses are also a popular width for minicomputers. In addition, 16-bit microprocessor systems may use 32-bit memory, because this larger memory data width requires only 7 check bits, a lower percentage overhead of check bits to data bits.

Figures 2a and *2b* show a simplified block diagram of the DP8400 with its control signals. The numerous control signals provide ease of use in the many varied applications of this chip. There are three latch enable signals DLE, CSLE and $\overline{\text{OLE}}$. Whenever DLE is high, data on the data I/O port D0–15 is entered into the data input latch DIL, and is latched in as DLE goes low. This allows either processor or memory data to be present on the data bus for only 3 ns prior to, and held over for 10 ns after DLE goes low. The data can then be removed if desired. Similarly, CSLE, when high, allows check bits on the check bit I/O port and external data on the syndrome I/O port to enter the check bit and syndrome input latches (CIL and SIL), respectively. These are latched in as CSLE goes low. (In 16-bit operation, $\overline{\text{OES}}$, Output Enable Syndromes, will be set low permanently, inhibiting CSLE to SIL, which remains in the power-up reset condition so that it does not affect the simplified block diagram.) $\overline{\text{OLE}}$, when set low, allows internal information into the data and check bit output latches (and the syndrome output latch, not shown). As $\overline{\text{OLE}}$ goes high, this information becomes latched. For some less complex designs, DLE, CSLE and $\overline{\text{OLE}}$ may be linked together. Providing $\overline{\text{OLE}}$ was low to allow corrected data into DOL, then $\overline{\text{OB0}}$ and $\overline{\text{OB1}}$, when set low, enable the two data output buffers to present corrected data to the system. Data is enabled or disabled within 15 ns of these inputs going low or high, respectively.

The DP8400 has three mode pins, M2, M1 and M0, which offer eight major modes of operation, designated 0 to 7. The most important two are Normal Write and Normal Read, and for these M1 and M0 are set low. M2 is READ/$\overline{\text{WRITE}}$ so Normal Write is mode 0 and Normal Read is mode 4. Other modes are used for the Double Complement Correct approach (Modes 1, 3 and 5) and for diagnostics (Modes 2 and 6). Mode 7 used when expanded to more than 16 data bits and fast correction times are required.

NORMAL OPERATION WITH A 16 DATA BIT MEMORY

The basic requirements for normal operation of the DP8400 are that it generates check bits, detect errors and correct them with minimum delays, and that it be easy to use. In normal operation M1 and M0 are set low. *Figure 2a* shows how the DP8400 generates check bits when writing data to memory. DLE may be kept high, $\overline{\text{OLE}}$ low, CSLE low, and M2 low so that the DP8400 is in Mode 0. System data is presented to the data I/O port on pins D0–15, and enters DIL, where it connects to the check bit generator CG. The six generated check bits pass through COL and are enabled (with M2 low) onto the check bit I/O port. The six generated check bits will appear 30 ns after the 16 data bits are presented to the data I/O port. A write to memory will now store the 16 data bits and 6 corresponding check bits in the selected location of memory. The write cycle is therefore slowed down by 30 ns, which in most memory systems is not significant.

Figure 2b shows the paths when reading from memory, with DLE set high to enter the memory data bits into DIL, and CSLE also set high to enter memory check bits into CIL. M2 is set high so that the DP8400 is in Mode 4. The Any Error flag, AE, becomes valid 35 ns after memory data and check bits are valid. Error flags E1 and E0 become valid approximately 15 ns later. Thus, if AE is low, no further operations are necessary. For fast 16-bit microprocessor systems, it may be necessary to introduce a wait state every read cycle to first determine if an error exists. If no error is detected the wait state is removed and the read cycle continues.

If an error is detected, then the error flags E1 and E0 must be examined to determine the required action. If the error is a single data bit error, DOL will by now contain corrected data. If there is no check bit error, then COL, which follows CIL when in Mode 4, now contains the original check bits. By taking $\overline{\text{OLE}}$ high, corrected data bits are latched in DOL, and correct check bits in COL. The memory is now disabled, so that $\overline{\text{OB0}}$ and $\overline{\text{OB1}}$ can be set low to enable corrected data onto the data bus, and M2 set low to enable the contents of COL onto the check bit bus. A write to the same location of memory will therefore remove the data bit error if

it was a soft error. The microprocessor can read the corrected data once the wait signal is removed.

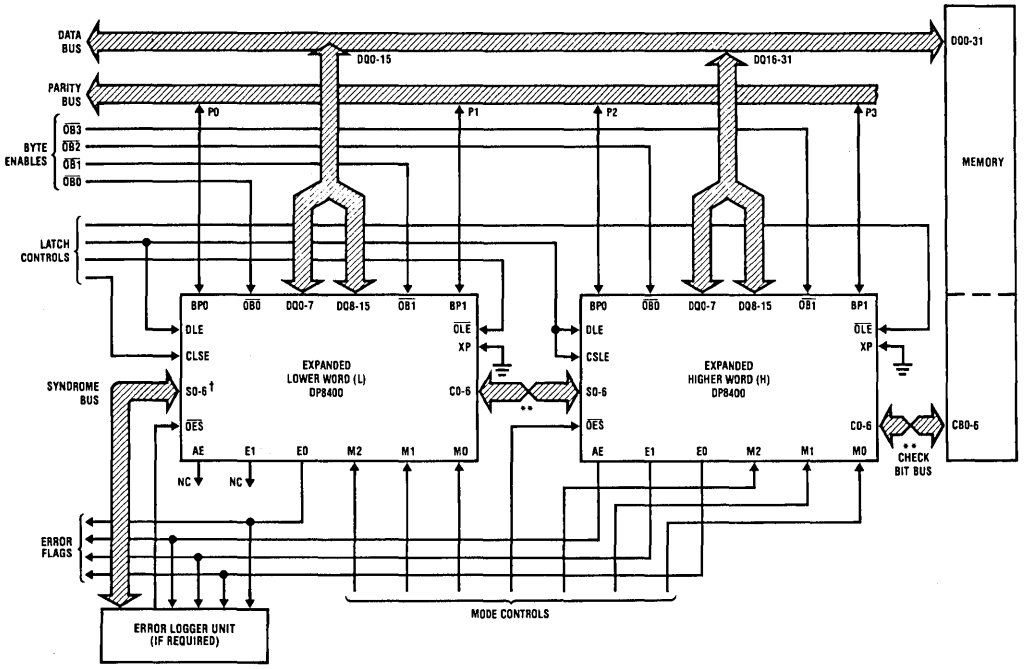
If the error is a single check bit error, DLE should be set low. DOL contains the contents of DIL, still correct data. Memory can now be disabled so that $\overline{OB0}$ and $\overline{OB1}$, when set low, output correct data, and M2 when set low, allows the generated check bits from DIL to be output on the check bit I/O port. A write to the same location of memory will remove the check bit error if it was a soft error. The microprocessor now reads this correct data when the wait signal is removed. If a double bit error is detected, then other approaches may be taken, as described in the data sheet and later in this application note.

The primary features of the DP8400 are discussed in the data sheet; there are, however, a number of other features that become very useful once a designer becomes acquainted with error correcting techniques.

These include: expansion beyond 16 data bits, diagnostic routines, error logging (allowing some double error correction), and a novel approach offering fast correction of any double error. This application note discusses how the DP8400 has been designed to function in all of these applications, making it the most versatile and comprehensive error correction chip available.

ERROR CHECKING AND CORRECTING FOR WIDER-THAN-16-BITS DATA WIDTHS

At present, most 16-bit microprocessor systems use a 16-bit wide main memory, partly for simplicity, and also because main memories, in general, have not become large enough in size to justify otherwise. The data sheet shows how to accomplish this with one DP8400, utilizing the matrix of Table I. It is fairly easy to use a memory of twice the microprocessor data width to reduce total chip count when incorporating error correction capability. One example would be a complex 8-bit microprocessor using large main memory. If the memory data width is kept at eight bits, then five check bits are required for error correction for each byte of data. If four banks of memory are required, each bank comprising 13 chips, then 52 total memory chips are required and only 62% of the memory is used for system data. If the memory data width is increased to 16 bits for the same microprocessor-based system, then six check bits are required.



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†Refer to discussion in "Other Modes of Operation" under Clearing SIL.

** Connection sequence must be done according to Table VIII.

FIGURE 3. 32-Bit Error Detection and Correction

The memory now comprises two banks each of 22 chips, totaling 44 memory chips–a savings of eight memory chips. This saving is offset somewhat by the need to incorporate byte-writing capability, which does require extra components and slows down the memory write cycle. One DP8400 is still needed, using all 16 bits, and two bidirectional buffers are also required.

As a second example, using a 16-bit microprocessor with a memory of eight banks, each comprising 16 bits of data and six check bits, the total is 8 × 22 or 176 memory chips. Once the memory is widened to 32 data bits with seven check bits, only four banks are required, and the total number of memory chips reduces to 4 × 39, or 156—a savings of 20 memory chips. This is offset a little by the fact that an extra DP8400 is required, and slightly slower memory write and read cycles are necessary. In some cases, therefore, widening the memory data bus becomes more practical for large memories.

Saving memory chips is just one reason why there is a need to be able to expand the DP8400 beyond 16 data bits. Most minicomputers now use 32-bit wide data busses, and soon there will be some 32-bit microprocessors. Other systems use 24 bits, 48 bits, 52 bits, 64 bits or a variety of other data widths. The DP8400 has been configured to be expandable to any data width, even beyond 80 bits, merely by inserting an additional DP8400 for each 16-bit increment in memory data.

A section of the chip shown in the data sheet Block Diagram comprises the syndrome input and output latches, SIL and-SOL, and a dedicated syndrome I/O port. This port has a number of uses not normally needed in simple 16-bit single error correction applications.

One use of this syndrome port is for data widths wider than 16 bits. Only one DP8400 is required with 16 data bits or less, but if a system uses more than 16 memory data bits, additional DP8400s are required. For example, two DP8400s, one with its 16-bit data port connected to the lower word, and the other to the higher word, can be configured to generate check bits, and detect and correct errors for a 32-bit memory as shown in *Figure 3*. For writing to memory, both chips will still generate six check bits from the two words of 16 bits. But with more than 26 total data bits, seven check bits are required. Therefore, it is necessary to combine the two sets of check bits to produce seven composite check bits to be written to memory as shown in the flow path depicted in *Figure 4a*. This is achieved by outputting the six generated check bits from the lower word DP8400 (designated L), and inputting them to H, the higher word DP8400. The syndrome port of H is available to receive these check bits from L, to be loaded into SIL of H, provided CSLE is high. The six outputs from SIL combine with the six check bits generated in H to create seven composite check bits, and this 7-bit combination is output on the check bit port to the memory check bits. Table II shows one of twelve possible ways to combine the two sets of check bits. Note that the lower word matrix for bits 0 and 15 is identical to Table I with the addition of all "0"s for the seventh check bit. The higher word matrix for bits 16 to 31 uses the same rows but in a different order, implying that the check bits from L must be cross-connected to H. For example, memory check bit 5 is generated from check bit 1 of L and check bit 5 of H. Both chips are therefore set to normal write mode when generating check bits.

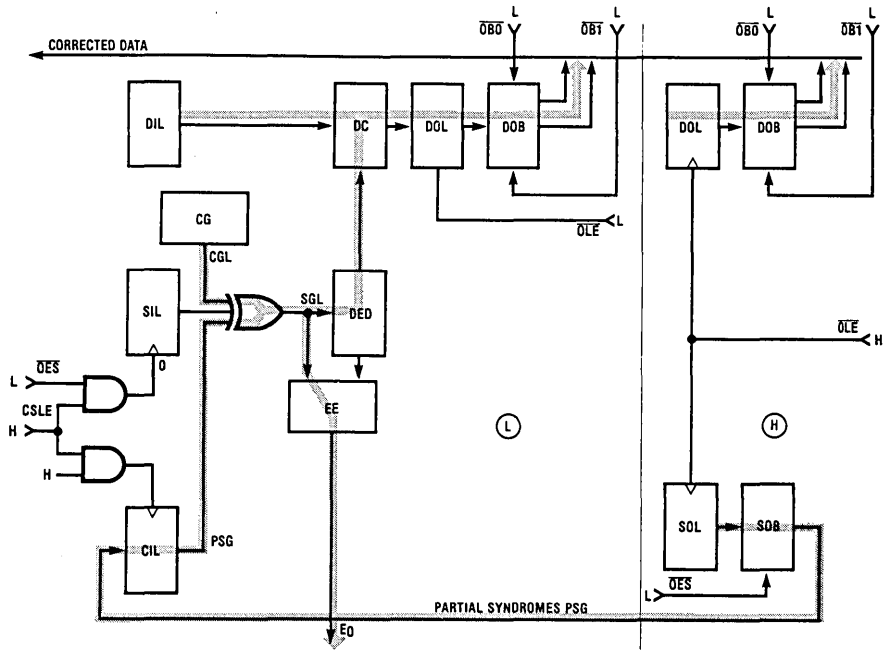

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FIGURE 4a. E²C² 32-Bit Configuration, Error-Correct Flow Path

When reading from memory, the two chips first need to detect for an error. *Figure 4b* shows the flow path through the chips. L is set to normal write mode and H to normal read mode. Memory data is supplied to both chips so that L generates six check bits from the lower word data bits, and feeds them to SIL of H, the same as for writing. H also generates its own check bits which combine with those from L, and these seven composite check bits are compared with the seven memory check bits fed into CIL of H. This combining, plus comparison of check bits, is equivalent to seven 3-input Exclusive-OR gates. The output of these Exclusive-OR gates are the seven syndrome bits, and these can be decoded to determine the type of error. First, if there is no error, error flag AE of H will remain inactive because memory data is correct, provided $\overline{OLE}$ is kept low, and DOL of both L and H will contain correct data. Second, if there is a memory check bit error, only one of the seven syndromes will go high and the three error flags of H will indicate a check bit error as in Table III. Note that memory data is still correct, and with $\overline{OLE}$ low, DOL of both L and H contain correct data. Third, if there is a single data error in bits 16-31, the syndromes of H are such that the data error locator will locate the error and correct it, so again DOL of both L and H contain correct data. This is because the seventh syndrome bit is low for an error in the higher word, so that we have a six syndrome bit word as in Table I, to be decoded as normal to correct the error. In each of these three cases, DOL of both L and H contained correct data, and the common condition for these is either that AE(H) is "0", or E1(H) is "1".

The fourth case is more complex. In the previous three cases, correct data has been available in both DOL about 50 ns after memory data became valid. Now with a single data error in bits 0–15, AE(H) is a "1", E1(H) a "1", and EO(H) a "0", but L does not have sufficient information to locate the error. It is first necessary to feed back the partially generated syndromes of H back to L, and this is achieved by reversing the direction of the common bus. First L is placed in normal read mode so that L's generated check bits become disabled. Next, the partial syndromes in H are enabled onto the bus by setting $\overline{OES}$ of H low, so that its syndrome I/O port outputs the combined Exclusive-OR of CG(H) and CIL(H), which is transferred to CIL of L. These partial syndromes then combine with CG(L) to generate valid syndrome bits in L, demonstrated by the flow path of *Figure 4c*. If there is, in fact, a data bit error in bits 0–15, the seventh syndrome bit will go low, allowing the remaining six bits to be decoded to locate the error as per the columns of Table II. This switching around of the common bus, therefore, takes more time to correct the error in L, equivalent to a total time of approximately 100 ns. The fifth kind of error is identified as a double error. In this case, the error flags indicate the double error and the system can take the necessary action.

A logical approach when using two DP8400s would be to first see if there is any need to reverse the common bus by monitoring AE(H), and when it is low, to output directly from DOL of both chips by setting $\overline{OB0}$ and $\overline{OB1}$ of each low. The System Data Valid flag should be set active at this time. If the AE(H) output is high and the error flags do not indicate a double error, then the common bus should be switched around and the System Data Valid signal set true. If the error is a double error, the user may utilize a number of alternatives, including the Double Complement Correct method.

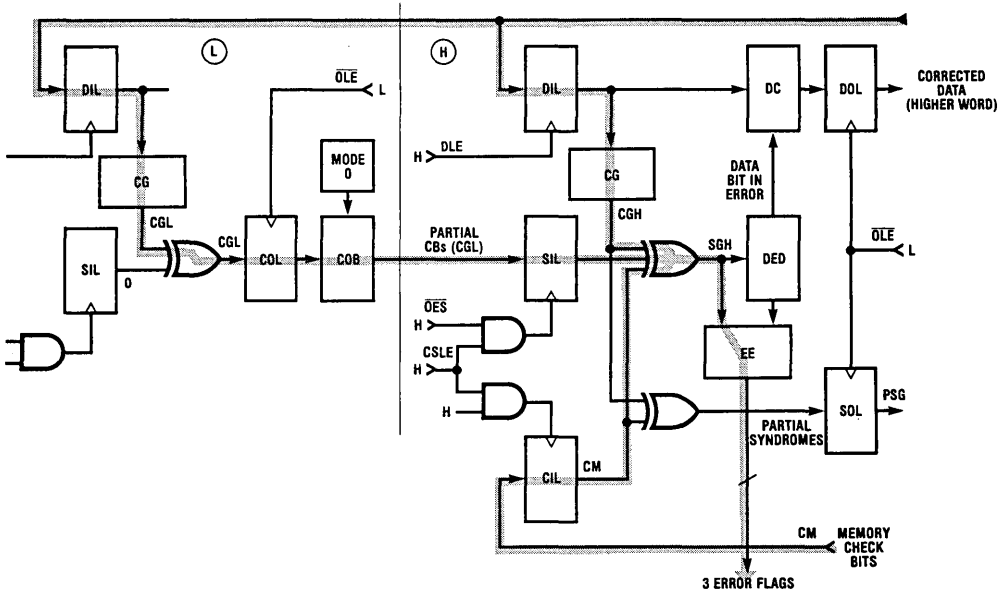

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FIGURE 4b. E²C² 32-Bit Configuration, Detect Flow Path

TABLE I. Data In to Check Bit Generate, or Data Bit Error to Syndrome-Generate Matrix (16-Bit Configuration)

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
		GENERATE CHECK BITS																DQ0–15
GENERATED SYNDROMES	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	
	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1	
	2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2*	GENERATED CHECK BITS
	3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3*	
	4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4	
	5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5	
		4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	0	
		3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	1	
		HEXADECIMAL EQUIVALENT OF SYNDROME BITS																	

*C2, C3 generate odd parity.

TABLE II. Data Bit Error to Syndrome-Generate Matrix (32-Bit Configuration)

		L																H															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
																																		DQ0–31
	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	1	0	1	1	0	1	1	0	1	1	1
	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
	*2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
SYNDROMES	*3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3
	4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
	5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2
	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0
		4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	2	A	A	1	2	2	3	8	B	9	8	1	A	3	B	9	0	HEX
		3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	3	1	4	6	6	5	4	5	3	4	6	5	2	7	6	7	1	

*CG2, CG3 generate odd parity.

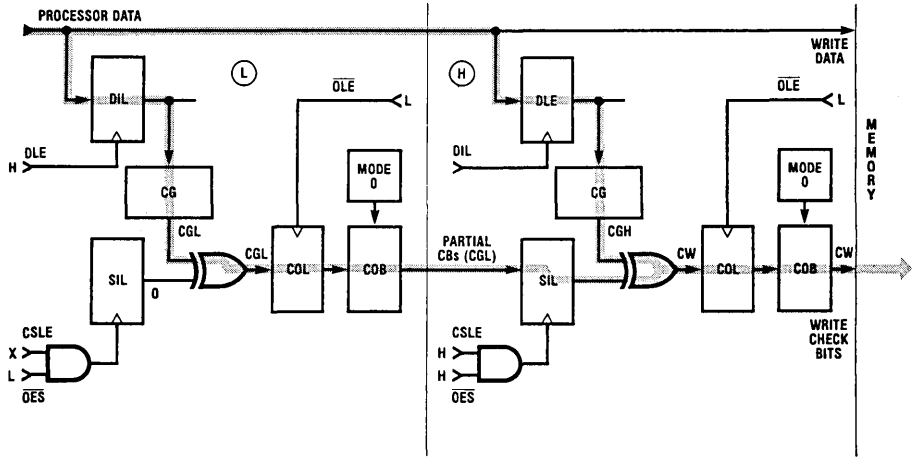

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FIGURE 4c. E²C² 32-Bit Configuration, Write Flow Path

TABLE III. Error Flags After Normal Read (32-Bit Configuration)

AE (H)	E1 (H)	E0(H)	E0(L)*	Error Type
0	0	0	0	No Error
1	1	0	0	Single check bit error
1	1	1	0	Single data bit error (H)
1	1	0	1	Single data bit error (L)
1	0	0	0	Double bit error
	All Others			Invalid conditions

*E0 (L) is valid after transfer of partial syndromes from higher to lower.

This approach to wider data width error detection and correction is termed the cascade configuration, and it requires only the one additional DP8400. The cascade approach can be used with up to five DP8400s controlling 80 data bits. The advantage is that only one additional DP8400 is required per 16 data bits, although write and read times become progressively slower as the number of DP8400s is increased. This is because of the time taken for the generated check bits to ripple through from the lowest to highest chips when writing and detecting, and then ripple back the other way for correcting.

In many memory systems, speed is of utmost importance and for faster systems, it is possible to connect the DP8400s in a parallel configuration using additional ICs. Application Note AN-308 describes this approach in detail.

The user may, therefore, select one of these approaches (or a combination of both) for systems using memory data widths of more than 16 bits.

DIAGNOSTIC CAPABILITIES OF THE DP8400

The DP8400 has been designed with system fault diagnois in mind. In fact, it is possible under microprocessor control with the DP8400 in site on the memory board to fully test every gate inside the DP8400 activated in normal operation, and also to diagnose all memory check bits. The DP8400 has two main diagnostic modes–modes 2 and 6. In other words, with M1 set high and M0 set low, information can be written to or read from the chip.

Mode 6 allows the memory check bits to be read onto the higher byte bits 8–14, and syndromes to be read on the lower byte bits 0–6, as shown in *Figure 5a*. The remaining two bits, 7 and 15, are the error flags E1 and E0 that were valid when mode 6 was entered. The syndrome bits will be the internally generated syndromes if $\overline{OES}$ is low (mode 6A), or external syndromes input on the syndrome I/O port if $\overline{OES}$ is high (mode 6B). The external syndromes could be obtained from an error logger/syndrome injector unit—this is an error logger with the capability of injecting syndromes back to the DP8400. Therefore, by being able to read the externally stored syndromes, the microprocessor can monitor or store the syndromes whenever needed.

Mode 2 transfers system data from the higher byte into CIL, instead of DIL, to simulate check bits. This can be used in three ways. First, as shown in *Figure 5b*, the simulated check bits can be latched in CIL by taking CSLE low. If the DP8400 is now set to normal read, mode 4, and new data is presented then, provided DLE is high and CSLE is kept low, the DP8400 will perform a normal read operation as if it were reading memory check bits. The results of this simulated read may be checked by enabling DOL to see if an error (if inserted) was corrected. Or as a further check, by entering mode 6, the predicted generated syndromes and error flags may be checked. Second, also while in mode 2, the simulated check bits appear at the check bit port (from the data bus higher byte) available to be written to the check bit portion of memory as shown in *Figure 4c*. $\overline{OLE}$ is set high before the original simulated check bits are removed and then memory data is subsequently placed on the data bus. A write to memory will now write known data and simulated check bits to the selected location. By writing known data to the memory check bits in mode 2, and then reading the memory check bits in mode 6, each check bit in each location can be validated. Third, it is possible in mode 2 with $\overline{OES}$ low to transfer data from the higher byte to the syndrome I/O port, also shown in *Figure 5c*. But first the generated check bits must be all low. This is attained by previously loading all "1"s into DIL in an earlier cycle. This is useful when using an error logger in conjunction with the DP8400 to feed the syndrome word into the logger whenever an error occurs.

ERROR LOGGING WITH SYNDROME INJECTION CAPABILITY

An important application of the dedicated syndrome I/O port is for error logging. This is because the internally generated syndromes derived during reading are available on this port, provided $\overline{OES}$ is set low. These syndromes indicate the exact location of a single error, whether it is in the data bits or check bits; they are therefore useful to be stored for error logging. Every time an error occurs when indicated by error flag AE, the syndromes corresponding to this error can be logged.

The syndrome word can be fed from SOL via the Syndrome Output Buffer onto the external syndrome bus. An Error Logger connected to this bus, as shown in *Figure 6*, will store the syndrome word in the same location as the corresponding address of each error that ocurs. An intelligent error logger will differentiate between new errors and ones that have occurred previously, by logging only new errors and ignoring ones that have already occurred. An easy way to determine this would be to compare the incoming memory address with the address of errors contained in the logger. If a match is not found and an error occurs, the new address and corresponding syndromes are logged. If a match is found, then whether an error occurs or not,

no further action is necessary. Tag bits may be provided to indicate whether the error is hard or soft.

For example, if an error has already been logged at a particular address and that address is re-written to, then if the error repeats subsequently, it is a hard error, and if not, it is a soft error. So, if a tag bit is set when a write occurs to a previously logged address and a subsequent error is detected at that address, a second tag bit is set indicating a hard error. A better approach would be to have the DP8400 correct and rewrite to the same location all in the same cycle, as soon as a single error is detected. The first error detected in a location is classified as a soft error until it recurs, and if an error does recur, a tag bit is set to indicate a hard error. It is assumed here that multiple soft errors will not occur in the same location.

Now that the error logger contains error information, it is necessary for the microprocessor to retrieve it. The DP8400 makes this easy, because the external syndrome bus data can be transferred to the data bus as described for operation in mode 6. If the error logger is made capable of outputting stored syndromes, and subsequently outputting the corresponding address one byte at a time, then all the relevant information can be retrieved by the microprocessor. The user may choose to store this in nonvolatile memory in the event of a power failure. When power returns, it will be desirable to restore this information back to the error logger, and this can be achieved by first loading DIL with all "1"s to create all generated check bits low. Now the addresses and syndromes can be loaded from the higher byte of the microprocessor through the syndrome I/O port one byte at a time, with DP8400 in mode 2, to the error logger.

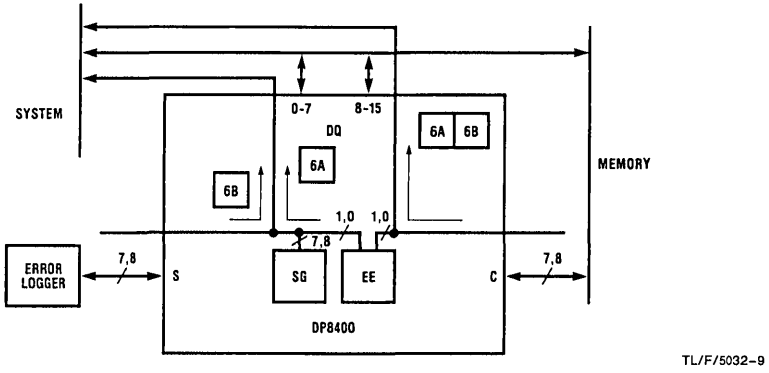

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FIGURE 5a. Read Internal Generated Syndromes and Check Bit Port (Mode 6A) or Read Syndrome Port and Check Bit Port (Mode 6B)

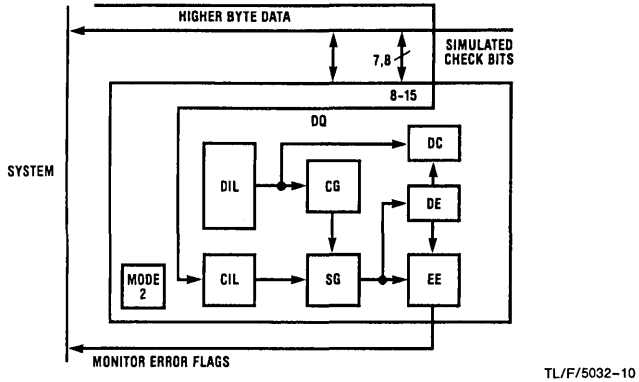

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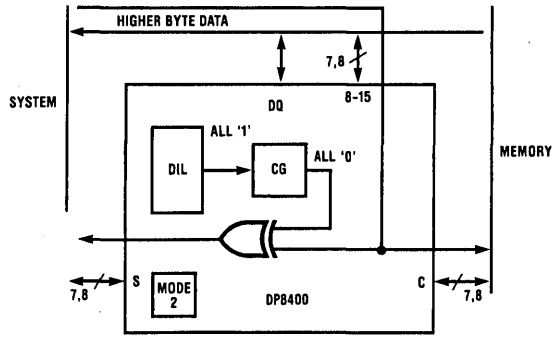
FIGURE 5b. Diagnostic Read – Compare Simulated Check Bits with Check Bits Generated from Data Stored in Previous Cycle



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1) DIAGNOSTIC WRITE: WRITE HIGHER DATA BYTE TO CHECK BIT BUS (MODE 2)

2) TRANSFER HIGHER DATA BYTE TO SYNDROME BUS (MODE 2, PREVIOUS CYCLE LATCHED ALL '1's IN DIL TO MAKE CG = 0)

FIGURE 5c. DP8400: Mode 2

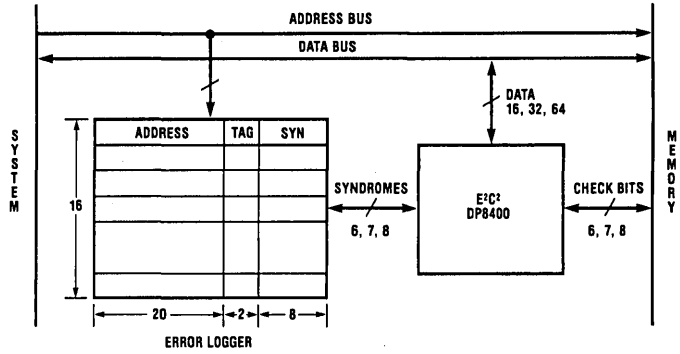

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FIGURE 6. Error Logger Connected to DP8400 Syndrome Port

CORRECTING DOUBLE ERRORS USING THE ERROR LOGGER

It is possible to take the error logging function one stage further. As described so far, the error logger has been storing single errors (data bit or check bit). What if a double error is detected? If it is detected without any previous history at that address, one solution would be to perform a Double Complement to attempt to correct both errors. If this is not done, no useful information can be obtained. If both errors are corrected, the error logger records the syndromes of both, and tags whether they were both hard, or one hard and one soft. But, if there is a previous history at this address of a single error, then it is fair to assume that the second error has subsequently occurred. In this case, if the error logger could be made to inject the syndromes of the first error into the DP8400, the DP8400 would correct this error so that its DOL would then contain data with one error (if both errors are data bit errors). It is necessary at this point to wrap-around DOL back to DIL and allow the DP8400 to correct the second error. This approach is much faster than the Double Complement approach and at the same time offers full error logging capability.

ANY DOUBLE ERROR CORRECTION USING THE DOUBLE SYNDROME DECODE APPROACH

The data sheet shows how the DP8400 can perform double error correction using the Double Complement Approach, provided at least one of the errors was hard. For very large memories, this may not be adequate, as some systems will require total double error correction capability–quickly, without having to wait two additional memory cycles. Some of these systems will also require triple error detect capability. Fortunately, the matrix of the DP8400 has been configured to allow both of these capabilities. Most modern error detection/correction matrices use a modified version of Hamming's original code. The Hamming code allows single errors to be corrected, however, two errors may not be detected as such. For 16 data bits, five check bits are required. Modified Hamming codes allow double error detect capability, as well, by arranging that the Exclusive-OR of the syndrome words of any two bits in error produces an even parity syndrome word. A parity check on the syndrome bus will, therefore, indicate two errors (or no error, but in this case, the Any Error flag will be inactive). For 16 data bits, six check bits are required for single/double error detect and single error correction capabilities.

The DP8400 has a matrix that goes one step further by using a version of the Nelson code. This costs no additional on-chip gates to those required for a Modified Hamming code. To be able to correct any two errors, it is necessary to be able to determine their location, and no present version of the Modified Hamming code is able to do this. There are matrices that do exist that can generate 12 check bits from 16 data bits (or 14 check bits from 32 data bits) for writing, and then generate 12 (or 14) syndrome bits when reading, so that the location of both errors can be determined and corrected. But, because most applications do not require this degree of integrity and associated expense, they are not very popular. It would be ideal if two DP8400s could be configured as in *Figure 7a*, with each generating a different set of check bits and a different set of syndrome bits so that the double syndrome word could be unique and decodable for any two bits in error. Fortunately, National Semiconductor has achieved this by incorporating a feature called the Rotational Syndrome Word Generator, which uses rotated data to the secondary DP8400.

The primary DP8400 generates check bits when writing, and syndrome bits when reading, as in a normal 16-bit system. But the data port of the secondary DP8400 receives data shifted by a number of bits, usually one bit. In other words, for this secondary chip, system data bit 0 connects to DQ1, system data bit 1 to DQ2, etc. Each DP8400 has its own dedicated six memory check bits, which are obviously different from each other due to the data shifting on the secondary DP8400. The Nelson code is such that during a read, not only does each DP8400 generate a different set of syndrome bits, but the double syndrome word (comprising 12 bits for 16 data bits) is unique for any two bits in error. It is necessary to be able to output these syndromes as they occur and to do this, $\overline{OES}$ of both chips is set low during the time memory data is valid.

Now that we have a unique double syndrome word for any two bits in error, it is necessary to decode it to correct both errors. The easiest way to do this is to connect the double syndrome word to the address inputs of a registered PROM (a PROM with latchable data out) as shown in *Figure 7b*. In this example, 12 syndrome bits require 4k addressing capability, and 32k registered PROMs will be made available soon. Some of the addresses of the RPROM will be used for double errors and each address will be unique for any two bits in error. The corresponding data out could, therefore, contain one of the syndrome words. Double errors may be caused by two data bit errors, a data bit and primary check bit error, a data bit and secondary check bit error, a primary and secondary check bit error, or two errors in either primary or secondary check bits. In these cases, if the RPROM address stores the syndrome word for one of the two errors, this will be available at the output of the RPROM when enabled.

First of all, this data must be latched in the RPROM register, and then the $\overline{OES}$ input to each DP8400 must be set high to deactivate the two syndrome output buffers. Next, the RPROM data must be enabled onto the primary syndrome bus so the primary DP8400 can enter this syndrome word, representing one of the two bits in error with CSLE high. At the same time, the primary DP8400 must be set to mode 7 so that the syndrome word appears on the internal syndrome bus, replacing the generated syndromes. If $\overline{OLE}$ is now set from low to high, DOL will contain either one or no error, depending on where the two errors were located. In other words, the DP8400 has just corrected one of the errors. By setting $\overline{OLE}$ low, then disabling memory and enabling $\overline{OB0}$ and $\overline{OB1}$ of the primary DP8400, this data is output on the data bus and back into the DIL with DLE high. There is now only one data error, and this can be corrected by setting the DP8400 to normal read, mode 4.

Thus, both errors have been corrected at a fairly fast rate. For example, for a 50 ns RPROM, the total time to generate double syndromes, feed back a one-error syndrome word to the primary DP8400, correct it, wraparound, and correct again, may take less than 120 ns total.

Only a few of the addresses in the RPROM are required for double errors. Some double syndrome words represent single errors and triple errors. All single bit errors also produce a unique double syndrome word different from all double bit errors.

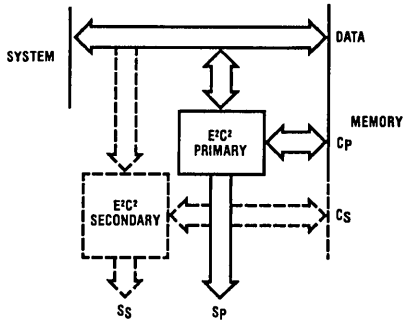

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FIGURE 7a. 2 Different Generators

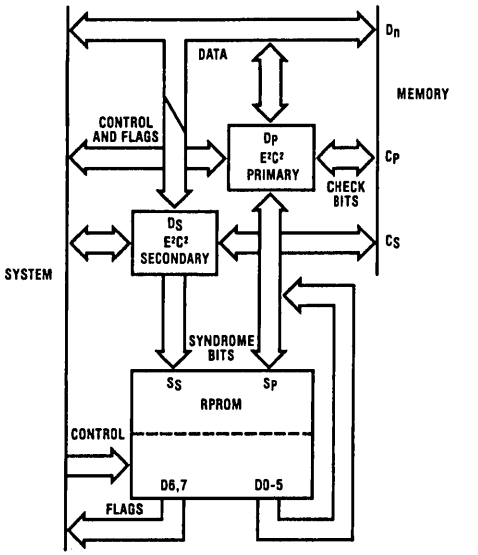

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FIGURE 7b

In fact, nearly all triple bit errors produce unique double syndrome words different from single and double bit errors. Those that do not produce unique double syndrome words, duplicate syndrome words of other single, double, and triple bit errors; however, these comprise only about 5 percent of the total. We can say, therefore, that this approach will correct not only all double bit errors, but will detect 95 percent of all triple bit errors. Note that with error correction systems utilizing the modified Hamming code, the majority of triple bit errors are interpreted as single bit errors and falsely corrected as such. It is up to the designer to determine the chances of three errors occurring in a memory location, and the (likely) consequences that they will be falsely corrected. If this condition is undesirable, then the Double Syndrome Decode Method offers greatly enhanced integrity; in fact, if the three errors detected do have a unique double syndrome word, they can be corrected. As stated, no presently used Modified Hamming code offers a unique double syndrome word for multiple errors; this is only possible with a Nelson code. This example was largely for 16 data bits, but the idea will work for other data widths.

In the 16-bit example, the RPROM has to output only six bits representing the syndrome bits of a bit in error. This leaves two spare bits which can be used as flags, and the user can program his RPROM accordingly. One solution is to use these flags to indicate the type of action required—whether to correct at all, correct once, or correct twice by wrapping around.

BLOCK DIAGRAM OF THE DP8400

This Application Note discusses first the single error correction, showing a simplified block diagram of the chip for both a write cycle to generate check bits, and a read cycle to detect errors and correct single bit errors.

The most important requirement when accessing memory is that these operations be performed with minimal memory delays. The DP8400, therefore, has been structured internally to minimize series propagation delays through the chip. A full block diagram of the DP8400 is shown, and first impressions are that there might be excessive delays in the various paths due to the additional blocks that have been added to the basic functional block diagram. In fact, this is not the case, because the DP8400 has been configured in bipolar Schottky logic and uses the AND-OR-INVERT gate in many of the blocks. This type of gate structure is used in multiplexers, Exclusive-OR gates and fall-through latches. It is possible, therefore, to combine these functions into one wide gate, reducing the propagation delays through some of these blocks to that of one gate. For example, the check bit output latch COL receives its input from an Exclusive-OR gate followed by a multiplexer. These three functions can be combined into one wide gate, and this greatly reduces the time taken to generate check bits.

THE DP8400—A VERSATILE ERROR CHECKER/ CORRECTOR FOR ALL APPLICATIONS

It was shown earlier how the DP8400 was able to detect single and double errors, and correct single errors. For 8- and 16-bit systems, these could easily be accomplished with a minimum of extra circuitry. The DP8400 can also be used in complex high integrity systems. In fact, investigations are still progressing as to its immense capabilities. It is the only error correction circuit capable of these features, and yet it still provides very fast throughput. For these reasons, the DP8400 should become the industry standard error correction chip for the foreseeable future.

DP8400s in 64-Bit Expansion

National Semiconductor
Application Note 308
Chuck Pham

The purpose of this Application Note is to provide memory designers with detailed information on the DP8400 parallel expansion method. This method allows fast check bit generation, error detection, and error correction. A thorough understanding of the 16-bit implementation is a prerequisite. Included in this note are the following: error correction expansion matrix; detailed steps for check bit generation, error detection and error correction; an example of a single error correction; and the detailed wiring diagram for the 64-bit configuration.

The Error Correction Expansion Matrix

For a 16-bit word, the DP8400 reads data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate six check bits from the 16 bits of data. This 16-bit matrix contains 16 unique syndrome patterns corresponding to each error location which allows the DP8400's Data Error Decoder (DED) to identify the data error location.

The DP8400 is easily expandable to other data configurations. For a 32-bit data word with seven check bits, two DP8400s are used. Three DP8400s can be used for 48 bits, four DP8400s for 64 bits, and five DP8400s for 80 bits, all with eight check bits. In order to expand the DP8400, additional check bits are required to provide the unique characteristic of the single data error syndrome. For expansion beyond 24 bits, check bits 6 and 7 (C6 and C7) are used. Note that these check bits can be configured to be always either zero or word parity, depending on the input voltage level of the Expansion Pin (XP). By rearranging all eight check bits (C0–C7) of each DP8400, we can obtain many different matrices that meet the above requirement. One of these is shown in Table I. For illustration, this matrix will be used throughout this application note to clarify the E^2C^2 expansion concept.

Check Bit Generation, Error Detection And Error Correction

CHECK BIT GENERATION (*Figure 1*)

In the Check Bit Generation mode, all four DP8400s are set to mode 0, normal write. The 64 bits of data from the system data bus are enabled into the Data Input Latches (DIL) of each DP8400. The individual Check Bit Generation (CG) of the four DP8400s then produce eight parity bits, or partial check bits, derived from the input data. (Note that all the syndrome input latches should be cleared so that only the partial check bits will pass through the Check Bit Output Latches/Buffers (COL and COB). In the normal write mode, the COBs are always enabled onto each check bit port. This allows the partial check bits to be combined externally in

TABLE I. Data Bit Error to Syndrome-Generate Matrix, 64-Bit Configuration

The partial code of device 0:

Error Locations (Data Bit Numbers)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7

The partial code of device 1:

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7

The partial code of device 2:

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0

The partial code of device 3:

48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C6
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C7

Check Bit Generation, Error Detection And Error Correction (Continued)

the eight 74S280s' parity generators/checkers to produce eight composite check bits. Table II. shows how these check bits are generated.

Table II. Composite Check Bits Generation

Ccomp. 0 = C(0)0 ⊕ C(1)1 ⊕ C(2)6 ⊕ C(3)4
Ccomp. 1 = C(0)1 ⊕ C(1)5 ⊕ C(2)3 ⊕ C(3)5
Ccomp. 2 = C(0)2 ⊕ C(1)6 ⊕ C(2)5 ⊕ C(3)3
Ccomp. 3 = C(0)3 ⊕ C(1)4 ⊕ C(2)4 ⊕ C(3)6
Ccomp. 4 = C(0)4 ⊕ C(1)3 ⊕ C(2)2 ⊕ C(3)2
Ccomp. 5 = C(0)5 ⊕ C(1)2 ⊕ C(2)7 ⊕ C(3)0
Ccomp. 6 = C(0)6 ⊕ C(1)0 ⊕ C(2)1 ⊕ C(3)1
Ccomp. 7 = C(0)7 ⊕ C(1)7 ⊕ C(2)0 ⊕ C(3)7

Notes:

Ccomp: composite check bit.

C(X)N: the partial check bit N of device X.

(Refer to Table I. for clarification).

To aid in fast error detection during memory read cycles, these composite check bits are complemented and written into memory along with the system data. If the system data has vacated the data bus, the Output Enables ($\overline{OB0}$ and $\overline{OB1}$) must be set low so that the original data word with its eight composite check bits can be written into memory.

DETECTION MODE (*Figure 2*)

In the Detection mode, again all the DP8400s are set to mode 0, normal write, then the partial check bits derived from the memory data bits are generated in a manner similar to that described for the check bit generation mode. These partial check bits are then associatively compared with the memory check bits in the eight 74S280s to produce eight external $\overline{\text{Composite Syndrome}}$ bits. As explained in the check bit generation mode, the composite check bits are complemented before being written into memory. This shows why complemented Composite Syndrome bits are produced instead of true composite syndromes. Then, if any bits on the $\overline{\text{Composite Syndrome}}$ bus go low, this will cause the 74S30 NAND gate to go high, giving the Any Error indication. If there is no error, all $\overline{\text{Composite Syndrome}}$ bits remain high. These $\overline{\text{Syndrome}}$ bits are also latched into the 74ALS533 Octal D-type Transparent Latch (with inverted output). The composite syndromes are then fed into the syndrome ports of the DP8400s in different combinations for each, for error-type determination and/or error correction.

CORRECTION MODE: (*Figure 3*)

Upon receiving the Any Error indication during the detection mode, it takes an additional step to determine the error type and to correct a single data error. All the DP8400s should be set to mode 7B (which is mode 7 with $\overline{OES}$ high), this mode enables the external syndromes directly to the Syndrome Generator (SG) and then the Data Error Decoder (DED) of each chip. For a single data error, the input syndrome will be unique for that error location; consequently, only one DP8400 can decode that error location and correct that bit. The other three do not indicate an error and do not change their data output latch contents. This corrected data can be output to the system data bus by means of $\overline{OB0}$ and $\overline{OB1}$. The DP8400 that decodes the data error location will indicate a single data error, while all others indicate a check bit error. If there was a single check bit error or a double bit error, then all the DP8400s will indicate a check bit error or a double bit error, respectively, through their error flags.

AN EXAMPLE OF A SINGLE DATA ERROR CORRECTION

Assuming all zero data is to be written into memory, we obtain the following set of partial check bits for all DP8400s:

C0 = 0 C4 = 0
C1 = 0 C5 = 0
C2 = 1 C6 = 0
C3 = 1 C7 = 0

Note that each DP8400 contains the basic 16-bit matrix (C0—C5). Therefore, the first six partial check bits are the same for all devices; only C6 and C7 are different. With the 64-bit configuration using the above 64-bit matrix, C6 = C7 = 0 (by connecting XP directly to V_{CC}) for the devices 0, 1, and 2; and C6 = C7 = word parity (by leaving XP pin floating) for the device 3. However, with all zero data, word parity is also zero (even parity). Therefore, the above partial check bits are obtained.

Using the formulas given in Table II, the composite check bits are as follows:

Ccomp. 0 = 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0
Ccomp. 1 = 0 ⊕ 0 ⊕ 1 ⊕ 0 = 1
Ccomp. 2 = 1 ⊕ 0 ⊕ 0 ⊕ 1 = 0
Ccomp. 3 = 1 ⊕ 0 ⊕ 0 ⊕ 0 = 1
Ccomp. 4 = 0 ⊕ 1 ⊕ 1 ⊕ 1 = 1
Ccomp. 5 = 0 ⊕ 1 ⊕ 0 ⊕ 0 = 1
Ccomp. 6 = 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0
Ccomp. 7 = 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0

Note that these composite check bits are complemented before they are written into memory. Thus, the memory check bits read later from memory are 1100 0101.

If an error has occurred in the data position 35 which is bit 3 of device 2, then the partial check bits C(3) N produced during the detection mode are as follows:

C(3)0 = 1 C(4) = 0
C(3)1 = 1 C(5) = 0
C(3)2 = 0 C(6) = 0
C(3)3 = 1 C(7) = 0

The partial check bits of other devices are unchanged. Consequently, the newly generated composite check bits (Ccomp) and the total syndrome bits are:

Bit #	Newly Generated Composite Check Bits		Memory Check Bits		$\overline{\text{Composite Syndrome}}$
0	0	⊕	1	=	1
1	1	⊕	0	=	1
2	0	⊕	1	=	1
3	1	⊕	0	=	1
4	0	⊕	0	=	0
5	1	⊕	0	=	1
6	1	⊕	1	=	0
7	1	⊕	1	=	0

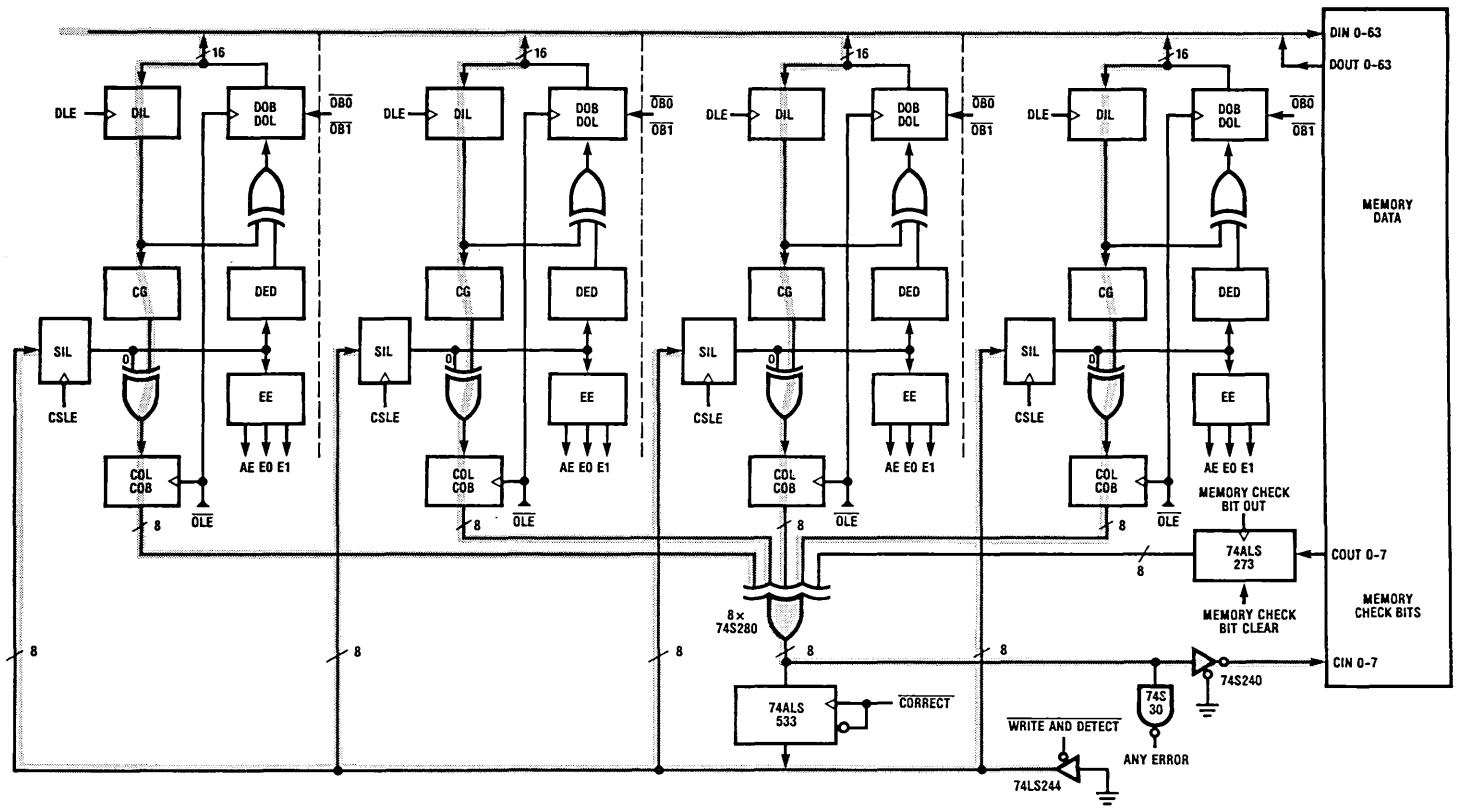

FIGURE 1. E²C² Simplified Block Diagram—64-bit Parallel Expansion, Check-Bit Generation

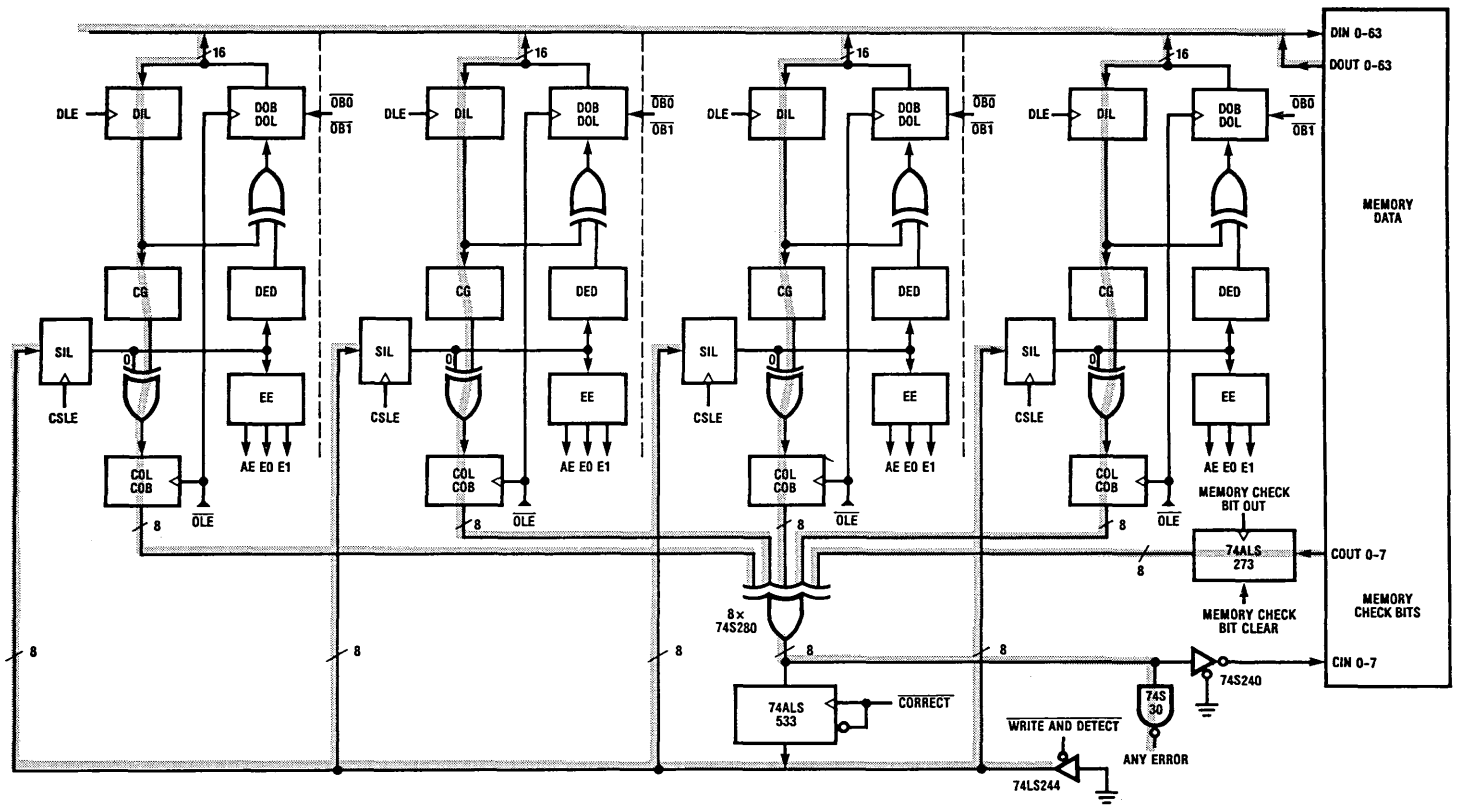

FIGURE 2. E²C² Simplified Block Diagram — 64-Bit Parallel Expansion, Error Detection

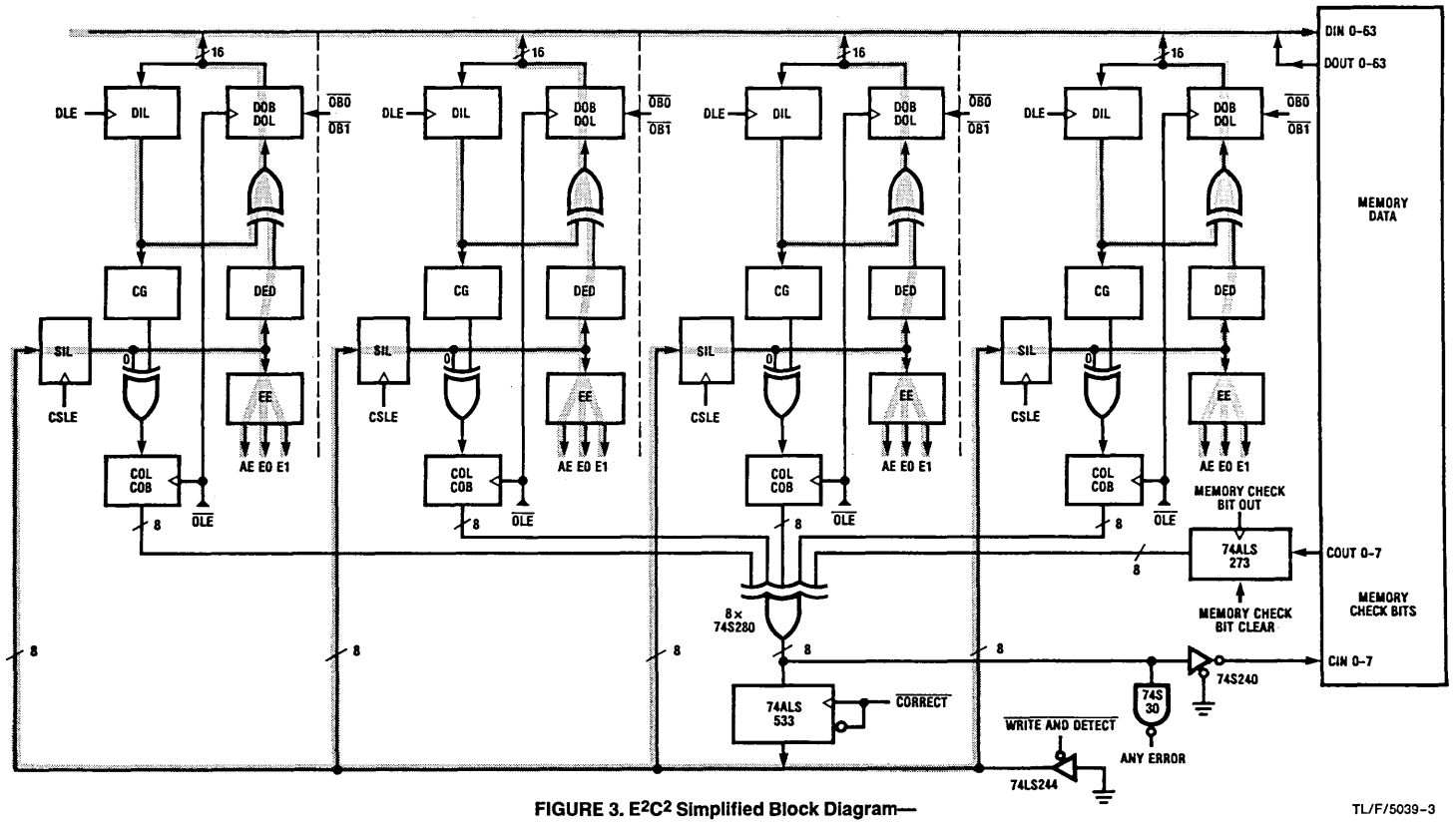

FIGURE 3. E²C² Simplified Block Diagram—64-Bit Parallel Expansion, Error Determination and Correction

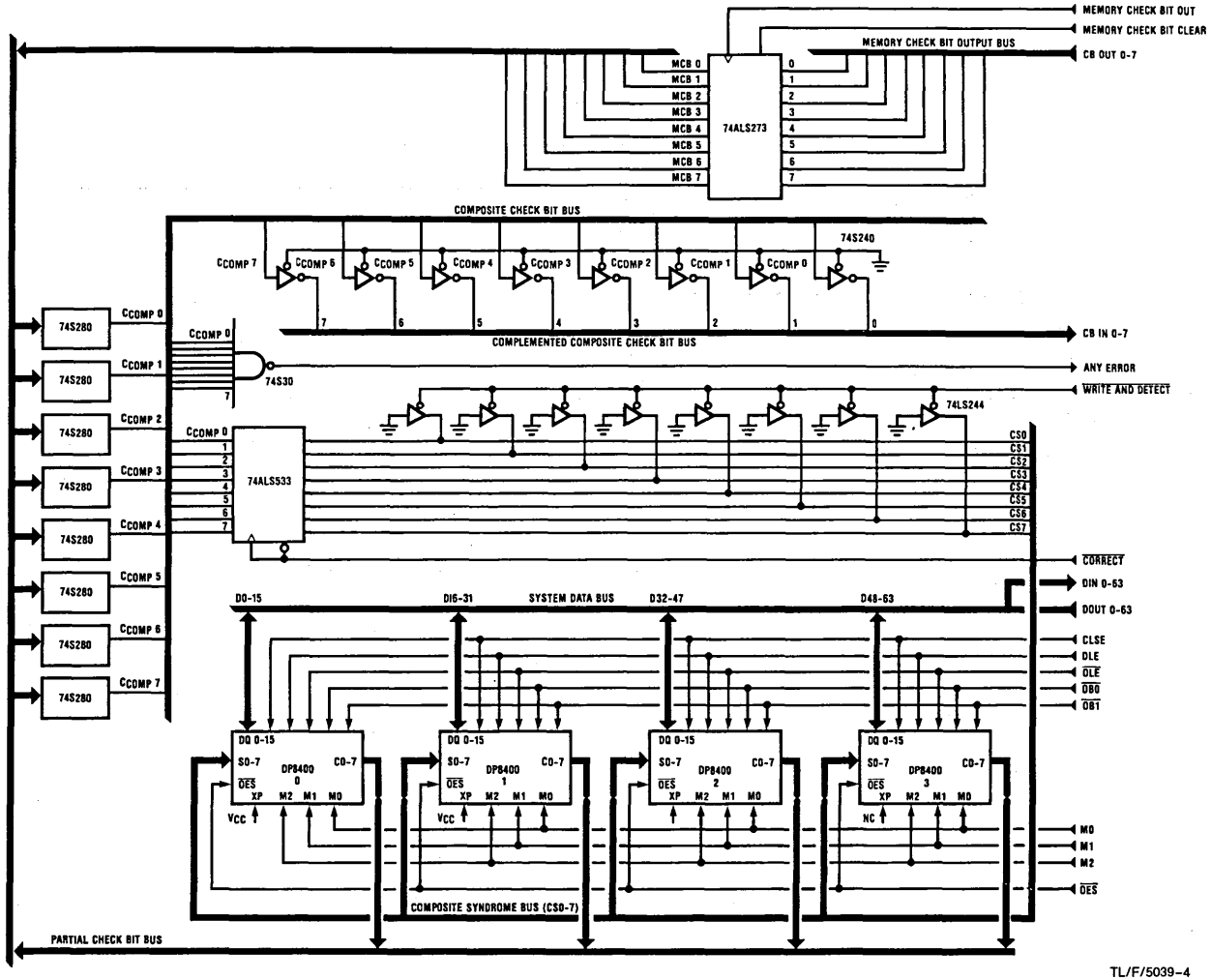

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FIGURE 4. E²C² 64-Bit Parallel Expansion, Detailed Block Diagram

Check Bit Generation, Error Detection And Error Correction (Continued)

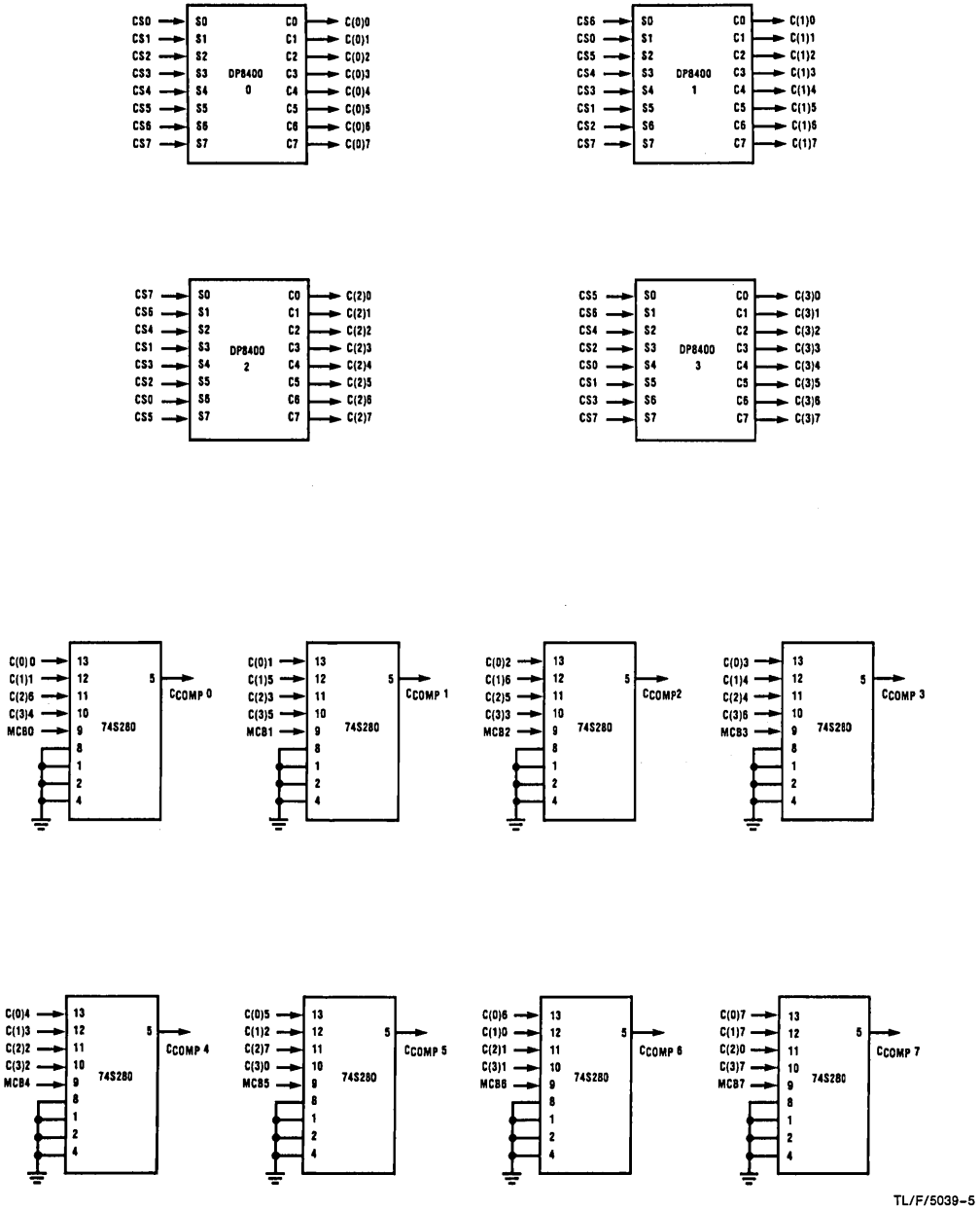

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FIGURE 5. E²C² 64-Bit Parallel Expansion

Check Bit Generation, Error Detection And Error Correction (Continued)

The composite syndrome 11010000 is that of the error location 35. Since the syndrome is unique and fed reordered to each DP8400, only device 2 will recognize this syndrome pattern and complement its data bit 3. Then the corrected data can be output to the system data bus when $\overline{OB0}$ and $\overline{OB1}$ of all four DP8400s go low. Devices 0, 1, and 3 all output the same data they received from memory. Only device 2 changes its (erroneous) data. Refer to *Figure 6* below for the timing diagrams of a memory write and memory read cycle (detect then correct).

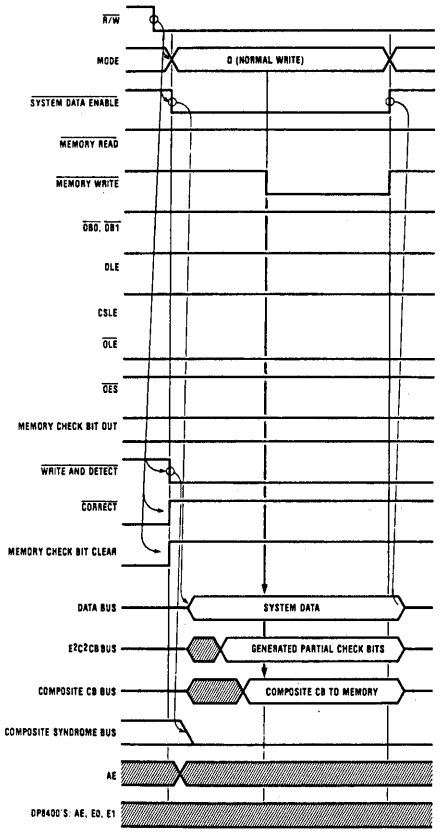

FIGURE 6A. E²C² 64-Bit Parallel Expansion Memory Write Cycle

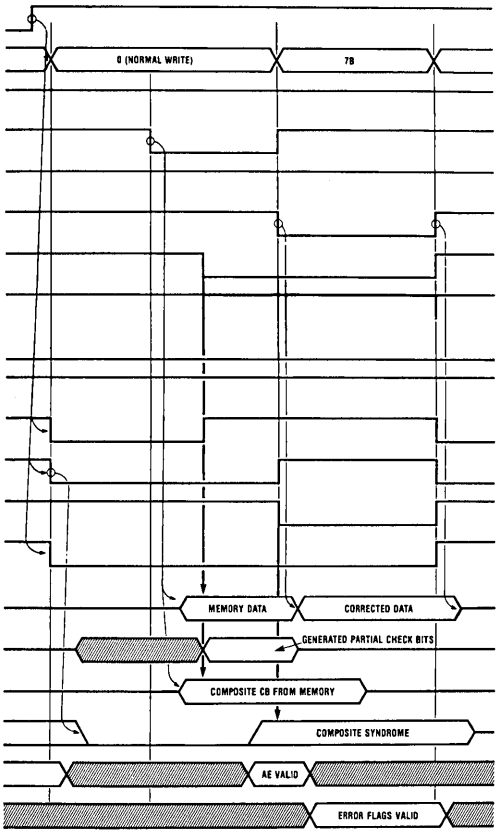

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FIGURE 6B. E²C² 64-Bit Parallel Expansion Memory Read Cycle (Detect Then Correct)

ERROR CORRECTION THE HARD WAY

A double complement correct cycle in an ECC system forms a sophisticated double-bit error correction and management system

by Bob Nelson

The use of parity, the most common error detection method, can be expanded from simple error detection in data words to the correction of single-bit errors by means of a double complement correct cycle. The double complement method can also be used to advantage in combination with error checking and correction systems to detect and correct hard and soft combinations of double-bit errors, provided no more than one of such errors is soft. In addition, this technique points the way to more sophisticated double-bit error correction and error management systems.

A parity bit is assigned a value of 1 or 0 on the basis of the number of 1s in the data word. The value of the parity bit depends on whether the parity system chosen is odd or even. Thus, in an odd parity system, the sum of the 1s in the data word and the parity bit will always be odd, whereas in an even parity system, the sum of the 1s in the data word and the parity bit will always be even (Fig 1). All examples in this discussion, except for those in Fig 1, use odd parity. A single parity bit can be used to detect a single-bit error occurring during a memory read cycle, and the technique can be expanded to provide even further error handling.

Parity error detection and correction

During a memory write, the parity bit which is created as a result of the data is written to the memory along with the data word for storage. When a read cycle occurs, parity generation is again performed on the data word, creating a new parity bit, which is then compared with the original parity bit read from memory. If a difference exists between the two parity bits, an error has occurred. Although this error cannot be located with the information given, and may have occurred in any bit location in the data word or even in the parity bit, if it is a hard error, its location can be determined through the use of additional memory cycles.

Data Word	Parity	Number of 1s	System
10001010	1	4	even
10001010	0	3	odd
01101001	1	5	odd

Fig 1 Odd and even parity. Value of parity bit is generated to satisfy chosen parity system (even or odd) so that sum of all 1s, including parity bit, will conform to even or odd parity system

If an error is detected during a memory read cycle, a simple procedure called the double complement method will determine if the error is hard, and, if so, correct it. The method includes a routine during which the suspect data and parity bit are complemented and presented to the same location in memory for a write cycle. Following the write, a read cycle is performed, and if the error is a hard error, the memory will repeat it by providing the data with the error bit complemented again. After a second complement, the data will be correct. At the end of such a correct cycle the memory contains the complemented data, and one additional write cycle must be performed to restore the data in memory (Fig 2).

During a double complement correct cycle involving a data word containing an even number of bit locations, the parity test is performed after the second read and before the second complement. If the error is hard, a parity error will once again be detected following the second read. If the error is soft, a parity error will not result following the second read. For data words containing an odd number of bit locations, parity testing

1st write	11010011	0	original data
1st read	11010111	0	PE (parity error)
D→$\overline{D}$	00101000	1	data are complemented
2nd write	00101000	1	complemented data
2nd read	00101100	1	PE (parity error)
$\overline{D}$→D	11010011	0	data are complemented

↑ hard error location

Fig 2 Hard error correction with parity. Single parity bit can be used to correct single-bit hard error with double complement method. On each memory read, original parity bit is read and new parity check is done on bits in data word. New parity bit is then compared with that read for validity

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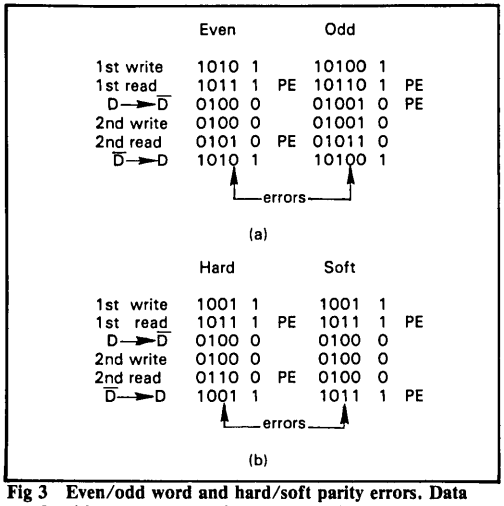

Fig 3 Even/odd word and hard/soft parity errors. Data words with even number of bits do not yield parity error on second read (a), nor soft error (b). Hard error, however, will be corrected

must be performed at different times during the correct cycle. In both cases, a double complement correct cycle can determine the type of error and, if it is hard, correct it (Fig 3).

If the bit in error is hard, the double complement correct can also be used to determine the bit's location in the data word. To do this, the data word and parity must be stored in a register when an error is detected. At the conclusion of the hard error correcting cycle, the location of the failing bit is determined by comparing the correct data with the contents of the register (Fig 4).

Thus, the use of a single parity bit not only makes it possible to deduce the error type, but also to locate and correct hard errors. This technique is useful for low cost terminal and word processing systems since, where retry is acceptable, the small amount of additional hardware

...the double complement method...also points the way to more sophisticated double-bit error correction and error management systems.

required can often eliminate the cost of an unscheduled service call. If a hard error can be detected, a double complement correct cycle will correct it, and the technique combined with an error checking and correction (ECC) system can also provide extended error correction capability when hard errors are involved.

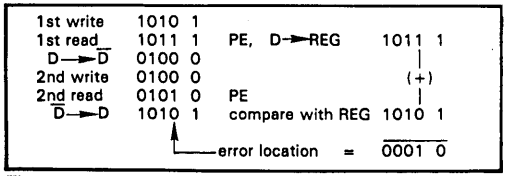

Fig 4 Locating hard errors with parity. Use of register for temporary storage enables double complement cycle to locate single hard error

ECC and double complement

The double complement method in combination with an ECC system can correct additional errors, both hard and soft. The ECC system under discussion here uses the code implemented by National Semiconductor in the DP8400 ECC device (Fig 5) to perform 1-bit error correction and 2-bit error detection. In an ECC system for 16-bit data words, such as the one discussed here, six parity bits are generated. Each of the parity bits is assigned a value as a function of the sum of the 1s in a unique combination of selected bits in the data word. Partial word parity bits in an ECC system are referred to as check bits. For simplicity, odd parity will be used in the examples, although in most ECC systems, including those implemented with the DP8400, a combination of odd and even parity is used to improve memory diagnostic capabilities.

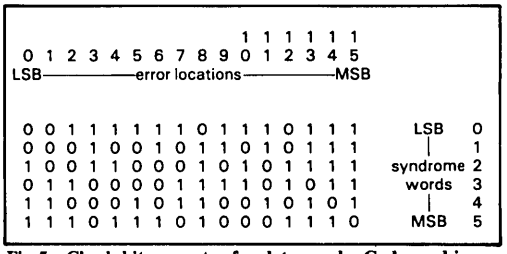

Fig 5 Check bit generator for data words. Code used is that implemented in National Semiconductor's DP8400 ECC device

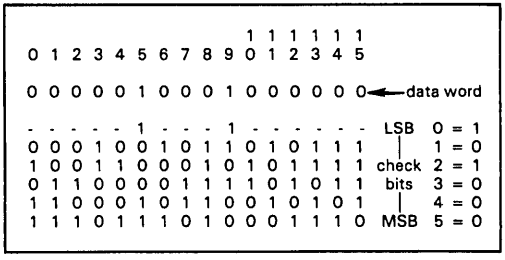

Fig 6 Error check bits are generated by presenting the data word to ECC code matrix and noting corresponding 1s. In first row, bits 5 and 9 correspond with 1s in matrix. Thus, to maintain odd parity LSB of check bits is set to 1

An ECC code forms a matrix (Fig 6) to which a data word can be presented for the generation of check bits. Given a data word, such as 0000010001000000, and the uppermost horizontal row of the matrix in Fig 7, check bit 0 is to be assigned a value based on the sum of corresponding 1s in that row and the data word. Using odd parity, the corresponding 1s in locations 5 and 9 dictate

Write	0000010001000000	000101	
Read	0000010001010000	000101	error in 11
Generate	0000010001010000	010110	new check bits
XOR check bits		010011	
			syndrome bits

Fig 7 Generating syndromes for locating error. Syndrome word is result of exclusive OR (XOR) of error check bits. No-error condition would result in syndrome word of all 0s

a value of 1 for the parity bit. For check bit 1, the selected location of correspondence is 9 only. Check bit 1 is assigned a value of 0 for odd parity. The complete set of check bits for this particular word is 000101 (05 HEX).

After check bit generation, the data and check bits go to the memory. During the read a new set of check bits are generated and compared against the check bits read from memory. The results of this check bit compare, an exclusive OR (XOR) function, are the syndromes (Fig 7). The single error indicating syndrome word is unique and is interpreted by the syndrome decoder to indicate the column in the matrix corresponding to the error location. The matrix or code is therefore a check bit generator for data, but a syndrome generator for error locations.

The...method in combination with an ECC system can correct additional errors, both hard and soft.

	5 9		
1st write	0000000000000000	110011	original data
1st read	0000010001000000	110011	2 errors
D→$\overline{D}$	1111101110111111	001100	complement
2nd write	1111101110111111	001100	
2nd read	1111101111111111	001100	hard error fixed
$\overline{D}$→D	0000010000000000	110011	complement
		000010	new check bits
		$\overline{110001}$	syndromes for bit 5

Fig 8 Correction of hard and soft errors. In the case of data word with one hard and one soft error, double complement method has corrected hard error and determined existence of soft error, which is then located by syndrome word and can be corrected

The check bits, or partial word parity bits, generated by modified Hamming codes and the code used in the DP8400, are also capable of providing complete error reporting. Since the single error reporting syndrome words contain an odd number of 1s and the total number of 1s is greater than one, 2-bit errors can easily be distinguished from a 1-bit or detectable triple-bit error. The DP8400 monolithic ECC device performs this error determination by counting the number of 1s in the error indicating syndrome words. When no error exists, the syndrome word contains no 1s, and when a single check is in error, a single 1 is present in the syndrome word. When an odd number of data bits are in error, the number of 1s in the syndrome word is odd and greater than 1 (3 or 5 in this example); if an even number of bits are in error, the syndrome word contains an even number of 1s greater than 0 (2, 4, or 6).

An ECC system implemented with the DP8400 can, at minimum, detect 100% of 2-bit errors; all of these errors are correctable if no more than one of them is soft. The device has complement write and read modes to allow the double complement correct technique to be used with no additional hardware, and other ECC devices can be used with additional components to implement the function.

In Fig 8, a soft error exists in location 5 and a hard error in location 9. During a memory read, the generated

The matrix or code is...a check bit generator for data, but a syndrome generator for error locations.

syndromes are the XOR of the single error that indicates syndrome words representing the error locations. 110001 (+) 001011 = 111010 [31 (+) 0B = 3A HEX]. Since a double error is indicated—an even number of 1s in the syndrome word—the data and check bits are complemented and placed in the output registers for presentation to the memory. After the memory write and subsequent read, the new data are complemented and stored in the data input latch. The error in location 5 remains in the data. A new set of check bits is generated from the data in the data input latch and compared with that in the check bit input latch, producing the syndrome word 110001 (31 HEX), which corrects the remaining error.

A detected double-bit error followed by a double complement correct cycle is properly reported as to initial error type. If the detected errors were both soft, for example, no change would occur in the data or check bit, and the ECC device error flags would again report a double-bit error. If, after the second read and complement, the error flags still report a single-bit error, the hard error (of a hard and soft combination) has been corrected and only the soft error remains. Of course, the single remaining error will be corrected in the normal manner by the ECC device. In the case of a double hard error, the error flags will report a no-error condition following the second read cycle, indicating that both errors were corrected and that the data are valid.

SIMPLIFICATION OF 2-BIT ERROR CORRECTION

Bit by bit, errors can be detected and eliminated through the use of an error matrix

by Bob Nelson

A computer-generated code, which generally obeys the rules attributed to the Hamming code and many of its variations, can be used to extend error detection and error correcting efficiency in an error checking and correction system. Such a code has been implemented by National Semiconductor on the DP8400, an expandable error checking and correction device packaged in a 48-pin dual inline package. The DP8400 can be used in a minimum hardware implementation of a 2-bit error correction system which will serve as an introduction to the rotational syndrome word generator, and also lead the way to expanding the error correcting capabilities even further.

Syndrome words

The code used in an error checking and correction (ECC) system designed to correct 1-bit errors and detect 2-bit errors for 16-bit data words may be viewed as a 16 x 6 matrix (Fig 1). The matrix describes the error locations and the syndrome bit positions so that the upper left bit of the matrix defines the least significant bit (LSB) for both the error locations and the syndrome bit locations. Each vertical column of the matrix contains the syndrome word (syndrome bits) for that error location in the data word. For any number of errors, the syndrome word generated by presenting the data word to the matrix is the exclusive OR (XOR) of the syndrome words defined by the error positions. To correct an error, the location of the error must be uniquely identified, and thus the 16 vertical columns must each be unique. A modified Hamming code generates a unique syndrome word for every possible data bit error location and hence may be referred to as a syndrome word generator.

Using syndrome words containing an odd number of 1s is the most common "modification" to the Hamming code. By ensuring that the syndrome words (vertical columns in the matrix) contain either three or five 1s, all applicable error conditions may be defined by counting the syndromes. The absence of a syndrome (ie, a syndrome containing all 0s and no 1s) indicates no error; an odd number greater than one (3 or 5 in this case) defines the location of a single-bit error. Any simultaneous double error will provide a syndrome word containing an even number of 1s greater than zero, while a single 1 in the syndrome word is indicative of a failure in the check bit portion of memory.

The rotational syndrome word generator described here also contains an odd number of 1s in each syndrome word. One additional characteristic common to both the Hamming code and most of its modified versions is that byte parity is an integral part of the matrix itself. However, the code implemented in the DP8400 ECC device and discussed here does not consider byte parity, or word parity, as a part of the code itself.

A 2-bit error correction system may be implemented in either of two ways. A code designed to allow 2-bit error correction may be used, or an existing single-bit error correct code may be extended by adding a second, different code which will ensure that each syndrome

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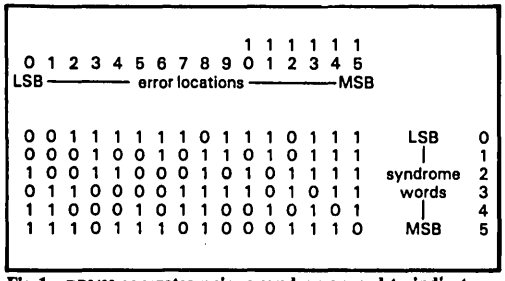

Fig 1 DP8400 generates unique syndrome word to indicate single-bit error position. Generated syndrome word containing all 0s means there is no error in data word.

word generated for any two error locations will be unique. Thus, a secondary, and different, 16 x 6 matrix connected to the primary matrix to form a 16 x 12 matrix will allow double-bit error correction if the XOR of the two 12-bit syndrome words produces a unique word for any two error locations.

Second matrix

The definition of an ECC matrix requires specifying a correspondence between error locations and syndrome words that defines the error location for each set of single-error syndromes. If a matrix is resequenced such that any error location corresponds to a syndrome word different from the original (primary) matrix, a second matrix has been created. For a 16-bit ECC matrix, 16!, or 2.092279 x 10^13, different codes exist. If a second code exists such that when it is combined with the first code (each containing the same syndrome words, but in a different sequence), a unique, larger syndrome word is generated for any two error locations, then an expandable code has been created (Fig 2).

The matrix, or code, used in the DP8400 device is defined such that if a second matrix, identical to the first but shifted by one bit position, is combined with the first, it would form just such a larger matrix. This matrix is fully rotational in that the secondary matrix need only be rotated, or shifted one error bit position to the left or right with respect to the primary matrix, to form larger, unique syndrome words regardless of the assigned correspondence of the primary matrix.

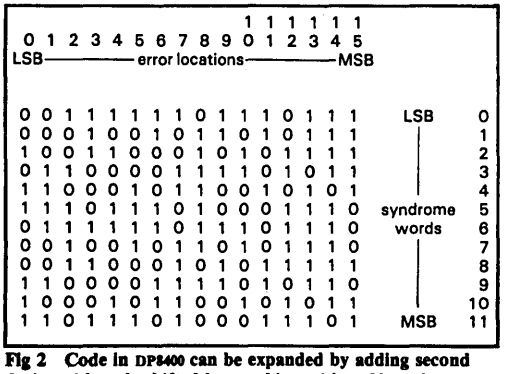

Fig 2 Code in DP8400 can be expanded by adding second device with code shifted by one bit position. Note that bottom six bits of each column are identical to top six bits in column to immediate right.

Implementation of this code in the DP8400 allows the data word size to be extended beyond 80 bits, using one device for each additional 16-bit word or portion thereof. The code function as a rotational syndrome word generator exists for all these defined word widths (Fig 3).

In addition to the rotational syndrome word generator, the DP8400 has two important features that permit an easy implementation of a 2-bit error correction system. During a memory read, the error indicating syndromes can be accessed directly by outputting them to the syndrome input/output (I/O) ports; syndrome can also be presented to the syndrome I/O ports to be XORed with the internally generated syndromes inside the DP8400. The internal syndrome decoder is provided with the result.

Error locations ⟶ 0 and 1
produce
HEX syndrome word ⟶ E34 (+) A78 = 44C
but
Error locations ⟶ 2 and 4
produce
HEX syndrome word ⟶ 1E9 (+) C65 = D8C

Fig 3 Unique syndrome is produced for each pair of error locations which is XOR of the locations. That syndrome can be decoded to identify pair in error.

If, for example, the internally generated 2-bit error syndromes are XORed with externally provided syndromes, representing one of the bits in error, the resulting syndromes representing the unknown error will be presented to the internal syndrome decoder. Once the unknown error is corrected, the data can be output to the data bus. The apparently correct data return zero syndromes (those containing all 0s) which, when XORed with the syndromes being injected, produce the syndromes representing the unknown error and present them to the syndrome decoder. This second error can then be corrected.

Using syndrome words containing an odd number of 1s is the most common "modification" to the Hamming code.

As described, the DP8400 is implemented for a 16-bit system. This "primary" ECC device will provide at its syndrome I/O pins the primary, or least significant six, syndrome bits of an extended matrix ECC system. A "secondary" ECC device is interfaced to the memory system with the data pin-to-system data bit correspondence rotated by one bit position, thus producing the extended matrix just described. The second device requires a second set of check bits; these secondary, or most significant six, syndrome bits are provided by the second DP8400.

The resulting 12-bit syndrome word can be externally decoded to provide the syndromes to be injected to effect 2-bit error correction. In system use, the externally decoded syndromes will be stored in a register. After the syndrome I/O port of the primary ECC device has been "turned around," the register outputs are enabled to allow syndrome injection.

Each of the DP8400 devices provides a set of error flags. Since each device maintains an independent check bit field in memory, errors occurring within a given check bit field are easily and quickly determined. If the errors, regardless of number, are confined solely to the check bit field of one of the devices, a no-error condition will be indicated.

The syndrome word generated by this system is unique for any combination of 2-bit data errors; both devices see an even number, greater than zero, of 1s in the syndrome word (Fig 4). For 2-bit errors involving one data bit and one check bit in either the primary or secondary check bit fields, the DP8400s report an even, greater than zero, and odd number of 1s in the syndromes; again, the syndromes are unique. The remaining type of 2-bit error, that in which both errors occur in either the primary or secondary check bit fields, produces its own unique syndrome word. However, since one DP8400 reports an even number of 1s in its syndrome word and the other reports all 0s, the data are known to be valid. In addition, in this particular 2-bit error correct system, nearly half of the 3-bit errors result in unique syndrome words and are therefore correctable as well.

Location/Error			Syndromes		Location/Error			Syndromes	
Data	Sec	Prim	Sec	Prim	Data	Sec	Prim	Sec	Prim
2	0	0	even	even	1	0	1	odd	even
1	1	1	even	even	2	1	0	odd	even
1	0	0	odd	odd	0	1	2	odd	even
0	1	1	odd	odd	1	1	0	even	odd
3	0	0	odd	odd	2	0	1	even	odd
1	0	2	odd	odd	0	2	1	even	odd
1	2	0	odd	odd					

Fig 4 Number and type of errors can be determined by looking at combination of even or odd numbers of 1s in the primary and secondary check bit fields.

Decoding the syndromes

A programmable read only memory (PROM) or electrically programmable read only memory (EPROM) is required as an external syndrome decoder for this 2-bit error correction system. The PROM address inputs are provided by the 12 syndrome bits generated by the two ECC devices. The least significant six bits of the PROM output byte provide, when required, the syndrome bits for subsequent injection into the primary DP8400. The remaining two bits of the PROM output byte provide flags defining the type of error and the contents of the six LSBs of the PROM output byte [Fig 5(a)].

The DP8400's error flags provide initial error determination; if an error that is not a single-bit error occurs, the external syndrome decoder will provide further error determination. Some types of error do not require syndrome injection and are referred to as "zero-pass" correctable errors. An example of such an error is one with a data bit and a secondary check bit in error. This type of error is corrected by the primary ECC device. An error type that requires "one-pass" correction is one with two data bits in error. In this case, syndromes representing a known error are injected into the DP8400, allowing correction of the unknown error. The remaining single error is then corrected.

The remaining error type, the "two-pass" error, can sometimes be a correctable 3-bit error. The syndromes representing a 2-bit error condition are injected, allowing correction of one error. The remaining 2-bit error produces a new set of syndromes which requires external (second-pass) decoding to produce a set of

MSB 7	6	5	4	3	2	1	LSB 0	
0	0	X	X	X	X	X	X	1 pass correctable
0	1	X	X	X	X	X	X	2 pass correctable
0	X	X	X	X	X	X	X	bits 0 to 5 = syndromes
1	0	X	X	X	X	X	X	not correctable
1	1	X	X	X	X	X	X	0 pass correctable
1	X	X	X	X	X	X	X	bits 0 to 5 <> syndromes

(a)

MSB 7	6	5	4	3	2	1	LSB 0	
1	X	X	X	X	X	X	1	primary check bit(s) in error
1	X	X	X	X	X	1	X	secondary check bit(s) in error
1	X	X	X	X	1	X	X	data bit(s) in error
1	X	X	0	0	X	X	X	1 bit in error
1	X	X	0	1	X	X	X	2 bits in error
1	X	X	1	0	X	X	X	3 bits in error
1	X	X	1	1	X	X	X	4 or more bits in error
1	1	0	X	X	X	X	X	output data from secondary ECC
1	1	1	X	X	X	X	X	output data from primary ECC

(b)

Fig 5 When a PROM is used as external syndrome decoder, its output byte can supply additional data about the error and how it is to be most efficiently corrected.

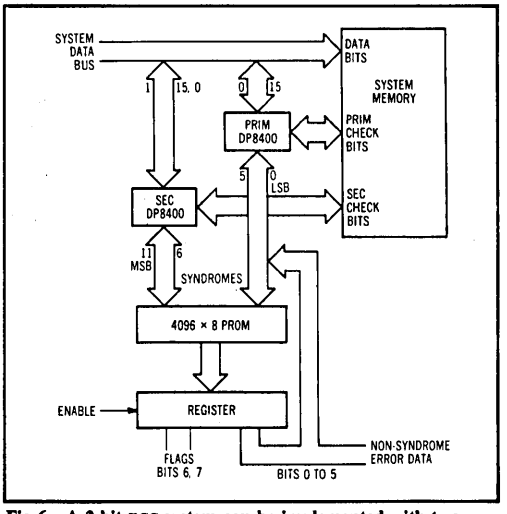

Fig 6 A 2-bit ECC system can be implemented with two DP8400s, a 4k-byte PROM for external syndrome decoding, and a register for temporary storage of syndromes error data. Note that the altered sequence of the lines from the secondary DP8400 reflects the bit rotation needed to expand the unique matrix.

```
3000 '*************************************************************************
3010 '***    'DC16AROM.BAS'        Bob Nelson - Sunnyvale CA - 9/15/81     ***
3020 '***    This program generates the syndrome decoder ROM code  for     ***
3030 '***    use in implementing a primary syndrome injection two  bit     ***
3040 '***    correction code generated by a single bit left   rotation     ***
3050 '***    of the secondary matrix.     The primary is a  Rotational     ***
3060 '***    Syndrome Generator as defined by National   Semiconductor     ***
3070 '***    in the DP8400.  The LPRINT routine may be replaced with a     ***
3080 '***    FILE generator or OUTP routine to facilitate the use of a     ***
3090 '***    PROM/EPROM programmer.....................................     ***
3100 '*************************************************************************
3110 '
3120 DEFINT A-Z:DIM SYND(16), PRI(16), ROM(4096,1)
3130 READ A:B=A:FOR C=0 TO 14:READ D:SYND(C)=D*64+A:PRI(C)=A:A=D
3140 NEXT:SYND(15)=B*64+A:PRI(15)=D
3150 DATA 52,56,41,7,37,49,35,25,62,11,13,19,44,55,47,31: 'NSC 80F/2 MATRIX
3160 ROM(0,1)=224:FOR A=1 TO 4095:ROM(A,1)=184:NEXT
3170 FOR A=0 TO 13:FOR B=A+1 TO 14:FOR C=B+1 TO 15                  '300 - 560
3180 AD=SYND(A) XOR SYND(B) XOR SYND(C):AE=PRI(A) XOR PRI(B)
3190 IF ROM(AD,1)=184 THEN ROM(AD,1)=AE+64 ELSE ROM(AD,1)=183
3200 NEXT:NEXT:NEXT
3210 FOR A=0 TO 14:FOR B=A+1 TO 15                                  '200 - 120
3220 AD=SYND(A) XOR SYND(B):ROM(AD,1)=PRI(A)
3230 FOR C=0 TO 5:P=2^C                                             '201 - 720
3240 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3250 IF (PRI(A) AND P)=0 THEN AF=PRI(A)+P+64 ELSE AF=PRI(A)-P+64
3260 IF ROM(AE,1)=184 THEN ROM(AE,1)=AF ELSE ROM(AE,1)=183
3270 NEXT
3280 FOR C=0 TO 5:S=64*2^C                                          '210 - 720
3290 IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
3300 IF ROM(AE,1)=184 THEN ROM(AE,1)=PRI(A) ELSE ROM(AE,1)=183
3310 NEXT:NEXT:NEXT
3320 FOR A=0 TO 15:AD=SYND(A):ROM(AD,1)=228                         '100 -  16
3330 FOR B=0 TO 5:P=2^B                                             '101 -  96
3340 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3350 ROM(AE,1)=205
3360 FOR C=B+1 TO 5:P=2^C                                           '102 - 240
3370 IF (AE AND P)=0 THEN AF=AE+P ELSE AF=AE-P
3380 IF ROM(AF,1)=184 THEN ROM(AF,1)=213 ELSE ROM(AF,1)=183
3390 NEXT:NEXT
3400 FOR B=0 TO 5:S=64*2^B                                          '110 -  96
3410 IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
3420 ROM(AE,1)=238
3430 FOR C=B+1 TO 5:S=64*2^C                                        '120 - 240
3340 IF (AE AND S)=0 THEN AF=AE+S ELSE AF=AE-S
3450 IF ROM(AF,1)=184 THEN ROM(AF,1)=245 ELSE ROM(AF,1)=183
3460 NEXT:NEXT
3470 FOR B=0 TO 5:P=2^B:FOR C=0 TO 5:S=64*2^C                       '111 - 596
3480 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3490 IF (AD AND S)=0 THEN AE=AE+S ELSE AE=AE-S
3500 FOR D=0 TO 5:E=2^D
3510 IF ROM(AE,1)=D THEN ROM(AE,1)=183:GOTO 3540
3520 IF ROM(AE,1)=184 THEN ROM(AE,1)=P
3530 NEXT D
3540 NEXT C:NEXT B:NEXT A
3550 FOR A=0 TO 5:FOR B=0 TO 5                                      '011 -  36
3560 AD=2^A+64*2^B:ROM(AD,1)=235
3570 FOR C=A+1 TO 5:AE=AD+2^C                                       '012 -  90
3580 IF ROM(AE,1)=184 THEN ROM(AE,1)=243 ELSE ROM(AE,1)=183
3590 NEXT
3600 FOR C=B+1 TO 5:AE=AD+64*2^C                                    '021 -  90
3610 IF ROM(AE,1)=184 THEN ROM(AE,1)=243 ELSE ROM(AE,1)=183
3620 NEXT:NEXT:NEXT
3630 FOR A=0 TO 5:AD=2^A:ROM(AD,1)=225                              '001 -   6
3640 FOR B=A+1 TO 5:AE=AD+2^B:ROM(AE,1)=233                         '002 -  15
3650 FOR C=B+1 TO 5:AF=AE+2^C                                       '003 -  20
3660 IF ROM(AF,1)=184 THEN ROM(AF,1)=241
3670 NEXT:NEXT:NEXT
3680 FOR A=0 TO 5:AD=64*2^A:ROM(AD,1)=226                           '010 -   6
3690 FOR B=A+1 TO 5:AE=AD+64*2^B:ROM(AE,1)=234                      '020 -  15
3700 FOR C=B+1 TO 5:AF=AE+64*2^C                                    '030 -  20
3710 IF ROM(AF,1)=184 THEN ROM(AF,1)=242
3720 NEXT:NEXT:NEXT
3730 B=0:C=0:FOR A=0 TO 4095:H$=HEX$(ROM(A,1)):       'LPRINT ARRAY
3740 B=B+1:C=C+1:IF LEN(H$)=1 THEN H$="0"+H$
3750 LPRINT USING "\   \";H$;:IF C<>16 THEN 3770
3760 C=0:LPRINT"  ";HEX$(A)
3770 IF B<>256 THEN 3790
3780 B=0:LPRINT:LPRINT
3790 NEXT
```

```
1000 '*************************************************************************
1010 '***     'DC16AMAP.BAS'        Bob Nelson - Sunnyvale CA - 9/15/81     ***
1020 '***     This program generates the syndrome maps for  a  primary     ***
1030 '***     syndrome injection implementation of a 16 bit  word  two     ***
1040 '***     bit error correct system utilizing a Rotational Syndrome     ***
1050 '***     Word Generator as implemented in the DP8400 by  National     ***
1060 '***     Semiconductor.   These maps are based on single bit left     ***
1070 '***     rotation of the secondary matrix.  The 'c' and 'd' notes     ***
1080 '***     in the maps denote  non-correctable  and  non-detectable     ***
1090 '***     three bit error conditions.............................      ***
1100 '*************************************************************************
1110 '
1120 DEFINT A-Z:DIM SYND(16),PRI(16),ROM(1132,1):P$="PRIMARY":S$="SECONDARY"
1130 READ A:B=A:FOR C=0 TO 14:READ D:SYND(C)=D*64+A:PRI(C)=A:A=D
1140 NEXT:SYND(15)=B*64+A:PRI(15)=D
1150 DATA 52,56,41,7,37,49,35,25,62,11,13,19,44,55,47,31: 'NSC 80F/2 MATRIX
1160 LPRINT "ONE DATA ERROR SYNDROME MAP":LPRINT
1170 FOR A=0 TO 15:LPRINT USING"##";A;:LPRINT"  ";:NEXT:LPRINT:LPRINT
1180 FOR A=0 TO 15:LPRINT HEX$(SYND(A));" ";:NEXT:LPRINT
1190 FOR A=1 TO 4:LPRINT:NEXT
1200 LPRINT"TWO DATA ERROR CORRECT SYNDROME MAP":LPRINT
1210 FOR A=1 TO 15:LPRINT USING"##";A;:LPRINT"   ";:NEXT:LPRINT:LPRINT
1220 FOR A=0 TO 14:FOR B=A+1 TO 15:AD=SYND(A) XOR SYND(B)          '200 - 120
1230 ROM(X,1)=AD:H$=HEX$(AD):IF LEN(H$)=2 THEN H$="0"+H$
1240 LPRINT H$;"  ";:X=X+1:NEXT B:LPRINT USING"###";A
1250 LPRINT TAB((A+1)*5+1);:NEXT A:FOR A=1 TO 4:LPRINT:NEXT
1260 FOR A=0 TO 5:S=64*2^A:FOR B=0 TO 5:P=2^B:FOR C=0  TO 15       '111 - 576
1270 AD=SYND(C):IF (AD AND P)=0 THEN AD=AD+P ELSE AD=AD-P
1280 IF (AD AND S)=0 THEN AD=AD+S ELSE AD=AD-S
1290 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT:A$=" "
1300 LPRINT"ONE DATA, ONE PRI, ONE SEC CHECK ERROR SYNDROME MAPS":LPRINT
1310 LPRINT:X=120:FOR A=0 TO 5:LPRINT"SECONDARY CHECK BIT";A:LPRINT
1320 FOR F=0 TO 15:LPRINT USING"##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1330 FOR B=0 TO 5:FOR C=0 TO 15:FOR E=0 TO 119
1340 IF ROM(E,1)=ROM(X,1) THEN A$="d":E0=E0+1:GOTO 1370 ELSE NEXT E
1350 FOR D=120 TO 695:IF D=X THEN D=D+1
1360 IF ROM(D,1)=ROM(X,1) THEN A$="c":E2=E2+1 ELSE NEXT D
1370 H$=HEX$ (ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1380 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING"####";B
1390 NEXT B:LPRINT:LPRINT:NEXT A
1400 LPRINT"576 ONE DATA, ONE PRI, ONE SEC CHECK errors are possible."
1410 LPRINT E0;"TWO DATA errors are not detectable.":LPRINT E2;
1420 LPRINT "ONE DATA, ONE PRI, ONE SEC CHECK errors are not correctable."
1430 LPRINT 100*((576-E0)/576):"PERCENT DETECT - ";
1440 LPRINT 100*((576-E0-E2)/576;"PERCENT CORRECT"
1450 FOR A=1 TO 4:LPRINT:NEXT:EA=E0:E0=0:EC=E2:E2=0
1460 X=0:FOR A=0 TO 15:AD=SYND(A):ROM(X,1)=AD:X=X+1:NEXT           '100 -  16
1470 FOR A=0 TO 5:P=2^A:FOR B=0 TO 5:S=64*2^B                      '011 -  36
1480 AD=P+S:ROM(X,1)=AD:X=X+1:NEXT:NEXT
1490 FOR A=0 TO 15:FOR B=A+1 TO 15:FOR C=B+1 TO 15                 '300 - 560
1500 AD=SYND(A) XOR SYND(B) XOR SYND(C)
1510 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1520 FOR A=0 TO 5:P0=2^A:FOR B=A+1 TO 5:P1=2^B                     '102 - 240
1530 FOR C=0 TO 15:AD=SYND(C):IF (AD AND P0)=0 THEN AD=AD+P0 ELSE AD=AD-P0
1540 IF (AD AND P1)=0 THEN AD=AD+P1 ELSE AD=AD-P1
1550 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1560 FOR A=0 TO 5:S0=64*2^A:FOR B=A+1 TO 5:S1=64*2^B               '120 - 240
1570 FOR C=0 TO 15:AD=SYND(C):IF (AD AND S0)<>0 THEN AD=AD+S0 ELSE AD=AD-S0
1580 IF (AD AND S1)=0 THEN AD=AD+S1 ELSE AD=AD-S1
1590 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1600 LPRINT"THERE DATA BIT ERROR SYNDROME MAPS":LPRINT:LPRINT
1610 X=52:A$="  ":FOR A=0 TO 13:LPRINT"DATA bit";A:LPRINT
1620 FOR D=A+2 TO 15:LPRINT USING"##";D;:LPRINT"   ";:NEXT:LPRINT:LPRINT
1630 FOR B=A+1 TO 14:FOR C=B+1 TO 15:FOR E=16 TO 51
1640 IF ROM(E,1)=ROM(X,1) THEN A$="d ":E0=E0+1:GOTO 1690 ELSE NEXT E
1650 FOR F=612 TO 1091
1660 IF ROM(F,1)=ROM(X,1) THEN A$="c ":E1=E1+1:GOTO 1690 ELSE NEXT F
1670 FOR G=52 TO 611:IF G=X THEN G=G+1
1680 IF ROM(G,1)=ROM(X,1) THEN A$="c ":E2=E2+1 ELSE NEXT G
1690 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1700 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING "###";B
1710 LPRINT TAB((B-A)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A
1720 LPRINT"560 THREE DATA BIT errors are possible.":LPRINT E0;
1730 LPRINT"ONE PRI, ONE SEC CHECK errors are not detectable.":LPRINT E1;
1740 LPRINT"ONE DATA, TWO PRI or TWO SEC CHECK errors are not correctable."
1750 LPRINT E2;"THREE DATA BIT errors are not correctable."
1760 LPRINT 100*((560-E0)/560);"PERCENT DETECT - ";
1770 LPRINT 100*((560-E0-E1-E2)/560);"PERCENT CORRECT"
1780 FOR A=1 TO 4:LPRINT:NEXT A:EA=EA+E0:EB=EB+E1:EC+EC+E2
1790 LPRINT"ONE DATA, TWO PRIMARY CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
1800 A$=" ":E0=0:E1=0:E2=0:FOR A=0 TO 4:LPRINT"PRIMARY check bit";A:LPRINT
1810 FOR F=0 TO 15:LPRINT USING "##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1820 FOR B=A+1 TO 5:FOR C=0 TO 15:FOR E=852 TO 1091
```

```
1830 FOR F=52 TO 611
1840 IF ROM(F,1)=ROM(X,1) THEN A$="c":E2=E2+1:GOTO 1860 ELSE NEXT F
1850 IF ROM(E,1)=ROM(X,1) THEN A$="c":E1=E1+1 ELSE NEXT E
1860 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1870 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING "####";B
1880 NEXT B:LPRINT:LPRINT:NEXT A
1890 LPRINT"240 ONE DATA, TWO PRIMARY CHECK errors are possible."
1900 LPRINT E1;"ONE DATA, TWO SECONDARY CHECK errors are not correctable."
1910 LPRINT E2;"THREE DATA BIT errors are not correctable."
1920 LPRINT"100 PERCENT DETECT - ";100*((240-E1-E2)/240);"PERCENT CORRECT"
1930 FOR A=1 TO 4:LPRINT:NEXT A:EB=EB+E1+E2:E1=0:E2=0
1940 LPRINT"ONE DATA, TWO SECONDARY CHECK ERROR SYNDROME MAPS":LPRINT
1950 LPRINT:FOR A=0 TO 4:LPRINT"SECONDARY check bit";A:LPRINT
1960 FOR F=0 TO 15:LPRINT USING "##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1970 FOR B=A+1 TO 5:FOR C=6 TO 15:FOR E=612 TO 851
1980 FOR F=52 TO 611
1990 IF ROM(F,1)=ROM(X,1) THEN A$="c":E2=E2+1:GOTO 2010 ELSE NEXT F
2000 IF ROM(E,1)=ROM(X,1) THEN A$="c":E1=E1+1 ELSE NEXT E
2010 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2020 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING "####";B
2030 NEXT B:LPRINT:LPRINT:NEXT A
2040 LPRINT"240 ONE DATA, TWO SECONDARY CHECK errors are possible."
2050 LPRINT E1;"ONE DATA, TWO PRIMARY CHECK errors are not correctable."
2060 LPRINT E2;"THREE DATA BIT errors are not correctable."
2070 LPRINT"100 PERCENT DETECT - ";100*((240-E1-E2)/240);"PERCENT CORRECT"
2080 FOR A=1 TO 4:LPRINT:NEXT A:EB=EB+E1+E2:A$="  ":C0=1:C1=64
2090 IF W=1 THEN P$="SECONDARY":S$="PRIMARY":C0=64:C1=1
2100 X=0:FOR A=0 TO 15:AD=SYND(A):FOR B=0 TO 5:P=C0*2^B        '101/110 -  96
2105 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
2110 ROM(X,1)=AE:X=X+1:NEXT B:NEXT A
2120 FOR A=0 TO 5:S=C1*2^A:FOR B=0 TO 15:FOR C=B+1 TO 15       '210/201 - 720
2130 AD=SYND(B) XOR SYND(C):IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
2140 ROM(X,1)=AE:X=X+1:NEXT C:NEXT B:NEXT A
2150 FOR A=0 TO 5:AD=C1*2^A:FOR B=0 TO 4:AE=AD+C0*2^B          '012/021 -  90
2160 FOR C=B+1 TO 5:ROM(X,1)=AE+C0*2^C:X=X+1:NEXT:NEXT:NEXT
2170 A$="  ":LPRINT"TWO DATA, ONE ";:LPRINT S$;
2180 LPRINT" CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
2190 X=96:E0=0:E1=0:E2=0:FOR A=0 TO 5:LPRINT S$;
2200 LPRINT" check bit";A:LPRINT
2210 FOR F=1 TO 15:LPRINT USING"##";F;:LPRINT"   ";:NEXT F:LPRINT:LPRINT
2220 FOR B=0 TO 14:FOR C=B+1 TO 15;FOR D=0 TO 95
2230 IF ROM(D,1)=ROM(X,1) THEN A$="d ":E0=E0+1:GOTO 2280 ELSE NEXT D
2240 FOR G=96 TO 815:IF G=X THEN G=G+1
2250 IF ROM(G,1)=ROM(X,1) THEN A$="c ":E2=E2+1:GOTO 2280 ELSE NEXT G
2260 FOR E=816 TO 905
2270 IF ROM(E,1)=ROM(X,1) THEN A$="c ":E1=E1+1 ELSE NEXT E
2280 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2290 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING"####";B
2300 LPRINT TAB((B+1)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A
2310 LPRINT"720 TWO DATA, ONE ";:LPRINT MID$(S$,1,3);
2320 LPRINT" CHECK errors are possible."
2330 LPRINT E0;"ONE DATA, ONE ";:LPRINT MID$(P$,1,3);
2340 LPRINT" CHECK errors are not detectable.":LPRINT E1;"TWO ";
2350 LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2360 LPRINT" CHECK errors are not correctable."
2370 LPRINT E2;"TWO DATA, ONE ";:LPRINT MID$(S$,1,3);
2380 LPRINT" CHECK errors are not correctable."
2390 LPRINT 100*((720-E0)/720);"PERCENT DETECT - ";
2400 LPRINT 100*((720-E0-E1-E2)/720);"PERCENT CORRECT"
2410 FOR A=1 TO 4:LPRINT:NEXT:EA=EA+E0:EB=EB+E1:EC=EC+E2
2420 LPRINT"TWO ";:LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2430 LPRINT" CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
2440 X=816:E0=0:E1=0:E2=0:FOR A=0 TO 5:LPRINT S$;
2450 LPRINT" check bit";A:LPRINT
2460 FOR F=1 TO 5:LPRINT USING "##";F;:LPRINT"   ";:NEXT F:LPRINT:LPRINT
2470 FOR B=0 TO 4:FOR C=B+1 TO 5
2480 FOR D=96 TO 815:IF ROM(D,1)=ROM(X,1) THEN A$="c ":E1=E1+1 ELSE NEXT D
2490 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2500 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING"##";B
2510 LPRINT TAB((B+1)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A:LPRINT"90 TWO ";
2520 LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2530 LPRINT" CHECK errors are possible.":LPRINT E1;"TWO DATA, ONE ";
2540 LPRINT MID$(S$,1,3);:LPRINT" CHECK errors are not correctable."
2550 LPRINT"100 PERCENT DETECT - ";100*((90-E1)/90);"PERCENT CORRECT"
2560 FOR A=1 TO 4:LPRINT:NEXT A:EA=EA+E0:EB=EB+E1:EC=EC+E2
2570 IF W=0 THEN W=1:GOTO 2090
2580 FOR A=1 TO 4:LPRINT:NEXT
2590 LPRINT"3290 THREE BIT ERRORS (all types) are possible."
2600 LPRINT EA;"of these errors cannot be detected."
2610 LPRINT EB+EC;"of these errors cannot be located."
2620 LPRINT 100*((3290-EA)/3290);"PERCENT DETECT - ";
2630 LPRINT 100*((3290-EA-EB-EC)/3290);"PERCENT CORRECT"
```

single-bit error syndromes. The error status at this point is that of a "one pass" error, and correction proceeds accordingly.

When a zero-pass error or a noncorrectable error occurs, the six LSBs from the PROM provide additional information. For example, a hexadecimal coded output from the PROM [Fig 5(b)] defines a 2-bit error in which one bit in error is a data bit and the other a primary check bit. The primary ECC device detects a 2-bit error while the secondary device detects only the data bit in error. Bit 5 of the PROM output directs the secondary device to output corrected data to the system. In most cases, bit 5 is a 1, and corrected data are output from the primary ECC device. Bits 0 through 4 of the PROM output define the error type and the number of bits in error (Fig 6) when the MSB (bit 7) is a 1. When the MSB is a 0, syndromes are required for correction, and bits 0 through 5 represent those syndromes.

Some types of error do not require syndrome injection and are referred to as "zero-pass" correctable errors.

The first of the two programs provided here is called "DC16AROM.BAS," and is a listing in hexadecimal representing the contents of the syndrome decoding PROM. The file may be presented to an output port for loading a PROM programmer if minor program changes are made. The second program, called "DC16AMAP.BAS," generates all the required syndrome maps, which include flags for all correctable 3-bit errors. These programs were written in Microsoft Basic and are compilable.

EFFORTLESS ERROR MANAGEMENT

Basic application of error management techniques is based on error history, including the double complement error correction cycle

by Bob Nelson

When implemented only in hardware, error management is generally limited to simple error logging. In most systems, error logging hardware is designed to capture the location of one error and use this information for maintenance purposes. In more sophisticated systems, however, software extends the error management function: after hardware obtains error information, data are accumulated on disk to expand storage capacity for information relating to error locations. Beyond the error information storage function of error management, which is useful for maintenance, some systems implement a correction procedure based on error history. If two errors occur in a memory word where an error has previously occurred, it is likely that both errors can be corrected. The basic error management system described in this article will provide a high correction rate for all 2-bit errors, except when two soft errors simultaneously occur in a memory word with no error history.

Error management system

The error management system comprises the central processing unit (CPU), the system memory, an error checking and correction (ECC) device, and an error management unit (EMU). The CPU is a 16-bit machine and requires commensurate memory. Actual memory, including the six check bits that the ECC device requires, is 22 bits wide. The ECC device is based on the DP8400 monolithic ECC unit manufactured by National Semiconductor. The EMU is a hypothetical device that can be implemented in hardware, partially or entirely, depending on system requirements.

The DP8400 provides several functions and features that allow easy implementation of a minimum hardware error management system. Error indicating syndrome words must be available to the EMU directly and syndrome injection capability must exist. (See "Simplification of 2-Bit Error Correction," Jan 1982, pp 127-136, for a discussion of the DP8400's syndrome input/output ports.) The DP8400 also provides the hardware required to perform a double complement correct cycle. Error flags must be provided to discriminate between 2-bit and detectable 3-bit errors; the DP8400 provides three such flags to include this function.

Vertical columns in the matrix shown in Fig 1 represent the single data bit error indicating syndrome words. A double data bit error syndrome word results from exclusive ORing (XOR) the two single-bit error indicating syndrome words that correspond to the bit locations in error. A detectable triple data bit syndrome word is any one of the ten syndrome words, not included as part of the matrix, which contains either three or five 1s. Syndrome words that represent check bit errors contain 1s in the syndrome word bit positions corresponding to the check bits in error, and 0s in the remaining bit positions. An error condition involving the data and check bit fields provides a syndrome word that represents the data bit(s) in error, XORed with a syndrome word representing the check bit(s) in error.

Error management unit

The EMU is memory intensive and uses memory in the form of an associative stack. Three fields constitute each of the 16 words in the stack: the 8-bit address field, which is the associative portion of the word; the 2-bit

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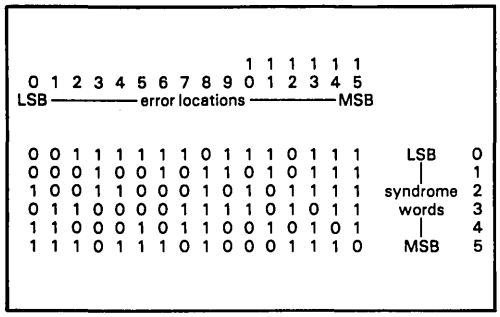

Fig 1 DP8400 syndrome word generator. Presenting errors to unique matrix produces syndrome words.

tag field; and the 6-bit syndrome field (Fig 2). The pointer addresses the stack. The EMU also contains a syndrome comparator, a temporary syndrome register, and a tag bit attribute register and comparator. The EMU monitors most ECC flags and provides flags of its own both to the ECC device and to the CPU; monitoring the memory address and comparing that address to the

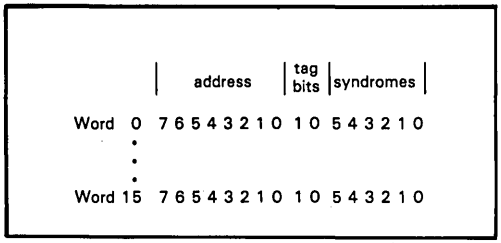

Fig 2 Associative stack organization. Of 16-bit address, eight address bits are most significant bits. Tag bits indicate type of error, and syndrome bits contain syndrome word.

stack's address field is a major function of the EMU. When the "stack full" flag is off, however, the number of words in the match area is limited by the location of the stack pointer. If a match occurs, ie, if the current memory address is an address at which an error occurred previously, the information obtained from the previous error can be used to correct more than one error bit. Each EMU function will be defined in a subsequent section of this article.

Single-bit error: first occurrence

Absence of a match, accompanied by single-bit error indicating flags, defines the first occurrence of such an error in the current address. The error may be in the data bit or check bit field of memory. Error address, tag bits (Fig 3), and single-bit error indicating syndrome word are stored in the EMU stack. Tag bits are assigned a value of 00, indicating a soft single-bit error. The stack pointer is then incremented and the ECC device corrects the single-bit error in the usual way. Stored syndromes contain an odd number of 1s. In Fig 4, data bit 5 fails at memory address 52 HEX, check bit 3 fails at address 45 HEX, and data bit 9 fails at address C7 HEX. Since the errors have not occurred previously at these addresses, they are given a tag bit value of 00. Logging errors should not impact the speed or function of the ECC system in performing single-bit error correction.

Tag Bits	Information Status
00	soft single-bit error
01	firm single-bit error
10	hard single-bit error
11	hard double-bit error

Fig 3 Tag bit field of stack indicates error type for more efficient processing by error management system. Tag bit field could be extended in other systems to provide more error information.

Double-bit error: first occurrence

When a double-bit error occurs at an address with no error history, the EMU exercises the only available option, a double complement correct cycle. As the ECC device enters the complement write mode, the syndrome word that represents the double-bit error condition is stored in the temporary syndrome register. Then the ECC system performs a double complement correct cycle to generate a second set of error flags. If two soft errors caused the initial indication of a 2-bit error, the second set of error flags will also indicate two errors and represent a noncorrectable condition. Any double-bit error situation other than that of two soft errors will produce error flags that indicate a correctable condition at the conclusion of the double complement correct cycle.

One hard and one soft

Error flags produced after the second complement of the double complement correct cycle indicate a single error if the initial error condition was one hard and one soft. At that point, the hard error will have been "corrected" and the remaining soft error indicated. The ECC device will generate a new single-bit error indicating syndrome word, which the EMU will XOR with the previously stored double-bit error indicating syndrome word. The result, which is the single-bit hard error indicating syndrome word, is stored in the stack.

To identify the bit as a single hard error, the tag bit field is set to a value of 10. After the error information is stored, the stack pointer is incremented. The ECC device corrects the single error in the usual manner. The remaining soft error may be either a check bit error or a data bit error. Fig 5 illustrates a soft error in data bit location 2 and a hard error in data bit location 11. A double complement cycle corrects the error in location 11. Representing the soft error, a new syndrome word is then XORed with the original syndrome word to produce

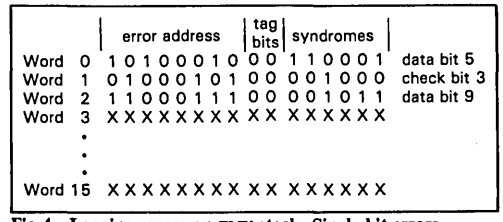

Fig 4 Logging errors on EMU stack. Single-bit errors occurring at addresses with no previous error history receive tag bit value of 00.

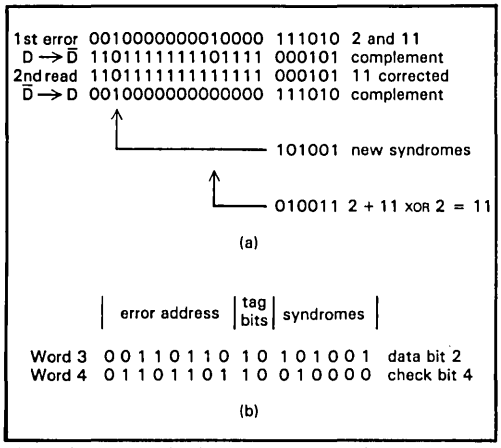

Fig 5 After correcting hard error in bit position 11 (a), system stores hard error syndrome on associative stack (b) and sets tag bit field to indicate single-bit hard error.

	error address	tag bits	syndromes	
Word 0	1 0 1 0 0 0 1 0	0 0	1 1 0 0 0 1	data bit 5
Word 1	0 1 0 0 0 1 0 1	0 0	0 0 1 0 0 0	check bit 3
Word 2	1 1 0 0 0 1 1 1	0 0	0 0 1 0 1 1	data bit 9
Word 3	0 0 1 1 0 1 1 0	1 0	1 0 1 0 0 1	data bit 2
Word 4	0 1 1 0 1 1 0 1	1 0	0 1 0 0 0 0	check bit 4
Word 5	1 0 0 0 0 1 0 0	1 1	1 0 1 0 0 0	2 hard
Word 6	X X X X X X X X	X X	X X X X X X	
•				
•				
•				
Word 15	X X X X X X X X	X X	X X X X X X	

Fig 6 Contents of EMU's stack containing initial occurrence of each error type.

the syndrome word that represents the hard error. These hard error syndromes are stored as shown in Fig 6, which also shows the storage of a hard check bit error at address 6D HEX.

Two hard

An ECC "no-error" flag, following a double complement correct cycle, indicates an initial error condition of two hard errors. Data following the second complement are correct; since no error exists, a syndrome word of all zeros is generated. The EMU will store the error address, the tag bits, and the contents of the temporary register. Tag bits will be given a value of 11, indicating a double-bit hard error. The stored syndrome word is then XORed with the contents of the temporary syndrome register and the new syndrome word from the ECC device (as with a one soft/one hard error condition), and the stack pointer is incremented. In this example, the information obtained from a double-bit hard error at address 84 HEX, including a syndrome word of 101000, is stored. A 2-bit error indicating syndrome word provides no information regarding the location of the errors. Errors in data bit locations 13 and 15, for example, produce the stored syndrome word as would errors in check bit locations 3 and 5. Fig 6 illustrates the contents of the associative stack portion of the EMU following the first occurrence of each type of error discussed. Word 5 in the stack represents the double-bit hard error.

Logging the errors

As errors occur at new addresses, error data are stored in the stack and the stack pointer is incremented. When information is entered in stack word 15 a "stack full" flag is set. The stack full flag directs the pointer to the lowest word address location in the stack containing the value 00 in the tag bit field. After storing data, the stack pointer goes to the next highest word address location that contains a 00 in the tag bit field. The stack contains the most recent error addresses at which single-bit soft errors occurred and all addresses at which firm or hard errors occurred. When no tag bit field contains 00, the "overflow" flag is provided and no additional stack storage occurs. However, logged error information is available to the system. One of the DP8400 modes, for example, allows data to be provided to the syndrome input/output ports and output through the data input/output ports, a capability that allows the error information to be dumped to the system disk for an additional level of storage. In another mode, the DP8400 can internally transfer data from the data input to the syndrome output, allowing the stack to be loaded from the system disk via the data bus.

Error locations are stored in real time by the logging procedure. Error resolution is defined by the correspondence of the memory address bits to the EMU address inputs. The EMU described here has eight address inputs that allow chip level error resolution in a 1M-byte memory system when 64k-bit dynamic random access memories are used. Since the EMU does not monitor the least significant eight memory address lines, error information—specifically the address and syndromes as stored in the EMU—represents a memory chip location. If a "read error" match occurs, only the tag bits and/or the stored syndrome word may be updated. Therefore, each unique error address can exist in a single stack location. Each stored word location defines one defective bit (chip) location if the syndrome word indicates a single-bit error. In some cases, the error information will represent two hard errors, which normally cannot be located.

Relocating the errors

In response to new error information, it may be desirable to change the error locations as defined by the syndrome words stored in the EMU. If a single-bit error is accompanied by an address match and tag bits representing a stored single-bit soft error, but if the syndrome comparison indicates that a different bit is in error, the syndrome field of the matching stack word should be changed to the new syndrome word. The ECC will correct the single-bit error in the normal manner, and the most recent soft error information for that memory address will be maintained. Previous soft error information can be off-loaded to a secondary storage device prior to the update.

Stored Error	Tags	Detected Error
1 bit, firm	01	1 soft, 1 hard
1 bit, hard	10	1 soft, 1 hard
1 bit, soft	00	1 soft, 1 hard
1 bit, soft	00	2 soft
1 bit, firm	01	2 hard
1 bit, hard	10	2 hard

Fig 7 Errors for syndrome injection in order of probability. Syndrome injection in the DP8400 allows faster correction than double complement method.

Maintenance help
Maintenance tools are a by-product of the EMU system. During the ECC procedure, error locations are identified and error types determined. EMU generated flags, which are provided when the stack contents reach a defined level, allow the error information to be offloaded to the system disk and the EMU to be cleared and reloaded with selected error information from disk. After the error information is loaded on disk, the system can be powered-down for maintenance. Following system power-up, suspect information about error location may be written to the EMU. This extended logging capability is part of the total error management system.

Redefinition
When a single-bit error occurs in a location at which a single-bit error has occurred previously, and the stored syndrome word is the same as the single-bit error indicating syndrome word generated by the ECC device, it may be necessary to redefine the error type. If the match provides tag information indicating a soft error (tag field = 00), the tag field will be changed to 01 to indicate a single-bit firm error. Such a redefinition is valid. For instance, a firm error may be an unproved hard error or an error-prone memory device sensitive to alpha particles, system noise, or both. Such an error can be treated as either a soft error or a hard error, or be given a definition based on the present error. For the purpose of this discussion, a firm error will be treated as a hard error.

With...double complement correct cycles, 100% of 2-bit errors can be corrected when...one of the errors is hard, regardless of...error history.

Although a soft error can occur in any given location within a chip, a second soft error is most likely to occur within the same chip. Error-prone chips are identified and tagged as firm error locations. In the EMU, both the syndromes and the address field are compared, providing higher error resolution within a word. In this EMU, the tag bit field is updated and the syndrome field is rewritten (if the second error is not in the same chip, the most recent single-bit error location in that word will be stored). The ECC device corrects the single-bit error in the normal manner.

Double-bit error: subsequent occurrence
When a double-bit error occurs and the EMU obtains a match, the contents of the tag bit field dictate the possible courses of action (Fig 7). If the tag bits are 11, for example, a double complement correct cycle is the only option. If the tag bits indicate a single-bit hard error location, a double complement correct cycle could be implemented. On the other hand, it is reasonable to assume that the stored syndrome word represents one of the two present error locations; in that case the error can be corrected without additional memory cycles.

One hard—one soft, one hard
If a match is obtained, tag bits are 10, and a 2-bit error has been detected, it is most likely that one error is soft and the other hard. Syndrome injection will obtain the fastest correction. The syndrome word in the stack, which usually represents the hard error location, is presented to the DP8400. There it is XORed with the internally generated syndrome word to provide the resulting soft error syndrome word, which is then presented to the syndrome decoder. After the ECC device corrects the soft error, it generates new check bits and zero syndromes. XORing the new syndromes with the still-injected hard error syndrome word, the unit decodes the hard error location and corrects the second error. This procedure allows correction of 2-bit errors without additional memory cycles, once the location of the hard error has been determined. Although a firm error is treated as a hard error, it must be given special consideration during system maintenance.

One soft—one soft, one hard
If a 2-bit error is detected and a match obtained with a tag of 01, the highest probability is that one error is soft and one is hard. The syndrome word from the stack is injected into the DP8400, where it is XORed with the internally generated syndrome word, providing the result to the syndrome decoder. Correcting the soft error, the ECC device generates new check bits and syndromes, XORs the new syndromes with the still-injected hard error syndrome word provided by the EMU, decodes the known error location, and corrects it. When the location of one error has been determined, this procedure allows high speed correction of 2-bit errors without additional memory cycles.

One soft—two soft
If a match is obtained, tag bits are 01, and a 2-bit error is detected, both errors are probably soft and can be corrected by syndrome injection. The syndrome word in the stack (which often represents one of the soft error locations) is presented to the DP8400, where it is XORed with the syndrome word, generated internally to provide the unknown soft error syndrome word to the syndrome decoder. Correcting the soft error, the ECC device generates new check bits and zero syndromes. XORing the new syndromes with the still-injected "known" soft error indicating syndrome word, it decodes the error location and corrects the second error. Thus, two soft errors can be corrected if the location of one is known.

One firm or hard—two hard
If two hard errors occur at an address where a single-bit hard error has been recorded previously, syndrome injection will usually accomplish the correction. The syndrome word in the stack, which most likely represents one of the hard error locations, is presented to the DP8400 where it is XORed with the internally generated syndrome word, providing the result to the syndrome decoder. The ECC device corrects the first error and generates new check bits and zero syndromes. XORing the new syndromes with the still-injected "known"

error indicating syndrome word, the unit corrects the second error. This procedure allows high speed correction of two hard errors when the location of one is known.

Double complement

The double complement error correction cycle is effective for locating hard errors in an error management system. This technique is effective when speed of error correction is of less concern than system integrity. Use of the double complement correct cycle following the detection of every error enhances error determination and correction. Immediate determination of single-bit hard errors improves the possibility that double-bit errors in the same defined address can be corrected. The next level of error detection and correction efficiency, using the double complement correct cycle for each detected error, includes those error types noted in Fig 8.

Stored Error	Tags	Detected Error
1 bit, soft	00	2 hard
1 bit, firm	01	2 soft
1 bit, hard	10	2 soft

Fig 8 Errors for double complement correction. When speed is of less priority, double complement method allows more precise error detection, logging, and correction.

One soft–two hard

A no-error indication from the ECC device following the double complement correct cycle will complete the definition of the error type—defined as a 2-bit error by the syndrome word stored in the temporary syndrome register—as a 2-bit hard error. If a match occurs but the tag bit field indicates a single-bit soft error, the tag bit field can be changed to 11, indicating two hard errors, and the syndrome field replaced with the contents of the temporary syndrome register. Error information can be offloaded to a secondary storage device before this update.

One firm or hard–two soft

If the ECC device generates error flags indicating a double-bit error at the conclusion of the double complement correct cycle, the 2-bit error that instigated the cycle remains and contains two soft errors. Since the only recorded error at the current memory location is hard, the errors are not recoverable and system operation terminates. In some systems, a firm error may be defined as a soft error, and data may be recovered. When offloading of soft errors is practiced, the disk or other storage mechanism can be interrogated for prior memory errors at the current address. These soft errors can be corrected if proper information is available.

Two hard–double error

When a match occurs and the tag bits indicate that an earlier 2-bit error has been recorded for the present memory address, ECC device's error flags identify the error type after the double complement correct cycle. If the present error is soft, system operation must be terminated—assuming that no additional relevant information regarding errors at this address is available from other sources. If the second set of error flags indicates that the present error is a 2-bit hard error, the errors can be corrected. Comparing the syndrome words in the temporary syndrome register and the stack will provide additional information. If the syndrome words do not match, three or four hard errors exist and system operation must be terminated.

Locating two hard errors

When the presence of two hard errors has been determined, a subsequent access at the same address will most likely indicate a single-bit error. If the single-bit error is in one of the two locations that had defined the previous 2-bit hard error, adequate information is available to locate the other error. The temporary syndrome register will store the single-bit error indicating syndrome word. Data are corrected by the double complement correct cycle, and the syndrome word in the stack can be replaced by the contents of the temporary syndrome register. The double-bit hard error indicating syndrome word can be offloaded and the word replaced. The new word will then be offloaded and XORed with the first syndrome word, keeping the result in the secondary storage element. Secondary storage is available for interrogation if additional errors occur in the same address. In more sophisticated error management systems, additional tag bits are made available in the EMU stack. One of these tag bits can be used to indicate that additional error information exists in secondary storage for that error address.

Summary

The simplified error management system presented here allows correction of double-bit errors if one of the errors has previously occurred. With the use of double complement correct cycles, 100% of 2-bit error correction is provided when at least one of the errors is hard, regardless of previous error history. Enhanced error logging is provided with error type determination capability. Maintenance aids are provided through the DP8400's bidirectional data transfer capability between the syndrome input/output and data input/output ports.

DP8400/8419 Error Correcting Dynamic RAM Memory System for the Series 32000®

National Semiconductor
Application Note 387
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INTRODUCTION

Three PAL's® (Programmable Array Logic devices) were used in this application in order to interface between the NS32016, DP8419 and the DP8400 to produce an error correcting memory system for the Series 32000 microprocessor family. The PAL Interface Controller (hereafter referred to as P.I.C.) takes care of all interfacing logic, no extra control logic is needed.

FEATURES

- The P.I.C. controls the following types of cycles:
  - A) READ cycles with no errors detected, ALWAYS CORRECT MODE (1 WAIT state inserted).
  - B) READ cycles with single error detected, the correct data will be written back to memory and given to the CPU. One WAIT state is inserted into the READ cycle and one WAIT state is inserted into the next access cycle (and the access is delayed) if it immediately follows the READ cycle.
  - C) READ cycles with more then one error detected. In this case the processor is interrupted and appropriate action can be taken.
  - D) WRITE cycles (no WAIT states).
  - E) BYTE WRITE cycles, or READ MODIFY WRITE cycles (3 WAIT states inserted). If more then one error is detected in the READ portion of this cycle the processor will be interrupted so appropriate action can be taken.
  - F) DRAM REFRESH cycles (may cause a maximum of 5 WAIT states to be inserted into an access cycle if the access occurs while the refresh is taking place).
- All single bit errors are automatically corrected and rewritten back to memory.
- All double bit errors are detected and cause a system interrupt.
- Can directly drive up to 2M bytes of Dynamic RAM (4 banks of 22 256k DRAMS, each bank being 16 data bits plus 6 check bits).
- The P.I.C. allows full use of the DP8400 and all its modes of operation, including:
  - A) The DIAGNOSTIC modes (can do a diagnostic test of the DP8400 without needing to use external memory).
  - B) The COMPLEMENT modes (useful for doing the DOUBLE COMPLEMENT METHOD to try to correct 2 errors).
- The P.I.C. interfaces between the DP8409A or DP8419 Dynamic RAM controller, the DP8400 Expandable Error Checker and Corrector, the NS32016 processor, the NS32201 Timing Control Unit, and the NS32082 Memory Management Unit (if used in the system).
- Provides outputs to interrupt the CPU and to insert WAIT states if needed.
- This interface uses PAL's whose equations and timing are given, allowing the user to customize the interface to his own requirements (even a different processor family) if he so desires.
- Can work at 10 MHz (using the new DP8419, DP8400-2, and common 120 ns 64k DRAMs). Operation at higher frequencies is possible.

DESCRIPTION

The P.I.C. consists of 3 PAL's and one 74LS164 parallel output serial shift register (see P.I.C. logic diagram). If greater speed is needed for the shift register (CPU clock speed is over 6 MHz) one could use some similar type of shift register in a faster type of logic ("AS, ALS, F"), or could make one out of D flip-flops (74AS174).

If one is using a CPU other then the Series 32000 and does not have a fast clock (FCLK, twice system clock frequency) he could substitute a 5 or 10 tap delay line for the shift register.

The P.I.C. uses a shift register as an aid in determining the state of the CPU and where it is in an access cycle. When either of the two outputs, "$\overline{\text{RASIN}}$" or "$\overline{\text{RFSH}}$", go true the shift register is enabled and begins producing a series of delays. These delays, along with specific signals from the CPU, are used in the interface to determine the state of the CPU and create the appropriate control signals for the DP8400, the DP8409A/DP8419, and the processor. Other CPUs should be able to customize this interface to their requirements by adjusting the appropriate equations.

The logic in the upper right hand corner of the P.I.C. logic diagram may not be needed (74LS374's, 74LS244, 74LS240's LED's and several SSI gates). The logic allows the latching of the DRAM bank (BA17, BA18), the syndrome (S0–S7), and the error flags (AE, E0, E1) during an error condition. The latched data will be displayed on the LED's (until the I/O RESET signal is applied) and can be read from the data bus by the CPU. The address in error could also be latched by this same logic, if desired.

The 2 input AND gate (U5) in the upper left of the P.I.C. logic diagram holds $\overline{\text{CS}}$ low until after $\overline{\text{RASIN}}$ goes high on the DP8409A/19. This is particularly useful for READ cycles with one ERROR where $\overline{\text{RASIN}}$ is extended beyond the end of the current cycle, perhaps into another access cycle.

In this application double bit errors, in the dynamic RAM, generate an interrupt to the CPU. All single bit errors are automatically corrected and rewritten back to memory.

During a SYSTEM RESET the internal flip-flops of PAL #1 are set to a refresh state by making the RESET input look like a refresh request (External logic was used to "NOR" the DP8409A/19 RFI/O input with a system RESET input to produce the PAL #1 RFI/O input).

The P.I.C. performs HIDDEN REFRESHES (CPU not accessing the Dynamic RAM controlled by the DP8409A, indicated by "/CS" being high) assuming a 4 "T" state processor access cycle.

The P.I.C. allows the full use of the DP8400 and all its modes of operation. For example, the DP8400 has excellent diagnostic capabilities included in modes "2" and "6". These modes allow one to perform a complete diagnostic test of the DP8400 without using the external memory. This is possible using an I/O port to control "M1 and M0" of the DP8400, along with the diagnostic control signals "DIAGCS and DIAGD" as follows:

1) The user can set the I/O signals "M1" and "DIAGCS" both high and perform a mode 2 DIAGNOSTIC WRITE to the DP8400 with user generated CHECK bits on the high byte of the data bus. The CHECK bits will be latched into the DP8400 (CSLE held low) until the user sets the I/O signal "DIAGCS" low.
2) The user can then set the I/O signals "M1" low and "DIAGD" high and perform a mode 0 WRITE, latching the user generated data in the DP8400 input latches (DLE held low).
3) Next, the user can perform a normal mode 4 READ. This will in effect be a diagnostic READ of the user generated data and check bits without using the external memory. In this way the DP8400 can be completely checked out during system initialization.
4) The syndromes, check bits, and error flags can also be read, provided $\overline{\text{ODLE}}$, $\overline{\text{OB0}}$, and $\overline{\text{OB1}}$ are low, using mode 6A or by reading the latches.
5) When the diagnostics are completed the user can return the DP8400 to normal functioning by resetting the I/O port outputs to the original DP8400 operating mode values ("M0, M1, DIAGCS, DIAGD" all low, and "$\overline{\text{I/O RESET}}$" high).

Using the I/O port signal "M0" the user could perform the DOUBLE COMPLEMENT METHOD to try to correct a DOUBLE bit error in the DRAM (see DP8400 data sheet for further information on the DOUBLE COMPLEMENT METHOD).

Another I/O port output, "I/O $\overline{\text{RESET}}$", allows the outputs "$\overline{\text{DOUBLERROR}}$" and "$\overline{\text{ERROR}}$" in PAL #3 to be reset. The signal "$\overline{\text{ERRLAT}}$" is used in this interface to latch the SYNDROME, DRAM bank, and ERROR flags during a CPU READ access with a single, double, or triple bit error. The CPU can READ these latched error signals by performing a memory READ from a specific memory location. (An OFF BOARD CHIP SELECT, "$\overline{\text{CS-OFFB}}$".) This READ will gate the latched error condition to the CPU data bus via the 74LS244 buffer and the signal $\overline{\text{SYNDROME-DATA}}$ (see the upper right hand corner of the P.I.C. controller logic diagram).

The PAL equations that follow are in the National Semiconductor PLAN™ format, which differs from the standard PALASM™ format.

EXAMPLE: PLAN FORMAT

"$\overline{\text{RASIN}}$:= RFSH * $\overline{\text{2D}}$ * ODLE"

This translates as, "$\overline{\text{RASIN}}$" is low after the rising edge of the input clock given that "$\overline{\text{RFSH}}$" was high and "2D" was low and "$\overline{\text{ODLE}}$" was high a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{RFSH}}$, and $\overline{\text{ODLE}}$ are outputs of the PAL and 2D is an input).

EXAMPLE: PALASM FORMAT

"RASIN := $\overline{\text{RFSH}}$ * $\overline{\text{2D}}$ * $\overline{\text{ODLE}}$"

The above expression means the same as the PLAN format expression except it is written in PALASM format. In other words "$\overline{\text{RASIN}}$" will go low after the rising edge of the clock given that "$\overline{\text{RFSH}}$" was high, "2D" was low and "$\overline{\text{ODLE}}$" was high a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{RFSH}}$, and $\overline{\text{ODLE}}$ are outputs and 2D is an input).

Depending on the Specific type of PAL's and logic used the user can calculate the speed requirements for the DRAM at the specified processor frequency as follows:

Here both "t_{RAC}" and "t_{CAC}" must be calculated and considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "t_{RAC}" and "t_{CAC}" parameters calculated.

EXAMPLE SYSTEM, 10 MHz, DP8400-2, DP8419, FAST "A" PART PALs

#1) $\overline{\text{RASIN}}$ low = T1 − 2 ns (F_{CLK} − PHI1 skew) + 15 ns ("A" PAL clocked output) = 100 − 2 + 15 = 113 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ low = 20 ns maximum (DP8419)

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ low = 80 ns (DP8419 $\overline{\text{RASIN}}$-$\overline{\text{CAS}}$ low maximum)

#4) 74F244 transceiver delay = 7 ns maximum

#5) DP8400-2 data setup time to "CSLE, DLE" = 10 ns maximum

#6) Minimum "CSLE, DLE" delay into "T3" = Minimum "A" PAL delay − minimum FCLK to PHI1 skew = 8 − 2 = 6 ns minimum

"t_{RAC}" = T1 + T2 + TW − #1 − #2 − #4 − #5 + #6
= 100 + 100 + 100 − 113 − 20 − 7 − 10 + 6
= 156 ns

"t_{CAC}" = T1 + T2 + TW − #1 − #3 − #4 − #5 + #6
= 100 + 100 + 100 − 113 − 80 − 7 − 10 + 6
= 96 ns

Therefore the DRAM chosen should have a "t_{RAC}" less than or equal to 156 ns and a "t_{CAC}" less than or equal to 96 ns. Standard 150 ns DRAMs meet this criteria.

Approximately 150 ns minimum RAS precharge time.

Approximately 200 ns minimum CAS precharge time.

Approximately 230 ns minimum RAS pulse width.

Approximately 180 ns minimum CAS pulse width.

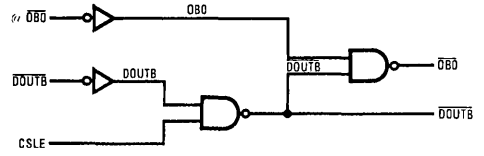
One must also consider the WRITE command to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lead times when choosing DRAMs for this system. During a READ access cycle, with a single bit error, a READ-MODIFY-WRITE access is performed. Here, the WRITE command to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lead times are one half period in length. This may present a problem to systems operating at frequencies of 10 MHz or greater. One can alleviate this problem by inserting an extra WAIT state into READ access cycles (see Use of P.I.C. at higher operating frequencies, #3) or by using external drivers from the PAL "WE" output to the DRAM "WE" input (thereby speeding up the $\overline{\text{WIN}}$ to $\overline{\text{WE}}$ delay and guaranteeing a greater $\overline{\text{WE}}$ to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lead time).

USE OF THE P.I.C. AT HIGHER FREQUENCIES

1) If one is using this interface above 4–6 MHz he should consider using the fast PAL's* (example "PAL16R8A" instead of "PAL16R8"), a fast shift register (example 74F164), external fast logic (such as "AS, ALS, or F" type 74XX series) or the faster "B" type PALs to produce outputs "$\overline{\text{DOUTB}}$, $\overline{\text{OB0}}$, $\overline{\text{OB1}}$" to the DP8400, and the new DP8400-2 error correction chip. The fast PAL's* have an input to output maximum time of 25 ns, and 15 ns if it is a registered output. The slow PAL's* have an input to output maximum time of 35 ns, and 25 ns if it is a registered output.

One needs to produce "$\overline{DOUTB}$, $\overline{OB0}$, $\overline{OB1}$" faster at higher CPU speeds to guarantee that the CPU reads valid data during a READ access cycle. To do this he could use external fast logic as shown in the following figure.

Using the above example we can calculate (assuming a 10 MHz 32000 series processor) the time required to have valid data at the CPU data input pins.



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@$\overline{OB1}$ would have the same configuration as $\overline{OB0}$

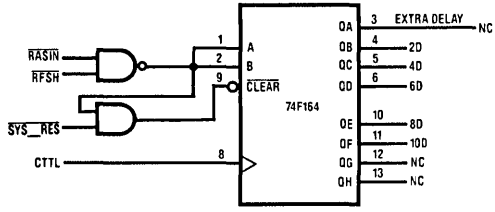
13 ns (maximum time of CSLE into state T3 assuming fast "A" PAL) +9 ns (maximum 74ALS00 propagation delay) + 9 ns (max 74ALS00 prop delay) +36 ns (maximum DP8400-2 "$\overline{OB0}$, $\overline{OB1}$" to output valid delay) + 7 ns (maximum 74F245 propagation delay) + 20 ns (data setup time required for the series 32000 with respect to the CTTL-clock) = 94 ns ***This value must not exceed 100 ns for a 10 MHz processor.

The delay of "$\overline{DOUTB}$" is to allow the DP8400 data, check bit and syndrome latches "DLE, and CSLE" to latch the data and check bits before turning off the DRAM output buffers.

The delay of "$\overline{OB0}$ and $\overline{OB1}$" allow the DRAM output buffers to turn off before the DP8400 starts driving the DP8400 memory data bus. In general the DRAM output buffers should turn off much faster then the DP8400 output buffers can turn on, so the user may want to allow "$\overline{OB0}$, $\overline{OB1}$" to become valid at the same time as "$\overline{DOUTB}$" transitions high.

2) In order to allow the use of slower DRAMs at higher CPU speeds one may want to slow down access cycles by adding an extra WAIT state.

To do this one could replace the 74LS164 IC with the following circuit:



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Here "CTTL" was used instead of "FCLK" with a 74F164.

The "$\overline{RFSH}$" PAL equation must be adjusted to keep "$\overline{RFSH}$" 5 clock periods long, as follows:

$\overline{RFSH}$: = $\overline{RFIO}$*INCY*$\overline{2D}$
+$\overline{RFSH}$*$\overline{RFIO}$
+$\overline{RFSH}$*$\overline{6D}$
+$\overline{RFSH}$*CTTL

If WAIT states are also wanted in WRITE access cycles the "$\overline{CWAIT}$" equations must include the following term:

+RFSH * $\overline{INCY}$ * $\overline{TSO}$ * DDIN * $\overline{2D}$

If one wants to keep WRITE cycles without WAIT states inserted then the "$\overline{RASIN}$" equations must be modified for HIDDEN REFRESH and WRITE cycles as follows:

+RFSH * $\overline{RASIN}$ * $\overline{INCY}$ * $\overline{2D}$

3) Another possibility for this interface at higher frequencies would be to adjust READ access cycles by adding another WAIT state to them, as well as adjusting BYTE WRITE cycles.

Using this method one would need another stage for the shift register or use a 74F164 and use CTTL as its clock instead of FCLK. If one looks at the above figure, using the 74F164, for reference the extra stage "10D" would be used. This would allow one to make the READ access cycle one "T" state longer by adjusting the READ and READ with error "$\overline{RASIN}$" equations.

To make the READ access cycle one "T" state longer another WAIT state would have to be added to READ cycles (making a total of 2 WAIT states) and the latch signals "$\overline{ODLE}$" and "CSLE" must be adjusted by delaying them back ½ "T" state (allowing a ½ cycle longer access time). This also has the advantage of allowing the other ½ cycle of time to get the data valid at the inputs of the Series 32000 CPU.

The BYTE WRITE access cycle could also be adjusted by delaying the signals "$\overline{ODLE}$" and "CSLE" by ½ cycle. No other equations need to be touched. This would allow an extra ½ cycle for access time during BYTE WRITE access cycles.

This would allow a standard 150 ns to possibly 200 ns DRAM in a 10 MHz system [80.5 ns + ½ "T" state (50 ns) = 130.5 ns column access time (t_{CAC})] but would sacrifice by having 2 WAIT states in READ access cycles.

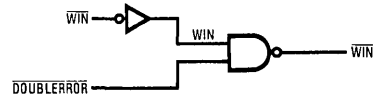
4) One also must be careful to make sure that $\overline{CS}$ is low, during an access, a minimum of 30 ns (DP8409A, 15 ns DP8419) before $\overline{RASIN}$ transitions low. If this is a problem one could tie $\overline{CS}$ permanently low (disabling hidden REFRESH) and use the system transceivers to select the memory system.

OTHER OPTIONS

If one is using the NS32082 Memory Management unit in a Series 32000 system he should connect the output "$\overline{PAV}$" (Physical Address Valid) to the P.I.C. instead of the address strobe output "$\overline{ADS}$".

An output for the BUS PARITY ERROR in a data transfer from the CPU to memory could also be detected, from the error flags and "AE" of the DP8400, and used to interrupt the CPU. However, the P.I.C. does not make use of that feature of the DP8400, though it would be very easy to add.

If one does not want to WRITE corrected data to memory in case of a DOUBLE BIT error, in READ access cycle, he could disable the WRITE signal, "$\overline{WIN}$", during a DOUBLE BIT error as follows:



TL/F/8400–3

NS32016, DP8400, DP8409A PALs Inputs and Outputs

PIN NUMBER OF THE PAL ON THE LEFT

PAL #1 Inputs

1)	"FCLK"	Fast Clock (twice "CTTL" frequency) from NS32201.
2)	"CTTL"	Output clock from NS32201.
3)	"$\overline{CS}$"	Chip Select for the Dynamic RAM controlled by the DP8409A and DP8400.
4)	"$\overline{DDIN}$"	Data Direction in, from NS32016, indicates the direction of the data transfer during a bus cycle.
5)	"RFIO"	Refresh request output from the DP8409A, also is used as a reset input to set PAL to a known state.
6)	"$\overline{INCY}$"	Output from PAL #2 indicating that the NS32016 is in an access cycle.
7)	"$\overline{AOHBE}$"	If address bit 0 and high byte enable (from NS32016) are both low this input is high. Used to determine when byte operations are in progress.
8)	"2D"	"RASIN" or "RFSH" delayed by 2 periods of FCLK. This output is from the external shift register.
9)	"$\overline{ERRLAT}$"	Output from PAL #3 indicating that any error, "AE", was valid during a READ access cycle.
11)	"$\overline{OE}$"	Enables PAL outputs.
12)	"4D"	"2D" delayed by 2 periods of RFCK, also an output of the external shift register.
18)	"6D"	"4D" delayed by 2 periods of RGCK, also an output of the external shift register.
19)	"8D"	"6D" delayed by 2 periods of RGCK, also an output of the external shift register.

PAL #1 Outputs

17)	"$\overline{RASIN}$"	Input to DP8409A
16)	"$\overline{RFSH}$"	Input to DP8409A, causes the DP8409A to enter mode 1 to do a refresh.
15)	"$\overline{WIN}$"	This output is used as an input to the DP8409A. It causes a WRITE to the DRAM.
14)	"$\overline{CYCLED}$"	This output is used in many other equasions and functions as a signal that the particular access cycle is midway to completion.

PAL #2 Inputs

1)	"$\overline{RFSH}$"	Output from PAL #1 that indicates whether the DRAMs are being refreshed.
2)	"$\overline{RASIN}$"	Output from PAL #1.
3)	"AO"	Output from NS32016, address bit 0.
4)	"$\overline{HBE}$"	Output from NS32016, high byte enable.
5)	"$\overline{DDIN}$"	Data Direction in, from NS32016.
6)	"$\overline{ADS}$"	Address strobe from NS32016.
7)	"$\overline{TSO}$"	Output from NS32016.
8)	"2D"	Output from the shift register.
9)	"$\overline{CS}$"	Chip select for the DRAM.
11)	"$\overline{CYCLED}$"	Output from PAL #1.
13)	"$\overline{ODLE}$"	Output Latch Enable to the DP8400 (Output from PAL #3).

PAL #2 Outputs

19)	"$\overline{PBUF1}$"	This signal enables the high byte of the processor, through the CPU transceiver, onto the DP8400/ Memory data bus.
18)	"$\overline{OB1}$"	Controls DP8400 output buffer for byte "1".
17)	"$\overline{OB0}$"	Controls DP8400 output buffer for byte "0".
16)	"$\overline{PBUF0}$"	This signal enables the low byte of the processor, through the CPU transceiver, onto the DP8400/ Memory data bus.
15)	"$\overline{DOUTB}$"	Controls memory buffers that interface between the DRAM and the DP8400 memory data bus.
14)	"$\overline{INCY}$"	Output indicating that the NS32016 is in an access cycle.
12)	"$\overline{CWAIT}$"	Output to NS32016 that causes WAIT states to be inserted into the NS32016 bus cycles.

PAL #3 Inputs

1)	"FCLK"	Fast clock from NS32201.
2)	"CTTL"	System clock from the NS32201.
3)	"DIAGCS"	Enable input from I/O port for diagnostics to enable "CSLE", check bit syndrome latch enable.
4)	"DIAGD"	Enable input from I/O port for diagnostics to enable "DLE", data latch enable.
5)	"$\overline{RESET}$"	Reset input from I/O port to reset PAL error latches.
6)	"CSRASIN"	Output from the PAL #1 logically "NOR"ed with the DRAM Chip Select signal. This indicates the beginning of a selected DRAM access cycle.
7)	"AE"	Output from DP8400 indicating an error.
8)	"E01"	This is the "E0" and "E1" error flags, of the DP8400, logically "NOR"ed together.
9)	"$\overline{DOUTB}$"	Controls memory buffers that interface between the DRAM and the DP8400/memory data base.
11)	"$\overline{OE}$"	Enables the PAL outputs.
12)	"$\overline{AOHBE}$"	If address bit 0 AND high byte enable (from NS32016) are both low this input is high. Used to determine when byte operations are in progress.
19)	"$\overline{DDIN}$"	Data Direction in, from NS32016.

PAL #3 Outputs

18)	"$\overline{ODLE}$"	Output that controls both the DP8400 Data latch and output latches. This output goes directly to both the "DLE" and $\overline{OLE}$ pin of the DP8400.
17)	"$\overline{CSLE}$"	Output that controls the DP8400 Check bit Syndrome latch. This output goes directly to the "CSLE" pin of the DP8400, it is only inverted so the PAL programmer will program it correctly.

NS32016, DP8400, DP8409A PALs Inputs and Outputs (Continued)

16) "$\overline{\text{MODECC}}$" Output that is used as an input to the DP8400. This signal controls whether the DP8400 is in READ or WRITE Mode.

15) "$\overline{\text{DOUBLERR}}$" Used to interrupt the system when a double bit error has been detected during a READ cycle.

14) "$\overline{\text{ERRLAT}}$" Used in the PAL controller to indicate that an error has occurred during a $\overline{\text{CS}}$ READ cycle or a $\overline{\text{CS}}$ BYTE WRITE cycle, as indicated by "AE" being valid. This signal can be used to latch the DRAM bank in error, the SYNDROME of the error, the ERROR flags, and the DRAM address (of the data in error) when a DRAM error occurs.

13) "$\overline{\text{ERROR}}$" This output is used to display the DRAM bank in error, the syndrome of the error, and the error flags of the DP8400 when a single, double, or triple bit error occurs. The preceding error condition is held in an external error register (74LS374's). The contents of the registers are displayed on LED's to help the user diagnose where a DRAM problem may reside in the memory system.

PAL NUMBER 1

```
PAL16R4A
FCLK CTTL /CS /DDIN RFIO /INCY /A0HBE 2D /ERRLAT GND
/OE 4D NC /CYCLED /WIN /RFSH /RASIN 6D 8D VCC
/RASIN : = RFSH*/INCY*/4D*/CTTL*ERRLAT          ;Start /RASIN
    +RFSH*/RASIN*/INCY*/4D                      ;WRITE or hidden RFSH
    +RFSH*/CS*/RASIN*/INCY*/DDIN*/6D            ;READ cycle
    +RFSH*/CS*/RASIN*/INCY*DDIN*/A0HBE*WIN      ;BYTE WRITE cycle
    +RFSH*/CS*/RASIN*/INCY*DDIN*/A0HBE*CTTL     ;Extend BYTE WRITE
    +RFSH*/CS*/RASIN*/DDIN*/ERRLAT*/8D          ;READ w/error

/RFSH : = /RFIO*INCY*RASIN                  ;RFSH in idle states or in long
       +/RFSH*/RFIO                         ; accesses of other devices or
       +/RFSH*/8D                           ; at the beginning of an access
       +/RFSH*CTTL

/WIN : =
     RFSH*/CS*/RASIN*/ERRLAT*6D*/CTTL*/DDIN     ;READ w/error
     +/WIN*RFSH*/RASIN*/ERRLAT*6D               ;READ w/error continue
     +RFSH*/CS*/RASIN*DDIN*2D*CTTL*A0HBE        ;WRITE
     +/WIN*RFSH*/CS*/RASIN*DDIN*2D*A0HBE        ;WRITE continue
     +RFSH*/CS*/RASIN*DDIN*/A0HBE*/CYCLED*/CTTL ;BYTE WRITE
     +/WIN*RFSH*/CS*/RASIN*DDIN*/A0HBE*6D       ;BYTE WRITE continue

/CYCLED : =
    RFSH*/RASIN*/CS*DDIN*4D*/A0HBE*/CTTL        :BYTE WRITE
    +RFSH*/RASIN*/CS*DDIN*/A0HBE*4D*/CYCLED     ;BYTE WRITE
    +RFSH*/RASIN*/CS*/DDIN*2D*/CTTL             :READ, READ w/error
    +RFSH*/RASIN*/CS*/DDIN*4D*/CYCLED           ;READ, READ w/error
    +RFSH*/RASIN*/CS*DDIN*2D*A0HBE              ;WRITE
    +RFSH*/RASIN*CS*2D*/CTTL                    ;HIDDEN REFRESH
    +RFSH*/CYCLED*/ERRLAT                       :Finish for READ w/error
    +RFSH*/CYCLED*CTTL                          ;Finish
```

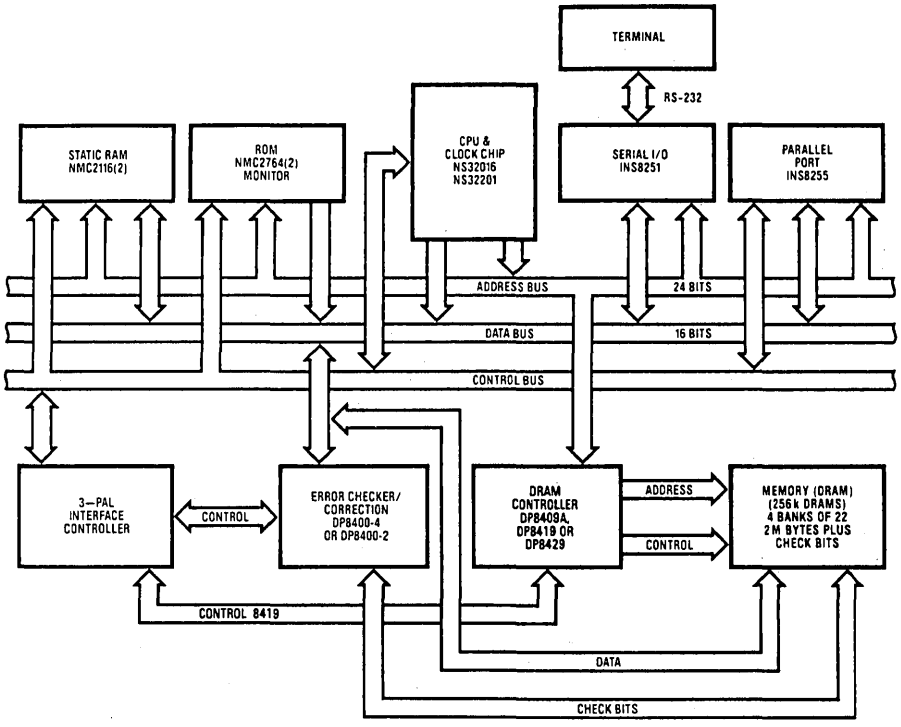
PAL NUMBER 2

```
PAL16L8A
/RFSH /RASIN A0 /HBE /DDIN /ADS /TS0 2D /CS GND
/CYCLED /CWAIT /ODLE /INCY /D0UTB /PBUF0 /0B0 /0B1 /PBUF1 VCC

IF (VCC) /PBUF1 =
   RFSH*/CS*/INCY*/DDIN*2D*/HBE                    ;READ or READ w/error
   +RFSH*/CS*/INCY*DDIN*A0*/HBE*D0UTB*/0DLE*2D     ;BYTE WRITE high
   +RFSH*/CS*/INCY*DDIN*2D*/0B0*A0*/HBE            ;BYTE WRITE cont
   +RFSH*/CS*/INCY*DDIN*/A0*/HBE*D0UTB             ;word WRITE

IF (VCC) /0B1 =
   RFSH*/CS*/INCY*/DDIN*2D*/CYCLED*D0UTB           ;READ or READ w/error
   +RFSH*/CS*/INCY*DDIN*/A0*HBE*2D*/0DLE*D0UTB     ;BYTE WRITE low
   +RFSH*/CS*/INCY*DDIN*/A0*HBE*2D*/0B1*D0UTB      ;BYTE WRITE cont
   +RFSH*/0B1*D0UTB*2D                             ;READ w/error hold

IF (VCC) /0B0 =
   RFSH*/CS*/INCY*/DDIN*2D*/CYCLED*D0UTB        ;READ or READ w/error
   +RFSH*/CS*/INCY*DDIN*A0*/HBE*2D*/0DLE*D0UTB  ;BYTE WRITE high
   +RFSH*/CS*/INCY*DDIN*A0*/HBE*2D*/0B0*D0UTB   ;BYTE WRITE cont
   +RFSH*/0B0*D0UTB*2D                          ;READ w/error hold

IF (VCC) /PBUF0 =
   RFSH*/CS*/INCY*/DDIN*2D*/A0                  ;READ or READ w/error
  +RFSH*/CS*/INCY*DDIN*/A0*HBE*D0UTB*/0DLE*2D   ;BYTE WRITE low
  +RFSH*/CS*/INCY*DDIN*2D*/A0*HBE*/0B1          ;BYTE WRITE cont
  +RFSH*/CS*/INCY*DDIN*/A0*/HBE*D0UTB           ;word WRITE

IF (VCC) /D0UTB =
    RFSH*/CS*/INCY*/DDIN*2D*CYCLED              ;READ or READ w/error
    +RFSH*/CS*/INCY*DDIN*/A0*HBE*2D*0DLE*0B1    ;BYTE WRITE low
    +RFSH*/CS*/INCY*DDIN*A0*/HBE*2D*0DLE*0B0    ;BYTE WRITE high

IF (VCC) /INCY = RFSH*/ADS*/2D*CYCLED       ;Start INCY
      +RFSH*/CS*/TS0*/2D                    ;Start INCY for access
                                            ; after forced refresh
                                            ; or READ w/error
      +RFSH*/INCY*CYCLED                    ;Continue
      +RFSH*/INCY*/TS0*/CS                  ;Continue for /CS access

IF (/CS) /CWAIT =
    /RFSH*/TS0                              ;Access in RFSH
    +RFSH*/TS0*RASIN                        ;Access after forced RFSH
    +RFSH*/INCY*/TS0*/DDIN*/2D              ;READ cycle
    +RFSH*/INCY*/TS0*DDIN*/A0*HBE*CYCLED    ;BYTE WRITE
    +RFSH*/INCY*/TS0*DDIN*A0*/HBE*CYCLED    ;BYTE WRITE
    +RFSH*/TS0*/CYCLED*/2D*RASIN            ;WAIT after READ w/error
```

PAL NUMBER 3

```
PAL16R6A
FCLK CTTL DIAGCS DIAGD /RESET CSRASIN AE E01 /DOUTB GND
/OE /AOHBE /ERROR /ERRLAT /DOUBLERR /MODECC /CSLE /ODLE /DDIN VCC

/ODLE : = CSRASIN*/DDIN*/DOUTB*/CTTL                ;Read
        +CSRASIN*/DDIN*/MODECC*CSLE*ODLE            ;Read with error
        +CSRASIN*DDIN*/AOHBE*/DOUTB*/CTTL           ;Byte Write
        +/ODLE*CSRASIN*DDIN*/AOHBE*CTTL             ;Continue during Byte Write
        +CSRASIN*DDIN*/AOHBE*/MODECC*CSLE*ODLE      ;Byte Write
        +CSRASIN*DDIN*AOHBE*/CTTL                   ;Word Write
        +/ODLE*CSRASIN*CTTL                         ;Hold "/ODLE"
        +/ODLE*DIAGD                                ;Hold "/ODLE" for
                                                    ;  diagnostics

/CSLE : = CSRASIN*/DDIN*/DOUTB*/CTTL                ;Read
        +CSRASIN*/DDIN*/MODECC                      ;Read with error
        +CSRASIN*DDIN*/AOHBE*/DOUTB*/CTTL           ;Byte Write
        +CSRASIN*DDIN*/AOHBE*/MODECC                ;Byte Write
        +CSRASIN*DDIN*AOHBE*/CTTL                   ;Word WRITE
        +/CSLE*CSRASIN*CTTL                         ;Hold "/CSLE"
        +/CSLE*DIAGCS                               ;Hold "/CSLE" for
                                                    ;  diagnostics

/MODECC :=
    CSRASIN*/ODLE*/DDIN*/CTTL          ;READ or Write w/error
   +CSRASIN*/ODLE*DDIN*/AOHBE*/CTTL    ;BYTE WRITE
   +CSRASIN*DDIN*AOHBE                 ;WORD WRITE
   +/MODECC*CSRASIN                    ;Hold "/MODECC"

/DOUBLERR :=
  /DIAGCS*/DIAGD*RESET*CSRASIN*/ODLE*/CTTL*AE*E01  ;Double bit error
                                                   ;  during READs
                                                   ;  or BYTE WRITEs
  +/DOUBLERR*RESET                                 ;Hold "/DOUBLERR"

/ERRLAT :=
    /DIAGCS*/DIAGD*CSRASIN*/ODLE*/CTTL*AE       ;Any Error during
                                                ;  READ or BYTE WRITE
    +/ERRLAT*CSRASIN                            ;Continue "/ERRLAT" during
                                                ;  READ or during BYTE WRITE

/ERROR  :=  /DIAGD*/DIAGCS*RESET*CSRASIN*/ERRLAT ;Store error syndrome
                                                 ;  and RAS bank and
                                                 ;  error flags
             +/ERROR*RESET                       ;Hold until RESET

;The output, "/CSLE", is shown inverted so the PAL will be
;programmed correctly, in other words, "/CSLE" goes low after the
;rising edge of FCLK given that one of its input equations was
;low a setup time before FCLK transitioned high. The output,
;"/CSLE", should go straight to the pin "CSLE" of the DP8400.
```

DP8400, DP8409A, NS32016 Error Correcting Dynamic RAM Computer System



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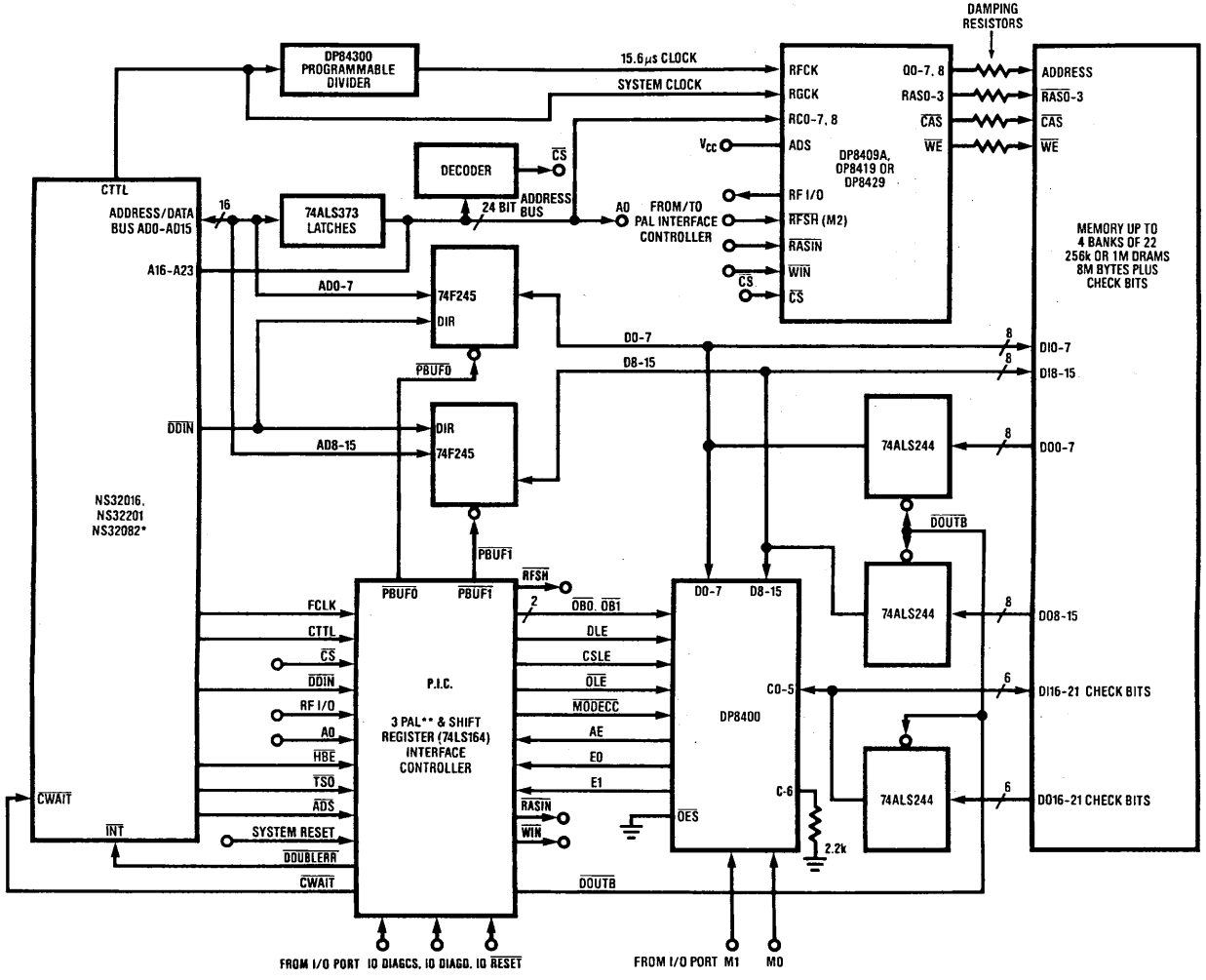
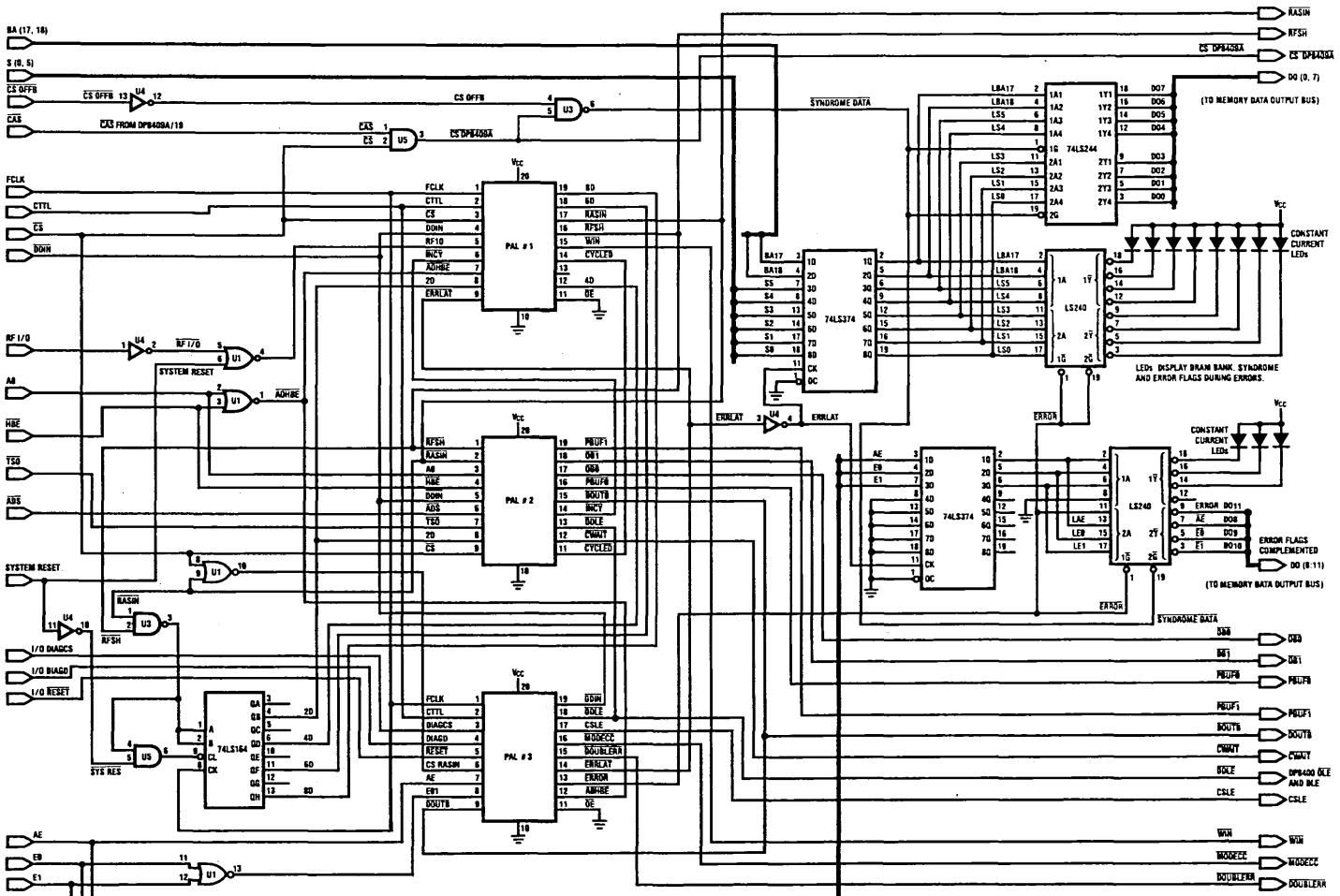
NS32016, DP8400, DP8409A or DP8418 Error Correcting Memory System



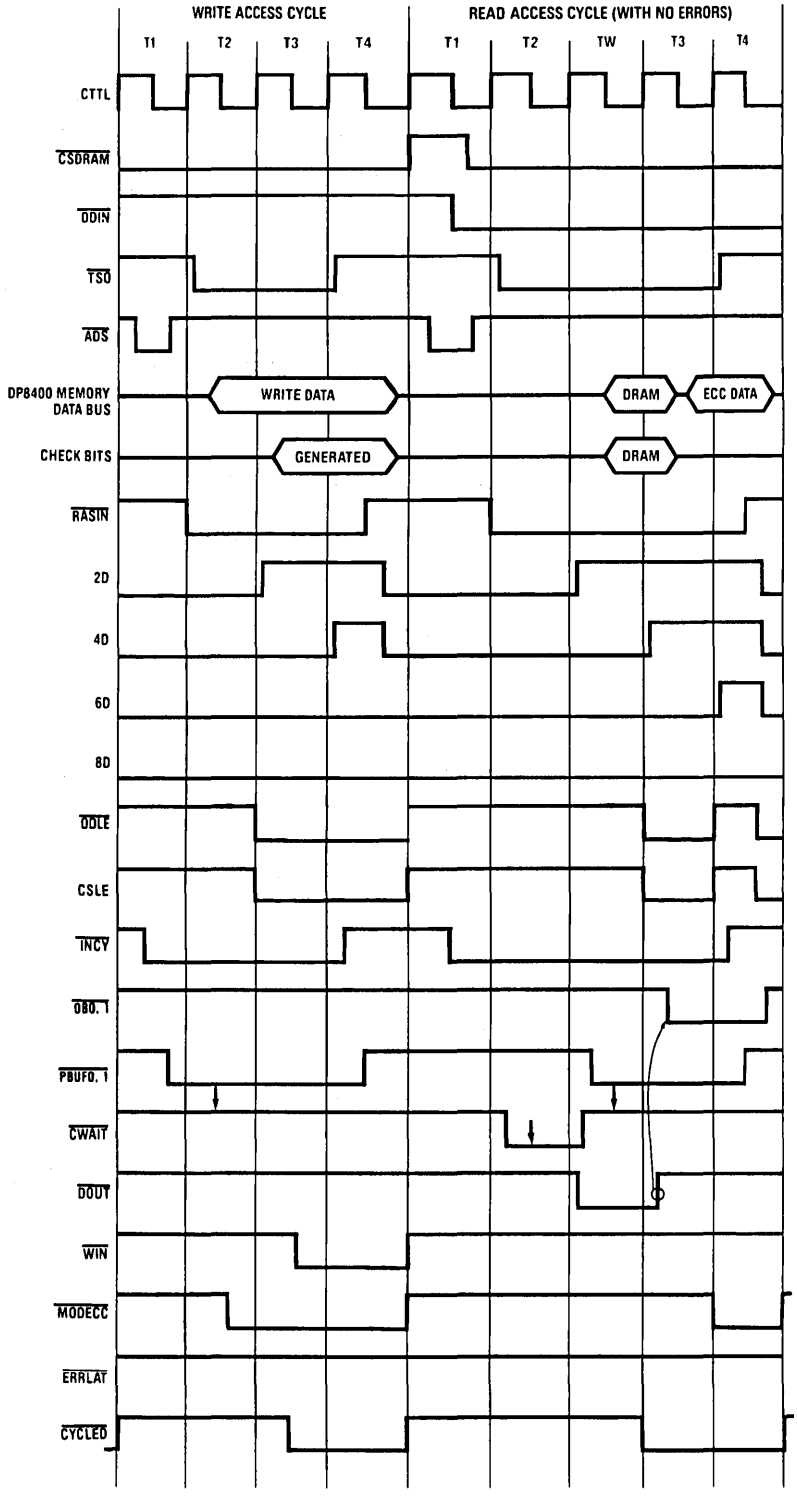
TL/F/8400–5

*IF system contains NS32082 MMU $\overline{PAV}$ should be used in place of $\overline{ADS}$

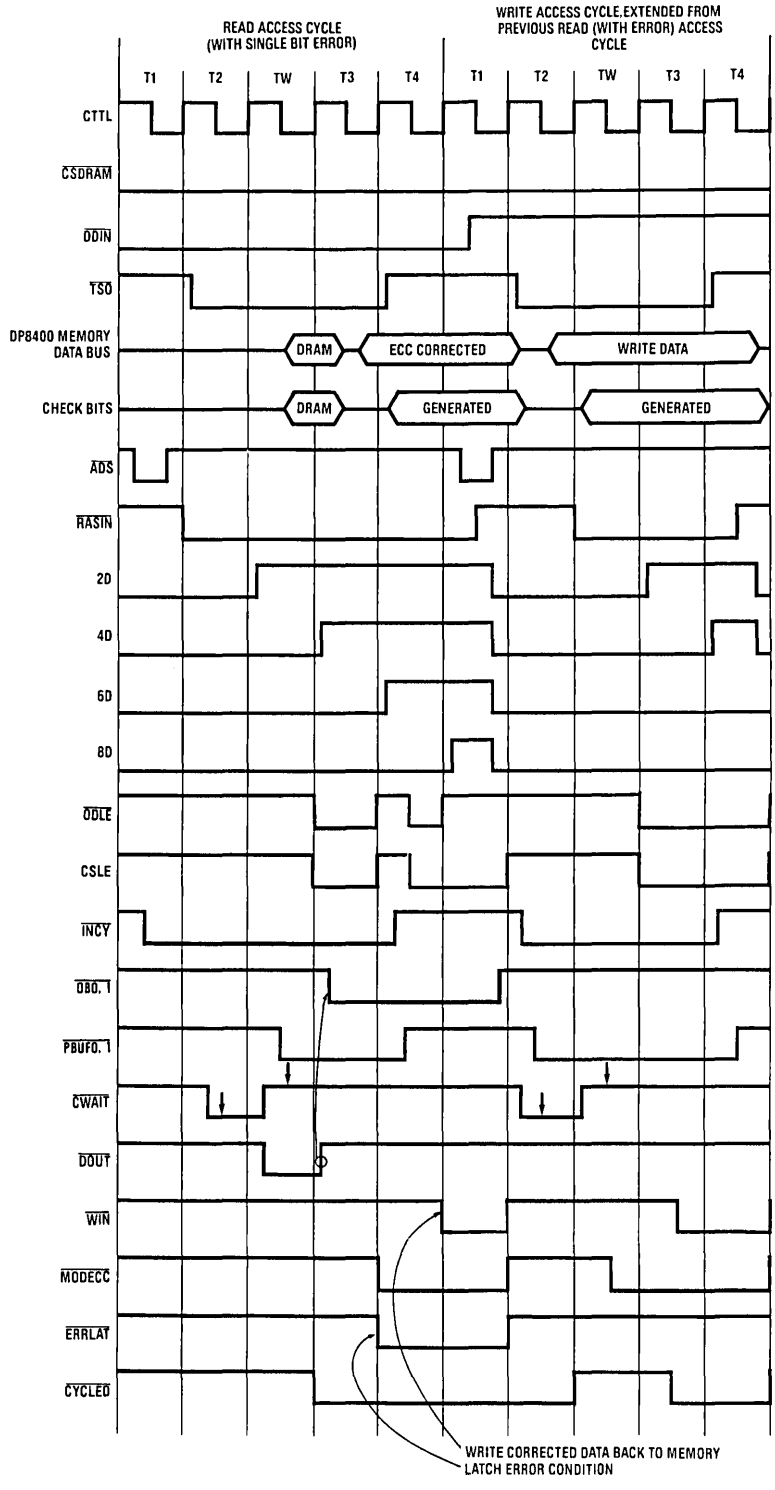
P.I.C. 3 PAL and Shift Register Interface Controller



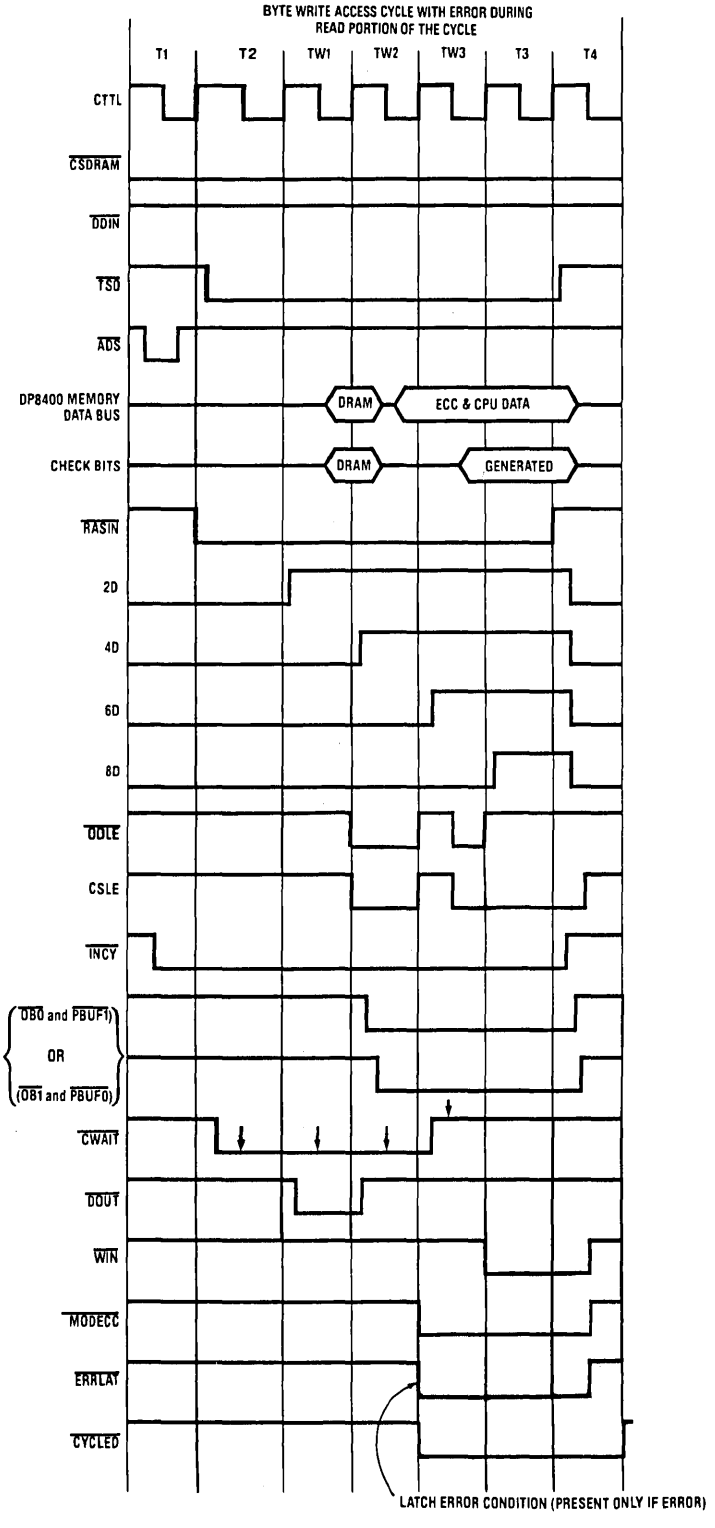
TL/F/8400-6


WRITE ACCESS CYCLE
READ ACCESS CYCLE (WITH NO ERRORS)
T1
T2
T3
T4
T1
T2
TW
T3
T4
CTTL
CSDRAM
ODIN
TSO
ADS
DP8400 MEMORY DATA BUS
WRITE DATA
DRAM
ECC DATA
CHECK BITS
GENERATED
DRAM
RASIN
2D
4D
6D
8D
ODLE
CSLE
INCY
OBO.1
PBUFO.1
CWAIT
DOUT
WIN
MODECC
ERRLAT
CYCLED

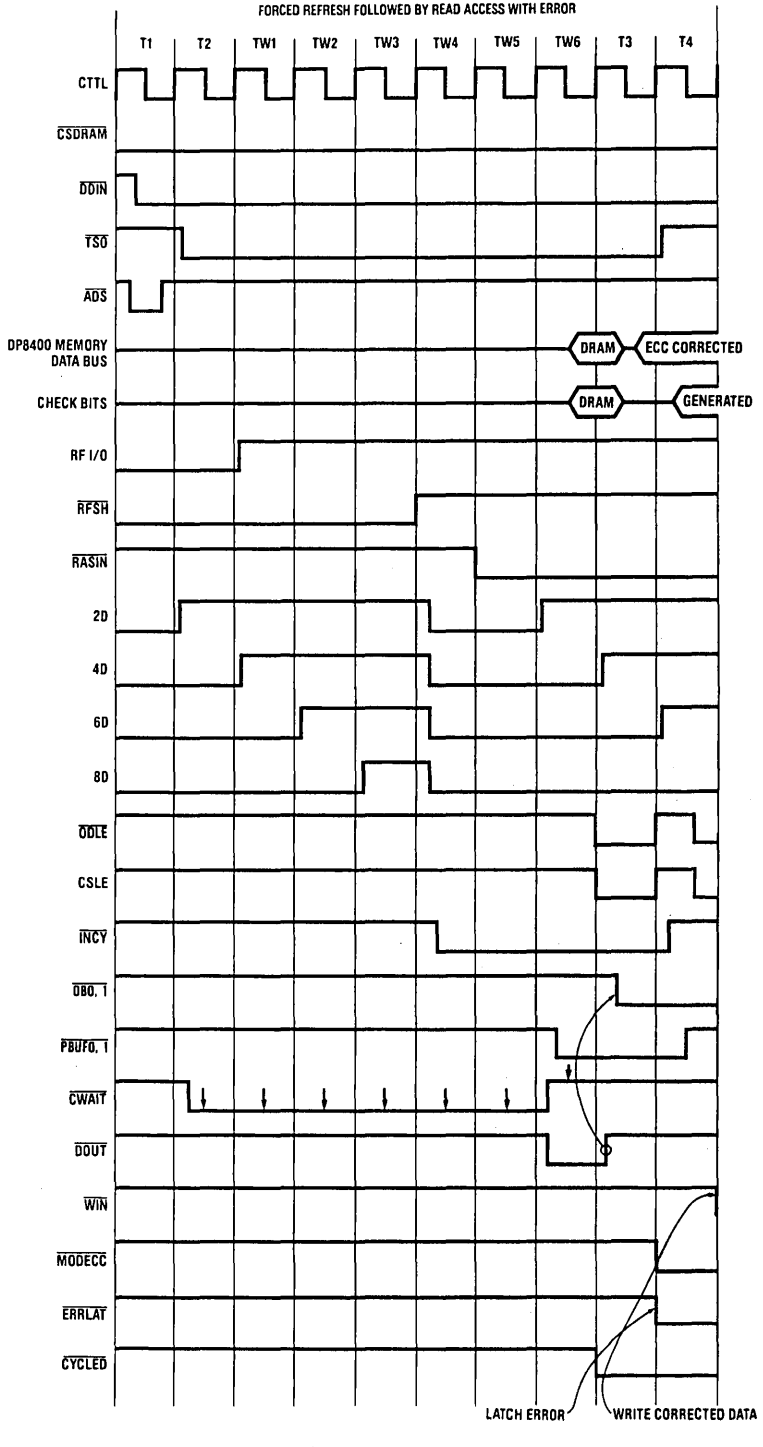
TL/F/8400–7


READ ACCESS CYCLE
(WITH SINGLE BIT ERROR)
WRITE ACCESS CYCLE EXTENDED FROM
PREVIOUS READ (WITH ERROR) ACCESS
CYCLE
T1
T2
TW
T3
T4
T1
T2
TW
T3
T4
CTTL
CSDRAM
ODIN
TSO
DP8400 MEMORY
DATA BUS
DRAM
ECC CORRECTED
WRITE DATA
CHECK BITS
DRAM
GENERATED
GENERATED
ADS
RASIN
2D
4D
6D
8D
ODLE
CSLE
INCY
OBO.1
PBUFO.1
CWAIT
DOUT
WIN
MODECC
ERRLAT
CYCLEO
WRITE CORRECTED DATA BACK TO MEMORY
LATCH ERROR CONDITION

TL/F/8400–8


BYTE WRITE ACCESS CYCLE WITH ERROR DURING READ PORTION OF THE CYCLE
T1
T2
TW1
TW2
TW3
T3
T4
CTTL
CSDRAM
DDIN
TSO
ADS
DP8400 MEMORY DATA BUS
DRAM
ECC & CPU DATA
CHECK BITS
DRAM
GENERATED
RASIN
2D
4D
6D
8D
DDLE
CSLE
INCY
(DBO and PBUF1)
OR
(DB1 and PBUF0)
CWAIT
DOUT
WIN
MODECC
ERRLAT
CYCLED
LATCH ERROR CONDITION (PRESENT ONLY IF ERROR)

TL/F/8400–9


FORCED REFRESH FOLLOWED BY READ ACCESS WITH ERROR
T1
T2
TW1
TW2
TW3
TW4
TW5
TW6
T3
T4
CTTL
CSDRAM
DDIN
TSO
ADS
DP8400 MEMORY DATA BUS
DRAM
ECC CORRECTED
CHECK BITS
DRAM
GENERATED
RF I/O
RFSH
RASIN
2D
4D
6D
8D
ODLE
CSLE
INCY
OBO, 1
PBUF0, 1
CWAIT
DOUT
WIN
MODECC
ERRLAT
CYCLED
LATCH ERROR
WRITE CORRECTED DATA

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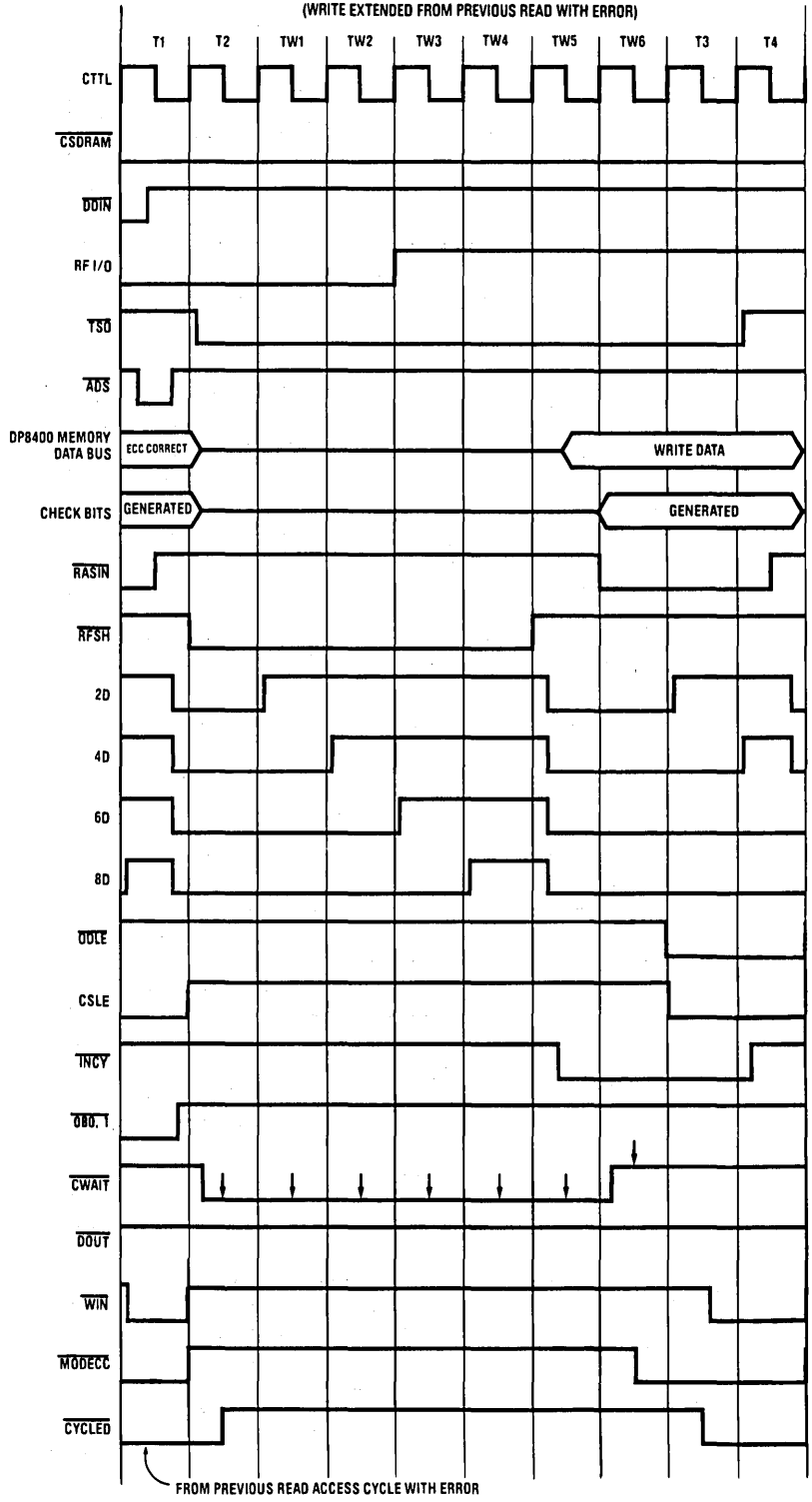
FORCED REFRESH WITH WRITE ACCESS AT THE SAME TIME
(WRITE EXTENDED FROM PREVIOUS READ WITH ERROR)



TL/F/8400–11

Section 3

Microprocessor Interface and Applications

Section Contents

Selection Guide

One of the great strengths of the DP8400 DRAM Interface Family is its General purpose open-architecture approach. Applications and hardware support for all the major 8-, 16-, and 32-bit microprocessors (not just National's) are provided through the DP84XX2 Family. Each of these devices has been tailored to provide a general purpose but efficient interface between the DP8409A, 8417, 8418, 8419, 8428, 8429 DRAM controller/drivers and each of the major cpu's. Each device uses a 20 pin standard PAL device such as the PAL16R4A as its building block. Programming equations have been written and hard programmed into each device which supply all the control signals needed to perform memory read, write, refresh, and arbitration. In order to allow for system customization, the programming equations for each device are printed in each data sheet.

Microprocessor to DRAM Controller Interface
a SELECTION GUIDE

Device #	Microprocessor Supported	DRAM Cont./ Drivers Supported	Max. Prop Delay		V_{CC}	Typ. I_{CC}	Process	Operating Temp.	Package	Page No.
			"A" PAL	"B" PAL						
DP84412	NS32008/16/32	DP8409A, 17, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA	Junction Isolated (S) or Oxide Isolated (ALS)	0°–70°C	20J, N, V	3-24
DP84512	NS32332	DP8417, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA		0°–70°C	20J, N, V	3-64
DP84322	68000/08/10 (≤10 MHz)	DP8409A, 17, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA		0°–70°C	20J, N, V	3-9
DP84422	68000/08/10 (≥10 MHz)	DP8409A, 17, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA		0°–70°C	20J, N, V	3-37
DP84522	68020	DP8417, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA		0°–70°C	20J, N, V	3-65
DP84432	8086/88/186/188	DP8409A, 17, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA		0°–70°C	20J, N, V	3-51
DP84532	80286	DP8409A, 17, 18, 19, 28, 29	25 ns	15 ns	+5V ±10%	120 mA		0°–70°C	20J, N, V	3-81

National Semiconductor Corporation

PRELIMINARY

DP84300 Programmable Refresh Timer

General Description

The DP84300 programmable refresh timer is a logic device which produces the desired refresh clock required by all dynamic memory systems.

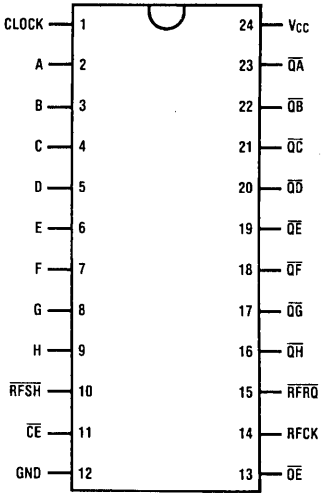
Additional circuitry has been included in the device to minimize logic required by memory systems to perform refresh control.

Features

- One chip solution to produce RFCK timing for the DP8408A, DP8409A, DP8417, DP8418, DP8419, DP8428, DP8429 dynamic RAM controllers
- Programmable refresh clock timer allows for a maximum refresh period with most system clocks
- Timing is completely synchronous with the input clock, preventing race conditions present in some memory controllers
- Includes a refresh request output, simplifying the design of refresh logic in discrete controllers

Connection & Block Diagrams

Dual-In-Line Package



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Top View

Order Number DP84300N
See NS Package Number N24A

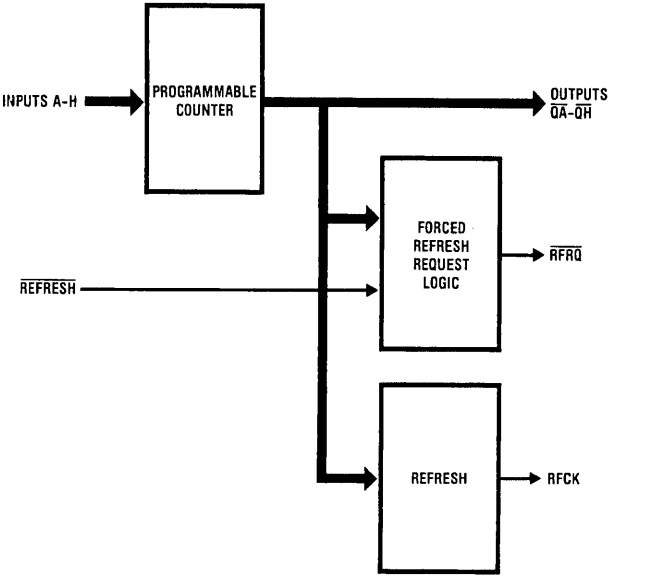

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FIGURE 1

Recommended Operating Conditions (Commercial)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			16	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	180	mA

DP84300 Switching Characteristics over recommended ranges of temperature and V_{CC}

Symbol	Parameter		Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ±5%			Units
				Min	Typ	Max	
t_{PD}	Clock to Output		C_L = 45 pF		35	50	ns
t_{PZX}	Pin 13 to Output Enable		C_L = 45 pF		20	35	ns
t_{PXZ}	Pin 13 to Output Disable		C_L = 5 pF		20	35	ns
t_{PZX}	Input to Output Enable		C_L = 45 pF		35	45	ns
t_{PXZ}	Input to Output Disable		C_L = 5 pF		35	45	ns
t_W	Width of Clock	High		25			ns
		Low		35			ns
t_{SU}	Set-Up Time			50			ns
t_H	Hold Time			0	−15		ns
f_{MAX}	Maximum Frequency			12.5			MHz

Mnemonic Description

INPUT SIGNALS

CLOCK — Provides a time base for the programmable divider.

A-H — Program inputs A through H. These inputs select the number of clock cycles that will produce one refresh period. These inputs are binary encoded, with input A the LSB, and H the MSB. Additionally, all zeros produce the maximum count of 256, and an input of one will reset the counter to one.

$\overline{\text{REFRESH}}$ — This input is used to reset the refresh request output ($\overline{\text{RFRQ}}$).

$\overline{\text{OE}}$ — Output enable. Places the outputs in TRI-STATE®.

$\overline{\text{CE}}$ — Counter enable. This input, when low, enables the timer clock and, when high, stalls the timer.

OUTPUT SIGNALS

$\overline{\text{QA}}$-$\overline{\text{QH}}$ — Refresh timer outputs $\overline{\text{QA}}$ through $\overline{\text{QH}}$. Timer starts at programmed input and counts down to one.

$\overline{\text{RFRQ}}$ — Refresh request. This output goes low on the rising edge of the refresh clock (RFCK). The first input clock edge after the $\overline{\text{REFRESH}}$ input is set low clears this output.

RFCK — Refresh clock. The period of the clock is determined by setting conditions on input pins A through H. This output is low for 20 clocks, and high for the remainder of the period.

Functional Description

The DP84300 block diagram is shown in *Figure 1*. This circuit is basically an 8-bit programmable counter. The user selects the number of input clock cycles required per refresh period and sets the binary equivalent on inputs A through H. A signal of that period is produced at the refresh clock (RFCK) output. This output stays low for 20 clock cycles, and goes high for the balance of the period.

When used with the DP8409A dynamic RAM controller, this duty cycle allows the DP8409A the maximum probability to perform a hidden refresh, while still allowing ample time for the DP8409A to perform a forced refresh when needed.

An additional output is provided to ease the design of systems that don't use the DP8409A. This output is called refresh request ($\overline{\text{RFRQ}}$). Refresh request becomes true at the rising edge of refresh clock, and becomes false on the first rising edge of the input clock after a refresh.

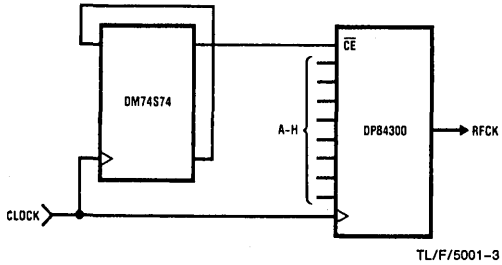
In systems where a divisor of more than 256 is needed, an expansion input ($\overline{\text{CE}}$) has been provided. When this input is high, all counter-related timing is suspended. This excluded actions due to the $\overline{\text{REFRESH}}$ input. The circuits in *Figures 2a* and *2b* show how to expand the range of the timer by 2x or by up to 4096 clock cycles. *Figures 3a* and *3b* show two typical applications using the DP84300.

By using the clock enable input, it is also possible to change the duty cycle of the refresh clock. The circuits in *Figures 4a* and *4b* show how this may be done.

To reset the counter to a known state, select an input divisor of one. On the next clock edge the counter will reset to one. On the next clock edge whatever input divisor that is present on input A-H will be loaded into the counters.

TABLE I. Divider Constants for Generation of a 15.5 μs Clock

CPU Clock Frequency	Divisor Input	Actual Period of Output	% Chance of Hidden Refresh
2 MHz	31	15.5 μs	35%
3 MHz	46	15.3 μs	56%
4 MHz	62	15.5 μs	67%
5 MHz	77	15.6 μs	74%
6 MHz	93	15.5 μs	78%
7 MHz	109	15.6 μs	81%
8 MHz	124	15.5 μs	83%
9 MHz	140	15.6 μs	85%
10 MHz	155	15.5 μs	87%



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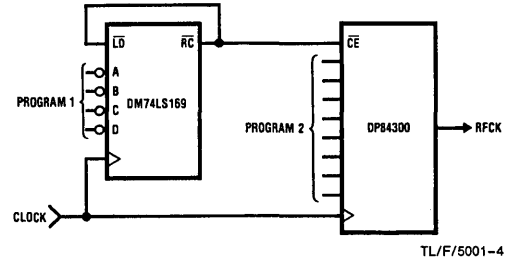
Period of RFCK = 2x program input

FIGURE 2a. Expansion of Clock Divisor by 2x



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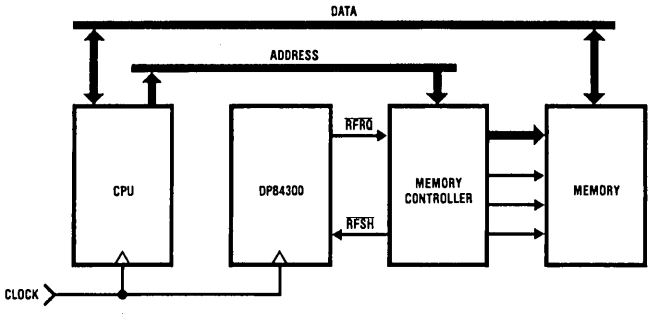
Period of RFCK 2 = program A × program B

$\overline{\text{RFCK}}$ is low for 20x program 1 clocks

Maximum period of RFCK is 4096 clocks

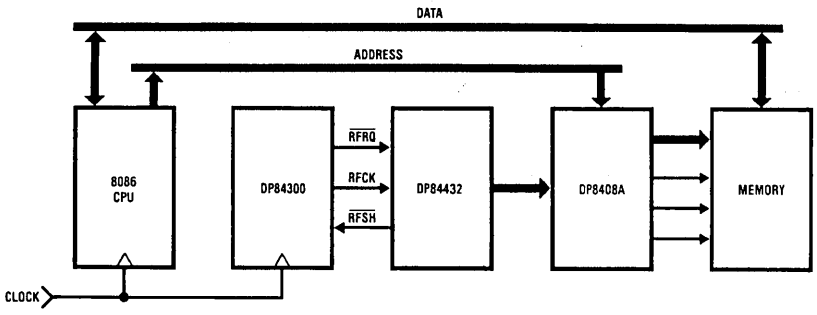
FIGURE 2b. Typical Expansion for the DP84300

Functional Description (Continued)



TL/F/5001-5

FIGURE 3a. Dynamic Memory System Using DP84300



TL/F/5001-6

FIGURE 3b. 8086 System Using Dynamic RAMs DP8408A, DP84300, and DP84432

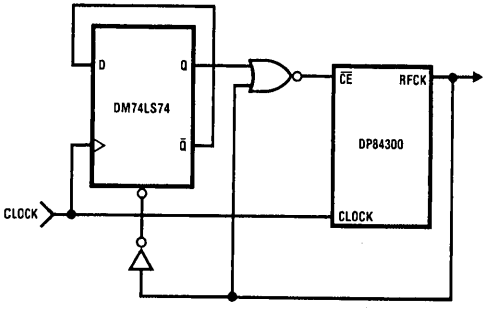


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FIGURE 4a. Circuit for Extending RFCK Low to 40 Clocks

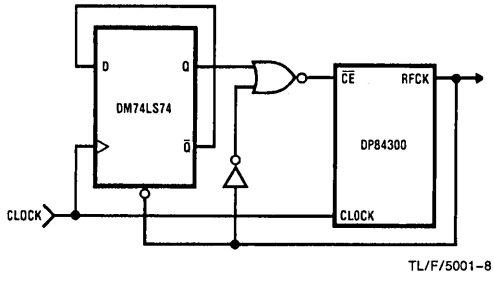

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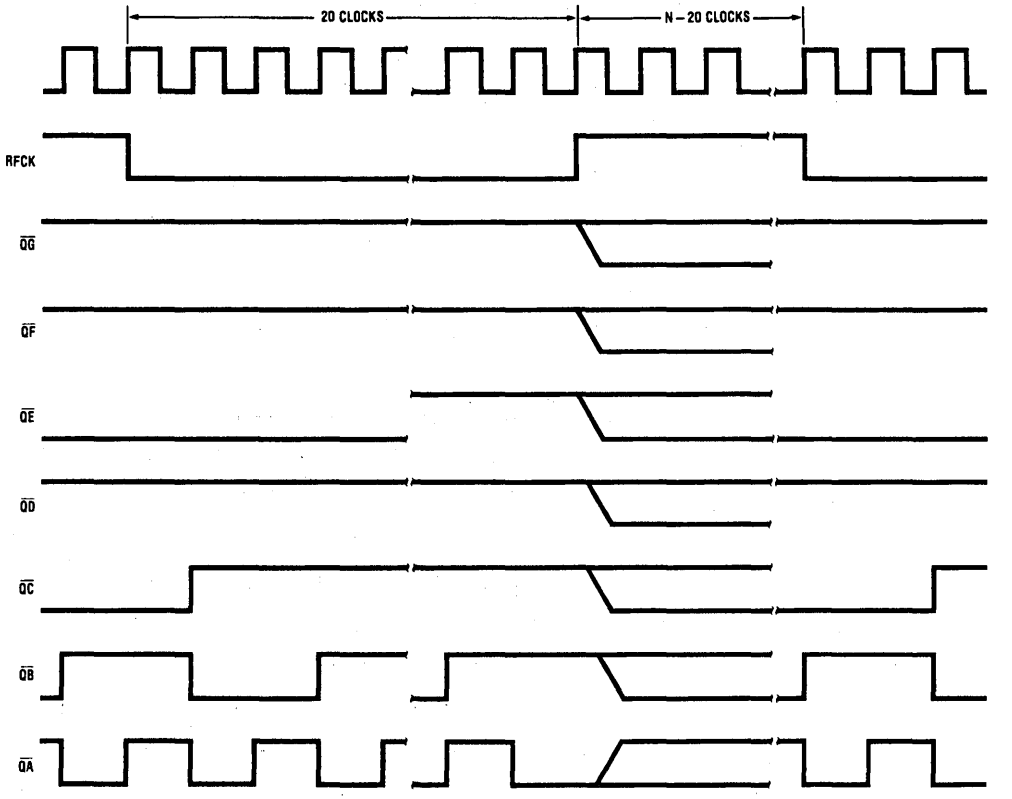
FIGURE 4b. Circuit for Extending RFCK High by 2x

Timing Diagrams

Refresh Timer Outputs



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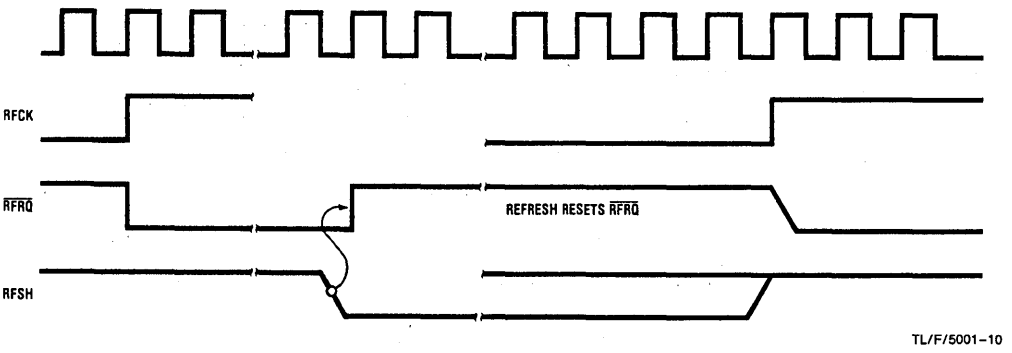
$\overline{\text{REFRESH REQUEST}}$ ($\overline{\text{RFRQ}}$) Output Timing



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National Semiconductor Corporation

DP84322 Dynamic RAM Controller Interface Circuit for the 68000 CPU

General Description

The DP84322 dynamic RAM controller interface is a Programmable Array Logic (PAL®) device which allows for easy interface between the DP8409A, 17, 18, 19, 28, 29 dynamic RAM Controllers and the 68000/008/010 microprocessors.

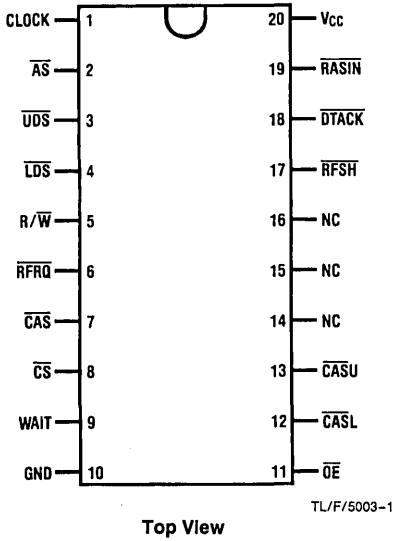
The DP84322 supplies all the control signals needed to perform memory read, write and refresh. Logic is included for inserting a wait state when using fast CPUs.

Features

- Provides 3-chip solution for the 68000 CPU and dynamic RAM interface (DP84300, DP84322, & DP8409A)
- Works with all 68000 speed versions
- Possibility of operation at 8 MHz with no wait states
- Performs hidden refresh
- $\overline{\text{DTACK}}$ is automatically inserted for both memory access and memory refresh
- Performs forced refresh using typically 4 CPU clocks
- Standard National Semiconductor PAL part (DMPAL16R4)
- PAL logic equations can be modified by the user for his specific application and programmed into any of the PAL in the National Semiconductor PAL family, including the new high speed PALs.

Connection and Block Diagrams

Dual-In-Line Package



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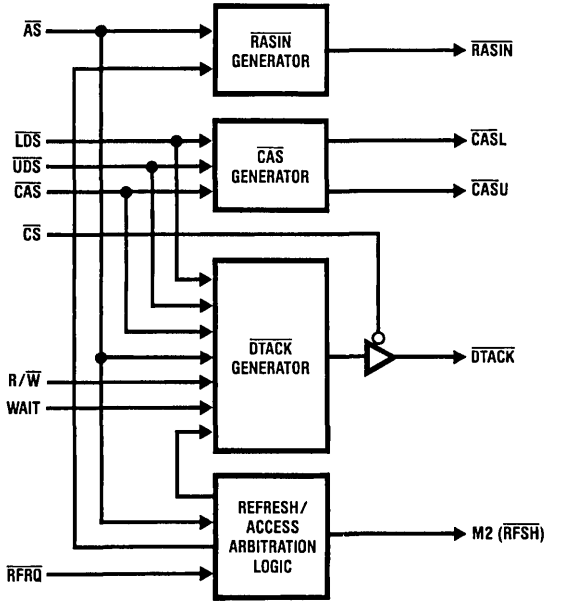
Top View

Order Number DP84322J or DP84322N
See NS Package Number J20A or N20A



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Recommended Operating Conditions (Commercial)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			24 (Note 2)	mA

	Min	Typ	Max	Units
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	225(1)	mA

Switching Characteristics over recommended ranges of temperature and V_{CC} (Note 3)

Symbol	Parameter		Test Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ±5%			Units
				Min	Typ	Max	
t_{PD}	Input to Output		C_L = 50 pF		15	25	ns
t_{PD}	Clock to Output				10	15	ns
t_{PZX}	Pin 11 to Output Enable				10	20	ns
t_{PXZ}	Pin 11 to Output Disable		C_L = 5 pF		11	20	ns
t_{PZX}	Input to Output Enable		C_L = 50 pF		10	25	ns
t_{PXZ}	Input to Output Disable		C_L = 5 pF		13	25	ns
t_w	Width of Clock	High		15			ns
		Low		15			ns
t_{su}	Set-Up Time			25			ns
t_h	Hold Time			0	−10		ns

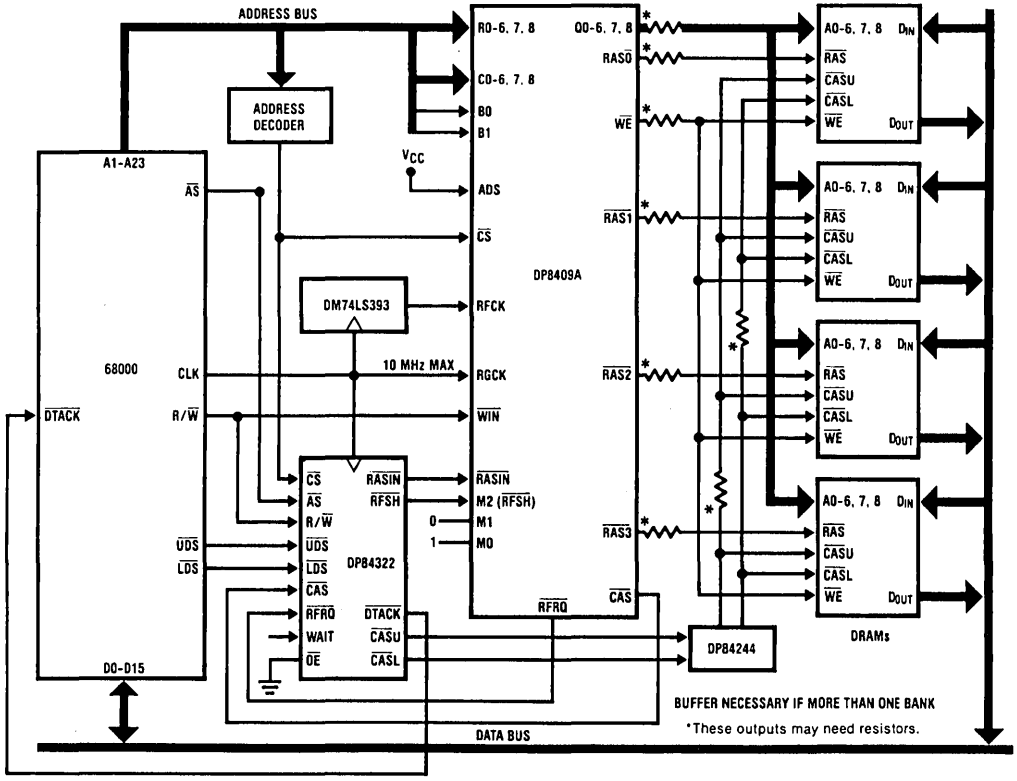
Note 1: I_{CC} = max at minimum temperature.

Note 2: One output at a time; otherwise 16 mA.

Note 3: If a PAL16R4B PAL is used, the Switching Characteristics will improve correspondingly.

System Block Diagram

DP84322 and DP8409A for 68000 CPU



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Mnemonic Description

INPUT SIGNALS

CLOCK — The clock signal determines the timing of the outputs and should be connected directly to the 68000 clock input.

$\overline{AS}$ — Address Strobe from the 68000 CPU. This input is used to generate $\overline{RASIN}$ to the DP8409A.

$\overline{UDS}$, $\overline{LDS}$ — Upper and lower data strobe from the 68000 CPU. These inputs, together with $\overline{AS}$, R/$\overline{W}$, provide $\overline{DTACK}$ to the 68000.

R/$\overline{W}$ — Read/write from the 68000 CPU, when WAIT = 0. Selects processor speed when WAIT = 1 ("1" = 4 to 6 MHz, "0" = 8 MHz).

$\overline{CAS}$ — Column Address Strobe from the DP8409A. This input, together with $\overline{LDS}$ and $\overline{UDS}$, provides two separate $\overline{CAS}$ outputs for accessing upper and lower memory data bytes.

$\overline{CS}$ — Chip Select. This input enables $\overline{DTACK}$ output. $\overline{CS}$ = 0, $\overline{DTACK}$ output is enabled; $\overline{CS}$ = 1, $\overline{DTACK}$ output is TRI-STATE®.

$\overline{RFRQ}$ — Refresh Request. This input requests the DP84322 for a forced refresh.

WAIT — This input allows the necessary wait state to be inserted for memory access cycles.

OUTPUT SIGNALS

$\overline{RASIN}$ — This output provides a memory cycle start signal to the DP8409A and provides $\overline{RAS}$ timing during hidden refresh.

$\overline{CASU}$, $\overline{CASL}$ — These signals are the separate $\overline{CAS}$ outputs needed for byte writing.

$\overline{DTACK}$ — This output is used to insert wait states into the 68000 memory cycles when selected and during a forced refresh cycle where the CPU attempts to access the memory. This output is enabled when $\overline{CS}$ input is low and at TRI-STATE when $\overline{CS}$ is high.

$\overline{RFSH}$ — This output controls the mode of the DP8409A. It always goes low for 4 CPU clock periods when $\overline{AS}$ is inactive and a forced refresh is requested through $\overline{RFRQ}$ input. This allows the DP8409A to perform an automatic forced refresh.

Functional Description

MEMORY ACCESS

As a 68000 bus cycle begins, a valid address is output on the address bus A1–A23. This address is decoded to provide Chip Select ($\overline{CS}$) to the DP8409A. After the address becomes valid, $\overline{AS}$ goes low and it is used to set $\overline{RASIN}$ low from the DP84322 interface circuit. Note that $\overline{CS}$ must go low for a minimum of 10 ns before the assertion of $\overline{RASIN}$ for a proper memory access. As an example, with a 8 MHz 68000, the address is valid for at least 30 ns before $\overline{AS}$ goes active. $\overline{AS}$ then has to ripple through the DP84322 to produce $\overline{RASIN}$. This means the address is valid for a minimum of 40 ns before $\overline{RASIN}$ goes low, and the decoding of $\overline{CS}$ should take less than 30 ns. At this speed the DM74LS138 or DM74LS139 decoders can be selected to guarantee the 10 ns minimum required by $\overline{CS}$ set-up time going low before the access $\overline{RASIN}$ goes low (t_{CSRL} of the DP8409A). This is important because a false hidden refresh may take place when the minimum t_{CSRL} is not met. Typically $\overline{RASIN}$ occurs at the end of S2. Subsequently, selected $\overline{RAS}$ output, row to column select and then $\overline{CAS}$ will automatically follow $\overline{RASIN}$ as determined by mode 5 of the DP8409A. Mode 5 guarantees a 30 ns minimum for row address hold time (t_{RAH}) and a minimum of 8 ns column address set-up time (t_{ASC}). If the system requires instructions that use byte writing, then $\overline{CASU}$ and $\overline{CASL}$ are needed for accessing upper and lower memory data bytes, and they are provided by the DP84322. In the DP84322, $\overline{LDS}$ and $\overline{UDS}$ are gated with $\overline{CAS}$ from the DP8409A to provide $\overline{CASL}$ and $\overline{CASU}$, therefore designers need not be concerned about delaying $\overline{CAS}$ during write cycles to assure valid data being written into memory. The 8 MHz 68000 specifies during a write cycle that data output is valid for a minimum of 30 ns before $\overline{DS}$ goes active. Thus, $\overline{CASL}$ and $\overline{CASU}$ will not go low for at least 40 ns after the output data becomes stable, guaranteeing the 68000 valid data is written to memory.

Furthermore, the gating of $\overline{UDS}$, $\overline{LDS}$ and $\overline{CAS}$ allows the DP84322 interface controller to support the test and set instruction (TAS). The 68000 utilizes the read-modify-write cycle to execute this instruction. The TAS instruction provides a method of communication between processors in a multiple processor system. Because of the nature of this instruction, in the 68000, this cycle is indivisible and the Address Strobe $\overline{AS}$ is asserted throughout the entire cycle, however $\overline{DS}$ is asserted twice for two accesses: a read then a write. The dynamic RAM controller and the DP84322 respond to this read-modity-write instruction as follows (refer to the TAS instruction timing diagram for clarification). First, the selected $\overline{RAS}$ goes low as a result of $\overline{AS}$ going low, and this $\overline{RAS}$ output will remain low throughout the entire cycle. Then the DP84322's selected $\overline{CAS}$ output ($\overline{CASL}$ or $\overline{CASU}$) goes low to read the specified data byte. After this read, $\overline{DS}$ goes high causing the selected $\overline{CAS}$ to go high. A few clocks later R/$\overline{W}$ goes low and then $\overline{DS}$ is reasserted. As $\overline{DS}$ goes low, the selected $\overline{CAS}$ goes low strobing the CPU's modified data into memory, after which the cycle is ended when $\overline{AS}$ goes high.

The two $\overline{CAS}$ outputs from the DP84322, however, can only drive one memory bank. For additional driving capability, a memory driver such as the DP84244 should be added to drive loads of up to 500 pF.

Since this DP84322 interface circuit is designed to operate with all of the 68000 speed versions, a status input called WAIT is used to distinguish the 8 MHz from the others. The WAIT input should be set low for 6 MHz or less allowing full speed of operation with no wait states. Data Transfer Acknowledge input ($\overline{DTACK}$) of the 68000 at these speeds is automatically inserted during S2 for every memory transaction cycle and is then negated at the end of that cycle when $\overline{UDS}$ and/or $\overline{LDS}$ go high. For the 8 MHz 68000 however, a wait state is required for every memory transaction cycle. At these speeds, the WAIT input is set high, selecting the DP8409A's $\overline{CAS}$ output to generate $\overline{DTACK}$ and again $\overline{DTACK}$ is negated at the end of the cycle when $\overline{UDS}$ or $\overline{LDS}$ goes high. Note that $\overline{DTACK}$ output is enabled only when the DP8409A's $\overline{CS}$ is low. Therefore when the 68000 is accessing I/O or ROM (in other words, when the DP8409A is not selected), the DP84322's $\overline{DTACK}$ output goes high impedance logic '1' through the external pull-up resistor and it is now up to the designer to supply $\overline{DTACK}$ for a proper bus cycle.

The following table indicates the maximum memory speed in terms of the DRAM timing parameters: t_{CAC} (access-time from $\overline{CAS}$) and t_{RP} ($\overline{RAS}$ precharge time) required by different 68000 speed versions:

Microprocessor Clock	Maximum t_{CAC}	Minimum t_{RP}	Minimum t_{RAS}
8 MHz	125 ns	140 ns	220 ns
6 MHz	90 ns	170 ns	290 ns
4 MHz	270 ns	280 ns	450 ns

Pin 5 (R/$\overline{W}$ input to the DP84322) is not used as R/$\overline{W}$ when the WAIT input is high. Therefore, when WAIT is high and pin 5 is low, this is configured for the 8 MHz 68000. The dynamic RAM controller in this configuration operates in mode 5 and mode 1.

When both WAIT and pin 5 are high, this is configured for 4 MHz and 6 MHz 68000, allowing only two microprocessor clocks for memory refresh. Furthermore, the designer can use the DP8408A because the dynamic RAM controller now operates in mode 0 and mode 5 or mode 6. In addition, the programmable refresh timer, DP84300, should be used to determine the refresh rate (RFCK) and to provide the refresh request ($\overline{RFRQ}$) input to the DP84322. The refresh timer can provide over two hundred different divisors. $\overline{RFRQ}$ is given at the beginning of every RFCK cycle and remains active until M2 goes low for memory refresh. The DP84322 samples $\overline{RFRQ}$ when $\overline{AS}$ is high, then sets M2 low for two microprocessor clocks, taking the DP8408A or DP8409A to the external control refresh mode. $\overline{RASIN}$ for this refresh is also issued by the DP84322. If a memory access is pending, $\overline{RASIN}$ for this access will not be given until it is delayed for approximately one microprocessor clock, allowing $\overline{RAS}$ precharge time for the dynamic RAMs.

The following table indicates different memory speeds in terms of the DRAM parameters required by 4 MHz and 6 MHz 68000:

Microprocessor Clock	Maximum t_{CAC}	Minimum t_{RAS}	Minimum t_{RP}	Minimum t_{RAH}
4 MHz	290 ns	200 ns	225 ns	20 ns
6 MHz	110 ns	125 ns	140 ns	20 ns

DP8408A, DP8409A operate in mode 6 and mode 0.

Functional Description (Continued)

When WAIT = 1, pin 5 = 0 (8 MHz), the PAL controller supports read and write cycles with one inserted wait state, forced refresh with five wait states inserted if $\overline{CS}$ is valid, and hidden refresh. This PAL mode does not support the TAS instruction.

When WAIT = pin 5 = 1 (4–6 MHz), the PAL controller supports read and write cycles with no wait states inserted, and forced refresh with two wait states inserted if $\overline{CS}$ is valid. This PAL mode does not support the TAS instruction and only supports hidden refresh when used in mode 5 with the DP8409A controller.

The DP84322 can possibly be operated at 8 MHz with no wait states (WAIT = "0") given the following conditions:

FAST PAL (PAL16R4A)

$$S2 + S3 + S4 + S5 = 250 \text{ ns}$$

$\overline{RASIN}$ delay = 60 ns ($\overline{AS}$ low max.)

+ 25 ns (Fast PAL delay) = 85 ns max.

$\overline{RASIN}$ to $\overline{CAS}$ delay DP8409-2 = 130 ns max.

External $\overline{CASH,L}$ generation using 74S02 and 74S240

7.5 ns (74S02) + 10 ns (74S240) − 7.5 ns (less load on 8409 $\overline{CAS}$ line) = 10 ns max.

Transceiver delay (74LS245) = 12 ns max.

68000 data setup into S6 = 40 ns min.

$\therefore$ Minimum t_{CAC} = 53 ns

= 250 − 85 − 130 − 10 − 12 + 40

Minimum t_{RAS} = 240 ns

Minimum t_{RP} = 150 ns

Minimum t_{RAH} = 20 ns

REFRESH CYCLE

Since the access sequence timing is automatically derived from $\overline{RASIN}$ in mode 5, R/$\overline{C}$ and $\overline{CASIN}$ are not used and now become Refresh Clock (RFCK) and $\overline{RAS}$-generator clock (RGCK) respectively. The Refresh Clock RFCK may be divided down from RGCK, which is the microprocessor clock, using the DM74LS393 or DM74LS390. RFCK provides the refresh time interval and RGCK the fast clock for all-$\overline{RAS}$ refresh if forced refreshing is necessary. The DP8409A offers both hidden refresh in mode 5 and forced refresh in mode 1 with priority placed on hidden refreshing. Assume 128 rows are to be refreshed, then a 16 μs maximum clock period is needed for RFCK to distribute refreshing of all the rows over the 2 ms period.

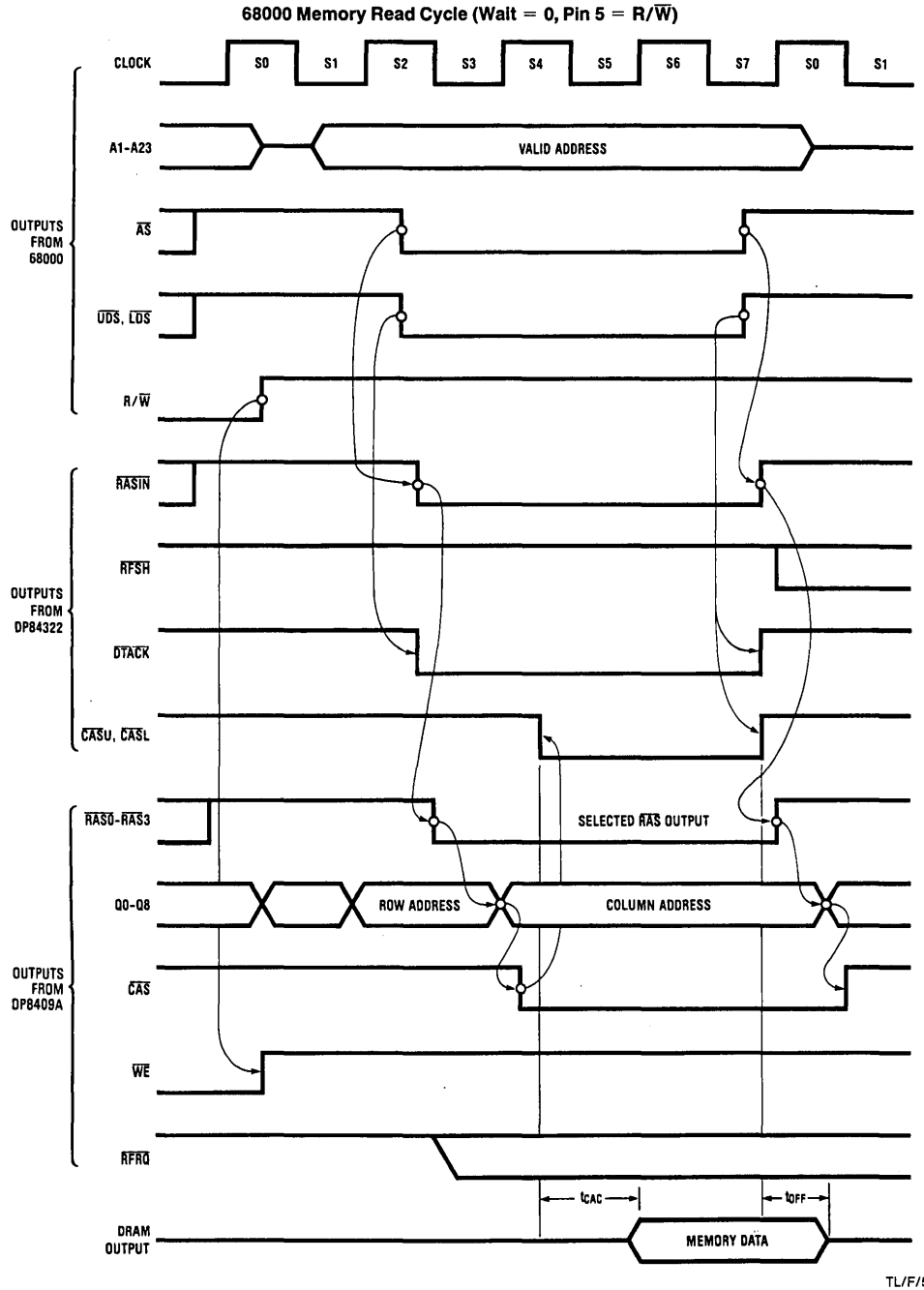
The DP8409A provides hidden refreshing in mode 5 when the refresh clock (RFCK) is high and the microprocessor is not accessing RAM. In other words, when the DP8409A's chip select is inactive because the microprocessor is accessing elsewhere, all four $\overline{RAS}$ outputs follow $\overline{RASIN}$, strobing the contents of the on-chip refresh counter to every memory bank. $\overline{RASIN}$ going high terminates the hidden refresh and also increments the refresh counter, preparing it for the next refresh cycle. Once a hidden refresh has taken place, a forced refresh will not be requested by the DP8409A for the current RFCK cycle.

However, if the microprocessor continuously accessed the DP8409A and memory while RFCK was high, a hidden refresh could not have taken place and now the system must force a refresh. Immediately after RFCK goes low, the Refresh Request signal ($\overline{RFRQ}$) from the DP8409A goes low, indicating a forced refresh is necessary. First, when $\overline{RFRQ}$ goes low any time during S2 to S7, the controller interface circuit waits until the end of the current memory access cycle and then sets M2 ($\overline{RFSH}$) low. This refresh takes four microprocessor clocks to complete. If the current cycle is another memory cycle, the 68000 will automatically be put in four wait states. Alternately, when $\overline{RFRQ}$ goes low while $\overline{AS}$ is high during S0 to S1, M2 is now set low at S2. Therefore, it requires an additional microprocessor clock for this refresh. Once the DP8409A is in mode 1 forced refresh, all the $\overline{RAS}$ outputs remain high until two RGCK trailing edges after M2 goes low, when all $\overline{RAS}$ outputs go low. This allows a minimum of one and a half clock periods of RGCK for $\overline{RAS}$ precharge time. As specified in the DP8409A data sheet, the $\overline{RAS}$ outputs remain low for two clock periods of RGCK. The refresh counter is incremented as the $\overline{RAS}$ outputs go high. Once the forced refresh has ended, M2 is brought high, the DP8409A back to mode 5 auto access. Note that $\overline{RASIN}$ for the pending access is not given until it has been delayed for a full microprocessor clock, allowing $\overline{RAS}$ precharge time for the coming access.

If the 68000 bus is inactive (i.e., the 68000's instruction queue is full, or the 68000 is executing internal operations such as a multiply instruction, or the 68000 is in halt state . . .) and a refresh has been requested, a refresh will also take place because $\overline{RFRQ}$ is continuously sampled while $\overline{AS}$ is high. Therefore, refreshing under these conditions will be transparent to the microprocessor. Consequently, the system throughput is increased because the DP84322 allows refreshing while the 68000 bus is inactive.

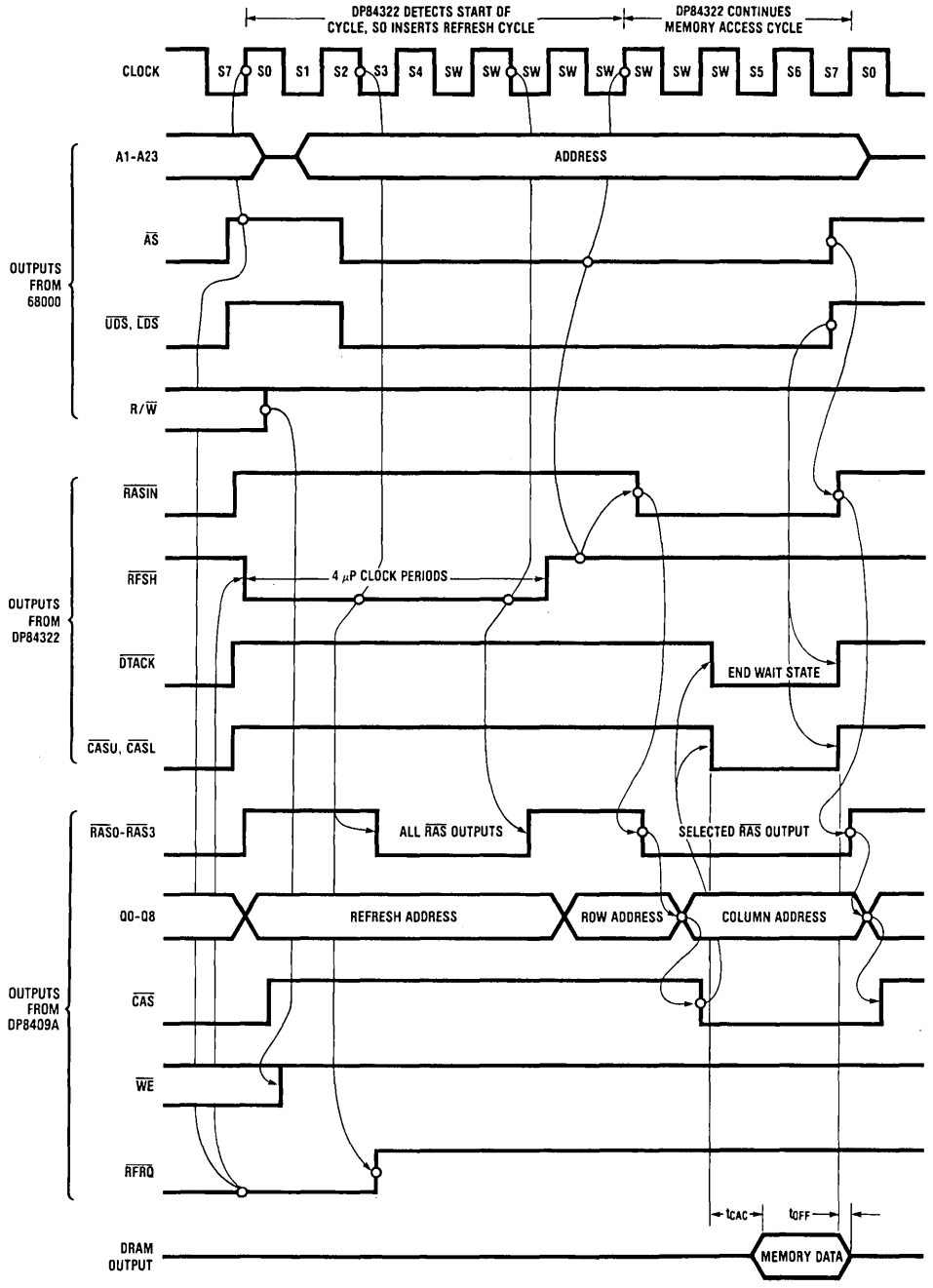
The 84322 is a standard National Semiconductor PAL part (DMPAL16R4). The user can modify the PAL equations to support his particular application. The 84322 logic equations function table (functional test), and logic diagram can be seen at the end of this data sheet.

System Timing Diagrams



System Timing Diagrams (Continued)

68000 Memory Read Cycle and Forced Refresh (Wait = 0, Pin 5 = R/$\overline{W}$)
(4 Wait Clock Periods Inserted for Forced Refresh)



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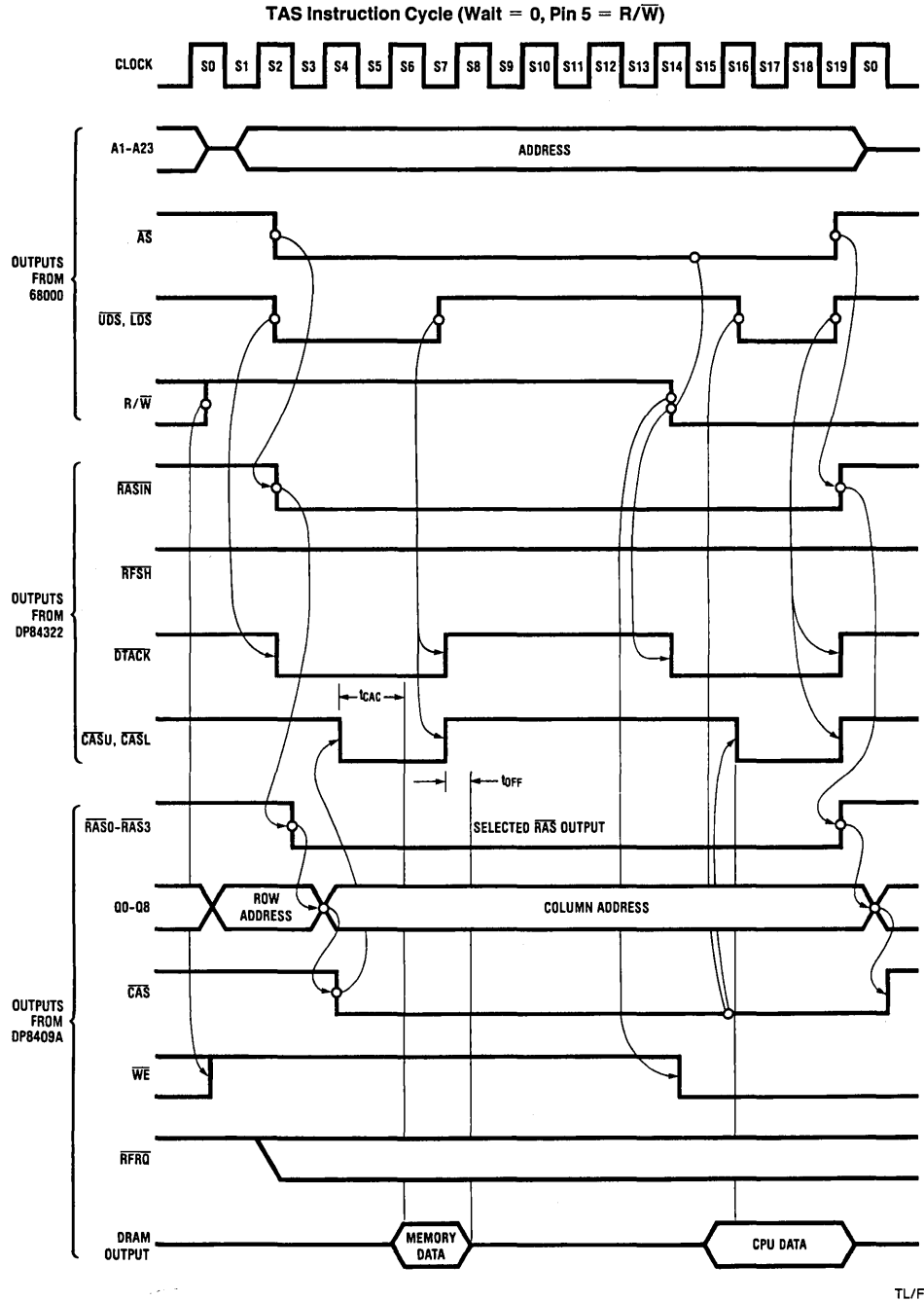
System Timing Diagrams (Continued)



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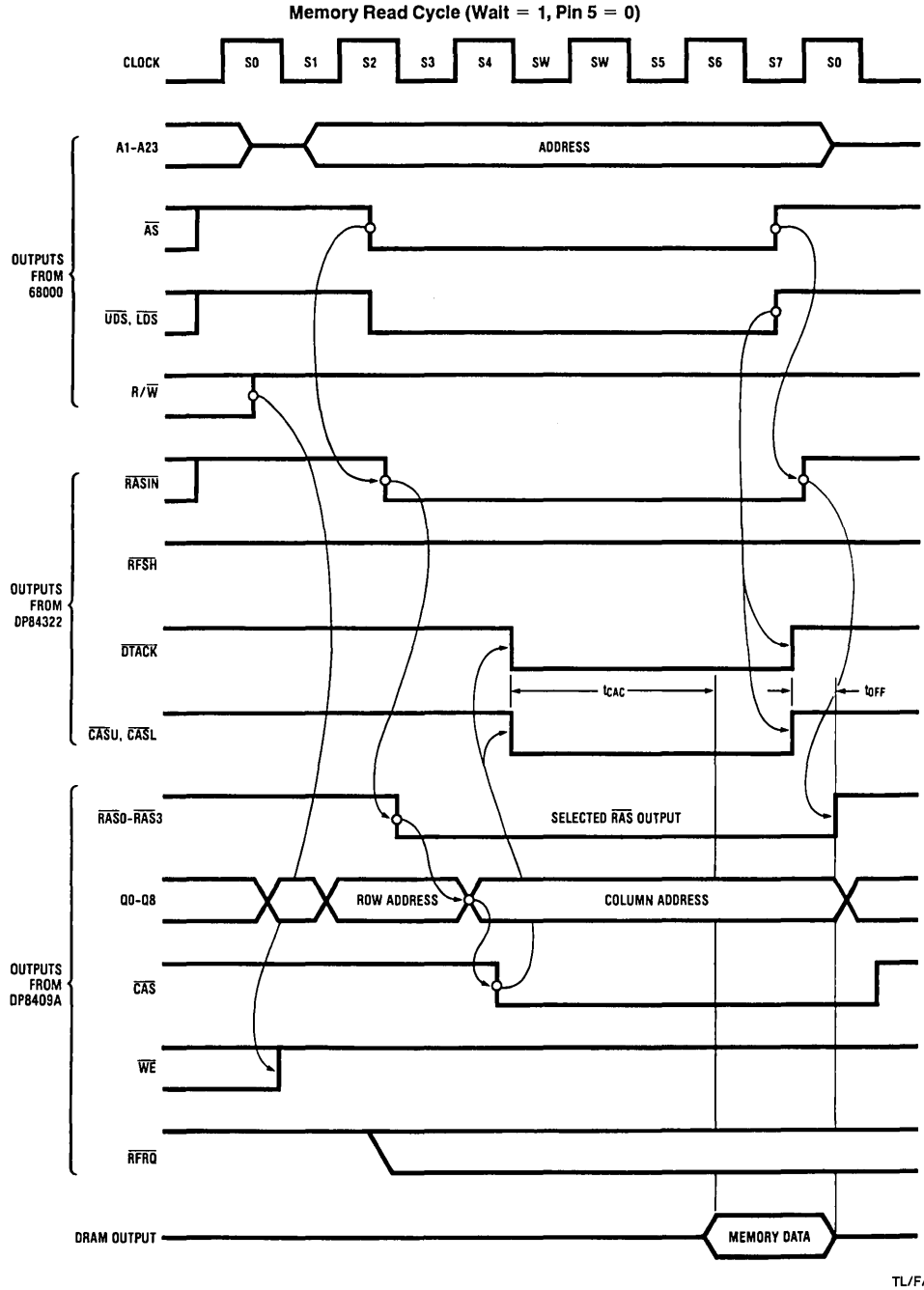
System Timing Diagrams (Continued)



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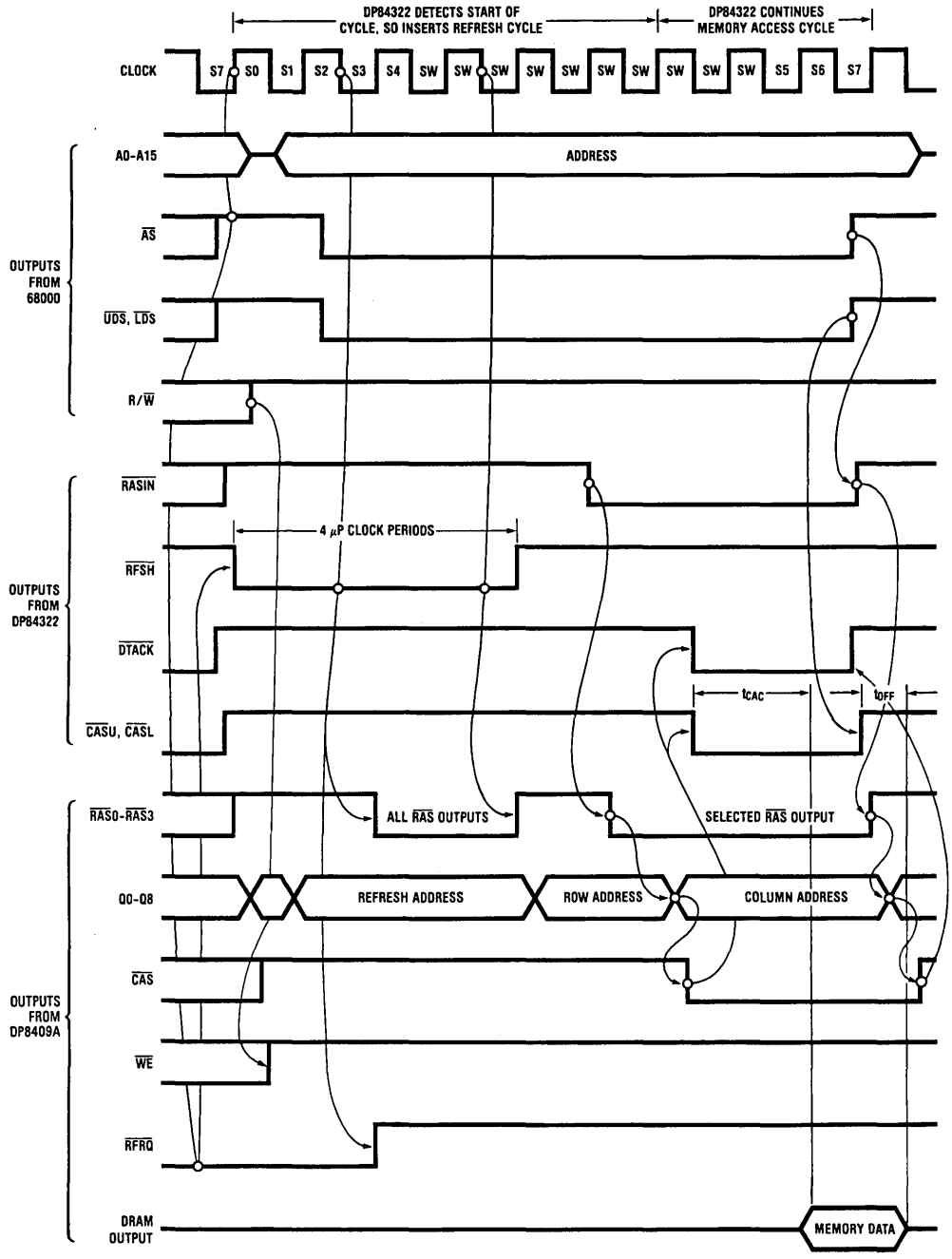
System Timing Diagrams (Continued)

Memory Read Cycle and Forced Refresh (Wait = 1, Pin 5 = 0)



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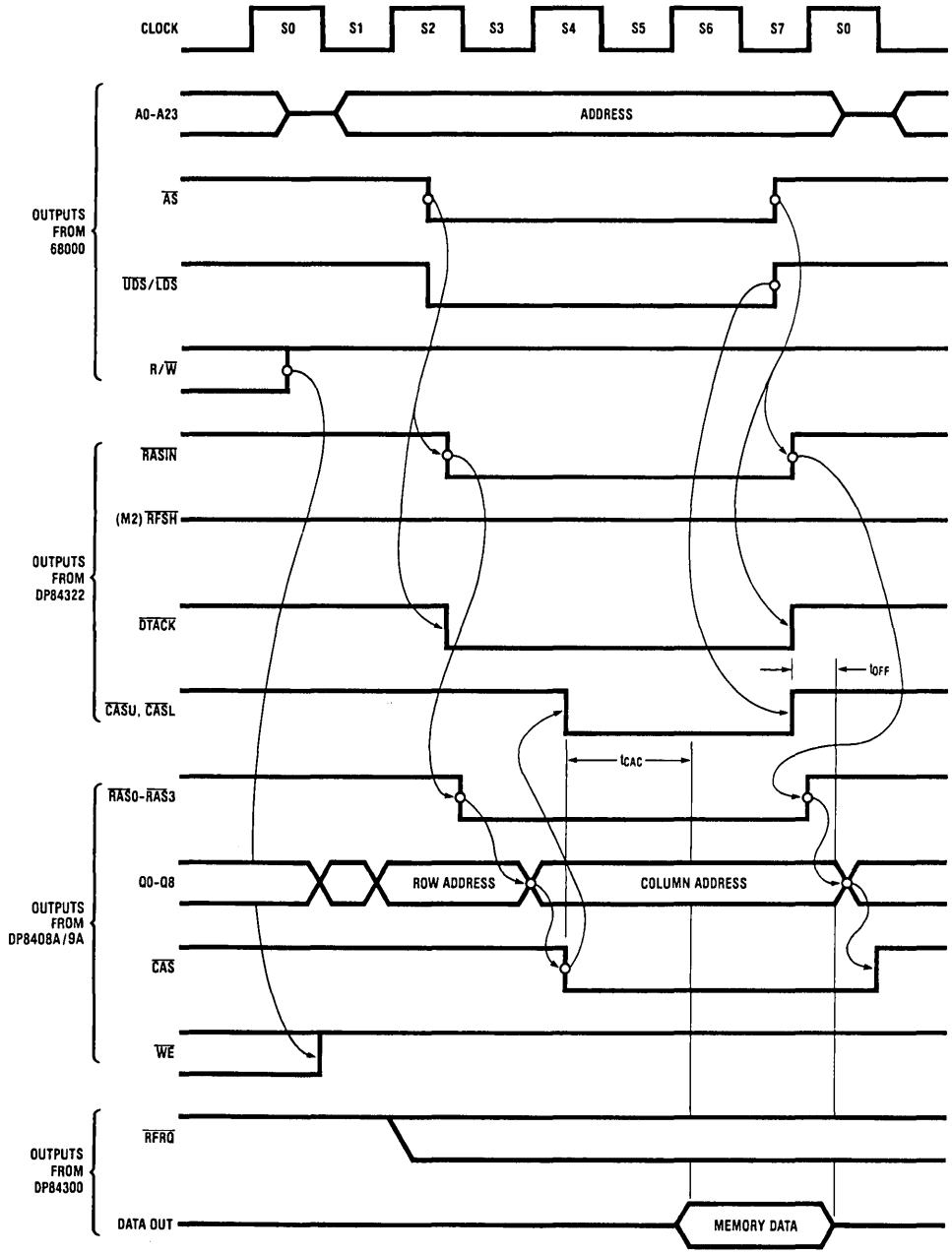
System Timing Diagrams (Continued)

68000 Memory Read Cycle (Wait and Pin 5 = 1)



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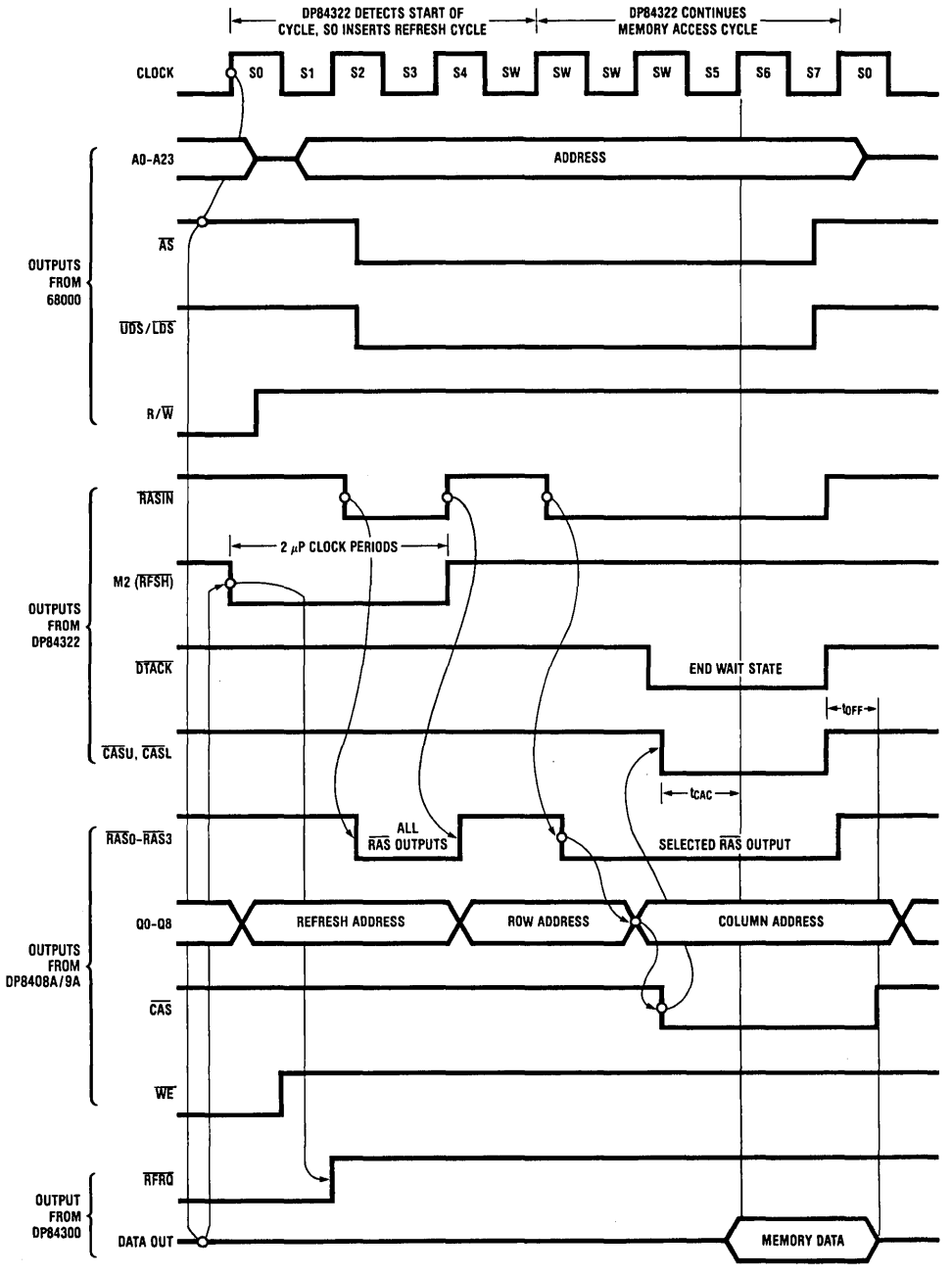
System Timing Diagrams (Continued)

68000 Memory Read Cycle and Memory Refresh (Wait and Pin 5 = 1)



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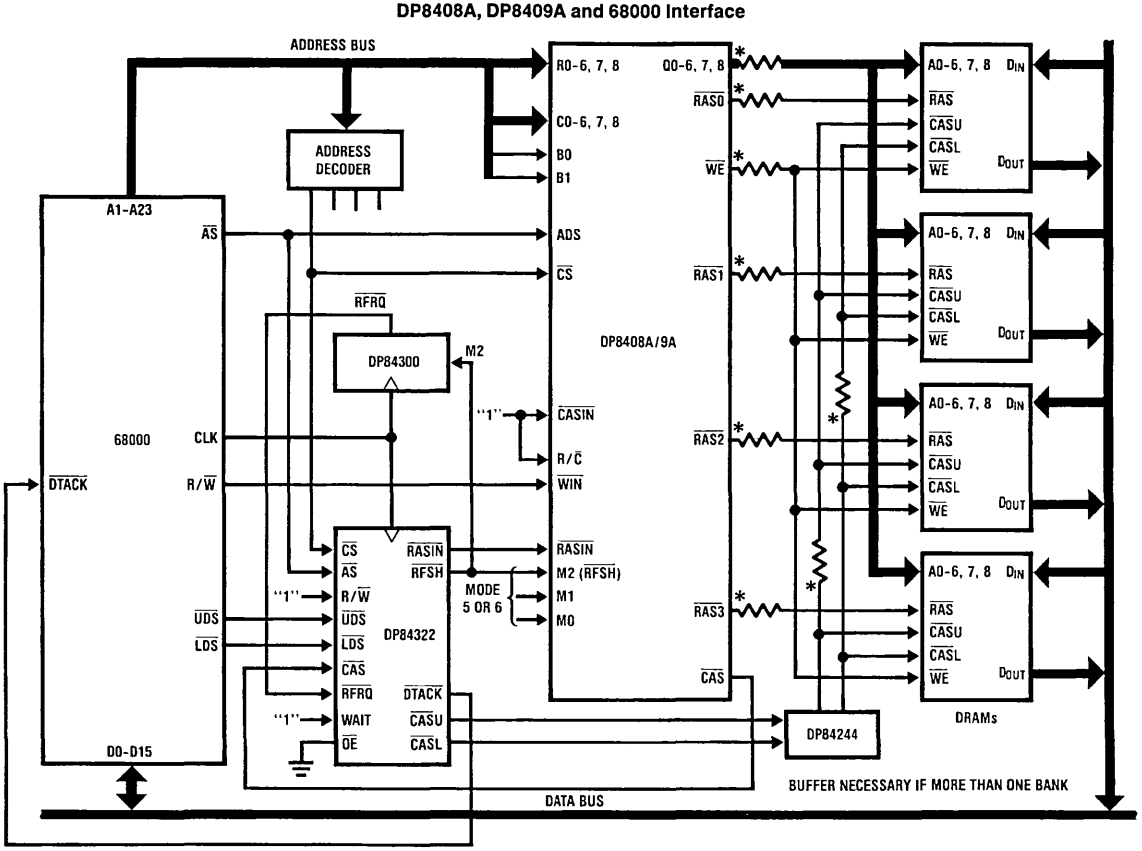

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*These outputs may need resistors.

PAL Boolean Equations

PAL16R4 DP84322 Dynamic RAM Controller Interface for the MC68000-DP8409A Memory System

CK /AS /UDS /LDS R /RFRQ /CAS /CS WAIT GND /OE /CL /CU /C /B /A /RFSH /DTACK /RASIN VCC

IF (VCC) RASIN = AS • /RFSH • /A + RFSH • R • A • WAIT

IF (CS) DTACK = /R • CAS • WAIT + UDS • /A • /B • /WAIT + LDS • /A • /B • /WAIT + AS • /R • /A • /B • /WAIT + AS • /RFSH • R • /A • /B • WAIT

RFSH: = /AS • RFRQ + RFSH • /R • /C • WAIT + RFSH • R • /A • WAIT + RFSH • /C • /WAIT

A: = RFSH

B: = A

C: = B

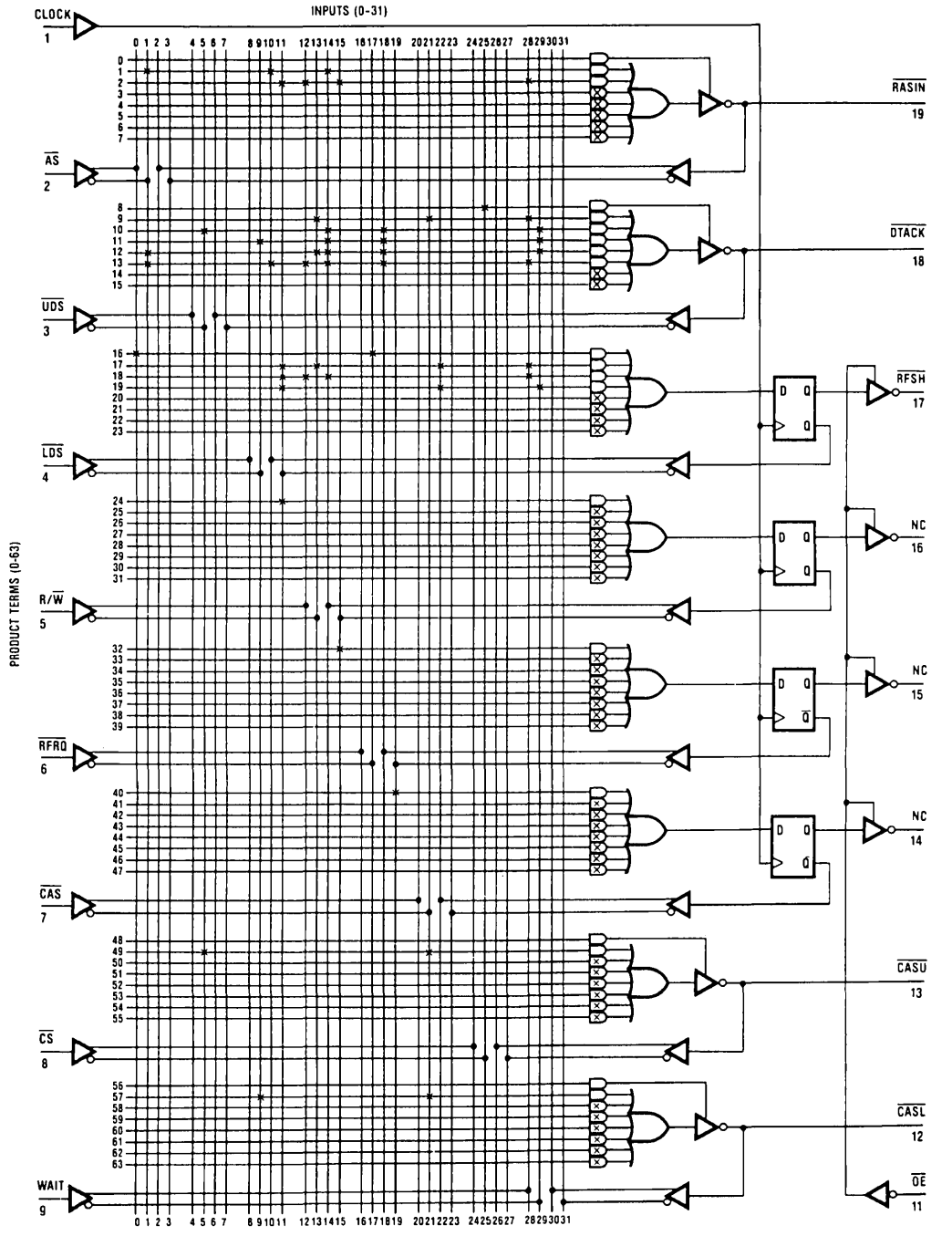
IF (VCC) CU = UDS • CDS

IF (VCC) CL = LDS • CAS

Function Table

CK	$\overline{AS}$	$\overline{UDS}$	$\overline{LDS}$	R	$\overline{RFRQ}$	$\overline{CAS}$	$\overline{CS}$	WAIT	$\overline{OE}$	$\overline{CL}$	$\overline{CU}$	$\overline{C}$	$\overline{B}$	$\overline{A}$	$\overline{RFSH}$	$\overline{DTACK}$	$\overline{RASIN}$
C	H	L	L	H	H	H	H	L	L	H	H	X	X	X	X	X	H
C	H	L	L	H	H	L	H	L	L	L	L	X	X	X	X	X	H
C	H	L	H	H	H	L	H	L	L	H	L	X	X	X	X	X	H
C	H	H	L	H	H	L	H	L	L	L	H	X	X	X	X	X	H
C	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	Z	H
C	L	L	H	H	H	H	L	L	L	H	H	H	H	H	H	L	L
C	L	L	H	H	H	L	L	L	L	H	L	H	H	H	H	L	L
C	L	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	L
C	L	H	H	L	H	L	L	L	L	H	H	H	H	H	H	L	L
C	L	L	H	L	H	L	L	L	L	H	L	H	H	H	H	L	L
C	H	H	H	L	H	H	L	L	L	H	H	H	H	H	H	H	H
C	H	H	H	L	L	H	L	L	L	H	H	H	H	H	L	H	H
C	H	H	H	L	L	H	L	L	L	H	H	H	H	L	L	H	H
C	L	H	L	L	H	H	L	L	L	H	H	H	L	L	L	H	H
C	L	H	L	L	H	H	L	L	L	H	H	L	L	L	L	H	H
C	L	H	L	L	H	H	L	L	L	H	H	L	L	L	H	H	H
C	L	H	L	L	H	H	L	L	L	H	H	L	L	H	H	H	L
C	L	H	L	L	H	L	L	L	L	L	H	L	H	H	H	L	L
C	L	H	L	L	H	L	L	L	L	L	H	H	H	H	H	L	L
C	H	H	H	L	H	L	L	L	L	H	H	H	H	H	H	H	H
C	H	H	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H
C	H	H	H	L	L	H	L	H	L	H	H	H	H	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	H	L	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	H	H	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	H	H	H	L
C	L	L	L	L	H	L	L	H	L	L	L	L	H	H	H	L	L
C	H	H	H	L	H	L	L	H	L	H	H	H	H	H	H	L	H
C	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	Z	H
C	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H
C	H	H	H	H	L	H	L	H	L	H	H	H	H	L	L	H	L
C	L	L	H	H	H	H	L	H	L	H	H	H	L	L	H	H	H
C	L	L	H	H	H	H	L	H	L	H	H	L	L	H	H	H	L
C	L	L	H	H	H	L	L	H	L	H	L	L	H	H	H	L	L
C	H	H	H	H	H	L	L	H	L	H	H	H	H	H	H	H	H
C	H	H	H	H	H	H	L	H	H	H	H	Z	Z	Z	Z	H	H

DP84322 Logic Diagram PAL 16R4



TL/F/5003–12

National Semiconductor Corporation

DP84412 Dynamic RAM Controller Interface Series Circuit for the Series 32000® CPU

General Description

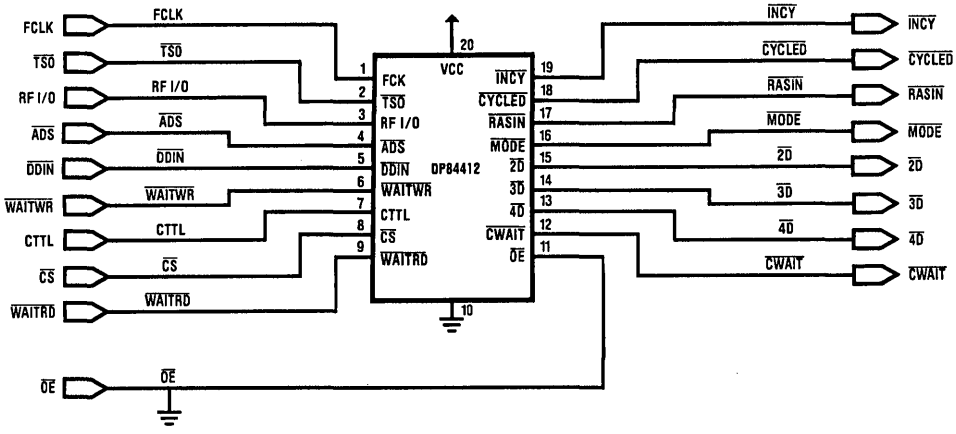
The DP84412 is a new Programmable Array Logic (PAL®) device, that replaces the DP84312, designed to allow an easy interface between the National Semiconductor Series 32000 family of processors and the National Semiconductor DP8409A, DP8429, or DP8419 DRAM controller.

The new DP84412 supplies all the control signals needed to perform memory read, write and refresh and work with the National Semiconductor Series 32000 family of processors up to 10 MHz. Logic is also included to insert WAIT states, if wanted, into the microprocessor READ or WRITE cycles when using fast CPUs.

Features

- Provides a 3-chip solution for the Series 32000 family, dynamic RAM interface (DP8409A or DP8419, DP84412, and clock divider).
- Works with all Series 32000 family speed versions up to 10 MHz.
- Operation of Series 32000 processor at 10 MHz with no WAIT states.
- Controls DP8409A or DP8419 Mode 5 accesses, hidden refreshes and Mode 1 Forced Refreshes automatically.
- Inserts WAIT states in READ or WRITE cycles automatically depending on whether $\overline{\text{WAITRD}}$ or $\overline{\text{WAITWR}}$ are low, or if $\overline{\text{CS}}$ becomes active during a forced Refresh cycle.
- Uses a standard National Semiconductor PAL part (DMPAL16R6A).
- The PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new very high speed PALs ("B" PAL parts).

Connection Diagram



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Order Number DP84412J or DP84412N
See NS Package Number N20A or J20A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	Operating	Programming		Operating	Programming
Supply Voltage, V_{CC}	7V	12V	Off-State Output Voltage	5.5V	12V
Input Voltage	5.5V	12V	Storage Temperature Range	−65°C to +150°C	

Recommended Operating Conditions

Symbol	Parameter		Commercial			Units
			Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
t_w	Width of Clock	Low	15	10		ns
		High	15	10		
t_{su}	Setup Time from Input or Feedback to Clock		25	16		ns
t_h	Hold Time		0	−10		ns
T_A	Operating Free-Air Temperature		0	25	75	°C
T_C	Operating Case Temperature					°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −3.2 mA COM	2.4	2.8		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 24 mA COM		0.3	0.5	V
I_{OZH}	Off-State Output Current	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.4V			−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.02	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V V_O = 0V		−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max			120	180	mA

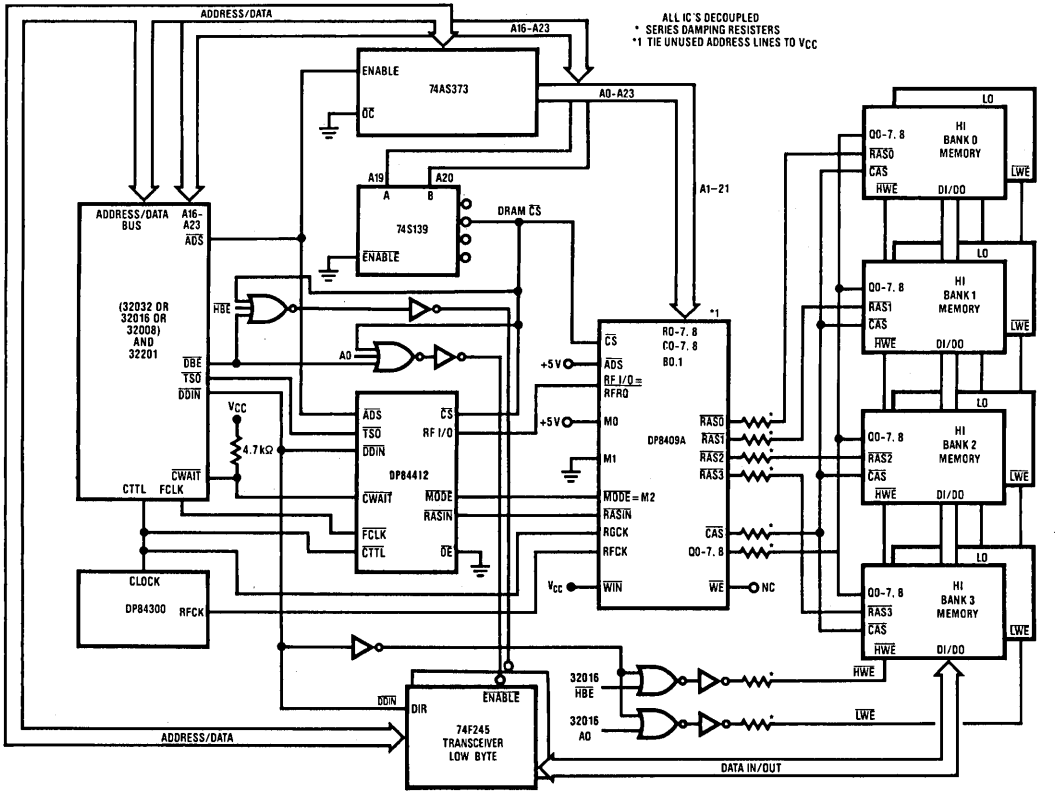
Switching Characteristics Over Recommended Ranges of Temperature and V_{CC}

V_{CC} = 5V ±10%. Commercial: T_A = 0°C to 75°C, V_{CC} = 5V ±5%

Symbol	Parameter	Test Conditions R1, R2	Commercial			Units
			Min	Typ	Max	
t_{PD}	Input or Feedback to Output	CL = 50 pF		15	25	ns
t_{CLK}	Clock to Output or Feedback			10	15	ns
t_{PZX}	Pin 11 to Output Enable			10	20	ns
t_{PXZ}	Pin 11 to Output Disable	C_L = 5 pF		11	20	ns
t_{PZX}	Input to Output Enable	C_L = 50 pF		10	25	ns
t_{PXZ}	Input to Output Disable	C_L = 5 pF		13	25	ns
f_{MAX}	Maximum Frequency		25	30		ns

V_{CC} = Max at minimum temperature.

PAL For Series 32000 Family Systems



TL/F/8397–2

Mnemonic Description

INPUTS SIGNALS

1) "FCLK" Fast clock from the NS32201 TCU clock chip, this signal runs at twice the speed of the system clock.

2) "$\overline{\text{TSO}}$" From the NS32201 TCU clock chip, this signal indicates the start of the "T2" state and goes high at the beginning of the "T4" state.

3) "RFI/O" $\overline{\text{RFRQ}}$ (refresh request) in mode 5. From 8409A, an active low signal.

4) "$\overline{\text{ADS}}$" From the Series 32000 CPU, address strobe. If the system includes the MMU (NS32082) then $\overline{\text{PAV}}$ should be connected to this input.

5) "$\overline{\text{DDIN}}$" Used to differentiate between READ and WRITE cycles, and to allow $\overline{\text{CS}}$ READ cycles to start early.

6) "$\overline{\text{WAITWRITE}}$" This signal is used to add a WAIT state into a $\overline{\text{CS}}$ WRITE access cycle, and delay $\overline{\text{RASIN}}$ until the end of the "T2" clock period.

7) "CTTL" From the NS32201 TCU clock chip, this signal runs at the system clock frequency.

8) "$\overline{\text{CS}}$" From decoder chip (chip select) (active low).

9) "$\overline{\text{WAITREAD}}$" Used to insert 1 wait state into the Series 32000 READ bus cycle. The wait state allows the use of memory with longer access times (t_{CAC}). An active low signal.

10) "$\overline{\text{OE}}$" This input enables the outputs of the "D-Flip Flop" outputs of the PAL.

OUTPUTS SIGNALS

1) "$\overline{\text{MODE}}$" This pin goes to M2 on the DP8409A to change from mode 5 to mode 1 (only used for forced refresh).

2) "$\overline{\text{2DLY}}$" Delay used internal to the PAL.

3) "$\overline{\text{3DLY}}$" Delay used internal to the PAL.

4) "$\overline{\text{4DLY}}$" Delay used internal to the PAL.

5) "$\overline{\text{RASIN}}$" To the 8409A (creates RASs). Goes low earlier for READ cycles than WRITE cycles.

6) "$\overline{\text{CYCLED}}$" Goes active low once a hidden refresh (non $\overline{\text{CS}}$ cycle) or DRAM access has been performed. $\overline{\text{CYCLED}}$ always goes low at the beginning of the "T3" processor state. This signal goes high (reset) by the end of the processor bus cycle as indicated by $\overline{\text{TSO}}$ being high.

7) "$\overline{\text{CWAIT}}$" This output inserts "WAIT" or "HOLD" states into the NS32016 machine cycles (only WAIT states are used in this application). This output is in "not enabled" condition when $\overline{\text{CS}}$ is high (not chip selected).

8) "$\overline{\text{INCYCLE}}$" This signal goes active from the CPU $\overline{\text{ADS}}$ signal. This signal indicates that the processor is doing an access somewhere in the system. This signal stays low for several T states of the access cycle.

Functional Description

The following description applies to both the DP8409A and the DP8419 dynamic RAM controllers.

A memory cycle starts when chip select ($\overline{\text{CS}}$) and address strobe ($\overline{\text{ADS}}$) are true. $\overline{\text{RASIN}}$ is supplied from the DP84412 to the DP8409A dynamic RAM controller, which then supplies a $\overline{\text{RAS}}$ signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8409A switches the address outputs to the column address. The DP8409A then supplies the required $\overline{\text{CAS}}$ signal to the DRAM. In order to do byte operations it is suggested that the user provide external logic, as shown in the system block diagram, to produce a HIGH WRITE ENABLE and/or a LOW WRITE ENABLE. To differentiate between a READ and a WRITE, the $\overline{\text{DDIN}}$ signal from the CPU is used. $\overline{\text{DDIN}}$ is also supplied to the external WRITE ENABLE logic.

A refresh cycle is started by one of two conditions. The refresh cycle caused by the first condition is called a hidden refresh. This occurs when refresh clock (RFCK) is high, $\overline{\text{CS}}$ is not true, and $\overline{\text{RASIN}}$ goes true. Here the CPU is accessing something else in the system and the DRAM can be refreshed at that time, thereby being transparent to the CPU. The second type of refresh is called forced refresh. This occurs if no hidden refresh was performed while RFCK was high. When RFCK transitions low a refresh request ($\overline{\text{RFRQ}}$) is generated. If there is not a DRAM access in progress the DP84412 will force a refresh by putting the DP8409A into mode 1 (automatic forced refresh mode). If the CPU tries to access the DRAM during a forced refresh cycle WAIT states will be inserted into its cycles until the forced refresh is over and the DRAM $\overline{\text{RAS}}$ precharge time has been met. Then the pending DRAM access will be allowed to take place.

The DP84412 also allows forced refreshes to take place during long accesses of other devices. For instance, if EEPROM takes several microseconds to write to, the DRAM will still be refreshed while that access is in progress.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories or allow time to generate parity. This is accomplished by inserting a WAIT state into the processor access cycle. The DP84412 can insert WAIT states into either READ or WRITE cycles, or both. The extra WAIT state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

System Interface Description

All members of the Series 32000 family of processors are able to use the DP84412.

The DP84412 differentiates between READ and WRITE cycles, allowing the $\overline{\text{RASIN}}$ signal to start earlier during a READ cycle compared to a WRITE cycle.

$\overline{\text{RASIN}}$ during a READ cycle will always start at the beginning of the "T2" processor cycle. The user must also guarantee that $\overline{\text{CS}}$ is valid a minimum of 30 ns before $\overline{\text{RASIN}}$ becomes valid. The worst case would be at 10 MHz where FCLK preceeds PHI1 by a maximum of 10 ns. $\overline{\text{RASIN}}$ can occur a minimum of approximately 8 ns after FCLK. Therefore $\overline{\text{CS}}$ must occur a minimum of 32 ns (30 ns+2 ns) before the rising edge of PHI1 at 10 MHz.

The user may want to tie $\overline{\text{CS}}$ low on the DP8409A/19 (disable HIDDEN REFRESH) and use the system transceivers to select the DRAM. In this case one only needs to concern himself with the 10 ns address setup time to $\overline{\text{RASIN}}$.

System Interface Description (Continued)

The DP84412 can be used in a system with the MMU (NS32082) but the signal $\overline{PAV}$ would be connected to the $\overline{ADS}$ input instead of $\overline{ADS}$.

Several other critical parameters in this application that involve the input signals $\overline{DDIN}$, $\overline{CWAIT}$, $\overline{TSO}$, and FCLK. These parameters become most critical at 10 MHz where it is suggested that they are directly connected to the corresponding pins of the Series 32000 family ICs.

This section of the data sheet goes through the calculation of the "tRAC" ($\overline{RAS}$ access time) and "tCAC" ($\overline{CAS}$ access time) required by the DRAM for the Series 32000 family CPUs to operate at a particular clock frequency without introducing wait states into the processor access cycles. Both "tRAC" and "tCAC" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "tRAC" and "tCAC" parameters calculated. In order to determine the "tRAC" and "tCAC" needed the DP8419 and fast PALs ("B" type PALs) timing parameters were used. If the user is using the DP8408A/09A or a slower PAL device he should substitute their respective delays into the equations below.

Most all of the calculations contained in this note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from RAS exceeded 200 ns. This is because DRAMs can be found with row access times up to 150 ns that require only 15 ns row address hold times.

EXAMPLE DRAM TIMING CALCULATIONS

A) 8 MHz Series 32000 CPU, No Wait states

#1) $\overline{RASIN}$ = T1 − 2 ns (FCLK to PHI1 skew) + 12 ns ("B" PAL clocked output) = 125 − 2 + 12 = 135 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum (DP8419)

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = data setup to PHI2 T.E. + maximum PHI2 F.E. to PHI1 R.E. = 15 + 5 = 20 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 125 + 125 + 125 − 135 − 20 − 7 − 20 = 193 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 135 − 77 − 7 − 20 = 136 ns

Therefore the DRAM chosen should have a "tRAC" less then or equal to 193 ns and a "tCAC" less than or equal to 136 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one and one half clock periods = 125 + 62 = 187 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 125 + 62 + 35 = 222 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns (maximum $t_{RPDL} - t_{RPDH}$ for the DP8409-2) = 250 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 250 − 70 = 180 ns.

The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times and the $\overline{RAS}$ pulse width would be increased by one clock period (125 ns in this case). A WAIT state in WRITE cycles would just increase the $\overline{RAS}$ pulse width by one clock period.

B) 10 MHz Series 32000, No Wait States

#1) $\overline{RASIN}$ low = T1 − 2 ns (FCLK − PHI1 skew) + 12 ns ("B" PAL clocked output) = 100 − 2 + 12 = 110 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns maximum (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = data setup to PHI2 T.E. + maximum PHI2 F.E. to PHI1 R.E. = 15 + 5 = 15 ns minimum

"tRAC" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 100 + 100 + 100 − 110 − 20 − 7 − 15 = 148 ns

"tCAC" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 100 + 100 + 100 − 110 − 77 − 7 − 15 = 91 ns

Therefore the DRAM chosen should have a "tRAC" less then or equal to 148 ns and a "tCAC" less than or equal to 91 ns. Standard 120 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one and one half clock periods = 100 + 50 = 150 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 100 + 50 + 35 = 185 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns (maximum $t_{RPDL} - t_{RPDH}$ for the DP8409-2) = 200 − 5 = 195 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 200 − 70 = 130 ns.

The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times and the $\overline{RAS}$ pulse width would be increased by one clock period (100 ns in this case). A WAIT state in WRITE cycles would just increase the $\overline{RAS}$ pulse width by one clock period.

SUGGESTIONS

It is suggested that the DP8409A could be used up to 8 MHz. Above 8 MHz one should use the DP8409-2 or the DP8419. Also, fast PALs ("A" or "B" parts) should be used at 8 MHz and above.

INTERPRETING THE DP84412 PAL EQUATIONS

The boolean equations for the DP84412 were written using the standard PALASM™ format. In other words the equation: "IF (V_{CC}) RASIN = INCY*$\overline{MODE}$*4D*DDIN" will mean;

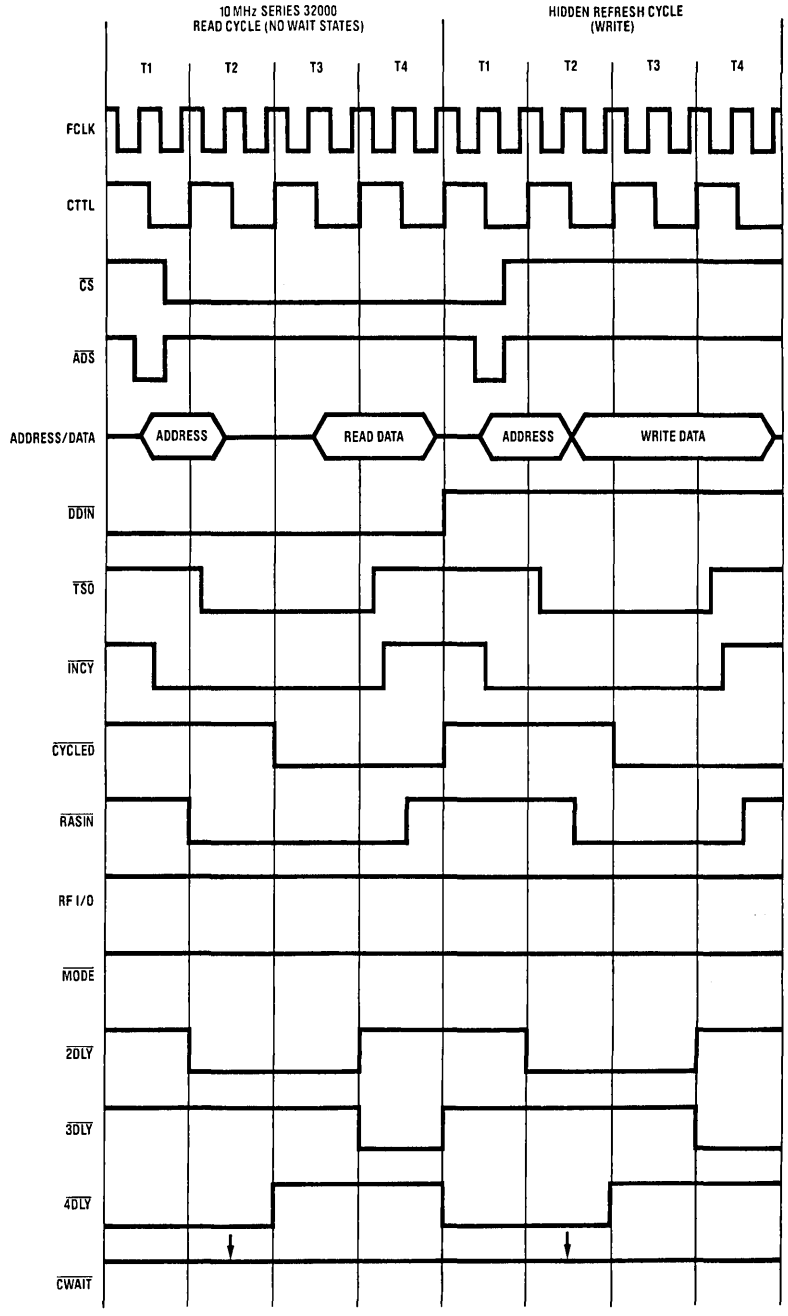
The output "$\overline{RASIN}$" (see pin list for DP84412) will be active low (inverted RASIN) when the output "$\overline{INCY}$" is low (making INCY high) AND the output "$\overline{MODE}$" is high AND the output "$\overline{4D}$" is low (making 4D high) AND the input $\overline{DDIN}$ is low (making DDIN high).

PAL Boolean Equations

```
PAL16R6A     ;FAST PAL
NEW PAL FOR THE NATIONAL SEMICONDUCTOR NS32016, 32008, 32032
NATIONAL SEMICONDUCTOR (WORKS UP 10 MHz)

FCLK /TSO RFIO /ADS /DDIN /WAITWR CTTL /CS /WAITRD GND
/OE /CWAIT 4DLY 3DLY 2DLY MODE RASIN CYCLED INCY VCC

RASIN := INCY*/CYCLED*/MODE*/CTTL*DDIN+      ;Start /RASIN fast during
                                             ; "READ" cycle
         INCY*/MODE*2DLY*/WAITWR+            ; ''WRITE'' cycle without WAIT states
         /CS•INCY•/MODE•2DLY+                ; Hidden Refresh /RASIN
         CS•INCY•/MODE•2DLY•WAITWR•/CTTL+    ; ''WRITE'' cycle with WAIT states
         RASIN•INCY•/MODE•2DLY               ; continue /RASIN

CYCLED := /MODE*2DLY*/WAITWR*/DDIN*/CTTL+        ;No WAITS inserted
          /MODE*2DLY*/WAITRD*DDIN*/CTTL+         ;No WAITS inserted
          /MODE*2DLY*4DLY*WAITRD*DDIN*/CTTL+     ;WAIT in READ cycle
          /MODE*2DLY*4DLY*WAITWR*DDIN*/CTTL+     ;WAIT in WRITE cycle
          CYCLED*TSO*/MODE+
          CYCLED*/MODE*CTTL

MODE := /RFIO*/INCY*/2DLY*/CTTL+             ;forced refresh during idle
                                             ;states, in long cycles,
        MODE*/3DLY+                          ;or at the end of a cycle
        MODE*/4DLY+
        MODE*CTTL

2DLY := MODE*/4DLY*/CTTL+
        2DLY*CTTL+
        INCY*/CYCLED*/MODE*/3DLY*4DLY*/CTTL+
        CS*DDIN*WAITRD*INCY*/MODE*2DLY*/3DLY*/4DLY+    ;extend 2DLY if
        CS*/DDIN*WAITWR*INCY*/MODE*2DLY*/3DLY*/4DLY    ; WAIT states
                                                       ;  are wanted

3DLY := 2DLY*/4DLY*/CTTL+
        3DLY*CTTL

4DLY := 3DLY*/CTTL+
        4DLY*CTTL+
        /INCY*/MODE*/CTTL+
        INCY*/MODE*/2DLY*/CTTL

IF (VCC) INCY = ADS*/MODE+
           CS*TSO*/CYCLED*/MODE*/2DLY*4DLY+    ;Start INCY for CS
           INCY*/CYCLED+                       ;access after forced
           INCY*2DLY                           ;refresh

IF (CS) CWAIT=CS*TSO*/CYCLED*/MODE*/2DLY*4DLY+  ;for Access during
                                                ;forced refresh
   CS*TSO*MODE+                                 ;during forced refresh
   CS*INCY*/CYCLED*DDIN*WAITRD*/MODE*2DLY*/3DLY*4DLY+
                                                ; /CS READ cycle with
                                                ; WAIT states
   CS*INCY*/CYCLED*/DDIN*WAITWR*/MODE*2DLY*/3DLY*4DLY
                                                ; /CS WRITE cycle with
                                                ; WAIT states
```

FIGURE 1. Equations for the Series 32000 Family Interface PAL

System Timing Diagrams



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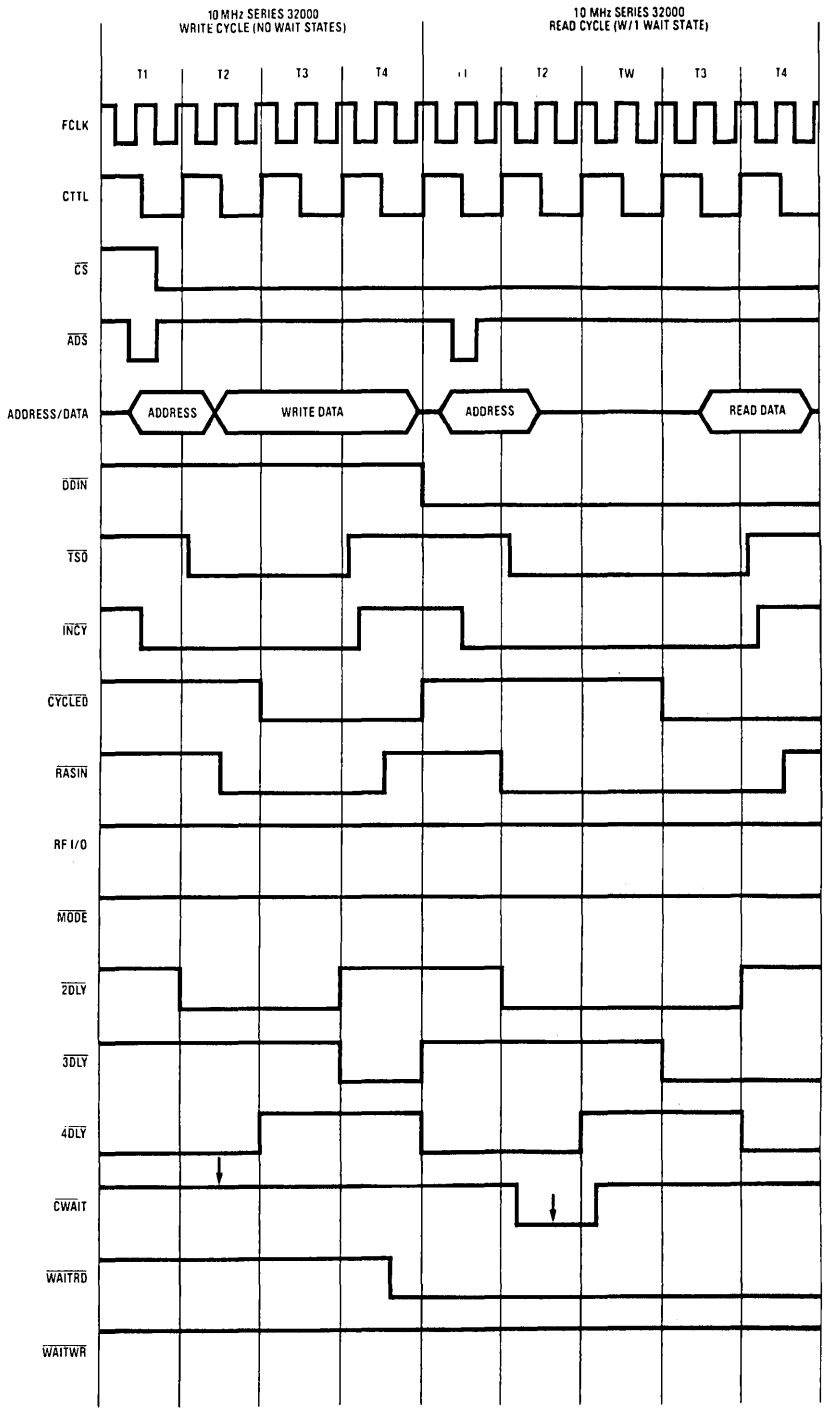
System Timing Diagrams (Continued)



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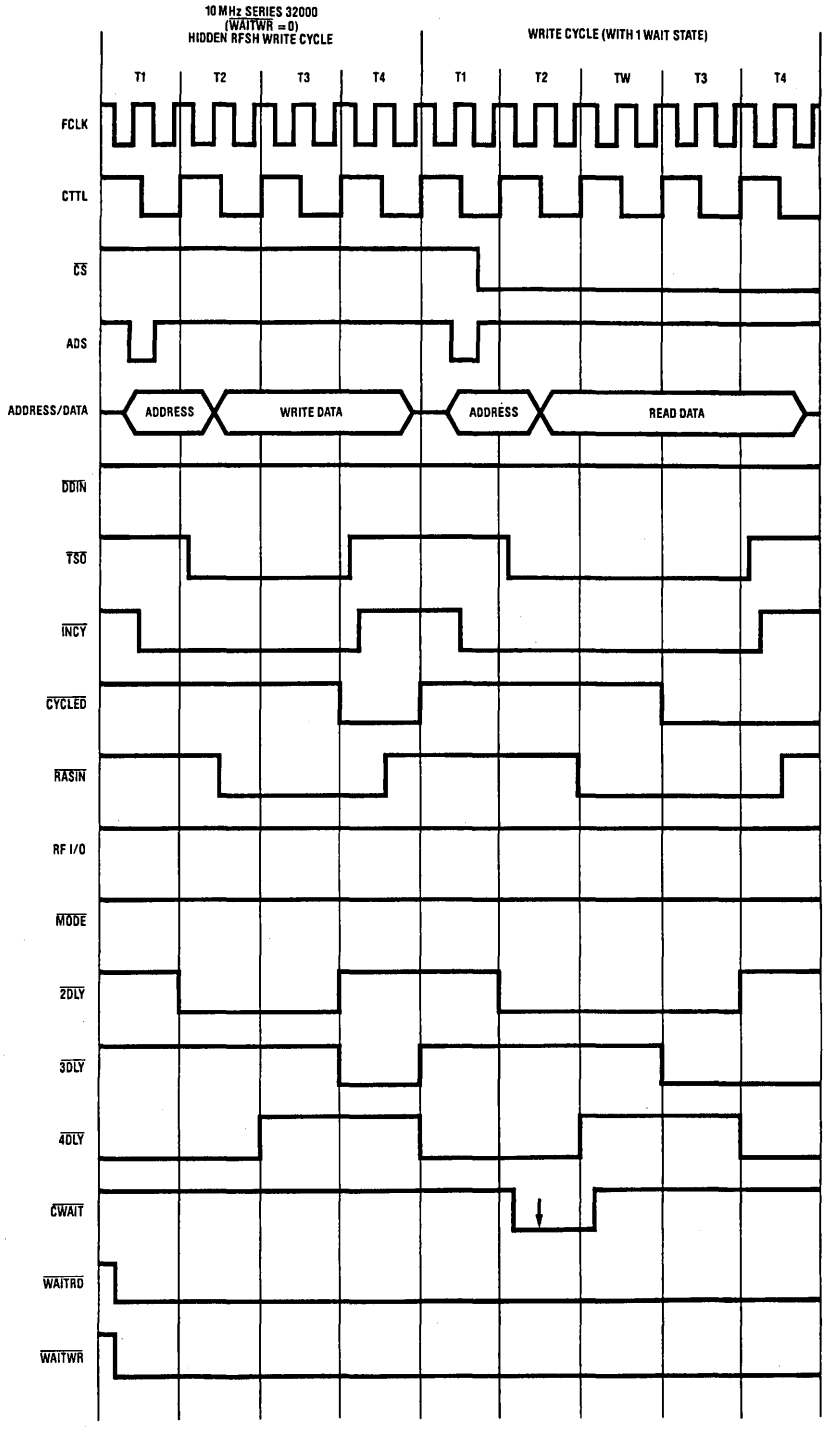
System Timing Diagrams (Continued)



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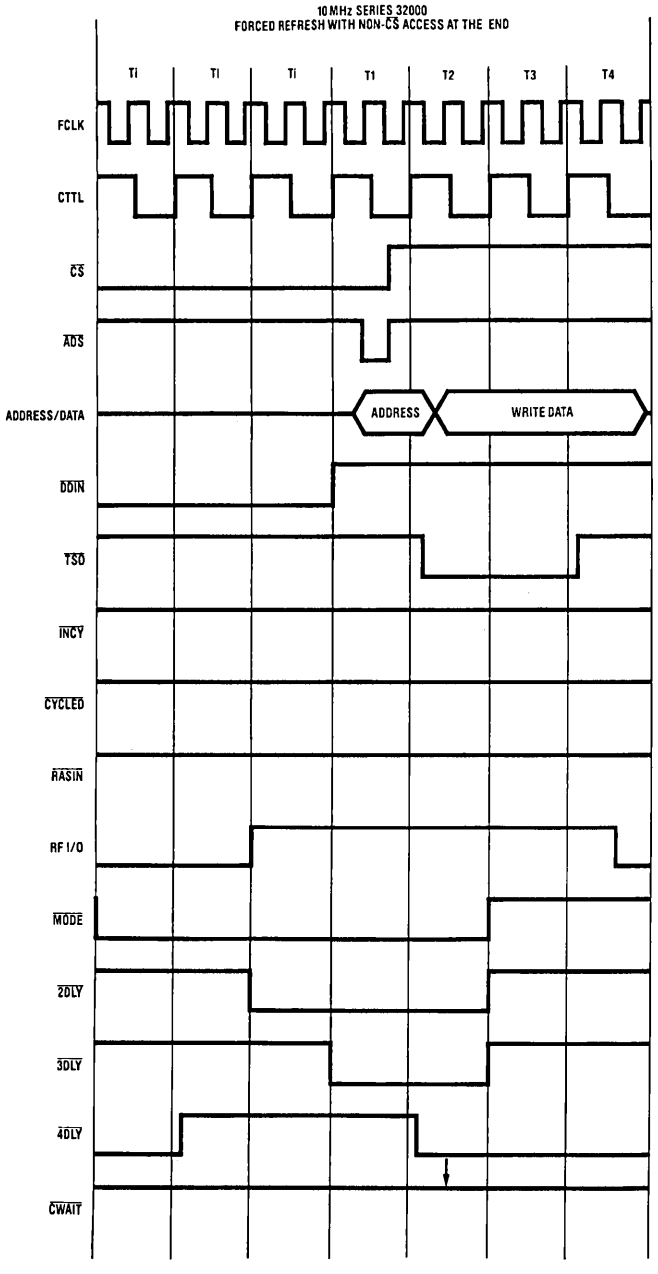
System Timing Diagrams (Continued)



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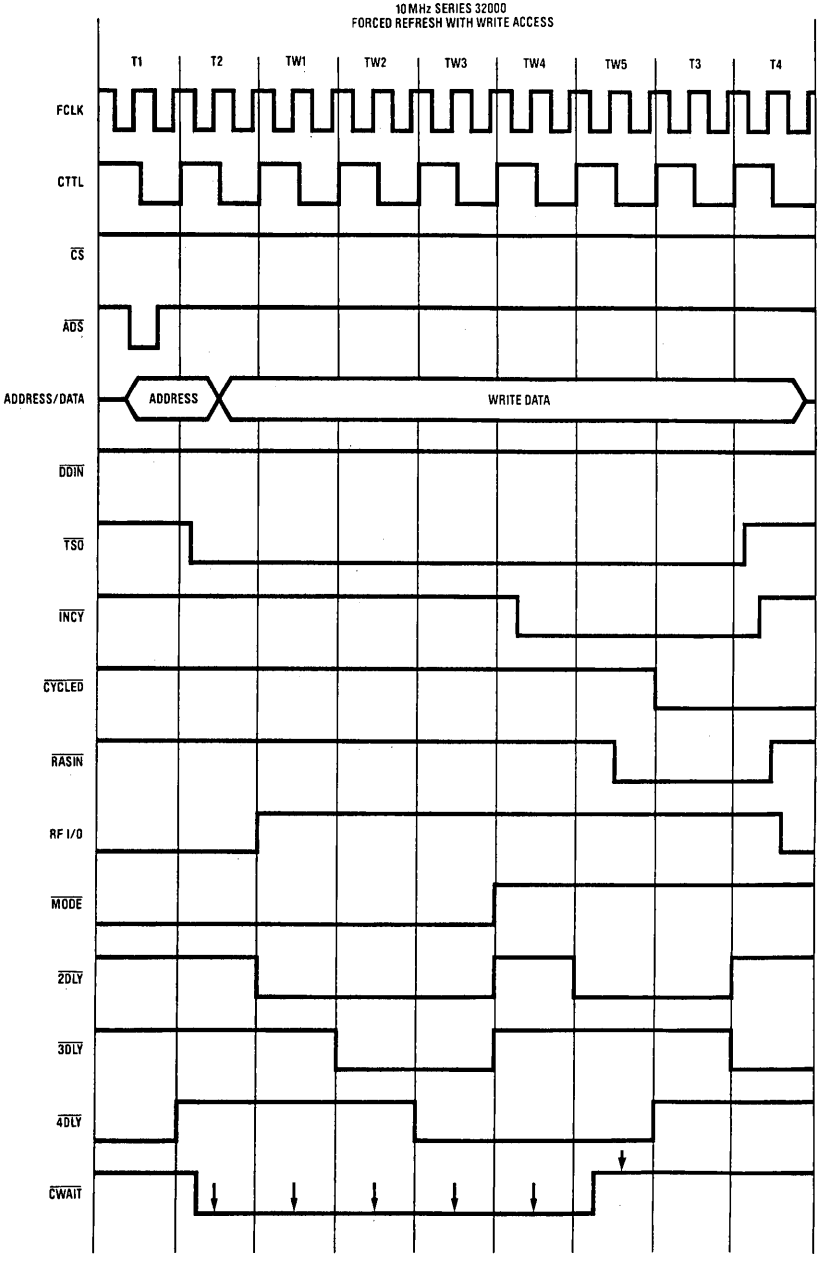
System Timing Diagrams (Continued)



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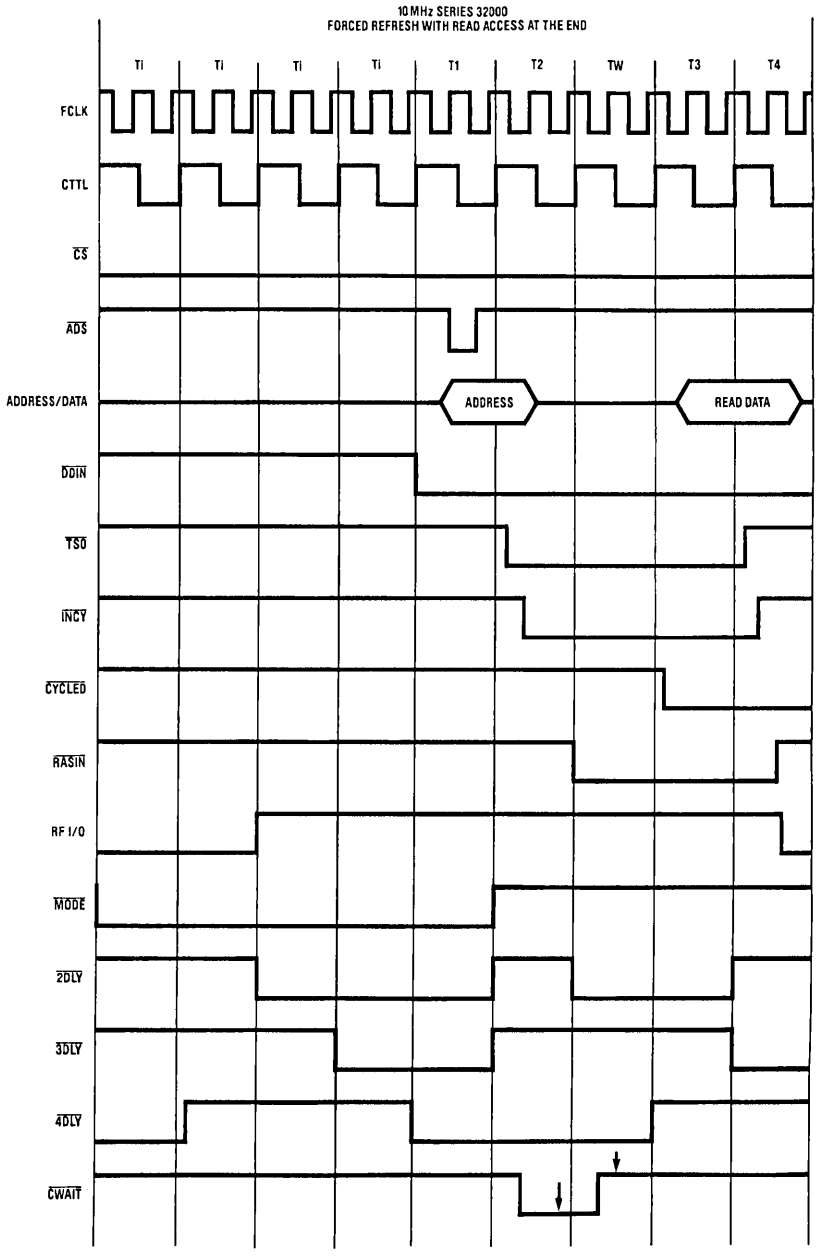
System Timing Diagrams (Continued)



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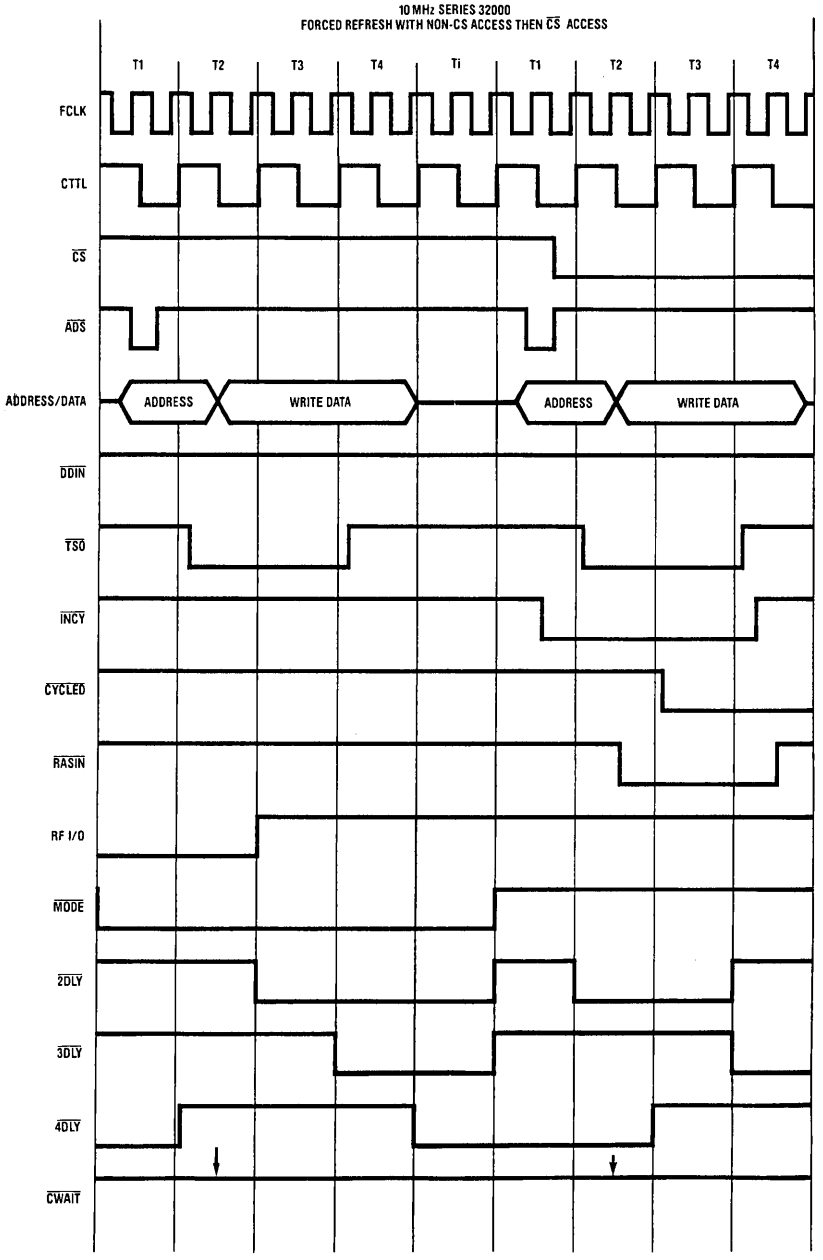
System Timing Diagrams (Continued)



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National Semiconductor Corporation

PRELIMINARY

DP84422 Dynamic RAM Controller Interface Circuit for the 68000/008/010 CPU(s)

General Description

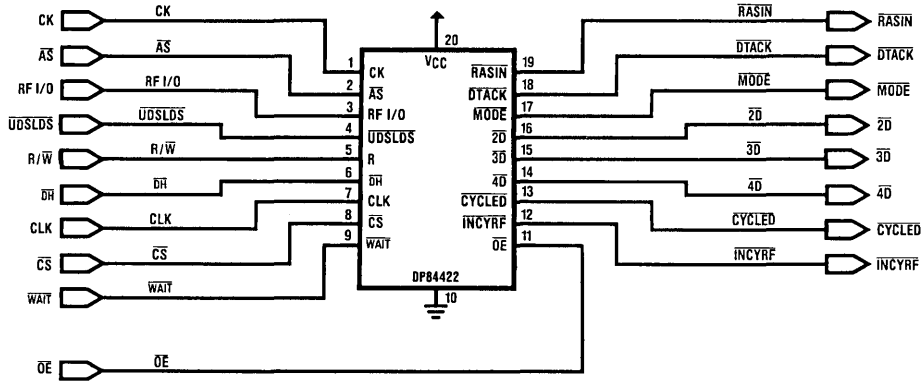
The DP84422 is a new Programmable Array Logic (PAL®) device, that replaces the DP84322, designed to allow an easy interface between the Motorola 68000 family of processors and the National Semiconductor DP8409A, DP8429, or DP8419 DRAM controller.

The new DP84422 supplies all the control signals needed to perform memory read, write, read modify write (as in the Test and Set, "TAS", instruction), and refresh and work with the 68000 family of processors up to 12.5 MHz. Logic is also included to insert WAIT states, if wanted, into the microprocessor READ or WRITE cycles when using fast CPUs.

Features

- Provides a 3-chip solution for the 68000 family, dynamic RAM interface (DP8409A or DP8419, DP84422, and clock divider).
- Works with all 68000 family speed versions up to 12.5 MHz.—(68008; 68000; and 68010).
- Operation of 68000 processor at 10 MHz with no WAIT states.
- Controls DP8409A or DP8419 Mode 5 accesses, hidden refreshes and Mode 1 Forced Refreshes automatically.
- Inserts WAIT states in READ or WRITE cycles automatically depending on when $\overline{WAIT}$ is low, or if chip select becomes active during a forced Refresh cycle.
- Uses a standard National Semiconductor PAL part (DMPAL16R4A).
- The PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new very high speed PALs ("B" PAL parts).

Connection Diagram



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Order Number DP84422J or DP84422N
See NS Package J20A or N20A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	Operating	Programming		Operating	Programming
Supply Voltage, V_{CC}	7V	12V	Off-State Output Voltage	5.5V	12V
Input Voltage	5.5V	12V	Storage Temperature Range	−65°C to +150°C	

Recommended Operating Conditions

Symbol	Parameter		Commercial			Units
			Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
t_w	Width of Clock	Low	15	10		ns
		High	15	10		
t_{su}	Setup Time from Input or Feedback to Clock		25	16		ns
t_h	Hold Time		0	−10		ns
T_A	Operating Free-Air Temperature		0	25	75	°C
T_C	Operating Case Temperature					°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −3.2 mA COM	2.4	2.8		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 24 mA COM		0.3	0.5	V
I_{OZH}	Off-State Output Current	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.4V			−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.02	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max			120	180	mA

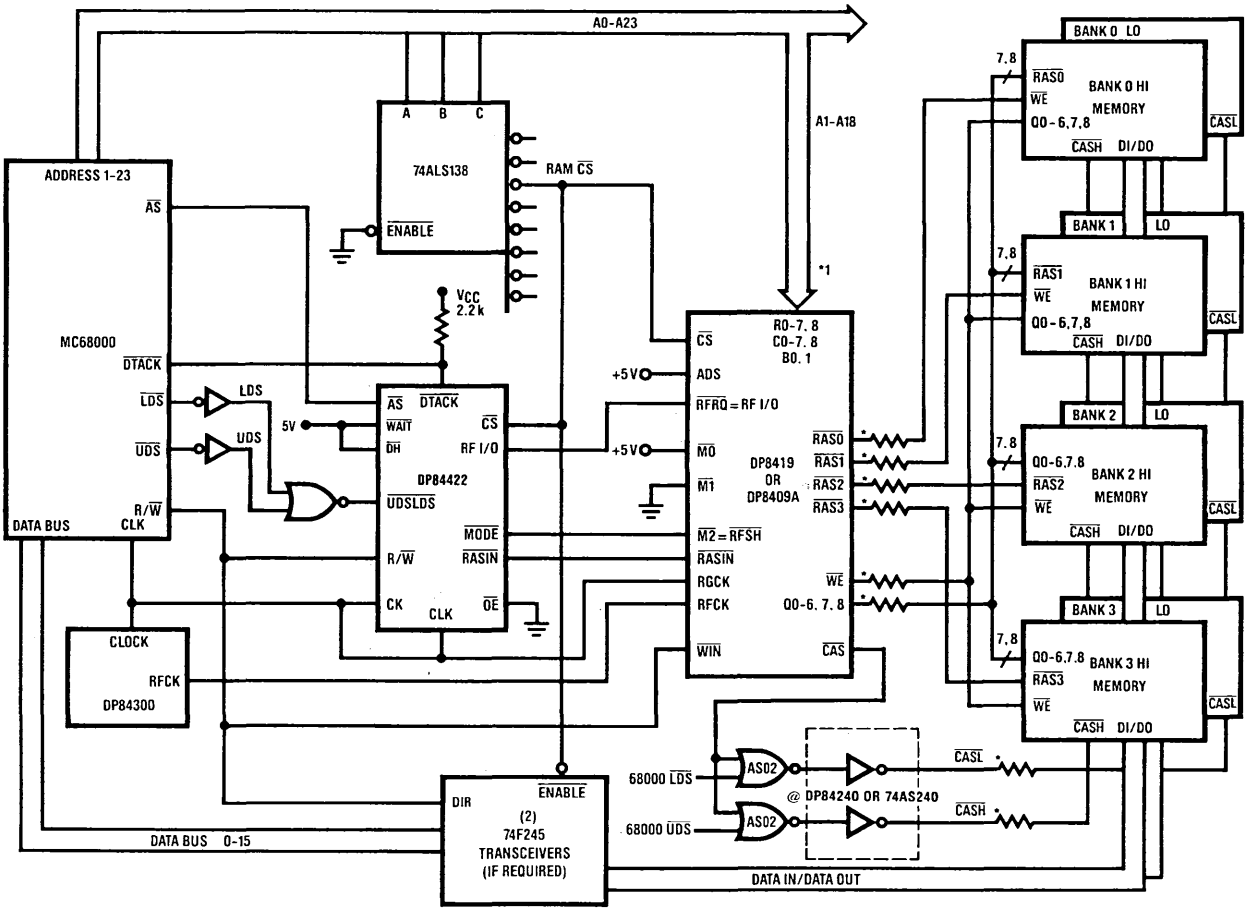
Switching Characteristics Over Recommended Ranges of Temperature and V_{CC}

V_{CC} = 5V ± 10% Commercial: T_A = 0 to 75°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions R1, R2	Commercial			Units
			Min	Typ	Max	
t_{PD}	Input or Feedback to Output	CL = 50 pF		15	25	ns
t_{CLK}	Clock to Output of Feedback			10	15	ns
t_{PZX}	Pin 11 to Output Enable			10	20	ns
t_{PXZ}	Pin 11 to Output Disable	C_L = 5 pF		11	20	ns
t_{PZX}	Input to Output Enable	C_L = 50 pF		10	25	ns
t_{PXZ}	Input to Output Disable	C_L = 5 pF		13	25	ns
f_{MAX}	Maximum Frequency		25	30		ns

V_{CC} = Max. at minimum temperature

ALL IC'S DECOUPLED
* SERIES DAMPING RESISTERS
*1 TIE UNUSED ADDRESS LINES TO V_{CC}
@ For maximum speed use 1 driver per 1/2 bank of DRAM.
This circuit provides direct support of the 68000 Test and Set Instruction using PAGE MODE DRAMs.



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Mnemonic Description

INPUT SIGNALS

1) "CLK", "CK" This is the 68000 CPU clock.
2) "$\overline{AS}$" This is the 68000 address strobe pin. This signal also tells when the 68000 is in a cycle.
3) "$\overline{CS}$" This is the chip select signal for the DP8409A.
4) "R" This is the READ/$\overline{WRITE}$ pin from the 68000.
5) "RFIO" This is the RFIO, used as refresh request, from the DP8409A.
6) "$\overline{WAIT}$" This pin allows the insertion of 1 WAIT state in a $\overline{CS}$ Access cycle if low. As an example; if the user wants 1 WAIT state in READ accesses but 0 WAIT states in WRITE accesses he can invert the "R/$\overline{W}$" input to this input.
7) "$\overline{UDSLDS}$" This input was produced by inverting the two terms $\overline{UDS}$ and $\overline{LDS}$ and then logically "NOR"ing them together. This input is low whenever one or both $\overline{UDS}$ or $\overline{LDS}$ are low. This pin is used in order to support the 68000 "TAS" instruction. This signal is used in the "$\overline{DTACK}$" PAL output.
8) "$\overline{DH}$" This input allows the user to disable the DP8409A/19 hidden refresh, when low, provided he also ties "$\overline{CS}$" low on the DP8409A/19. When this input is low "$\overline{RASIN}$" is only brought low when a "$\overline{CS}$" access ("$\overline{CS}$" input to PAL low) is in progress
9) "$\overline{OE}$" Must be tied low to enable DP84422 outputs.

OUTPUT SIGNALS

1) "$\overline{CYCLED}$" This signal goes low once a hidden refresh or an access has been done as indicated by $\overline{2DLY}$ and $\overline{3DLY}$ being low. This signal goes high once the cycle is over as indicated by $\overline{AS}$ going high. See also "$\overline{DH}$ input
2) "$\overline{RASIN}$" This signal goes low following $\overline{AS}$ during an access or hidden refresh. See also "$\overline{DH}$" input.
3) "$\overline{DTACK}$" This signal causes WAIT states to be inserted into the 68000 processor cycles if it is not low a setup time before S4 falling clock edge.
4) "$\overline{INCYRF}$" This signal indicates that an access has been requested during a forced refresh cycle. This signal is used to insert WAIT states during the forementioned condition or to prevent a "non-$\overline{CS}$" access cycle from automatically starting.
5) "$\overline{MODE}$" This signal is used to pull the DP8409A pin M2 low in order to go to mode 1 to do a forced refresh.
6) "$\overline{2DLY}$" This signal is an internal delay.
7) "$\overline{3DLY}$" This signal is an internal delay.
8) "$\overline{4DLY}$" This signal is an internal delay.

Functional Description

The following description applies to both the DP8409A, DP8429, and the DP8419 dynamic RAM controllers.

A memory cycle starts when chip select ($\overline{CS}$) and address strobe ($\overline{AS}$) are true. $\overline{RASIN}$ is supplied from the DP84422 to the DP8409A dynamic RAM controller, which then supplies a $\overline{RAS}$ signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8409A switches the address outputs to the column address. The DP8409A then supplies the required $\overline{CAS}$ signal to the DRAM. In order to do byte operations it is suggested that the user provide external logic, as shown in the system block diagram, to produce a HIGH CAS and a LOW CAS. To differentiate between a READ and a WRITE, the R/$\overline{W}$ signal from the CPU is used.

A refresh cycle is started by one of two conditions. The refresh cycle caused by the first condition is called a hidden refresh. This occurs when refresh clock (RFCK) is high, $\overline{CS}$ is not true, and $\overline{RASIN}$ goes low. Here the CPU is accessing something else in the system and the DRAM can be refreshed at that time, thereby being transparent to the CPU. The second type of refresh is called forced refresh. This occurs if no hidden refresh was performed while RFCK was high. When RFCK transitions low a refresh request (RFRQ) is generated. If there is not a DRAM access in progress the DP84422 will force a refresh by putting the DP8409A into mode 1 (automatic forced refresh mode). If the CPU tries to access the DRAM during a forced refresh cycle WAIT states will be inserted into its cycles until the forced refresh is over and the DRAM $\overline{RAS}$ precharge time has been met. Then the pending DRAM access will be allowed to take place.

The DP84422 also allows forced refreshes to take place during long accesses of other devices. For instance, if EEPROM takes several microseconds to write to, the DRAM will still be refreshed while that access is in progress.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories or allow time to generate parity. This is accomplished by inserting a WAIT state into the processor access cycle. The DP84422 can insert WAIT states into either READ cycles, WRITE cycles, READ MODIFY WRITE cycles, or both READ and WRITE cycles or the READ and WRITE portion of a READ MODIFY WRITE cycle. The extra WAIT state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

During a Test and Set instruction $\overline{CAS}$ is generated twice while $\overline{RAS}$ is low. In order for this instruction to execute properly Page Mode DRAMs must be used.

System Interface Description

All members of the Motorola 68000 family of processors are able to use the DP84422.

$\overline{RASIN}$ during a READ cycle will always start at the beginning of the "S3" processor cycle. The user must guarantee that $\overline{CS}$ is valid a minimum of 30 ns before $\overline{RASIN}$ becomes valid, unless the PAL "$\overline{DH}$" input is low and the DP8409A/19 "$\overline{CS}$" input is tied low (hidden refresh disabled).

System Interface Description (Continued)

Several critical parameters in this application involve the input system CLOCK and the ADDRESS STROBE, $\overline{AS}$. These parameters become most critical at higher frequencies (10 MHz and above) where it is suggested that they are directly connected to the corresponding pins of the Motorola 68000 family ICs.

This section of the data sheet goes through the calculation of the "t_{RAC}" ($\overline{RAS}$ access time) and "t_{CAC}" ($\overline{CAS}$ access time) required by the DRAM for the 68000 family CPUs to operate at a particular clock frequency without introducing wait states into the processor access cycles. Both "t_{RAC}" and "t_{CAC}" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "t_{RAC}" and "t_{CAC}" parameters calculated. In order to determine the "t_{RAC}" and "t_{CAC}" needed the DP8419 and fast PALs ("B" type PALs) timing parameters were used. If the user is using the DP8408A/09A or a slower PAL device he should substitute their respective delays into the equation below.

Most all of the calculations contained in this note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from RAH exceeded 200 ns. This is because DRAMs can be found with row access times up to 150 ns that require only 15 ns row address hold times.

The calculated "t_{RAC}" and "t_{CAC}" may differ from the actual system values depending upon the external circuitry used to produce "$\overline{CASH}$" and "$\overline{CASL}$". The DP8409A/19 "$\overline{RASIN}$–$\overline{CAS}$" low will be approximately 10–15 ns less than the value given in the data sheet because of the small loading on the DP8409A/19 "$\overline{CAS}$" output. The external circuitry needed to produce "$\overline{CASH, L}$" should be loaded such that the column address (from DP8409A/19 is valid when "$\overline{CASH, L}$" goes low. For this reason "$\overline{RASIN}$–$\overline{CASH, L}$" may be longer than the value used in the "t_{RAC}, t_{CAC}" calculations, and therefore may give a smaller "t_{RAC}, t_{CAC}" then was calculated.

EXAMPLE DRAM TIMING CALCULATIONS

A) 8 MHz 68000, No WAIT States

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 125 + 60 + 15 = 220 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 15 ns minimum

"t_{RAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (min) − #1 − #2 − #4 − #5
= 125 + 125 + 125 + 55 − 200 − 20 − 7 − 15
= 188 ns

"t_{CAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (min) − #1 − #3 − #4 − #5
= 125 + 125 + 125 + 55 − 200 − 77 − 7 − 15
= 131 ns

Therefore the DRAM chosen should have a "t_{RAC}" less than or equal to 188 ns and a "t_{CAC}" less than or equal to 131 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one and one half clock periods = 125 + 55 = 180 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 125 + 55 + 35 = 215 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns (maximum $t_{RPDL} - t_{RPDH}$ for the DP8409-2) = 250 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 250 − 70 = 180 ns.

The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times, the $\overline{CAS}$ pulse width, and the $\overline{RAS}$ pulse width would be increased by one clock period (125 ns in this case). A WAIT state in WRITE cycles would just increase the $\overline{RAS}$ and $\overline{CAS}$ precharge by one clock period.

B) 10 MHz 68000, No WAIT states

#1) $\overline{RASIN}$ low = S0 + S1 + $\overline{AS}$ low (maximum) + "B" PAL combinational output delay maximum = 100 + 55 + 15 = 170 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time = 10 ns minimum

"t_{RAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) + S6 (min) − #1 − #2 − #4 − #5
= 100 + 100 + 100 + 45 − 170 − 20 − 7 − 10
= 138 ns

"t_{CAC}" = (S0 + S1) + (S2 + S3) + (S4 + S5) − S6 (min) − #1 − #3 − #4 − #5
= 100 + 100 + 100 + 45 − 170 − 77 − 7 − 10
= 81 ns

Therefore the DRAM chosen should have a "t_{RAC}" less than or equal to 138 ns and a "t_{CAC}" less than or equal to 81 ns. Standard 120 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one and one half clock periods = 100 + 45 = 145 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8419) = 100 + 45 + 35 = 180 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns (maximum $t_{RPDL} - t_{RPDH}$ for the DP8419) = 200 − 5 = 195 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 50 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8419) = 200 − 50 = 150 ns.

The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times, the $\overline{CAS}$ pulse width, and the $\overline{RAS}$ pulse width would be increased by one clock period (100 ns in this case). A WAIT state in WRITE cycles would just increase the $\overline{RAS}$ and $\overline{CAS}$ precharge by one clock period.

Interpreting the DP84422 PAL Equations

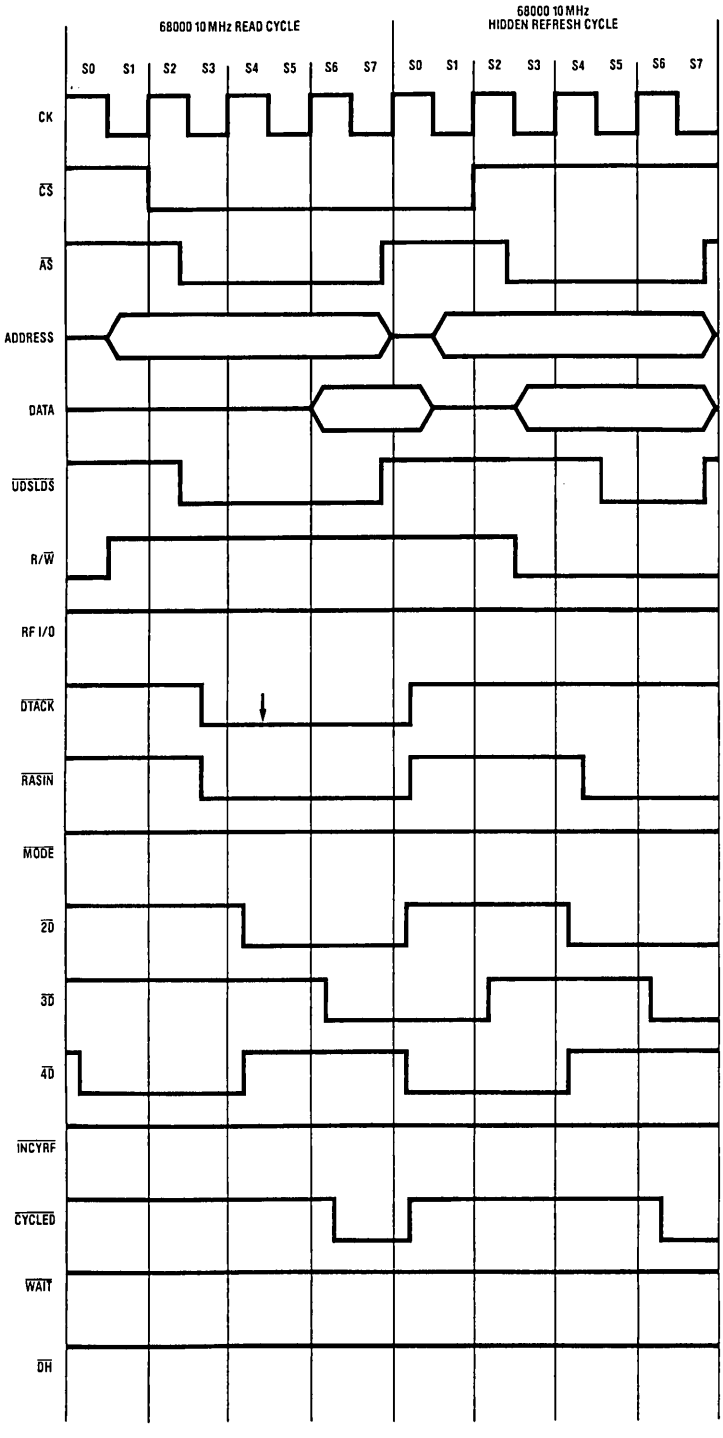
The boolean equations for the DP84422 were written using the standard PALASM™ format. In other words the equation: "IF (VCC) RASIN = INCY *$\overline{MODE}$*4D*$\overline{R}$" will mean;

The output "$\overline{RASIN}$" (see pin list for DP84422) will be active low (inverted $\overline{RASIN}$) when the output "$\overline{INCY}$" is low (making INCY high) AND the output "$\overline{MODE}$" is high AND the output "$\overline{4D}$" is low (making 4D high) and the input R/$\overline{W}$ is low (making $\overline{R}$ high).

```
PAL16R4A ; FAST PAL
NEW PAL FOR THE MOTOROLA 68000 PROCESSOR
(WORKS UP TO 12.5MHZ)
CK /AS RFIO /UDSLDS R /DH CLK /CS /WAIT GND
/OE /INCYRF /CYCLED /4DLY /3DLY /2DLY /MODE /DTACK /RASIN VCC
IF (VCC) RASIN =
 CS*/INCYRF*AS*/MODE*4DLY*/CYCLED*/CLK+          ;Start RASIN
 /CS*/INCYRF*AS*/MODE*2DLY*/CYCLED*/DH+          ;RASIN for Hidden RFSH
 CS*INCYRF*AS*/MODE*4DLY*/CYCLED*/CLK+           ;Start RASIN after RFSH
 CS*RASIN*/MODE*AS+                              ;Hold RASIN valid
 RASIN*/MODE*2DLY                                ;Hold RASIN valid

IF (VCC) CYCLED =/MODE*2DLY*3DLY*/4DLY+          ;Start "CYCLED", does not allow
                 CYCLED*AS+                      ;  glitch after refresh
                 /MODE*CYCLED*/CLK+              ;End on rising edge of CLK
                 /CS*AS*/MODE*/2DLY*/3DLY*/4DLY  ;Start during long accesses of other
                                                 ; devices

IF (VCC) INCYRF =MODE*AS+                        ;Set Access during Refresh
                 INCYRF*4DLY*AS                  ;Hold it while 4DLY is low

IF (CS) DTACK = AS*/WAIT*/R*/MODE*/CLK+          ;0 WAIT's for WRITE
        AS*WAIT*/R*/MODE*2DLY*/CLK+              ;1 WAIT for WRITE
        UDSLDS*/WAIT*R*/MODE*/CLK+               ;0 WAIT's for READ
        UDSLDS*WAIT*R*/MODE*2DLY*/CLK+           ;1 WAIT for READ
        DTACK*2DLY*/MODE+                        ;Continue DTACK
        DTACK*AS*RASIN*/MODE*/CYCLED+            ;Continue DTACK
        DTACK*AS*/R*/MODE                        ;Continue DTACK in RMW
                                                 ;  cycle
MODE : = /RFIO*/AS*/CYCLED*/RASIN+               ;For IDLE states or beginning
                                                 ;  states of 68000 cycle
        /CS*/RFIO*AS*CYCLED*/2DLY*/3DLY*/RASIN+  ;For RFSH during long cycles
                                                 ;  of other devices
        MODE*/3DLY+
        MODE*/4DLY
2DLY : = MODE*/4DLY+
        /INCYRF*AS*/CYCLED*/MODE*/3DLY*4DLY+     ;Start 2DLY
        CS*INCYRF*AS*/CYCLED*/MODE*/3DLY*4DLY+   ;Start 2DLY after RFSH
        /MODE*2DLY*/3DLY+
        CS*WAIT*AS*/MODE*2DLY*3DLY*/4DLY+        ;Make 2DLY longer
        CS*AS*/R*CYCLED*/MODE*/2DLY*/3DLY*/4DLY  ;Start second 2DLY for
                                                 ;the TAS instruction
3DLY : = 2DLY*/4DLY
4DLY : = 3DLY+
         /AS*/MODE+
         /CS*/RFIO*AS*CYCLED*/2DLY*/3DLY*/RASIN*/MODE ;Need for beginning of forced refresh to
                                                 ; inhibit "2DLY"
```

FIGURE 1. Equations for New 68000 PAL That Supports the 68000 "TAS" Instruction

System Timing Diagrams



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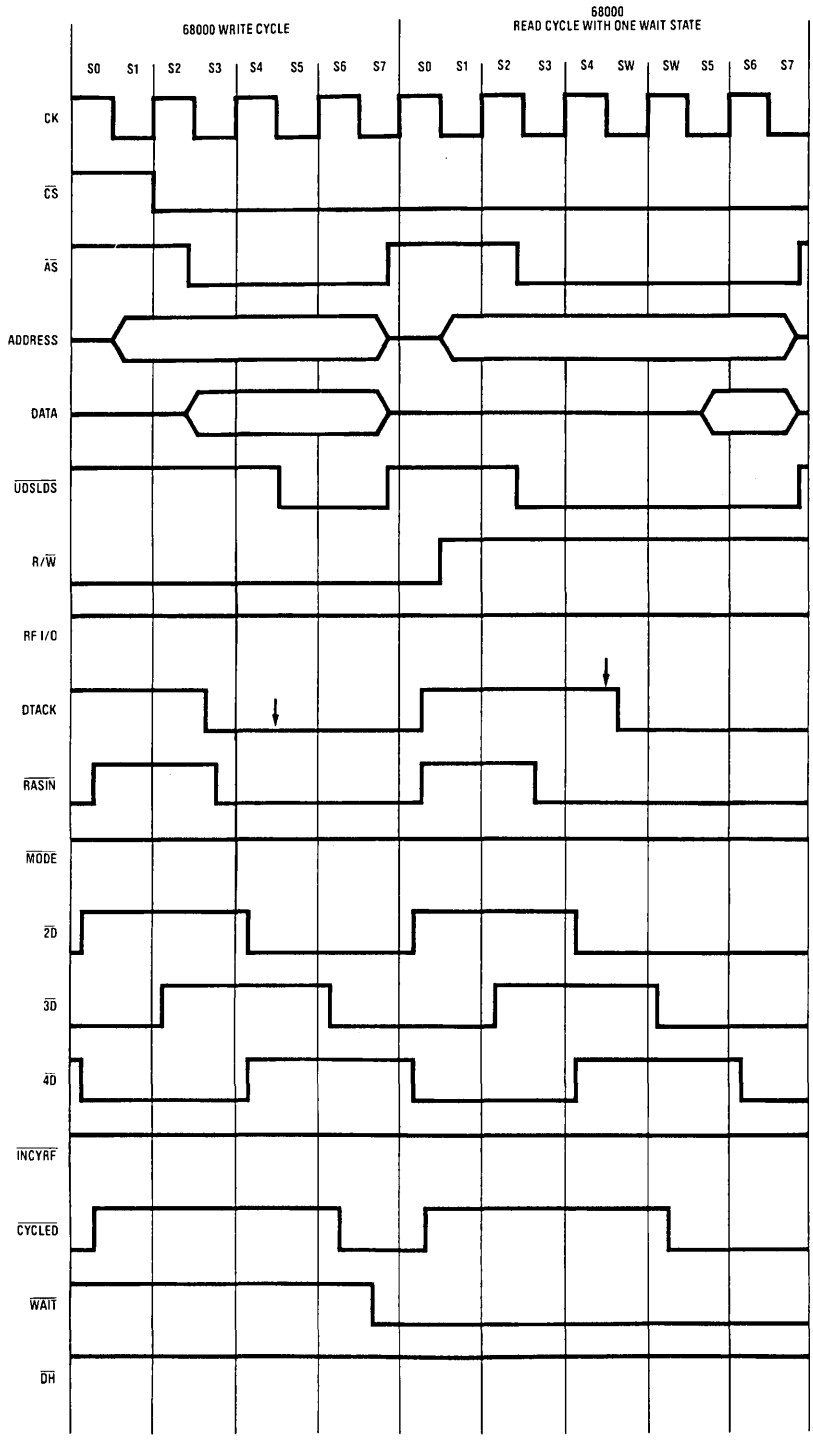
System Timing Diagrams (Continued)



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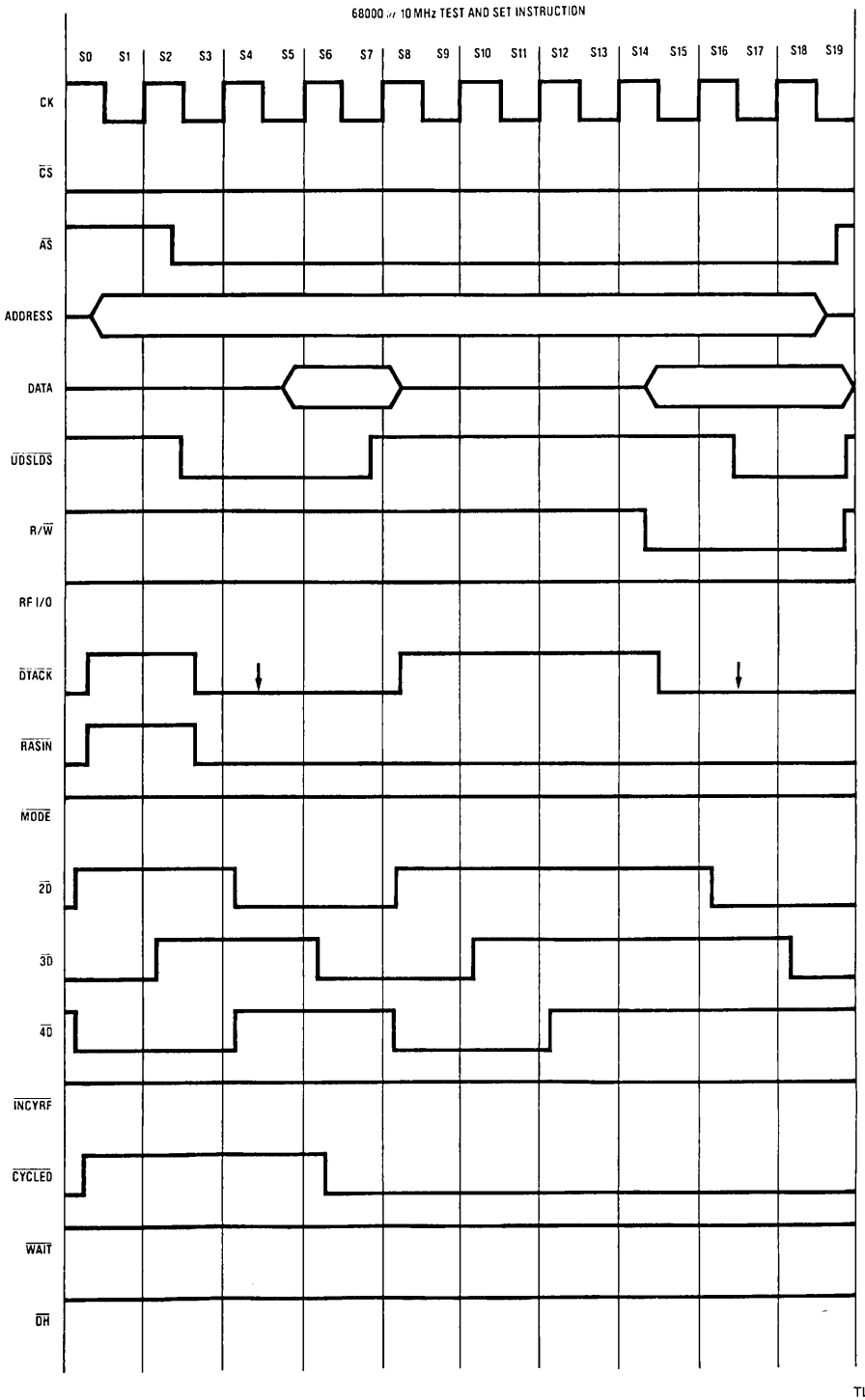
System Timing Diagrams (Continued)



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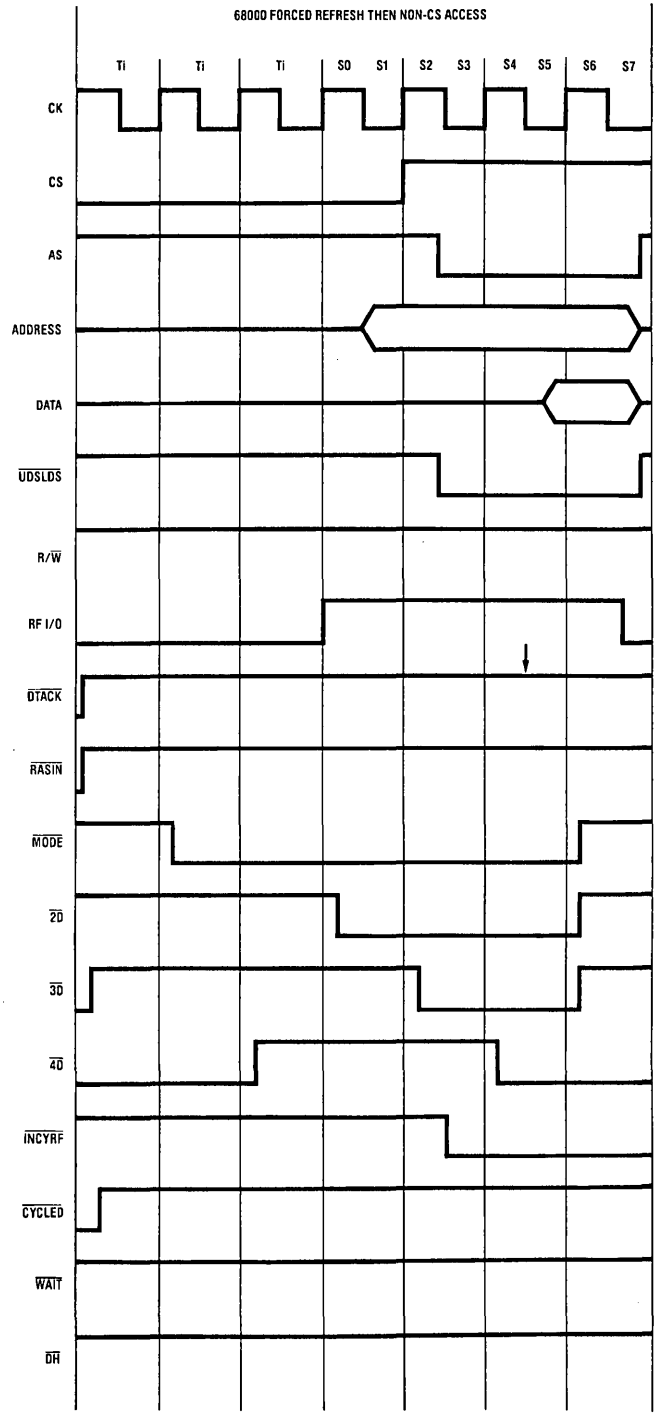
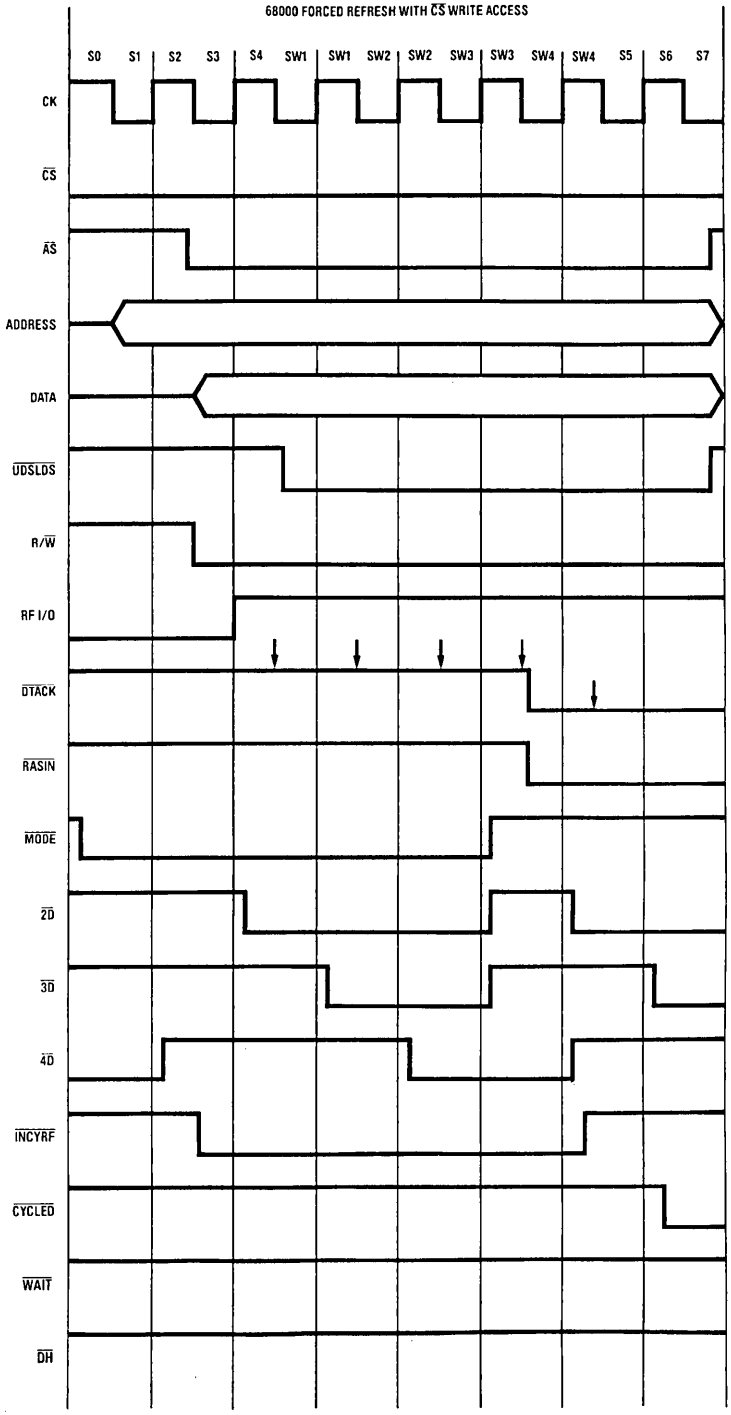
System Timing Diagrams (Continued)



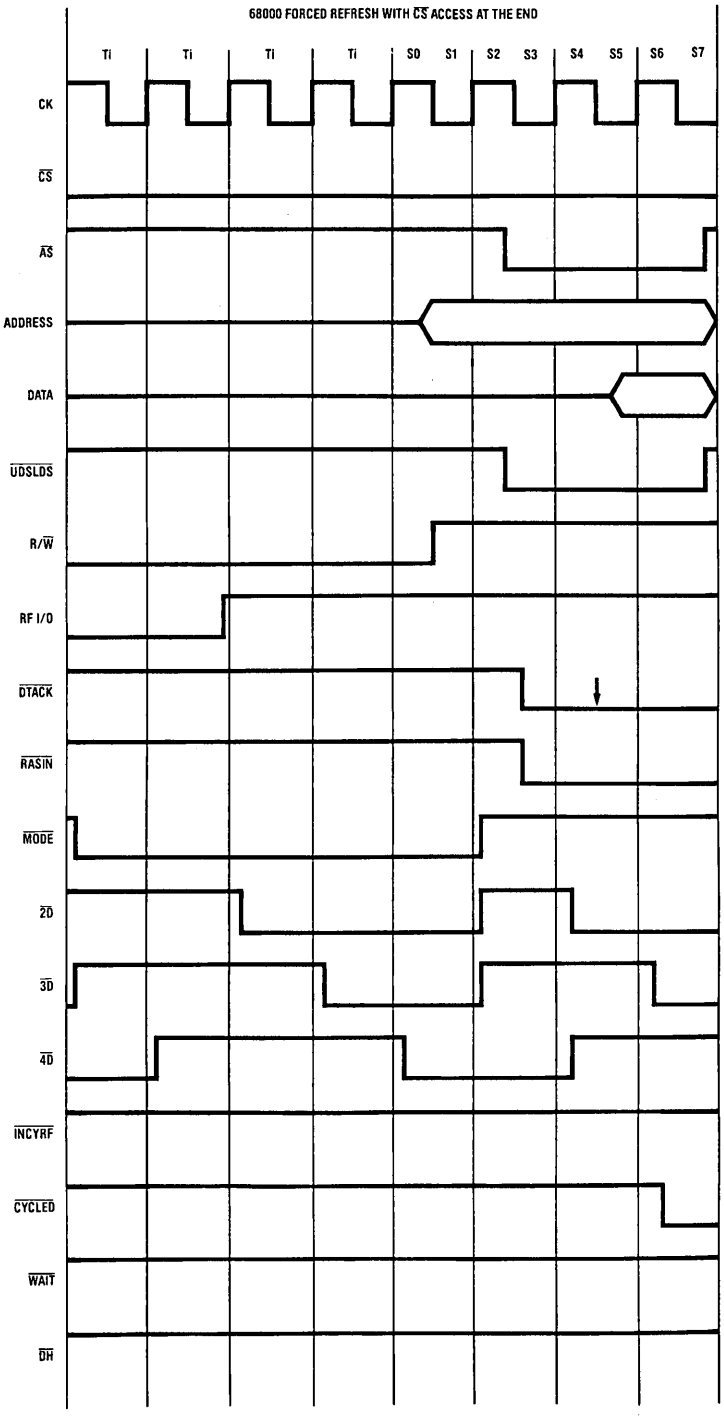
TL/F/8398–6

System Timing Diagrams (Continued)



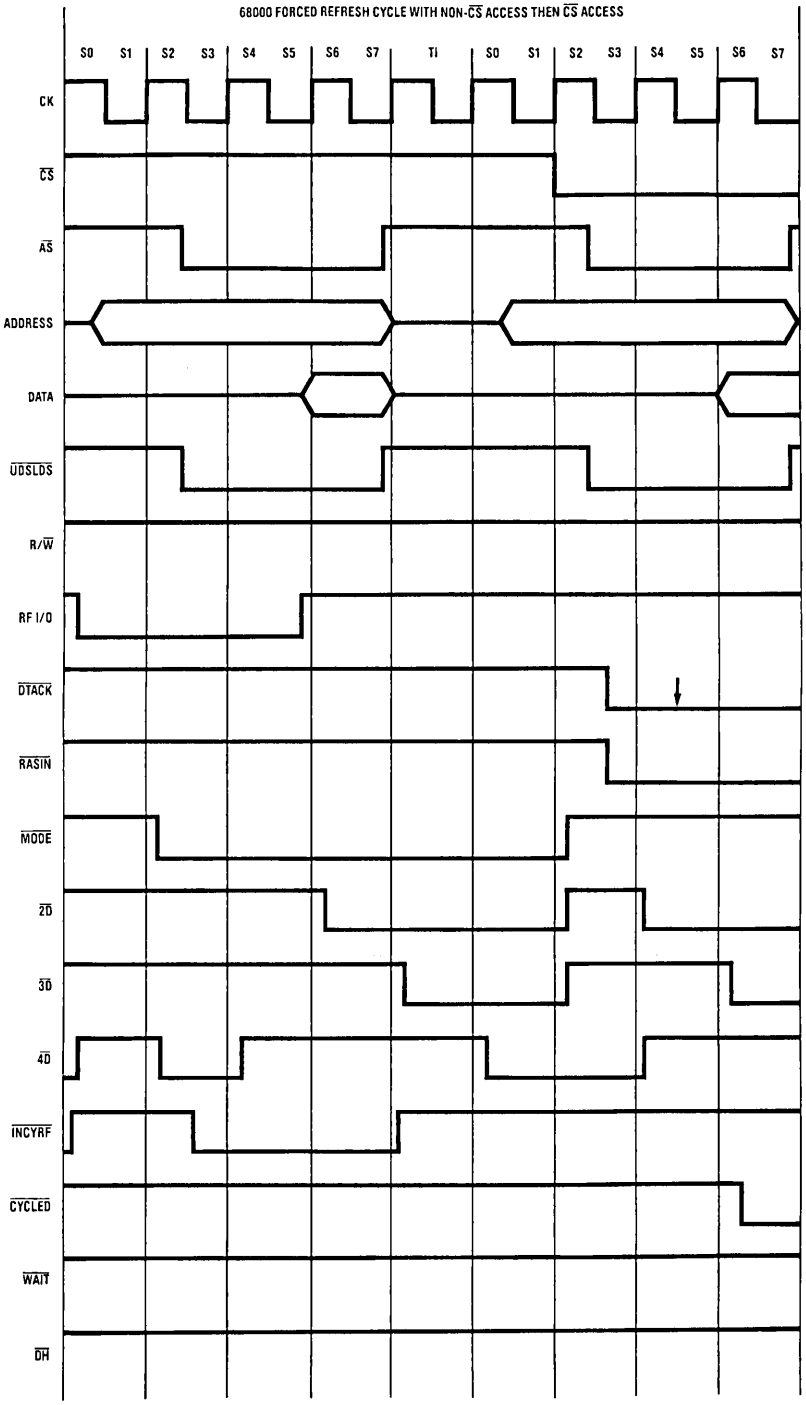
TL/F/8398–7

System Timing Diagrams (Continued)



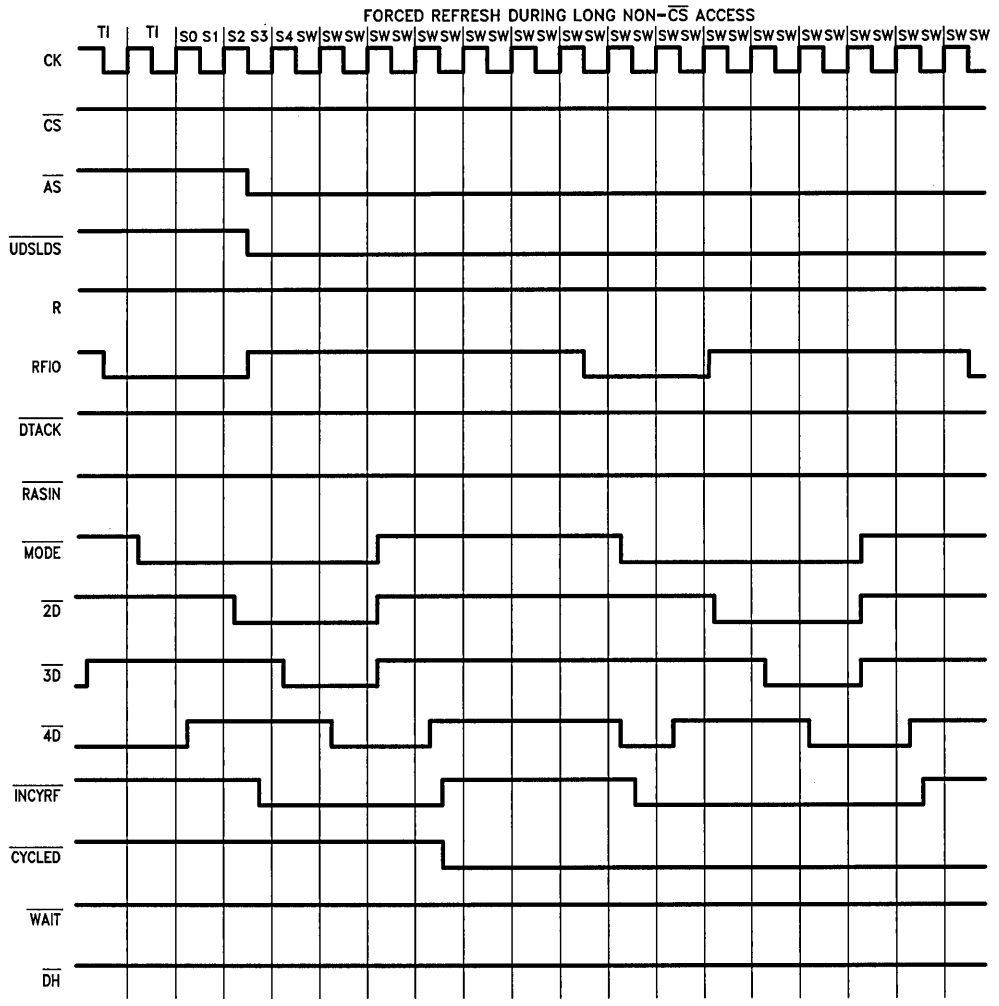
TL/F/8398–8

System Timing Diagrams (Continued)



TL/F/8398–9

System Timing Diagrams (Continued)



TL/F/8398–10

National Semiconductor Corporation

PRELIMINARY

DP84432 Dynamic RAM Controller Interface Circuit for the 8086/8088/80186/80188 CPU's

General Description

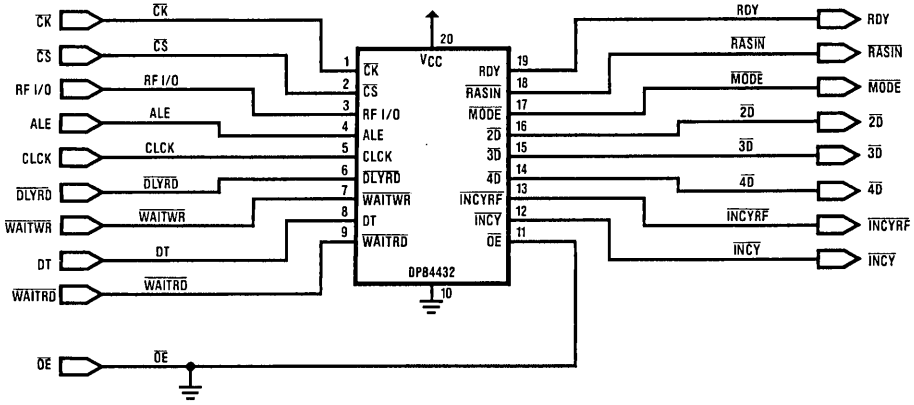
The DP84432 is a new Programmable Array Logic (PAL®) device, that replaces the DP84332, designed to allow an easy interface between the Intel 8088, 8086, 80188, 80186 CPU's and the National Semiconductor DP8409A, DP8429, or DP8419 DRAM controller.

The new DP84432 supplies all the control signals needed to perform memory read, write and refresh and work with the Intel processors up to 10 MHz. Logic is also included to insert WAIT states, if wanted, into the microprocessor READ or WRITE cycles when using fast CPU's.

Features

- Provides a 3-chip solution for the 8086 family, dynamic RAM interface (DP8409A or DP8419, DP84432, and clock divider)
- Works with all 8086 family speed versions up to 10 MHz
- Operation of 8086, 8088, 80186, 80188 at 10 MHz with no WAIT states
- Controls DP8409A or DP8419 Mode 5 accesses, hidden refreshes and Mode 1 Forced Refreshes automatically
- Inserts WAIT states in READ or WRITE cycles automatically depending on whether WAITRD or WAITWR are low, or if $\overline{CS}$ becomes active during a forced Refresh cycle
- Uses a standard National Semiconductor PAL part (DMPAL16R4A)
- The PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new very high speed PALs ("B" PAL parts)

Connection Diagram



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Order Number DP84432N or DP84432J
See NS Package Number N20A or J20A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

	Operating	Programming
Supply Voltage, V_{CC}	7V	12V
Input Voltage	5.5V	12V
Off-State Output Voltage	5.5V	12V
Storage Temperature Range	−65°C to +150°C	

DP84432 Recommended Operating Conditions

Symbol	Parameter		Commercial			Units
			Min	Typ	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
t_w	Width of Clock	Low	15	10		ns
		High	15	10		
t_{su}	Setup Time from Input or Feedback to Clock		25	16		ns
t_h	Hold Time		0	−10		ns
T_A	Operating Free-Air Temperature		0	25	75	°C
T_C	Operating Case Temperature					°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min., V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −3.2 mA COM	2.4	2.8		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min., V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = −24 mA COM		0.3	0.5	V
I_{OZH}	Off-state Output Current	V_{CC} = Max., V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.4V			−100	μA
I_I	Maximum Input Current	V_{CC} = Max., V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.4V				25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V			−0.02	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V V_O = 0V		−30	−70	−130	mA
I_{CC}	Supply Current†	V_{CC} = Max.			120	180	mA

Switching Characteristics Over Recommended Ranges of Temperature and V_{CC}

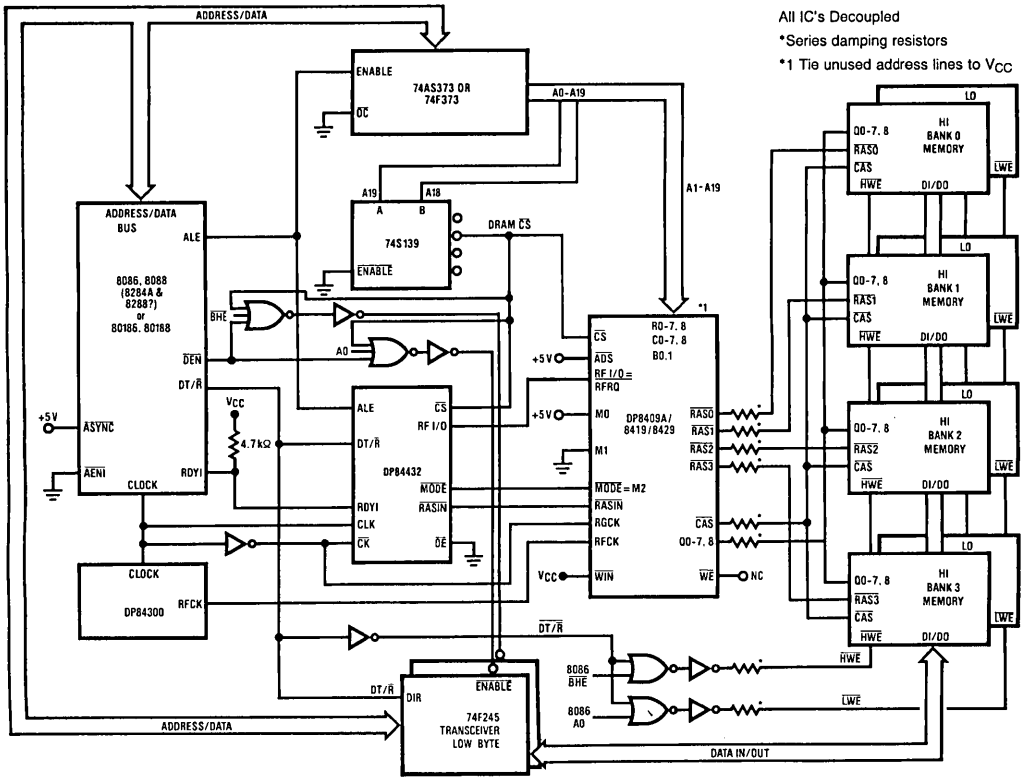
V_{CC} = 5V ± 10%. Commercial: T_A = 0 to 75°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions R1,R2	Commercial			Units
			Min	Typ	Max	
t_{PD}	Input or Feedback to Output	CL = 50 pF		15	25	ns
t_{CLK}	Clock to Output or Feedback			10	15	ns
t_{PZX}	Pin 11 to Output Enable			10	20	ns
t_{PXZ}	Pin 11 to Output Disable	C_L = 5 pF		11	20	ns
t_{PZX}	Input to Output Enable	C_L = 50 pF		10	25	ns
t_{PXZ}	Input to Output Disable	C_L = 5 pF		13	25	ns
f_{MAX}	Maximum Frequency		25	30		ns

V_{CC} = Max. at minimum temperature.

Block Diagram

8086 System Block Diagram



TL/F/8399-2

Mnemonic Description

INPUT SIGNALS

1) "$\overline{\text{CLOCK}}$" Inverted clock from 8284A or 8288. "$\overline{\text{CLOCK}}$" should be delayed from CLOCK (pin 5).

2) "$\overline{\text{CS}}$" From decoder chip (chip select) (active low).

3) "ALE" From 8086 (active high).

4) "RFI/O" $\overline{\text{RFRQ}}$ (refresh request) in mode 5. From 8409A, an active low signal.

5) "CLOCK" The non-inverted clock directly from the 8284A. This signal should be unbuffered to this input so as not to incur any extra delay in the $\overline{\text{RASIN}}$ generation time.

6) "$\overline{\text{DELAYREAD}}$" This input signal allows the user to delay when the $\overline{\text{RASIN}}$ signal becomes valid to the DP8409A during a READ cycle of the 8086. This input should be low when using the DP8409A unless an external delay line is used to guarantee a 30 ns $\overline{\text{CS}}$ to $\overline{\text{RASIN}}$ delay (for DP8409A or 15 ns for DP8419) or if the user can afford to disable the hidden refresh by permanently tying $\overline{\text{CS}}$ low on the DP8409A.

7) "$\overline{\text{WAITWRITE}}$" This signal is used to delay when $\overline{\text{RASIN}}$ becomes valid during an 8086 WRITE cycle and also adds a WAIT state into a $\overline{\text{CS}}$ WRITE access cycle. One may want to delay when $\overline{\text{RASIN}}$ becomes valid during a WRITE cycle when generating a parity bit for each byte. This would allow time to generate parity and be assured that the data and parity bit were both written to memory.

8) "DT/$\overline{\text{R}}$" or "$\overline{\text{S1}}$" Used to differentiate between READ and WRITE cycles, and to allow $\overline{\text{CS}}$ READ cycles to start early. If the system is not a minimum mode 8086 or 8088 system then the status signal "$\overline{\text{S1}}$" should be used instead of "DT/$\overline{\text{R}}$" so that the DP84432 knows immediately whether the CPU is doing a READ or a WRITE access cycle.

Mnemonic Description (Continued)

9) "WAITREAD" Used to insert 1 wait state into the 8086 READ bus cycle. The wait state following bus cycle "T3" allows the use of memory with longer access times (t_{CAC}). An active low signal.

10) "OE" This input enables the outputs of the "D-Flip Flop" outputs of the PAL.

OUTPUTS SIGNALS

1) "MODE" This pin goes to M2 on the DP8409A to change from mode 5 to mode 1 (only used for forced refresh).

2) "2DLY" Delay used internal to the PAL.

3) "3DLY" Delay used internal to the PAL.

4) "4DLY" Delay used internal to the PAL.

5) "RASIN" To the 8409A (creates RAS's).

6) "RDY1" To the 8284A or 8288 to insert wait states into the 8086 bus cycles (active low).

7) "INCYCLE REFRESH" This signal is used in the *Figure 1* PAL to detect that an access cycle was started during a DRAM refresh cycle. This allows the PAL to determine, later in the cycle, whether to restart the "INCYCLE" signal or not. If the CPU is not accessing the DRAM, as determined by "CS" being low, then "INCYCLE" is not restarted.

8) "INCYCLE" This signal goes active from the CPU ALE signal. This signal indicates that the processor is doing an access somewhere in the system. This signal stays low for several T states of the access cycle.

Functional Description

The following description applies to both the DP8409A and the DP8419 dynamic RAM controllers.

A memory cycle starts when chip select (CS) and address latch enable (ALE) are true. RASIN is supplied from the DP84432 to the DP8409A dynamic RAM controller, which then supplies a RAS signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8409A switches the address outputs to the column address. The DP8409A then supplies the required CAS signal to the DRAM. In order to do byte operations it is suggested that the user provide external logic, as shown in the system block diagram, to produce a HIGH WRITE ENABLE or a LOW WRITE ENABLE. To differentiate between a READ and a WRITE, the DT/R (or status signal "S1" in a maximum mode 8086 or 8088 system or in a 80186, 8188 system) signal from the CPU is inverted and also supplied to the external WRITE ENABLE logic.

A refresh cycle is started by one of two conditions. The refresh cycle caused by the first condition is called a hidden refresh. This occurs when refresh clock (RFCK) is high, CS is not true, and RASIN goes true. Here the CPU is accessing something else in the system and the DRAM can be refreshed at that time, thereby being transparent to the CPU. The second type of refresh is called forced refresh. This occurs if no hidden refresh was performed while RFCK was high. When RFCK transitions low a refresh request (RFRQ) is generated. If there is not a DRAM access in progress the DP84432 will force a refresh by putting the DP8409A into mode 1 (automatic forced refresh mode). If the CPU tries to access the DRAM during a forced refresh cycle WAIT states will be inserted into its cycles until the forced refresh is over and the DRAM RAS precharge time has been met. Then the pending DRAM access will be allowed to take place.

The DP84432 also allows forced refreshes to take place during long accesses of other devices. For instance, if EEPROM takes several microseconds to write to, the DRAM will still be refreshed while that access is in progress.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories or allow time to generate parity. This is accomplished by inserting a WAIT state into the processor access cycle. The DP84432 can insert WAIT states into either READ or WRITE cycles, or both. The extra WAIT state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

SYSTEM INTERFACE DESCRIPTION

The 80186 or 80188 will be able to use the DP84432 but it will be necessary to invert "ALE" of the 80186 or 80188 and logically NOR it with the "CLOCK" signal. This fix makes the 80186 or 80188 "ALE" signal appear to be similar to the 8086 or 8088 "ALE" signal. The 8088 will be able to use this PAL, but the 8088 will not need the logic necessary to produce LWE, HWE. The 80286 can not use this PAL because it's WAIT state logic is different. (See DP84532 data sheet).

The DP84432 differentiates between READ and WRITE cycles, allowing the RASIN signal to start earlier during a READ cycle compared to a WRITE cycle.

RASIN during a READ cycle can start during T1 or T2 of a processor cycle depending on whether the DELAYREAD input is set low or high. If DELAYREAD is false the user will need to use an external delay line to guarantee that CS will be valid a minimum of 30 ns before RASIN becomes true. If the user is willing to give up hidden refreshes (CS tied permanently low on DP8409A) he must only guarantee that the addresses are valid at the inputs of the DP8409A by a minimum of 10 ns before RASIN becomes valid.

This section of the data sheet goes through the calculation of the "tRAC" (RAS access time) and "tCAC" (CAS access time) required by the DRAM for the iAPX 86/88/186/188 family CPUs to operate at a particular clock frequency without introducing wait states into the processor access cycles. Both "tRAC" and "tCAC" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "tRAC" and "tCAC" parameters calculated. In order to determine the "tRAC" and "tCAC" needed the DP8419 and fast PALs ("B" type PALs) timing parameters were used. If the user is using the DP8408A/09A or a slower PAL device he should substitute their respective delays into the equations below.

Most all of the calculations contained in this note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from RAS exceeded 200 ns. This is because DRAMs can be found with row access times up to 150 ns that require only 15 ns row address hold times.

Functional Description (Continued)

EXAMPLE DRAM TIMING CALCULATIONS

A) IAPX 86/88 8 MHz, No WAIT states, "/DLYRD" = low

#1) $\overline{RASIN}$ low = 1 system clock period + 15 ns ("B" PAL combinational output delay) = 125 + 15 = 140 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ – $\overline{CAS}$ low) – 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"t_{RAC}" = T1 + T2 + T3 – #1 – #2 – #4 – #5
= 125 + 125 + 125 – 140 – 20 – 7 – 20 = 188 ns

"t_{CAC}" = T1 + T2 + T3 – #1 – #3 – #4 – #5
= 125 + 125 + 125 – 140 – 77 – 7 – 20 = 131 ns

Therefore the DRAM chosen should have a "t_{RAC}" less then or equal to 188 ns and a "t_{CAC}" less then or equal to 131 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately two clock periods = 125 + 125 = 250 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately two clock periods plus 50 ns (minimum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 125 + 50 = 300 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods – 5 ns (t_{RPDL}-t_{RPDH} for the DP8409-2) = 125 + 125 – 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods – 70 ns (maximum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 125 – 70 = 180 ns.

The above times are assuming the use of the DP8409-2 and a fast ("A" part) PAL. The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

B) 80186, 8 MHz, "$\overline{DLYRD}$" = HIGH, No Hidden Refresh ($\overline{CS}$ = Low), No Wait States

Minimum $\overline{RASIN}$ = 55 ns (min clk low) + 1 ns (min PAL delay) = 68 ns

Maximum Address Valid = 44 ns (ADD valid max) + 8 ns (74F373) = 52 ns

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 70 + 15 = 85 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 97 ns (DP8419 $\overline{RASIN}$ – $\overline{CAS}$ low) – 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 Transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"t_{RAC}" = T1 + T2 + T3 – #1 – #2 – #4 – #5
= 125 + 125 + 125 – 85 – 20 – 7 – 20 = 243 ns

"t_{CAC}" = T1 + T2 + T3 – #1 – #3 – #4 – #5
= 125 + 125 + 125 – 85 – 94 – 7 – 20 = 169 ns

Therefore the DRAM chosen should have a "t_{RAC}" less then or equal to 243 ns and a "t_{CAC}" less then or equal to 169 ns. Standard 200 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one clock period + 55 ns (minimum clock low) – 15 ns (maximum DP84432 clocked output delay for ending $\overline{RASIN}$) = 125 + 55 – 15 = 165 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one clock period + 55 ns (minimum clock low) – 15 ns (maximum clocked output delay for ending $\overline{RASIN}$) + 35 ns (minimum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 55 – 15 + 35 = 200 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods – 5 ns (t_{RPDL}-t_{RPDH} for the DP8409-2) = 125 + 125 – 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods – 70 ns (maximum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 125 – 70 = 180 ns.

C) 8086, 8 MHz, $\overline{CS}$ Tied Low (no hidden refresh), $\overline{DLYRD}$ = HIGH, No Delay Line Needed, No Wait States

Minimum $\overline{RASIN}$ = 69 ns (min clk low) + 13 ns (min PAL delay) = 82 ns

Maximum Address Valid = 60 ns (ADD valid max) + 8 ns (74F373) = 68 ns

The address must be valid a minimum of 10 ns before $\overline{RASIN}$ goes valid at the inputs of the DP8409A or DP8419, which it will be given the ICs used in this example.

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 82 + 15 = 97 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 97 ns (DP8419 $\overline{RASIN}$ – $\overline{CAS}$ low) – 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 Transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"t_{RAC}" = T1 + T2 + T3 – #1 – #2 – #4 – #5
= 125 + 125 + 125 – 97 – 20 – 7 – 20 = 231 ns

"t_{CAC}" = T1 + T2 + T3 – #1 – #3 – #4 – #5
= 125 + 125 + 125 – 97 – 94 – 7 – 20 = 157 ns

Therefore the DRAM chosen should have a "t_{RAC}" less then or equal to 231 ns and a "t_{CAC}" less then or equal to 157 ns. Standard 200 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) + 15 ns (maximum DP84432 clocked output delay for ending $\overline{RASIN}$) = 125 + 69 – 15 = 179 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) – 15 ns (maximum clocked output delay for ending $\overline{RASIN}$) + 35 ns (minimum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 69 – 15 + 35 = 214 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods – 5 ns (t_{RPDL}-t_{RPDH} for the DP8409-2) = 125 + 125 – 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods – 70 ns (maximum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 125 – 70 = 180 ns.

3

Functional Description (Continued)

D) 8086, 10 MHz, $\overline{CS}$ Tied Low (no hidden refresh), $\overline{DLYRD}$ = HIGH, No Delay Line Needed, No Wait States

MINIMUM $\overline{RASIN}$ = 52 ns (min clk low) + 13 ns (min PAL delay) = 65 ns

MAXIMUM ADDRESS VALID = 50 ns (ADD valid max) + 8 ns (74F373) = 58 ns

The address must be valid a minimum of 10 ns before $\overline{RASIN}$ goes valid at the inputs of the DP8409A or DP8419. As an example use two 74ALS04 inverters to guarantee a minimum delay of 4 ns, therefore MINIMUM $\overline{RASIN}$ = 69 ns

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 61 + 15 = 76 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F245 Transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 5 ns minimum

"t_{RAC}" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 100 + 100 + 100 − 76 − 20 − 7 − 5 = 192 ns

"t_{CAC}" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 100 + 100 + 100 − 76 − 77 − 7 − 5 = 135 ns

Therefore the DRAM chosen should have a "t_{RAC}" less then or equal to 192 ns and a "t_{CAC}" less then or equal to 135 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) − 15 ns (maximum DP84432 clocked output delay for ending $\overline{RASIN}$) = 125 + 69 − 15 = 179 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) − 15 ns (maximum clocked output delay for ending $\overline{RASIN}$) + 35 ns (minimum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 69 − 15 + 35 = 214 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns (t_{RPDL}-t_{RPDH} for the DP8409-2) = 125 + 125 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum t_{RICL}-t_{RICH} for the DP8409-2) = 125 + 125 − 70 = 180 ns.

SUGGESTIONS

It is suggested that the DP8409A is to be used up to 8 MHz. Above 8 MHz one should use the DP8409-2 or the DP8419. Also fast PALs ("A" parts) should be used at 8 MHz and above. If very fast PALs are used ("B" parts) the access will be 10 ns faster than calculated in the above sections.

These suggestions occur because of DRAM parameters that must be met, such as:

1) $\overline{CAS}$ ACCESS TIME—time from $\overline{CAS}$ valid until data is available at the DRAM outputs.

2) $\overline{RAS}$ PRECHARGE TIME—minimum amount of time from $\overline{RAS}$ high until $\overline{RAS}$ transitions low again.

3) $\overline{CAS}$ PRECHARGE TIME—minimum amount of time from $\overline{CAS}$ high until $\overline{CAS}$ transitions low again.

4) $\overline{RAS}$ PULSE WIDTH—minimum $\overline{RAS}$ valid time during an access, this usually occurs during a WRITE operation since $\overline{RASIN}$ is generated later then in a READ operation.

5) $\overline{CAS}$ PULSE WIDTH—minimum $\overline{CAS}$ valid time during an access.

6) DATA IN SETUP TIME—the data, during a DRAM WRITE access cycle, must be valid at the DRAM inputs when WRITE ENABLE or $\overline{CAS}$ transitions low, whichever occurs last.

For instance, during a WRITE operation, one does not want $\overline{CAS}$ to go valid until the data to be written is setup at the inputs to the dynamic RAM. Therefore an 8086 running at 5 MHz should use a DP8409A and a slower DP84432 PAL.

EXAMPLE: 8086, 5 MHz, DP8409A, DP84432 (fast PAL "A" part)

MINIMUM $\overline{RASIN}$ = 3 ns (min clk inversion) + 7 ns (min fast PAL clocked output) + 13 ns (min combinational fast PAL output) = 23 ns into the T2 CPU cycle.

MINIMUM $\overline{CAS}$ = MINIMUM $\overline{RASIN}$ + MINIMUM $\overline{RASIN}$ TO $\overline{CAS}$ TIME = 23 + 95 = 118 ns

MINIMUM DATA VALID during an 8086 WRITE at 5 MHz = 110 ns

MINIMUM DATA VALID at DRAM input = MINIMUM DATA VALID + MINIMUM TRANSCEIVER DELAY (74F245) = 110 + 7 = 117 ns

Therefore, worst case, the data could be valid 1 ns before $\overline{CAS}$ becomes valid at the DRAM inputs. Most DRAMs specify 0 ns setup time so this is OK, but if the DP8409A is driving less then the full load specified in the data sheet $\overline{CAS}$ could become valid before the data was available at the DRAM inputs. Therefore the user may want to use a slower PAL or adjust the PAL equations to start the WRITE later in the access cycle. For example, the second equation in the $\overline{RASIN}$ term could be adjusted as follows to accomplish a later $\overline{RASIN}$ during WRITE cycles:

change "$\overline{CS}$*$\overline{INCY}$*$\overline{MODE}$*2D*$\overline{WAITWR}$" to
"$\overline{CS}$*$\overline{INCY}$*$\overline{MODE}$*2D*$\overline{WAITWR}$*$\overline{CLK}$"

At higher frequencies one generally wants to generate WRITE as the DP84432 does in order to guarantee that the $\overline{CAS}$ pulse width is great enough.

INTERPRETING THE DP84432 PAL EQUATIONS

The boolean equations for the DP84432 were written using the standard PALASM™ format. In other words the equation:

"IF (VCC) RASIN = INCY*$\overline{MODE}$*4D*$\overline{DT}$" will mean;

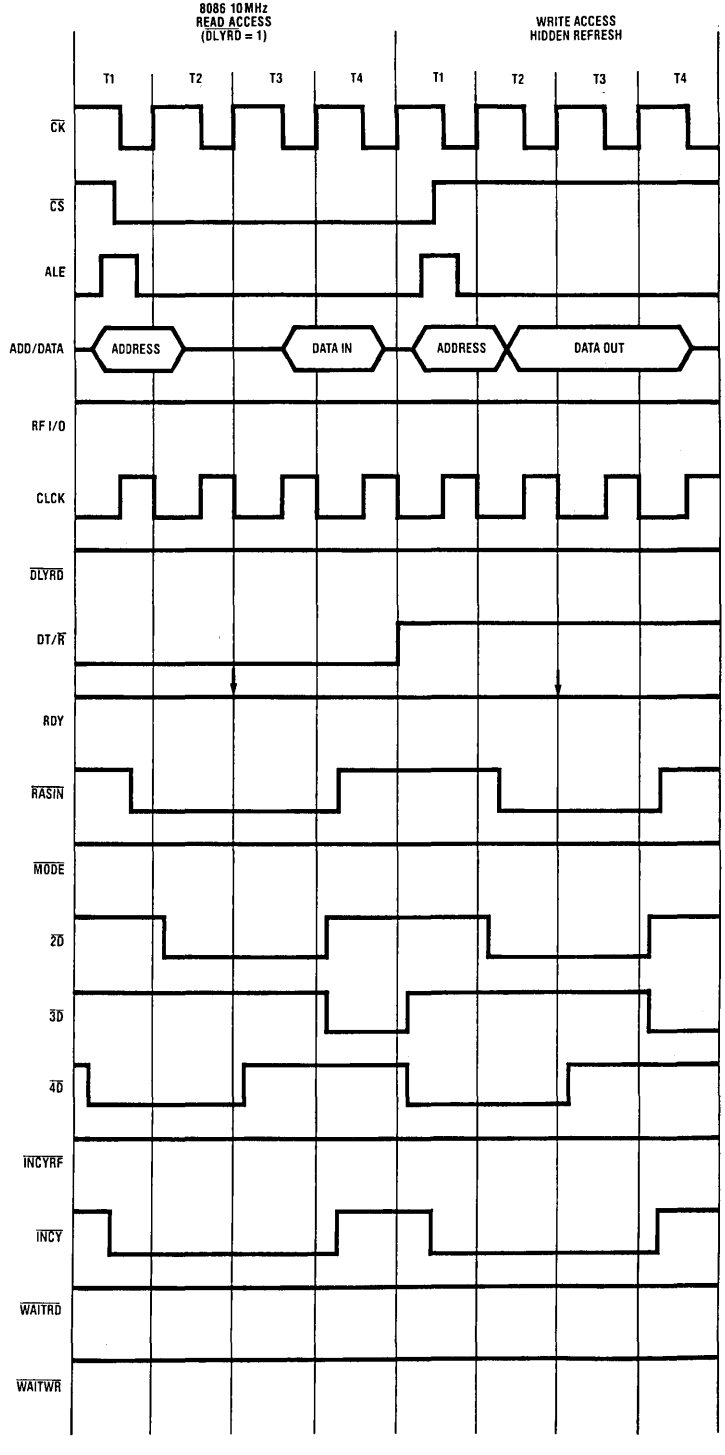
The output "$\overline{RASIN}$" (see pin list for DP84432) will be active low (inverted RASIN) when the output "$\overline{INCY}$" is low (making INCY high) AND the output "$\overline{MODE}$" is high AND the output "$\overline{4D}$" is low (making 4D high) AND the input DT/R is low (making $\overline{DT/R}$ high).

PAL Boolean Equations

```
    PAL16R4A     ;FAST PAL
    NEW PAL FOR INTEL PROCESSORS 8086, 8088, 80186, 80188
    NATIONAL SEMICONDUCTOR (WORKS UP TO 10 MHz)

    /CK /CS RF10 ALE CLK /DLYRD /WAITWR DT /WAITRD GND /OE
    /INCY /INCYRF /4D /3D /2D /MODE /RASIN RDY VCC

IF (VCC) RASIN =
  INCY*/MODE*4D*/DT*/DLYRD*CLK+              ;Start RASIN, early READ
  CS*INCY*/MODE*2D*/WAITWR+                  ;Start RASIN, early WRITE
  CS*INCY*/INCYRF*/ALE*/MODE*/3D*/DT*/CLK+   ;Start READ
  CS*INCY*/MODE*2D*DT*WAITWR*CLK+            ;Late WRITE
  /CS*INCY*/MODE*2D+                         ;Hidden RFSH
  RASIN*INCY*/ALE*/MODE*/3D*4D+              ;Continue RASIN
  RASIN*/MODE*2D                             ;Continue RASIN

IF (VCC) INCYRF = ALE*MODE+                  ;Start INCYCLE in REFRESH
                  INCYRF*MODE+               ;Continue INCY in REFRESH
                  INCYRF*4D*/CLK             ;Continue INCY in REFRESH

MODE := /RF10*/INCY*/2D+                ;Forced RFSH at beginning
                                        ; of a cycle, during IDLE
        MODE*/3D+                       ; states, or during long
        MODE*/4D                        ; accesses of other devices

2D := MODE*/4D+
  INCY*/MODE*4D+
  CS*/DT*WAITRD*INCY*/MODE*2D*/3D*/4D+      ;Extend for "CS READ" cycle
  CS*DT*WAITWR*INCY*/MODE*2D*/3D*/4D        ;Extend for "CS WRITE" cycle

3D := 2D*/4D

4D := 3D+
      /INCY*/MODE+
      INCY*/MODE*/2D

IF (VCC) INCY = ALE*/MODE+          ;Start INCY for access
         INCY*/INCYRF*/MODE*/3D*4D+ ;Continue INCY during access
         INCY*/MODE*2D+             ;End INCY during access
         CS*INCYRF*/MODE*/2D*/3D*4D+ ;Start INCY after REFRESH
         CS*INCY*/MODE*/3D*4D*/RDY  ;Continue INCY after REFRESH

IF (CS) /RDY = CS*INCYRF*/2D*/3D*4D+        ;Access at end of RFSH cycle
        CS*/RDY*/MODE*/2D*/3D*4D+           ;Continue RDY after RFSH
        CS*MODE+                            ;Continue RDY after RFSH
        CS*/DT*WAITRD*INCY*/MODE*2D*/3D*4D+  ;WAIT for "CS READ"
        CS*DT*WAITWR*INCY*/MODE*2D*/3D*4D    ;WAIT for "CS WRITE"
```

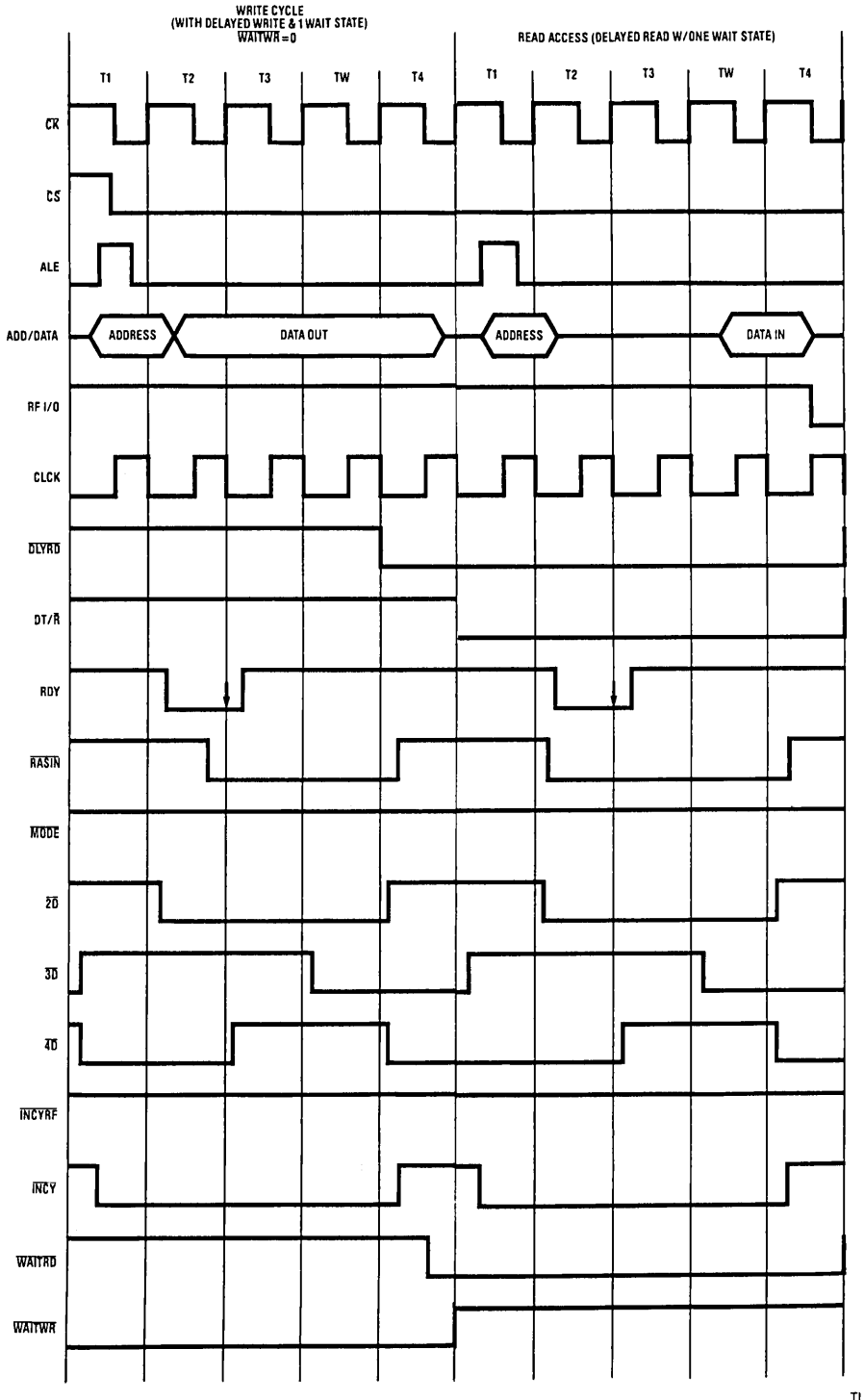
FIGURE 1. Equations for the DP84432 Standard Interface PAL (Works in Minimum or Maximum Mode)

System Timing Diagrams



TL/F/8399–3

System Timing Diagrams (Continued)



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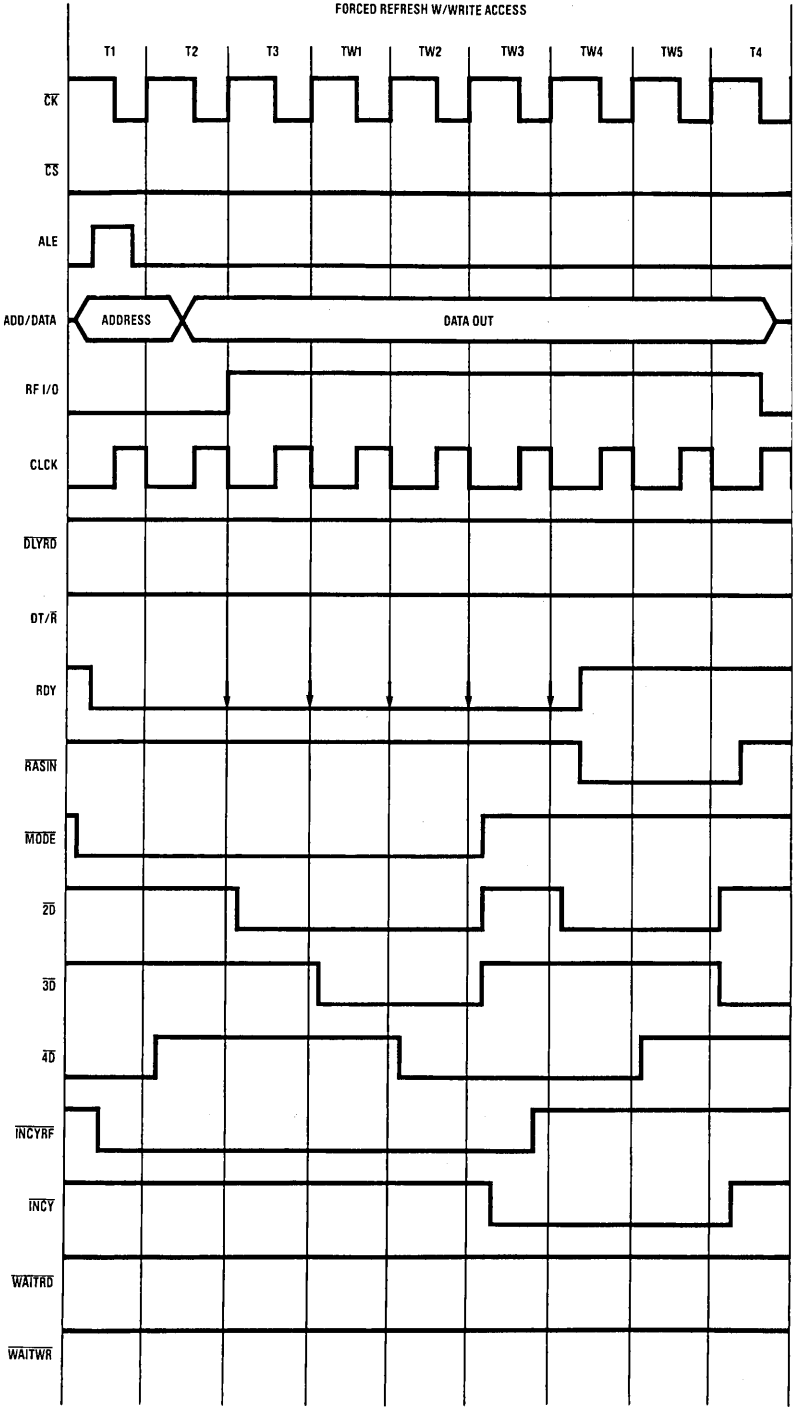
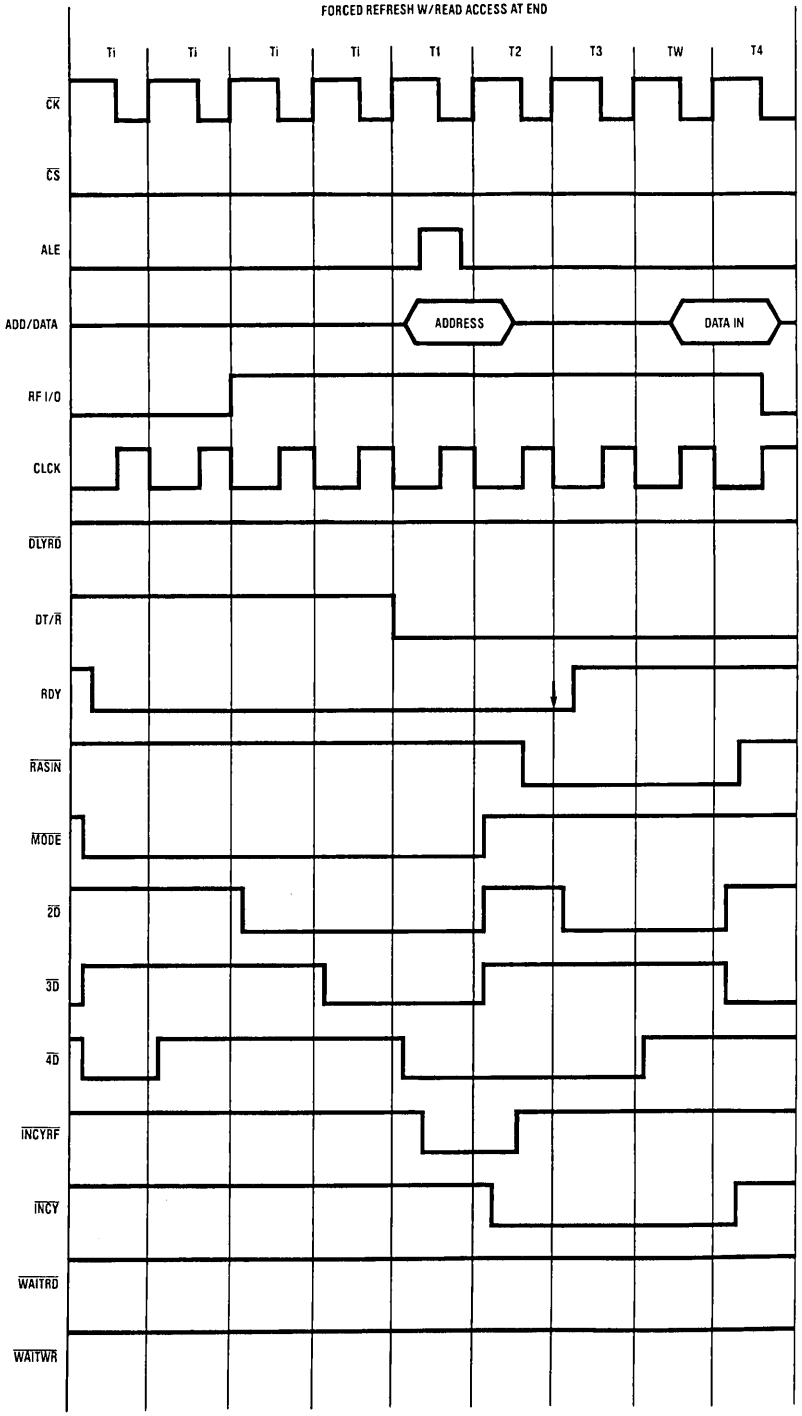
System Timing Diagrams (Continued)



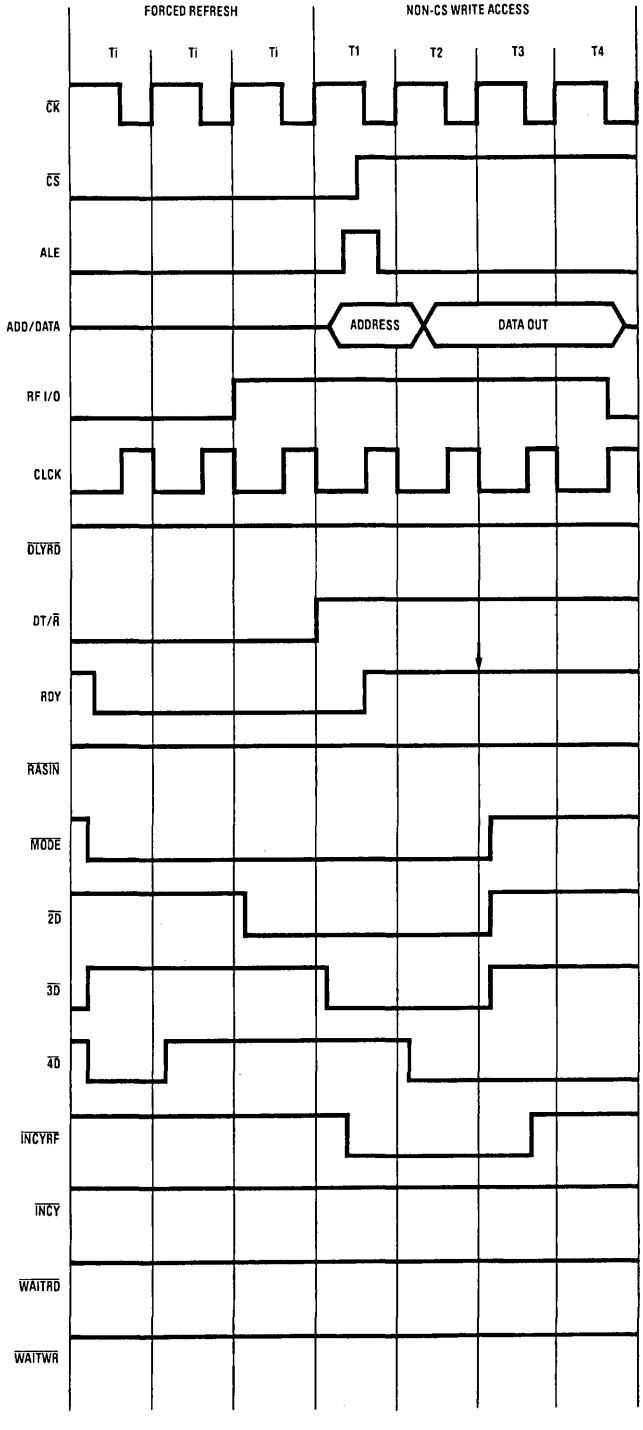
TL/F/8399–6

System Timing Diagrams (Continued)



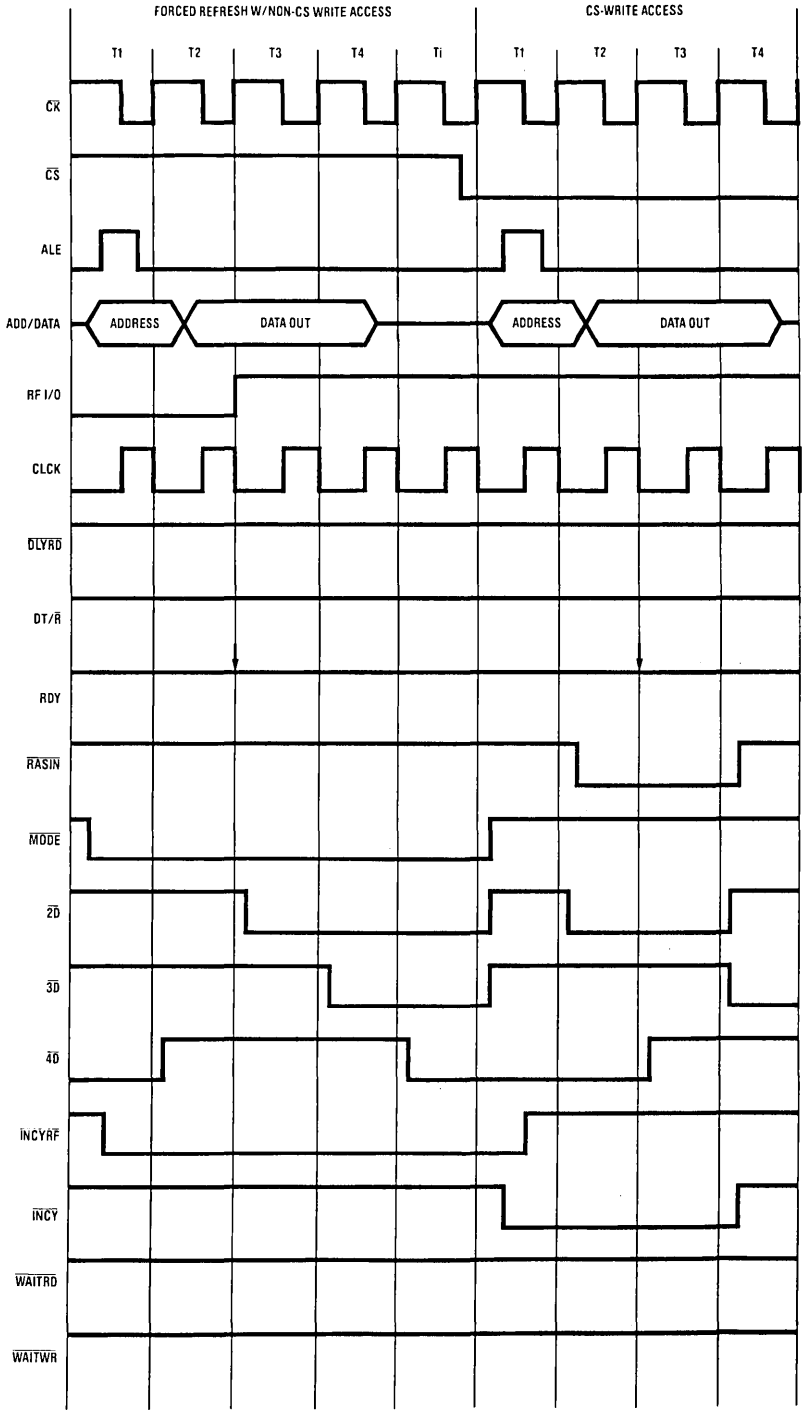
TL/F/8399–7

System Timing Diagrams (Continued)



TL/F/8399–8

System Timing Diagrams (Continued)



TL/F/8399–9

National Semiconductor Corporation

PRELIMINARY

DP84512 Dynamic RAM Controller Interface Circuit for the NS32332

General Description

This is a PAL (Programmable Array Logic) device designed to allow an easy interface between the National Semiconductor NS32332 microprocessor and the National Semiconductor DP8417/18/19/28/29 dynamic RAM controller.

This PAL supplies all the control signals needed to perform memory read, burst read, write, and refresh operations up to a frequency of 15 MHz.

Features

- Provides a 3-chip solution for the NS32332/DP8418 (or DP8428) dynamic RAM interface (1 PAL, DP8418 and clock divider)
- Works with all speed versions of the NS32332 up to 15 MHz
- Allows operation of NS32332 at 12 MHz with no WAIT states with standard 120 ns 256k or 1M DRAMs
- Controls DP8417/18/19/28/29 mode 5 accesses and mode 0 forced refreshes automatically
- Allows READ accesses in burst mode
- CPU WAIT states are automatically inserted during contention between DRAM accesses and DRAM refreshes
- Uses standard National Semiconductor PALs (i.e., DMPAL16R4A, the user may want to use faster versions of these PALs at higher CPU operating frequencies)
- The PAL programming equations are provided with comments for easy user modification to his specific requirements

National Semiconductor Corporation

PRELIMINARY

DP84522 Dynamic RAM Controller Interface Circuit for the 68020 CPU

General Description

This is a Programmable Array Logic (PAL®) device designed to allow an easy interface between the 68020 microprocessor and the National Semiconductor DP8417, DP8418, DP8419, DP8428 or DP8429 dynamic memory controllers.

This PAL supplies all the control signals needed to perform memory read, write, and refresh operations up to a frequency of 16.7 MHz.

Features

- Provides a 3 or 4 chip solution for the 68020/DP8418 (or DP8428) dynamic RAM interface (1 or 2 PALs, DP8418, and clock divider)
- Works with all speed versions of the 68020 up to 16.7 MHz
- Allows operation of 68020 at 12.5 MHz with 1 WAIT state with standard 120 ns 256k DRAMs
- Controls DP8418/28 mode 5 accesses and mode 1 or 0 forced refreshes automatically
- Allows memory interleaving if desired
- CPU WAIT states are automatically inserted during contention between memory interleaving/DRAM accesses/DRAM refreshes
- Uses standard National Semiconductor PALs (i.e., DMPAL16R4A; the user may want to use faster versions of these PALs at higher CPU operating frequencies)
- The PAL programming equations are provided with comments for easy user modification to his specific requirements

Functional Description

The following description applies only to the DP8418 or DP8428 since "RFI/O" going low initiates a mode 0 externally controlled forced refresh. This forced refresh resets the internal refresh request logic on the DP8418 or DP8428, but will not reset the internal logic on the DP8409A.

A memory cycle starts when chip select ($\overline{CS}$) and the address strobe ($\overline{AS}$) become true. $\overline{RASIN}$ is supplied from the PALs to the DP8418 DRAM controller, which then supplies $\overline{RAS}$ to the selected $\overline{RAS}$ bank. After the necessary row address hold time, the DP8418 switches the address outputs to the column address. The DP8418 then supplies the required $\overline{CAS}$ signal to the DRAM.

The first PAL (PAL #1) supports byte operations by producing four WRITE enables, one for each possible byte of the 32 bit word (upper, upper middle, lower middle, and lower write enable). These WRITE enables are produced externally from the 68020 "DATA STROBE" and "READ/WRITE" outputs. Since it is possible that all WRITE cycles may be LATE WRITE cycles ("WRITE ENABLE" occurring after "COLUMN ADDRESS STROBE") memory buffers should be used instead of transceivers to separate the data in from the data out of the DRAMs.

The second PAL (PAL #2) supports byte operations by producing four COLUMN ADDRESS STROBES, one for each of the possible bytes of the 32-bit word. This PAL terminates the DP8418 "$\overline{RASIN}$" input early but holds the DRAM data valid by latching the byte "$\overline{CAS}$'s" externally. This method of supporting byte writes allows transceivers to be used, or to directly connect the DRAM data in and data out pins to the 68020 data bus I/O pins.

Hidden REFRESH cycles are not allowed in this set of PALs because of the need for adequate $\overline{RAS}$ precharge times in all circumstances and the desire not to be inserting WAIT states into access cycles of other system elements.

These PALs perform externally controlled forced refreshes automatically (mode 0). A refresh cycle occurs when the DP8418 input RFCK transitions low and the RFIO signal goes low requesting a refresh cycle. The PAL responds by pulling RFSH low (M2 and M0) if there are no current DRAM accesses in progress. If a DRAM access is in progress the PAL waits until the current access is completed before performing the forced refresh cycle. If an access is requested during the forced refresh cycle WAIT states are automatically inserted into the access cycle until the refresh cycle is completed and adequate $\overline{RAS}$ precharge has been completed. The pending DRAM access cycle is then performed. The input signal "$\overline{NOWAIT}$" allows one to vary the amount of time required to do a refresh (see the description of the "$\overline{NOWAIT}$" input in the pin description section). In one of the timing diagrams the "$\overline{RFSH}$" output was tied to the "$\overline{NOWAIT}$" input to decrease the length of the refresh cycle but still insert one wait state in normal DRAM access cycles (see *Figure 5*).

The first PAL (PAL #1) supports memory interleaving to guarantee adequate $\overline{RAS}$ precharge time during two consecutive accesses to the same DRAM bank. This is performed by looking at the lower address bit or bits, A2 and/or A3. If the processor is sequentially accessing the DRAM each $\overline{RAS}$ output will have plenty of precharge time. But if the system tries to access the same bank twice in a row the access will be delayed until adequate $\overline{RAS}$ precharge time has been met. During this time WAIT states will automatically be inserted into the pending access cycle.

The second PAL (PAL #2) guarantees adequate $\overline{RAS}$ precharge time (one and one half system clock periods) by ending the DP8418 "$\overline{RASIN}$" input early. The DRAM data is held valid by externally latching the DRAM "$\overline{CAS}$" input as explained earlier. This has the additional benefit of sim-

Functional Description (Continued)

plifying the memory interface of the 68020 by eliminating the external components needed for interleaving, though as one approaches 16.7 MHz the interleaving circuitry may again become necessary to guarantee adequate "$\overline{\text{RAS}}$" precharge time.

For PAL #1 an external "D type" flip-flop or another PAL could be used for the support of memory interleaving. If one is not using memory interleaving (10 MHz or below) the "PREVO" input can be used for some other function and the equations of "$\overline{\text{RASIN}}$" that employ "PREVO" can be adjusted.

The PAL equations for this interface are written in the National Semiconductor PLAN™ format, which differs from the standard PALASM™ format.

EXAMPLE: PLAN FORMAT

```
/RASIN := RFSH*/2D*/AS
```

This translates as, "$\overline{\text{RASIN}}$" is low after the rising edge of the input clock given that "$\overline{\text{RFSH}}$" was high and "$\overline{\text{2D}}$" was low and "$\overline{\text{AS}}$" was low a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{2D}}$, and $\overline{\text{RFSH}}$ are outputs of the PAL and $\overline{\text{AS}}$ is an input).

EXAMPLE: PALASM FORMAT

```
/RASIN := /RFSH*2D*AS
```

The above expression means the same as the PLAN format expression except it is written in PALASM format. In other words; "$\overline{\text{RASIN}}$" will go low after the rising edge of the clock given that "$\overline{\text{RFSH}}$" was high, "$\overline{\text{2D}}$" was low, and "$\overline{\text{AS}}$" was low a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{2D}}$, and $\overline{\text{RFSH}}$ are outputs of the PAL and $\overline{\text{AS}}$ is an input).

Depending on the specific type of PALs and logic used the user can calculate the speed requirements for the DRAM at the specified processor frequency as follows:

CALCULATION OF DRAM "t_{RAC}" $\overline{\text{RAS}}$ ACCESS TIME AND "t_{CAC}" $\overline{\text{CAS}}$ ACCESS TIME REQUIRED FOR A 12.5 MHz 68020, 1 WAIT STATE, MICROPROCESSOR SYSTEM

#1) $\overline{\text{RASIN}}$ generation time = "S0" + "S1" + 1 combinational output delay of the PAL generating the "$\overline{\text{RASIN}}$" output (assume DMPAL16R4B) = 80 ns + 15 ns = 95 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ out delay of the DP8418 = 20 ns maximum (used to determine "t_{RAC}")

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ out delay of the DP8418 DRAM contoller driving a load of 2 banks of 256k DRAMs, each bank containing 36 (32 DRAMs plus byte parity) = 72 DRAMs

Since this is under the specified load in the data sheet (approximately 88 DRAMs) approximately 3 ns can be subtracted from the data sheet number, giving 80 ns − 3 ns = 77 ns maximum (used to determine "t_{CAC}")

#4) 74AS244 buffer delay = 7 ns maximum

#5) Data setup time required from the falling edge of "S4" clock = 10 ns maximum

A normal 12.5 MHz 68020 access cycle (with 1 WAIT state inserted) contains 4 clock periods of 80 ns per period.

The required DRAM "t_{RAC}" (row access time) can be calculated from

S0 + S1 + S2 + S3 + SW1 + SW2 + S4
(minimum 1/2 period) − #1 − #2 − #4 − #5
= 40 + 40 + 40 + 40 + 40 + 40 + 35
− 95 − 20 − 7 − 10 = 143 ns

The required DRAM "t_{CAC}" (column access time) can be calculated from

S0 + S1 + S2 + S3 + SW1 + SW2 + S4
(minimum 1/2 period) − #1 − #3 − #4 − #5
= 40 + 40 + 40 + 40 + 40 + 40 + 35
− 95 − 77 − 7 − 10 = 86 ns

The DRAMs selected for this system must satisfy both the "t_{RAC} and t_{CAC}" requirements. Therefore the DRAMs must have a "t_{RAC}" (row access time) less then or equal to 143 ns and a "t_{CAC}" (column access time) less than or equal to 86 ns to be used in this system, under worst case conditions, for a 1 WAIT state 12.5 MHz 68020 system. Common 120 ns 64k or 256k DRAMs meet this specification. If one is using PAL #2, producing external "CAS's" and not using any external transceivers he could possibly use 150 ns DRAMs in the above example.

If one is using PAL #2, the calculated "t_{RAC}" and "t_{CAC}" may differ from the actual system values, depending upon the external circuitry used to produce the byte "$\overline{\text{CAS}}$'s". The DP8418 "$\overline{\text{RASIN}}$–$\overline{\text{CAS}}$" low will be approximately 10–15 ns less than the value given in the data sheet because of the small loading on the DP8418 "$\overline{\text{CAS}}$" output. The external circuitry needed to produce the byte "$\overline{\text{CAS}}$'s" should be loaded such that the column address (from DP8418) is valid when "$\overline{\text{CAS}}$" goes low. For this reason "$\overline{\text{RASIN}}$-byte $\overline{\text{CAS}}$" may be longer than the value used in the "t_{RAC}, t_{CAC}" calculations, and therefore may give a smaller "t_{RAC}, t_{CAC}" than was calculated.

68020 PAL Inputs and Outputs

(Pin number of the PAL on the left)

PAL #1 Inputs

1) "CK"	This is the system clock.
2) "$\overline{\text{AS}}$"	Address strobe from 68020.
3) "$\overline{\text{RFRQ}}$"	This is the refresh request from the DP8418.
4) "$\overline{\text{CS}}$"	This is the chip select (see system block diagram).
5) "R"	READ/$\overline{\text{WRITE}}$ output pin from the 68020.
6) "CLK"	The system clock.
7) "PREVO"	This output holds the previously accessed DRAM "$\overline{\text{RAS}}$" bank.
8) "B0"	This input is the address bit "A2" and is used to determine which "$\overline{\text{RAS}}$" bank the system is accessing.
9) "$\overline{\text{NOWAIT}}$"	This PAL always inserts one WAIT state into every 68020 access cycle. This input,

68020 PAL Inputs and Outputs (Continued)

if low, allows the DRAM to be accessed with no wait states inserted into the access cycle. This input also, if low during a refresh, shortens the length of the refresh cycle by one clock period. This causes the $\overline{RAS}$ pulse width (during a refresh) and the $\overline{RAS}$ precharge time (after a refresh) to be shorter.

11) "$\overline{OE}$" This input enables the PAL outputs.

PAL #1 Outputs

19) "$\overline{XDLY}$" This signal is used to guarantee one period of "$\overline{RFSH}$" high to "$\overline{RASIN}$" low time and to guarantee two periods of RAS precharge time in consecutive accesses to the same DRAM bank.

18) "$\overline{RASIN}$" This signal causes $\overline{RAS}$ (or $\overline{RAS}$s) to go low during a DRAM access or refresh.

17) "$\overline{RFSH}$" This signal initiates a DRAM Refresh.

16) "$\overline{1DLY}$" A delay that is used internally.

15) "$\overline{2DLY}$" A delay that is used internally.

14) "$\overline{RFREQ}$" Refresh request (from the DP8418) synchronized to the system clock.

13) "$\overline{RFREQCK}$" This input synchronizes "$\overline{RFREQ}$" to the falling edge of the input system clock "CLK" and is used in arbitrating between refreshes and accesses (see "$\overline{RASIN}$" equations).

12) "$\overline{DSACK}$" This output goes to the 68020 "$\overline{DSACK0}$, $\overline{1}$" data acknowledge input. This output allows WAIT states to be inserted into DRAM access cycles during access/refresh/RAS precharge contention.

Interface PAL #1 Boolean Equations

This PAL will work up to 16.7 MHz with the 68020. This PAL uses mode 0 (M0 = M1 = M2 = low) for doing externally controlled forced refreshes, guaranteeing more than 2.5 periods of RGCK RAS pulse width ("NOWAIT" = high). If "NOWAIT" is low the refresh is shortened by one clock period. This PAL will only work with the DP8417/18/19/28/29 since it uses mode 0 to reset the RFSH request (RFIO) signal.

```
DMPAL16R4A
CK   AS   RFRQ   CS   R   CLK   PREVO   BO   /NOWAIT   GND
/OE  /DSACK  /RFREQCK  /RFREQ  /2DLY  /1DLY  /RFSH  /RASIN  /XDLY  VCC

IF (VCC) /XDLY = RFSH*/2DLY*RASIN*PREVO*BO      ;Same bank interleave
     +RFSH*/2DLY*RASIN*/PREVO*/BO               ;Same bank interleave
     +/RFSH*1DLY*/2DLY*/RASIN*NOWAIT*/CLK       ;"/XDLY" low during RFSH
     +/RFSH*1DLY*2DLY*RASIN*RFREQ*/NOWAIT       ;"/XDLY" low during RFSH
     +/XDLY*/RFSH*RFREQ                         ;Hold "/XDLY" low
     +/XDLY*RASIN*/AS*CLK                       ;Hold "/XDLY" low

IF (VCC) /RASIN = /RFSH*RFREQ*/1DLY            ;RFSH "/RASIN"
  +/RASIN*/RFSH*/2DLY*XDLY                     ;Hold "/RASIN" low
  +RFSH*RFREQCK*/AS*/CS*PREVO*/BO*CLK          ;Start "/RASIN"
  +RFSH*RFREQCK*/AS*/CS*/PREVO*BO*CLK          ;Start "/RASIN"
  +RFSH*RFREQCK*/AS*/CS*2DLY*XDLY*CLK          ;After idle states
  +/RASIN*RFSH*/AS*/CS                         ;Hold "/RASIN" low
  +/RASIN*/CLK                                 ;Hold "/RASIN" low

IF (VCC) /RFREQCK = /RFREQ*/CLK                ;Start from falling clock
     +/RFREQCK*/RFREQ                          ;  edge

IF (VCC) /DSACK = /CS*RFSH*/RASIN*NOWAIT*/CLK  ;One WAIT state
  +/DSACK*/CS*RFSH*/RASIN*/AS                  ;Hold "/DSACK" low
  +/CS*RFSH*/AS*/NOWAIT*XDLY                   ;No WAIT state in access

/RFSH := /RFREQ*RASIN*/1DLY*/2DLY              ;Start RFSH
     +/RFREQ*RASIN*1DLY                        ;Start RFSH
     +/RFSH*/RFREQ                             ;Hold RFSH low
     +/RFSH*/RASIN                             ;Hold RFSH low
     +/RFSH*/1DLY                              ;Hold RFSH low

/1DLY := /RFSH*2DLY*/RFREQ                     ;Start "/1DLY" during RFSH
     +/RFSH*/1DLY*2DLY*XDLY                    ;Continue "/1DLY" during RFSH
     +RFSH*/RASIN                              ;Start "/1DLY" during /RASIN

/2DLY := /RFSH*/1DLY                           ;Start "/2DLY" during RFSH
     +/RFSH*2DLY*/RFREQ*/NOWAIT                ;Shorten RFSH
     +RFSH*/RASIN*/1DLY                        ;Start "/2DLY" during /RASIN
     +RFSH*/RASIN*/NOWAIT                      ;Shorten access

/RFREQ := /RFRQ                                ;Synchronize to system clock
```

Interface PAL #1 Between 68020 and DP8418/28 (Continued)

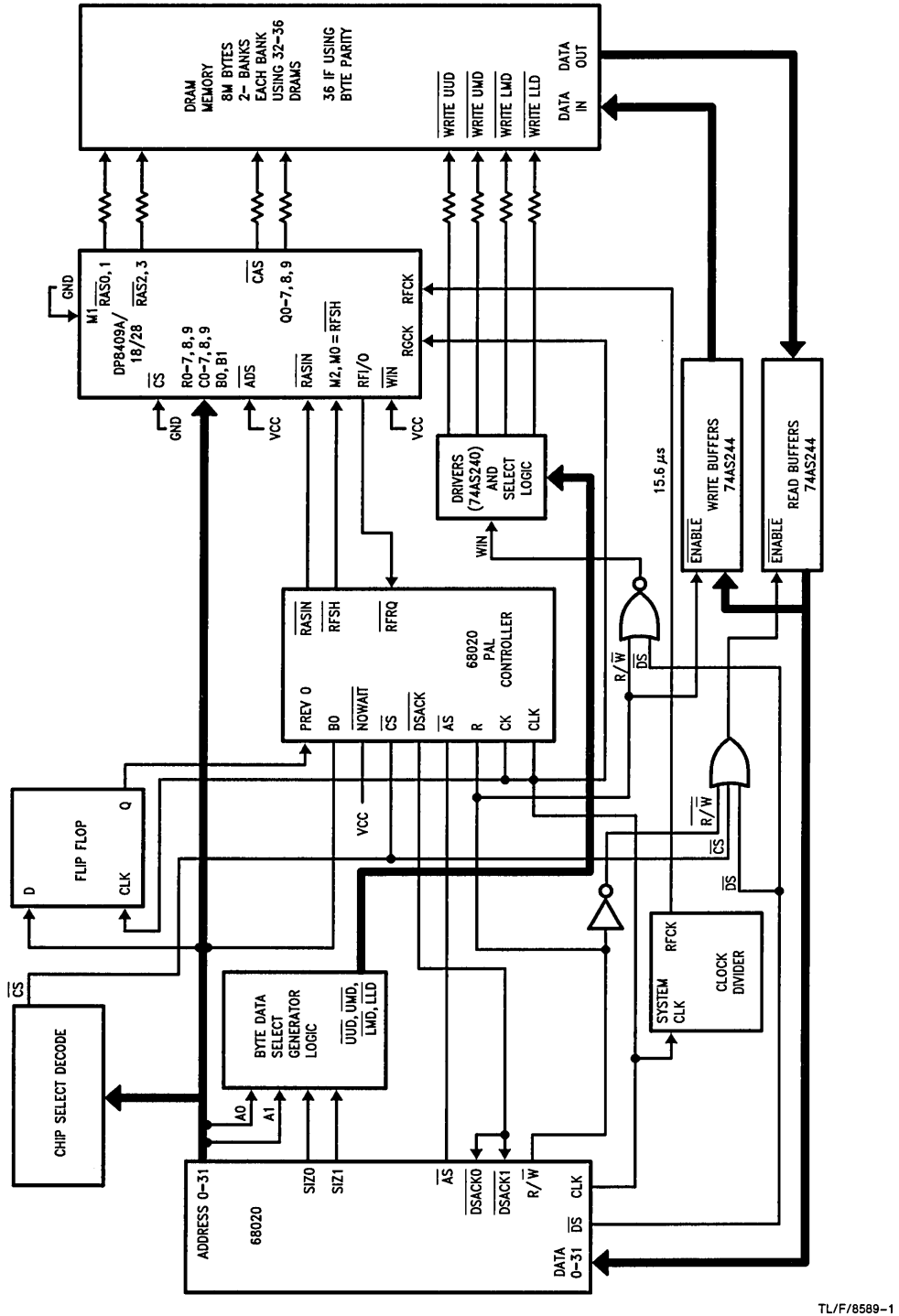


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FIGURE 1. 68020 System Diagram for PAL #1

Interface PAL # 1 Between 68020 and DP8418/28 (Continued)

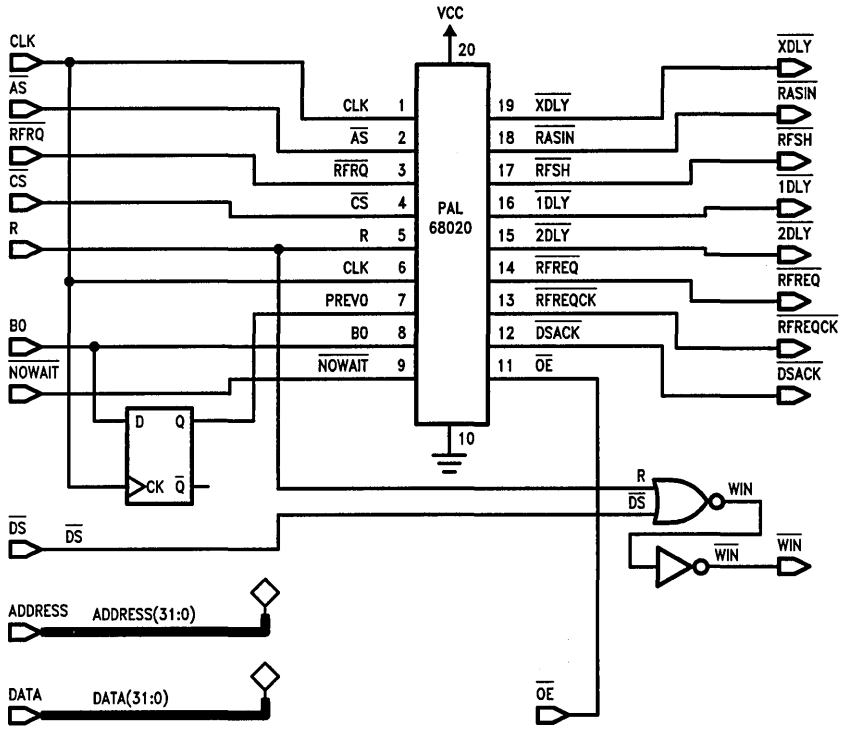

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FIGURE 2. PAL # 1 Simulation Diagram

Interface PAL # 1 System Timing Diagram

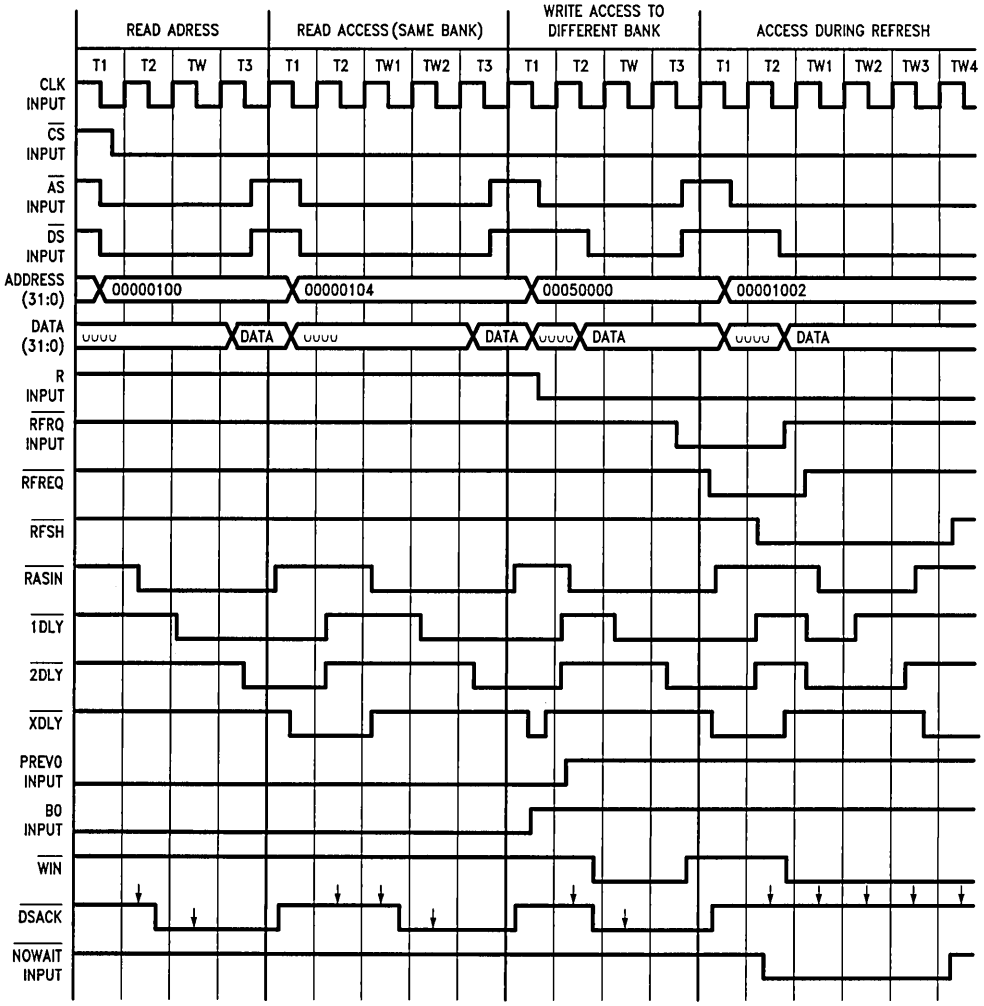

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FIGURE 3

Interface PAL # 1 System Timing Diagram (Continued)

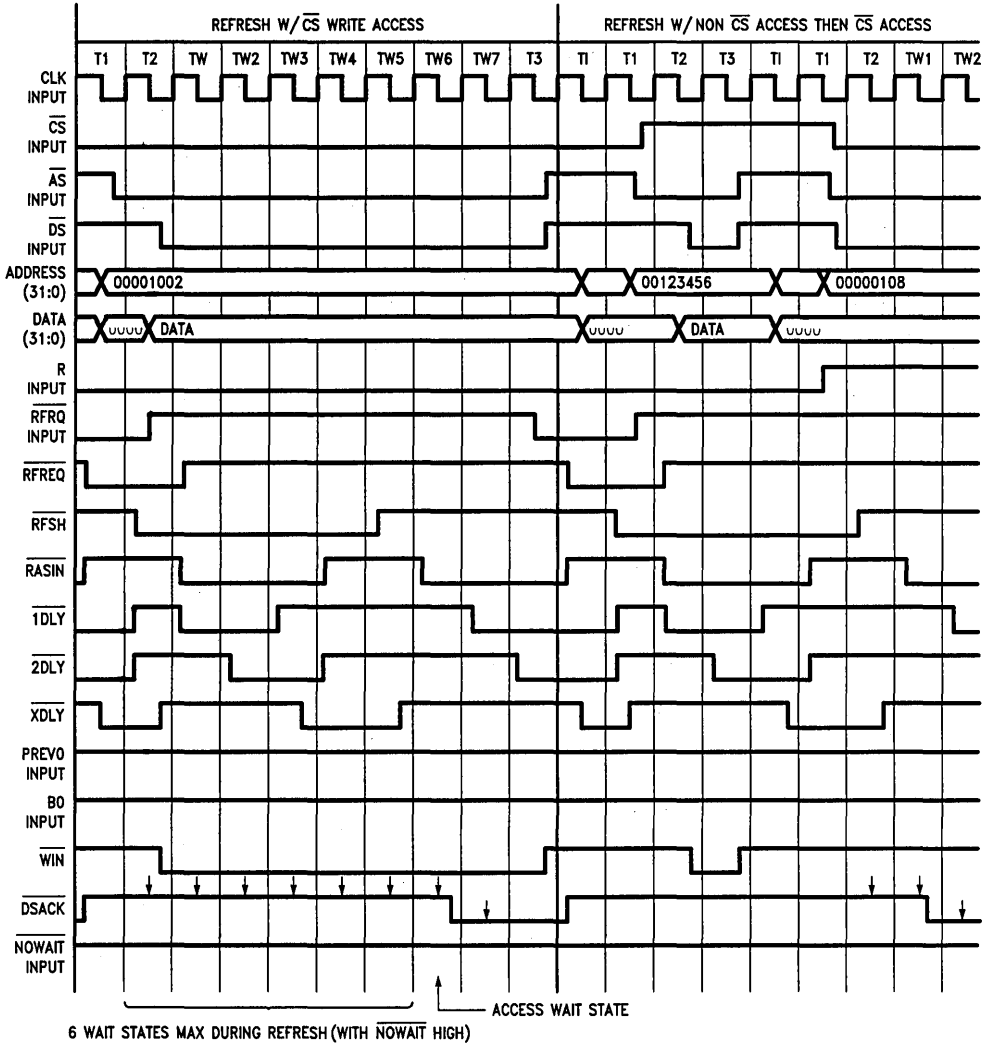

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FIGURE 4

Interface PAL # 1 System Timing Diagram (Continued)

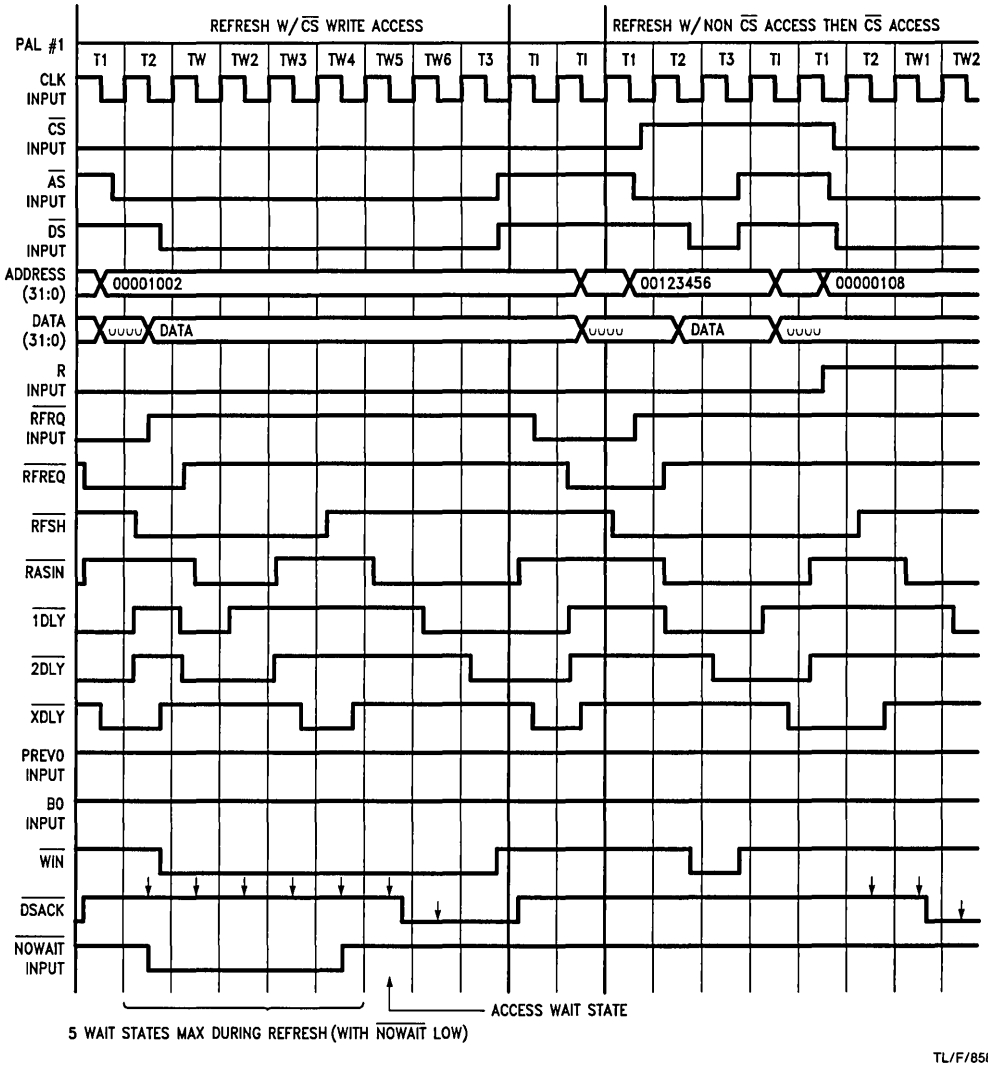

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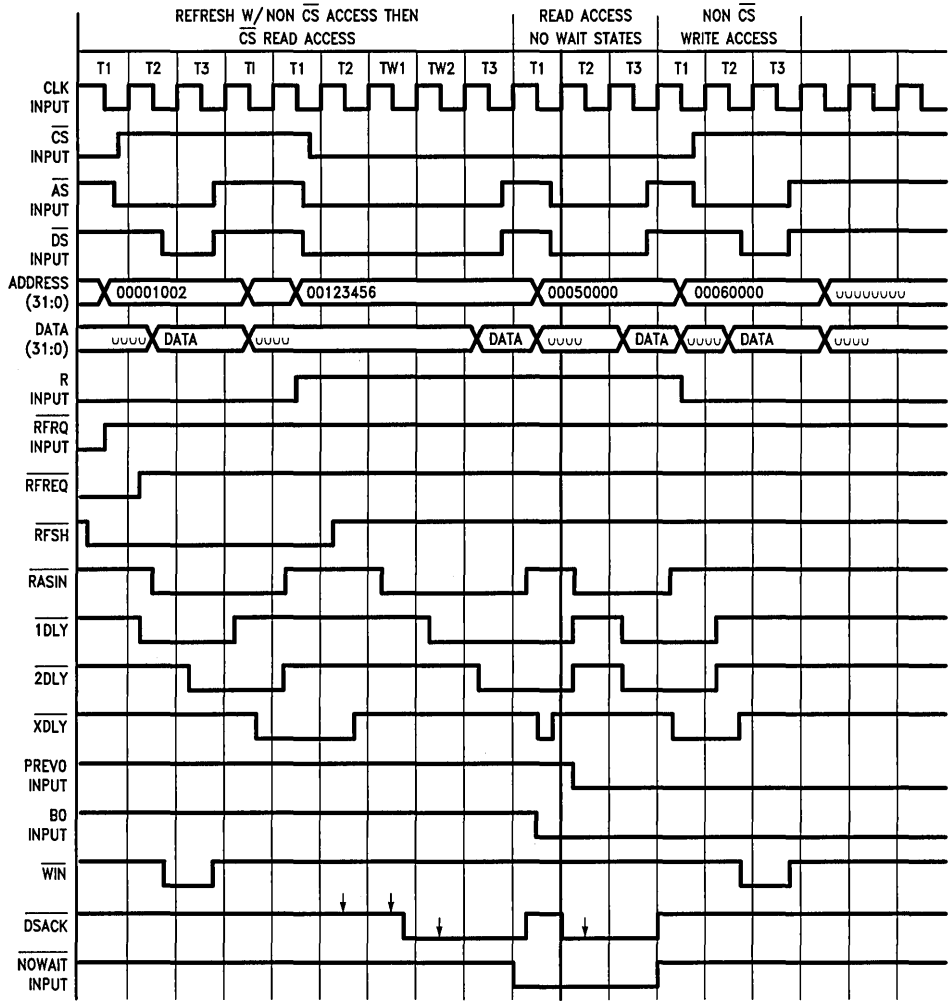
FIGURE 5

Interface PAL # 1 System Timing Diagram (Continued)



TL/F/8589–6

FIGURE 6

Interface PAL #2 Boolean Equations

This PAL is similar to PAL #1 but ends "$\overline{\text{RASIN}}$" one half period earlier than PAL #1 and relies on the external generation of byte "$\overline{\text{CAS}}$'s" to hold the data valid during 68020 READ access cycles.

```
DMPAL16R4A
CK  /AS  /RFRQ  /CS  R  CLK  NC1  NC2  /NOWAIT  GND
/OE  /DSACK  /RFREQCK  /RFREQ  /2DLY  /1DLY  /RFSH  /RASIN  /XDLY  VCC

IF (VCC) /XDLY = RFSH*/2DLY*/AS                  ;"/XDLY" during access
     +/RFSH*1DLY*/2DLY*/RASIN*NOWAIT*/CLK        ;"/XDLY" during RFSH
     +/RFSH*1DLY*2DLY*RASIN*RFREQ*/NOWAIT        ;"/XDLY" during RFSH
     +/RFSH*/XDLY*RFREQ                          ;Hold "/XDLY" low
     +/XDLY*RASIN*/AS*CLK                        ;Hold "/XDLY" low

IF (VCC) /RASIN = /RFSH*RFREQ*/1DLY          ;RFSH "/RASIN"
  +/RFSH*/RASIN*/2DLY*XDLY                   ;Hold in RFSH
  +/RFSH*/RASIN*/CLK                         ;Hold in RFSH
  +RFSH*RFREQCK*/AS*/CS*XDLY*CLK             ;Start "/RASIN"
  +RFSH*RFREQCK*/AS*/CS*2DLY*XDLY*CLK        ;After idle states
  +RFSH*/RASIN*/AS*/CS*XDLY                  ;Hold "/RASIN" low
  +RFSH*/RASIN*CLK                           ;Hold "/RASIN" low

IF (VCC) /RFREQCK = /RFREQ*/CLK              ;Start from falling clock
     +/RFREQCK*/RFREQ                        ;  edge

IF (VCC) /DSACK = /CS*RFSH*/RASIN*NOWAIT*/CLK   ;One WAIT state
  +/DSACK*/CS*RFSH*/RASIN*/AS                   ;Hold "/DSACK" low
  +/CS*RFSH*/AS*/NOWAIT*XDLY                    ;No WAIT state in access

/RFSH := /RFREQ*RASIN*/1DLY*/2DLY            ;Start RFSH
     +/RFREQ*RASIN*1DLY                      ;Start RFSH
     +/RFSH*/RFREQ                           ;Hold RFSH low
     +/RFSH*/RASIN                           ;Hold RFSH low
     +/RFSH*/1DLY                            ;Hold RFSH low

/1DLY := /RFSH*2DLY*/RFREQ                ;Start "/1DLY" during RFSH
     +/RFSH*/1DLY*2DLY*XDLY               ;Continue "/1DLY" during RFSH
     +RFSH*/RASIN                         ;Start "/1DLY" during /RASIN

/2DLY := /RFSH*/1DLY                      ;Start "/2DLY" during RFSH
     +/RFSH*2DLY*/RFREQ*/NOWAIT           ;Shorten RFSH
     +RFSH*/RASIN*/1DLY                   ;Start "/2DLY" during /RASIN
     +RFSH*/RASIN*/NOWAIT                 ;Shorten access

/RFREQ := /RFRQ                           ;Synchronize to system clock
```

Interface PAL #2 68020 System Diagram

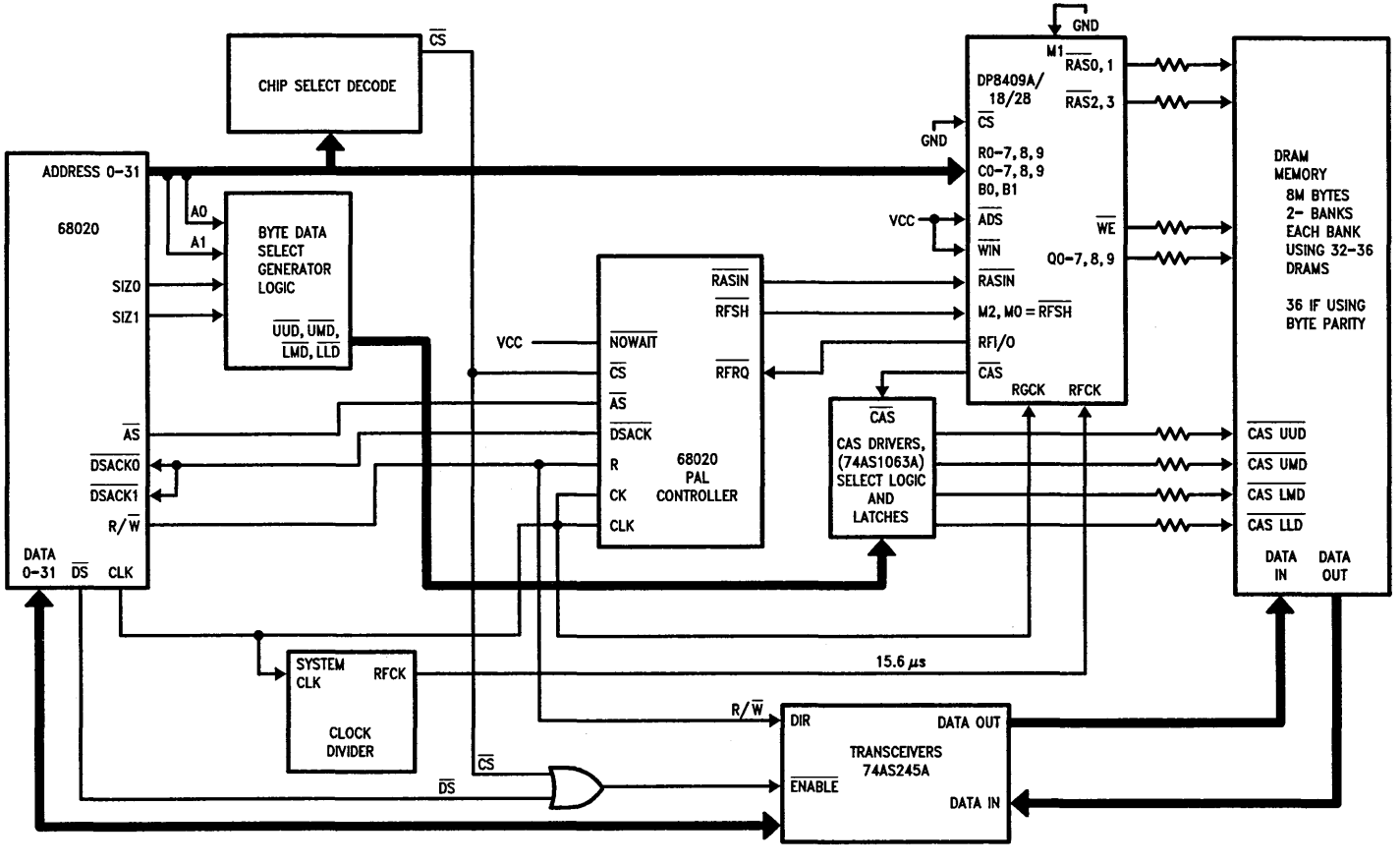


FIGURE 7

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Interface PAL #2 CAS Driver, Select Logic, and Latches

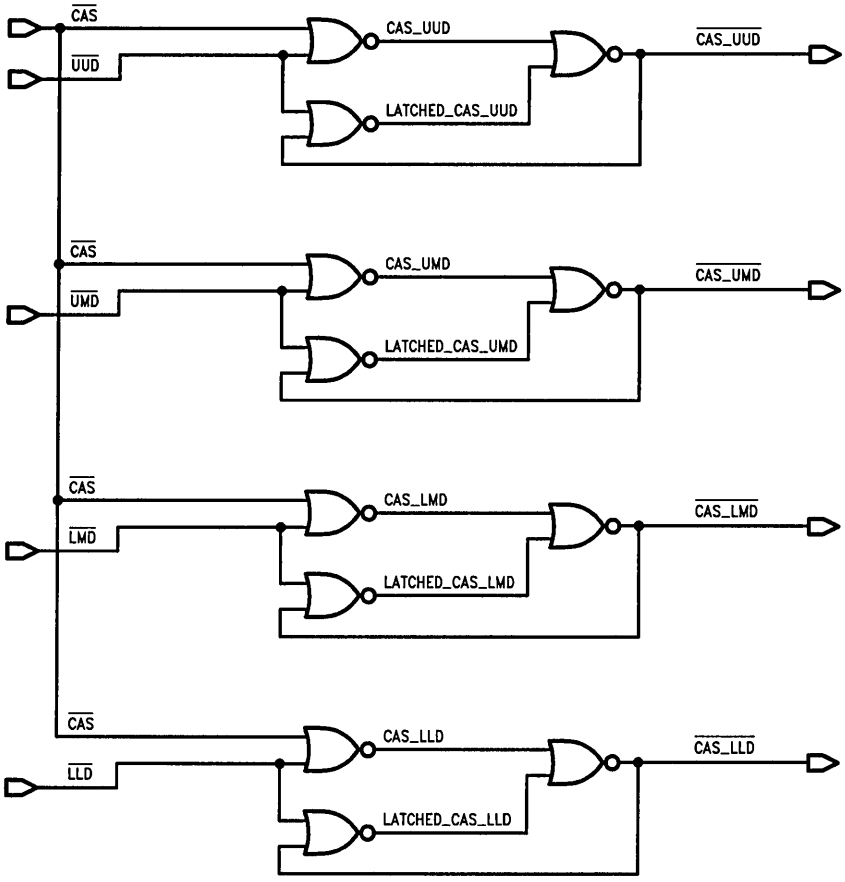

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FIGURE 8

Interface PAL #2 68020 System Timing Diagram

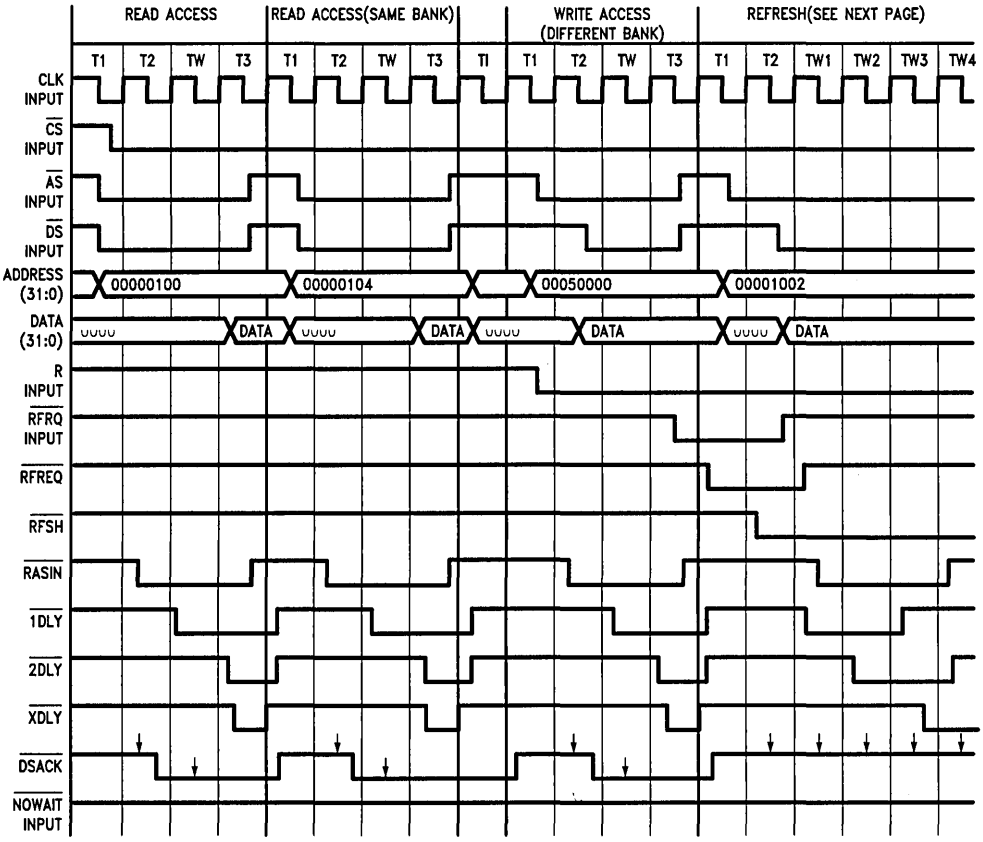

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FIGURE 9

Interface PAL #2 Between 68020 and DP8418 (Continued)

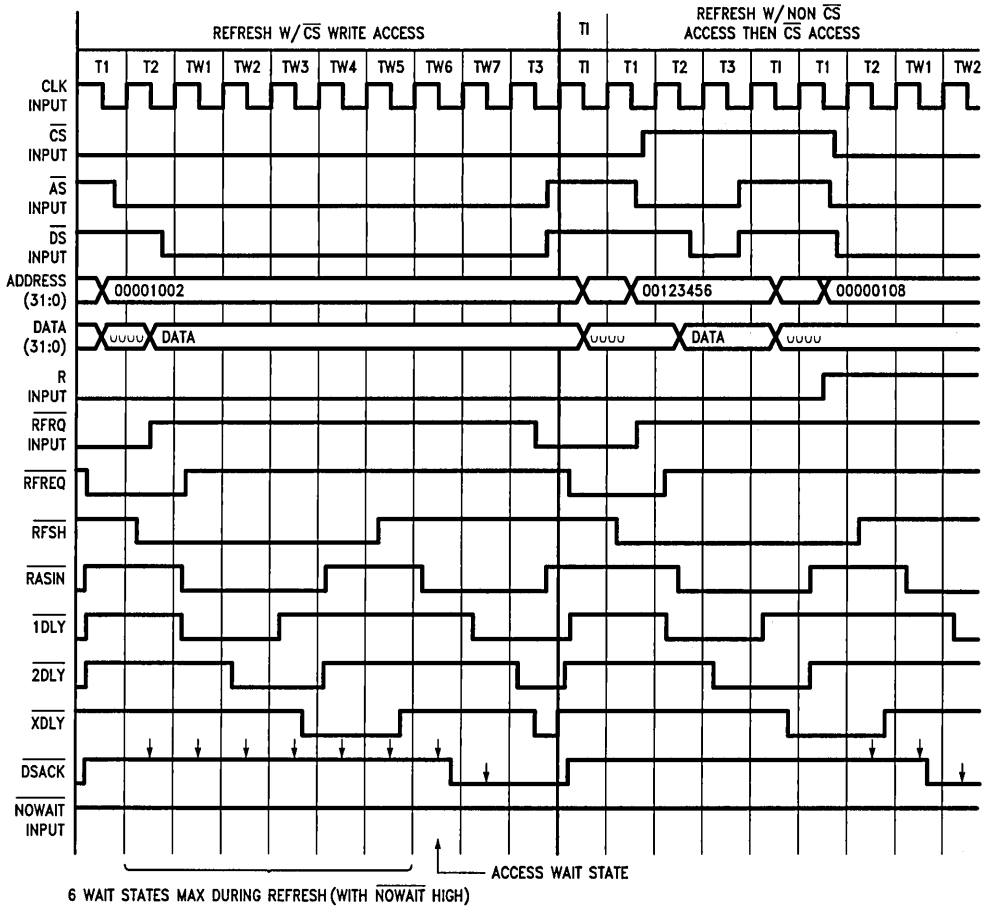

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FIGURE 10. System Timing

Interface PAL #2 Between 68020 and DP8418 (Continued)

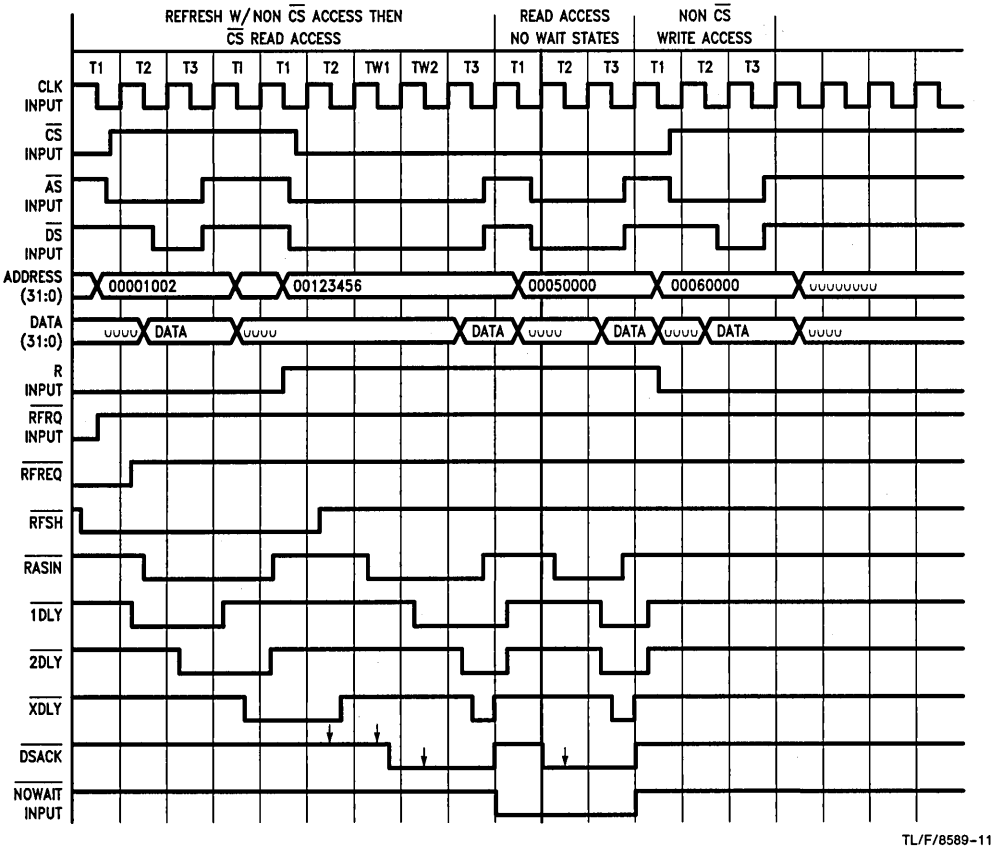

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FIGURE 11. System Timing

National Semiconductor Corporation

PRELIMINARY

DP84532 Dynamic RAM Controller Interface Circuit for the iAPX 286 CPU

General Description

This is a Programmable Array Logic (PAL®) device designed to allow an easy interface between the 80286 microprocessor and the National Semiconductor DP8419/29 or DP8409A dynamic memory controllers.

This PAL supplies all the control signals needed to perform memory read, write, and refresh operations up to a frequency of 16 MHz.

Features

- Provides a 3- or 4-chip solution for the 80286/DP8419 (or DP8409A/29) dynamic RAM interface (1 or 2 PALs, DP8419, and clock divider)
- Works with all speed versions of the 80286 up to 10 MHz
- Allows operation of 80286 at 8 MHz with no WAIT states with standard 120 ns 256k DRAMs
- Controls DP8409A/19 mode 5 accesses and mode 0 or 1 forced refreshes automatically
- Allows memory interleaving if desired
- CPU WAIT states are automatically inserted during contention between memory interleaving/DRAM accesses/DRAM refreshes
- Uses standard National Semiconductor PALs (i.e., DMPAL16R6A and DMPAL16R4A; the user may want to use faster versions of these PALs at higher CPU operating frequencies)
- The PAL programming equations are provided with comments for easy user modification to his specific requirements

Functional Description

The following description applies to both the DP8409A, DP8419 and DP8429.

A memory cycle starts when chip select ($\overline{CS}$) and the status ($\overline{S0}$*$\overline{S1}$) become true. $\overline{RASIN}$ is supplied from the PALs to the DP8419 DRAM controller, which then supplies $\overline{RAS}$ to the selected $\overline{RAS}$ bank. After the necessary row address hold time, the DP8419 switches the address outputs to the column address. The DP8419 then supplies the required $\overline{CAS}$ signal to the DRAM. In order to do byte operations a HIGH WRITE ENABLE and a LOW WRITE ENABLE are produced from PAL #2. All WRITE cycles are LATE WRITE cycles, to assure that valid data is written to the DRAMs. A $\overline{WRITE}$ strobe is produced by PAL #1 to assure enough $\overline{WIN}$ pulse width and to guarantee that valid data is latched into the DRAMs when writing to them. Memory buffers are used externally, to separate the data in from the data out of the DRAMs during LATE WRITE cycles.

Hidden REFRESH cycles are not allowed in this set of PALs because of the need for adequate $\overline{RAS}$ precharge times in all circumstances and the desire not to be inserting WAIT states into access cycles of other system elements.

These PALs perform automatic or externally controlled forced refreshes (mode 0 or 1). A refresh cycle occurs when the DP8419 input RFCK transitions low and the RFIO signal goes low requesting a refresh cycle. The PAL responds by pulling $\overline{RFSH}$ (M2, and/or MO depending on whether mode 1 or 0 is desired) low if there are no current DRAM accesses in progress. If a DRAM access is in progress the PAL waits until the current access is completed before performing the forced refresh cycle. If an access is requested during the forced refresh cycle WAIT states are automatically inserted into the access cycle until the refresh cycle is completed and adequate $\overline{RAS}$ precharge has been completed. The pending DRAM access cycle is then performed.

In order to guarantee adequate $\overline{RAS}$ precharge time during two consecutive accesses to the same DRAM bank, memory interleaving is performed by looking at the two lower address bits, A1 and A2. If the processor is sequentially accessing the DRAM, each $\overline{RAS}$ output will have plenty of precharge time. But if the system tries to access the same bank twice in a row the access will be delayed until adequate $\overline{RAS}$ precharge time has been met. During this time WAIT states will automatically be inserted into the pending access cycle.

The 8 MHz 80286 has two "T" states ("T_S" and "T_C"), it is possible for these PALs to get one clock phase out of sync with the 80286 CPU during access cycles pending while performing a refresh cycle. The two 8 MHz "T" states of the CPU contain four 16 MHz clock periods ("CLK" output of 82284 clock generator). This 2X clock is the clock the interface described herein uses. In other words, the PALs produce a $\overline{RASIN}$ output that is low for three 16 MHz clock periods for the 8 MHz 80286. Since WAIT states insert two 16 MHz clock periods and $\overline{RASIN}$ can start one clock period after $\overline{RFSH}$ transitions high, it is possible for $\overline{RASIN}$ to start one period early and go high one period before the access cycle ends, thus not holding the data valid during a READ access cycle long enough. To counteract this problem the term "ALE" is used in several of the PAL equations ($\overline{RASIN}$, $\overline{1DLY}$, and 2DLY) to sync the $\overline{RASIN}$ output to the access cycle. See the timing diagrams (*Figure 6*) and PAL equations for some further insight into the potential problems. This synchronization could also have been done externally by holding $\overline{CAS}$ low until either $\overline{MWTC}$ or $\overline{MRDC}$ go high, thus holding the READ data valid until the access cycle is over.

Two PALs were designed for this PAL interface. PAL #2 is used mostly for the support of memory interleaving. If one is not using memory interleaving (6 MHz or below) PAL #2 can be omitted and the PAL #1 "$\overline{PRECH}$" input can be tied high. The high and low memory write strobes can be produced externally.

Functional Description (Continued)

The PAL equations for this interface are written in the National Semiconductor PLAN™ format, which differs from the standard PALASM™ format.

EXAMPLE: PLAN FORMAT

```
/RASIN := RFSH*/2D*ALE
```

This translates as, "$\overline{\text{RASIN}}$" is low after the rising edge of the input clock given that "$\overline{\text{RFSH}}$" was high and "$\overline{\text{2D}}$" was low and "ALE" was high a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{2D}}$, and $\overline{\text{RFSH}}$ are outputs of the PAL and ALE is an input).

EXAMPLE: PALASM FORMAT

```
RASIN := /RFSH*2D*ALE
```

The above expression means the same as the PLAN format expression except it is written in PALASM format. In other words, "$\overline{\text{RASIN}}$" will go low after the rising edge of the clock given that "$\overline{\text{RFSH}}$" was high, "$\overline{\text{2D}}$" was low, and "ALE" was high a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{2D}}$, and $\overline{\text{RFSH}}$ are outputs of the PAL and ALE is an input).

Depending on the specific type of PALs and logic used, the user can calculate the speed requirements for the DRAM at the specified processor frequency as follows:

CALCULATION OF DRAM "t_{RAC}" $\overline{\text{RAS}}$ ACCESS TIME AND "t_{CAC}" $\overline{\text{CAS}}$ ACCESS TIME REQUIRED FOR AN 8 MHz 80286, NO WAIT STATE, MICROPROCESSOR SYSTEM

#1) $\overline{\text{RASIN}}$ generation time = one period of the system clock + one 74AS244 gate delay (the system clock is inverted to the PALs) + one clocked output delay of the PAL generating the $\overline{\text{RASIN}}$ output (assume DMPAL16R6B) = 62.5 ns + 4.5 ns + 12 ns = 79 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ out delay of the DP8419 = 20 ns maximum (used to determine "t_{RAC}")

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ out delay of the DP8419 DRAM controller driving a load of 4 banks of 256k DRAMs, each bank containing 18 (16 DRAMs plus byte parity) = 72 DRAMs

Since this is under the specified load in the data sheet (approximately 88 DRAMs) approximately 3 ns can be subtracted from the data sheet number, giving 80 ns − 3 ns = 77 ns maximum (used to determine "t_{CAC}").

#4) 74AS244 buffer delay = 7 ns maximum

#5) Data setup time required from the end of "T_C" phase 2 clock cycle = 10 ns minimum

A normal 8 MHz 80286 access cycle contains 4 clock periods (16 MHz) of 62.5 ns per period = 250 ns

The required DRAM "t_{RAC}" (row access time) can be calculated from 250 ns − #1 − #2 − #4 − #5 = 134 ns

The required DRAM "t_{CAC}" (column access time) can be calculated from 250 ns − #1 − #3 − #4 − #5 = 77 ns.

The DRAMs selected for this system must satisfy both the "t_{RAC}" and "t_{CAC}" requirements. Therefore the DRAMs must have a "t_{RAC}" (row access time) less than or equal to 134 ns and a "t_{CAC}" (column access time) less than or equal to 77 ns to be used in this system, under worst case conditions, for a no WAIT state, 8 MHz 80286 system. Common 120 ns 256k DRAMs meet this specification.

Other Options

In the system block diagram, buffers (74AS244s) were used to isolate the data in from the data out of the DRAM. This is needed because all WRITE accesses are late WRITEs (READ-MODIFY-WRITE cycles). In this system a HIGH and LOW WRITE enable were produced. The user could just as well have produced a HIGH and LOW CAS. In producing a HIGH and LOW CAS, the user would need the $\overline{\text{WRITE}}$ output of PAL #1 (to bring CAS low during a WRITE), A0 and $\overline{\text{BHE}}$ (for byte WRITEs), and the DT/$\overline{\text{R}}$ signal (for determining whether the access is a READ or WRITE access). Also, by generating a HIGH and LOW CAS, the system can use transceivers instead of buffers in the DRAM data path. The only problem with this approach is that $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ out may take a little longer since $\overline{\text{CAS}}$ goes through some external logic.

80286 PAL Inputs and Outputs

(Pin number of the PAL on the left)

PAL #1 INPUTS

1) "$\overline{CLK}$" This is the inverted system clock ("CLK") of the 82284 clock generator.

2) "$\overline{CS}$" This is the latched chip select (see system block diagram).

3) "$\overline{RFRQ}$" Refresh request from the DP8419.

4) "$\overline{S0}$" Status pin from the 80286.

5) "$\overline{S1}$" Status pin from the 80286.

6) "ALE" Address latch enable from 82288.

7) "NC1" No contact.

8) "$\overline{PRECH}$" This signal indicates that a back-to-back access cycle, to the same DRAM bank, is taking place. In this situation, the PAL controller will delay "$\overline{RASIN}$" until adequate $\overline{RAS}$ precharge time has been guaranteed, and also insert WAIT states into the present access cycle to accommodate the extra precharge time.

9) "NC2" No contact.

11) "$\overline{OE}$" This input enables the PAL outputs.

PAL #1 OUTPUTS

19) "$\overline{CYREQ}$" This signal indicates that an access was requested during a Refresh or during the precharge time of the previous access.

18) "$\overline{RFREQ}$" This output guarantees that the refresh request occurs within 15 ns after the system clock. This is necessary in order for the refresh/access arbitration to work correctly.

17) "$\overline{RASIN}$" This signal causes $\overline{RAS}$ (or $\overline{RAS}$s) to go low during a DRAM access or refresh.

16) "$\overline{RFSH}$" This signal initiates a DRAM Refresh.

15) "$\overline{1DLY}$" A delay that is used internally.

14) "$\overline{2DLY}$" A delay that is used internally.

13) "$\overline{SYNRDY}$" This output goes to the 82284 clock generator synchronous ready input. This output inserts WAIT states into DRAM access cycles during access/refresh/RAS precharge contention.

12) "$\overline{WRITE}$" This output produces a WRITE strobe for the DRAMs.

PAL #2 INPUTS

1) "ALE" This is the address latch enable input from the 82288.

2) "B0" This is the "A1" address bit from the 80286.

3) "B1" This is the "A2" address bit from the 80286.

4) "$\overline{RASIN}$" This signal causes $\overline{RAS}$ (or $\overline{RAS}$s) to go low during a DRAM access or refresh.

5) "$\overline{1DLY}$" This is a delay used internal to the PALs.)

6) "$\overline{RFSH}$" This signal initiates a DRAM Refresh.

7) "$\overline{WRITE}$" This output produces a WRITE strobe for the DRAMs.

8) "A0" This is the "A0" address bit from the 80286 and is used during byte read or byte write situations.

9) "$\overline{BHE}$" This is the high byte enable signal from the 80286 and is used during byte read or byte write situations.

11) "$\overline{OE}$" This input enables the PAL outputs.

PAL #2 OUTPUTS

19) "$\overline{PRECH}$" This signal indicates that a back-to-back access cycle, to the same DRAM bank, is taking place. In this situation, the PAL controller will delay "$\overline{RASIN}$" until adequate $\overline{RAS}$ precharge time has been guaranteed, and also insert WAIT states into the present access cycle to accommodate the extra precharge time.

18) "NC" No contact to this pin.

17) "$\overline{PREV0}$" Latches if the previous access was to Bank 0.

16) "$\overline{PREV1}$" Latches if the previous access was to Bank 1.

15) "$\overline{PREV2}$" Latches if the previous access was to Bank 2.

14) "$\overline{PREV3}$" Latches if the previous access was to Bank 3.

13) "$\overline{WINLOW}$" This is the low byte DRAM write input.

12) "$\overline{WINHIGH}$" This is the high byte DRAM write input.

Equations for PALs to Interface the DP8419 to the 80286

These PALs work up to 10 MHz and use mode 0 for doing externally controlled forced refreshes, guaranteeing 3 periods (of 2X clock from 82284) of RGCK RAS pulse width. This set of PALs will only work for the DP8419 since they use mode 0 forced refresh to reset the refresh request (RFIO) signal.

```
PAL #1
DMPAL16R6A
/CLK  /CS  /RFRQ  /S0  /S1  ALE  NC1  /PRECH  NC2  GND
/OE  /WRITE  /SYNRDY  /2DLY  /1DLY  /RFSH  /RASIN  /RFREQ  /CYREQ  VCC

IF (VCC) /CYREQ = /CS*/RFSH*S0*/S1                  ;Read access during RFSH
          +/CS*/RFSH*/S0*S1                         ;Write access during RFSH
          +/CYREQ*/RFSH                             ;Hold "/CYREQ" during RFSH
          +/CYREQ*RASIN                             ;Hold "/CYREQ"
          +/CYREQ*1DLY                              ;Hold "/CYREQ"
          +/CS*RASIN*1DLY*/2DLY*S0*/S1              ;Precharge needed during access
          +/CS*RASIN*1DLY*/2DLY*/S0*S1              ;Precharge needed during access

IF (VCC) /WRITE = /S0*S1*/CS*ALE                    ;Write access
          +/WRITE*1DLY                              ;Hold "/WRITE" low
          +/WRITE*/RFSH                             ;Hold "/WRITE" low
          +/WRITE*/RASIN                            ;Hold "/WRITE" low

/RFREQ := /RFRQ

/RASIN := /RFSH*/1DLY*/ALE                          ;RFSH "/RASIN" except if "ALE"
  +/RFSH*/1DLY*/RASIN                               ;Keep "/RASIN" low during RFSH
  +RFSH*/S0*S1*PRECH*RFREQ*/ALE*/CS                 ;WRITE access
  +RFSH*S0*/S1*PRECH*RFREQ*/ALE*/CS                 ;READ access
  +/RASIN*RFSH*2DLY                                 ;Hold "/RASIN" low
  +RFSH*/CYREQ*1DLY*2DLY*/ALE                       ;"/RASIN" after precharge delay
                                                    ;  or RFSH

/RFSH := /RFREQ*RASIN*1DLY*/2DLY                    ;Start RFSH after access
  +/RFREQ*RASIN*/1DLY*/2DLY                         ;Start RFSH after access
  +/RFREQ*RASIN*1DLY*2DLY*CYREQ                     ;Start RFSH after idle states
  +/RFSH*/1DLY                                      ;Hold RFSH low
  +/RFSH*/2DLY                                      ;Hold RFSH low
  +/RFSH*/RFREQ                                     ;Hold RFSH low

/1DLY := /RFSH*2DLY*/RFREQ                          ;"/1DLY" during RFSH
  +/RFSH*/RASIN*2DLY*/1DLY                          ;Hold "/1DLY" low
  +/RFSH*/RASIN*/1DLY*ALE                           ;Hold "/1DLY" low if "ALE"
  +RFSH*/RASIN                                     "/1DLY" during access

/2DLY := /RFSH*/RASIN                               ;"/2DLY" during RFSH
+/RFSH*/2DLY*ALE                                    ;Hold "/2DLY" low if "ALE"
+RFSH*/RASIN*/1DLY                                  ;"/2DLY" during access
+RFSH*/1DLY*/2DLY*/PRECH*RASIN*RFREQ                ;Hold "/2DLY" low for precharge

/SYNRDY := /CS*/RASIN*1DLY*RFSH                     ;"/SYNRDY" during an access
```

Equations for PALs to Interface the DP8419 to the 80286 (Continued)

```
PAL #2

DMPAL16R4A
ALE  B0  B1  /RASIN  /1DLY  /RFSH  /WRITE  A0  /BHE  GND
/OE  /WINHIGH  /WINLOW  /PREV3  /PREV2  /PREV1  /PREV0  NC  /PRECH  VCC

IF (VCC) /PRECH = RFSH*/B0*/B1*/PREV0*RASIN*/1DLY   ;Need precharge during
         +RFSH*B0*/B1*/PREV1*RASIN*/1DLY             ;  present access if
         +RFSH*/B0*B1*/PREV2*RASIN*/1DLY             ;  previous access bank =
         +RFSH*B0*B1*/PREV3*RASIN*/1DLY              ;  present access bank

/PREV0 := /B0*/B1                          ;Previous access to bank 0

/PREV1 := B0*/B1                           ;Previous access to bank 1

/PREV2 := /B0*B1                           ;Previous access to bank 2

/PREV3 := B0*B1                            ;Previous access to bank 3

IF (VCC) /WINLOW = RFSH*/RASIN*/1DLY*/A0*/WRITE    ;"/WRITE" during access

IF (VCC) /WINHIGH = RFSH*/RASIN*/1DLY*/BHE*/WRITE  ;"/WRITE" during access
```

Equations for PALs to Interface the DP8409A or DP8419 to the 80286

These PALs work up to 10 MHz with the DP8419 and up to a frequency where the minimum RGCK high or low pulse width (of 82284 2X clock) is equal to or greater than 35 ns for the DP8409A. These PALs only guarantee 2 system clock periods of RAS low during refresh and 2 periods of RAS precharge time (of 82284 2X clock) between consecutive accesses to the same RAS bank.

```
PAL #1

DMPAL16R6A
/CLK  /CS  /RFRQ  /S0  /S1  ALE  NC1  /PRECH  NC2 GND
/OE  /WRITE  /SYNRDY  /2DLY  /1DLY  /RFSH  /RASIN  /RFREQ  /CYREQ  VCC

IF (VCC) /CYREQ = /CS*/RFSH*S0*/S1          ;Read access during RFSH
           +/CS*/RFSH*/S0*S1                ;Write access during RFSH
           +/CYREQ*/RFSH                    ;Hold "/CYREQ" during RFSH
           +/CYREQ*RASIN                    ;Hold "/CYREQ"
           +/CYREQ*1DLY                     ;Hold "/CYREQ"
           +/CS*RASIN*1DLY*/2DLY*S0*/S1     ;Precharge needed during access
           +/CS*RASIN*1DLY*/2DLY*/S0*S1     ;Precharge needed during access

IF (VCC) /WRITE = /S0*S1*/CS*ALE            ;Write access
           +/WRITE*1DLY                     ;Hold "/WRITE" low
           +/WRITE*/RFSH                    ;Hold "/WRITE" low
           +/WRITE*/RASIN                   ;Hold "/WRITE" low

/RFREQ := /RFRQ

/RASIN := RFSH*/S0*S1*PRECH*RFREQ*/ALE*/CS      ;WRITE access
     +RFSH*S0*/S1*PRECH*RFREQ*/ALE*/CS          ;READ access
     +/RASIN*RFSH*2DLY                          ;Hold "/RASIN" low
     +RFSH*/CYREQ*1DLY*2DLY*/ALE                ;"/RASIN" after precharge
                                                ;  delay or RFSH

   /RFSH := /RFREQ*RASIN*1DLY*/2DLY             ;Start RFSH after access
        +/RFREQ*RASIN*/1DLY*/2DLY               ;Start RFSH after access
        +/RFREQ*RASIN*1DLY*2DLY*CYREQ           ;Start RFSH after idle states
        +/RFSH*/1DLY                            ;Hold RFSH low
        +/RFSH*/2DLY                            ;Hold RFSH low
        +/RFSH*/RFRQ                            ;Hold RFSH low
```

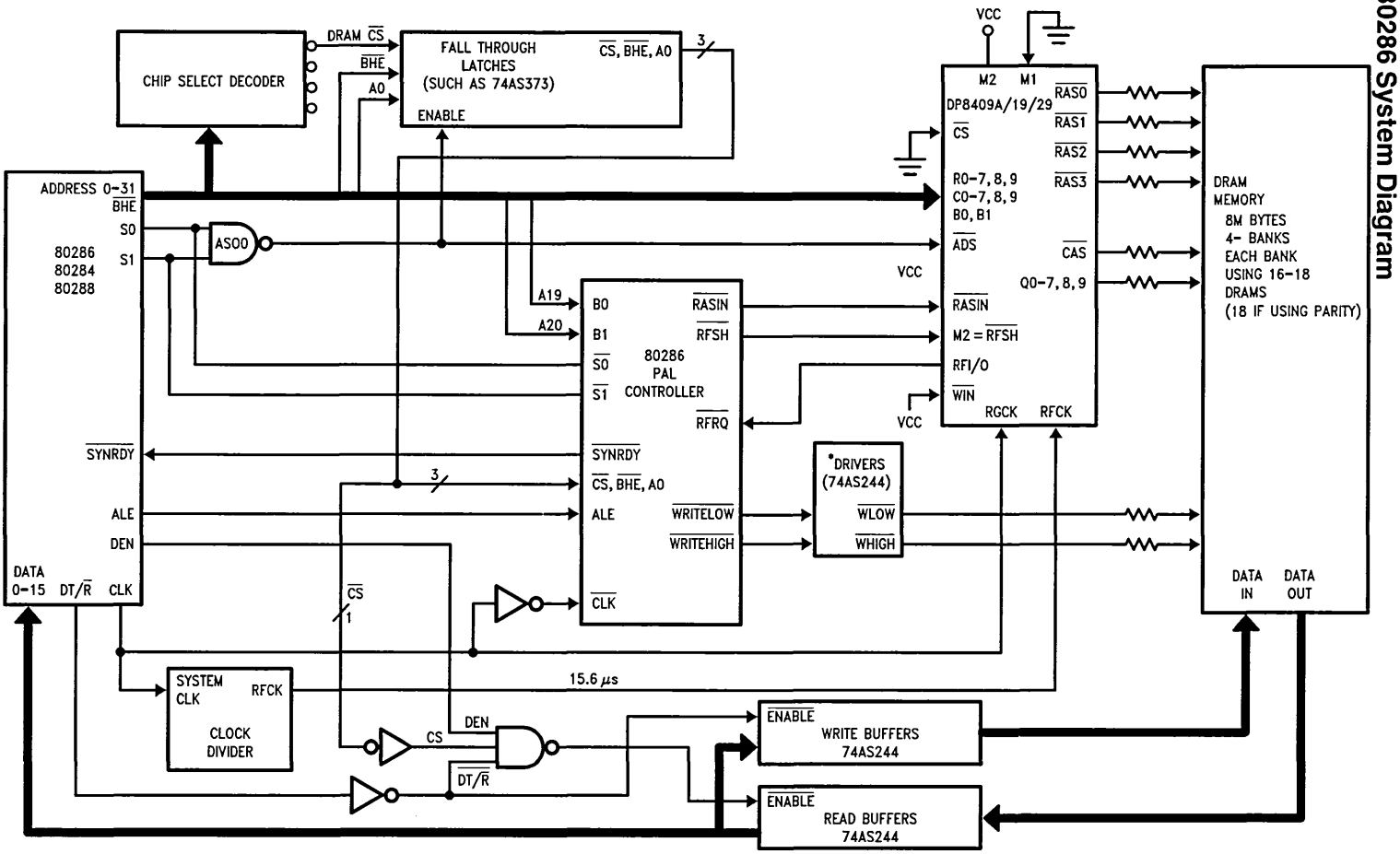
Equations for PALs to Interface the DP8409A or DP8419 to the 80286

(Continued)

```
/1DLY := /RFSH*2DLY*/RFRQ                    ;"/1DLY" during RFSH
      +/RFSH*/1DLY*2DLY                      ;Hold "/1DLY" low
      +RFSH*/RASIN                           ;"/1DLY" during access

/2DLY := /RFSH*/1DLY*/ALE                    ;"/2DLY" during RFSH
         +/RFSH*/2DLY*ALE                    ;Hold "/2DLY" low if "ALE"
         +RFSH*/RASIN*/1DLY                  ;"/2DLY" during access
         +RFSH*/1DLY*/2DLY*/PRECH*RASIN*RFREQ ;Hold "/2DLY" low for precharge

/SYNRDY := /CS*/RASIN*1DLY*RFSH              ;"/SYNRDY" during an access
```

If only 2 banks of DRAM were to be used the PAL interface would require only 1 PAL. The two inputs "$\overline{\text{PRECHOUT}}$ and NC" (pin #8 and #9) could be changed to "B0" and "$\overline{\text{PREVB0}}$" to allow interleaving of bank 0 and 1. "$\overline{\text{PREVB0}}$" could be produced externally using a "D" type flip-flop with "ALE" as its clock and "B0" as its input. The equations for "$\overline{\text{RASIN}}$" and "$\overline{\text{2DLY}}$" will have to be changed as follows:

```
/RASIN := /RFSH*/1DLY*/ALE                   ;RFSH "/RASIN"
  +/RFSH*/1DLY*/RASIN                        ;Hold "/RASIN" low in RFSH
  +RFSH*/S0*S1*B0*/PREVB0*RFREQ*/ALE*/CS     ;WRITE access
  +RFSH*/S0*S1*/B0*PREVB0*RFREQ*/ALE*/CS     ;WRITE access
  +RFSH*S0*/S1*B0*/PREVB0*RFREQ*/ALE*/CS     ;READ access
  +RFSH*S0*/S1*/B0*PREVB0*RFREQ*/ALE*/CS     ;READ access
  +/RASIN*RFSH*2DLY                          ;Hold ""/RASIN'' low
  +RFSH*/CYREQ*1DLY*2DLY*/ALE                ;"/RASIN" after precharge
                                             ;  delay or RFSH

/2DLY := /RFSH*/1DLY                         ;"/2DLY" during RFSH
   +/RFSH*/2DLY*ALE                          ;Hold "/2DLY" low if "ALE"
   +RFSH*/RASIN*/1DLY                        ;"/2DLY" during access
   +RFSH*/1DLY*/2DLY*/B0*/PREVB0*RASIN*RFREQ ;Hold "/2DLY" low for precharge
```

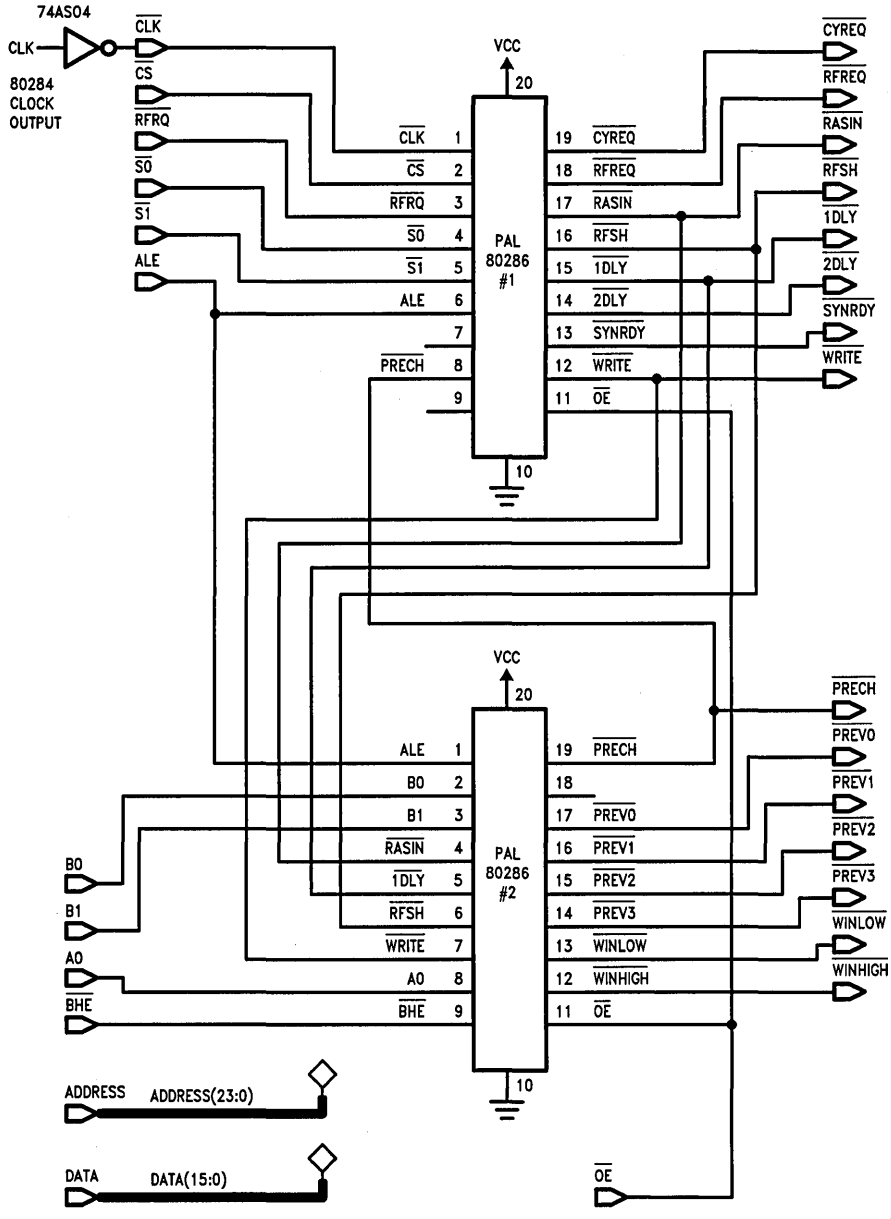


*Drivers may not be needed depending on the load being driven.

TL/F/8590-1

FIGURE 1

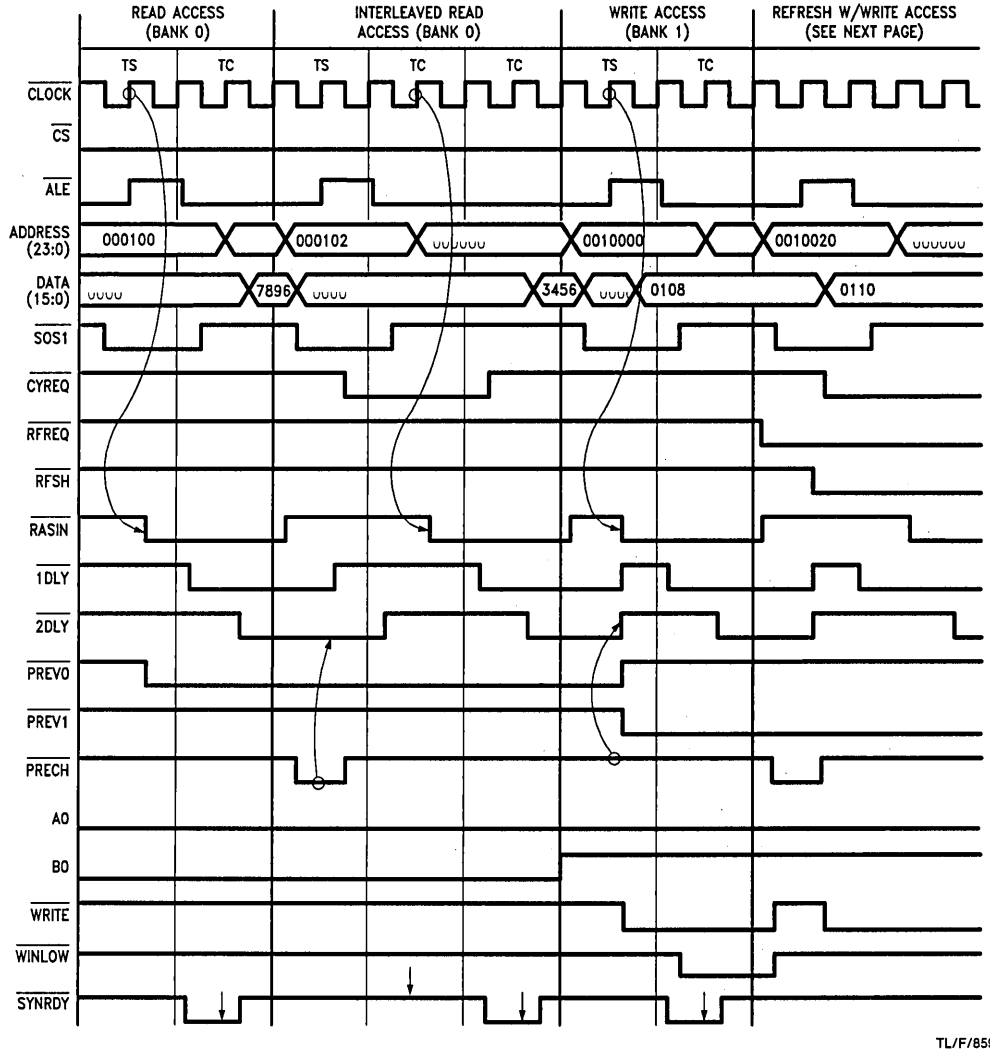
80286 System Diagram (Continued)



TL/F/8590–2

FIGURE 2. 80286 PALs

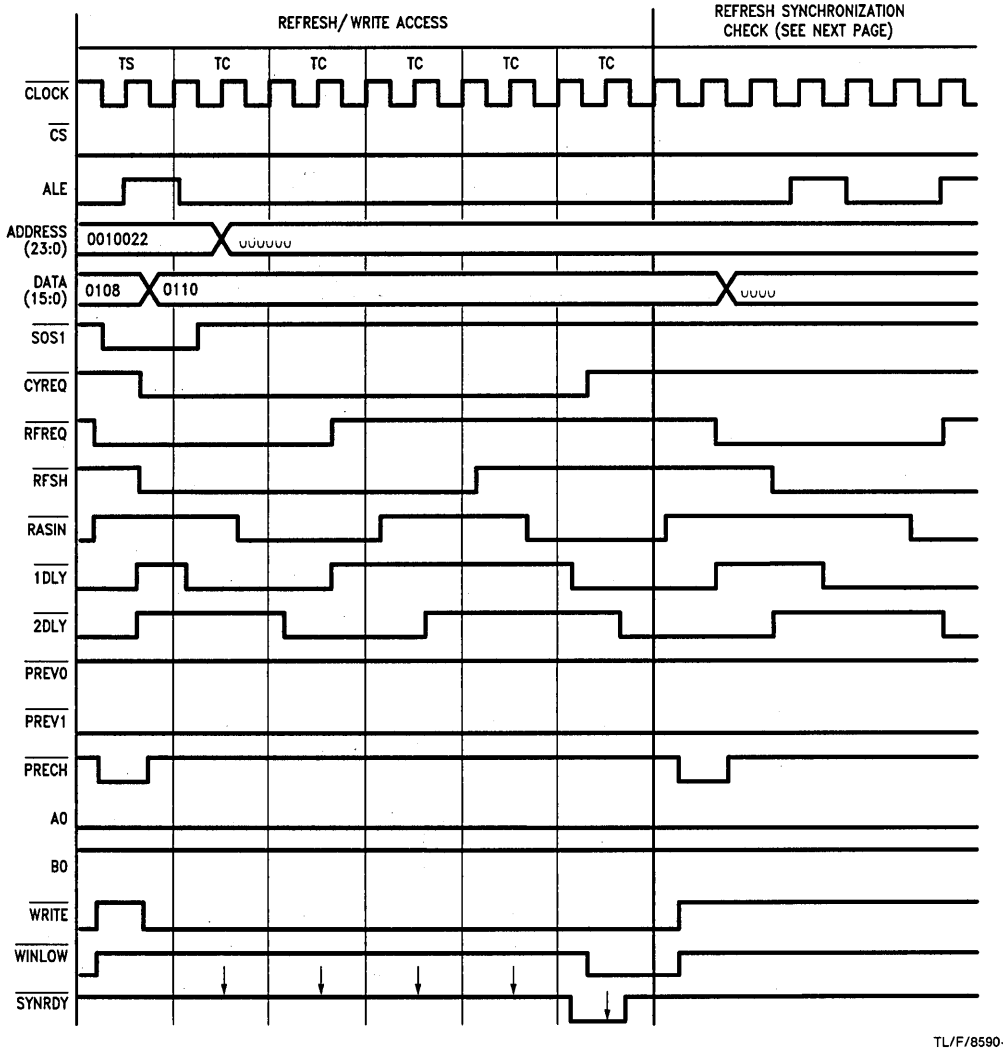
System Timing Diagram



TL/F/8590–3

FIGURE 3

System Timing Diagram (Continued)



TL/F/8590–4

FIGURE 4

System Timing Diagram (Continued)

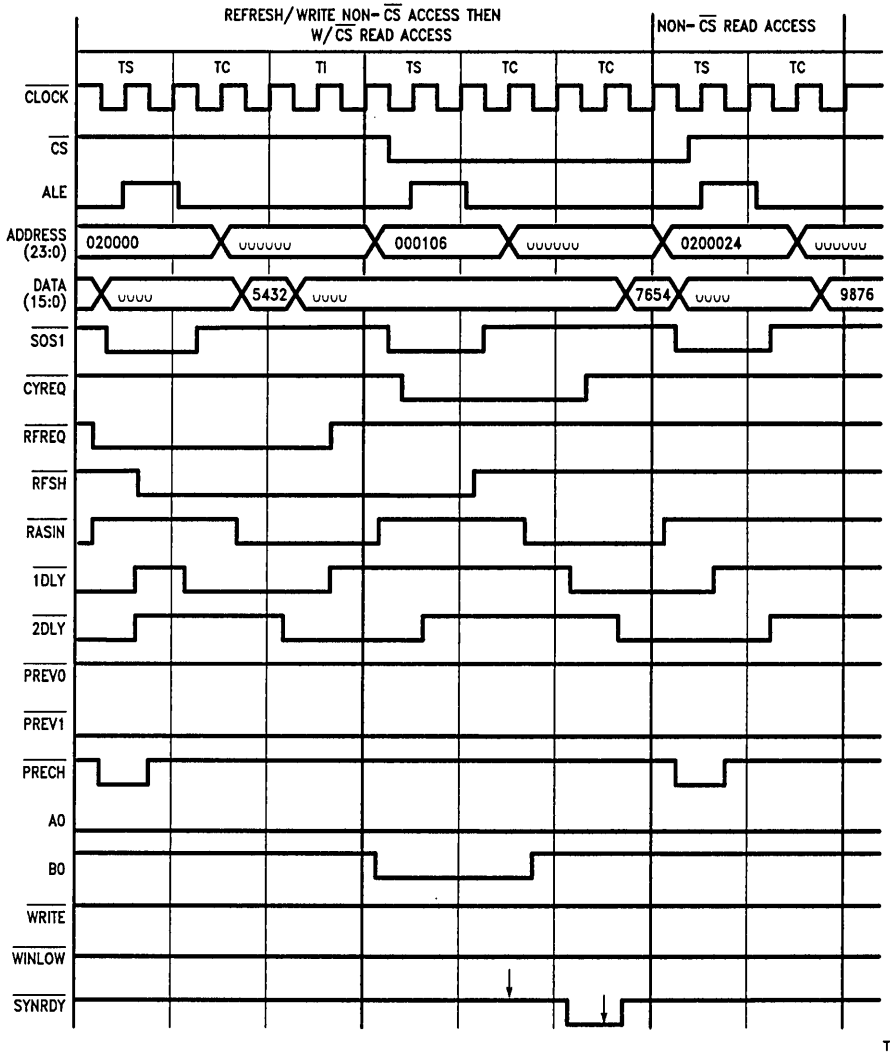


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FIGURE 5

System Timing Diagram (Continued)

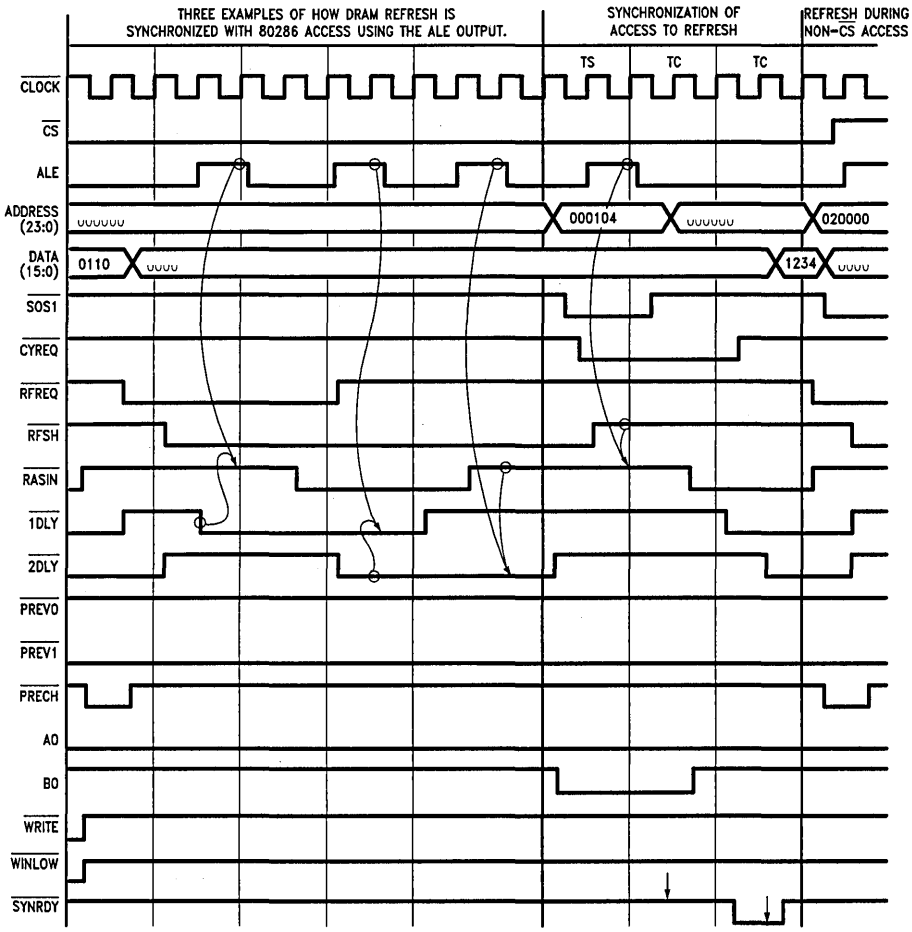

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FIGURE 6

Interfacing the DP8408A/09A To Various Microprocessors

National Semiconductor
Application Note 309
Chuck Pham, Webster (Rusty) Meier

High storage density and low cost have made dynamic RAMs the designer's choice in most memory applications. However, the major drawback of dynamic RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for some minimum time after $\overline{RAS}$ (namely the row address hold time of the dynamic RAMs, t_{RAH}), the column address is set up and then $\overline{CAS}$ occurs. In addition, refreshing must be done periodically to keep all memory cells charged.

With the introduction of the DP8408A Dynamic RAM Controller/Driver, the above complexities are simplified. The DP8408A is housed in a 48-pin package with eight multiplexed address outputs (Q0–7) and six control outputs ($\overline{RAS}$0–3, $\overline{CAS}$, $\overline{WE}$). It consists of two 8-bit address latches and an 8-bit refresh counter. All the output drivers are capable of driving 500 pF loads.

The following discussion demonstrates a typical application of the DP8408A Dynamic RAM Controller/Driver in Z8000™- and Z80®-based systems. The DP8408A basically has six modes of operation: Externally Controlled Refresh, Externally Controlled All-$\overline{RAS}$ Write, Externally Controlled Access, Auto Access (slow t_{RAH}), Auto Access (fast t_{RAH}) and Set End of Count.

The DP8408A, operating in the auto access mode, requires only $\overline{RASIN}$ to initiate a memory access cycle because all the dynamic RAM's control signals are automatically delayed from this input. (Refer to *Figure 1* for the auto access timing sequence.)

In the following applications, the DP8408A operates in either mode 5 or mode 6 Auto Access and mode 1 or 2 Externally Controlled Refresh to provide minimum additional logic.

The DP8408A and Z8000 Interface

MEMORY ACCESS CYCLE

Figure 2a shows the detailed block diagram of Z8000 and the DP8408A interface. Consider a memory cycle of the Z8000; first, the memory address is output on the Address and Data multiplexed bus (AD0–15) during T1 and is latched to the DP8408A by $\overline{AS}$. Simultaneously, $\overline{MREQ}$ goes low and is used to provide $\overline{RASIN}$ to initiate a memory transaction cycle. Then the selected $\overline{RAS}$ output, row address hold time (t_{RAH}), column address set up time (t_{ASC}) and $\overline{CAS}$ output will follow $\overline{RASIN}$ as determined by the auto access modes. A maximum of one wait state is required for 6 MHz and 10 MHz CPUs. This wait state is automatically inserted by the $\overline{CAS}$ output of the DP8408A. For systems using byte-writing, the DM74S158 provides two separate $\overline{CAS}$ outputs for accessing the low and high byte of memory. Note that $\overline{DS}$ from the Z8000 is also gated with the DP8408A's CAS output to generate $\overline{CASL}$ and $\overline{CASH}$. This guarantees the valid data from the Z8000 being written into memory during memory write cycles. Refer to *Figure 3* for the detailed memory transaction cycle timing.

The following formula allows the designer to determine the proper memory speed in terms of t_{CAC} (access time from $\overline{CAS}$):

$$t_{CAC}\ \text{max.} = 3 \times t_{cC} - \text{tdc(MR)} - t_{RICL} - t_{CASdly} - t_{sDR}(C) - 15.$$

The Z8000 parameters:

t_{cC}: clock cycle time

$t_{sDR}(C)$: read data to clock ↓ set up time

tdc(MR): clock to $\overline{MREQ}$ delay

The DP8408A, 74S158 and 74LS245 parameters:

t_{RICL}: RASIN to CAS delay

t_{CASdly}: the propagation delay of the 74S158

15 ns: the propagation delay of the 74LS245 (at 50 pF load)

For the 10 MHz CPU and the DP8408A:

$t_{CAC}\ \text{max.} = 300 - 40 - 131 - 14 - 10 - 15 = 90$ ns.

- t_{RICL} max. (mode 6) = 131 ns at 15 pF load.
- t_{CASdly} max. = 14 ns at 50 pF load.

Since $\overline{MREQ}$ is connected directly to $\overline{RASIN}$, t_{RP} ($\overline{RAS}$ precharge time) and t_{RAS} ($\overline{RAS}$ pulse width) are determined by $\overline{MREQ}$ high and low, respectively.

MEMORY REFRESH CYCLE

The Z8000 CPU contains a refresh rate counter for automatic memory refresh. This counter should be programmed during the processor initialization to determine the refresh rate. Since memory refresh is automatically inserted by the Z8000, there is no additional refresh arbitration logic allowed. The CPU's STATUS 3 (ST3) output can be directly connected to the M2 ($\overline{RFSH}$) pin of the DP8408A. During the memory refresh cycle, ST3 goes low, setting the DP8408A in the external control refresh mode (mode 2). Then all four $\overline{RAS}$ outputs will follow $\overline{MREQ}$ to strobe the DP8408A's refresh address to all memory banks (the Z8000 refresh address is ignored). As $\overline{MREQ}$ goes high again, the DP8408A increments its refresh counter, preparing it for the next refresh cycle. Refer to *Figure 4* for the refresh cycle timing. Note that ST3 also goes low during the internal cycle, I/O reference cycle and interrupt acknowledge cycle, but the memory will not be refreshed because $\overline{MREQ}$ is not active during these cycles. The DP8408A on-chip refresh counter will not be incremented when M2 goes low unless $\overline{MREQ}$ is inserted.

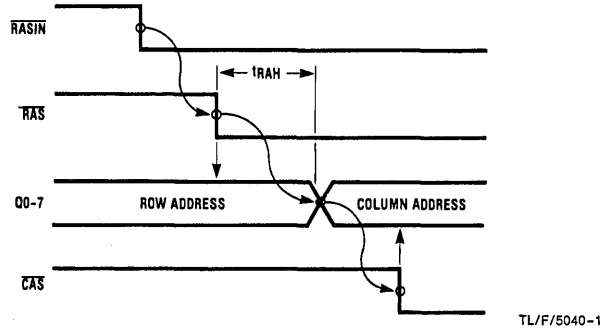

FIGURE 1. Auto Access Timing Sequence (Mode 5 or Mode 6)

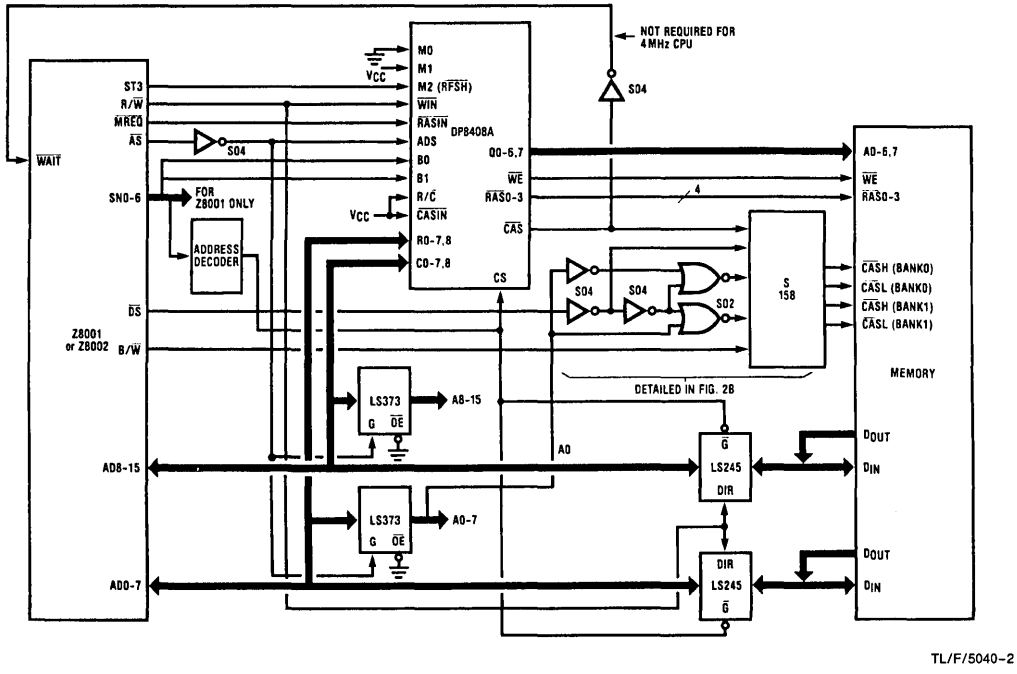

FIGURE 2a. Z8000 and DP8408A Interface

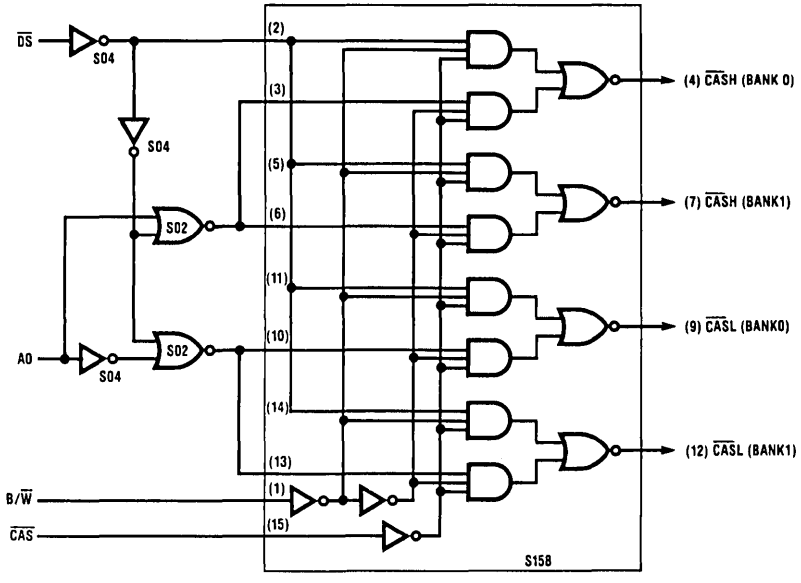

FIGURE 2b. CASH and CASL Decoder

When the processor is in either halt state (by executing the privileged HALT instruction) or single-stepping mode (when STOP) input is low), it introduces memory refresh cycles. However, care should be taken when the CPU is in either a WAIT state or a Bus Acknowledge cycle, that the dynamic RAM refresh will not take place. If these conditions occur over a long period of time, a burst refresh is recommended. This can be done by toggling RASIN while keeping M2 low, until all the rows of the dynamic RAM have been refreshed, then the CPU can resume its operations.

The DP8408A and Z80A® Interface

INSTRUCTION FETCH CYCLE

Figure 5 shows the detailed interconnections between the DP8408A, the Z80 and the Dynamic RAMs. *Figure 6* shows the timing during an M1 cycle (op code fetch). The program counter is output on the address bus at the beginning of the M1 cycle. One-half clock later MREQ goes active. This input is used to provide RASIN to the DP8408A to access the dynamic memory. Subsequently, the selected RAS output, Row to Column Select and then CAS output will automatically follow RASIN as determined by the Auto Access modes of the DP8408A. The RD line also goes active to indicate a memory read cycle is in progress. After t_{CAC} (access time from CAS), read data becomes valid. This data is sampled on the rising edge of T3, then both MREQ and RD go inactive. Immediately following this, RFSH goes low, putting the DP8408A in the Externally Controlled Refresh mode. The MREQ goes active causing all four RAS outputs to go active to perform a refresh to all the banks of the dynamic RAMs. Note that during memory refresh cycles, the refresh address from the CPU is output on the address bus. However, the contents of the DP8408A on-chip refresh counter are used instead to provide the row address to the dynamic memory array. Since the Z80 provides only a 7-bit refresh address, it is an advantage to use the DP8408A 8-bit refresh counter to support 64k dynamic RAMs directly. The DP8408A refresh counter is incremented as MREQ returns high, ending the memory refresh. The RFSH goes inactive returning the DP8408A back to the Auto Access mode, preparing it for the next access cycle.

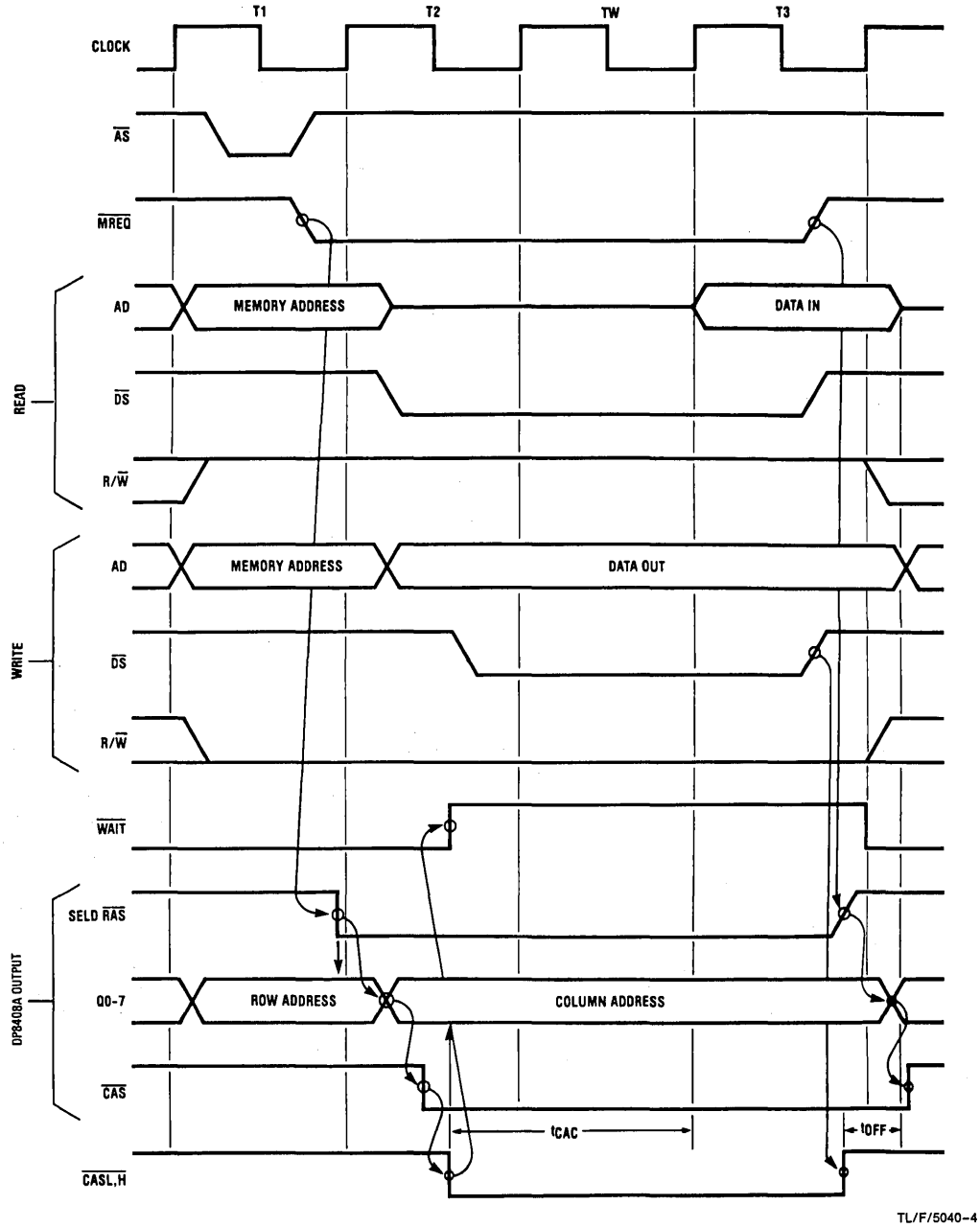

FIGURE 3. Memory Transaction Cycles

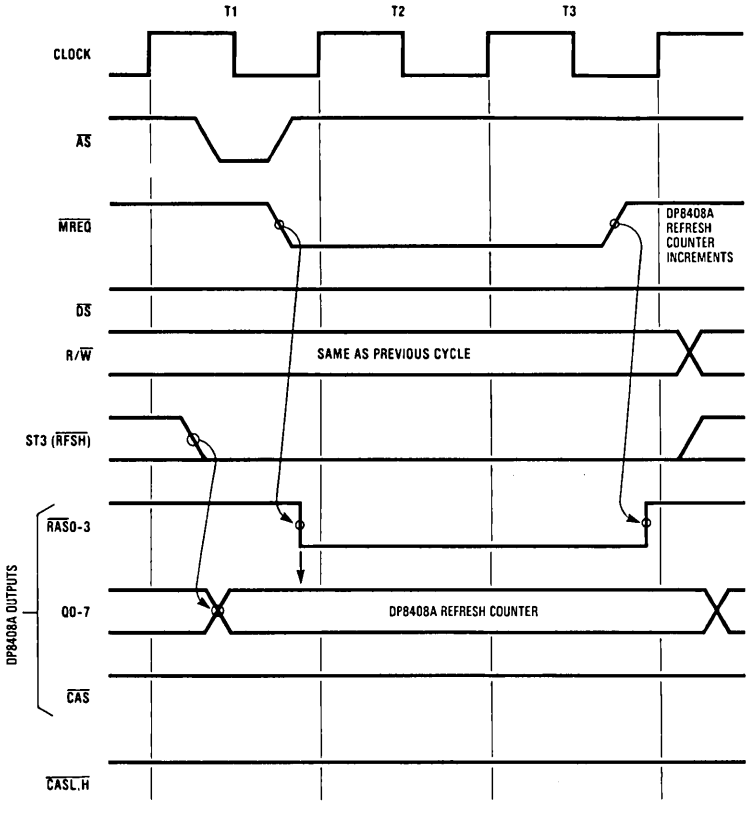

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FIGURE 4. Memory Refresh Cycle

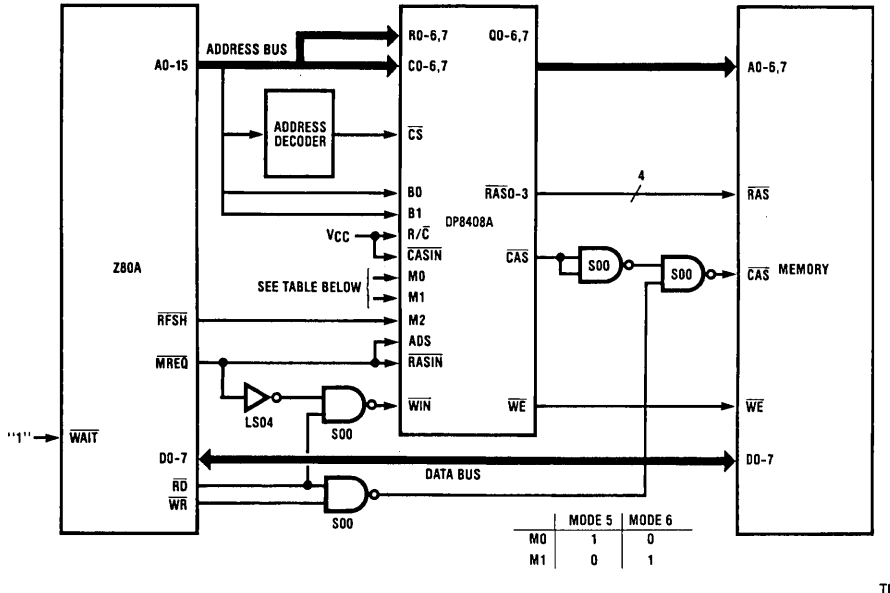

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FIGURE 5. DP8408A and Z80A Interface

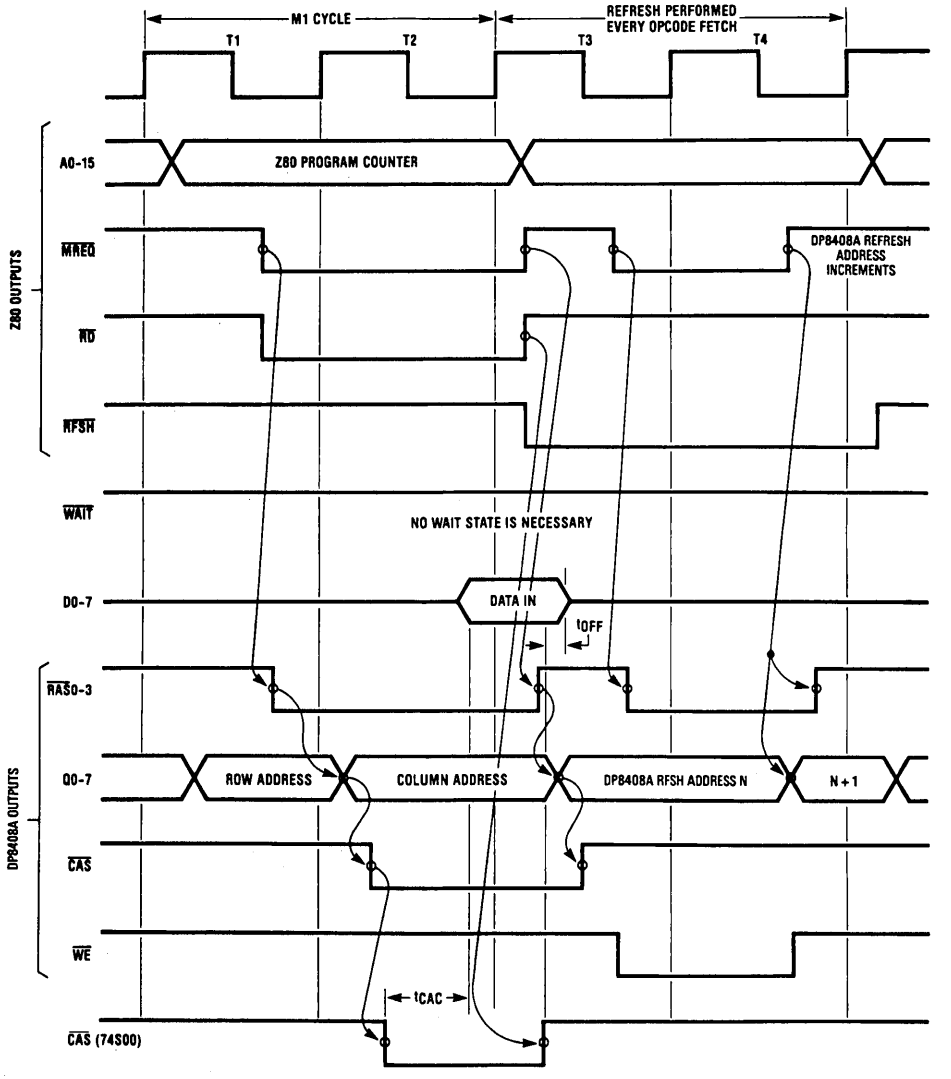

FIGURE 6. Z80A Op Code Fetch Cycle Showing Memory Refresh

MEMORY ACCESS CYCLE

Figure 7 shows the timing of the memory read and memory write cycle other than for the M1 op code fetch cycle. Similar to the op code fetch cycle, $\overline{MREQ}$ is used to provide $\overline{RASIN}$. $\overline{MREQ}$ goes active after the address to the memory has had time to stabilize. Again, $\overline{RAS}$ output, Row to Column Select and then $\overline{CAS}$ output will automatically follow $\overline{RASIN}$ to access the specified memory location. For a memory read cycle, both $\overline{MREQ}$ and $\overline{RD}$ go active, and as a result, $\overline{WIN}$ remains high (refer to *Figure 5*), which allows a memory read operation to occur. On the other hand, only $\overline{MREQ}$ goes active during a write cycle, which forces $\overline{WIN}$ low, indicating an early write cycle. It should be noted that the $\overline{CAS}$ output to the memory array will not go low until $\overline{WR}$ goes low during memory write cycles as this guarantees the valid CPU data will be written into memory.

It is worth mentioning that the Z80 CPU provides powerful block transfer instructions. An example is the LDIR (load, increment and repeat); using only this instruction, the programmer can move any block of data from the location pointed to by the D and E registers. This operation is repeated until the byte counter (B and C registers) reaches zero. Thus, this single instruction can move any block of data from one location to any other. Due to the fact that this instruction is refetched after each data byte transfer, the memory refresh cycle always takes place even though a transfer of up to 64k bytes of data may be performed. Furthermore, when the CPU has executed the software HALT instruction and is waiting for an interrupt before normal CPU operations can resume, the CPU executes NOP instructions to maintain memory refresh activity.

However, care should be taken when the CPU is in either WAIT state or a Bus Acknowledge cycle, the dynamic RAM refresh will not take place. If these conditions occur long enough, a burst refresh is recommended, and it can be done by toggling $\overline{RASIN}$ while keeping M2 low until all the rows of the dynamic RAM have been refreshed before the CPU can resume its operation.

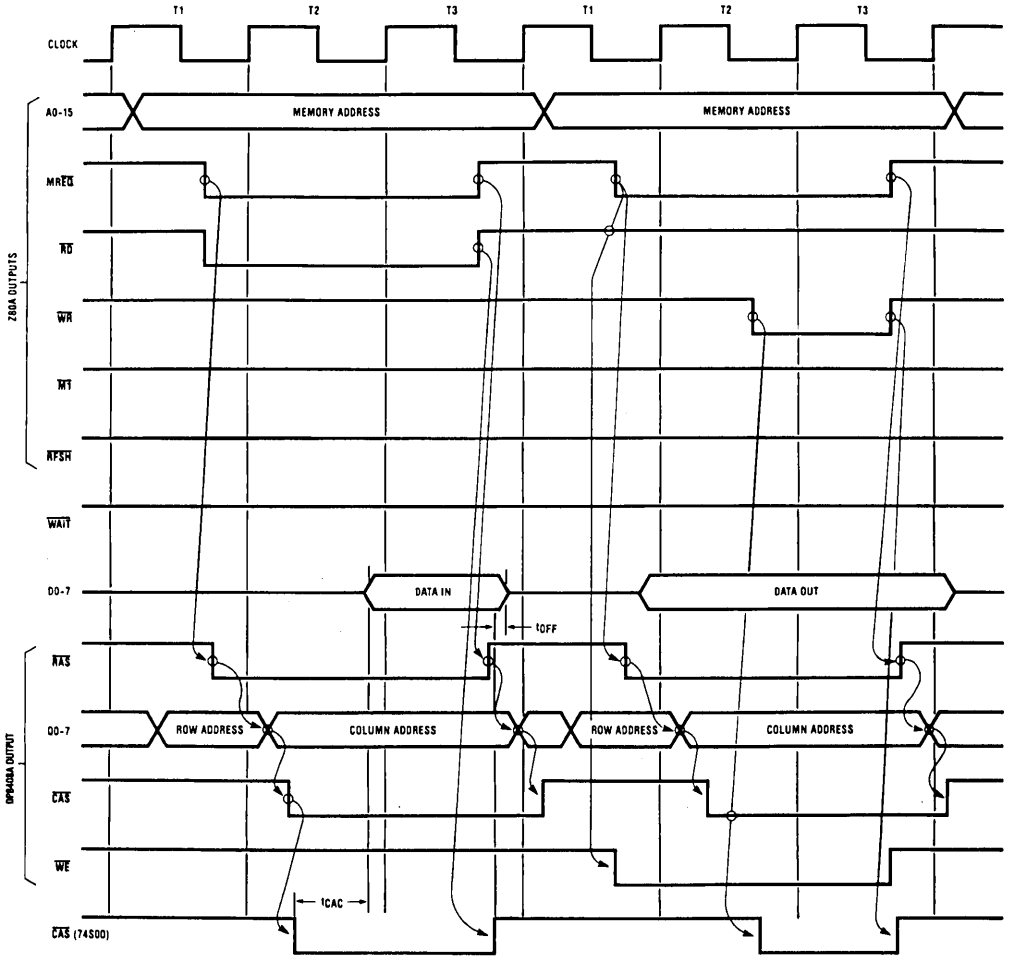

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FIGURE 7. Z80A Memory Read and Memory Write Cycle

The following formulas allow designers to select the appropriate dynamic memory, based on different CPU and DP8408A speed versions, to allow the CPU full speed of operation:

max. t_{CAC}: $1.5 \times t_{Cmin} - t_{DL\phi}(MR) - tRICL - t_{CASDLY} - t_{S\phi}(D)$

min. t_{RP}: $tw(MRH) = tw(\phi H) + t_f - 20$

min. t_{RAS}: $tw(MRL) - 20 = t_C - 50$

Dynamic RAM Parameters:

t_{CAC}: access time from $\overline{CAS}$

t_{RP}: $\overline{RAS}$ precharge time

t_{RAS}: $\overline{RAS}$ pulse width

Z80 Parameters:

t_C: clock period

$tw(\phi H)$: clock pulse width, clock high

tf: clock fall time

$t_{DL\phi}(MR)$: $\overline{MREQ}$ delay from falling edge of clock, $\overline{MREQ}$ low

$t_{S\phi}(D)$: Data set up time to rising edge of clock during M1 cycle

DP8408A and 74S00 Parameters:

t_{RICL}: $\overline{RASIN}$ to $\overline{CAS}$ output delay

t_{CASDLY}: propagation delay of the two 74S00 NAND gates

For example, if the Z80A (4 MHz) and the DP8408A are used, then:

max. t_{CAC}: $1.5(250) - 85 - 132 - 13 - 50 = 95$ ns

min. t_{RP}: $110 + 20 - 20 = 110$ ns

min. t_{RAS}: $t_C - 50 = 200$ ns

t_{RICL} max.

(mode 6): 132 ns at 15 pF load

t_{CASDLY} max.: 13 ns at 50 pF load

Therefore, in this case, the designer should choose a dynamic memory which has maximum t_{CAC} of 95 ns, minimum t_{RP} of 110 ns and minimum t_{RAS} of 200 ns.

DP8409A and MC68B09E Interface

DP8409A OVERVIEW

The DP8409A Dynamic RAM Controller/Driver is designed to control all multiplexed-address dynamic RAMs. It consists of two 9-bit address latches and a 9-bit refresh counter, thus allowing control of all 16k, 64k, and the coming generation 256k dynamic RAMs. More important, all the DP8409A outputs are capable of driving 500 pF loads.

The DP8409A basically has eight modes of operation: Externally Controlled Refresh, Automatic Forced Refresh, Internal Auto Burst Refresh, All $\overline{RAS}$ Auto Write, Externally Controlled Access, Auto Access (slow t_{RAH} and with hidden refresh), Fast Auto Access (fast t_{RAH}) and Set End of Count. Of all these modes, Auto Access (mode 5) and Auto Forced Refresh (mode 1) are the most popular and will be used throughout this application. Mode 5 requires only $\overline{RASIN}$ to initiate a memory access cycle, because all the dynamic RAM's control signals are automatically delayed from this input, as shown in *Figure 1*. To attain maximum system throughput, it is obviously advantageous to perform refreshes without interrupting the system. The DP8409A can do this by monitoring the $\overline{CS}$ input to see if it is high. If $\overline{CS}$ is high, the RAMs are not being accessed. If $\overline{CS}$ is high for one cycle, the DP8409A performs a hidden refresh during this cycle, and stops in time for the system to start another access. But if a hidden refresh does not occur in a specific time slot, a refresh must be forced and this can be done by using Mode 1, Automatic Forced Refresh.

To perform automatic forced refresh, the DP8409A must receive two clock signals: the refresh period clock, RFCK, and RGCK, the $\overline{RAS}$-generator clock; RGCK can be the microprocessor clock. It takes approximately four RGCK clock periods to perform this automatic forced refresh. The DP8409A gives preference to hidden refresh using RFCK as a level reference. The refresh time slot commences as RFCK goes high. If $\overline{CS}$ goes high while RFCK is high, the refresh counter is enabled in the address outputs. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$; so to perform a hidden refresh, $\overline{RASIN}$ must be set low and the refresh counter gets incremented as $\overline{RASIN}$ goes high. The DP8409A allows only one such hidden refresh to occur with a clock cycle of RFCK to minimize power consumption.

If a hidden refresh does not occur the DP8409A must force a refresh before RFCK begins a new cycle on a low-to-high transition. Therefore, as RFCK goes low (and a hidden refresh has not occurred), RF I/O (Refresh Request) goes low, requesting that a refresh be performed. When the system acknowledges the request, it sets M2 low, and prevents further access to the DP8409A. Then two RGCK negative edges after M2 has gone low, all four $\overline{RAS}$ outputs go low and remain low for two RGCK clock periods. After all four $\overline{RAS}$ outputs have gone low, M2 can go high any time to end the Automatic Forced Refresh. The DP8409A allows only one automatic refresh to occur within a clock cycle of RFCK.

MEMORY ACCESS

The MC68B09E starts a memory access cycle when E goes low, then the memory address becomes valid on the Address Bus A0–15. This address is decoded to provide Chip Select ($\overline{CS}$) to the DP8409A. Then Q goes high and sets $\overline{RASIN}$ low from the PAL® Control Logic as shown in *Figure 12*. Note that $\overline{CS}$ must go low for a minimum of 10 ns before the assertion of $\overline{RASIN}$ for a proper memory access. This is important because a false hidden refresh may take place when this 10 ns minimum setup time is not met. $\overline{RASIN}$ goes low initiating the auto access sequence as shown in *Figure 1*. Mode 5 guarantees a 30 ns minimum for row address hold time and a minimum of 8 ns column address set up time. $\overline{RASIN}$ remains low until E goes low at the end of the current access cycle. Using the 16R6A Programmable Array Logic (25 ns PAL), the maximum access time from $\overline{CAS}$ of the selected dynamic RAM is determined as follows:

Max. t_{CAC}: $3 \times 125 - 25 - 160 - 40 = 150$ ns 8409A

t_{CAC}: $3 \times 125 - 25 - 130 - 40 = 180$ ns 8409A-2

Q high to

E low: 3×125 ns (8 MHz clock) $= 375$ ns

Q high to
$\overline{RASIN}$ low: 25 ns (16R6 A PAL Parameter)
$\overline{RASIN}$ to $\overline{CAS}$
Output low: 160 ns (DP8409A's t_{RICL}, Mode 5, at 500 pF load)
130 ns (DP8409A-2's t_{RICL})
Read data setup time (before E going low): 40 ns

MEMORY REFRESH

As described above, $\overline{RASIN}$ goes active when Q and/or E are high. This scheme, therefore, maximizes chances for hidden refresh because $\overline{CS}$ is high during nondynamic memory cycle. For example, when the CPU is executing internal operation or the CPU is accessing ROM or I/O, $\overline{CS}$ is high during these times. The DP8409A therefore performs a hidden refresh as $\overline{RASIN}$ goes low, assuming that RFCK is high.

However, if no hidden refresh occurs while RFCK was high, RF I/O goes low immediately after the RFCK high-to-low transition requests a forced refresh. The PAL Control Logic samples RF I/O, when E and Q are high and low respectively, to set M2 (RFSH) low, as shown in *Figure 13*. Once M2 has gone low, a forced refresh automatically occurs (as described in the DP8409A Overview). M2 remains low for four system clock periods to allow for this forced refresh. If the current microprocessor cycle is a nondynamic memory cycle ($\overline{CS}$ is high), this refresh is transparent to the microprocessor and $\overline{STRETCH}$ remains high (E and Q are not stretched). Nevertheless, if the current cycle is a dynamic memory access cycle, $\overline{STRETCH}$ goes low stretching E and Q for a maximum of four system clocks. $\overline{RASIN}$ for the pending access will be issued a full system clock after M2 has gone high; this is to allow some $\overline{RAS}$ precharge time for the dynamic RAM. After this, memory will be accessed in the manner as described in the Memory Access Cycle.

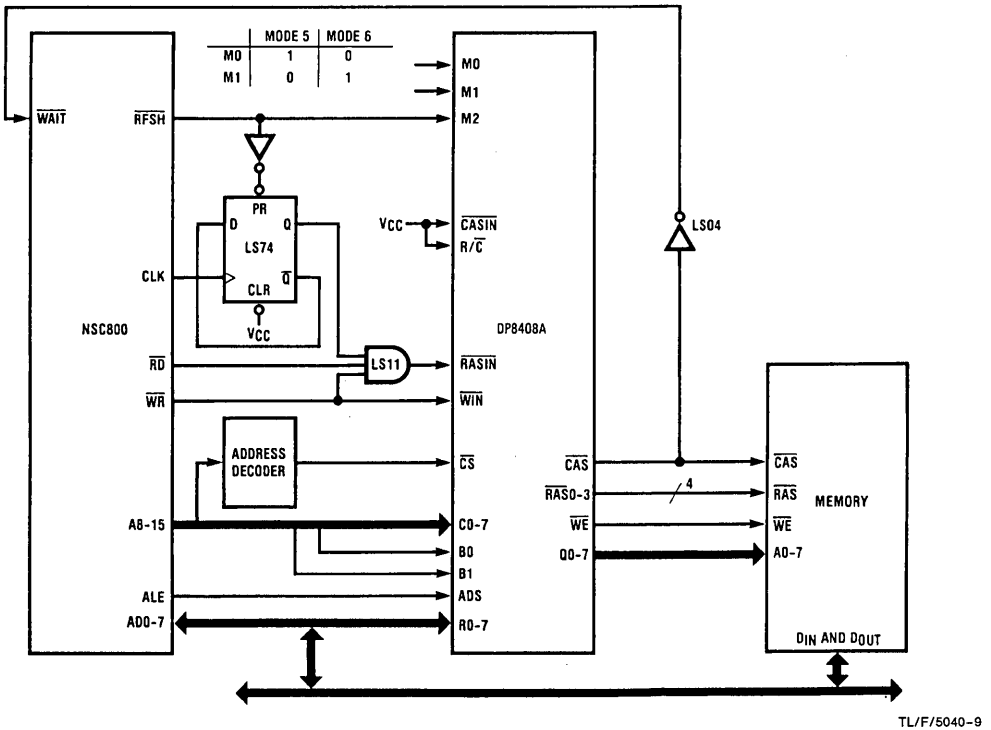

FIGURE 8. NSC800 and DP8408A Interface

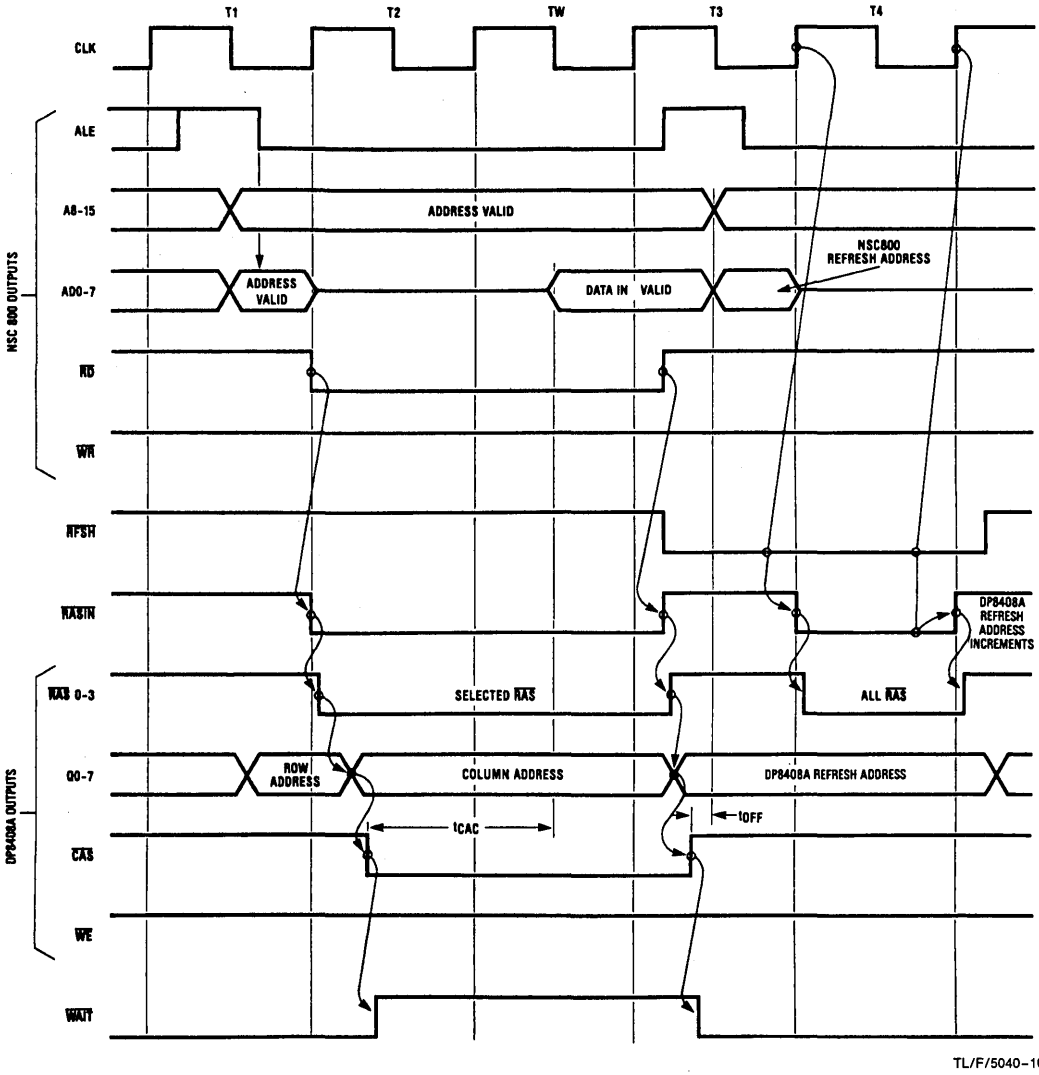

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FIGURE 9. NSC800 Op Code Fetch Cycle Showing Memory Refresh

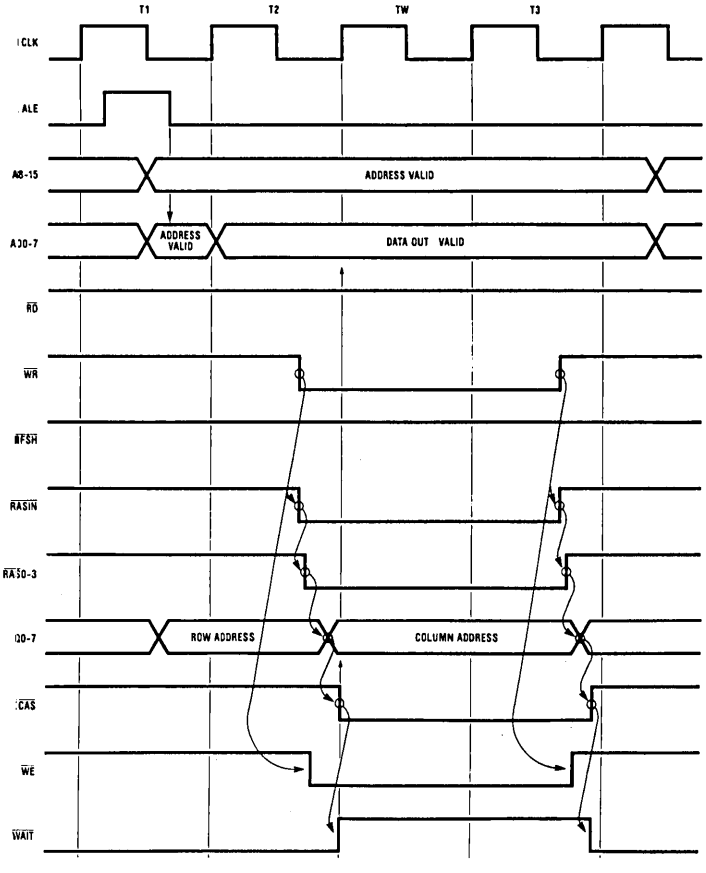

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FIGURE 10. NSC800 Memory Write Cycle

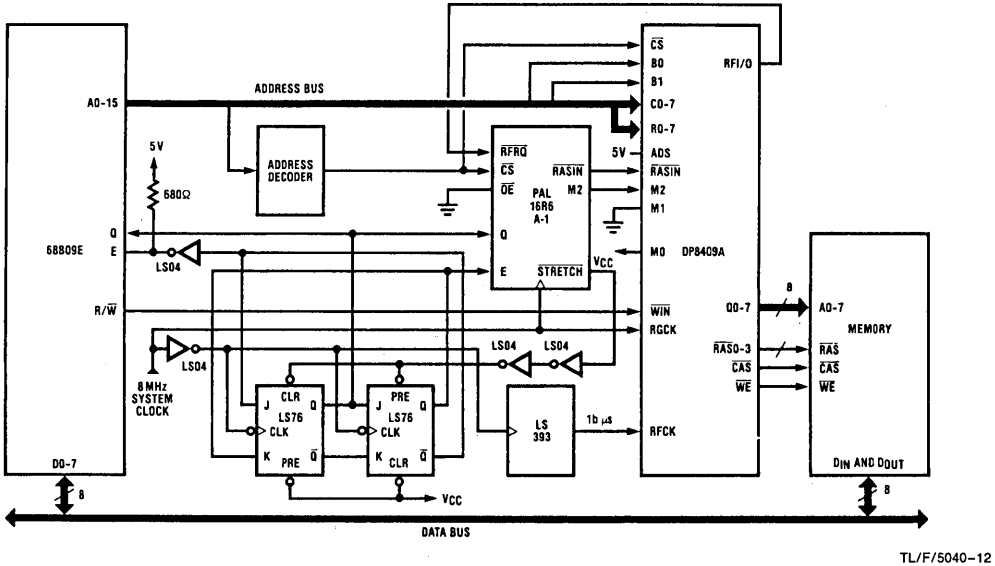

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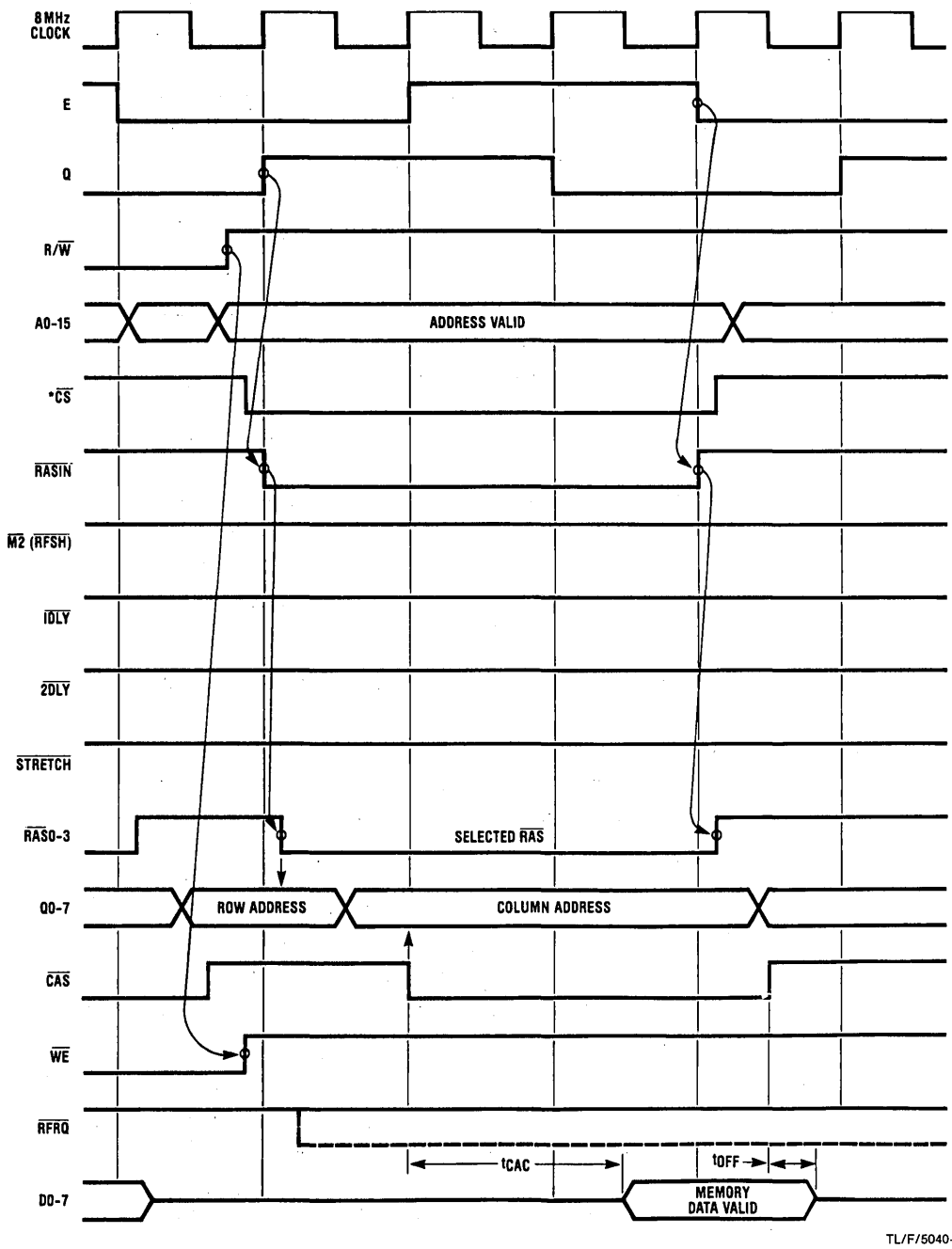
FIGURE 11. MC68B09E and DP8409A Interface



*If CS is high throughout this cycle (RFCK is also high), hidden refresh occurs instead of a memory access.

FIGURE 12. MC68B09E Memory Read Cycle

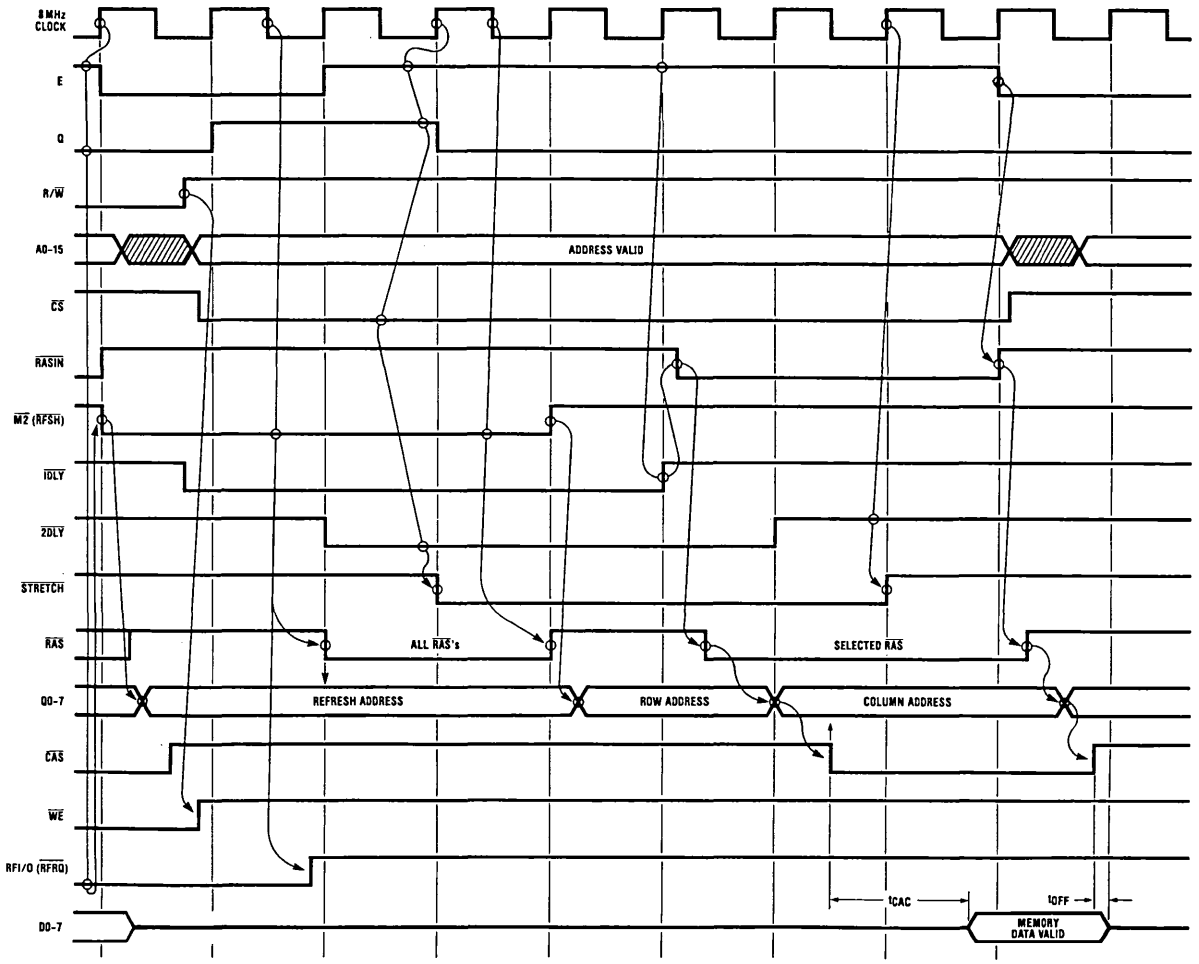


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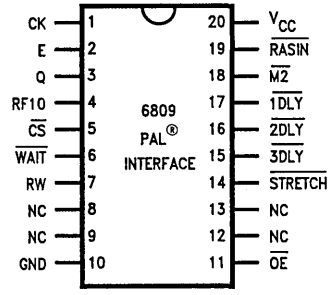
FIGURE 13. MC68B09E Forced Refresh and Memory Read Cycle

```
PAL16R6A
User Part #
6809/8409A Interface PAL
National Semiconductor
CK E Q RFIO /CS /WAIT RW A B GND /OE C D /STRETCH
/3DLY /2DLY /1DLY /M2 /RASIN VCC
If (VCC) RASIN=CS*E*/M2*/1DLY +
               CS*Q*/M2
M2:=E*/RFIO*/Q +
    M2*/3DLY
1DLY:=M2
2DLY:=1DLY
3DLY:=2DLY
STRETCH:=CS*2DLY*E +
         CS*WAIT*E*Q*RW
;DESCRIPTION:
;The above equations are written in standard PALASM™ format.
;Also included in the logic is a ""/WAIT"" (active low) input. This
;input will allow the insertion of one WAIT state in a READ
;access cycle if it is tied low. If WAIT states are wanted in
;both READ and WRITE access cycles the ""RW"" input in the STRETCH
;equation should be deleted.
;The user should make sure that CS is valid at the DP8409A input a
;minimum of 30 ns before RASIN is valid. If the user does not
;care about the HIDDEN REFRESH feature of the DP8409A, CS can be
;tied permanently low. In this configuration the RASIN term can
;transition whenever is convenient.
```

Dual-In-Line Package



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Top View

Dual Port Interface for the DP8417/18/19/28/29 DRAM Controller

National Semiconductor
Application Note 436
Webster (Rusty) B. Meier

INTRODUCTION

This application note describes a general purpose dual port interface to the DP8417/18/19/28/29 DRAM controller. A PAL® (Programmable Array Logic) device is used to implement this interface. The PAL contains the logic necessary to arbitrate between the three ports (Refresh, Port A, and Port B), provide WAIT states to Port A or B when necessary, and an output to multiplex the Port A or B addresses to the DRAM controller.

FEATURES

- Provides a versatile dual port interface to the DP8417/18/19/28/29 DRAM controller
- Provides arbitration circuitry between DRAM refresh cycles, Port A accesses, and Port B accesses
- Allows for Port A and Port B to be synchronous or asynchronous to the input system clock
- Guarantees a minimum of one and one half system clock periods of RAS precharge time between grants to any two ports
- Provides WAIT state logic to both PORT A and Port B to handle contention problems between ports
- Differentiates between READ and WRITE accesses for Port A allowing Port A WRITE accesses to begin later than READ accesses

DESCRIPTION

This hardware arbitrates access to the dynamic RAM controlled by the DP8419 (or any of the related family members: DP8417/18/19/28/29) to either:

1) A Refresh cycle, "$\overline{\text{GRNTRF}}$"

2) Port A, "$\overline{\text{GRNTA}}$"

3) Port B, "$\overline{\text{GRNTB}}$"

Refresh always has the highest priority and will always occur immediately upon a refresh request ($\overline{\text{RFRQ}}$) given that an access by Port A or B is not currently in progress. Port A has a higher priority than Port B though the scheme used attempts to give both ports a more equal priority. The arbiter does this by leaving Port A or Port B granted, after an access by that particular port, as long as no other ports are currently trying to access the DRAM. This scheme is used because data tends to be transferred in bursts from a particular port.

Once a port is granted, subsequent requests by that port immediately access the DRAM, until another port gains access to the DRAM (see *Figure 11* of the timing waveforms for Port A).

The term "$\overline{\text{WINA}}$" (write enable for Port A) is used to cause "$\overline{\text{RASIN}}$" to be generated later for a WRITE access than a READ access. This may be necessary to guarantee that valid data is written to the DRAM during WRITE accesses. If Port B is asynchronous this input is not needed because Port B requests are delayed through the external synchronization circuitry. If Port B is synchronous both ports should mux to the "$\overline{\text{WIN}}$" input, and use this input in generating the "$\overline{\text{RASIN}}$" output of the PAL.

This arbiter guarantees one and one half system clock periods of RAS precharge between accesses of different ports. It is up to the user to guarantee the precharge time between consecutive accesses from the same port. This arbiter assumes a minimum of one period high time between access requests from a particular port.

Hidden Refresh is not supported in any of the following dual port schemes for several reasons:

1) If "$\overline{\text{CS}}$", of the DP8419, is not permanently tied low the user must guarantee a "$\overline{\text{CS}}$-$\overline{\text{RASIN}}$" minimum time of 34 ns for the DP8419. This could slow down the access time of several of the dual port schemes presented.

2) In order to do hidden refresh a port must be granted during a non-$\overline{\text{CS}}$ access cycle. When the port is granted during a non-$\overline{\text{CS}}$ access cycle the other port may be requesting the dual ported memory also and have to wait for it. A possible problem is that the non-$\overline{\text{CS}}$ access may not even be causing a hidden refresh at that time so in essence the other port is being slowed down for no reason (i.e. a hidden or forced refresh may have already been done during that period of the refresh clock).

If either Port A or B tries to access the DRAM during a refresh WAIT states will automatically be inserted into that port's access cycle. Also if one of the ports tries to access the DRAM while the other port is, WAIT states will automatically be inserted into the appropriate port's access cycle. The user may want to change the "$\overline{\text{WAIT}}$" state equations depending upon the processor or bus being interfaced to.

The DUAL PORT ARBITER gives access to the refresh cycle via the M2 ($\overline{\text{RFSH}}$) pin of the DP8419. The $\overline{\text{GRNTB}}$ output of the DUAL PORT CONTROLLER acts as a multiplexor signal to enable either PORT A or PORT B. Once enabled the Port selected will enable its addresses, write enable, $\overline{\text{LOCK}}$ control signal, and data to the DP8419 and its controlled memory. The user must be careful to assure that a particular port will not be locked ("$\overline{\text{LOCK}}$" low while "$\overline{\text{GRNTA}}$ or B" is low) for more than 15.6 μs (RFCK period) or the system may miss a refresh.

The Dual Port scheme presented assumes that all "PORT REQUEST" inputs are synchronous to the system clock input to the PAL (i.e. "PORT REQUESTs" occur following a rising edge of the system clock). If a specific "PORT REQUEST" is asynchronous to the system clock it has to be synchronized to the system clock by running it through two flip-flops (see "AREQB" and "ARFRQ" in the system block diagram). The two "$\overline{\text{RFRQ}}$" synchronizing flip-flops are needed for the PAL refresh logic to work correctly.

The Dual Port scheme presented does not assume the use of any specific processor. Therefore, the user may require some external logic to interface the Dual Port PAL to a specific microprocessor or bus.

Figures 1–5 show several suggestions for circuits used to generate "$\overline{\text{REQA}}$" for different CPU's. The PAL equations were designed assuming a National Semiconductor Series 32000® CPU on Port A. In the "$\overline{\text{RASIN}}$" equations for Port A WRITE cycles were started one half period later than READ

cycles and both READ and WRITE accesses were ended one half period after "$\overline{REQA}$" went high (this is to make up for WRITE accesses starting one half period after "$\overline{REQA}$"). The user may wish to modify these equations (and possibly the "$\overline{WAITA}$" equations) depending upon the specific CPU being used.

EXAMPLE: DETERMINING THE REQUIRED MEMORY SPEED ("t_{RAC}" AND "t_{CAC}") FOR A SERIES 32000 TO RUN AT 10 MHz WITHOUT WAIT STATES

Assume the Series 32000 is synchronously interfaced to Port A.

#1) $\overline{RASIN}$ low = T1 + 6 ns (PHI1 to CTTL Rising edge maximum) + 12 ns ("B" PAL clocked output) + 15 ns ("B" PAL combinational output) = 100 + 6 + 12 + 15 = 133 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 70 ns (DP8419-70) − 3 ns (72 DRAMs instead of 88 DRAMs spec'd in data sheet) = 67 ns maximum

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" clock cycle = 15 ns maximum

"t_{RAC}" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 100 + 100 + 100 − 133 ns − 20 − 7 − 15 = 125 ns

"t_{CAC}" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 100 + 100 + 100 − 133 ns − 67 − 7 − 15 = 78 ns

Therefore the DRAM chosen should have a "t_{RAC}" less than or equal to 125 ns and a "t_{CAC}" less than or equal to 78 ns. Standard 120 ns DRAMs meet this criteria.

The following is an example of how to interpret the PAL equations correctly. These equations are presented in the format specified by the National Semiconductor PLAN format. CAUTION, this format differs from the much used PALASM format.

EXAMPLE: $\overline{GRNTRF}$:= $\overline{RFRQ}$*GRNTA*$\overline{GRNTB}$

This reads, the active low flip-flop output "$\overline{GRNTRF}$" is low following the rising edge of the input clock given that, the active low input "$\overline{RFRQ}$" is low AND the active low output "$\overline{GRNTA}$" is high AND the active low output "$\overline{GRNTB}$" is high a setup time before the input clock transitions high. (Notice that $\overline{RFRQ}$ is interpreted as being low.)

POSSIBLE MODIFICATIONS TO THIS APPLICATION

In this application "$\overline{REQB}$" is synchronized to the falling edge of the system clock input of the PAL. Generating "$\overline{REQB}$" from the falling clock edge allows minimum delay from the asynchronous request to the synchronized request producing "$\overline{GRNTB}$" and or "$\overline{RASIN}$". Producing "$\overline{REQB}$" in this way also delays "$\overline{RASIN}$" during a port B access because of the effect of the "$\overline{GTOA}$" term. In order to calculate the t_{RAC} and t_{CAC} of the DRAM (see Series 32000 example above) the delay to "$\overline{RASIN}$" low would be: "$\overline{AREQB}$" low (asynchronous request B) + SYNCHRONIZATION delay (2 flip-flops) + 3 input NAND gate delay of "$\overline{GTOA}$" + PAL delay for "$\overline{RASIN}$".

If "$\overline{REQB}$" is synchronized to the rising edge of the system clock there is a potential danger of getting glitches on the "$\overline{RASIN}$" output of the PAL as a result of the "$\overline{GTOA,B}$" terms. The glitches are possible under the condition of both "$\overline{REQA}$" and "$\overline{REQB}$" going low during a single clock period. For example, if Port B is currently granted ("$\overline{GRNTB}$" low) and "$\overline{REQA}$" goes low more than one inverter gate delay before "$\overline{REQB}$" goes low the "$\overline{GTOA}$" term will initially be high, then go low, then back high. This could cause a small glitch at the beginning of "$\overline{RASIN}$". This glitch can be avoided by guaranteeing that either the requests are separated by at least a three input NAND gate delay (as is the case in this application note) or that when two requests happen within one clock period they happen within one inverter gate delay of each other. The circuits shown below, in *Figure 1*, could be used to guarantee that when two requests happen within one clock they occur within one gate delay of each other.

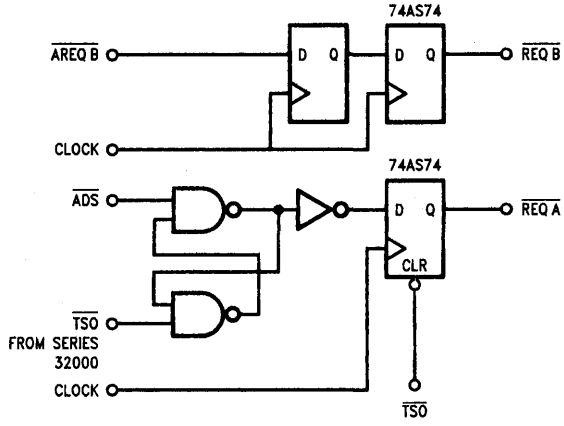

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FIGURE 1. Alternative Request Generating Circuits

IDEAS ON GENERATING "$\overline{\text{REQA}}$" FOR SEVERAL DIFFERENT MICROPROCESSORS.

*$\overline{\text{REQA}}$, $\overline{\text{REQB}}$, $\overline{\text{RFRQ}}$ should have a minimum setup time of approximately 20 ns before the rising edge of the system clock.

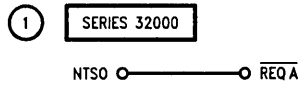

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FIGURE 2. Series 32000 "$\overline{\text{REQA}}$"

Minimum of 2 periods $\overline{\text{RAS}}$ precharge between successive accesses.

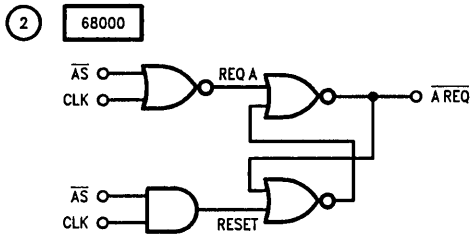

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FIGURE 3. 68000 "$\overline{\text{REQA}}$"

Minimum of 1½ periods of $\overline{\text{RAS}}$ precharge.

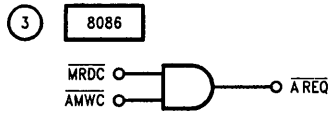

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FIGURE 4. 8086 "$\overline{\text{REQA}}$" Method #1

Minimum of 2 periods of $\overline{\text{RAS}}$ precharge.

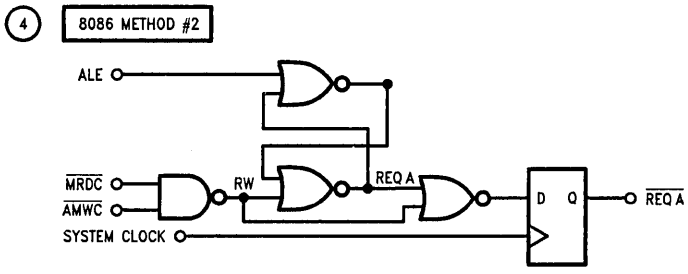

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FIGURE 5. 8086 "$\overline{\text{REQA}}$" Method #2

(For faster speed, minimum of 1 period of $\overline{\text{RAS}}$ precharge.)

DUAL PORT PAL #1 INPUTS

1) "CLOCK" System clock.
2) "$\overline{\text{REQA}}$" A synchronous access request from Port A.
3) "$\overline{\text{WINA}}$" WRITE ENABLE from Port A. This input is used to delay "$\overline{\text{RASIN}}$" during WRITE accesses.
4) "$\overline{\text{REQB}}$" A synchronous chip selected access request form Port B. "$\overline{\text{AREQB}}$" is run through two flip-flops to get "$\overline{\text{REQB}}$". Chip Select for Port B is assumed to be included within this input.
5) "$\overline{\text{RFRQ}}$" A synchronous refresh request.
6) "$\overline{\text{LOCK}}$" The "$\overline{\text{LOCK}}$" input is an active low signal that is driven by either Port A or Port B. This input, when low, causes the arbiter to keep the currently granted Port granted until the "$\overline{\text{LOCK}}$" input goes high. This input is useful in implementing atomic operations such as semaphores that are useful in multiuser/multitasking operating systems.
7) "$\overline{\text{GTOA}}$" This input is generated externally using the three signals $\overline{\text{REQA}}$, $\overline{\text{REQB}}$, and $\overline{\text{LOCK}}$ with some discrete logic. This input indicates that the arbiter will switch to Port A, given that Port B is currently granted. This input is needed to guarantee that when the arbiter switches control of the DRAM from Port B to Port A that $\overline{\text{GRNTB}}$ goes invalid before $\overline{\text{REQB}}$ is able to start another access (see the $\overline{\text{RASIN}}$ output term "PORTB RASIN" in PAL equations).

8) "GTOB" This input is generated externally using the three signals REQA, REQB, and LOCK with some discrete logic. This input indicates that the arbiter will switch to Port B given that Port A is currently granted. This input is needed to guarantee that when the arbiter switches control of the DRAM from Port A to Port B that GRNTA goes invalid before REQA is able to start another access (see the RASIN output term "PORTA RASIN" in PAL equations).
9) "CLK" This is the system clock input that may be used in the PAL equations (i.e. "WAIT").
10) "CSA" This input is the chip select input for Port A. It is used, along with "REQA", to request and cause an access to the DRAM.

DUAL PORT PAL #1, OUTPUTS

NOTE: All outputs are active low.

1) "RASIN" This is the RASIN input to the DP8419 for Port A, Port B, and refresh.
2) "GRNTA" This output is the grant output for Port A.
3) "GRNTB" This output functions as the grant output for both Port A (high) and Port B (low).
4) "GRNTRF" Goes to DP8419 M2 (RFSH) input. This causes an automatic forced refresh cycle.
5) "GRNT1D" Goes low one period after "GRNTA", "GRNTB", or "GRNTRF" go low. This output is used to guarantee that one period is allowed after arbitration before a "RASIN" is generated during a port access. This allows the particular port's address, write enable signal, and lock input to become valid before an access is started. This output also allows the PAL to determine when a particular port has been granted for several system clock periods. This information allows the arbiter to immediately generate "RASIN" for any subsequent memory accesses since the address is already muxed to the DRAM controller (see *Figure 11* for the timing waveforms for Port A).
6) "WAITA" This output functions as a WAIT input for Port A.
7) "GTORFSH" This input is generated internally and indicates that the arbiter will give access control over to the refresh Port at the next rising clock edge.
8) "XACKB" This output is generated external to the PAL and functions as a transfer acknowledge for Port B.

```
DUAL PORT PAL #1
PAL16R4B

CLOCK  /REQA  /WINA  /REQB  /RFRQ  /LOCK  /GTOA  /GTOB  CLK  GND
/OE  /CSA  /WAITA  /GRNT1D  /GRNTRF  /GRNTB  /GRNTA  /RASIN  /GTORFSH  VCC

/GRNTA  := /CSA*/REQA*GRNTRF*RFRQ*GRNTB          ;Start GRNTA
           +/LOCK*/GRNTA                         ;Continue GRNTA
           +/CSA*/REQA*RFRQ*/GRNTRF*GRNT1D       ;RFSH_TO_PORTA
           +/CSA*/GTOA*/*GRNTB*RFRQ*RASIN        ;PORTB_TO_PORTA
           +/CSA*/REQA*/GRNTA                    ;Hold GRNTA
           +/GRNTA*REQB*RFRQ                     ;Hold GRNTA

/GRNTB  := REQA*GRNTA*RFRQ*GRNTRF*/REQB          ;Start GRNTB
           +/LOCK*/GRNTB                         ;Continue GRNTB
           +/GTOB*/GRNTA*RFRQ*RASIN              ;PORTA_TO_PORTB
           +REQA*RFRQ*/GRNTRF*/REQB*GRNT1D       ;RFSH_TO_PORTB
           +/REQB*/GRNTB                         ;Hold GRNTB
           +/GRNTB*REQA*RFRQ                     ;Hold GRNTB
           +/GRNTB*CSA*RFRQ                      ;Hold GRNTB

/GRNTRF := GRNTA*GRNTB*/RFRQ                     ;Start GRNTRF
           +/GRNTRF*/RFRQ                        ;Continue GRNTRF
           +REQA*/GRNTA*LOCK*/RFRQ               ;PORTA_TO_RFSH
           +REQB*/GRNTB*LOCK*/RFRQ               ;PORTB_TO_RFSH
           +/GRNTRF*/GRNT1D                      ;Hold GRNTRF

/GRNT1D := /GRNTA*GTOB*GTORFSH                   ;GRNT1D for PORTA
           +/GRNTB*GTOA*GTORFSH                  ;GRNT1D for PORTB
           +/GRNTRF*/RFRQ                        ;GRNT1D for RFSH

IF (VCC) /GTORFSH =
         REQA*/GRNTA*LOCK*/RFRQ                  ;PORTA_TO_RFSH
         +REQB*/GRNTB*LOCK*/RFRQ                 ;PORTB_TO_RFSH
```

```
DUAL PORT PAL #1,
PAL16R4B (Continued)
IF (VCC) /RASIN =
/CSA*/REQA*/GRNTA*/GRNT1D*GTOB*GTORFSH*WINA          ;PORTA READ RASIN
+/CSA*/REQA*/GRNTA*/GRNT1D*GTOB*GTORFSH*/WINA*/CLK   ;PORTA WRITE RASIN
+/CSA*/REQA*/GRNTA*/GRNT1D*GTOB*GTORFSH*/WINA*/RASIN ;PORTA WRITE RASIN
+/GRNTA*/GRNT1D*/RASIN*CLK                          ;Hold PORTA RASIN
+/REQB*/GRNTB*/GRNT1D*GTOA*GTORFSH                  ;PORTB RASIN
+/GRNTRF*/GRNT1D*GTORFSH                            ;RFSH RASIN

IF (VCC) /WAITA = /CSA*/REQA*GRNTA                 ;Start WAITA
        +/CSA*/REQA*/WAITA*CLK                     ;WAIT until one half period after GRNTA
```

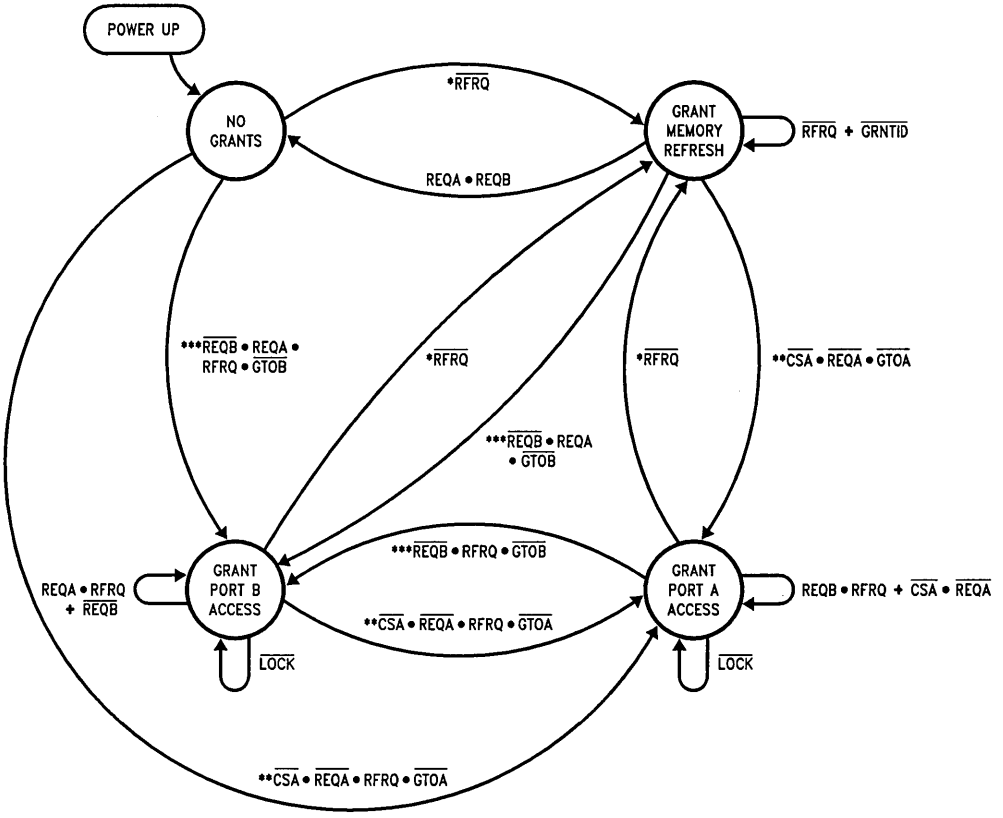

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FIGURE 6. Dual Port State Diagram

*Refresh has the highest priority
**Port A has the second highest priority
***Port B has the lowest priority

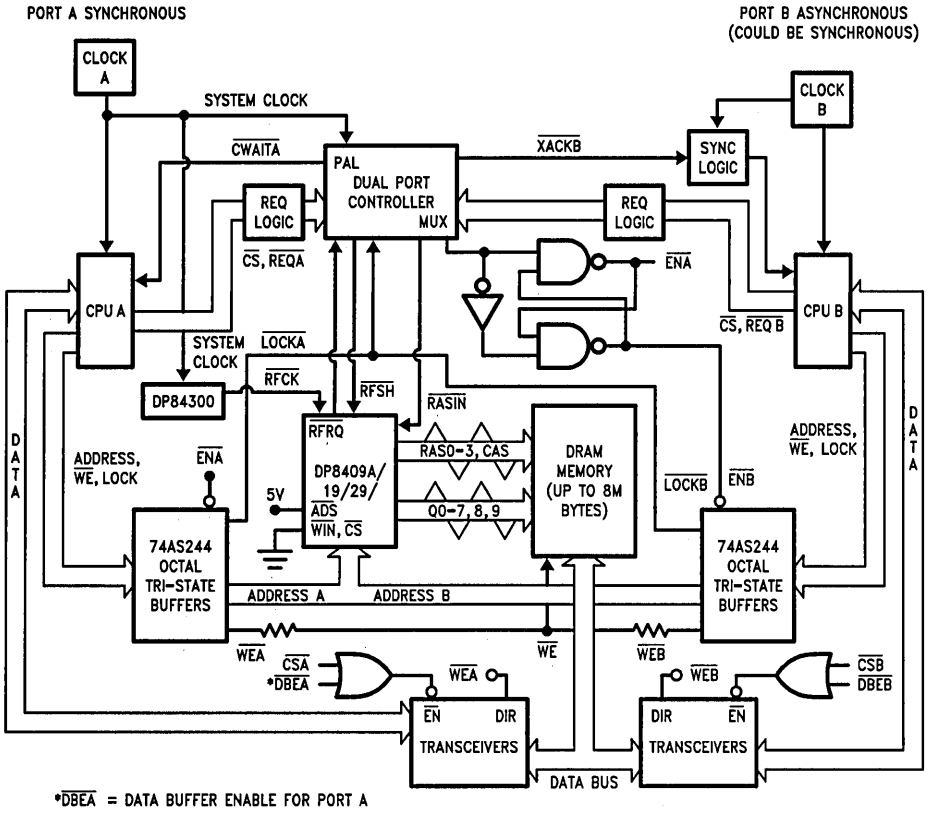

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FIGURE 7. Dual Port Interface

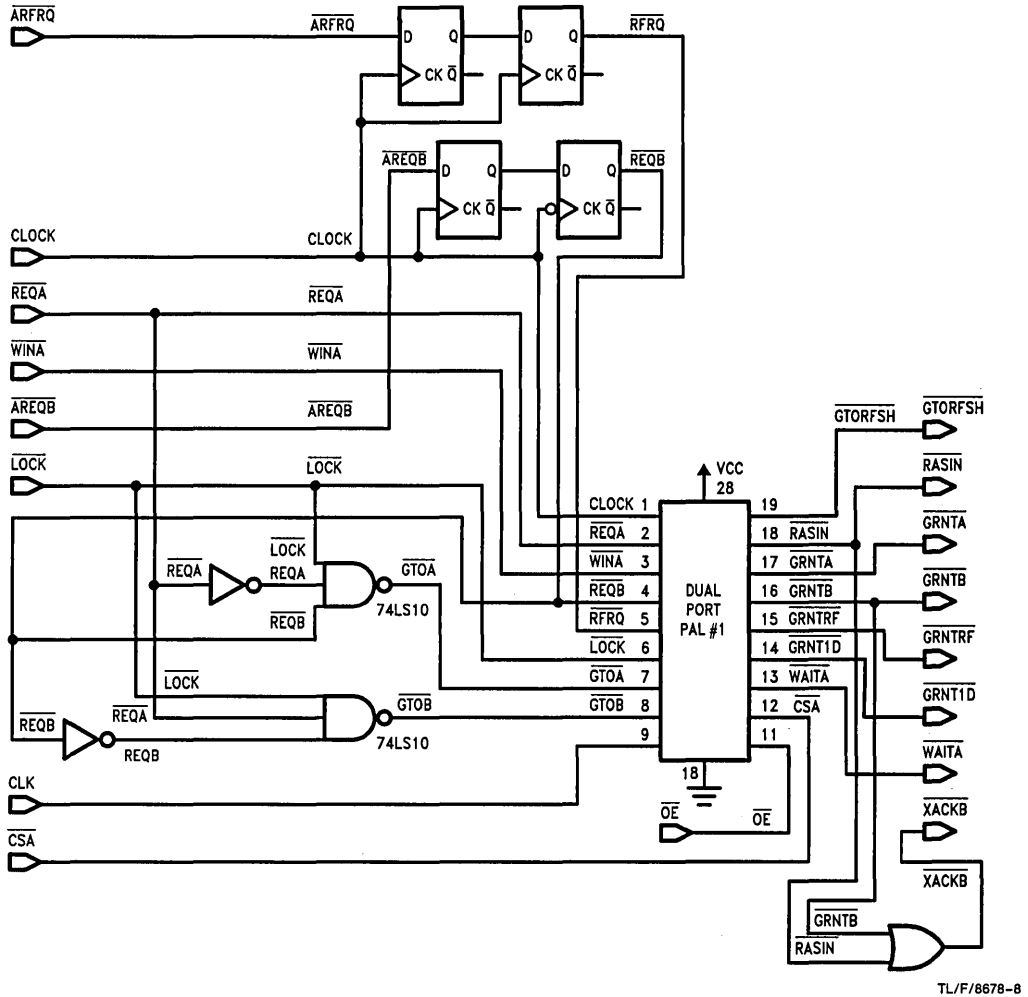

FIGURE 8. Dual Port PAL Controller Diagram

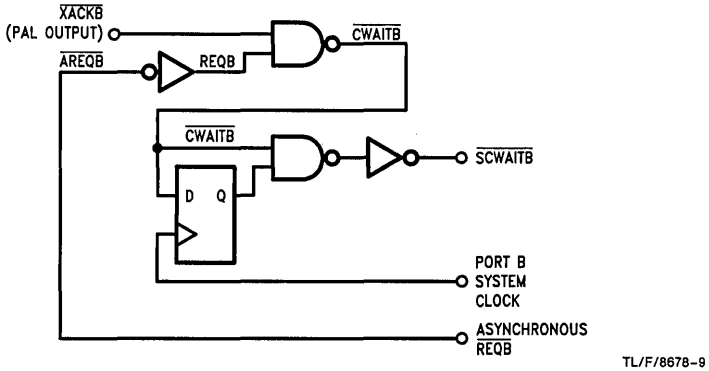

FIGURE 9. Asynchronous Port B transfer acknowledge ("XACKB") synchronizes circuit to produce "CWAITB" synchronous with the Port B clock "CTTL" ("SCWAITB")

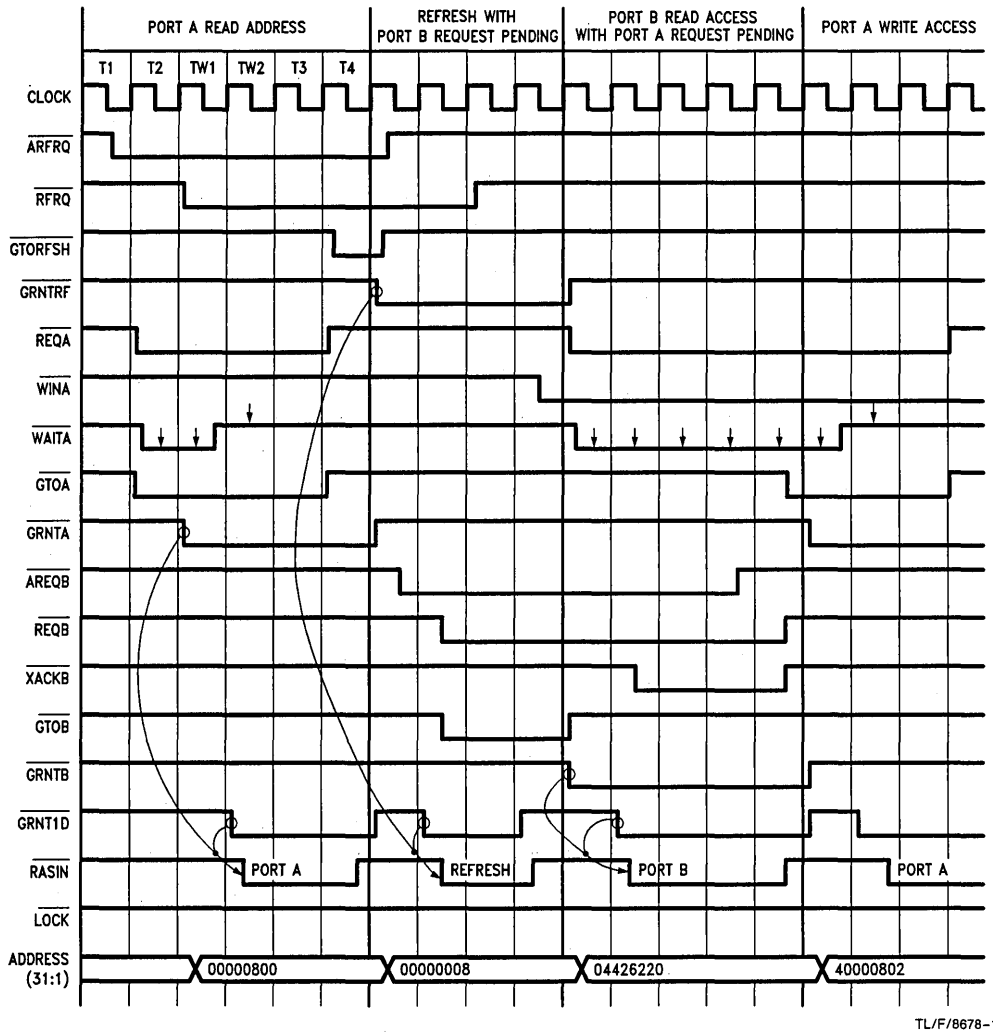

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FIGURE 10. Dual Port Timing

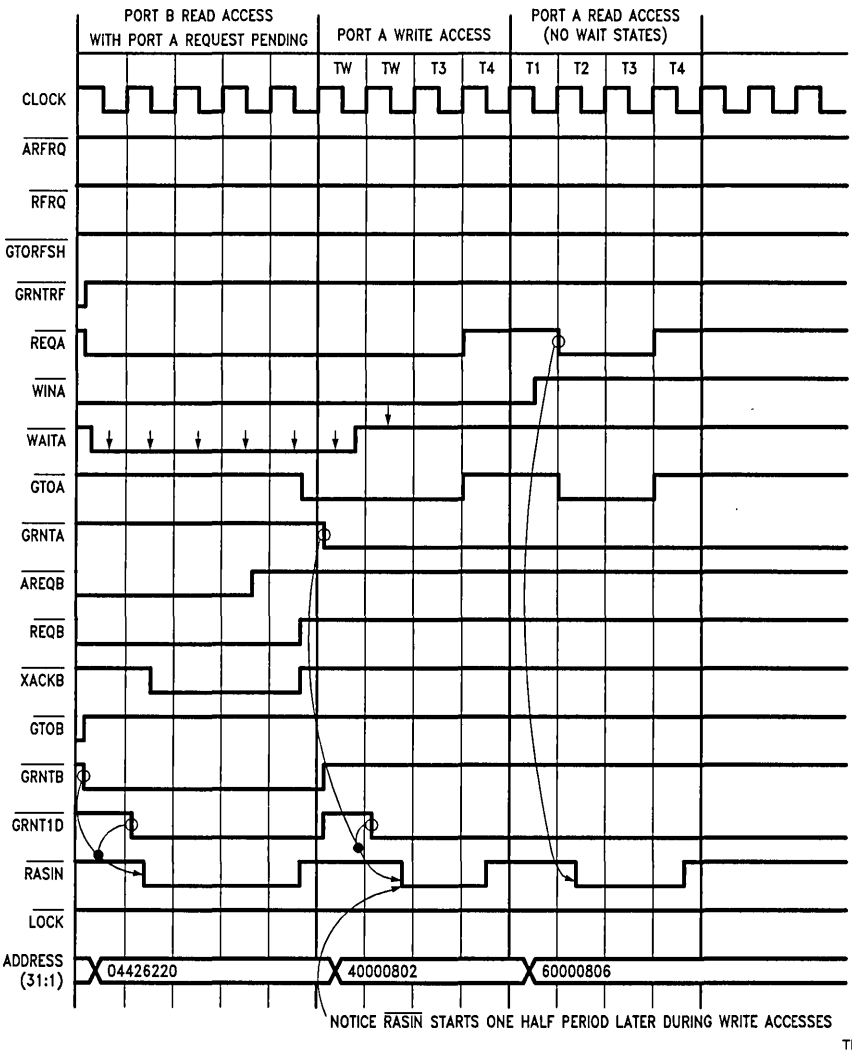

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FIGURE 11. Dual Port Timing

Section 4

Memory Drivers and Support

Section Contents

National Semiconductor Corporation

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

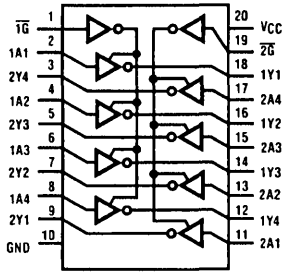
General Description

The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250 pF and 500 pF load capacitances.

Features

- t_{pd} specified with 250 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

Connection Diagram



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Top View

Order Number DP84240J or DP84240N
See NS Package Numbers J20A or N20A

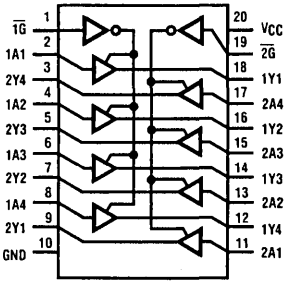
Truth Table

DP84240

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244



TL/F/5219–2

Top View

Order Number DP84244J or DP84244N
See NS Package Numbers J20A or N20A

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	L
L	H	H

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Cavity Package	1150 mW
Molded Package	1300 mW
Lead Temperature (soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C. (Notes 2 and 3.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 2.7V		0.1	20	μA
		V_{IN} = 7.0V			100	μA
$I_{IN(0)}$	Logical "0" Input Current	0 ≤ V_{IN} ≤ 0.4V		−50	−200	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −18 mA		−1	−1.2	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100 μA I_{OH} = −1 mA	V_{CC}−1.15 V_{CC} −1.5	4.3 3.9		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 10 μA I_{OL} = 12 mA		0.2 0.3	0.4 0.5	V
I_{1D}	Logical "1" Drive Current	V_{OUT} = 1.5V	−75	−250		mA
I_{0D}	Logical "0" Drive Current	V_{OUT} = 1.5V	+100	+150		mA
Hi-Z	TRI-STATE Output Current	0.4V ≤ V_{OUT} ≤ 2.7V	−100		+100	μA
I_{CC}	Supply Current DP84240	All Outputs Open All Outputs High All Outputs Low All Outputs Hi-Z		 16 74 80	 50 125 125	mA
	DP84244	All Outputs High All Outputs Low All Outputs Hi-Z		40 100 115	75 130 150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

Switching Characteristics V_{CC} = 5V ±10%, 0 ≤ T_A ≤ 70°C, all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (Note 3.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay from LOW-to-HIGH Output	*Figures 1 & 3*	C_L = 250 pF C_L = 500 pF	9 10	16 20	27 33	ns
t_{PHL}	Propagation Delay from HIGH-to-LOW Output		C_L = 250 pF C_L = 500 pF	9 12	16 20	25 31	ns
t_{PLZ}	Output Disable Time from LOW	*Figures 2 & 4*, S = 1, C_L = 50 pF			11	24	ns
t_{PHZ}	Output Disable Time from HIGH	*Figures 2 & 4*, S = 2, C_L = 50 pF			12	24	ns
t_{PZL}	Output Enable Time to LOW	*Figures 2 & 4*, S = 1, C_L = 500 pF			30	45	ns
t_{PZH}	Output Enable Time to HIGH	*Figures 2 & 4*, S = 2, C_L = 500 pF			23	35	ns
t_{SKEW}	Output-to-Output Skew (Note 4)	*Figures 1 & 3*, C_L = 500 pF			3		ns

Capacitance T_A = 25°C, f = 1 MHz, V_{CC} = 5V ±10%. (Note 3.)

Parameter	Conditions	Typ	Units
C_{IN}	All Other Inputs Tied Low	6	pF
C_{OUT}	Output in TRI-STATE Mode	20	pF

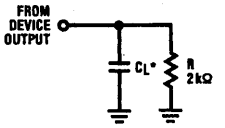
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T_A = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

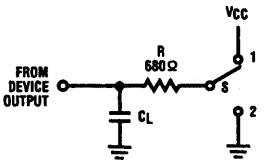
Switching Test Circuits



TL/F/5219–3

*C_L INCLUDES PROBE AND JIG CAPACITANCES

FIGURE 1. Capacitive Load Switching

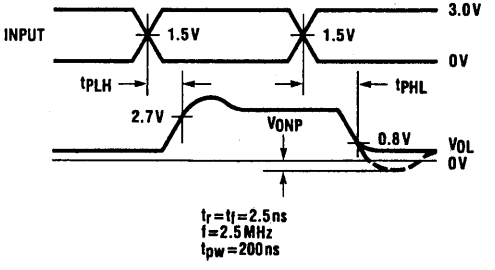


TL/F/5219–4

FIGURE 2. TRI-STATE Enable/Disable

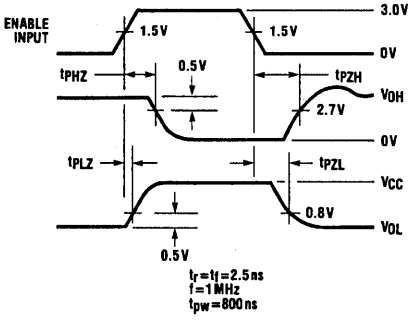
Typical Switching Characteristics

Voltage Waveforms



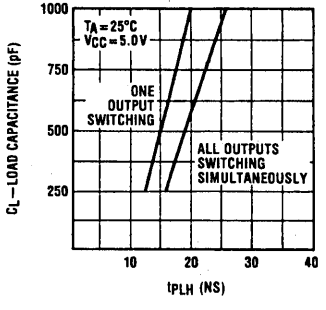
TL/F/5219–5

FIGURE 3. Output Drive Levels



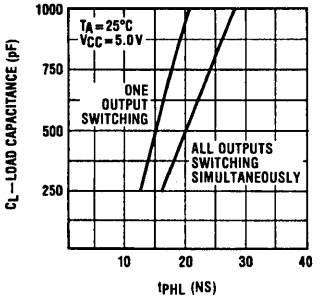
TL/F/5219–6

FIGURE 4. TRI-STATE Control Levels



TL/F/5219–7

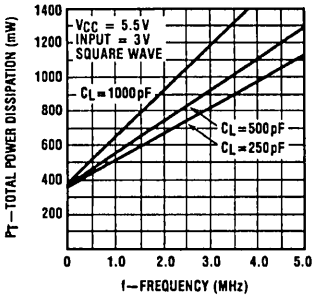
FIGURE 5. t_{PLH} Measured to 2.7V on Output vs. C_L



TL/F/5219–8

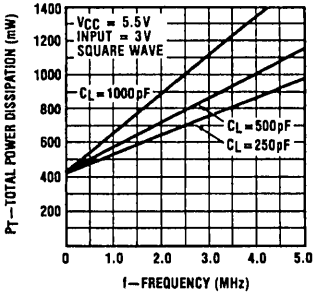
FIGURE 6. t_{PHL} Measured to 0.8V on Output vs. C_L

Typical Switching Characteristics (Continued)



TL/F/5219–9

FIGURE 7. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

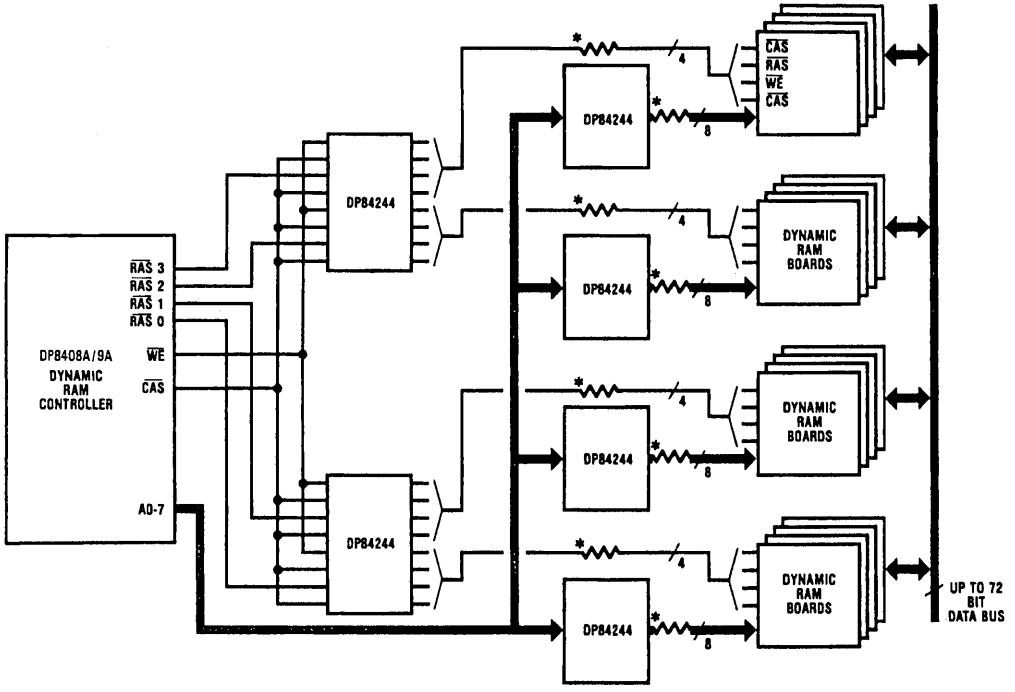


TL/F/5219–10

FIGURE 8. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

Typical Application

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)



TL/F/5219–11

National Semiconductor Corporation

PRELIMINARY

DS0025C Two Phase MOS Clock Driver

General Description

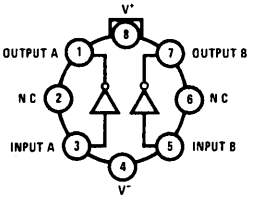
The DS0025C is a monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL line drivers or buffers such as the DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse width may be set by selection of the input capacitor eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead or 14-lead dual-in-line package
- High Output Voltage Swings—up to 25V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DS8830, DM7440
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package



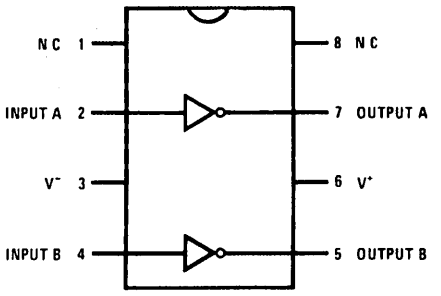
TL/F/5852–1

Note: Pin 4 connected to case.

Top View

Order Number DS0025CH
See NS Package Number H08C

Dual-In-Line Package

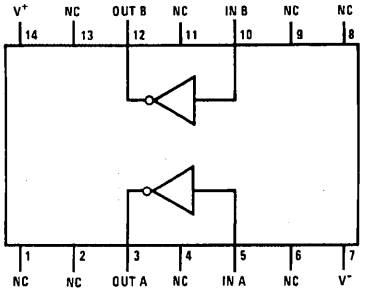


TL/F/5852–2

Top View

Order Number DS0025CJ-8
or DS0025CN
See NS Package Number J08A or N08E

Dual-In-Line Package



TL/F/5852–3

Top View

Order Number DS0025CJ
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

$(V^+ - V^-)$Voltage Differential	25V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Recommended Operating Conditions

V^+ V^- Differential Voltage 20V

	Min	Max
Temperature	0	70

Maximum Power Dissipation* at 25°C

8-Pin Cavity Package	1150 mW
14-Pin Cavity Package	1410 mW
Molded Package	1080 mW
Metal Can (TO-5) Package	670 mW

* Derate 8-pin cavity package 7.8 mW/°C above 25°C; derate 14-pin cavity package 9.5 mW/°C above 25°C; derate molded package 8.7 mW/°C above 25°C; derate metal can (TO-5) package 4.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) See test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{d\,ON}$	Turn-On Delay Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF			25	50	ns
$t_{d\,OFF}$	Turn-Off Delay Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF	(Note 4)	60	90	120	ns
			(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA		$V^+ - 1.0$	$V^+ - 0.7V$		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			$V^- + 0.7V$	$V^- + 1.5V$	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

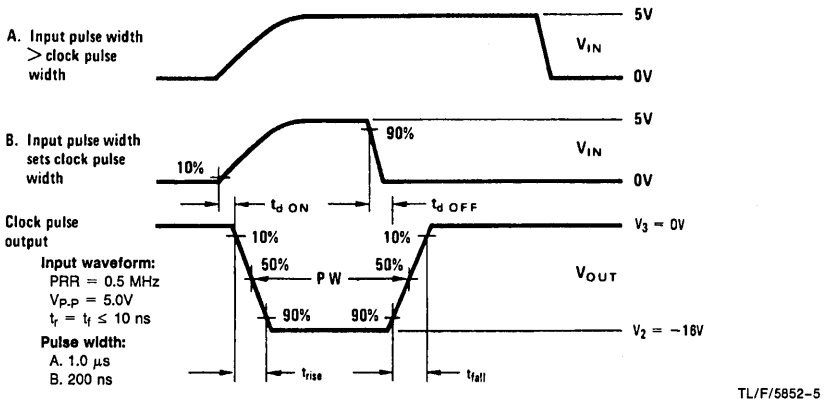
Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C range for the DS0025C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

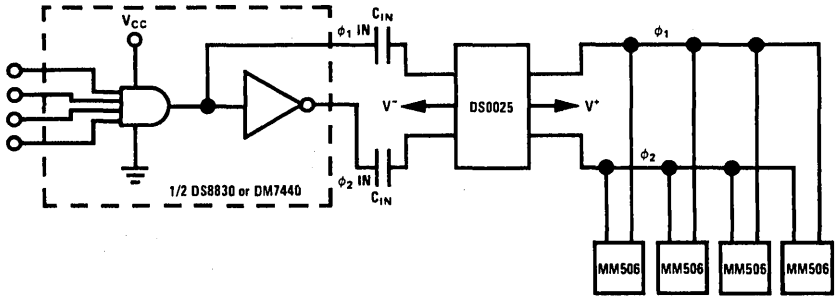
Note 5: Parameter values for input width greater than output clock pulse width.

Timing Diagram



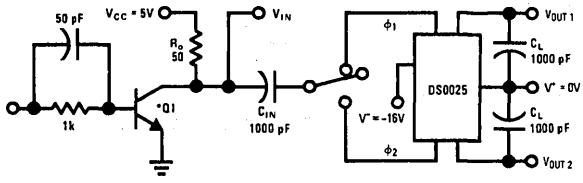
TL/F/5852–5

Typical Application



TL/F/5852-4

AC Test Circuit

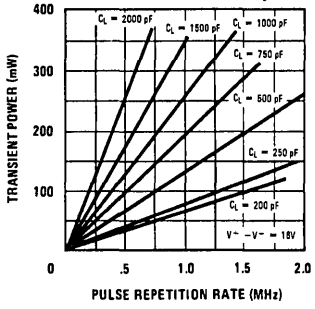


TL/F/5852-6

*Q1 is selected high speed NPN switching transistor.

Typical Performance

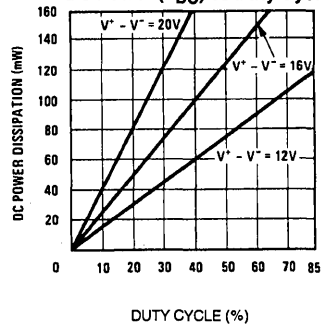
Transient Power vs Rep. Rate



TL/F/5852-7

$P_{AC} = (V^+ - V^-)^2 f C_L$

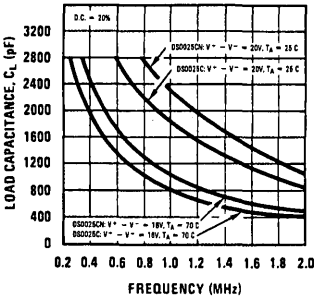
DC Power (P_{DC}) vs Duty Cycle



TL/F/5852-8

$$P_{DC} = \frac{V^+ - V^-)^2 (DC)}{1k}$$

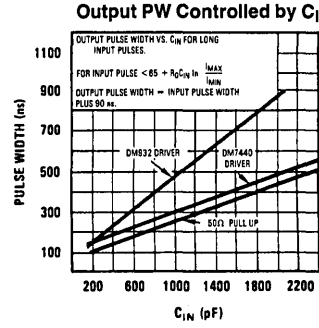
Maximum Load Capacitance



TL/F/5852-9

$$C_L < \frac{(P_{MAX})\ (1k) - (V^+ - V^-)^2\ (DC)}{(f)\ (1k)\ (V^+ - V^-)^2} < \frac{(I_{pk})\ (t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



TL/F/5852-10

I_{MAX} = Peak Current delivered by driver

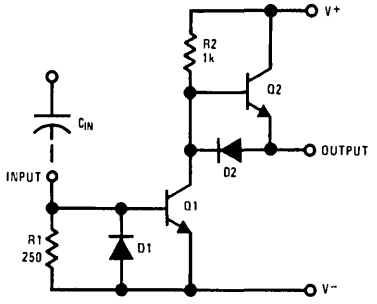
$$I_{MIN} \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

Applications Information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.



TL/F/5852–11

FIGURE 1. DS0025 Schematic (One-Half Circuit)

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns. For $V^+ - V^- = 20V$, $I = 0.8A$.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

$= 80$ mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power.

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30–50 ns and 16V amplitude over the temperature range 0°–70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power.

385 mW = transient output power.

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

For further information please refer to National Semiconductors Application Note AN-76.

National Semiconductor Corporation

DS0026/DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to ($V^+ - 0.1V$) in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

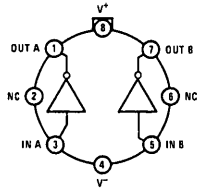
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

TO-5 Package

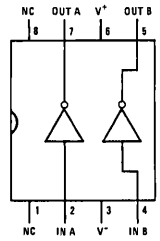


TL/F/5853-1

Note: Pin 4 connected to case.

Order Number DS0026H or DS0026CH See NS Package Number H08C

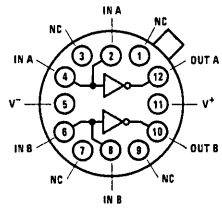
Dual-In-Line Package



TL/F/5853-2

Order Number DS0026CJ-8, or DS0026CN See NS Package Number J08A or N08E

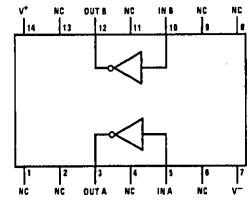
TO-8 Package



TL/F/5853-3

Order Number DS0026G or DS0026CG See NS Package Number G12C

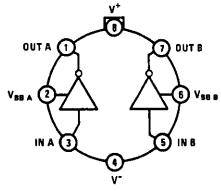
Dual-In-Line Package



TL/F/5853-4

Order Number DS0026J or DS0026CJ See NS Package Number J14A

TO-5 Package

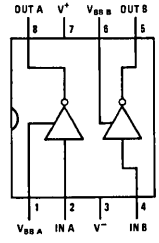


TL/F/5853-5

Note: Pin 4 connected to case.

Order Number DS0056H or DS0056CH See NS Package Number H08C

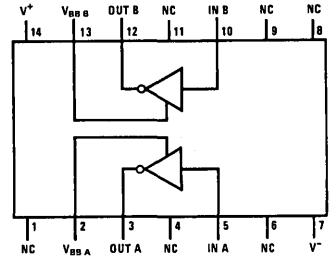
Dual-In-Line Package



TL/F/5853-6

Order Number DS0056J-8, DS0056CJ-8 or DS0056CN See NS Package Number J08A or N08E

Dual-In-Line Package



TL/F/5853-7

Order Number DS0056J or DS0056CJ See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
Metal Can (TO-5)	660 mW
Operating Temperature Range	
DS0026, DS0056	−55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_{OL} = 1$ mA			$V^- + 0.7$	$V^- + 1.0$	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{SS} \geq V^+ + 1.0V$, $I_{OH} = -1$ mA	DS0026	$V^+ - 1.0$	$V^+ - 0.8$		V
			DS0056	$V^+ - 0.3$	$V^+ - 0.1$		V
$I_{CC(ON)}$	"ON" Supply Current (one side on)	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$ (Note 6)	DS0026		30	40	mA
			DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics ($T_A = 25°C$) (Notes 5 and 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{ON}	Turn-On Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-Off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		15	18	ns
			$C_L = 1000$ pF		20	35	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		30	40	ns
			$C_L = 1000$ pF		36	50	ns
t_f	Fall Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		12	16	ns
			$C_L = 1000$ pF		17	25	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		28	35	ns
			$C_L = 1000$ pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

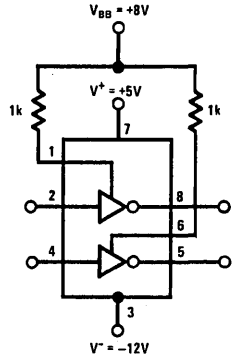
Note 4: All typical values for $T_A = 25°C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1$ kΩ (for one side) when output is low.

Note 7: The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Typical V_{BB} Connection



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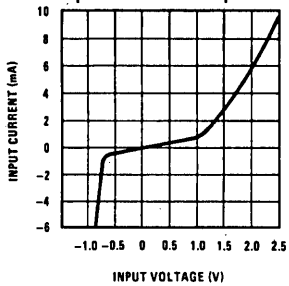
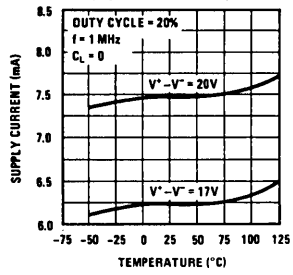
Typical Performance Characteristics

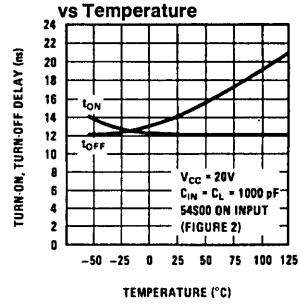
Input Current vs Input Voltage



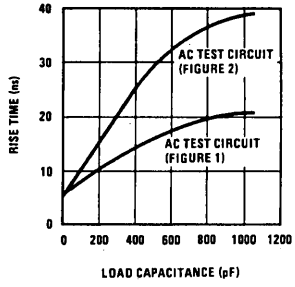
Supply Current vs Temperature



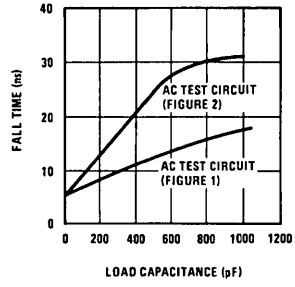
Turn-On and Turn-Off Delay vs Temperature



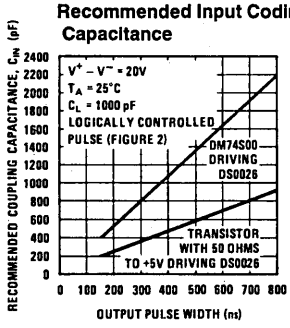
Rise Time vs Load Capacitance



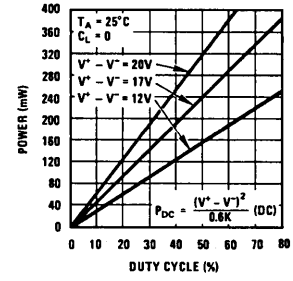
Fall Time vs Load Capacitance



Recommended Input Coding Capacitance



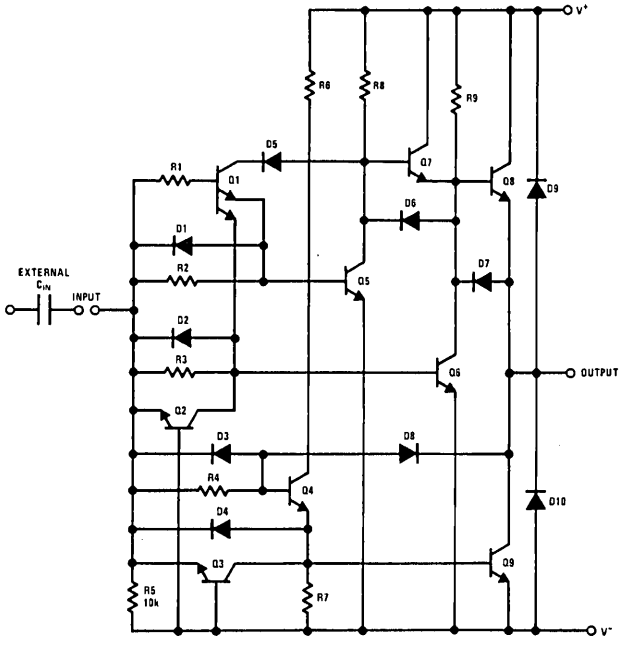
DC Power (P_{DC}) vs Duty Cycle



TL/F/5853–9

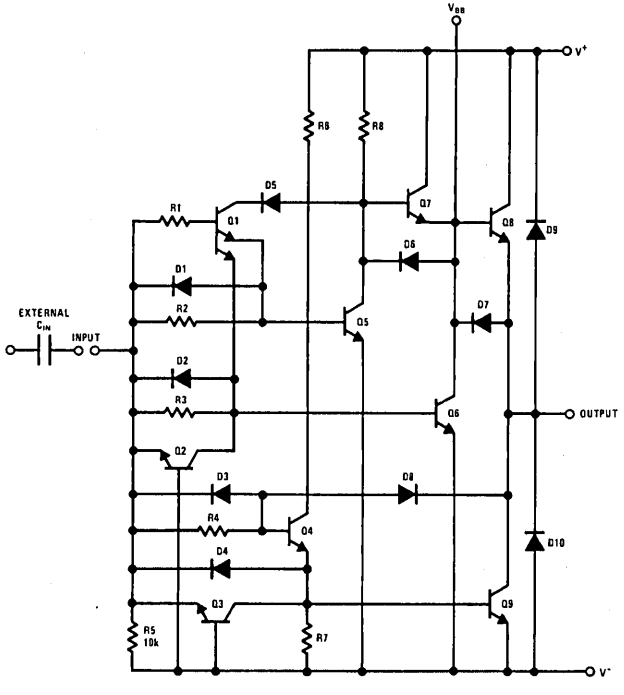
Schematic Diagrams

1/2 DS0026



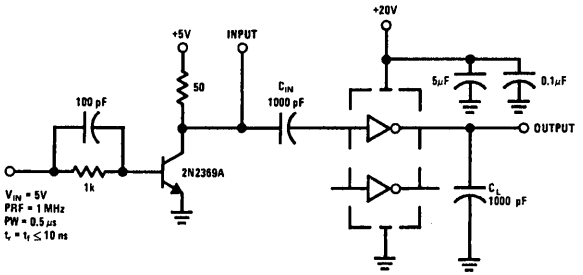
TL/F/5853–10

1/2 DS0056



TL/F/5853–11

AC Test Circuits and Switching Time Waveforms



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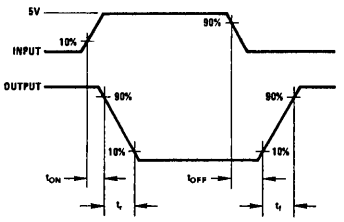

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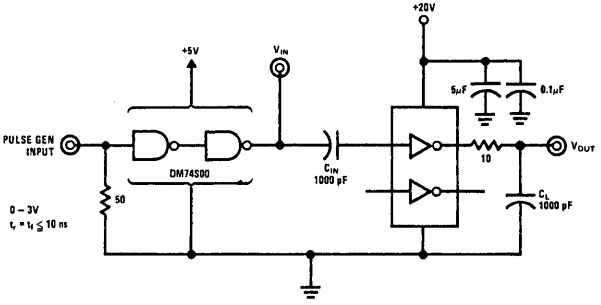
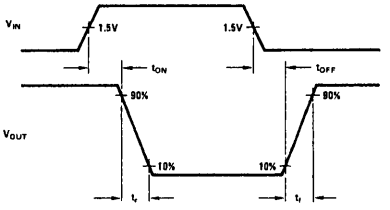
FIGURE 1



TL/F/5853–14

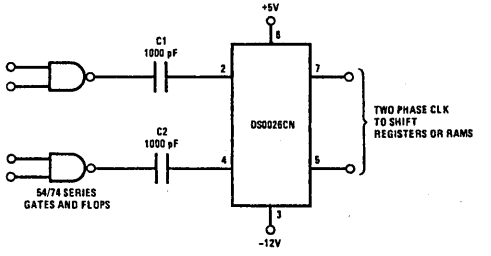


TL/F/5853–15

FIGURE 2

Typical Applications

AC Coupled MOS Clock Driver



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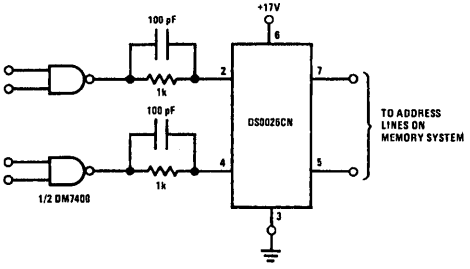
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



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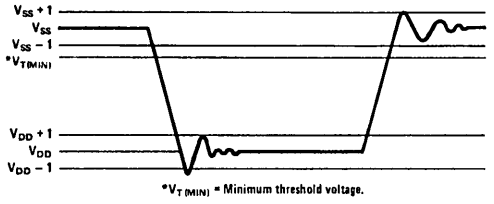
Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Application Hints (Continued)

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock specification, in diagram form, with idealized ringing sketched in. The



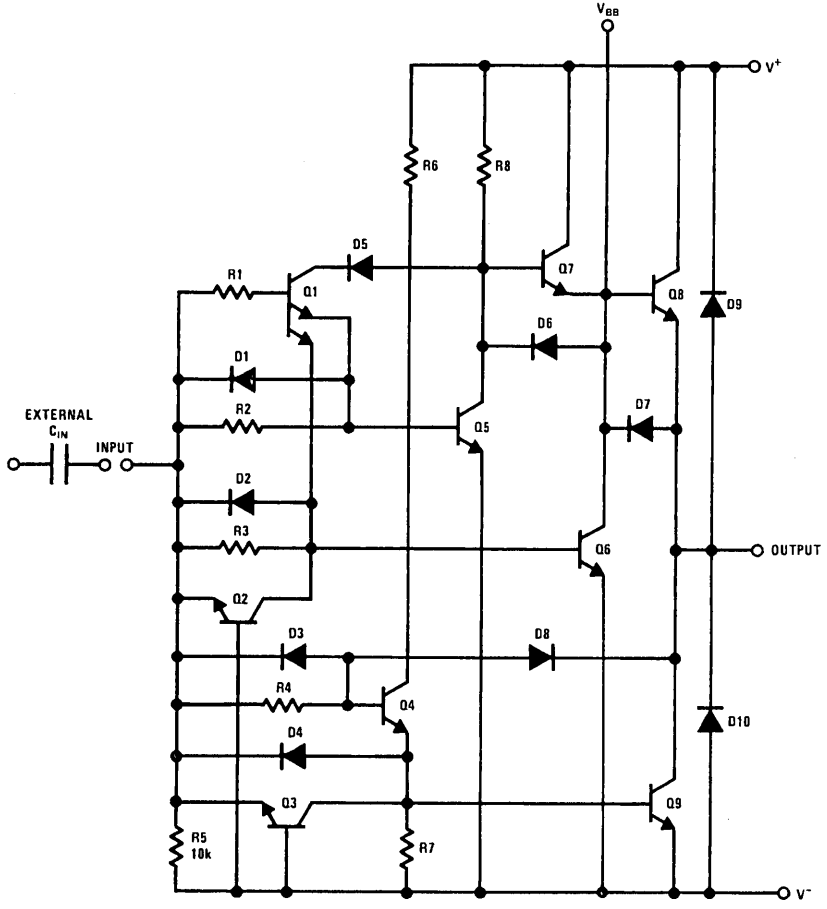
TL/F/5853–18

FIGURE 6. Clock Waveform

ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damp-



TL/F/5853–11

FIGURE 7. Schematic of 1/2 DS0056

Application Hints (Continued)

ing resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q8 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the V_{SS} − 1.0V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q8 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin on this line to zero.

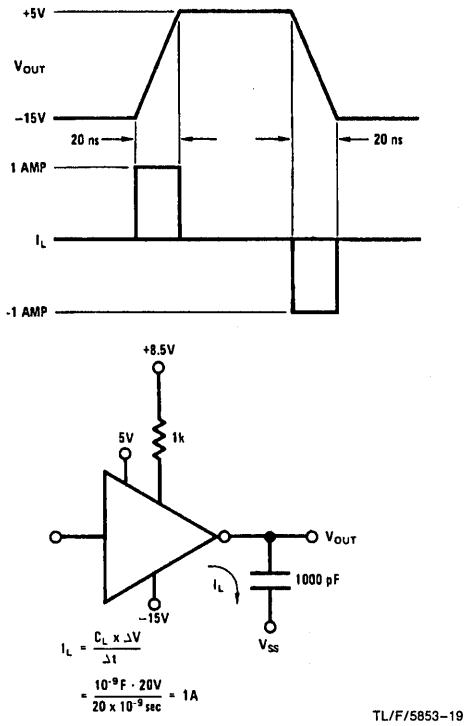


FIGURE 8. Clock Waveforms (Voltage and Current)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L.

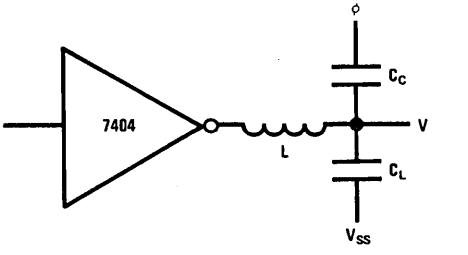


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of

Application Hints (Continued)

noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

National Semiconductor Corporation

DS3245 Quad MOS Clock Driver

General Description

The DS3245 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

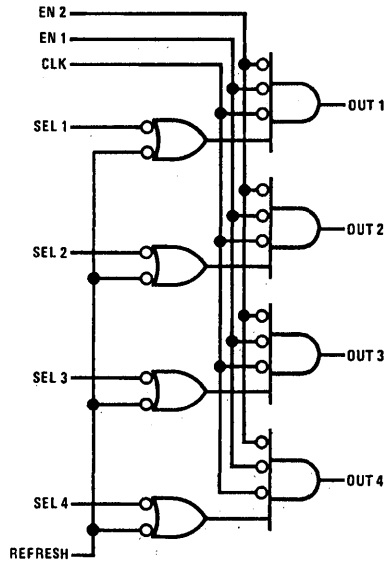
Only 2 supplies, 5 V_{DC} and 12 V_{DC}, are required without compromising the usual high V_{OH} specification obtained by circuits using a third supply.

The device features 2 common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

Features

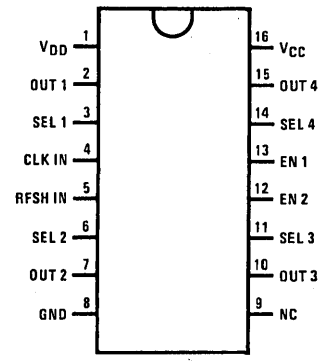
- TTL compatible inputs
- Operates from 2 standard supplies: 5 V_{DC}, 12 V_{DC}
- Internal bootstrap circuit eliminates need for external PNP's
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function equivalent to Intel 3245

Logic and Connection Diagrams



TL/F/5873-1

Dual-In-Line Package



TL/F/5873-2

Top View

Order Number DS3245J or DS3245N
See NS Package Number J16A or N16A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5V to +7V
Supply Voltage, V_{DD}	−0.5V to +14V
All Input Voltages	−1.0V to V_{DD}
Outputs for Clock Driver	−1.0V to V_{DD} + 1V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Supply Voltage, V_{DD}	11.4	12.6	V
Operating Temperature $9T_A$	0	75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{FD}	Select Input Load Current	V_F = 0.45V			−0.25	mA
I_{FE}	Enable Input Load Current	V_F = 0.45V			−1.0	mA
I_{RD}	Select Input Leakage Current	V_R = 5V			10	μA
I_{RE}	Enable Input Leakage Current	V_R = 5V			40	μA
V_{OL}	Output Low Voltage	I_{OL} = 5 mA, V_{IH} = 2V			0.45	V
		I_{OL} = −5 mA	−1.0			V
V_{OH}	Output High Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V	V_{DD} − 0.50			V
		I_{OH} = 5 mA			V_{DD} + 1.0	V
V_{IL}	Input Low Voltage, All Inputs				0.8	V
V_{IH}	Input High Voltage, All Inputs		2			V
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−1.0	−1.5	V

Power Supply Current Drain

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Current from V_{CC} Output in High State	V_{CC} = 5.25V, V_{DD} = 12.6V		26	34	mA
I_{DD}	Current from V_{DD} Output in High State	V_{CC} = 5.25V, V_{DD} = 12.6V		23	30	mA
I_{CC}	Current from V_{CC} Output in Low State	V_{CC} = 5.25V, V_{DD} = 12.6V		29	39	mA
I_{DD}	Current from V_{DD} Output in Low State	V_{CC} = 5.25V, V_{DD} = 12.6V		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +°C range. All typical values are for T_A = 25°C and V_{CC} = 5V and V_{DD} = 12V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Switching Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Conditions	Min(1)	Typ(2,4)	Max(3)	Units
t_{-+}	Input to Output Delay	$R_{SERIES} = 0$	5	11		ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 0$		20	32	ns
t_{+-}	Input to Output Delay	$R_{SERIES} = 0$	3	7		ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 0$		18	32	ns
t_T	Output Transition Time	$R_{SERIES} = 20\Omega$	10	17	25	ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 20\Omega$		27	38	ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 20\Omega$		25	38	ns

Capacitance $T_A = 25°C$(5)

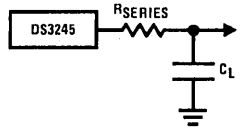
Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance, $\overline{I_1}, \overline{I_2}, \overline{I_3}, \overline{I_4}$			5	8	pF
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E1}, \overline{E2}$			8	12	pF

Note 1: $C_L = 150$ pF
Note 2: $C_L = 200$ pF
Note 3: $C_L = 250$ pF
} These values represent a range of total stray plus clock capacitance for nine 4k RAMs.

Note 4: Typical values are measured at 25°C.

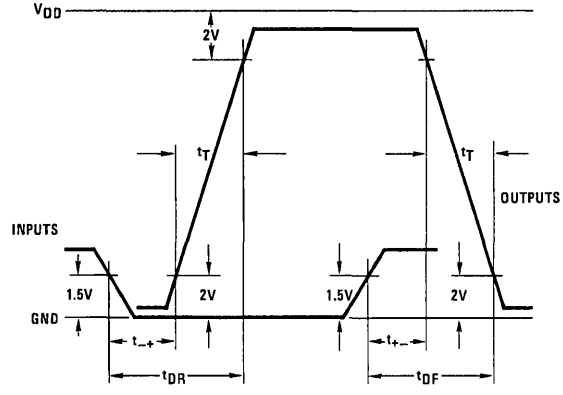
Note 5: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{BIAS} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

AC Test Circuit and Switching Time Waveforms



Input pulse amplitudes: 3V
Input pulse rise and fall times:
5 ns between 1V and 2V
Measurements points: see waveforms

TL/F/5873–3



TL/F/5873–4

National Semiconductor Corporation

DS1628/DS3628 Octal TRI-STATE® MOS Drivers

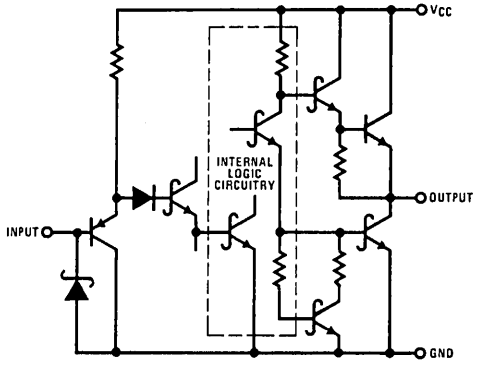
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

Features

- High speed capabilities
  - Typical 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4V min)
- High density
  - Eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams



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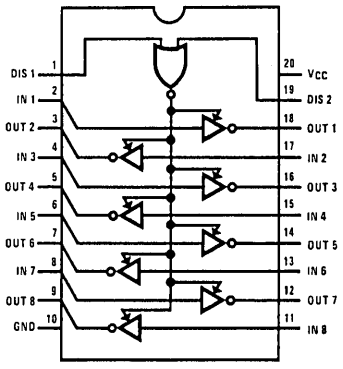
(Equivalent Input/Output Circuit)

Dual-In-Line Package



Top View

TL/F/5875–2

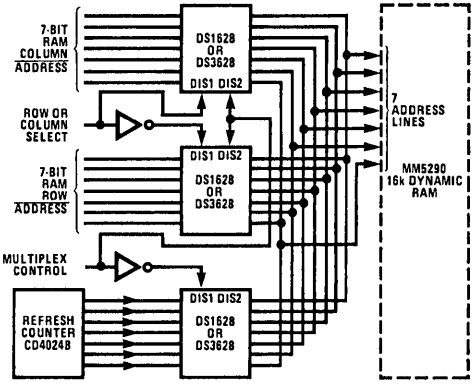
Order Number
DS1628J, DS3628J, DS3628N
See NS Package Number J20A or N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



TL/F/5875–3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1628	−55	+125	°C
DS3628	0	+70	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			−180	−400	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18 mA			−0.7	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1628	3.4	4.3		V
			DS3628	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1628		0.25	0.4	V
			DS3628		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1628	2.5	3.9		V
			DS3628	2.7	3.9		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1628/DS3628		0.35	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 6)			−150		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 6)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, DIS1 or DIS2 = 2.0V		−40	0.1	40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All Other Inputs = X, Outputs at Hi-Z		90	120	mA
			DIS1, DIS2 = 0V, Others = 3V Outputs on		70	100	mA
			All Inputs = 0V, Outputs Off		25	50	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 6)

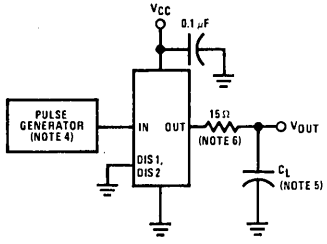
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{S+-}	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.0	5.0	ns
			C_L = 500 pF		6.5	8.0	
t_{S-+}	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		4.2	5.0	ns
			C_L = 500 pF		6.5	8.0	
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		4.2	6.0	ns
			C_L = 500 pF		19	22	
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		5.2	7.0	ns
			C_L = 500 pF		20	24	
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF to GND	R_L = 2 kΩ to V_{CC} (*Figure 2*)		19	25	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF to GND	R_L = 2 kΩ to GND (*Figure 2*)		13	20	ns

Switching Characteristics (Continued) (V_{CC} = 5V, T_A = 25°C) (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to GND, R_L = 400Ω to V_{CC} (*Figure 3*)		18	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to GND, R_L = 400Ω to GND (*Figure 3*)		8.5	15	ns

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_r, t_f



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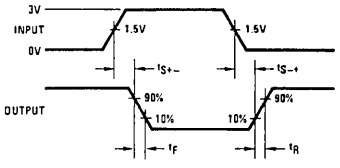
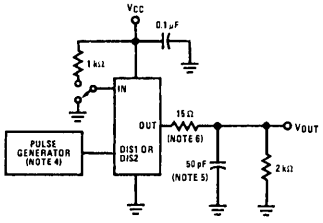


TL/F/5875-5

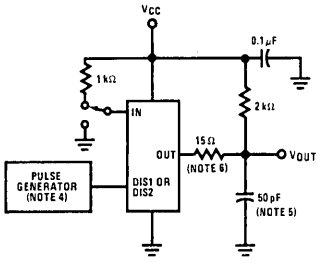
FIGURE 1

t_{ZH}

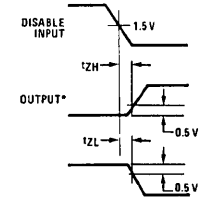


TL/F/5875-6

t_{ZL}



TL/F/5875-7

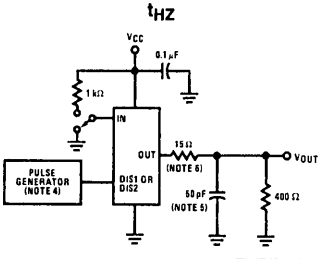


TL/F/5875-8

*ANY ONE OF EIGHT OUTPUTS

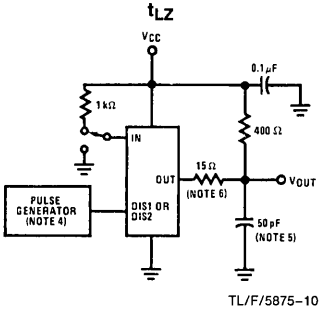
FIGURE 2

t_{HZ}

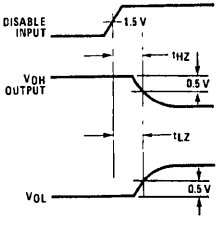


TL/F/5875-9

t_{LZ}



TL/F/5875-10



TL/F/5875-11

FIGURE 3

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1628 and across the 0°C to +70°C range for the DS3628. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages references to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 mHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: When measuring output drive current and switching response for the DS1628 and DS3628 a 15Ω resistor should be placed in series with each output.

National Semiconductor Corporation

DS1644/DS3644/DS1674/DS3674 Quad TTL to MOS Clock Drivers

General Description

The DS1644/DS3644 and DS1674/DS3674 are quad bipolar-to-MOS clock drivers with TTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transisitors are used on all inputs thereby minimizing input loading.

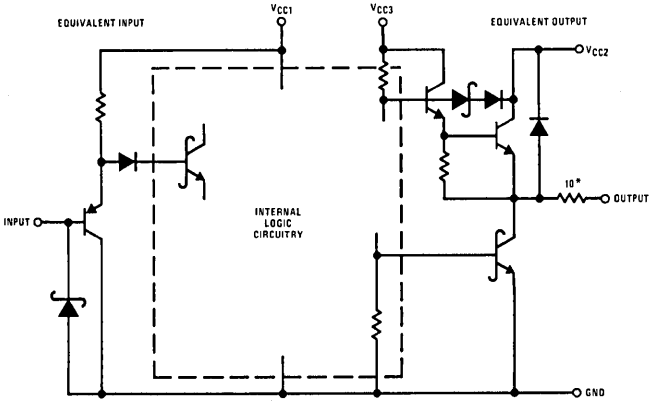
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1644/DS3644 contains a 10Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

- TTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS1644/DS3644)

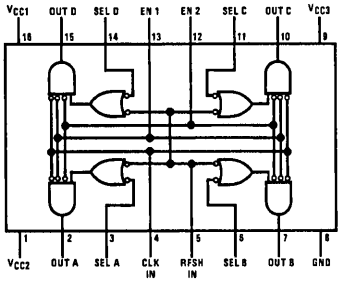
Schematic and Connection Diagrams



*DS1644/DS3644 only

TL/F/5876-1

Dual-In-Line Package



TL/F/5876-2

Top View
Order Number DS3644J, DS3674J, DS3644N or DS3674N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13.5V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
V_{CC1}			
DS1644, DS1674	4.5	5.5	V
DS3644, DS3674	4.75	5.25	V
V_{CC2}			
DS1644, DS1674	4.5	13.2	V
DS3644, DS3674	4.75	12.6	V
V_{CC3}			
DS1644, DS1674	V_{CC2}	16.5	V
DS3644, DS3674	V_{CC2}	15.75	V
Temperature, T_A			
DS1644, DS1674	−55	+125	°C
DS3644, DS3674	0	+70	°C

Electrical Characteristics

5V operation, (V_{CC1} = V_{CC2} = 5V, V_{CC3} = 12V); 12V operation, (V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = V_{CC2} + (3V ±10%)); DS1644, DS1674, ±10% power supply tolerances; DS3644, DS3674, ±5% power supply tolerances, unless otherwise noted. (Notes 2, 3 and 4).

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Select Inputs		0.01	10	μA
			All Other Inputs		0.04	40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Select Inputs		−40	−250	μA
			All Other Inputs		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2} −0.5	V_{CC2} −0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V			0.3	0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V			V_{CC2} +0.8	V_{CC2} +1.5	V
I_{CCH}	Supply Current Output High						
	I_{CC1}	All Inputs V_{IN} = 0V Outputs Open	V_{CC1} = Max		18	27	mA
	I_{CC2}		12V Operation		−2	−4	mA
	I_{CC3}				2	4	mA
	I_{CC2}		5V Operation		−8	−16	mA
	I_{CC3}				8	16	mA
I_{CCL}	Supply Currents Outputs Low						
	I_{CC1}	All Inputs V_{IN} = 5V Outputs Open	V_{CC1} = 5.25V		25	40	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		16	25	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1644, DS1674 and across the 0°C to +70°C range for the DS3644, DS3674. All typicals are given for T_A = 25°C.

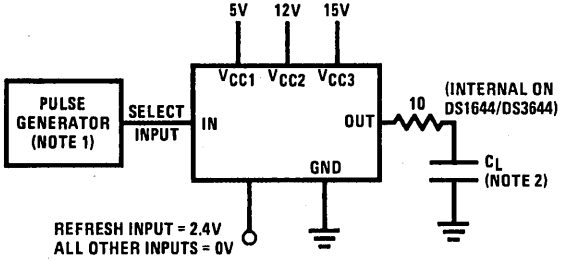
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For AC measurements, a 10Ω resistor must be placed in series with the output of the DS1674/DS3674. This resistor is internal to the DS1644/DS3644 and need not be added.

Switching Characteristics T_A = 25°C unless otherwise noted, (Note 4), (*Figures 1, 2, 3 and 4*)

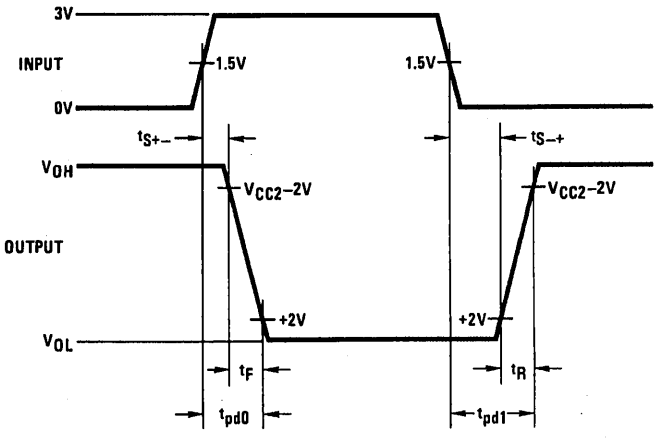
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{s+-}	Storage Delay Negative Edge	R_D = 10Ω	C_L = 100 pF		8	11	ns
			C_L = 400 pF		12	16	ns
t_{s-+}	Storage Delay Positive Edge	R_D = 10Ω	C_L = 100 pF		10	13	ns
			C_L = 400 pF		13	16	ns
t_F	Fall Time	R_D = 10Ω	C_L = 100 pF		9	16	ns
			C_L = 400 pF		17	24	ns
t_R	Rise Time	R_D = 10Ω	C_L = 100 pF		8	12	ns
			C_L = 400 pF		13	19	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 100 pF		17	27	ns
			C_L = 400 pF		29	40	ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 100 pF		18	25	ns
			C_L = 400 pF		26	35	ns

AC Test Circuits and Switching Time Waveforms



TL/F/5876–3

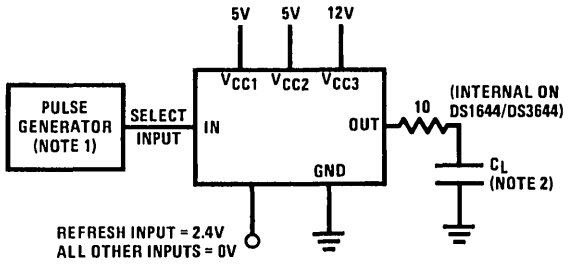
FIGURE 1. 12V Operation



TL/F/5876–4

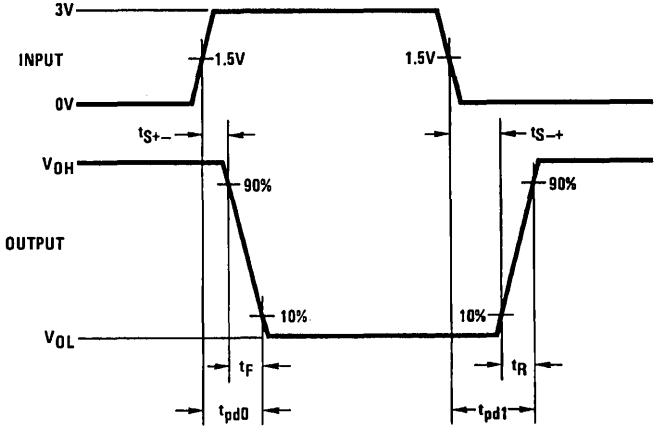
FIGURE 2. 12V Operation

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5876–5

FIGURE 3. 5V Operation



TL/F/5876–6

FIGURE 4. 5V Operation

Note 1: The pulse generator has the following characteristics. PPR = 1 MHz, $t_R \leq 10$ ns, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Truth Table

Input					Output
Enable 1	Enable 2	Select Input	Clock Input	Refresh Input	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

National Semiconductor Corporation

DS3647A Quad TRI-STATE® MOS Memory I/O Register

General Description

The DS3647A is a 4-bit I/O buffer register intended for use in MOS memory systems. This circuit employs a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. This circuit uses Schottky-clamped transistor logic for minimum propagation delay and employs PNP input transistors so that input currents are low, allowing a large fan-out for this circuit which is needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

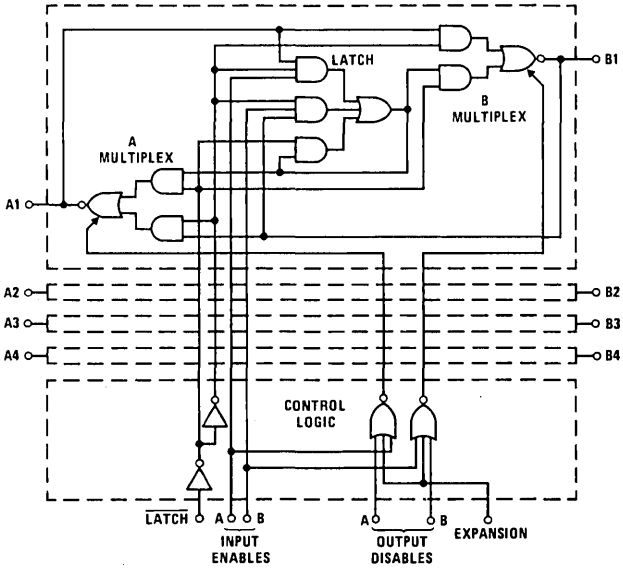
The DS3647A features TRI-STATE outputs. The "B" port outputs are designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA.

Data going from port "A" to port "B" and from "B" to port "A" is inverted in the DS3647A.

Features

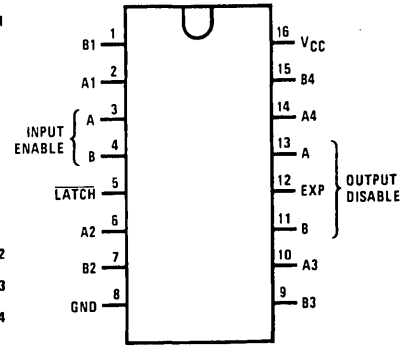
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL compatible
- Transmission line driver output

Logic and Connection Diagrams



TL/F/8354-1

Dual-In-Line Package



TL/F/8354-2

Top View

Order Number DS3647AD or DS3647AN
See NS Package Number D16C or N16A

4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65° to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 10.0 mW/° C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS3647A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	V_{CC}=5.5V, V_{IN}=5.5V	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	V_{CC}=5.5V, V_{IN}=0.5V	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC}=4.5V, I_{IN}=−18 mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	V_{CC}=4.5V, I_{OL}=20 mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	V_{CC}=4.5V	I_{OL}=30 mA		0.3	0.4	V
			I_{OL}=50 mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	I_{OH}=−1 mA	V_{CC}=5V	3.0	3.4		V
			V_{CC}=4.5V	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	I_{OH}=−5.2 mA, (Note 4)	V_{CC}=5V	2.9	3.3		V
			V_{CC}=4.5V	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	V_{CC}=4.5V to 5.5V, V_{OUT}=0V, (Note 4)		−50	−80	−120	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	V_{CC}=4.5V to 5.5V, V_{OUT}=0V, (Note 4)		−70	−120	−180	mA
I_{CC}	Power Supply Current	Exp=3V, A Ports=0V, B Ports Open, All Other Pins=0V	DS3647A		100	140	mA
		Enable A, Latch=3V, A Ports=0V, B Ports Open, All Other Pins=0V	DS3647A		70	105	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC}=5V and T_A=25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Only one output at a time should be shorted.

Switching Characteristics ($V_{CC}=5V$, $T_A=25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA TRANSFER B PORT TO A PORT						
t_{pd0}	Propagation Delay to a Logic "0"	$C_L=50$ pF, $R_L=280\Omega$, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	$C_L=50$ pF, $R_L=280\Omega$, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS3647A						
t_{pd0}	Propagation Delay to a Logic "0"	$C_L=50$ pF, $R_L=100\ \Omega$, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	$C_L=50$ pF, $R_L=100\ \Omega$, *(Figures 2 and 4)*		8.0	15	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS3647A						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before $\overline{\text{Latch}}$ Goes Low		5	0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low		10	5		ns

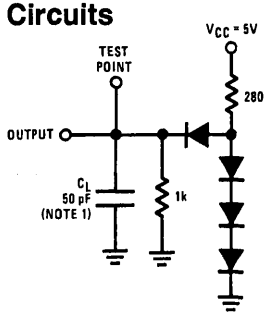
Product Description

Device Number	B Port To A Port Function	A Port To B Port Function	A Port Outputs	B Port Outputs
DS3647A	Inverting	Inverting	TRI-STATE	TRI-STATE

Truth Table

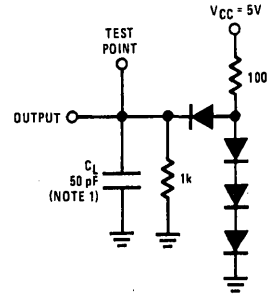
Input Enables		$\overline{\text{Latch}}$	Output Disables		Expansion	A Ports A1-A4	B Ports B1-B4	Comments
A	B		A	B				
1	0	1	0	0	0	Hi-Z	$\overline{A}$	Data in on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Data in on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	Data stored which is present when $\overline{\text{latch}}$ goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Data stored which is present when $\overline{\text{latch}}$ goes low
1	0	x	0	1	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on A, may be latched
0	1	x	1	0	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on B, may be latched
x	x	x	x	x	1	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits



TL/F/8354–3

FIGURE 1. A Port Load

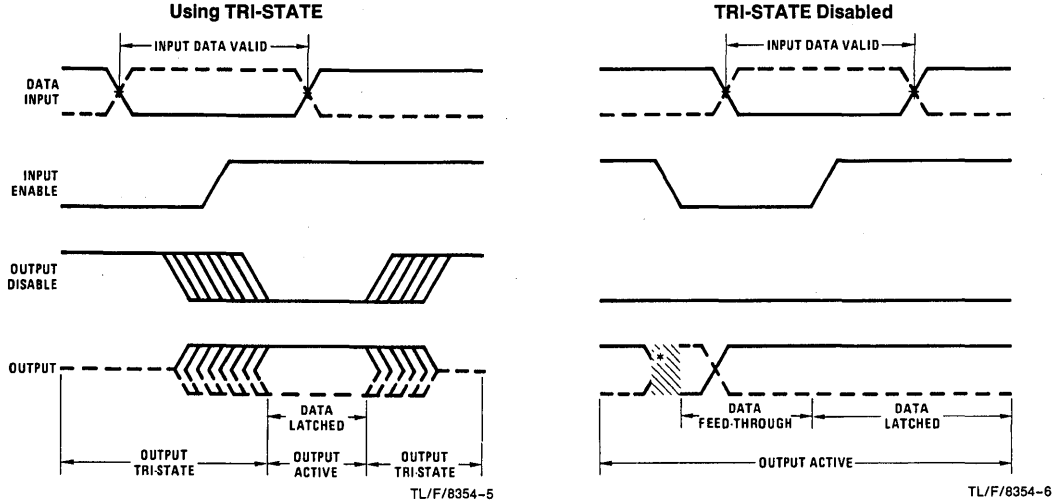


TL/F/8354–4

FIGURE 2. B Port Load

Note 1: C_L includes probe and jig capacitance.

Operating Waveforms

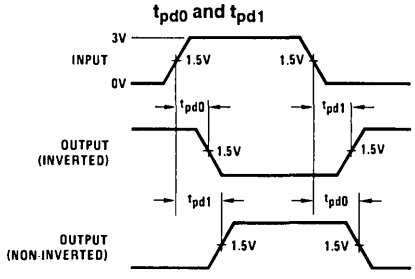


TL/F/8354–5

TL/F/8354–6

*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

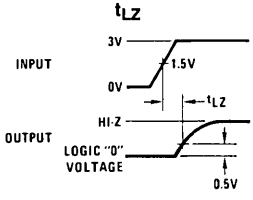
Switching Time Waveforms



TL/F/8354-7

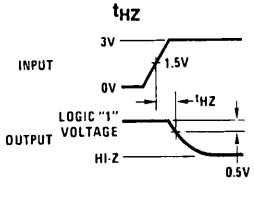
Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4



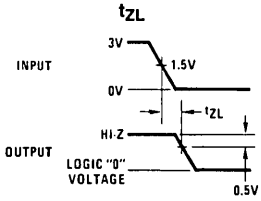
TL/F/8354-8

FIGURE 5



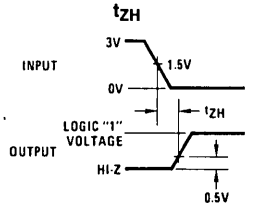
TL/F/8354-10

FIGURE 6



TL/F/8354-9

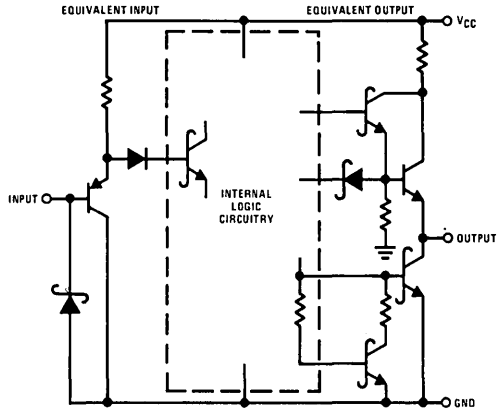
FIGURE 7



TL/F/8354-11

FIGURE 8

Schematic Diagram

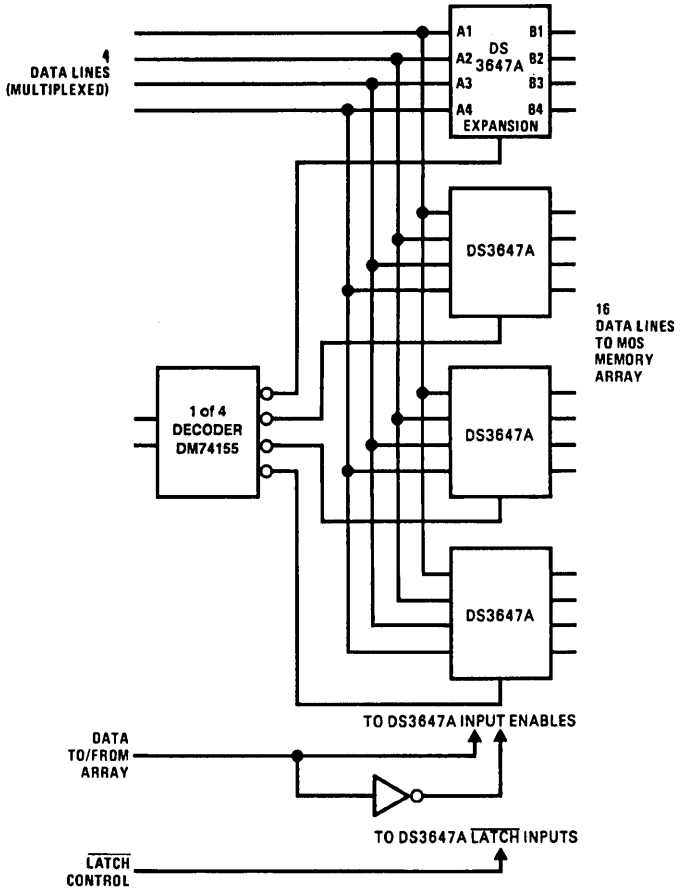


TL/F/8354-12

Note. Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3647A can be used as a register capable of multiplexing data lines.



TL/F/8354–13

National Semiconductor Corporation

DS1648/DS3648/DS1678/DS3678 TRI-STATE® TTL to MOS Multiplexers/Drivers

General Description

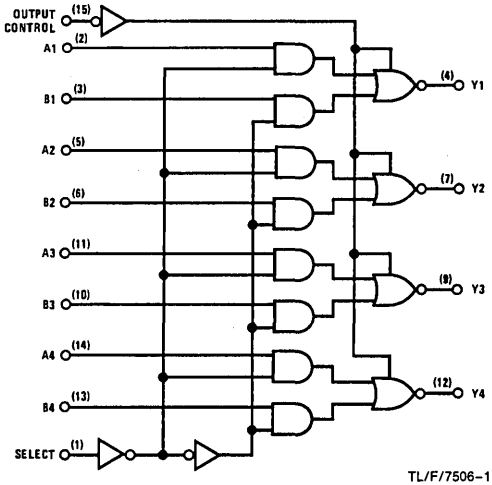
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

Features

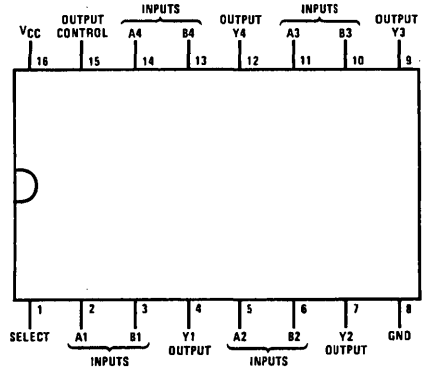
- TRI-STATE outputs interface directly with system-bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

Logic and Connection Diagrams



TL/F/7506–1

Dual-In-Line Package



TL/F/7506–2

Top View

Order Number DS1648J, DS3648J, DS1678J DS3678J, DS3648N or DS3678N
See NS Package Number J16A or N16A

4

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

* Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1648, DS1678	−55	+125	°C
DS3648, DS3678	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1648/DS1678	2.7	3.6		V
			DS3648/DS3678	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1648/DS1678		0.25	0.4	V
			DS3648/DS3678		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1648	2.4	3.5		V
			DS1678	2.5	3.5		V
			DS3648	2.6	3.5		V
			DS3678	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1648		0.6	1.1	V
			DS1678		0.4	0.5	V
			DS3648		0.6	1.0	V
			DS3678		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{Hi-Z}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Control = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Control = 3V All Other Inputs at 0V		42	60	mA
			All Inputs at 0V		20	32	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1648 and DS1678 and across the 0°C to +70°C range for the DS3648 and DS3678. All typical values for T_A = 25°C and V_{CC} = 5V.

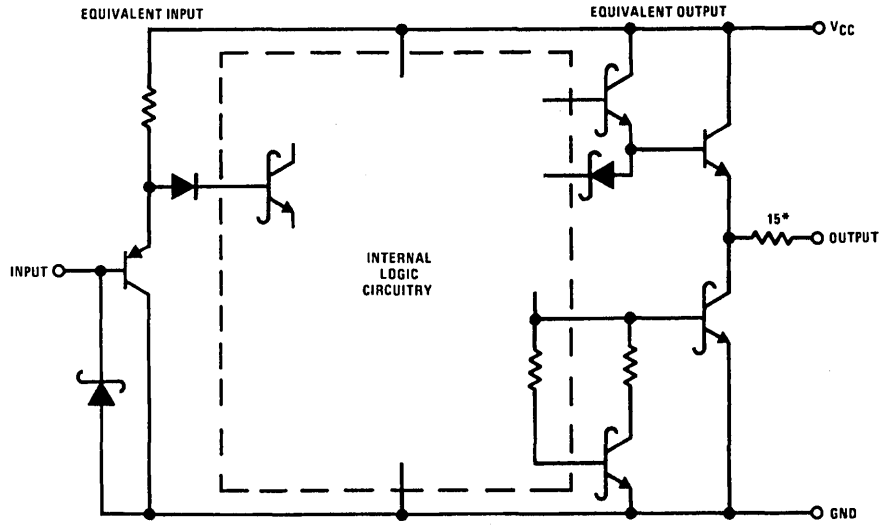
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1678 and DS3678 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1648/DS3648 and need not be added.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		5	7	ns
			C_L = 500 pF		9	12	ns
$t_{S\mp}$	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{ZL}	Delay from Output Control Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Output Control Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to GND *(Figure 2)*			8	15	ns
t_{LZ}	Delay from Output Control Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}, *(Figure 3)*			15	25	ns
t_{HZ}	Delay from Output Control Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to GND, *(Figure 3)*			10	25	ns
$t_{S\pm}$	Propagation Delay to Logical "0" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			12	15	ns
$t_{S\mp}$	Propagation Delay to Logical "1" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			14	17	ns
$t_{S\pm}$	Propagation Delay to Logical "0" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			16	20	ns
$t_{S\mp}$	Propagation Delay to Logical "1" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			14	20	ns

Schematic Diagram

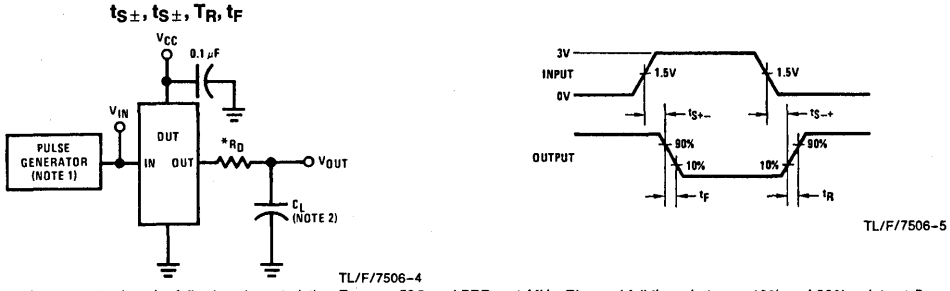


TL/F/7506–3

*DS1648/DS3648 only

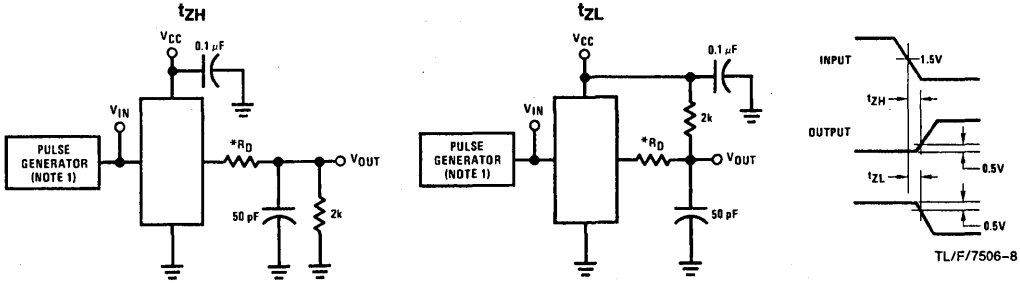
4

AC Test Circuits and Switching Time Waveforms



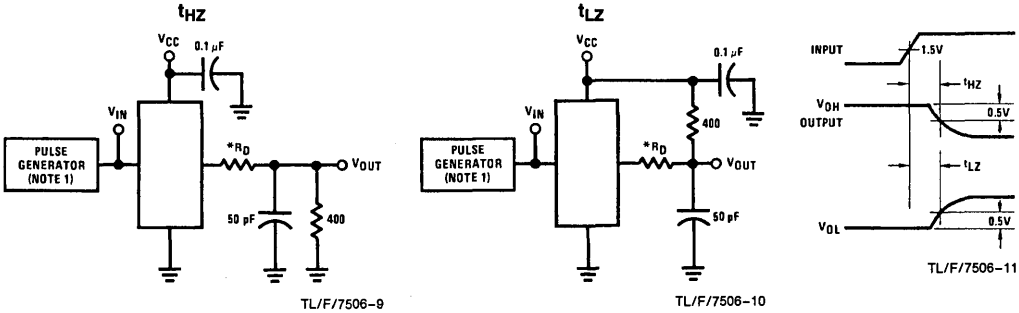
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.
Note 2: C_L includes probe and jig capacitance.

FIGURE 1



*Internal on DS1648 and DS3648

FIGURE 2



*Internal on DS1648 and DS3648

FIGURE 3

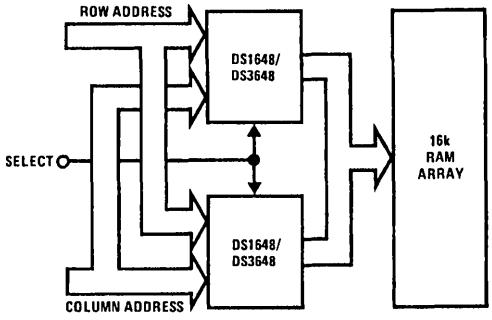
Truth Table

Output Control	Inputs			Outputs
	Select	A	B	
H	X	X	X	Hi-Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level
L = Low level
X = Don't care
Hi-Z = TRI-STATE mode

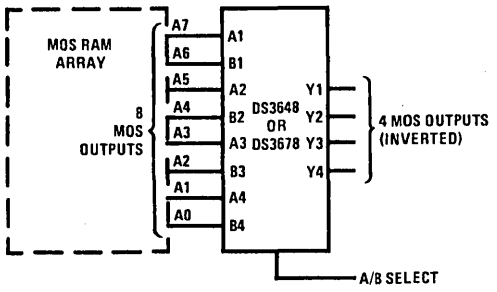
Typical Applications

Addressing 16k RAM



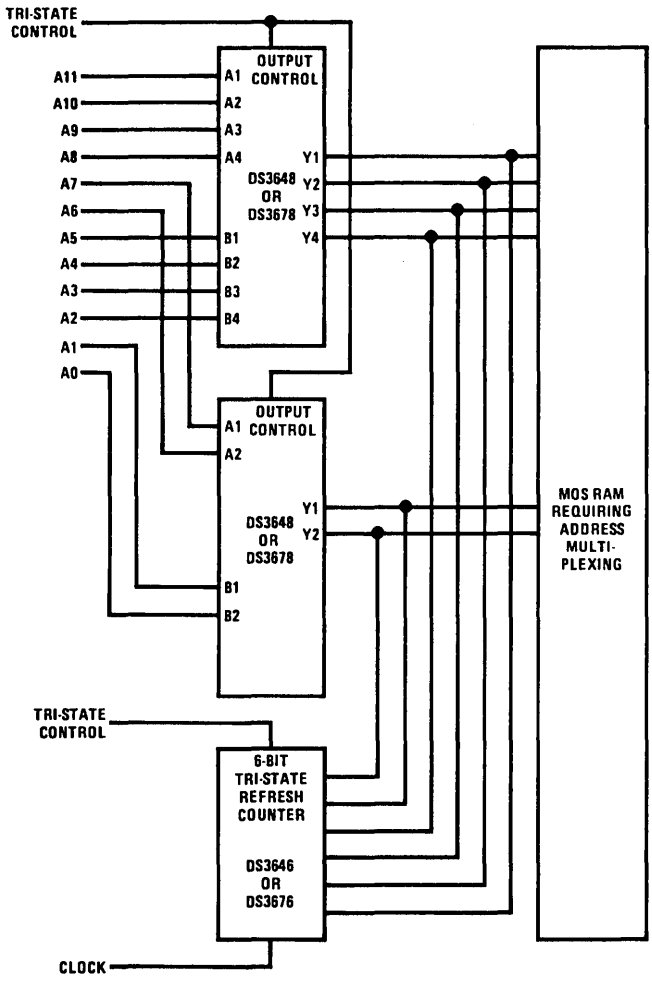
TL/F/7506–12

2:1 Multiplexing of RAM Outputs



TL/F/7506–14

Refreshing Using TRI-STATE Counter



TL/F/7506–13

National Semiconductor Corporation

DS1649/DS3649/DS1679/DS3679 Hex TRI-STATE® TTL to MOS Drivers

General Description

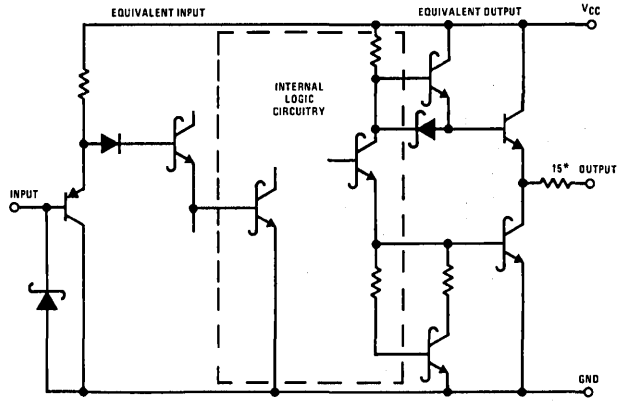
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



*DS1649/DS3649 only

TL/F/7515–1

Truth Table

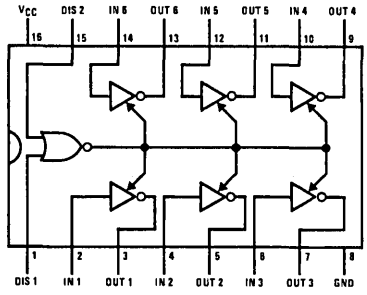
Disable Input		Input	Output
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care

Hi-Z = TRI-STATE mode

Connection Diagram

Dual-In-Line Package

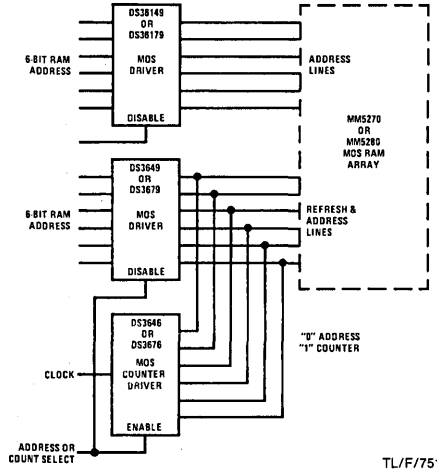


TL/F/7515–2

Top View

Order Number DS1649J, DS3649J, DS1679J, DS3679J, DS3649N or DS3679N
See NS Package Number J16A or N16A

Typical Application



TL/F/7515–3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}	4.5	5.5	V
Temperature (T_A)			
DS1649, DS1679	−55	+125	°C
DS3649, DS3679	0	+70	°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Electrical Characteristics (Note 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1649/DS1679	2.7	3.6		V
			DS3649/DS3679	2.8	3.6		
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1649/DS1679		0.25	0.4	V
			DS3649/DS3679		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1649	2.4	3.5		V
			DS1679	2.5	3.5		V
			DS3649	2.6	3.5		V
			DS3679	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1649		0.6	1.1	V
			DS1679		0.4	0.5	V
			DS3649		0.6	1.0	V
			DS3679		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V (Note 4)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, DIS1 or DIS2 = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All Other Inputs = X		42	75	mA
			All Inputs = 0V		11	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
$t_{S\pm}$	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		6	9	ns
			C_L = 500 pF		21	35	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to V_{CC} (*Figure 2*)			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to GND (*Figure 2*)			8	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF R_L = 400Ω to V_{CC} (*Figure 3*)			15	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF R_L = 400Ω to GND (*Figure 3*)			10	25	ns

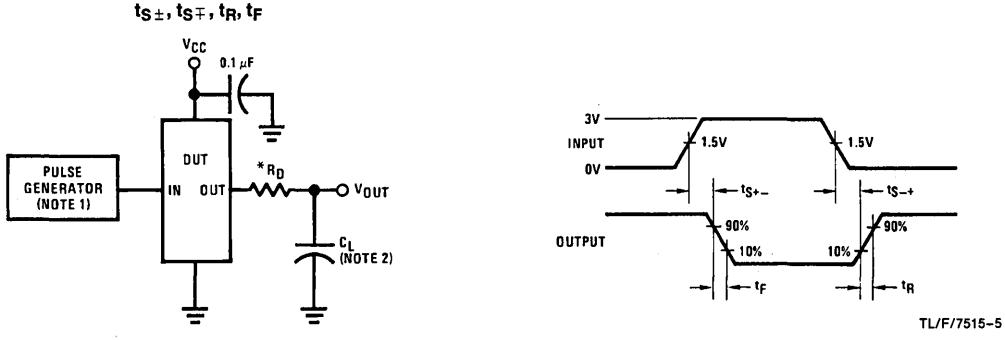
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1649 and DS1679 and across the 0°C to +70°C range for the DS3649 and DS3679. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

AC Test Circuits and Switching Time Waveforms

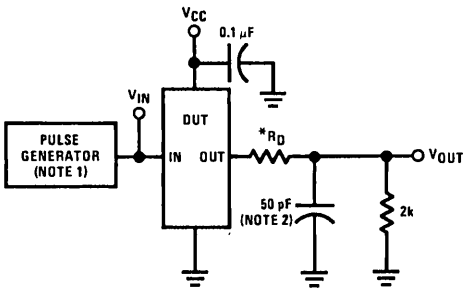


TL/F/7515-4

FIGURE 1

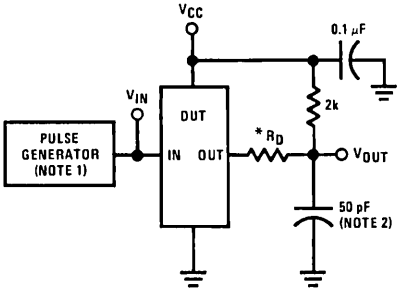
AC Test Circuits and Switching Time Waveforms (Continued)

t_{ZH}

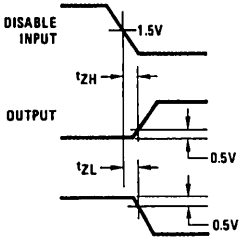


TL/F/7515-6

t_{ZL}



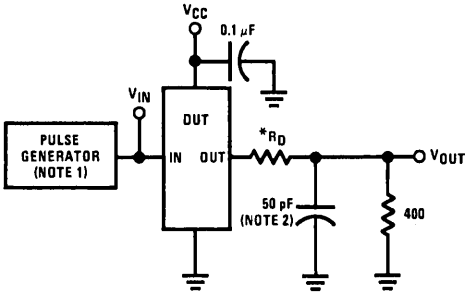
TL/F/7515-7



TL/F/7515-8

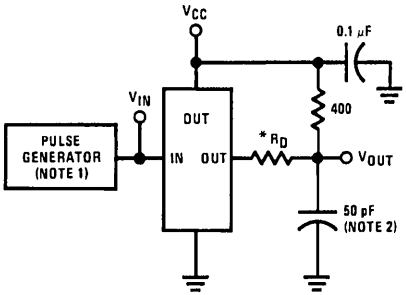
FIGURE 2

t_{HZ}

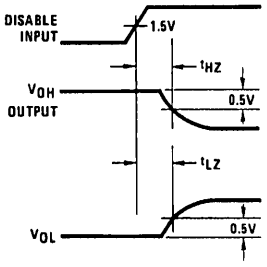


TL/F/7515-9

t_{LZ}



TL/F/7515-10



*Internal on DS1649 and DS3649

TL/F/7515-11

FIGURE 3

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$ and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.
Note 2: C_L includes probe and jig capacitance.

National Semiconductor Corporation

DS1651/DS3651, DS1653/DS3653 Quad High Speed MOS Sense Amplifiers

General Description

The DS1651/DS3651 and DS1653/DS3653 are TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated, offering a high impedance output state for bused organization.

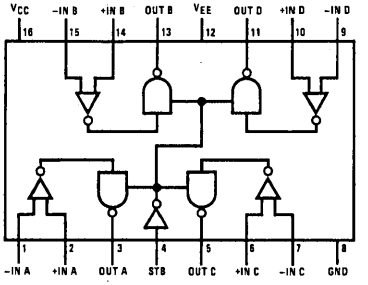
The DS1651/DS3651 has active pull-up outputs, and the DS1653/DS3653 offers open collector outputs providing implied "AND" operations.

Features

- High speed
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430 and MC3432

Connection Diagram

Dual-In-Line Package



Top View TL/F/7528–1

Order Number DS1651J, DS1653J, DS3651J, DS3653J, DS3651N or DS3653N
See NS Package Number J16A or N16A

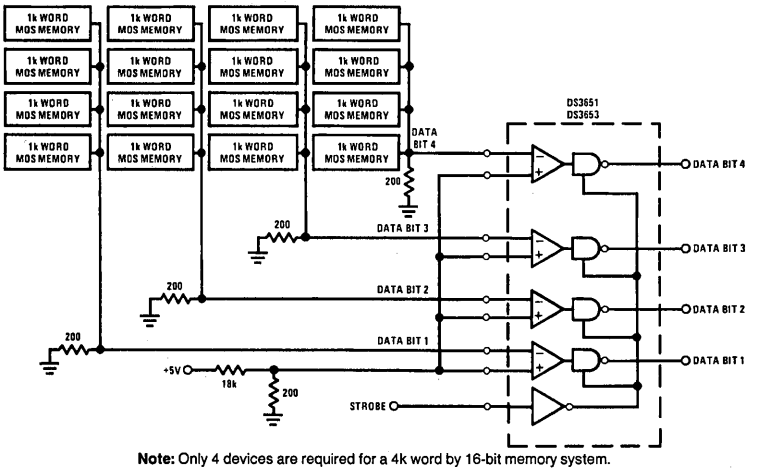
Truth Table

Input	Strobe	Output	
		DS3651	DS3653
$V_{ID} \geq 7$ mV $T_A = 0°C$ to $+70°C$	L H	H Open	Open Open
-7 mV $\leq V_{ID} \leq +7$ mV $T_A = 0°C$ to $+70°C$	L H	X Open	X Open
$V_{ID} \geq -7$ mV $T_A = 0°C$ to $+70°C$	L H	L Open	L Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate state

Typical Applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note: Only 4 devices are required for a 4k word by 16-bit memory system. TL/F/7528–2

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Power Supply Voltages	
V_{CC}	+7 V_{DC}
V_{EE}	−7 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Strobe Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temp. (Soldering, 10 seconds)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})			
DS1651, DS1653	4.5	5.5	V
DS3651, DS3653	4.75	5.25	V
Supply Voltage (V_{EE})			
DS1651, DS1653	−4.5	−5.5	V
DS3651, DS3653	−4.75	−5.25	V
Operating Temperature (T_A)			
DS1651, DS1653	−55	+125	°C
DS3651, DS3653	0	+70	°C
Output Load Current, (I_{OL})		16	mA
Differential Mode Input Voltage Range, (V_{IDR})	−5.0	+5.0	V
Common-Mode Input Voltage Range, (V_{ICR})	−3.0	+3.0	V
Input Voltage Range (Any Input to GND), (V_{IR})	−5.0	+3.0	V

Electrical Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range) VICR = −3V ≤ V_{IN} ≤ +3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = Max, V_{EE} = Max					20	µA
I_{IO}	Input Offset Current					0.5		µA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = Max, V_{EE} = Max, V_{IN} = 0.4V					−1.6	mA
$I_{IL(S)}$	Strobe Current (High State)	V_{CC} = Max,	V_{IN} = 2.4V	DS3651, DS3653			40	µA
		V_{EE} = Max	V_{IN} = V_{CC}				1	mA
			V_{IN} = 2.4V	DS1651, DS1653			100	µA
			V_{IN} = V_{CC}				1	mA
V_{OH}	Output Voltage (High States)	V_{CC} = Min, V_{EE} = Min	I_O = −400 µA	DS1651/DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = Min,	I_O = 16 mA	DS3651, DS3653			0.45	V
		V_{EE} = Min		DS1651, DS1653			0.50	
I_{CEX}	Output Leakage Current	V_{CC} = Min, V_{EE} = Min	V_O = Max	DS1653/DS3653			250	µA
I_{OS}	Output Current Short Circuit	V_{CC} = Max, V_{EE} = Max, (Note 4)		DS1651/DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = Max, V_{EE} = Max		DS3651			40	µA
				DS1651			100	µA
I_{CC}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				−17	−30	mA

4

Switching Characteristics $V_{CC} = 5\ V_{DC}$, $V_{EE} = -5\ V_{DC}$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 3*)	DS1651/ DS3651		23	45	ns
			DS1653/ DS3653		22	50	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 3*)	DS1651/ DS3651		22	55	ns
			DS1653/ DS3653		24	65	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	(*Figure 2*)	DS1653/ DS3653		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)	(*Figure 2*)	DS1653/ DS3653		13	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

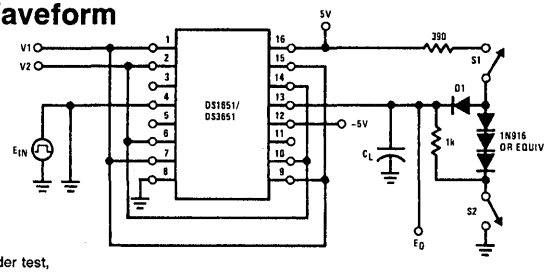
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3651, DS3653 and across the −55°C to +125°C range for the DS1651, DS1653. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{EE} = -5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1651, DS1653 and DS3651, DS3653 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differiential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Time Waveform



Note: Output of channel B shown under test, other channels are tested similarly.

TL/F/7528–3

Delay	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%

PRR = 1 MHz

Duty cycle = 50%

AC Test Circuits

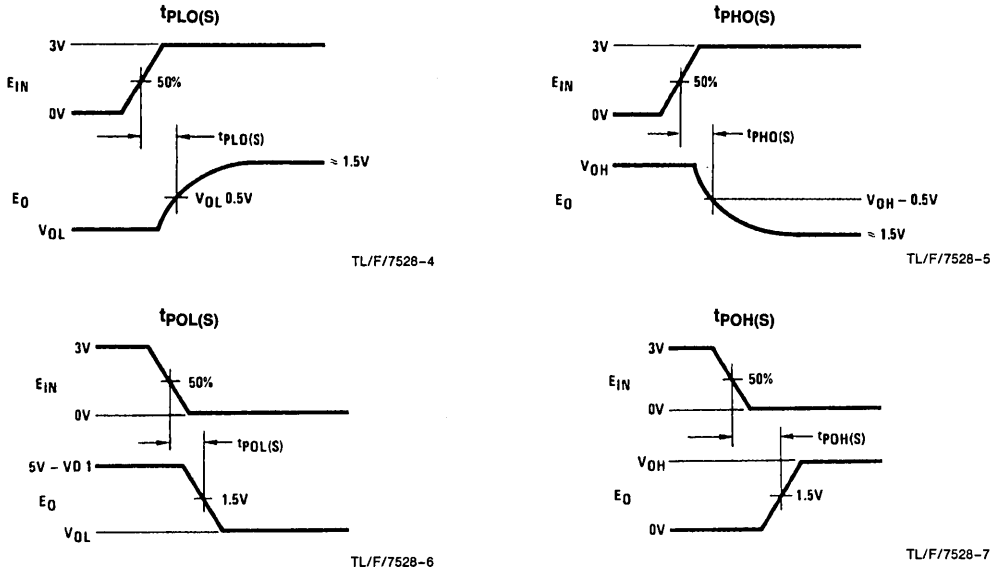
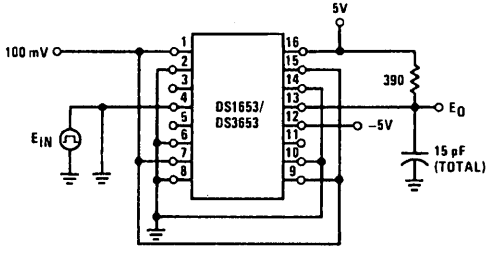
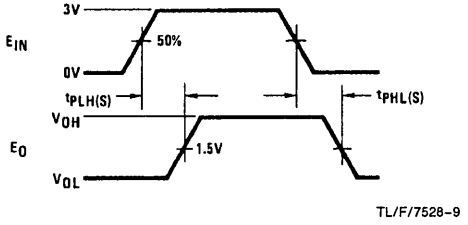


FIGURE 1. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$

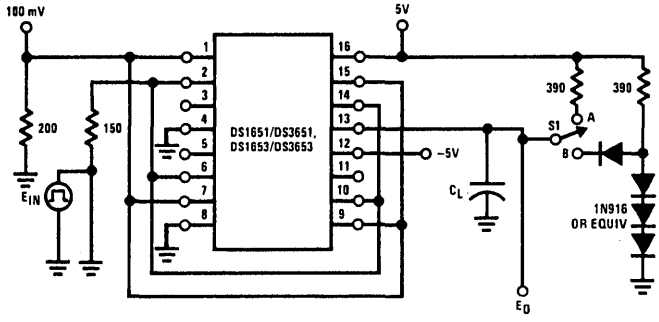


Note: Output of channel B shown under test, other channels are tested similarly.



Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

FIGURE 2. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

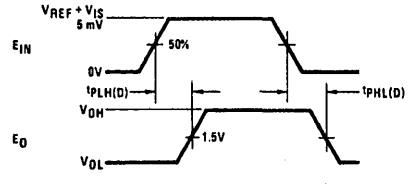


TL/F/7528–10

Note: Output of channel B shown under test, other channels are tested similarly.

S1 at "A" for DS1653/DS3653, C_L = 15 pF total for DS1653/DS3653

S1 at "B" for DS1651/DS3651, C_L = 50 pF total for DS1651/DS3651



TL/F/7528–11

E_{IN} waveform characteristics:

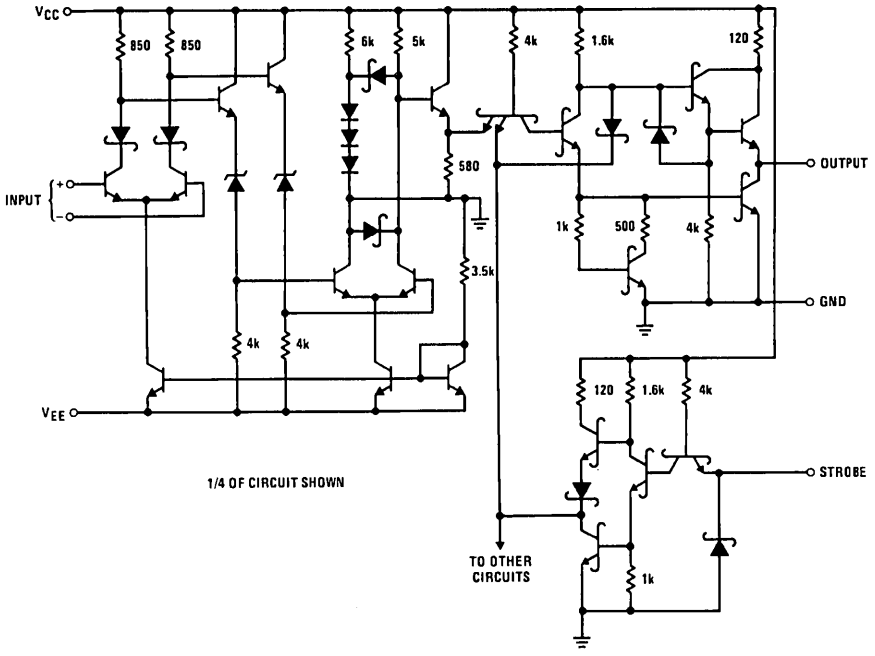
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%

PRR = 1 MHz, duty cycle = 500 ns

FIGURE 3. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

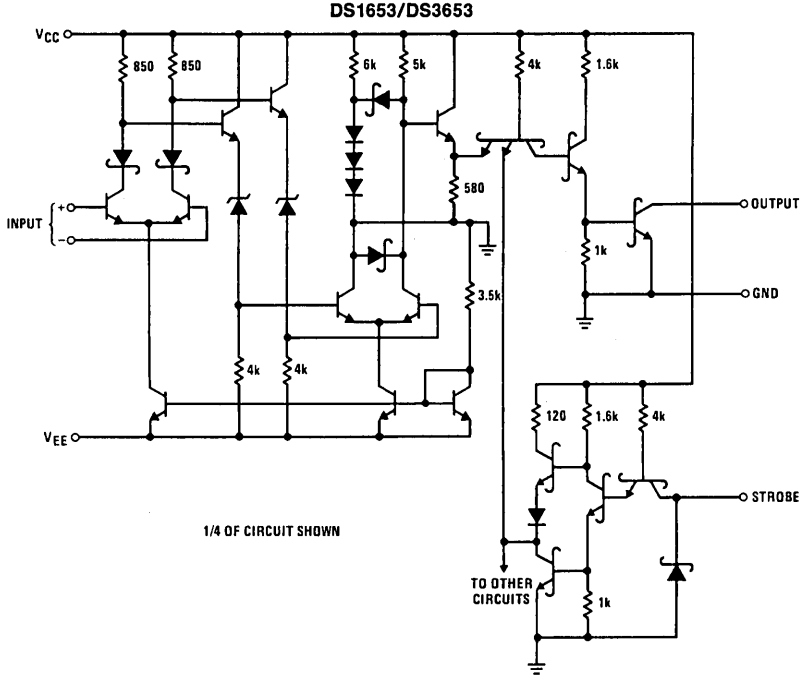
Schematic Diagrams

DS1651/DS3651



TL/F/7528–12

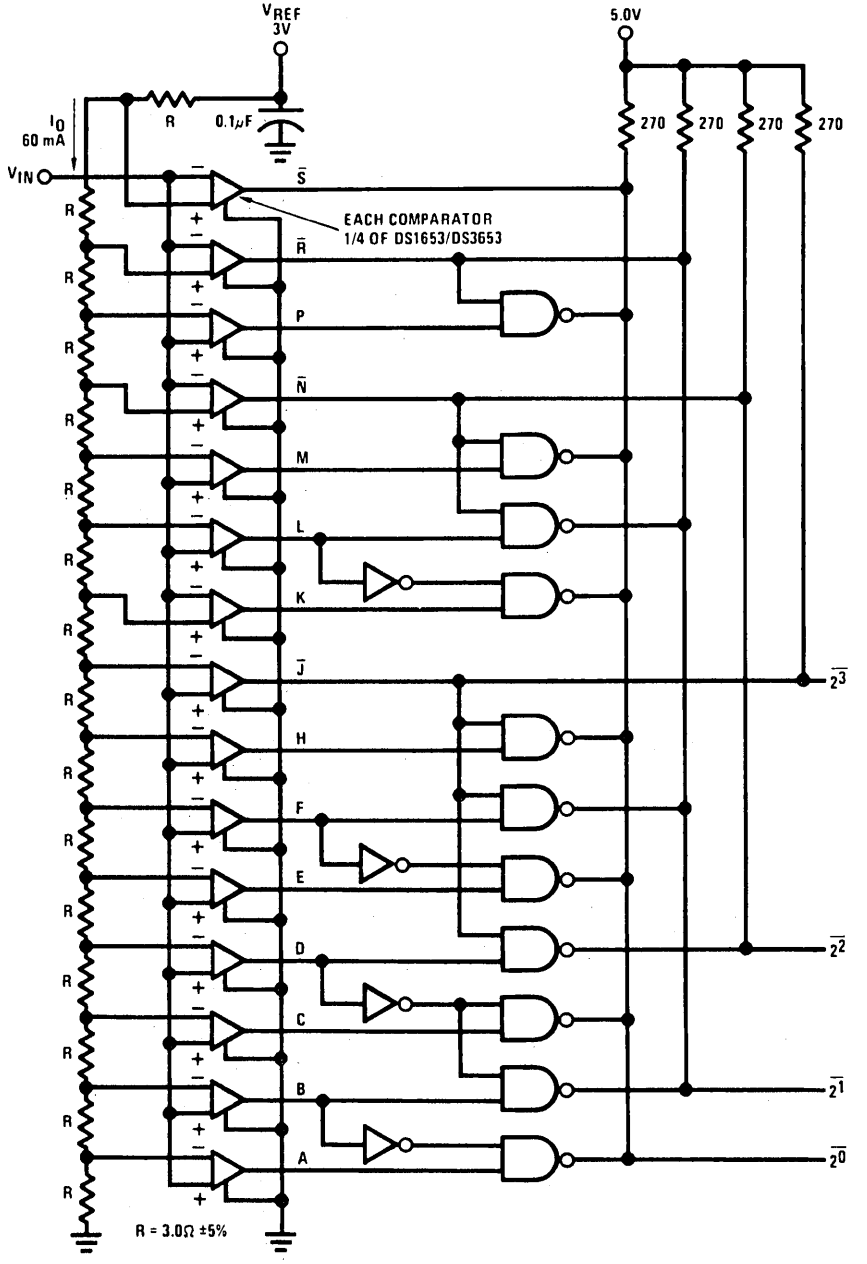
DS1653/DS3653



TL/F/7528–13

Typical Applications

4-Bit Parallel A/D Converter



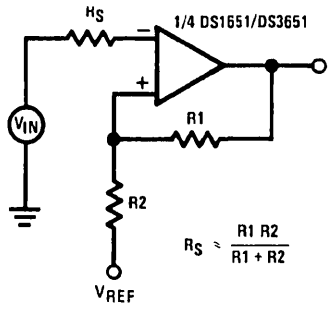
TL/F/7528–14

$\overline{2^0}$ = (Ā + B) (C̄ + D) (Ē + F) (H̄ + J) (K̄ + L) (M̄ + N) (P̄ + R) (S̄)
$\overline{2^1}$ = (B̄ + D) (F̄ + J) (L̄ + N) (R̄)
$\overline{2^2}$ = (D̄ + J) (N̄)
$\overline{2^3}$ = J̄

Conversion time ≃ 50 ns

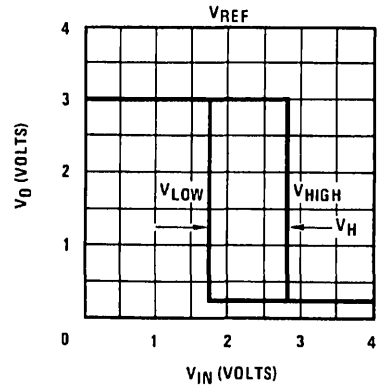
Typical Applications (Continued)

Level Detector with Hysteresis



TL/F/7528–15

Transfer Characteristics and Equations for Level Detector with Hysteresis



TL/F/7528–16

$$V_{HIGH} = V_{REF} + \frac{R2\,[V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

$$V_{LOW} = V_{REF} + \frac{R2\,[V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\,[V_{O(MAX)} - V_{O(MIN)}]$$

4

National Semiconductor Corporation

PRELIMINARY

DS3685 Hex TRI-STATE® Latch

General Description

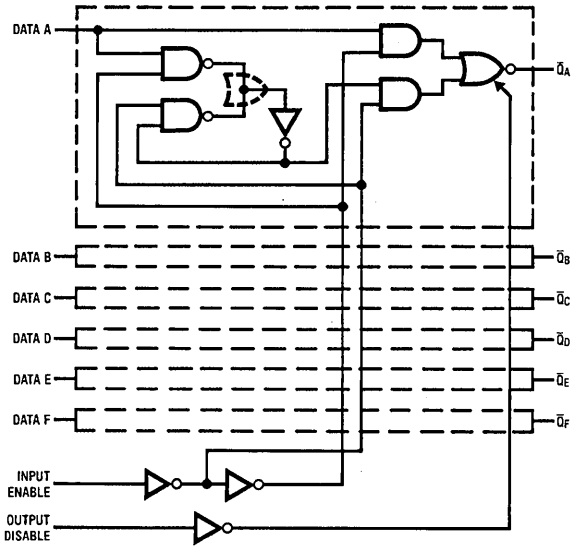
The DS3685 is a hex latch. PNP input transistors are used to reduce input currents, allowing large fan-out to these drivers. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs which allow bus operation.

The circuit employs a fall-through latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits.

Features

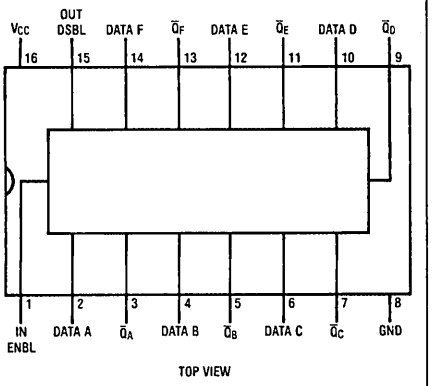
- TTL/LS compatible inputs
- PNP inputs minimize loading
- TRI-STATE outputs
- Fall-through latch design
- Minimum skew

Logic and Connection Diagrams



TL/F/5220–1

Dual-In-Line Package



TL/F/5220–2

Order Number DS3685J or DS3685N
See NS Package J16A or N16A

Truth Table

Input Enable	Output Disable	Data	Output	Operation
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = don't care

Hi-Z = TRI-STATE mode

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Maximum Power Dissipation* at 25°C

Cavity Package	1433 mW
Molded Package	1362 mW

* Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN}(1)$	Logical "1" Input Voltage			2.0			V
$V_{IN}(0)$	Logical "0" Input Voltage					0.8	V
$I_{IN}(1)$	Logical "1" Input Current	V_{IN} = 5.5V, V_{CC} = Max	Enable Inputs		0.1	40	μA
			Data Inputs		0.2	80	μA
$I_{IN}(0)$	Logical "0" Input Current	V_{IN} = 0.5V, V_{CC} = Max	Enable Inputs		−50	−300	μA
			Data Inputs		−100	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA			−0.75	−1.2	V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_{OUT} = 0V, (Note 4)		−40		−100	mA
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min	I_{OH} = −1 mA	2.5	3.5		V
			I_{OH} = −10 μA	2.8	3.8		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 20 mA		0.4	0.5	V
			I_{OL} = 10 μA		0.25	0.35	V
I_{HZ}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Disable = 2V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = 3V = 0V, Enable = 3V				90	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time Low-to-High Level Output	C_L = 15 pF, R_L = 280Ω, *(Figures 1 and 2)*		5.5	7.0	ns
t_{PLH}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 280Ω, *(Figures 1 and 2)*		4.5	6.0	ns
t_{PHL}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 2)*		8		ns
t_{PLH}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 2)*		6		ns
t_{SET-UP}	Set-Up Time on Data Input Before Input Enable Goes Low		10	0		ns
t_{HOLD}	Hold Time on Data Input After Input Enable Goes Low		0			ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 15 pF, *(Figures 1 and 3)*		8.2	15	ns

Switching Characteristics V_{CC} = 5V, T_A = 25°C, unless otherwise noted. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 15 pF, *(Figures 1 and 3)*		17	24	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 15 pF, *(Figures 1 and 4)*		7.7	14	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 15 pF, *(Figures 1 and 4)*		5.5	12	ns

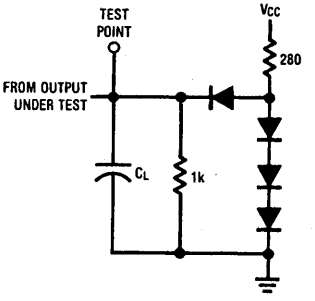
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3685. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

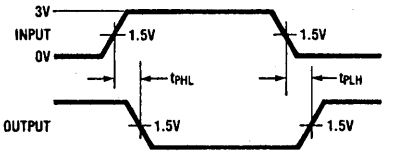
Note 4: Only one output should be shorted at one time.

AC Test Circuit and Switching Time Waveforms



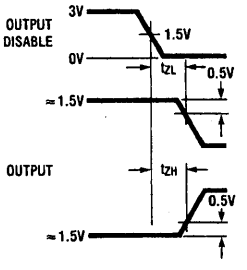
TL/F/5220–3

FIGURE 1



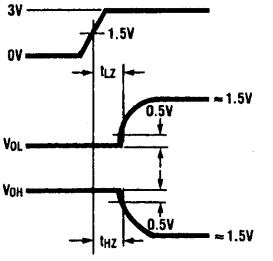
TL/F/5220–4

FIGURE 2



TL/F/5220–5

FIGURE 3

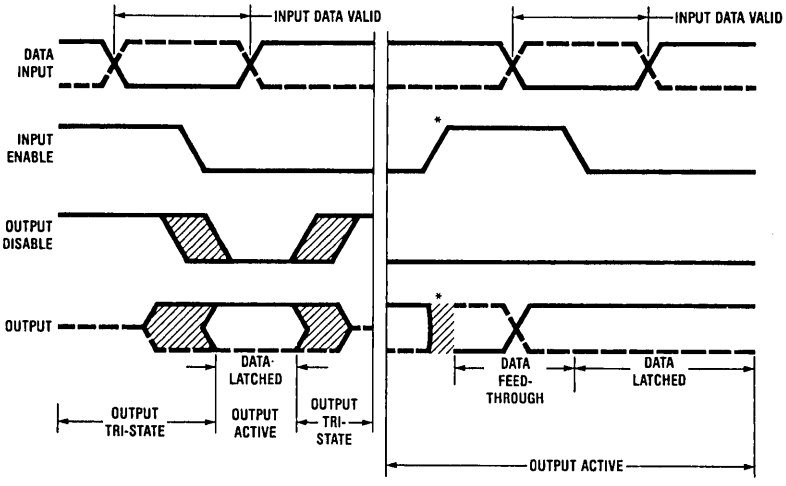


TL/F/5220–6

FIGURE 4

Input characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Operating Waveform



TL/F/5220–7

*When the Input Enable makes a positive transition the output will be indeterminate for a short duration. The positive transition of the Input Enable normally occurs during a don't-care timing state at the output.

National Semiconductor Corporation

DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

General Description

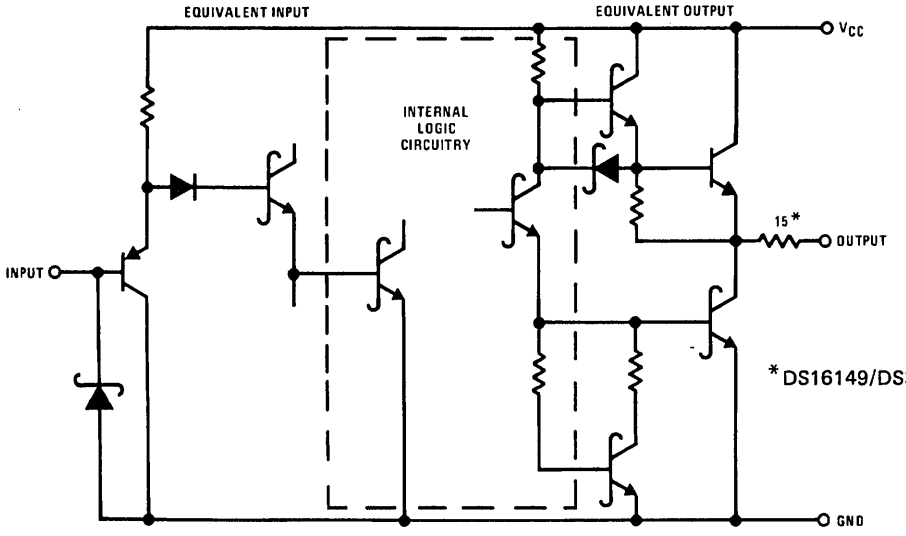
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS16149/DS36149 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



*DS16149/DS36149 only.

TL/F/7553–1

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 m/W°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS16149, DS16179	−55	+125	°C
DS36149, DS36179	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN}(1)$	Logical "1" Input Voltage			2.0			V
$V_{IN}(0)$	Logical "0" Input Voltage					0.8	V
$I_{IN}(1)$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN}(0)$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS16149/DS16179	3.4	4.3		V
			DS36149/DS36179	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS16149/DS16179		0.25	0.4	V
			DS36149/DS36179		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS16149	2.4	3.5		V
			DS16179	2.5	3.5		V
			DS36149	2.6	3.5		V
			DS36179	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS16149		0.6	1.1	V
			DS16179		0.4	0.5	V
			DS36149		0.6	1.0	V
			DS36179		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Disable Inputs = 0V, All Other Inputs = 3V		33	60	mA
			All Inputs = 0V	14		20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
$t_{S\mp}$	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	ns
t_{LH}	Delay from Disable Input to Logical "1"	R_L = 2 kΩ to Gnd, C_L = 50 pF, (*Figure 2*)			15	22	ns
t_{HL}	Delay from Disable Input to Logical "0"	R_L = 2 kΩ to V_{CC}, C_L = 50 pF, (*Figure 3*)			11	18	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

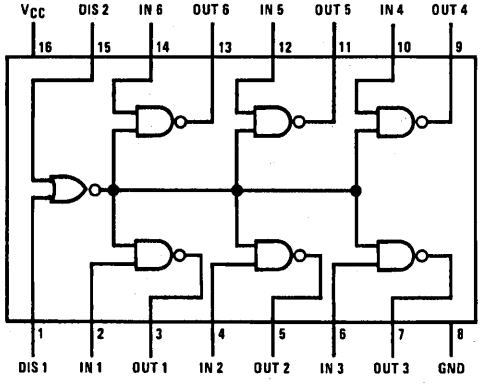
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16149 and DS16179 and across the 0°C to +70°C range for the DS36149 and DS36179. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS16179 and DS36179 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

Connection Diagram

Dual In-Line Package



TL/F/7553–2

Top View

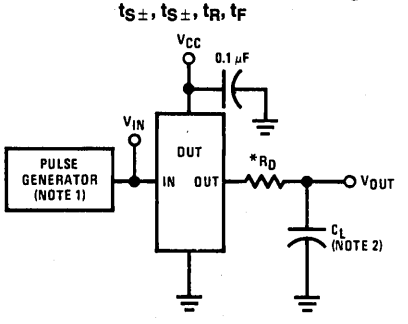
Order Number DS16149J, DS36149J, DS16179J, DS36179J, DS36149N or DS36179N
See NS Package Number J16A or N16A

Truth Table

Disable Input		Input	Output
DIS 1	DIS2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

AC Test Circuits and Switching Time Waveforms



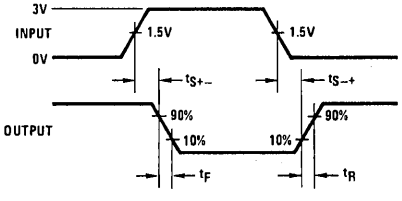


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FIGURE 1

AC Test Circuits and Switching Time Waveforms (Continued)

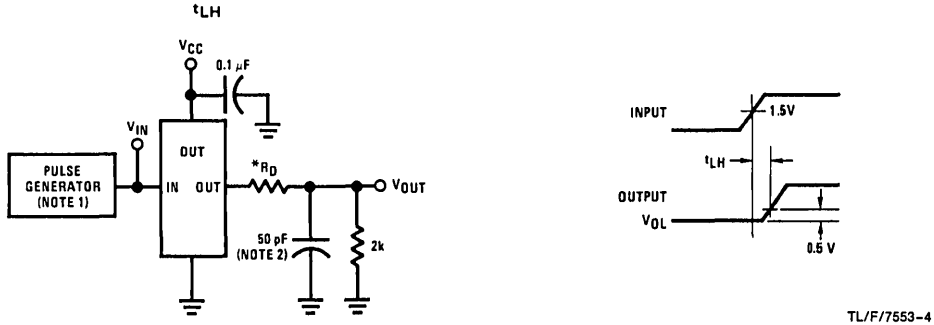


FIGURE 2

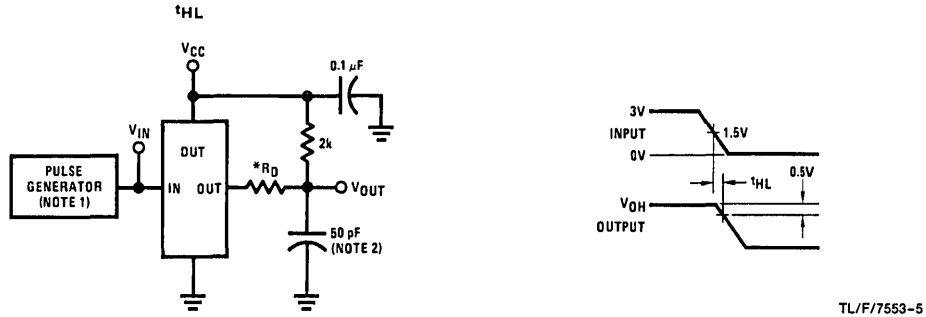


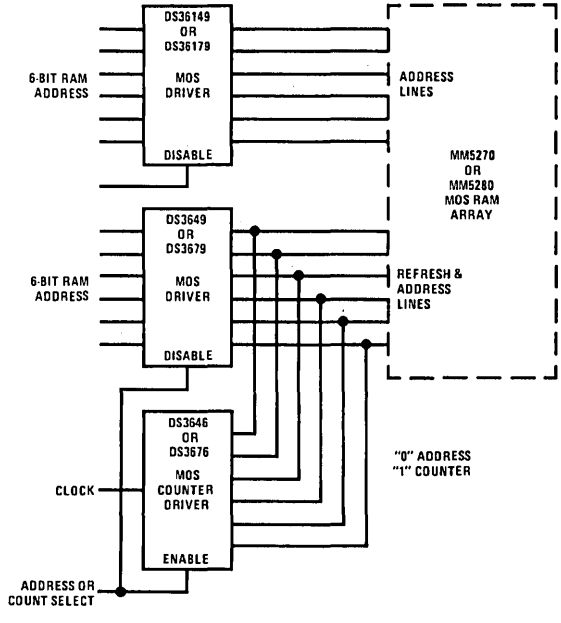
FIGURE 3

*Internal on DS16149 and DS36149

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

Typical Applications



National Semiconductor Corporation

DS75361 Dual TTL-to-MOS Driver

General Description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

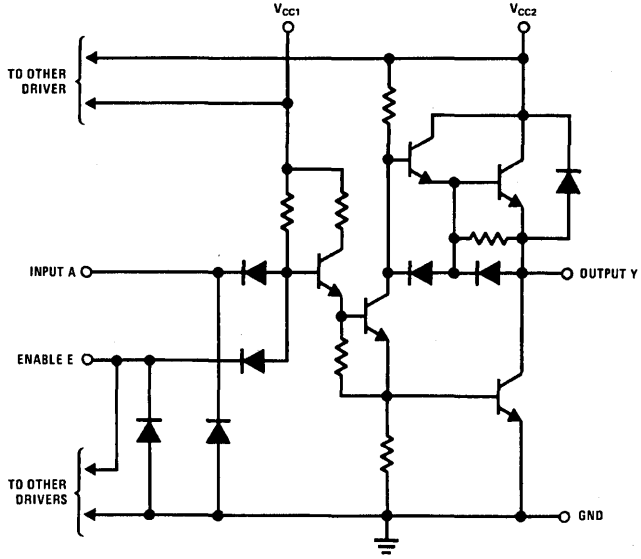
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

Features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams

(1/2 shown)



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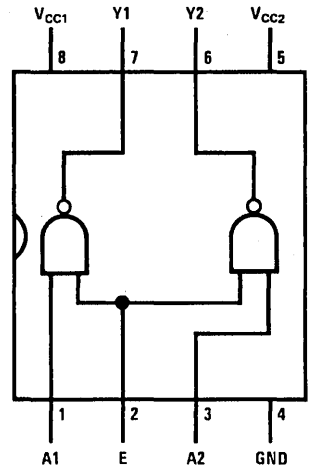
Dual-In-Line Package



TL/F/7557-1

Top View

Order Number DS75361J or DS75361N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage Range of V_{CC1} (Note 1)	−0.5 to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1022 mW
Lead Temperature 1/16 inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 inch from Case for 10 Seconds: N or P Package	200°C

*Derate molded package 8.2 mW/° above about 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC2} = 15V$ to 24V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	$V_{CC1} = 5.25V$, All Inputs at 0V,	$V_{CC2} = 24V$, No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	$V_{CC1} = 5.25V$, All Inputs at 5V,	$V_{CC2} = 24V$, No Load		16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, All Inputs at 5V,	$V_{CC2} = 24V$, No Load			0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$.

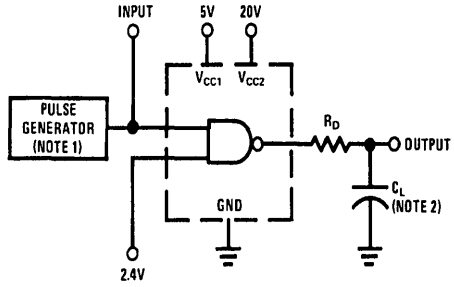
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between the A input of either driver and the common E input.

Switching Characteristics V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω *(Figure 1)*		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
tPLH	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

AC Test Circuit and Switching Time Waveforms



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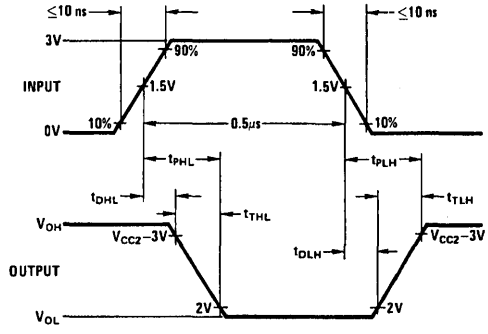


TL/F/7557–5

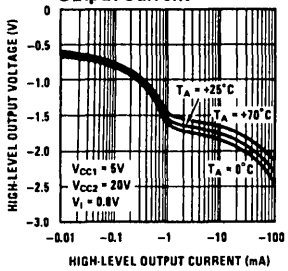
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

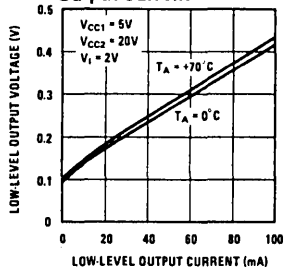
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

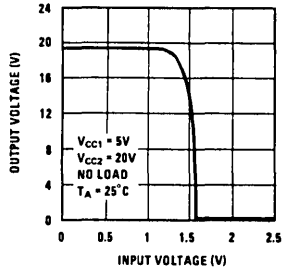
High-Level Output Voltage vs Output Current



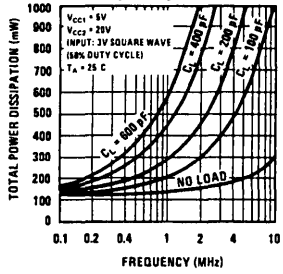
Low-Level Output Voltage vs Output Current



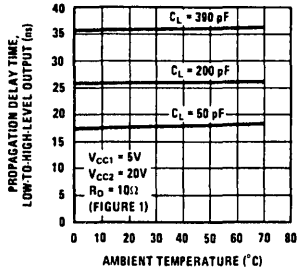
Voltage Transfer Characteristics



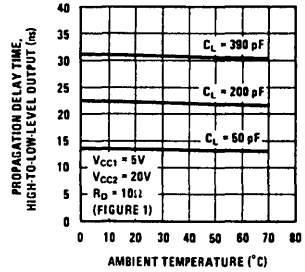
Total Dissipation (Both Drivers) vs Frequency



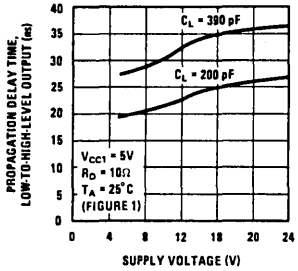
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



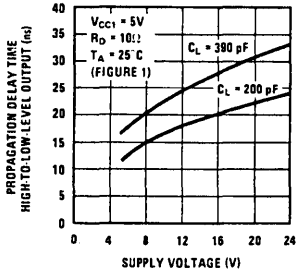
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



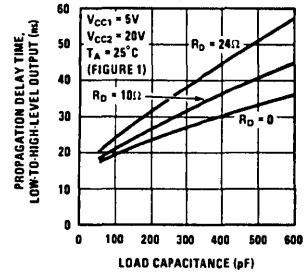
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



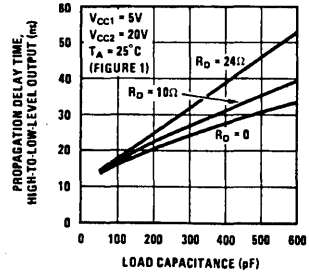
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



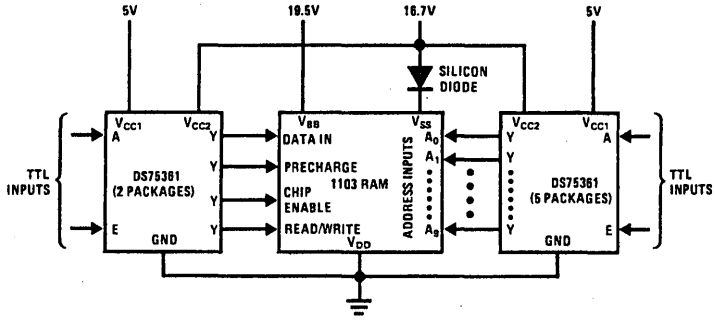
Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



TL/F/7557–2

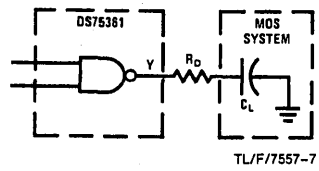
Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.



TL/F/7557-6

FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM



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Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\ mA}{2}\right) + (20V)\left(\frac{0\ mA}{2}\right) \right](0.6) + \left[(5V)\left(\frac{16\ mA}{2}\right) + (20V)\left(\frac{7\ mA}{2}\right) \right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

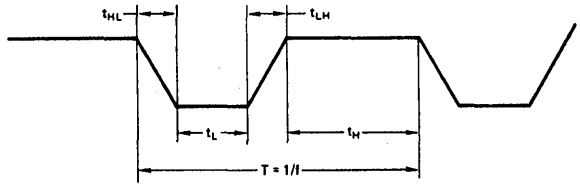
$P_{C(AV)} \approx$ (200 pF) $(19.2V)^2$ (2 MHz)

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\ (47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.



TL/F/7557-8

FIGURE 4. Output Voltage Waveform

National Semiconductor Corporation

PRELIMINARY

DS75365 Quad TTL-to-MOS Driver

General Description

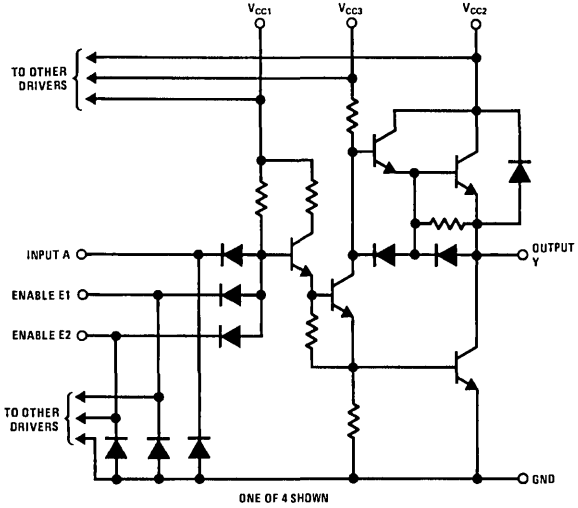
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} to the V_{CC2} pin.

Features

- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over side range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



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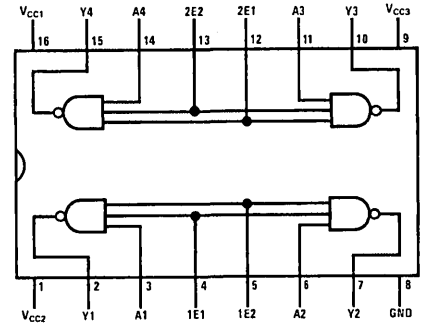
Dual-In-Line Package



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Top View
Positive Logic: $Y = \overline{A \bullet E1 \bullet E2}$

Order Number DS75365J or DS75365N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
nput Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\ \mu A$		$V_{CC2} - 0.3$	$V_{CC2} - 0.1$		V
		$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 1.2$	$V_{CC2} - 0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA

Electrical Characteristics (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-By Condition	V_{CC1} = 0V, V_{CC2} = 24V V_{CC3} = 24V, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-By Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for T_A = 25°C and V_{CC1} = 5V and V_{CC2} = 20V and V_{CC3} = 24V.

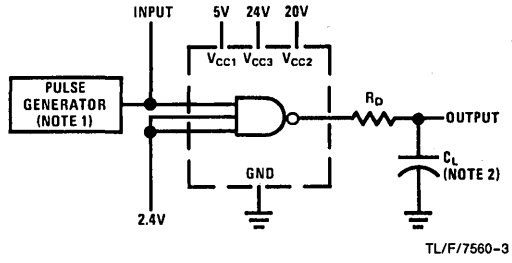
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF R_D = 24Ω (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms



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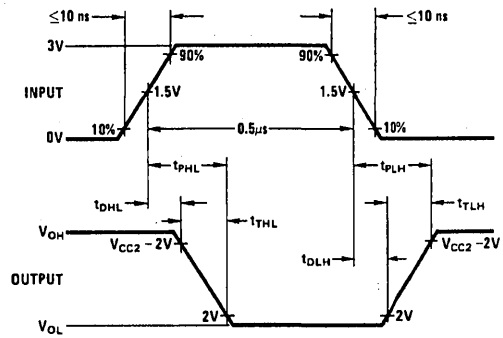

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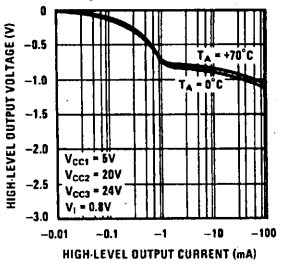
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 58Ω.

Note 2: C_L includes probe and jig capacitance.

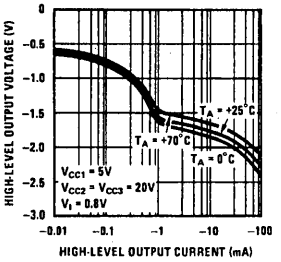
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

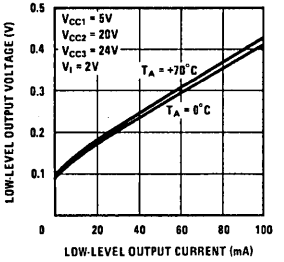
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current



Low-Level Output Voltage Output Current



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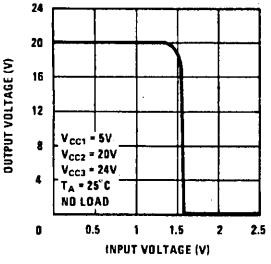
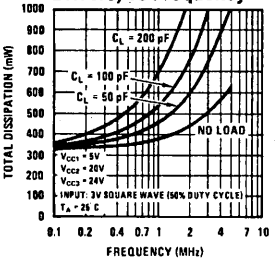
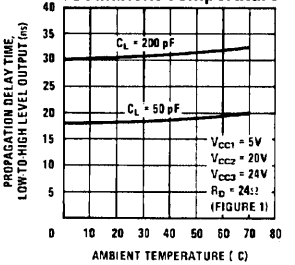
Voltage Transfer Characteristics



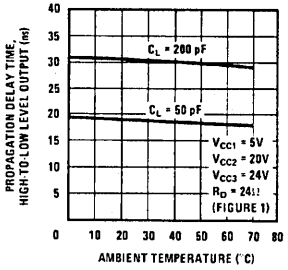
Total Dissipation (All Four Drivers) vs Frequency



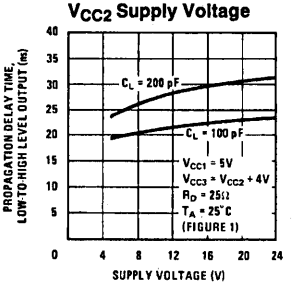
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



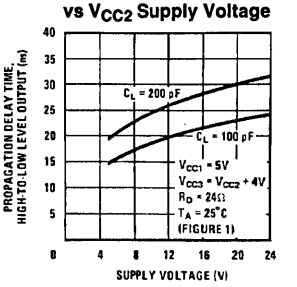
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



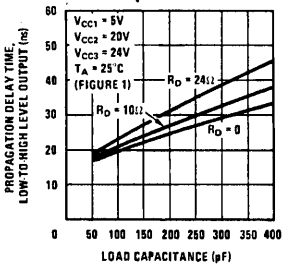
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



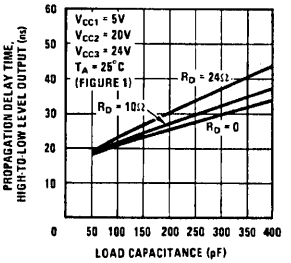
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



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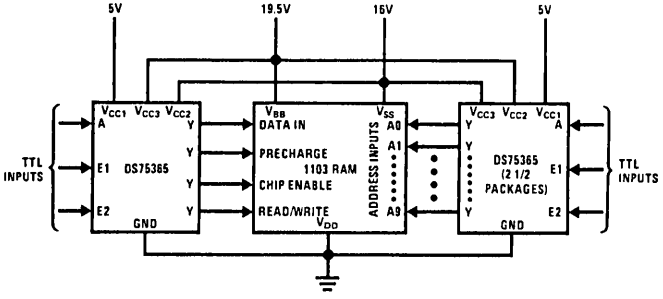

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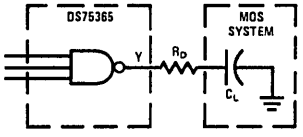
FIGURE 2. Interconnection of DS75365 Devices with 1103-Type Silicon-Gate MOS RAM

Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω (*Figure 3*).



Note: $R_D \cong 10\Omega$ to 30Ω (Optional)

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FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75365 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \cong C V C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \cong$ (100 pF) $(19.9V)^2$ (2 MHz)

$P_{C(AV)} \cong$ 79 mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \cong 4\,(58 + 79)$

$P_{T(AV)} \cong$ 548 mW typical for total package.

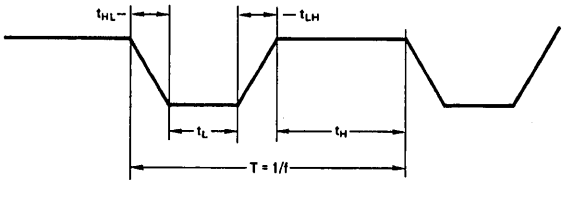

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FIGURE 4. Output Voltage Waveform

Applying Modern Clock Drivers to MOS Memories

National Semiconductor
Application Note 76
B. Siegel
M. Scott

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input waveforms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAMs (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage gold doped process utilizing a collector sinker to minimize $V_{CE\ SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

Parameter	Conditions ($V^+ - V^-$) = 17V	Value	Units
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022 μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001 μF, R0 = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1 mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

Parameter	Conditions ($V^+ - V^-$) = 17V	Value	Units
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001 μF, R_{IN} = 0Ω	7.5	ns
t_r	R0 = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1 mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent—derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \qquad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

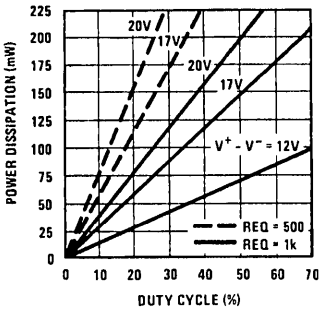
Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^- / I_{S(ON)} \qquad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time} + \text{"OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1*. For example if $V^+ = +5V$, $V^- = -12V$, Req = 500Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.



TL/F/7322–1

FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

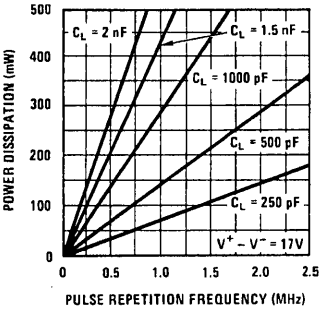
$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \qquad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2*. Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.



TL/F/7322–2

FIGURE 2. P_{AC} vs PRF

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \qquad (5)$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For $V^+ = 5V$, $V^- = -12V$, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$C_L \leq 1340$ pF (each driver)

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or approximately 20 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2* and *AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver; and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise".

Power Supply Decoupling

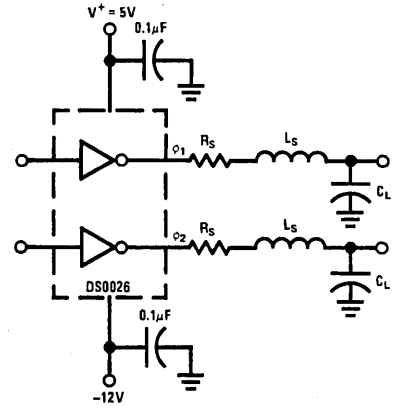
Although power supply decoupling is a wide spread and accepted practice, the question often rises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1 μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long or has significant dc resistance, the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3*. In this instance, a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$



TL/F/7322–3

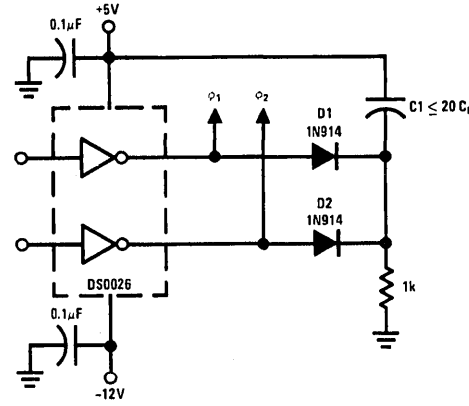
FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\ R_S\ C_L \qquad (7)$$

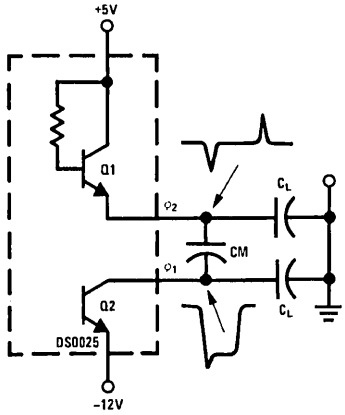
One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2\ fC_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.



TL/F/7322–4

FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

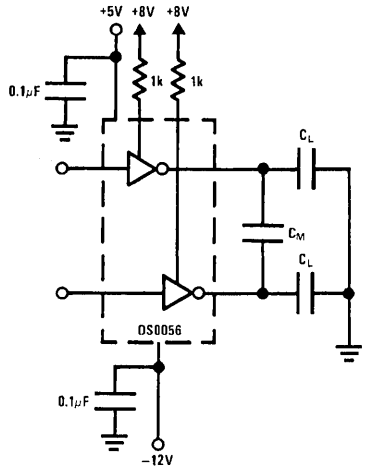


TL/F/7322–5

FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.



TL/F/7322–6

FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

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1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.
2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.
3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.
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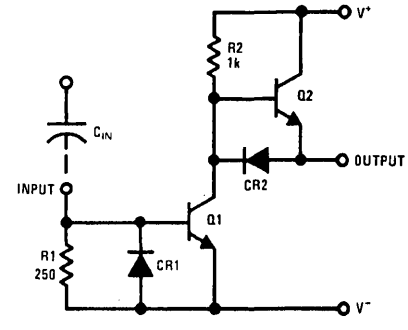
6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.
7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.
8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure 7*. With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.



TL/F/7322–7

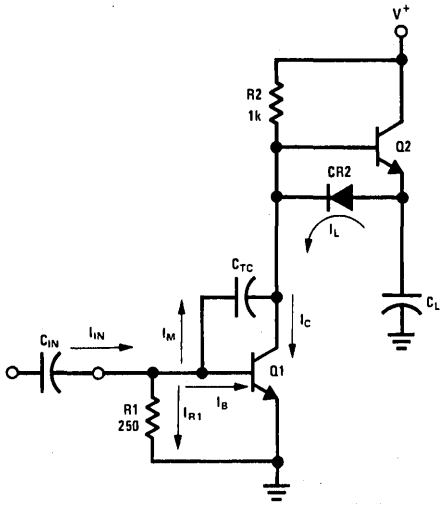
FIGURE 7. DS0025 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure 8*, the input current



TL/F/7322-8

FIGURE 8. Rise Time Model for the DS0025

must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \quad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M \gg I_{R1} \text{ and } I_B \gg I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \quad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \quad \text{(AI-3)}$$

where:

$$I_L = C_L\frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, and AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1} + 1)] = h_{FEQ1} I_{IN} \quad \text{(AI-4)}$$

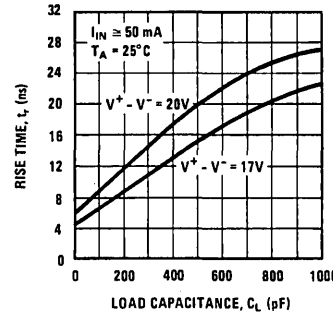
or

$$t_r \cong \frac{[C_L + (h_{FEQ1} + 1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \quad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 pF respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\,(17\text{V})}{(50\text{ mA})\,(20)}$$

or 21 ns may be expected for $V^+ = 5.0\text{V}$, $V^- = -12\text{V}$. *Figure 9* gives rise time for various values of C_L.

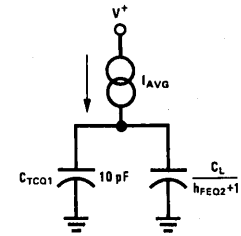


TL/F/7322-9

FIGURE 9. Rise Time vs C_L for the DS0025

Fall Time Considerations

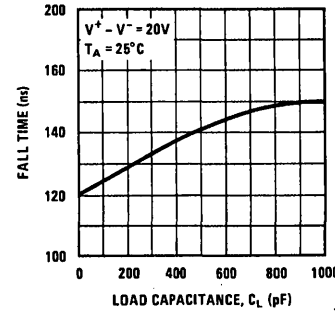
The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated



TL/F/7322-10

FIGURE 10. Fall Time Equivalent Circuit

with the circuit of *Figure 10*. In actual practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure 11* shows t_f as function of C_L.



TL/F/7322-11

FIGURE 11. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \quad \text{(AI-6)}$$

or

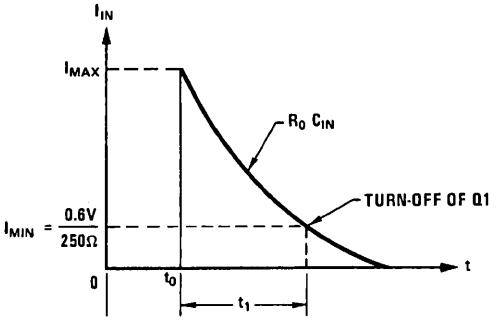
$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \quad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.



TL/F/7322–12

FIGURE 12. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure 12.* I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below $V_{BE}/R1$ or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0\, C_{IN}} \quad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \quad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \quad \text{(AI-10)}$$

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)(2200\text{ pF}) \ln$$

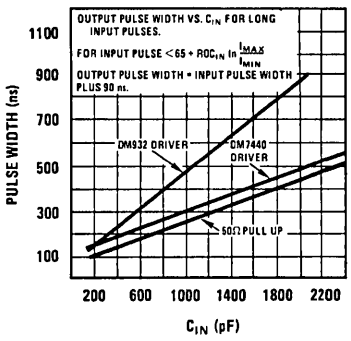
$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure 13.* For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

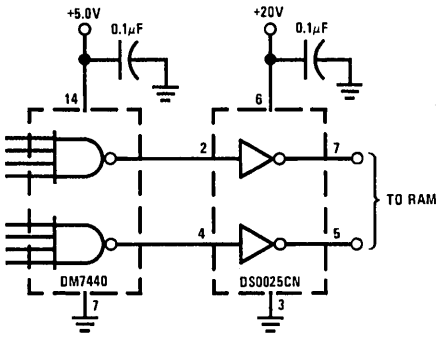
The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure 14* driving the address or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DH0034 may be employed as shown in *Figure 15.* Finally, the level shift may be accomplished using PNP transistors are shown in *Figure 16.*



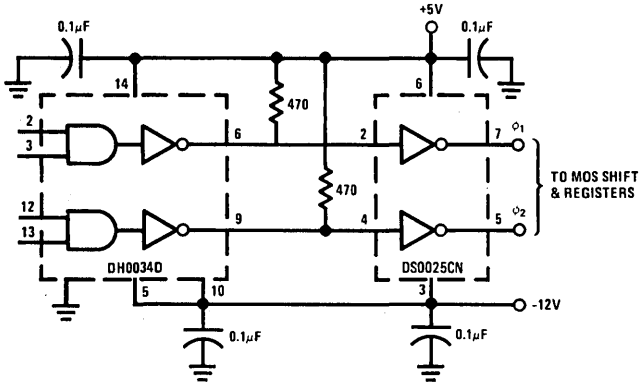
TL/F/7322–13

FIGURE 13. Output PW Controlled by C_{IN}



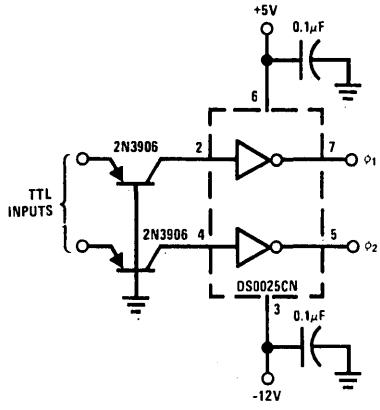
TL/F/7322–14

FIGURE 14. DC Coupled DS0025 Driving 1103 RAM



TL/F/7322-15

FIGURE 15. DC Coupled Clock Driver Using DH0034



TL/F/7322-16

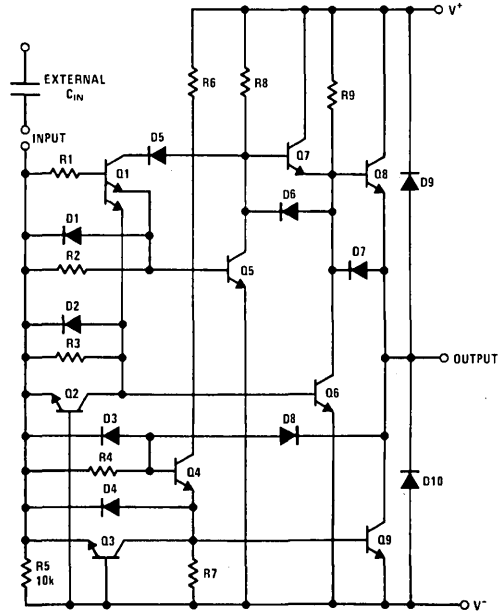
FIGURE 16. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure 17.* The device is typically AC coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q4, Q5, and Q6 are "OFF" allowing Q7 and Q8 to come "ON." R9 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q5 and Q6 turning them "ON." Simultaneously, Q7 and Q8 are snapped "OFF." As the input voltage rises (to about 1.2V), Q1 and Q4 turn-on. Multiple emitter transistor Q1 provides additional base drive to Q5 and Q6 assuring their complete and rapid turn-on. Since Q7 and Q8 were rapidly turned "OFF" minimal power supply current spiking will occur when Q9 comes "ON."



TL/F/7322-17

FIGURE 17. DS0026 Schematic (One-Half Circuit)

Q4 now provides sufficient base drive to Q9 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diodes D6 and D7 prevent avalanching Q7's and Q8's base-emitter junction as the collectors of Q5 and Q6 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V^-.

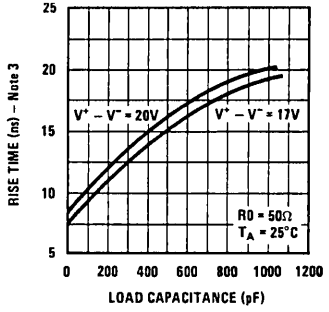
When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q2 and Q3 turn-on, pulling stored base charge out of Q4 and Q9 assuring their rapid turn-off. With Q1, Q5, Q6 and Q9 "OFF," Darlington connected Q7 and Q8 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\,\Delta V \qquad \text{(AII-1)}$$

For $C_L = 1000$ pF, $V^+ = 5.0V$, $V^- = -12V$, $t_r \cong 21$ ns. *Figure 18* shows DS0026 rise times vs C_L.



TL/F/7322–18

FIGURE 18. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

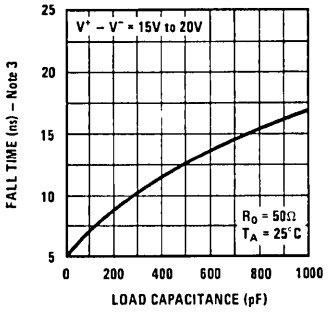
$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3
= 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)\,(h_{FEQ4} + 1)$
$\cong 500$

For the values given and $C_L = 1000$ pF, $t_f \cong 17.5$ ns. *Figure 19.* gives t_f for various values of C_L.

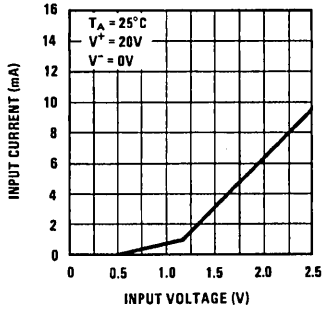


TL/F/7322–19

FIGURE 19. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure 20.* There is breakpoint at $V_{IN} \cong 0.6V$ which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).



TL/F/7322–20

FIGURE 20. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width ≅ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

$$t_1 = R0 C_{IN} \ln \frac{I_{MAX}}{I''_{MIN}} \qquad \text{(AII-3)}$$

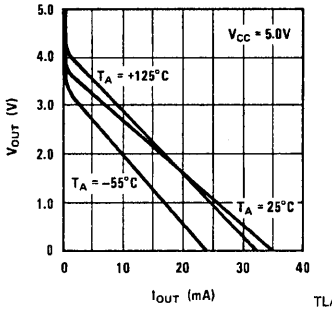
or

$$C_{IN} = \frac{t_1}{R0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

4

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure 21* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega)\ln\frac{20\text{ mA}}{1\text{ mA}}} = 560\text{ pF}$$

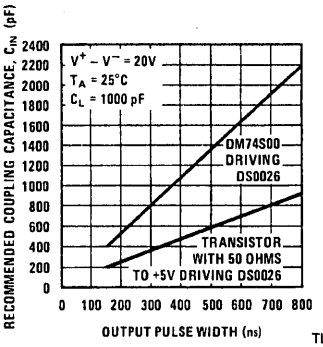


TL/F/7322–21

FIGURE 21. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure 22*.

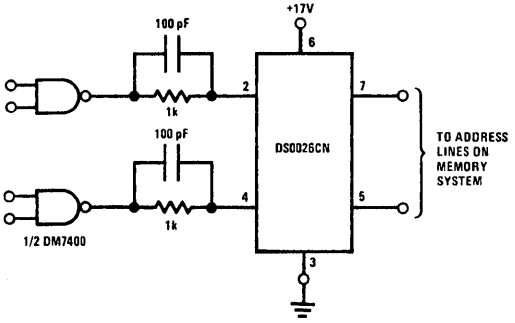


TL/F/7322–22

FIGURE 22. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

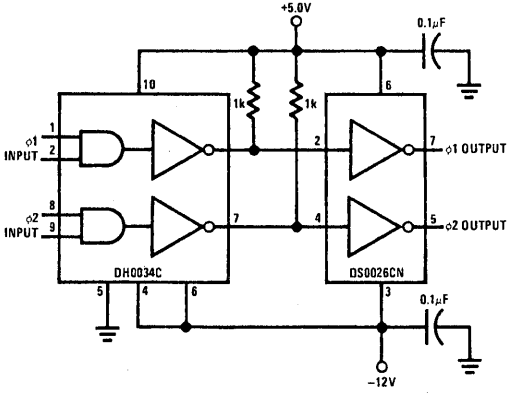
The DS0026 may be applied in direct coupled applications. *Figure 23* shows the device driving address or pre-charge lines on an MM1103 RAM.



TL/F/7322–23

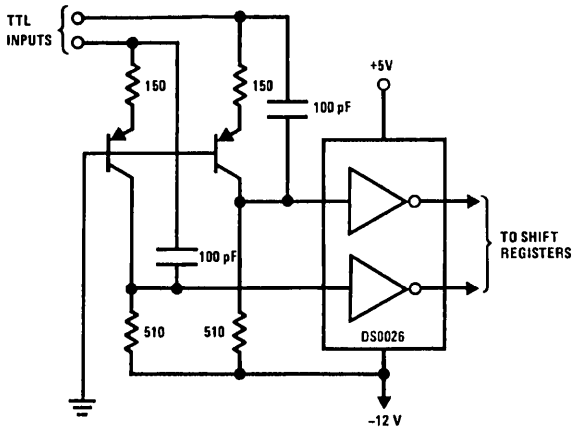
FIGURE 23. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuits of *Figure 24* or *25* are recommended.



TL/F/7322–24

FIGURE 24. Transistor Coupled MOS Clock Driver



TL/F/7322–25

FIGURE 25. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007	Direct coupled, single phase, TTL compatible clock driver.
MH0009	Two phase, direct or ac coupled clock driver.
MH0012	10 MHz, single phase direct coupled clock driver.
MH0013	Two phase, ac coupled clock driver.
DS0025C	Low cost, two phase clock driver.
DS0026C	Low cost, two phase, high speed clock driver.
DS3671	Dual bootstrapped MOS driver.
DS3674	Quad MOS clock driver.
DS75361	Dual TTL-to-MOS driver.
DS75365	Quad TTL-to-MOS driver.

MOS RAM Memory Address and Precharge Drivers

DS0025C	Dual address and precharge driver.
DS0026C	Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034	Dual high speed TTL to negative level converter.
DS8800	Dual TTL to negative level converter.
DS8810/ DS8812/ DS8819	Open collector TTL to positive high level MOS converter gates.
DS88L12	Active pull-up TTL to positive high level MOS converter gates.
DS3645/DS3675	Hex TRI-STATE® MOS driver.
DS3647A	Quad TRI-STATE MOS driver I/O register.
DS3648/DS3678	TRI-STATE MOS driver multiplexer.
DS3649/DS3679	Hex TRI-STATE MOS driver.
DS36149/ DS36179	Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS75107, DS75207	Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM309, LM340 Series	Positive regulators.
LM320 Series	Negative regulators.
LM325 Series	Dual ± regulators.

Section 5

Physical Dimensions/ Appendices

Section Contents

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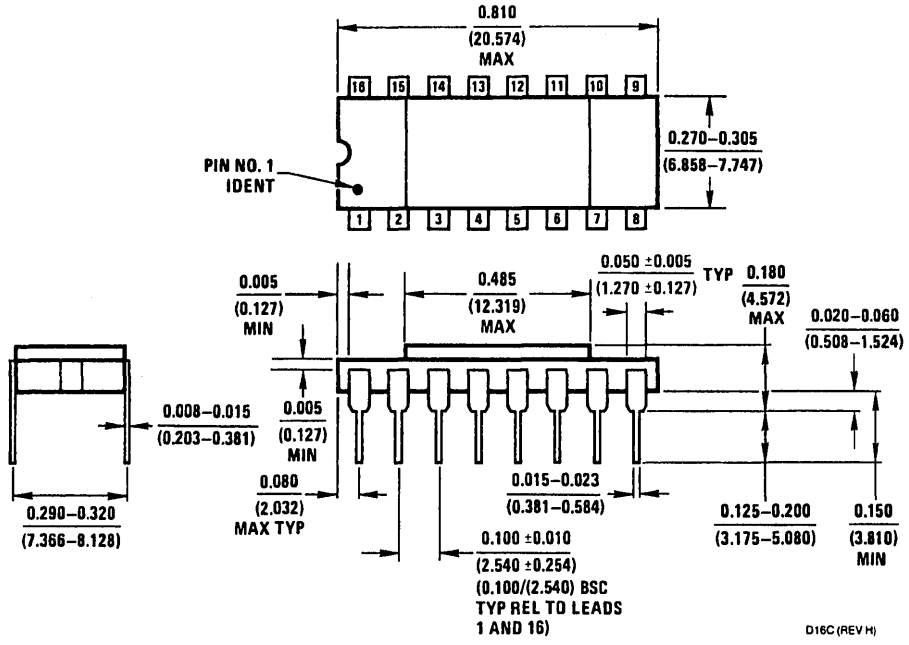

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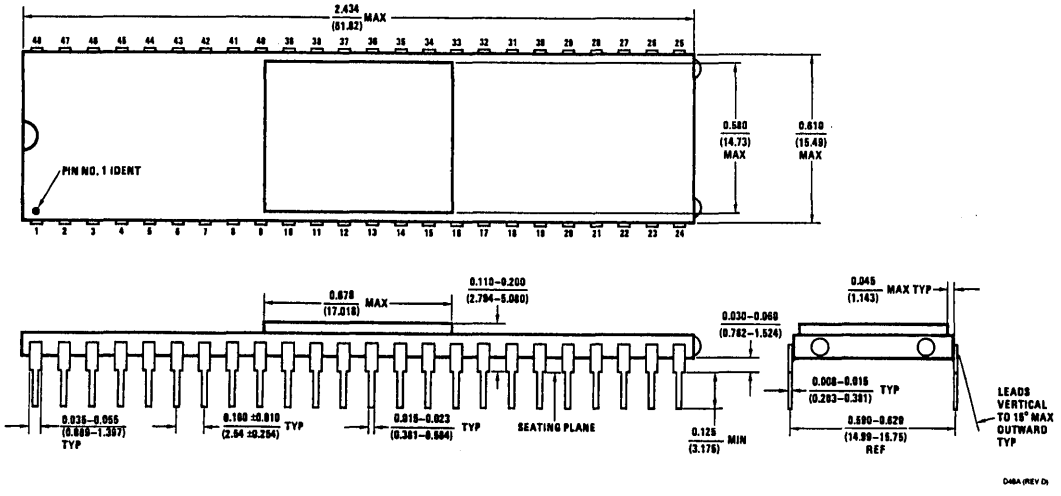

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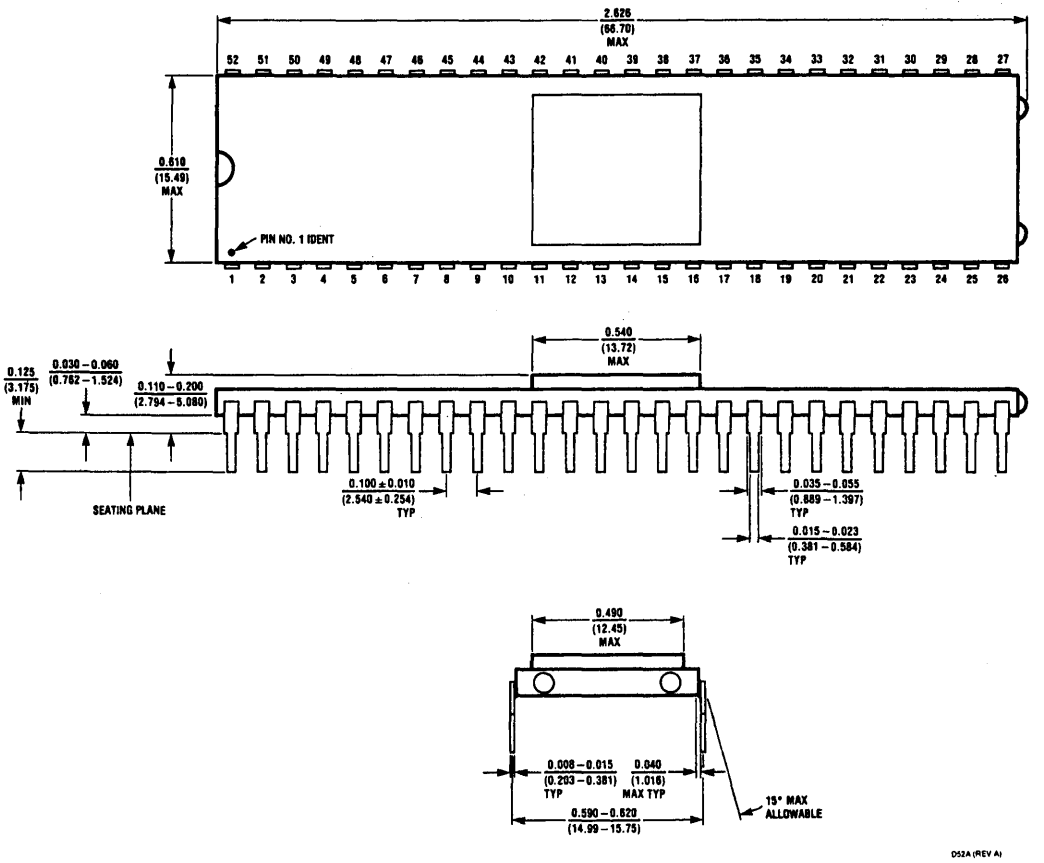

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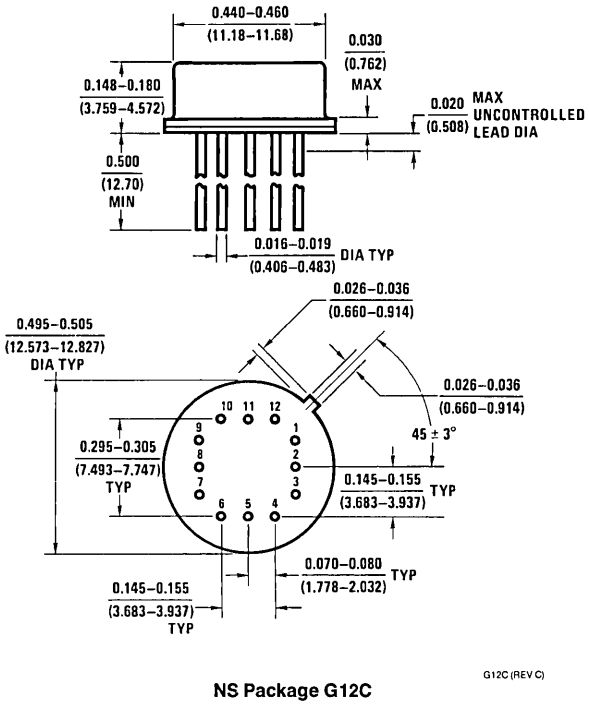

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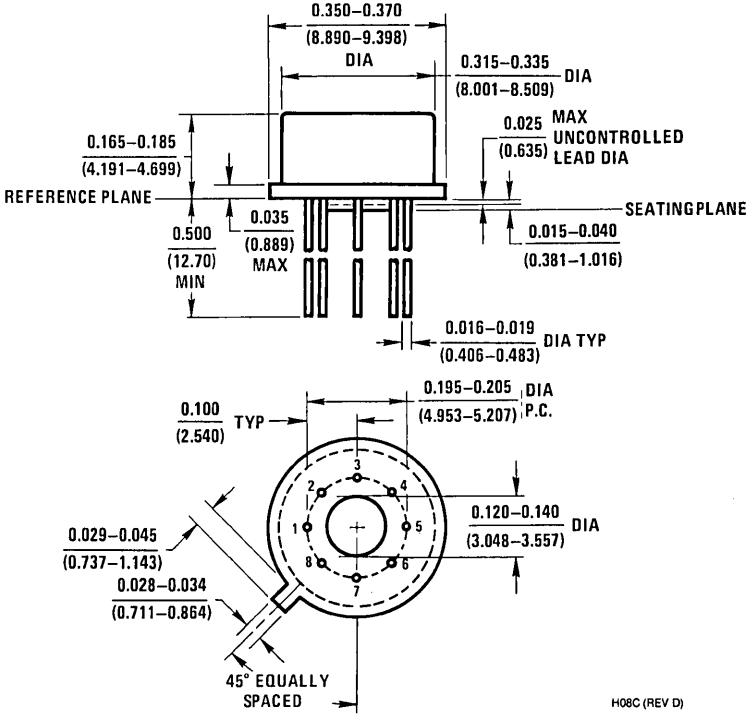

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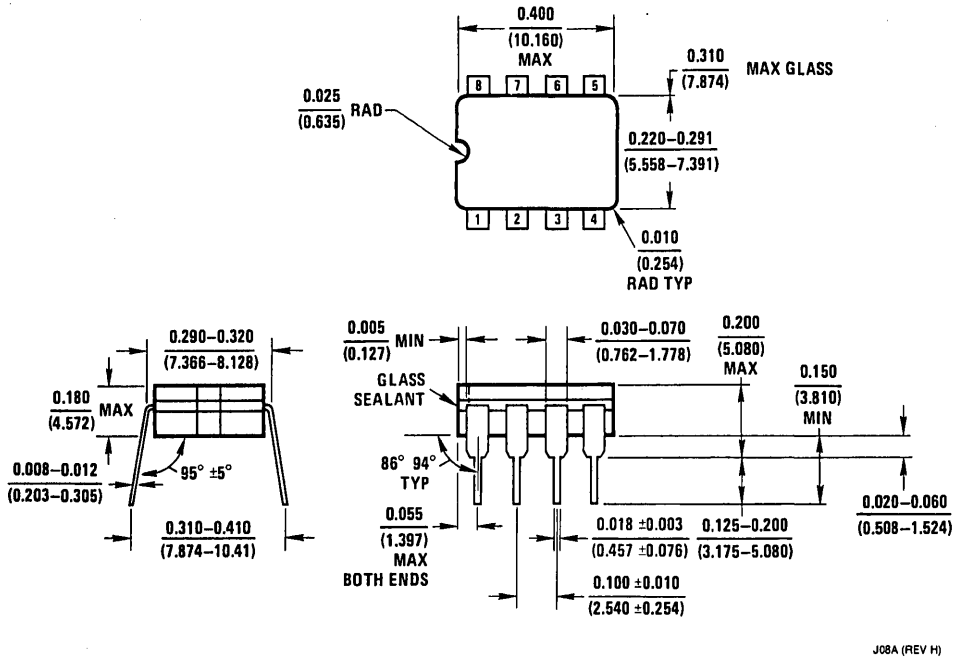

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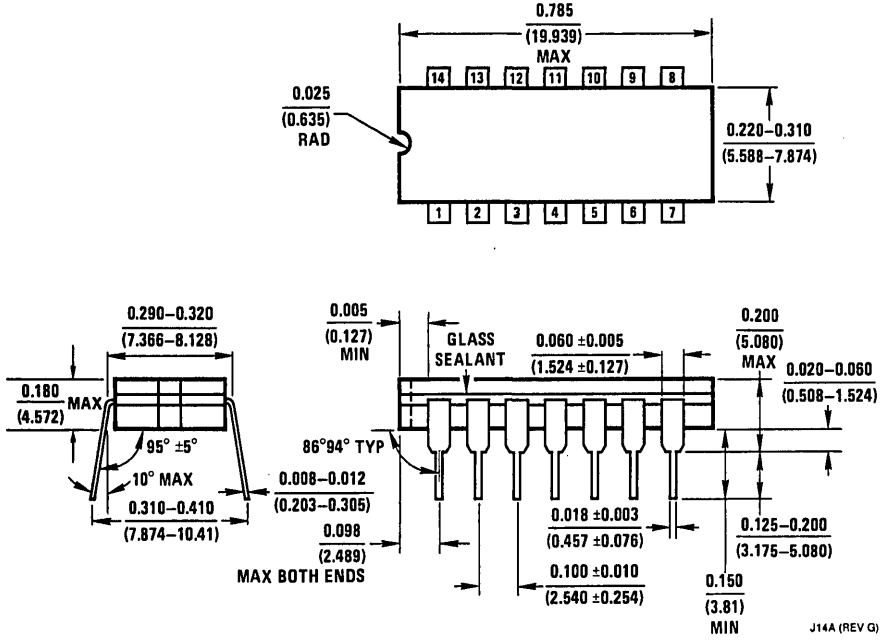

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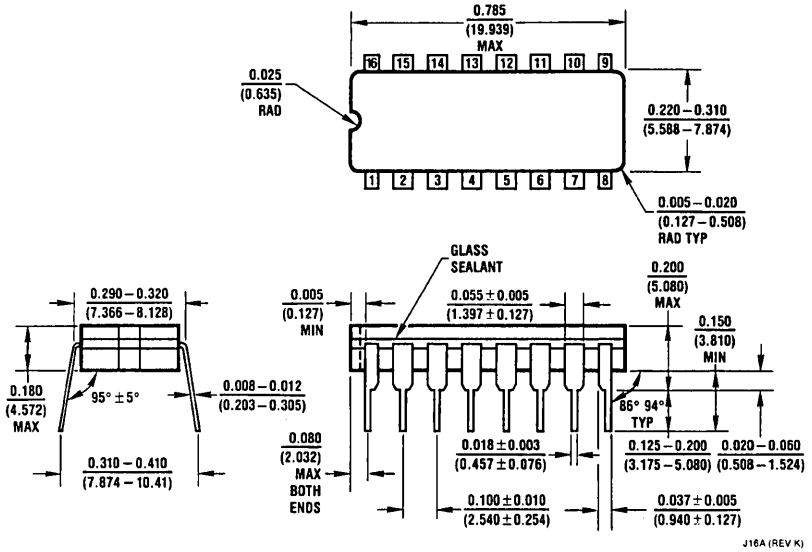

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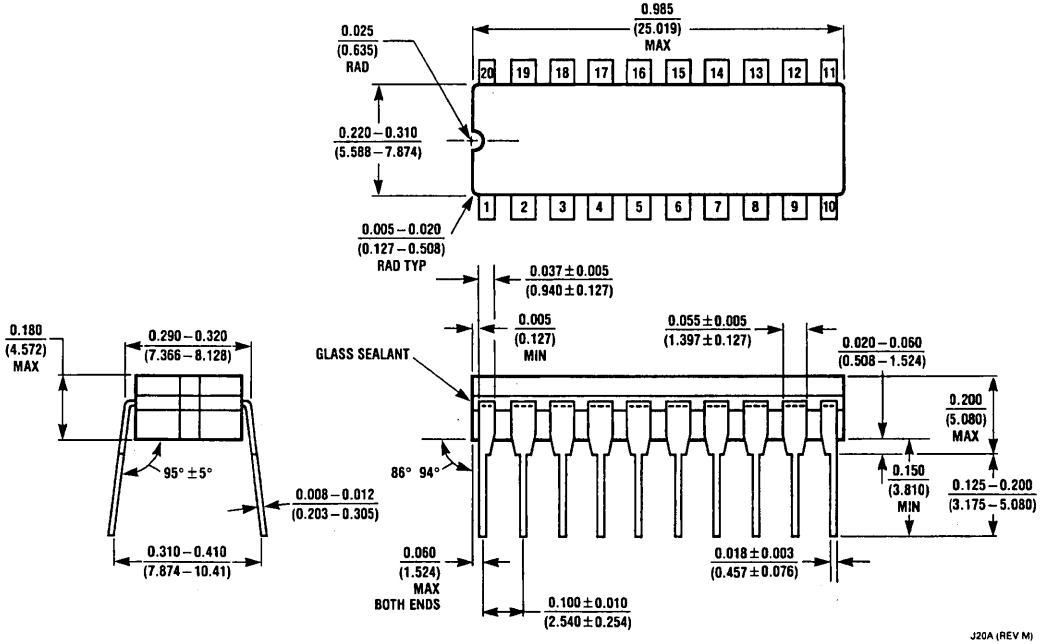

NS Package J20A

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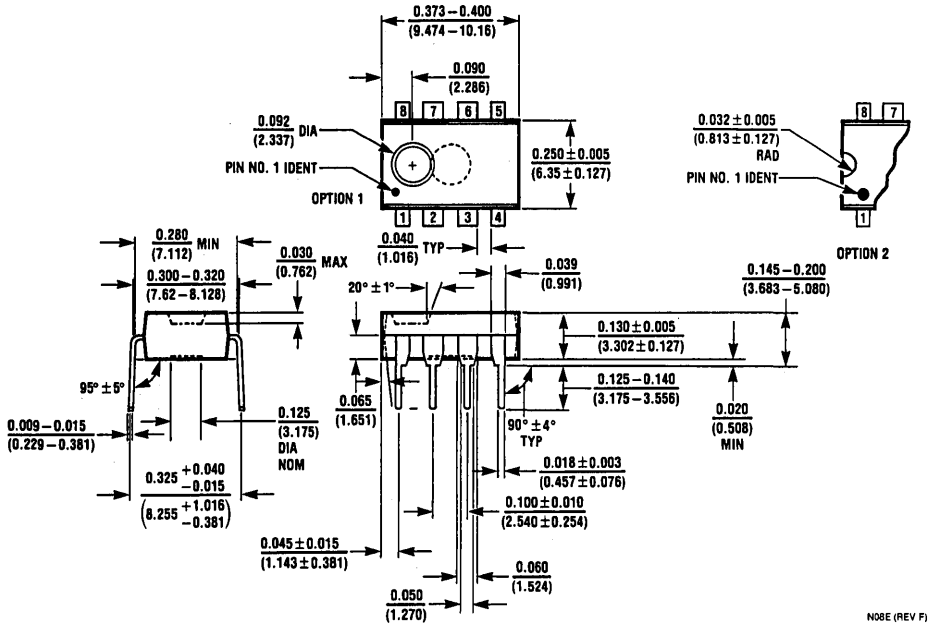

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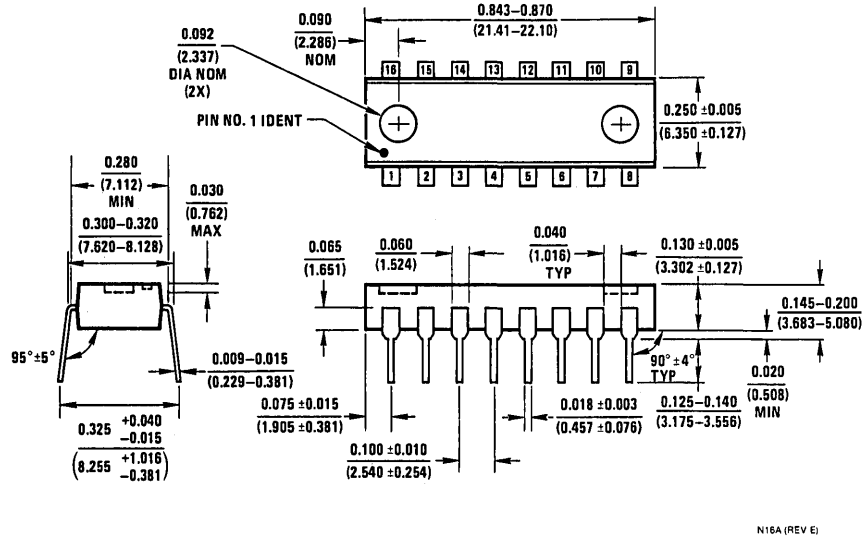

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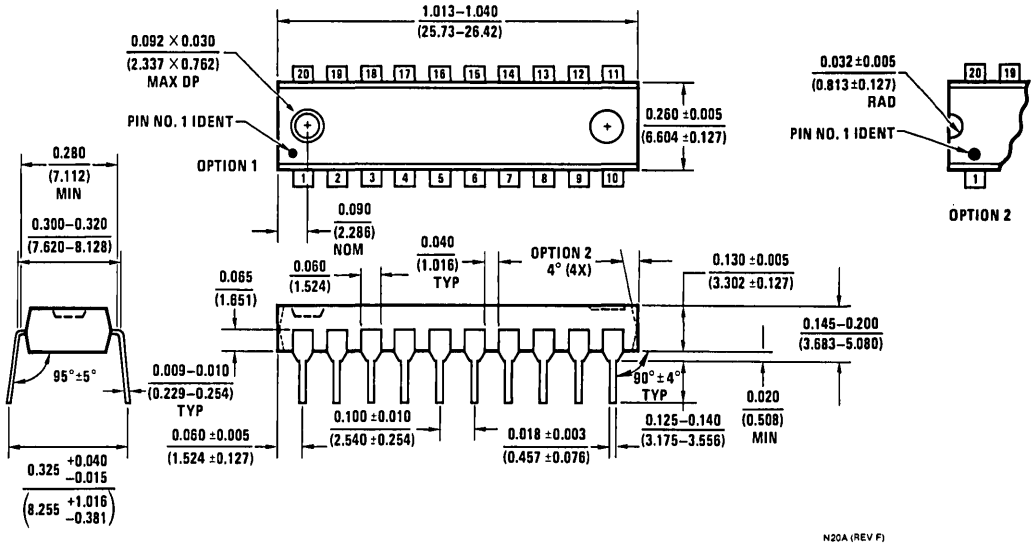

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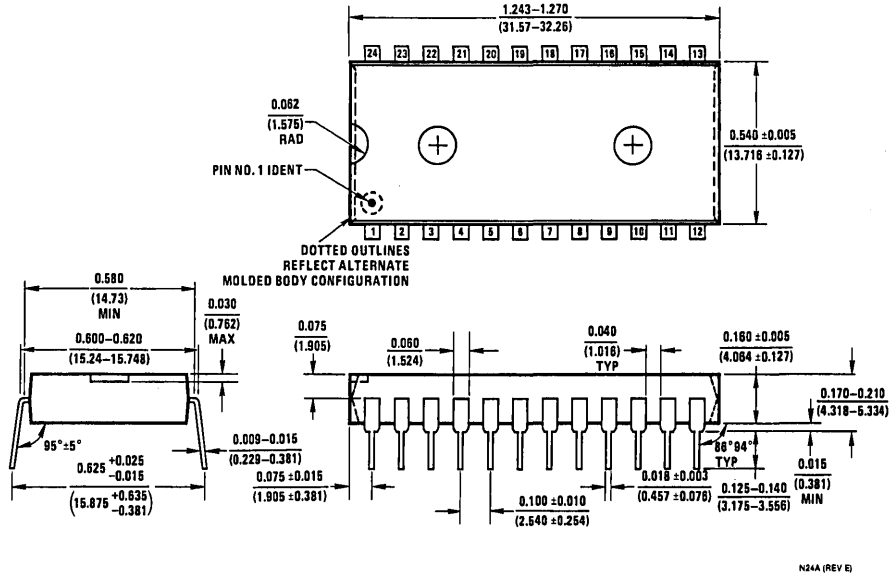

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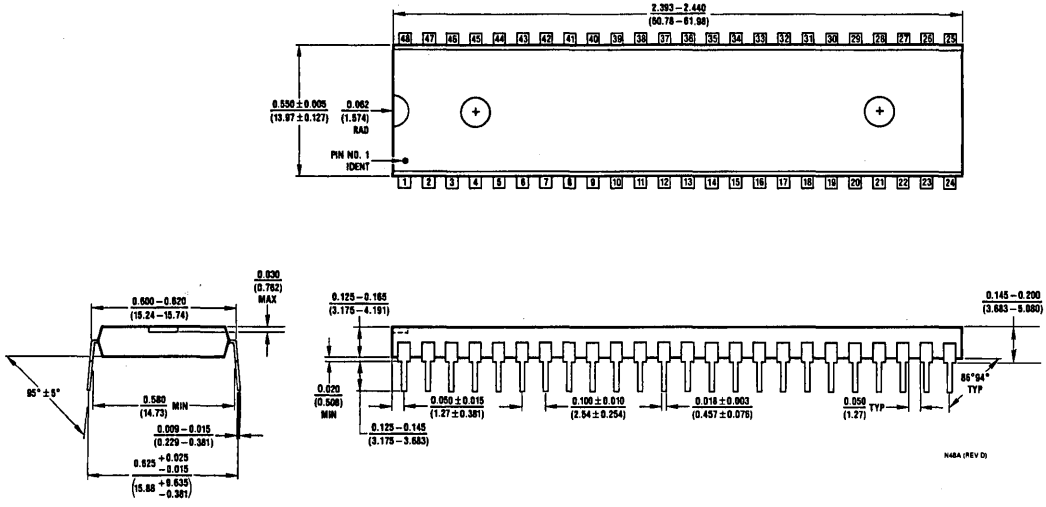

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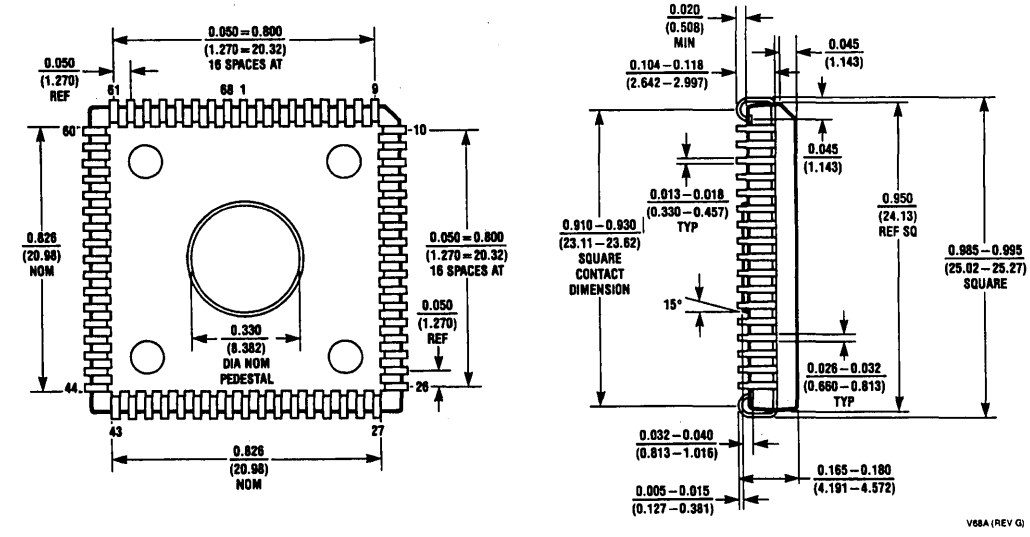

NS Package V68A

Solder Tail Sockets

Dimensioning:
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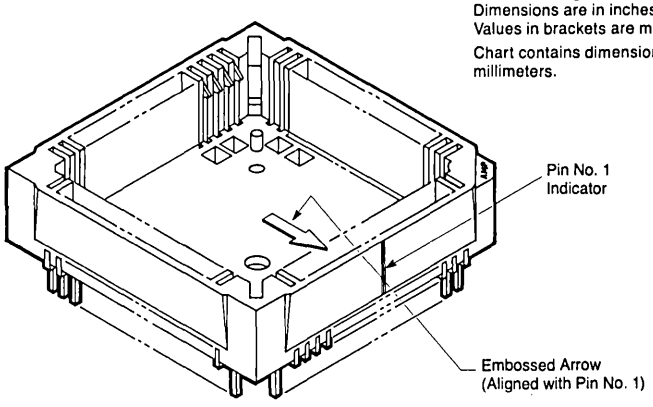
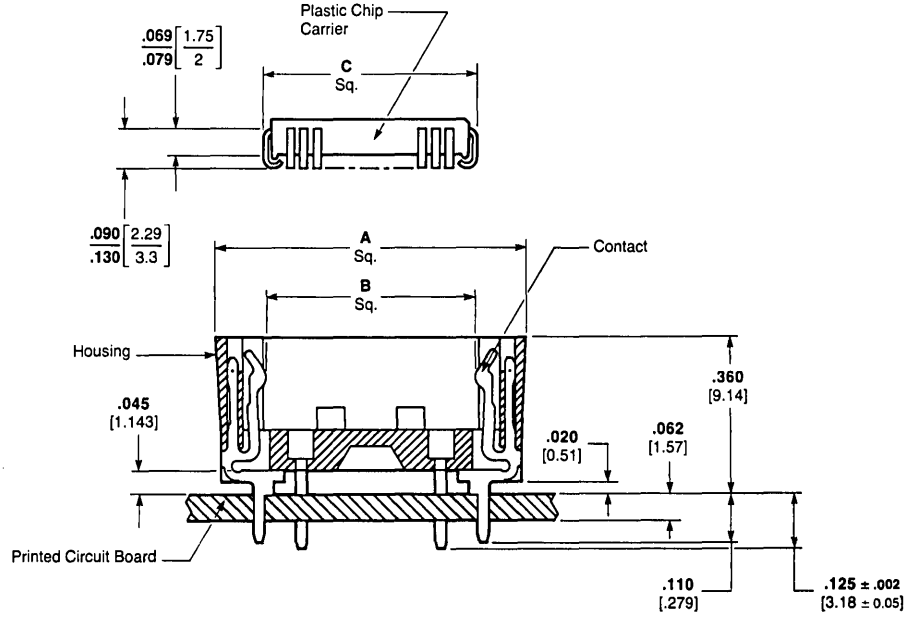
Values in brackets are metric equivalents.
Chart contains dimensions in inches over millimeters.



No. of Positions	Dimensions A	B	C	Socket Part Numbers	Replacement Contacts*
84	**1.385** 35.18	**1.163** 29.54	**1.195/1.185** 30.35/30.1	821573-1	821577 (Inner) 821576 (outer)
68	**1.185** 30.1	**.963** 24.46	**.995/.985** 25.27/25.02	821574-1	
44	**.885** 22.48	**.663** 16.84	**.695/.685** 17.65/17.4	821575-1	
28	**.685** 17.4	**.463** 11.76	**.495/.485** 12.57/12.32	821581-1	

*Contacts are press fit. After soldering, the housing can be removed and contact can be replaced.



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Surface Mount Sockets

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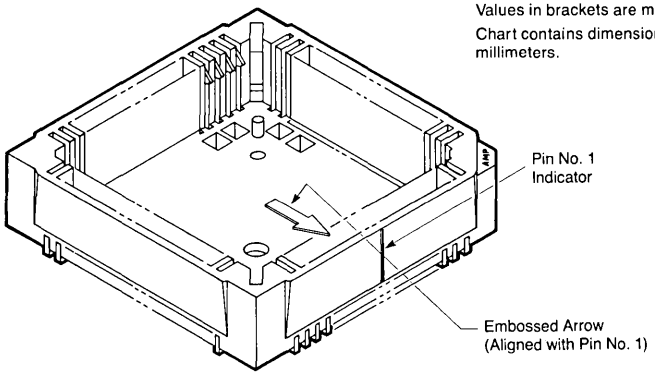
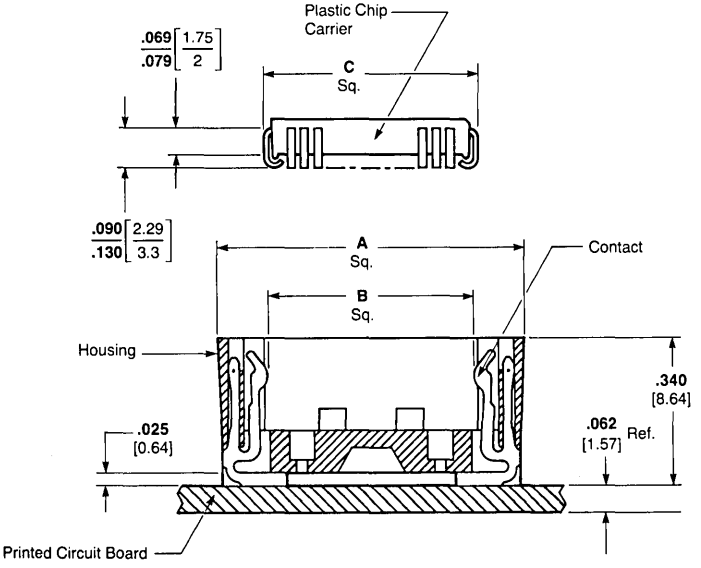
Chart contains dimensions in inches over millimeters.



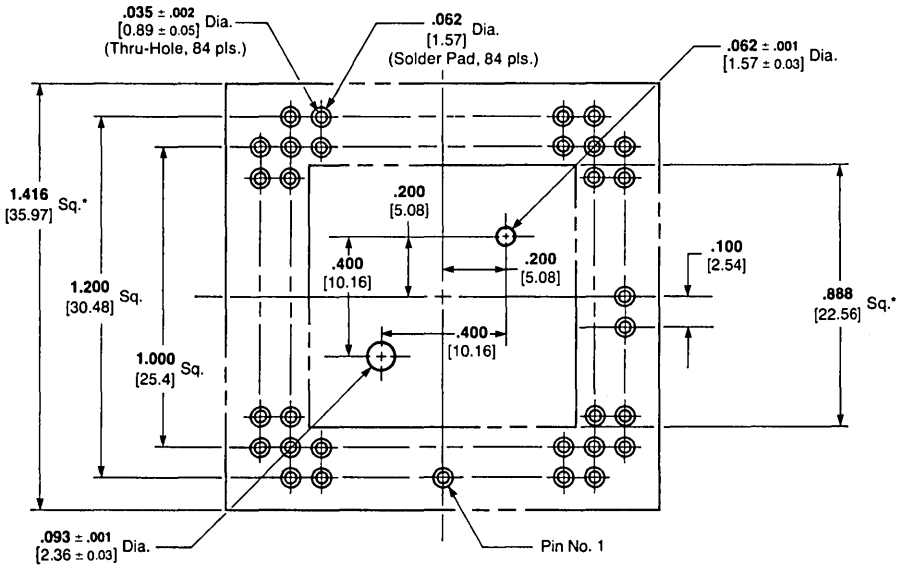
No. of Positions	Dimensions			Socket Part Numbers	Replacement Contacts*
	A	B	C		
84	**1.385** 35.18	**1.163** 29.54	**1.195/1.185** 30.35/30.1	821546-1	827522
68	**1.185** 30.1	**.963** 24.46	**.995/.985** 25.27/25.02	821542-1	
44	**.885** 22.48	**.663** 16.84	**.695/.685** 17.65/17.4	821548-1	
28	**.685** 17.4	**.463** 11.76	**.495/.485** 12.57/12.32	821579-1	

*Contacts are press fit. After soldering, the housing can be removed and contact can be replaced.

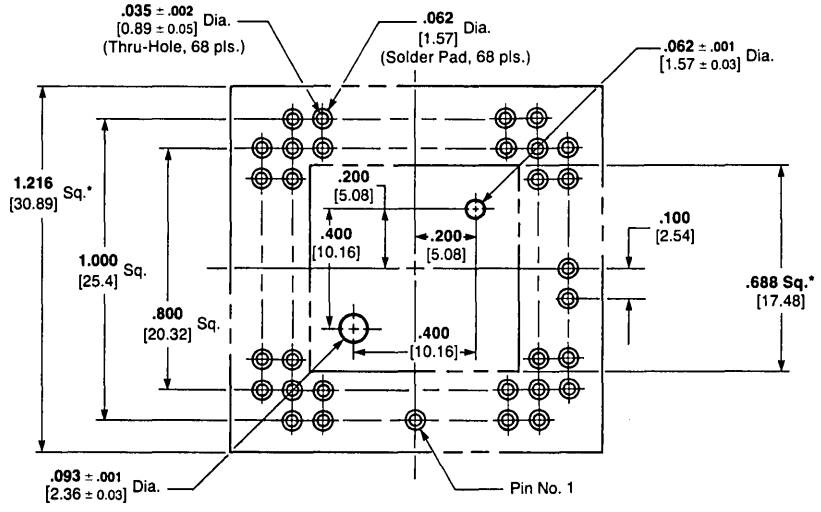


Recommended Printed Circuit Board Hole Pattern

Dimensioning:
Dimensions are in inches and millimeters.
Values in brackets are metric equivalents.



84 Position

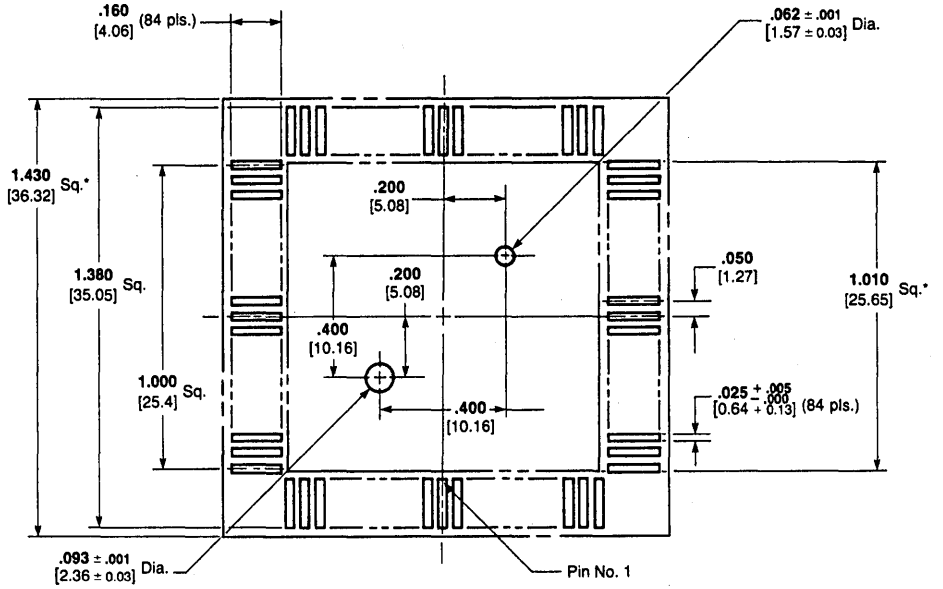


68 Position

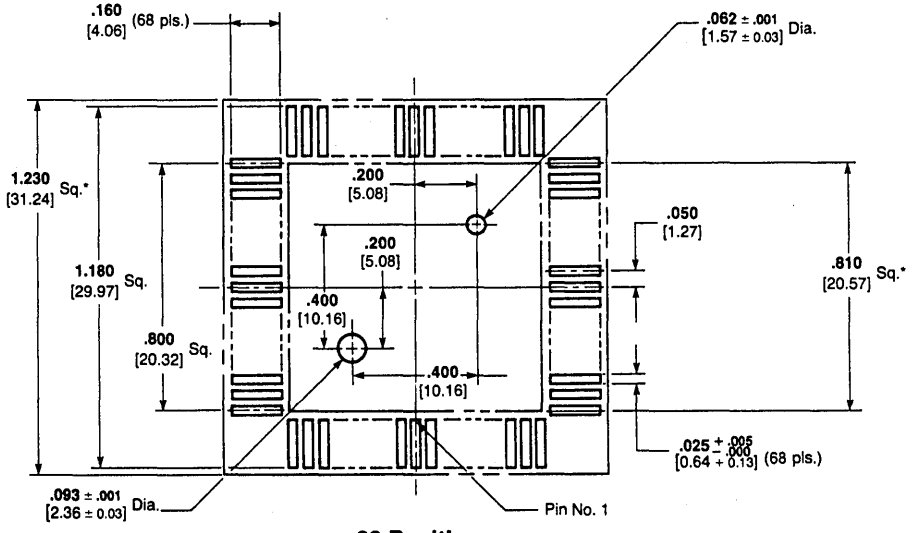
*No additional via. holes recommended between indicated dimensions.
Note: JEDEC printed circuit board pattern for .100 [2.54] grid through-holes.

Recommended Printed Circuit Board Pattern

Dimensioning:
Dimensions are in inches and millimeters.
Values in brackets are metric equivalents.



84 Position

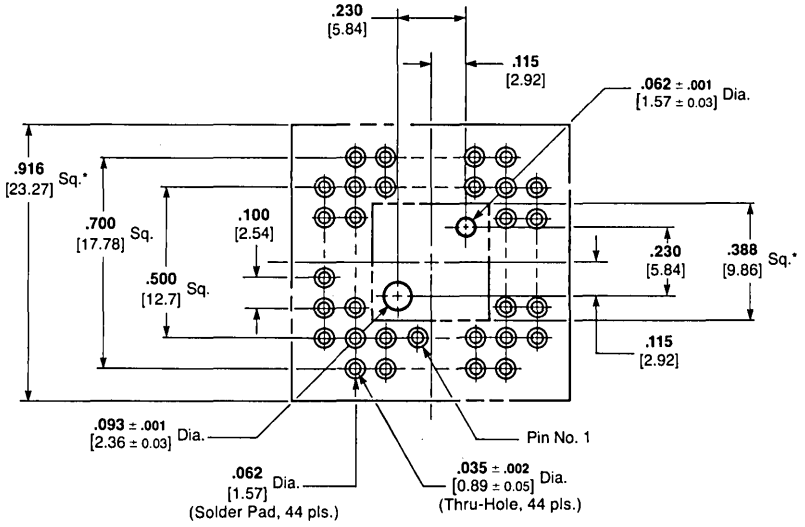


68 Position

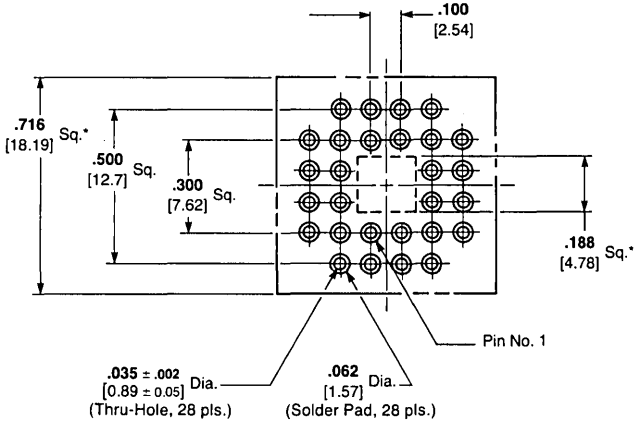
*No additional via. holes recommended between indicated dimensions.
Note: JEDEC printed circuit board pattern for .050 [1.27] centers surface mount pads.

Recommended Printed Circuit Board Hole Pattern

Dimensioning:
Dimensions are in inches and millimeters.
Values in brackets are metric equivalents.



44 Position

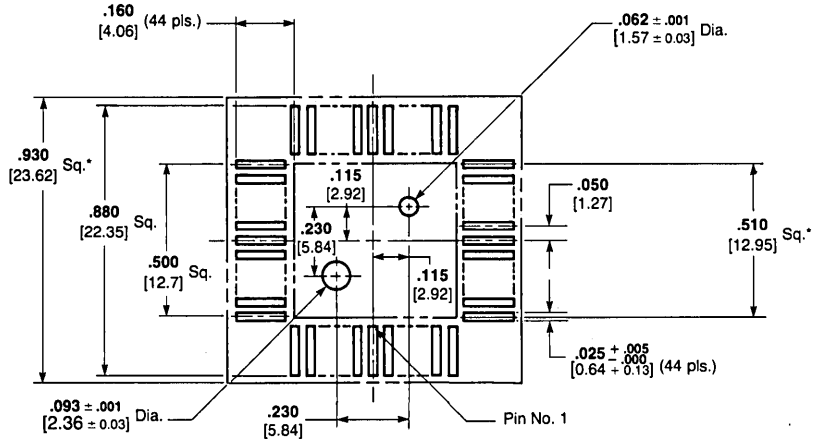


28 Position

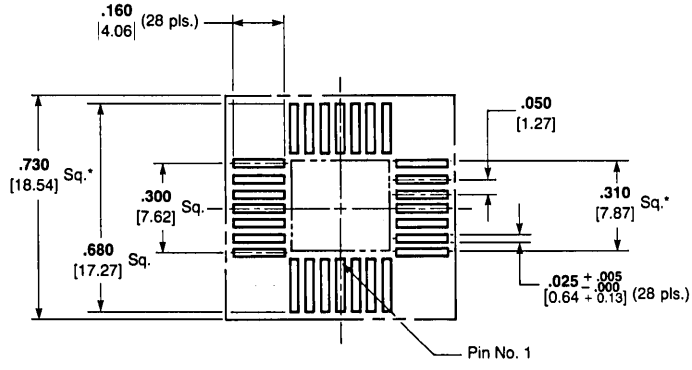
*No additional via. holes recommended between indicated dimensions.
Note: JEDEC printed circuit board pattern for .100 [2.54] grid through-holes.

Recommended Printed Circuit Board Pattern

Dimensioning:
Dimensions are in inches and millimeters.
Values in brackets are metric equivalents.



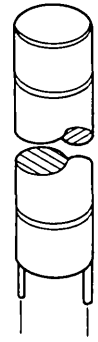
44 Position



28 Position

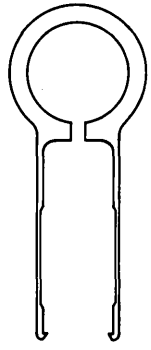
*No additional via. holes recommended between indicated dimensions.
Note: JEDEC printed circuit board pattern for .050 [1.27] centers surface mount pads.

Tooling



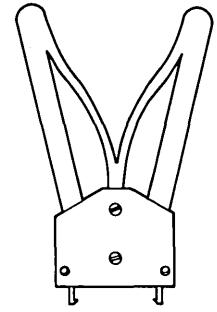
Insertion Tool

No. Positions	Part Number
44	821663-1
68 and 84	68381-1



Extraction Tool

No. Positions	Part Number
28	821598-1



Extraction Tool

No. Positions	Part Number
44	821591-1
68	821566-1
84	821590-1

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