National Semiconductor

400083

Advanced Peripherals

Real Time Clock

Handbook

Advanced Peripherals

REAL TIME CLOCK
HANDBOOK

1989 Edition

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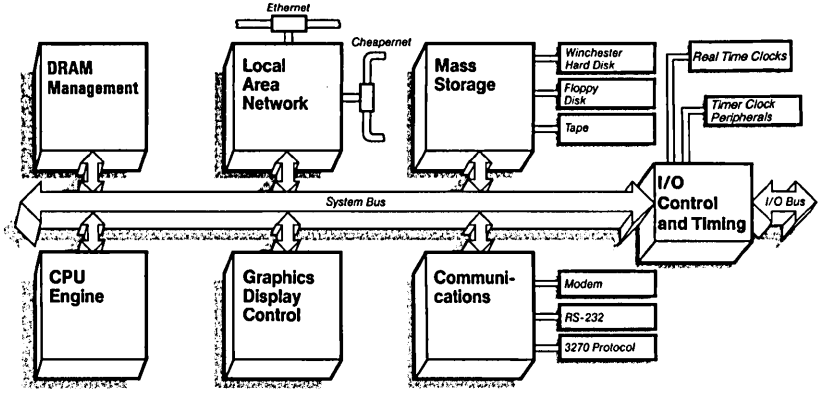
Introduction Advanced Peripherals



TL/XX/0058–1

National Semiconductor Advanced Peripherals products include complex VLSI peripheral circuits designed to serve a variety of applications. The Advanced Peripherals products are especially well suited for microcomputer and microprocessor systems such as graphics workstations, personal computers, and many others. National Semiconductor Advanced Peripherals devices are fully described in a series of databooks and handbooks.

Among the Advanced Peripherals books are the following titles:

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Today's large Dynamic Random Access Memory (DRAM) arrays require sophisticated high performance devices to provide timing access arbitration on board drive and control. National Semiconductor offers the broadest range of DRAM controllers with the highest "No-waitstate" performance available on the market. Controllers are available in Junction Isolated LS, Oxide Isolated ALS, and double metal CMOS for DRAMs from 64k bit through 4M bit devices, supporting memory arrays up to 64 Mbyte in size with only one LSI/VLSI device. For critical applications, National Semiconductor has developed several 16- and 32-bit Error Checking and Correction (ECC) devices to provide maximum data integrity. The Memory Support Handbook contains complete product information and several application notes detailing complete memory system design.

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National offers a family of Real Time Clocks (RTCs) and advanced Timer Clock Peripherals (TCPs). The RTC family provides a simple μP bus compatible interface to any system requiring accurate, reliable, on-going real time and calender functions. The TCP family offers the RTC, RAM and two 16-bit programmable timers with fast μP bus handshake controls for chip select, read and write. The Real Time Clock handbook includes complete product information and datasheets as well as applications information.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Section 1

Real Time Clocks and Timer Clock Peripherals

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TCP Family Comparison Guide

Features	DP8570A	DP8571A	DP8572A	DP8573A
TIMEKEEPING				
Mode	12 or 24 Hour	12 or 24 Hour	12 or 24 Hour	12 or 24 Hour
Range	0.01 sec thru Years	0.01 sec thru Years	0.01 sec thru Years	0.01 sec thru Years
Leap Year	Yes	Yes	Yes	Yes
Rollover	Status Bit	Status Bit	Status Bit	Status Bit
BUS				
Mode	Parallel	Parallel	Parallel	Parallel
Address (# Bits)	5	5	5	5
Data (# Bits)	8	8	8	8
Max Access Time (Address to Data Valid)	150 ns	150 ns	150 ns	150 ns
RAM				
On-Chip	44 Bytes	44 Bytes	44 Bytes	14 Bytes
Timer	2 16-Bit	2 16-Bit	No	No
INTERRUPTS				
Programmable	0.01 sec thru 1 sec	0.01 sec thru 1 sec	0.01 sec thru 1 sec	0.01 sec thru 1 sec
Alarm Compare	Yes	Yes	Yes	Yes
Standby Mode	Yes	Yes	Yes	Yes
Status Register	Yes	Yes	Yes	Yes
Timer	Yes	Yes	No	No
TIMEBASE				
Oscillator Frequency	4 Selectable (Note 1)	4 Selectable (Note 1)	4 Selectable (Note 1)	32.768 kHz
Buffered Oscillator Output	Yes	Yes	Yes	Yes
POWER SUPPLY				
Voltage				
Operational	4.5–5.5V	4.5–5.5V	4.5–5.5V	4.5–5.5V
Standby	2.2V min	2.2V min	2.2V min	2.2V min
Current (32.768 kHz)				
Operational	5 mA	5 mA	5 mA	5 mA
Standby (I_{DD} Max)	10 μA	10 μA	10 μA	10 μA
PROCESS TECHNOLOGY				
	microCMOS	microCMOS	microCMOS	microCMOS
PACKAGING				
Pins/Type	28 DIP 28 PCC (Note 2)	24 DIP (Note 2)	24 DIP (Note 2) 28 PCC (Note 2)	24 DIP (Note 2) 28 PCC (Note 2)

Note 1: 32 kHz, 32.768 kHz, 4.194304 MHz, 4.9152 MHz

Note 2: Socket equivalent pin outs

RTC Family Comparison Guide

Features	MM58167A	MM58274C
TIMEKEEPING		
Mode	24 Hour	12 or 24 Hour
Range	0.01 sec thru Months	0.1 sec thru Years
Leap Year	No	Yes
Rollover	Status Bit	Status Bit
BUS		
Mode	Parallel	Parallel
Address (# Bits)	5	4
Data (# Bits)	8	4
Max Access Time (Address to Data Valid)	1050 ns	650 ns
RAM		
On-Chip	56 Bits (14×4)	No
INTERRUPTS		
Programmable	0.1 sec thru Months	0.1, 0.5, 1, 5, 10, 30 and 60 sec
Alarm Compare	Yes	No
Standby Mode	Yes	No
Status Register	Yes	Yes
TIMEBASE		
Oscillator Frequency	32.768 kHz	32.768 kHz
Buffered Oscillator Output	No	Yes
POWER SUPPLY		
Voltage		
Operational	4.5–5.5V	4.5–5.5V
Standby	2.2V min	2.2V min
Current		
Operational	5 mA	1 mA
Standby (I_{DD} Max)	20 μA	10 μA
PROCESS TECHNOLOGY		
	CMOS	CMOS
PACKAGING		
Pins/Type	24 DIP 28 PCC	16 DIP 20 PCC

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PRELIMINARY

DP8570A Timer Clock Peripheral (TCP)

General Description

The DP8570A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, the Timers and their data RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Two independent multifunction 10 MHz 16-bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 8 possible clock inputs. Thus, by programming the input clocks and the timer counter values a very wide range of timing durations can be achieved. The range is from about 400 ns (4.915 MHz oscillator) to 65,535 seconds (18 hrs., 12 min.).

Power failure logic and control functions have been integrated on chip. This logic is used by the TCP to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided, and upon power failure detection, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel Resonant Oscillator
- Two 16-bit timers
  - 10 MHz external clock frequency
  - Programmable multi-function output
  - Flexible re-trigger facilities
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, timer and power fail interrupts
- Up to 44 bytes of CMOS RAM
- INTR/MFO pins programmable High/Low and push-pull or open drain

Block Diagram

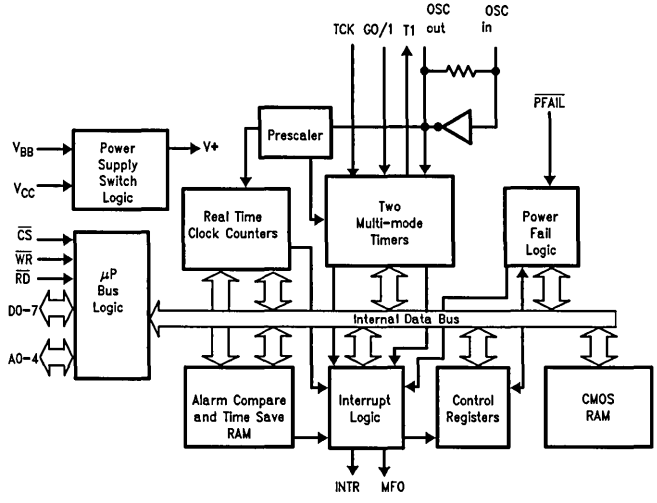

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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	4.5	5.5	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV

DC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} −0.1		V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock		0.8 0.1	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −4.0 mA	V_{CC} −0.1 3.5		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 4.0 mA		0.1 0.25	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5.0	μA
I_{LKG}	Output High Leakage Current T1, MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5.0	μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		260 1.0 12.0	μA mA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		8 20	mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		80 7.5	μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 8)	V_{CC} = GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		10 400	μA μA
I_{BLK}	Battery Supply Leakage	2.2V ≤ V_{BB} ≤ 4.0V	−5	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, $V_{BB} \leq V_{CC}$ −0.4V.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 4.5V ≤ V_{CC} ≤ 5.5V.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: This specification is tested with both the timers and OSC IN driven by a signal generator. Contents of the Test Register = 00(H), the MFO pin is not configured as buffered oscillator out and MFO, T1, INTR, are configured as open drain.

Note 8: This specification is tested with both the timers off, and only OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	20		ns
t_{RW}	Read Strobe Width (Note 9)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 10)	3		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		60	ns
t_{RCH}	Chip Select Hold after Read Strobe	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	50		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	20		ns
t_{WAH}	Address Hold after Write Strobe (Note 10)	3		ns
t_{CW}	Chip Select to End of Write Strobe	90		ns
t_{WW}	Write Strobe Width (Note 11)	80		ns
t_{DW}	Data Valid to End of Write Strobe	50		ns
t_{WDH}	Data Hold after Write Strobe (Note 10)	3		ns
t_{WCH}	Chip Select Hold after Write Strobe	0		ns
TIMER 0/TIMER 1 TIMING				
F_{TCK}	Input Frequency Range	DC	10	MHz
t_{CK}	Propagation Delay Clock to Output		120	ns
t_{GO}	Propagation Delay G0 to G1 to Timer Output (Note 12)		100	ns
t_{PGW}	Pulse Width G0 or G1	25		ns

Note 9: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 10: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

Note 11: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

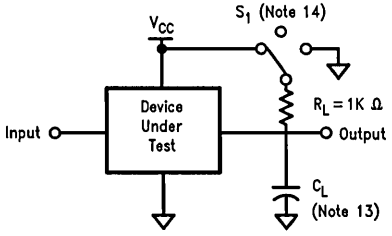
Note 12: Timers in Mode 3.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 14)	Active High +0.5V Active Low −0.5V

Note 13: C_L = 100 pF, includes jig and scope capacitance.

Note 14: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

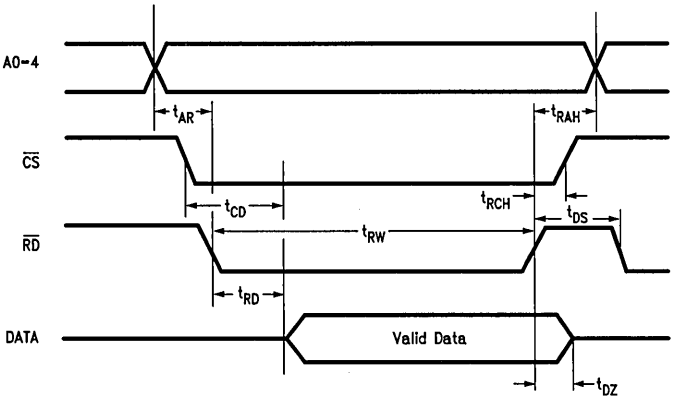
Symbol	Parameter (Note 15)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

Note 15: This parameter is not 100% tested.

Note 16: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Timing Waveforms

Read Timing Diagram



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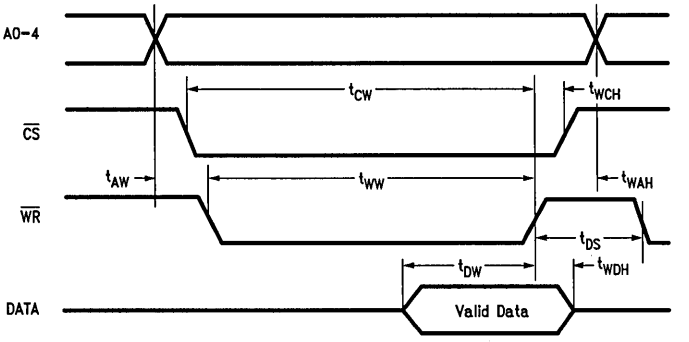
Write Timing Diagram



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General Description (Continued)

The DP8570A's interrupt structure provides four basic types of interrupts: Periodic, Alarm/Compare, Timer, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

One dedicated general purpose interrupt output is provided. A second interrupt output is available on the Multiple Function Output (MFO) pin. Each of these may be selected to generate an interrupt from any source. Additionally, the MFO pin may be programmed to be either as oscillator output or Timer 0's output.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the TCP. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input); OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator or the internal Timer 0. The MFO output can be programmed active high or low, open drain or push-pull. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output can be programmed active high or low, push-pull or open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the TCP. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the TCP goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the TCP programmed for single power supply only, and power applied to the V_{CC} pin.

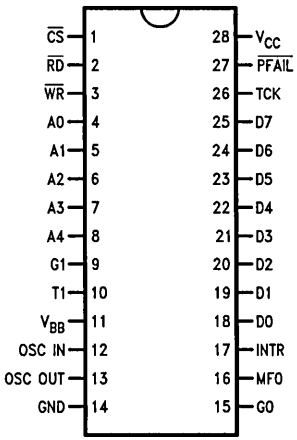
TCK, G1, G0, (Inputs), T1 (Output): TCK is the clock input to both timers when they have an external clock selected. G0 and G1 are active low enable inputs for timers 0 and 1 respectively. T1 is dedicated to the timer 1 output. The T1 output can be programmed active high or low, push-pull or open drain. Timer 0 output is available through MFO pin if desired. If in battery backed mode and a pull-up resistor is attached to T1, it should be connected to a voltage no greater than V_{BB}.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line



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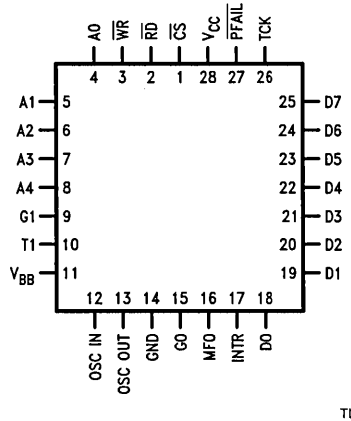
Top View

Order Number DP8570AJ or DP8570AN
See NS Package Number J28A or N28B

Plastic Chip Carrier



TL/F/8638–6

Top View

Order Number DP8570AV
See NS Package Number V28A

Functional Description

The DP8570A contains a fast access real time clock, two 10 MHz 16-bit timers, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the TCP are controlled by a set of nine registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1*.

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management
6. Timers

The memory map of the TCP is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.

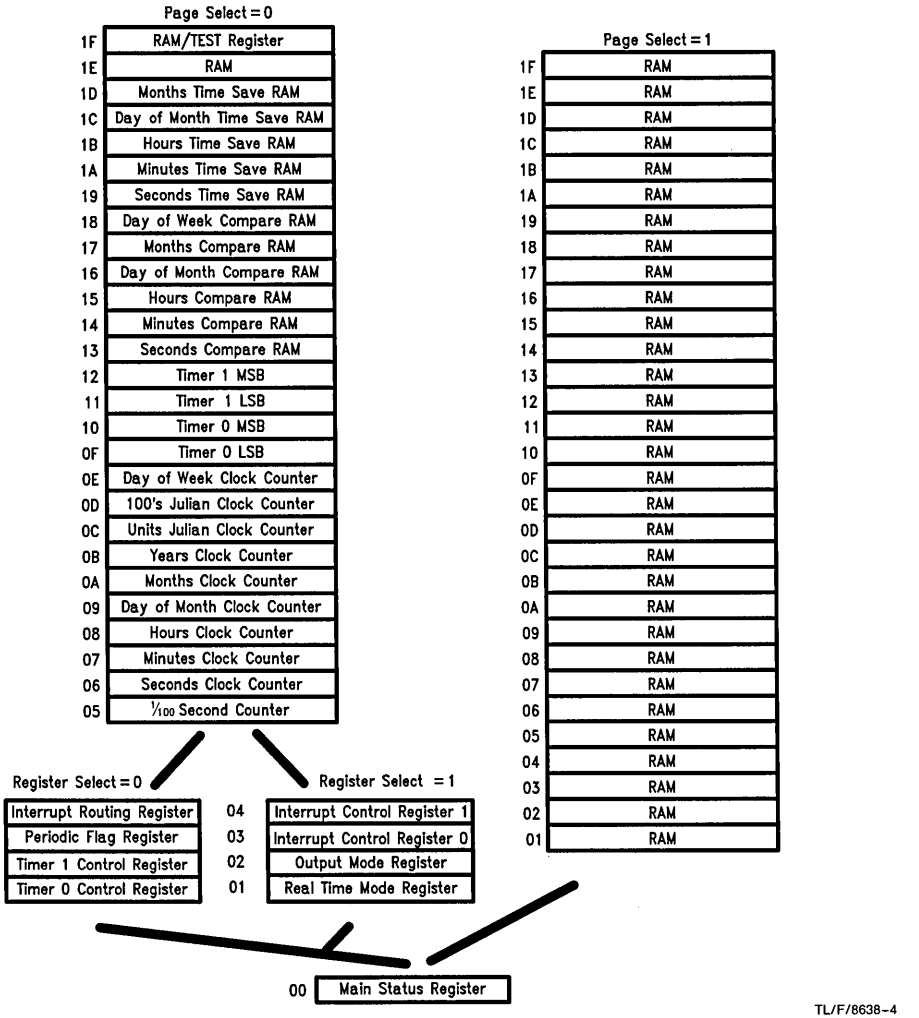


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FIGURE 2. DP8570A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the DP8570A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the TCP is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Interrupt Routing Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.768 kHz, 4.9152 MHz, and 4.194304 MHz.

Once 32 kHz is generated it feeds both timers and the clock. The clock and timer prescalers can be independently enabled by controlling the timer or clock Start/$\overline{\text{Stop}}$ bits.

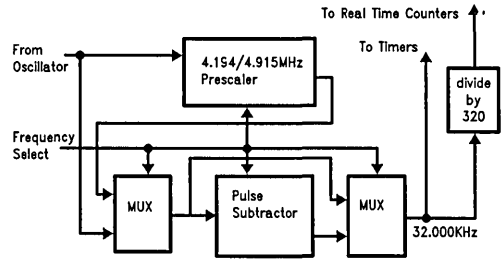

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FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

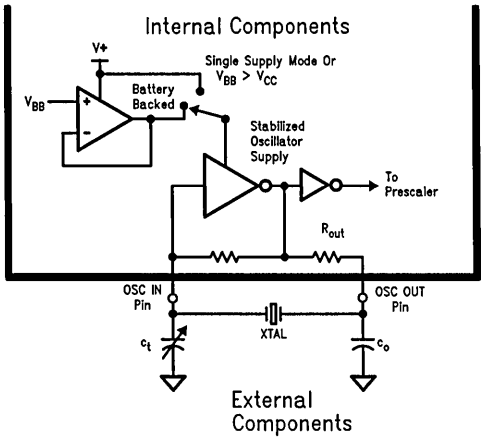

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FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The TCP has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1. Any of the interrupts can be routed to either the INTR pin or the MFO pin, depending on how the Interrupt Routing register is programmed. This, for example, enables the user to dedicate the MFO as a non-maskable interrupt pin to the CPU for power failure detection and enable all other interrupts to appear on the INTR pin. The polarity for the active interrupt can be programmed in the Output Mode Register for either active high or low, and open drain or push pull outputs.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Routing Register	0	0	04H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all TCP interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the TCP to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system.

Note that the Interrupt Status Flag will only monitor the state of the MFO output if it has been configured as an interrupt output (see Output Mode Register description). This is true, regardless of the state of the Interrupt Routing Register. Thus the Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm or Timer interrupts that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the appropriate Alarm or Timer interrupt enable bits are set (see *Figure 5*).

Disabling the periodic bits will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2–D5 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Four Categories:

1. The Timer Interrupts: For description see Timer Section.
2. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
3. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
4. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The TCP then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register. The Periodic Route bit in the Interrupt Routing Register is used to route the periodic interrupt events to either the INTR output or the MFO output.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the TCP when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set.

The Power Fail Route bit determines which output the interrupt will appear on. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the DP8570A provides circuitry to simplify design in battery backed systems. This circuitry switches over to the back up supply, and isolates the DP8570A from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{\text{PFAIL}}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{\text{PFAIL}}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

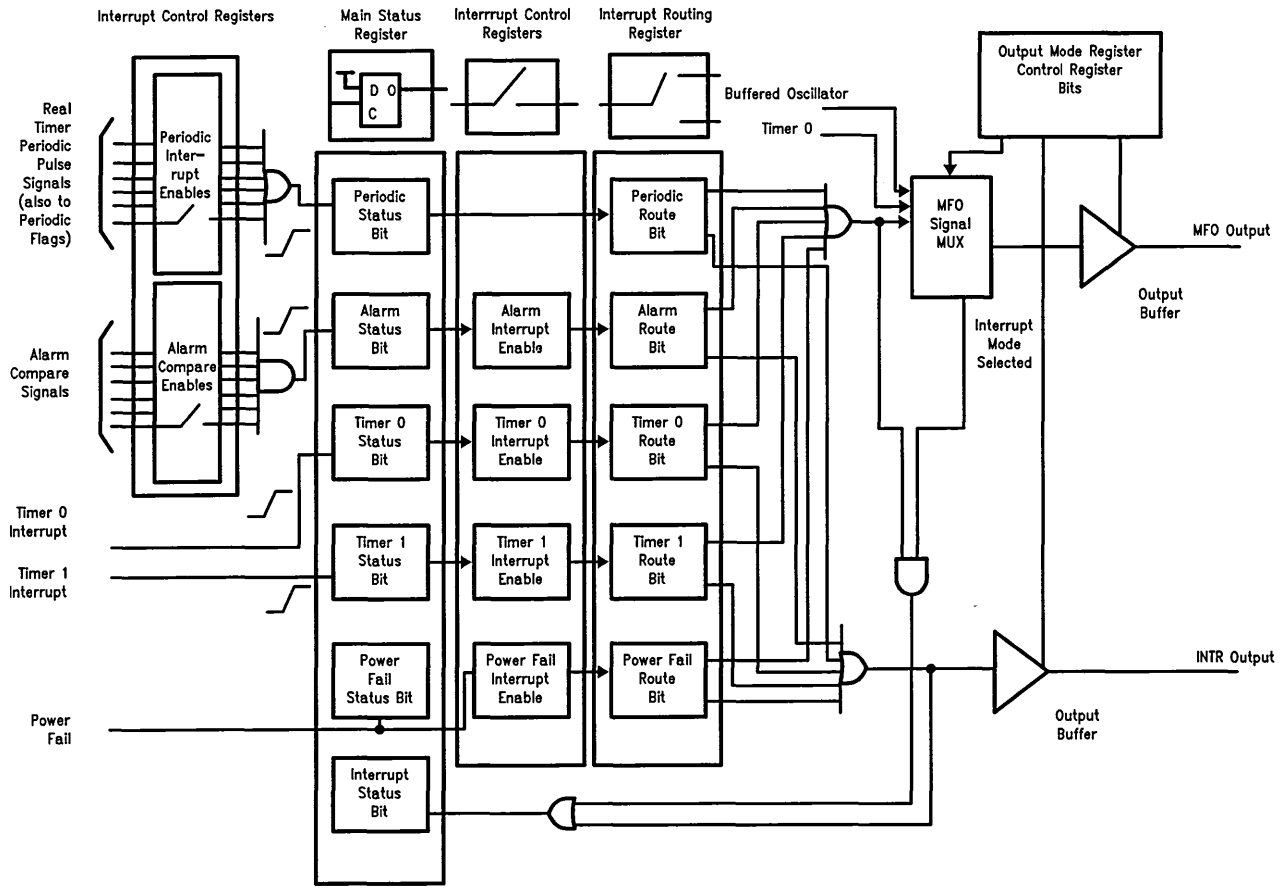

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FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

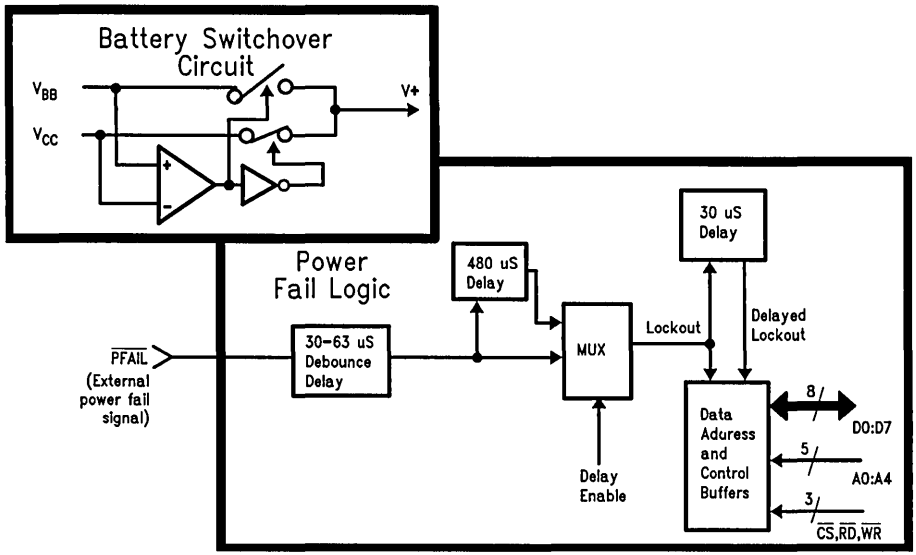

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

The user may choose to have this power failed signal lock-out the TCP's data bus within 30 μs min/63 μs max or to delay the lock-out to enable μP access after power failure is detected. This delay is enabled by setting the delay enable bit in the Routing Register. Also, if the lock-out delay was not enabled the TCP will disconnect itself from the bus within 30 μs min $\rightarrow$ 63 μs max. If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the DP8570A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the TCP it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{\text{PFAIL}}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the TCP will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the TCP will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{\text{PFAIL}}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
TCK, G0, G1	Not Isolated	Locked Out
$\overline{\text{PFAIL}}$	Not Isolated	Not Isolated
INTR, MFO T1	Not Isolated	Open Drain

The Timer and Interrupt Power Fail Operation bits in the Real-Time Mode Register determine whether or not the timers and interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{\text{PFAIL}}$ = 0. When $\overline{\text{PFAIL}}$ = 1

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the DP8570A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{\text{PFAIL}}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The DP8570A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC}. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the DP8570A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

TIMER FUNCTIONAL DESCRIPTION

The DP8570A contains 2 independent multi-mode timers. Each timer is composed of a 16-bit negative edge triggered binary down counter and associated control. The operation is similar to existing μP peripheral timers except that several features have been enhanced. The timers can operate in four modes, and in addition, the input clock frequency can be selected from a prescaler over a wide range of frequencies. Furthermore, these timers are capable of generating interrupts as well as hardware output signals, and both the interrupt and timer outputs are fully programmable active high, or low, open drain, or push-pull.

Figure 7 shows the functional block diagram of one of the timers. The timer consists of a 16-bit counter, two 8-bit input registers, two 8-bit output registers, clock prescaler, mode control logic, and output control logic. The timer and the data registers are organized as two bytes for each timer. Under normal operations a read/write to the timer locations will read or write to the data input register. The timer contents can be read by setting the counter Read bit (RD) in the timer control register.

TIMER INITIALIZATION

The timer's operation is controlled by a set of registers, as listed in Table III. These consist of 2 data input registers and one control register per timer. The data input registers contain the timers count down value. The Timer Control Register is used to set up the mode of operation and the input clock rate. The timer related interrupts can be controlled by programming the Interrupt Routing Register and Interrupt Control Register 0. The timer outputs are configured by the Output Mode Register.

TABLE III. Timer Associated Registers

Register Name	Register Select	Page Select	Address
Timer 0 Data MSB	X	0	10H
Timer 0 Data LSB	X	0	0FH
Timer 0 Control Register	0	0	01H
Timer 1 Data MSB	X	0	12H
Timer 1 Data LSB	X	0	11H
Timer 1 Control Register	0	0	02H
Interrupt Routing Register	0	0	04H
Interrupt Control Reg. 0	1	0	03H
Output Mode Register	1	0	02H

All these registers must be initialized prior to starting the timer(s). The Timer Control Register should first be set to select the timer mode with the timer start/$\overline{\text{stop}}$ bit reset. Then when the timer is to be started the control register should be rewritten identically but with the start/$\overline{\text{stop}}$ bit set.

TIMER OPERATION

Each timer is capable of operation in one of four modes. As mentioned, these modes are programmed in each timer's Control Register which is described later. All four modes operate in a similar manner. They operate on the two 8-bit data words stored into the Data Input Register. At the beginning of a counting cycle the 2 bytes are loaded into the timer and the timer commences counting down towards zero. The exact action taken when zero is reached depends on the mode selected, but in general, the timer output will change state, and an interrupt will be generated if the timer interrupts are unmasked.

Functional Description (Continued)

INPUT CLOCK SELECTION

The input frequency to the timers may be selected. Each timer has a prescaler that gives a wide selection of clocking rates. In addition, the DP8570A has a single external clock input pin that can be selected for either of the timers. Table IV shows the range of programmable clocks available and the corresponding setting in the Timer Control Register.

TABLE IV. Programmable Timer Input Clocks

C2	C1	C0	Selected Clock
0	0	0	External
0	0	1	Crystal Oscillator
0	1	0	(Crystal Oscillator)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	1/10 Second (10 Hz)
1	1	1	1 Second (1 Hz)

Note that the second and third selections are not fixed frequencies, but depend on the crystal oscillator frequency chosen.

Since the input clock frequencies are usually running asynchronously to the timer Start/$\overline{\text{Stop}}$ control bit, a 1 clock cycle error may result. This error results when the Start/Stop occurs just after the clock edge (max error). To minimize this error on all clocks an independent prescaler is used for each timer and is designed so that its Start/Stop error is less than 1 clock cycle.

The count hold/gate bit in the Timer Control Register and the external enable pins, G0/G1, can be used to suspend the timer operation in modes 0, 1, and 2 (in mode 3 it is the trigger input). The external pin and the register bit are OR'ed together, so that when either is high the timers are suspended. Suspending the timer causes the same synchronization error that starting the timer does. The range of errors is specified in Table V.

TABLE V. Maximum Synchronization Errors

Clock Selected	Error
External	+ Ext. Clock Period
Crystal	+ 1 Crystal Clock Period
Crystal/4	+ 1 Crystal Clock Period
10.7 kHz	+ 32 μs
1 kHz	+ 32 μs
100 Hz	+ 32 μs
10 Hz	+ 32 μs
1 Hz	+ 32 μs

MODES OF OPERATION

Bits M0 and M1 in the Timer Control Registers are used to specify the modes of operation. The mode selection is described in Table VI.

TABLE VI. Programmable Timer Modes of Operation

M1	M0	Function	Modes
0	0	Single Pulse Generator	Mode 0
0	1	Rate Generator, Pulse Output	Mode 1
1	0	Square Wave Output	Mode 2
1	1	Retriggerable One Shot	Mode 3

MODE 0: SINGLE PULSE GENERATOR

When the timer is in this mode the output will be initially low if the Timer Start/$\overline{\text{Stop}}$ bit is low (stopped). When this mode is initiated the timer output will go high on the next falling edge of the prescaler's input clock, the contents

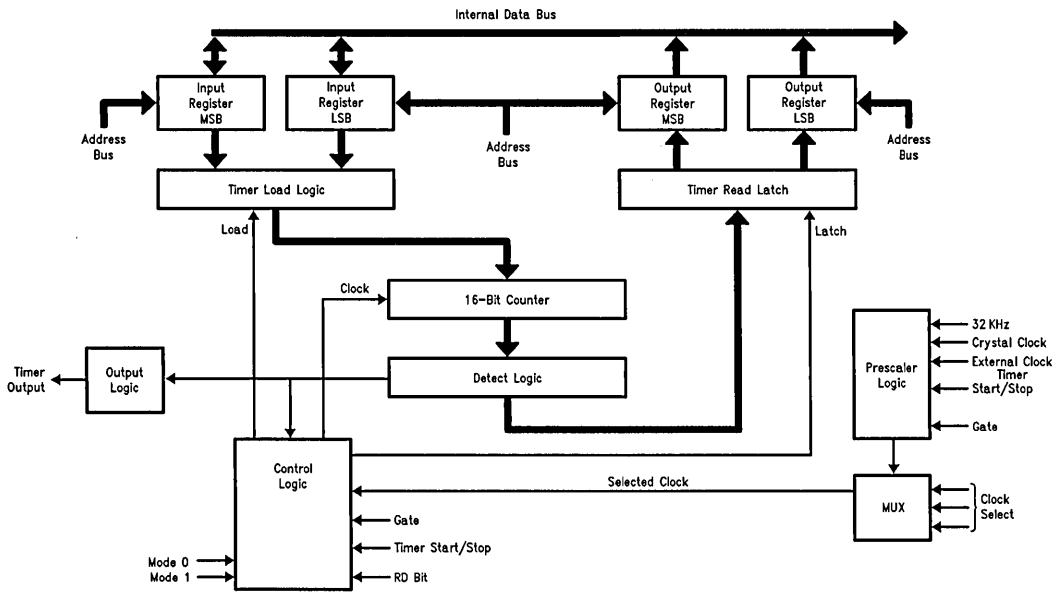

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FIGURE 7. DP8570A Timer Block Diagram

Functional Description (Continued)

of the input data registers are loaded into the timer. The output will stay high until the counter reaches zero. At zero the output is reset. The result is an output pulse whose duration is equal to the input clock period times the count value (N) loaded into the input data register. This is shown in *Figure 8*.

Pulse Width = Clock Period × N

An interrupt is generated when the zero count is reached. This can be used for one-time interrupts that are set to occur a certain amount of time in the future. In this mode the Timer Start/$\overline{\text{Stop}}$ bit (TSS) is automatically reset upon zero detection. This removes the need to reset TSS before starting another operation.

The count down operation may be temporarily suspended either under software control by setting the Count Hold/Gate bit in the timer register high, or in hardware by setting the G0 or G1 pin high.

The above discussion assumes that the timer outputs were programmed to be non-inverting outputs (active high). If the polarity of the output waveform is wrong for the application the polarity can be reversed by configuring the Output Mode Register. The drive configuration can also be programmed to be push pull or open drain.

MODE 1: RATE GENERATOR

When operating in this mode the timer will operate continuously. Before the timer is started its output is low. When the timer is started the input data register contents are loaded into the counter on the negative clock edge and the output is set high (again assuming the Output Mode Register is programmed active high). The timer will then count down to zero. Once the zero count is reached the output goes low for one clock period of the timer clock. Then on the next clock the counter is reloaded automatically and the countdown repeats itself. The output, shown in *Figure 9*, is a waveform whose pulse width and period is determined by N, the input register value, and the input clock period:

Period = (N + 1) (Clock Period)

Pulse Width = Clock Period

The G0 or G1 pin and the count hold/gate bit can be used to suspend the appropriate timer countdown when either is high. Again, the output polarity is controllable as in mode 0. If enabled, an interrupt is generated whenever the zero count is reached. This can be used to generate a periodic interrupt.

MODE 2: SQUARE WAVE GENERATOR

This mode is also cyclic but in this case a square wave rather than a pulse is generated. The output square wave period is determined by the value loaded into the timer input register. This period and the duty cycle are:

Period = 2(N + 1) (Clock Period) Duty Cycle = 0.5

When the timer is stopped the output will be low, and when the Start/$\overline{\text{Stop}}$ bit is set high the timer's counter will be loaded on the next clock falling transition and the output will be set high.

The output will be toggled after the zero count is detected and the counter will then be reloaded, and the cycle will continue. Thus, every N + 1 counts the output gets toggled, as shown in *Figure 10*. Like the other modes the timer operation can be suspended either by software setting the count hold/gate bit (CHG) in the Timer Control Register or by using the gate pins. An interrupt will be generated every falling edge of the timer output, if enabled.

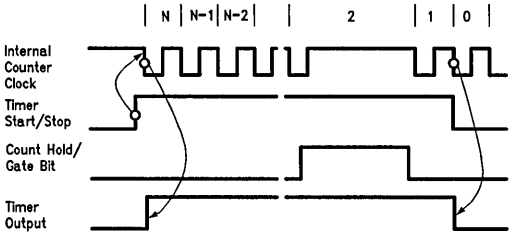

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FIGURE 8. Typical Waveforms for Timer Mode 0 (Timer Output Programmed Active High)

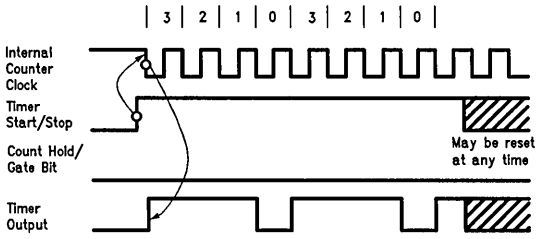

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FIGURE 9. Timing Waveforms for Timer Mode 1 (Timer Output Programmed Active High)

Functional Description (Continued)

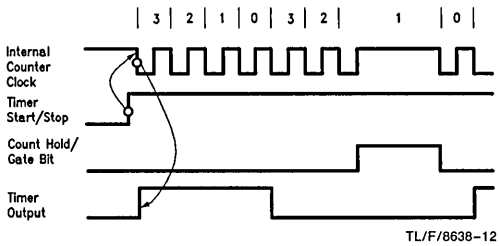


FIGURE 10. Timing Waveforms for Timer Mode 2 (Timer Output Programmed Active High)

MODE 3: RETRIGGERABLE ONE SHOT

This mode is different from the previous three modes in that this is the only mode which uses the external gate to trigger the output. Once the timer Start/$\overline{\text{Stop}}$ bit is set the output stays inactive, and nothing happens until a positive transition is received on the G1 or G0 pins, or the Count Hold/ Gate (CHG) bit is set in the timer control register. When a transition ocurs the one shot output is set active immediately; the counter is loaded with the value in the input register on the next transition of the input clock and the countdown begins. If a retrigger occurs, regardless of the current counter value, the counters will be reloaded with the value in the input register and the counter will be restarted without changing the output state. See *Figure 11*. A trigger count can occur at any time during the count cycle and can be a hardware or software signal (G0, G1 or CHG). In this mode the timer will output a single pulse whose width is determined by the value in the input data register (N) and the input clock period.

Pulse Width = Clock Period × N

Before entering mode 3, if a spurious edge has occurred on G0/G1 or the CHG bit is set to logic 1, then a pulse will appear at MFO or T1 or INTR output pin when the timer is started. To ensure this does not happen, do the following steps before entering mode 3: Configure the timer for mode 0, load a count of zero, then start the timer.

The timer will generate an interrupt only when it reaches a count of zero. This timer mode is useful for continuous "watch dog" timing, line frequency power failure detection, etc.

READING THE TIMERS

Normally reading the timer data register addresses, 0FH and 10H for Timer 0 and 11H and 12H for Timer 1 will result in reading the input data register which contains the preset value for the timers. During timer operation it is often useful to read the contents of the 16-bit down counter. This reading may be an erroneous value of FFFFH.

To read a timer, the μP first sets the timer read bit in the appropriate Timer Control Register high. This will cause the counter's contents to be latched to 2–8 bit output registers, and will enable these registers to be read if the μP reads the timer's input data register addresses. On reading the LSB byte the timer read bit is internally reset and subsequent reads of the timer locations will return the input register values.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 32 locations at one time. An internal switching scheme provides a total of 67 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table VII. They show the name, address and page locations for the DP8570A.

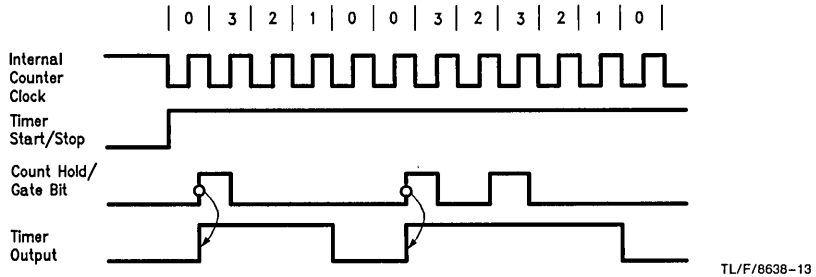


FIGURE 11. Timing Waveforms for Timer Mode 3, Output Programmed Active High

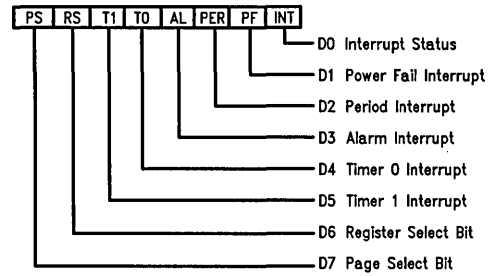
Functional Description (Continued)

TABLE VII. Register/Counter/RAM Addressing for DP8570A

A0-4	PS (Note 1)	RS (Note 2)	Description
CONTROL REGISTERS			
00	X	X	Main Status Register
01	0	0	Timer 0 Control Register
02	0	0	Timer 1 Control Register
03	0	0	Periodic Flag Register
04	0	0	Interrupt Routing Register
01	0	1	Real Time Mode Register
02	0	1	Output Mode Register
03	0	1	Interrupt Control Register 0
04	0	1	Interrupt Control Register 1
COUNTERS (CLOCK CALENDAR)			
05	0	X	1/100, 1/10 Seconds (0-99)
06	0	X	Seconds (0-59)
07	0	X	Minutes (0-59)
08	0	X	Hours (1-12, 0-23)
09	0	X	Days of Month (1-28/29/30/31)
0A	0	X	Months (1-12)
0B	0	X	Years (0-99)
0C	0	X	Julian Date (LSB) (1-99)
0D	0	X	Julian Date (0-3)
0E	0	X	Day of Week (1-7)
TIMER DATA REGISTERS			
0F	0	X	Timer 0 LSB
10	0	X	Timer 0 MSB
11	0	X	Timer 1 LSB
12	0	X	Timer 1 MSB
TIMER COMPARE RAM			
13	0	X	Sec Compare RAM (0-59)
14	0	X	Min Compare RAM (0-59)
15	0	X	Hours Compare RAM (1-12, 0-23)
16	0	X	DOM Compare RAM (1-28/29/30/31)
17	0	X	Months Compare RAM (1-12)
18	0	X	DOW Compare RAM (1-7)
TIME SAVE RAM			
19	0	X	Seconds Time Save RAM
1A	0	X	Minutes Time Save RAM
1B	0	X	Hours Time Save RAM
1C	0	X	Day of Month Time Save RAM
1D	0	X	Months Time Save RAM
1E	0	1	RAM
1F	0	X	RAM/Test Mode Register
01-1F	1	X	2nd Page General Purpose RAM

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block or the page selected.

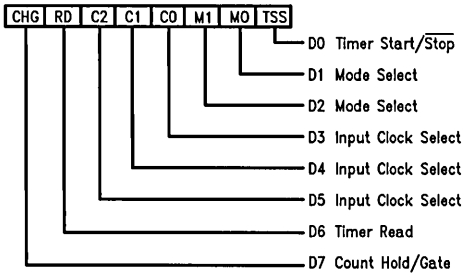
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3-D5 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1-D5: These five bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1, D3-D5 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

Functional Description (Continued)

TIMER 0 AND 1 CONTROL REGISTER



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These registers control the operation of the timers. Each timer has its own register.

D0: This bit will Start (1) or Stop (0) the timer. When the timer is stopped the timer's prescaler and counter are reset, and the timer will restart from the beginning when started again. In mode 0 on time out the TSS bit is internally reset.

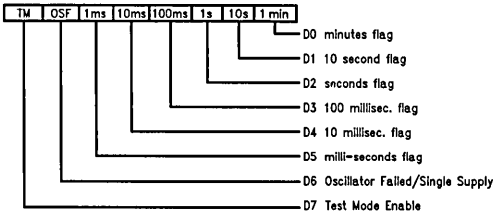
D1 and D2: These control the count mode of the timers. See Table VI.

D3–D5: These bits control which clock signal is applied to the timer's counter input. There is one external clock input pin (TCK) and either (or both) timer(s) can be selected to run off this pin: refer to Table IV for details.

D6: This is the read bit. If a one is written into this location it will cause the contents of the timer to be latched into a holding register, which can be read by the μP at any time. Reading the least significant byte of the timer will reset the RD bit. The timer read cycle can be aborted by writing RD to zero.

D7: The CHG bit has two mode dependent functions. In modes 0 through 2 writing a one to this bit will suspend the timer operation (without resetting the timer prescaler). However, in mode 3 this bit is used to trigger or re-trigger the count sequence as with the gate pins. If retriggering is desired using the CHG bit, it is not necessary to write a zero to this location prior to the re-trigger. The action of further writing a one to this bit will re-trigger the count.

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

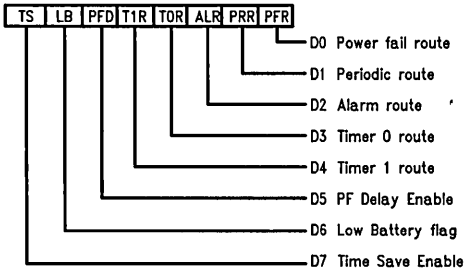
D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. This bit is automatically set on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/stop bit in the Real Time Mode Register, with the crystal oscillating.

When D6 is written to, it defines whether the TCP is being used in battery standby (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single supply mode applications. This bit is automatically set on initial power-up or an oscillator fail event. This disables the oscillator reference circuit, and requires that V_{BB} is connected to ground, and the single supply mode connected to V_{CC}. When this bit is set to zero, the oscillator reference is enabled. This allows operation in standard battery standby application.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table VII). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

INTERRUPT ROUTING REGISTER



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D0–D4: The lower 5 bits of this register are associated with the main interrupt sources created by this chip. The purpose of this register is to route the interrupts to either the MFO (multi-function pin), or to the main interrupt pin. When any bit is set the associated interrupt signal will be sent to the MFO pin, and when zero it will be sent to the INTR pin.

Functional Description (Continued)

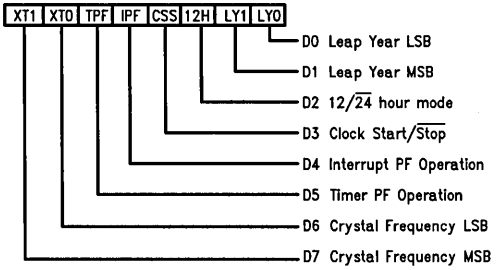
D5: The Delay Enable bit is used when a power fail occurs. If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



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D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/Stop bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the TCP is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Timer interrupts will also be functional provided that bit D5 is also set. Note that the MFO and INTR pins are configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register 0 and bits D6 and D7 of interrupt control register 1 will be reset when the TCP enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5: This bit controls the operation of the timers in standby mode. If set to a one the timers will continue to function when the TCP is in standby mode. The input pins TCK, G0, G1 are locked out in standby mode, and cannot be used.

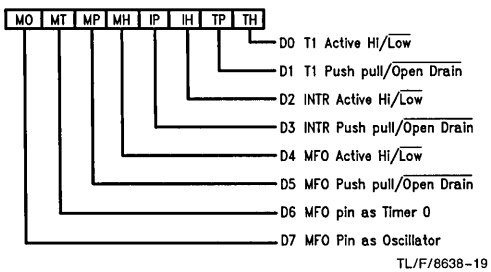
Therefore external control of the timers is not possible in standby mode. Note also that MFO and T1 pins are automatically reconfigured open drain during standby.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



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Functional Description (Continued)

D0: This bit, when set to a one makes the T1 (timer 1) output pin active high, and when set to a zero, it makes this pin active low.

D1: This bit controls whether the T1 pin is an open drain or push-pull output. A one indicates push pull.

D2: This bit, when set to a one makes the INTR output pin active high, and when set to a zero, it makes this pin active low.

D3: This bit controls whether the INTR pin is an open drain or push-pull output. A one indicates push-pull.

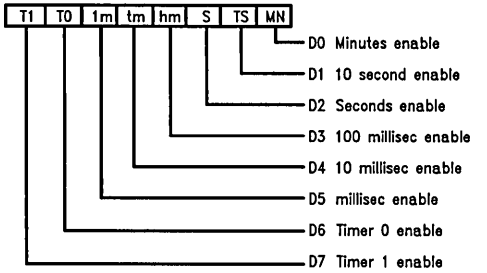
D4: This bit, when set to a one makes the MFO output pin active high, and when set to a zero, it makes this pin active low.

D5: This bit controls whether the MFO pin is an open drain or push-pull output. A one indicates push-pull.

D6 and D7: These bits are used to program the signal appearing at the MFO output, as follows:

D7	D6	MFO Output Signal
0	0	2nd Interrupt
0	1	Timer 0 Waveform
1	X	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0



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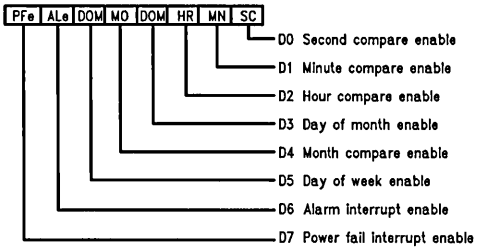
D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: These are individual timer enable bits. A one written to these bits enable the timers to generate interrupts to the μP.

INTERRUPT CONTROL REGISTER 1



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D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $\overline{\text{PFAIL}} = 0$.

This bit also enables the low battery detection analog circuitry.

If the user wishes to mask the power fail interrupt, but utilize the analog circuitry, this bit should be enabled, and the Routing Register can be used to route the interrupt to the MFO pin. The MFO pin can then be left open or configured as the Timer 0 or buffered oscillator output.

Control and Status Register Address Bit Map

Main Status Register PS = 0 RS = 0 ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R[1]	R[1]	R[1]	R[1]	R[2]	R[3]
Page Select	Register Select	Timer 1 Interrupt	Timer 0 Interrupt	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed.

Timer 0 Control Register PS = 0 RS = 0 Address = 01H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Timer 1 Control Register PS = 0 RS = 0 Address = 02H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Interrupt Routing Register PS = 0 RS = 0 Address = 04H

R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	Timer 1 Int. Route MFO/$\overline{INT}$	Timer 0 Int. Route MFO/$\overline{INT}$	Alarm Int. Route MFO/$\overline{INT}$	Periodic Int. Route MFO/$\overline{INT}$	Power Fail Int. Route MFO/$\overline{INT}$

6. Set and reset by V_{BB} voltage.

Real Time Mode Register PS = 0 RS = 1 Address = 01H

Crystal Freq. XT1	Crystal Freq. XT0	Timers EN on Back-Up	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	MFO as Timer 0	MFO PP/$\overline{OD}$	MFO Active HI/$\overline{LO}$	INTR PP/$\overline{OD}$	INTR Active HI/$\overline{LO}$	T1 PP/$\overline{OD}$	T1 Active HI/$\overline{LO}$

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

Timer 1 Interrupt Enable	Timer 0 Interrupt Enable	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

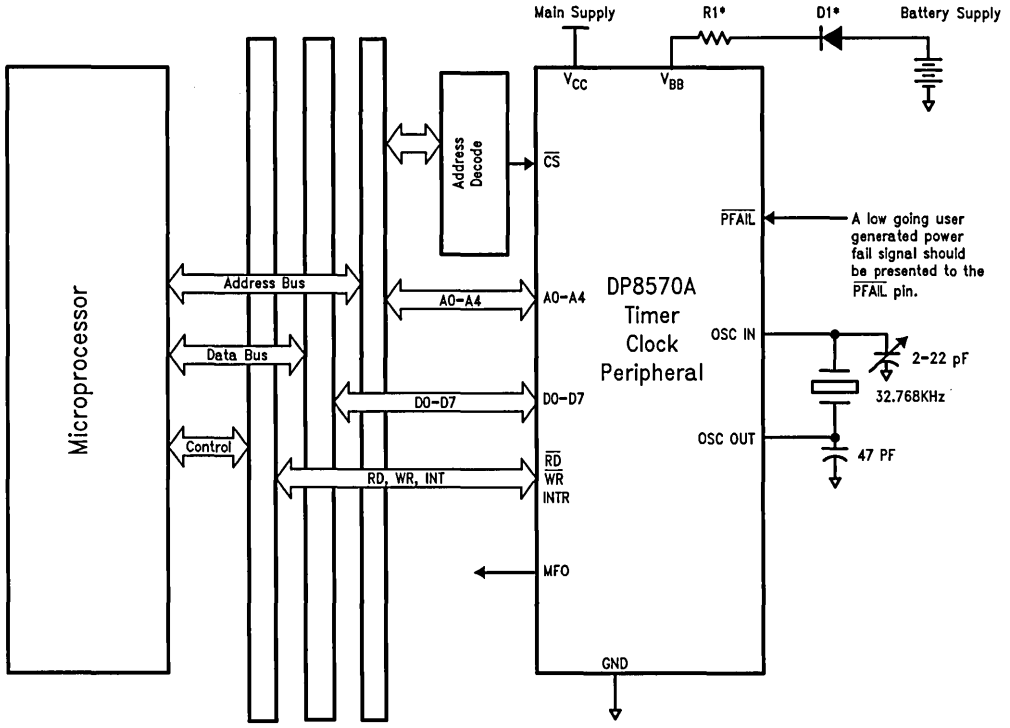
All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

Typical Application



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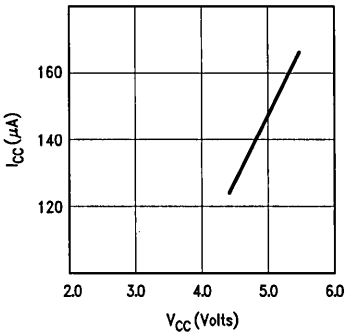
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode F_{OSC} = 32.768 kHz)



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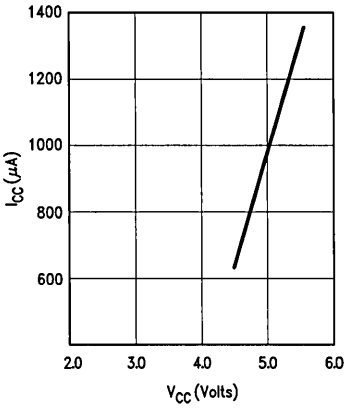
Operating Current vs Supply Voltage (Battery Backed Mode F_{OSC} = 32.768 kHz)



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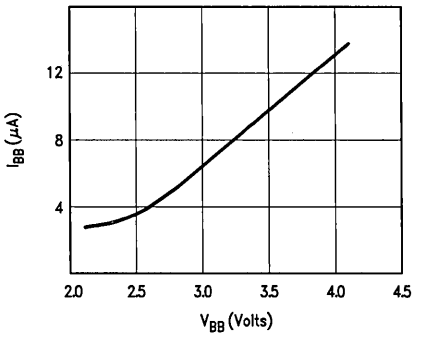
Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



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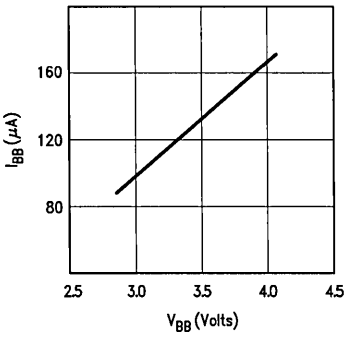
Standby Current vs Power Supply Voltage F_{OSC} = 4.194304 MHz



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National Semiconductor

PRELIMINARY

DP8571A Timer Clock Peripheral (TCP)

General Description

The DP8571A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, the Timers and their data RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Two independent multifunction 10 MHz 16-bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 7 possible clock inputs. Thus, by programming the input clocks and the timer counter values a very wide range of timing durations can be achieved. The range is from about 400 ns (4.915 MHz oscillator) to 65,535 seconds (18 hrs., 12 min.).

Power failure logic and control functions have been integrated on chip. This logic is used by the TCP to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided, and upon power failure detection, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel resonant oscillator
- Two 16-bit timers
  - 10 MHz external clock frequency
  - Programmable multi-function output
  - Flexible re-trigger facilities
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, timer and power fail interrupts
- Up to 44 bytes of CMOS RAM
- INTR/MFO pins programmable High/Low and push-pull or open drain

Block Diagram

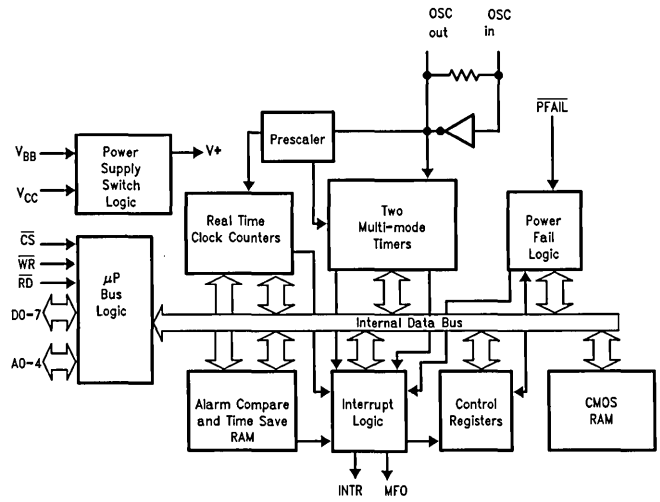

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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	4.5	5.5	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV

DC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} −0.1		V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock		0.8 0.1	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −4.0 mA	V_{CC} −0.1 3.5		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 4.0 mA		0.1 0.25	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5.0	μA
I_{LKG}	Output High Leakage Current T1, MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5.0	μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		260 1.0 12.0	μA mA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		8 20	mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		80 7.5	μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 8)	V_{CC} = GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		10 400	μA μA
I_{BLK}	Battery Supply Leakage	2.2V ≤ V_{BB} ≤ 4.0V	−5	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, $V_{BB} \leq V_{CC}$ −0.4V.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 4.5V ≤ V_{CC} ≤ 5.5V.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: This specification is tested with both the timers and OSC IN driven by a signal generator. Contents of the Test Register = 00(H), the MFO pin is not configured as buffered oscillator out and MFO, INTR, are configured as open drain.

Note 8: This specification is tested with both the timers off, and only OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	20		ns
t_{RW}	Read Strobe Width (Note 9)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 10)	3		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		60	ns
t_{RCH}	Chip Select Hold after Read Strobe	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	50		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	20		ns
t_{WAH}	Address Hold after Write Strobe (Note 10)	3		ns
t_{CW}	Chip Select to End of Write Strobe	90		ns
t_{WW}	Write Strobe Width (Note 11)	80		ns
t_{DW}	Data Valid to End of Write Strobe	50		ns
t_{WDH}	Data Hold after Write Strobe (Note 10)	3		ns
t_{WCH}	Chip Select Hold after Write Strobe	0		ns

Note 9: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 10: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

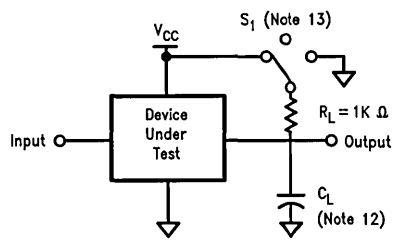
Note 11: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 13)	Active High +0.5V Active Low −0.5V

Note 12: C_L = 100 pF, includes jig and scope capacitance.

Note 13: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

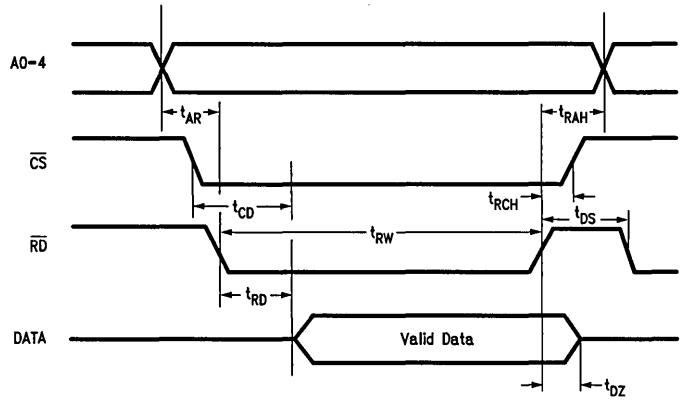
Symbol	Parameter (Note 14)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

Note 14: This parameter is not 100% tested.

Note 15: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Timing Waveforms

Read Timing Diagram



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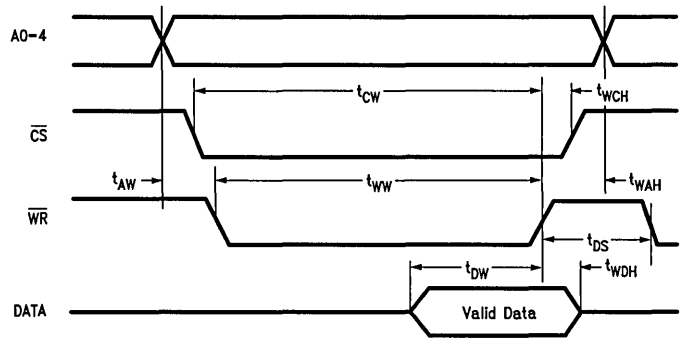
Write Timing Diagram



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General Description (Continued)

The DP8571A's interrupt structure provides four basic types of interrupts: Periodic, Alarm/Compare, Timer, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

One dedicated general purpose interrupt output is provided. A second interrupt output is available on the Multiple Function Output (MFO) pin. Each of these may be selected to generate an interrupt from any source. Additionally, the MFO pin may be programmed to be either as oscillator output or Timer 0's output.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the TCP. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input): OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator or the internal Timer 0. The MFO output can be programmed active high or low, open drain or push-pull. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output can be programmed active high or low, push-pull or open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the TCP. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the TCP goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

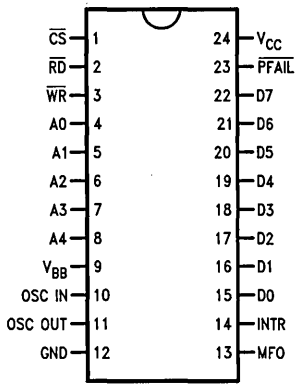
V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the TCP programmed for single power supply only, and power applied to the V_{CC} pin.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagram

Dual-In-Line



TL/F/9979–5

Top View

Order Number DP8571AJ
See NS Package Number J24F

Functional Description

The DP8571A contains a fast access real time clock, two 10 MHz 16-bit timers, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the TCP are controlled by a set of nine registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1*.

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management
6. Timers

The memory map of the TCP is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.

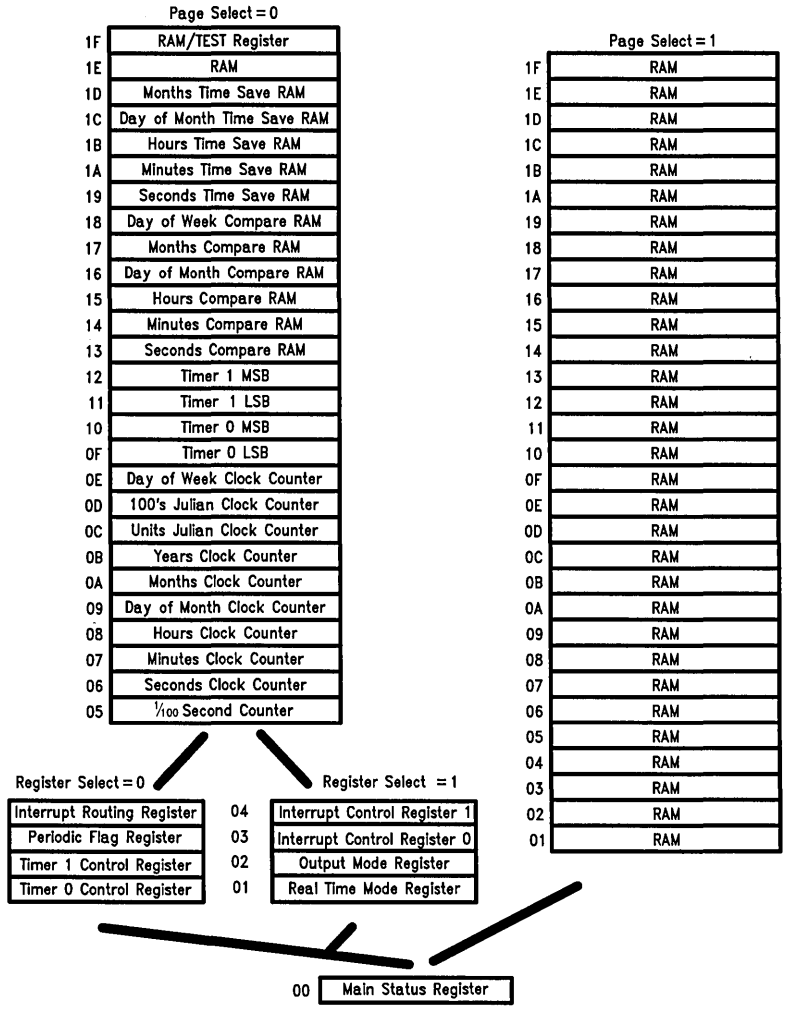


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FIGURE 2. DP8571A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the DP8571A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the TCP is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Interrupt Routing Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.768 kHz, 4.9152 MHz, and 4.194304 MHz.

Once 32 kHz is generated it feeds both timers and the clock. The clock and timer prescalers can be independently enabled by controlling the timer or clock Start/$\overline{\text{Stop}}$ bits.

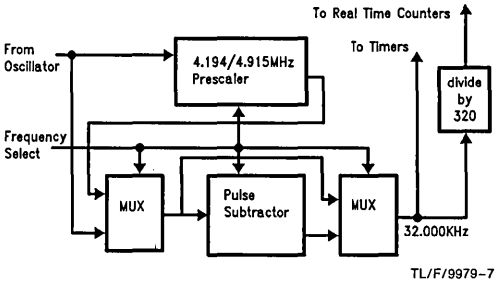

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FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

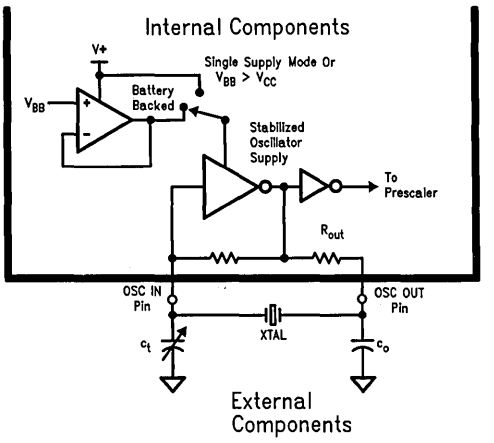

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FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The TCP has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1. Any of the interrupts can be routed to either the INTR pin or the MFO pin, depending on how the Interrupt Routing register is programmed. This, for example, enables the user to dedicate the MFO as a non-maskable interrupt pin to the CPU for power failure detection and enable all other interrupts to appear on the INTR pin. The polarity for the active interrupt can be programmed in the Output Mode Register for either active high or low, and open drain or push pull outputs.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Routing Register	0	0	04H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all TCP interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the TCP to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system.

Note that the Interrupt Status Flag will only monitor the state of the MFO output if it has been configured as an interrupt output (see Output Mode Register description). This is true, regardless of the state of the Interrupt Routing Register. Thus the Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm or Timer interrupts that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the appropriate Alarm or Timer interrupt enable bits are set (see *Figure 5*).

Disabling the periodic bits will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2–D5 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Four Categories:

1. The Timer Interrupts: For description see Timer Section.
2. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
3. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
4. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The TCP then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register. The Periodic Route bit in the Interrupt Routing Register is used to route the periodic interrupt events to either the INTR output or the MFO output.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the TCP when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set.

The Power Fail Route bit determines which output the interrupt will appear on. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the DP8571A provides circuitry to simplify design in battery backed systems. This circuitry switches over to the back up supply, and isolates the DP8571A from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{\text{PFAIL}}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{\text{PFAIL}}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

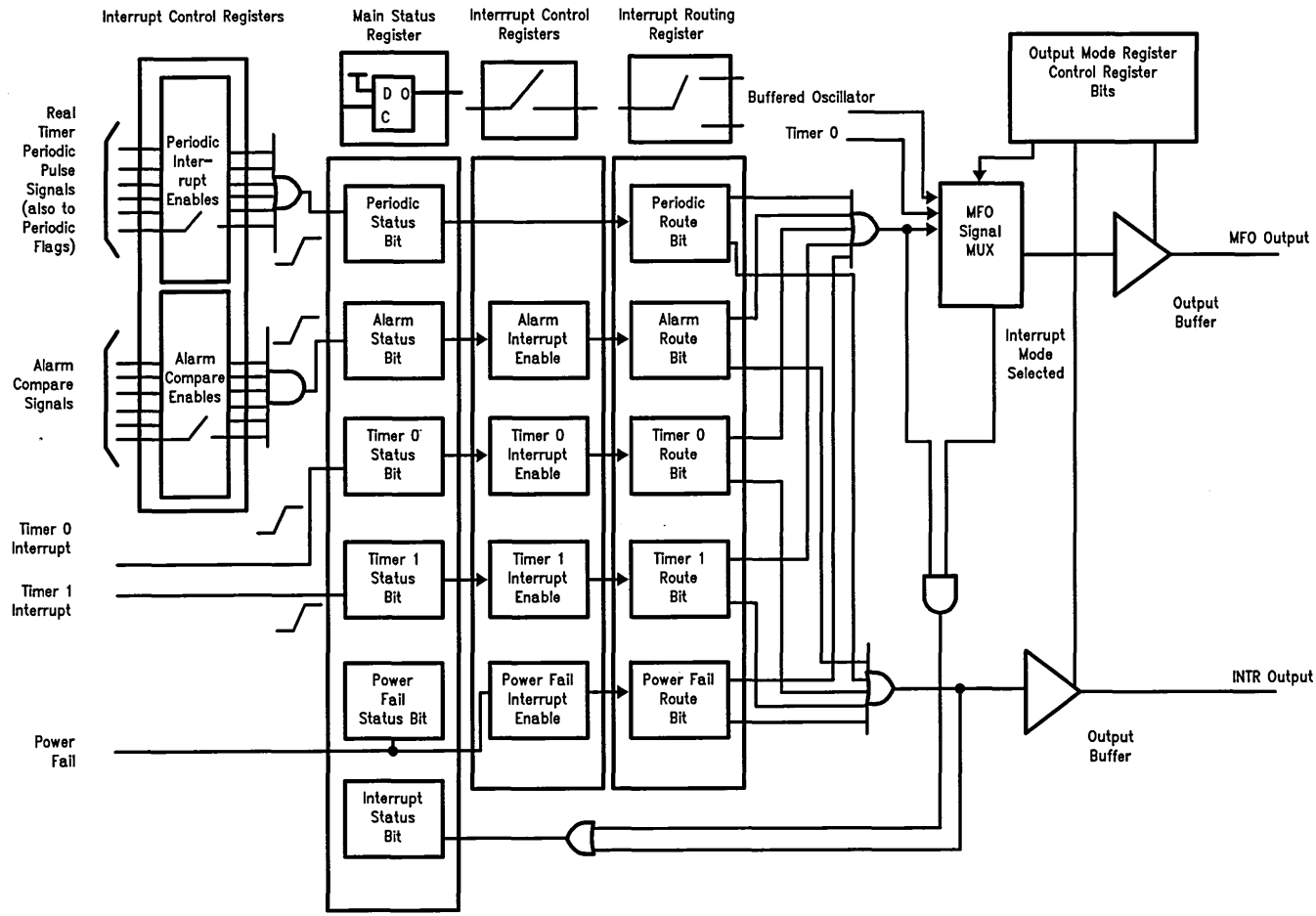

FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

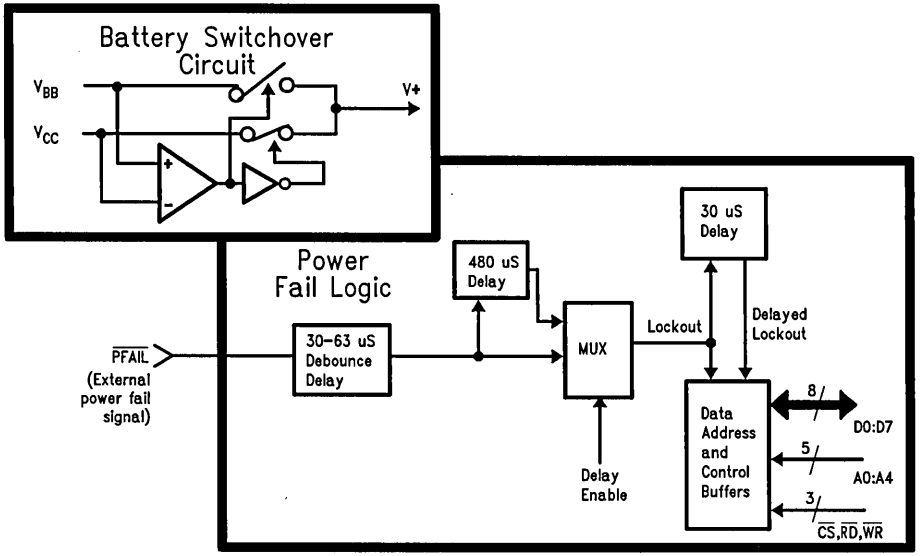

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

The user may choose to have this power failed signal lock-out the TCP's data bus within 30 μs min/63 μs max or to delay the lock-out to enable μP access after power failure is detected. This delay is enabled by setting the delay enable bit in the Routing Register. Also, if the lock-out delay was not enabled the TCP will disconnect itself from the bus within 30 μs min → 63 μs max. If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the DP8571A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the TCP it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{\text{PFAIL}}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the TCP will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the TCP will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{\text{PFAIL}}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
$\overline{\text{PFAIL}}$	Not Isolated	Not Isolated
INTR, MFO	Not Isolated	Open Drain

The Timer and Interrupt Power Fail Operation bits in the Real-Time Mode Register determine whether or not the timers and interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{\text{PFAIL}}$ = 0. When $\overline{\text{PFAIL}}$ = 1

1

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the DP8571A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{\text{PFAIL}}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The DP8571A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC}. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the DP8571A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

TIMER FUNCTIONAL DESCRIPTION

The DP8571A contains 2 independent multi-mode timers. Each timer is composed of a 16-bit negative edge triggered binary down counter and associated control. The operation is similar to existing μP peripheral timers except that several features have been enhanced. The timers can operate in four modes, and in addition, the input clock frequency can be selected from a prescaler over a wide range of frequencies. Furthermore, these timers are capable of generating interrupts and the Timer 0 output signal is available as a hardware output via the MFO pin. Timer 1 output, however, is not available as a hardware output signal. Both the interrupt and MFO outputs are fully programmable active high, or low, open drain, or push-pull.

Figure 7 shows the functional block diagram of one of the timers. The timer consists of a 16-bit counter, two 8-bit input registers, two 8-bit output registers, clock prescaler, mode control logic, and output control logic. The timer and the data registers are organized as two bytes for each timer. Under normal operations a read/write to the timer locations will read or write to the data input register. The timer contents can be read by setting the counter Read bit (RD) in the timer control register.

TIMER INITIALIZATION

The timer's operation is controlled by a set of registers, as listed in Table III. These consist of 2 data input registers and one control register per timer. The data input registers contain the timers count down value. The Timer Control Register is used to set up the mode of operation and the input clock rate. The timer related interrupts can be controlled by programming the Interrupt Routing Register and Interrupt Control Register 0. The timer outputs are configured by the Output Mode Register.

TABLE III. Timer Associated Registers

Register Name	Register Select	Page Select	Address
Timer 0 Data MSB	X	0	10H
Timer 0 Data LSB	X	0	0FH
Timer 0 Control Register	0	0	01H
Timer 1 Data MSB	X	0	12H
Timer 1 Data LSB	X	0	11H
Timer 1 Control Register	0	0	02H
Interrupt Routing Register	0	0	04H
Interrupt Control Reg. 0	1	0	03H
Output Mode Register	1	0	02H

All these registers must be initialized prior to starting the timer(s). The Timer Control Register should first be set to select the timer mode with the timer start/$\overline{\text{stop}}$ bit reset. Then when the timer is to be started the control register should be rewritten identically but with the start/$\overline{\text{stop}}$ bit set.

TIMER OPERATION

Each timer is capable of operation in one of four modes. As mentioned, these modes are programmed in each timer's Control Register which is described later. All four modes operate in a similar manner. They operate on the two 8-bit data words stored into the Data Input Register. At the beginning of a counting cycle the 2 bytes are loaded into the timer and the timer commences counting down towards zero. The exact action taken when zero is reached depends on the mode selected, but in general, the timer output will change state, and an interrupt will be generated if the timer interrupts are unmasked.

Functional Description (Continued)

INPUT CLOCK SELECTION

The input frequency to the timers may be selected. Each timer has a prescaler that gives a wide selection of clocking rates. Table IV shows the range of programmable clocks available and the corresponding setting in the Timer Control Register. Note that the output of Timer 1 may be used as the input to Timer 0. This is a cascade option for the timers and allows them to be clocked as a 32-bit down counter.

TABLE IV. Programmable Timer Input Clocks

C2	C1	C0	Selected Clock
0	0	0	Timer 1 Output
0	0	1	Crystal Oscillator
0	1	0	(Crystal Oscillator)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	1/10 Second (10 Hz)
1	1	1	1 Second (1 Hz)

Note that the second and third selections are not fixed frequencies, but depend on the crystal oscillator frequency chosen.

Since the input clock frequencies are usually running asynchronously to the timer Start/$\overline{\text{Stop}}$ control bit, a 1 clock cycle error may result. This error results when the Start/Stop occurs just after the clock edge (max error). To minimize this error on all clocks an independent prescaler is used for each timer and is designed so that its Start/Stop error is less than 1 clock cycle.

The count hold/gate bit in the Timer Control Register can be used to suspend the timer operation in modes 0, 1, and 2 (in mode 3 it is the trigger input). Suspending the timer causes the same synchronization error that starting the timer does. The range of errors is specified in Table V.

TABLE V. Maximum Synchronization Errors

Clock Selected	Error
External	+ Ext. Clock Period
Crystal	+ 1 Crystal Clock Period
Crystal/4	+ 1 Crystal Clock Period
10.7 kHz	+ 32 μs
1 kHz	+ 32 μs
100 Hz	+ 32 μs
10 Hz	+ 32 μs
1 Hz	+ 32 μs

MODES OF OPERATION

Bits M0 and M1 in the Timer Control Registers are used to specify the modes of operation. The mode selection is described in Table VI.

TABLE VI. Programmable Timer Modes of Operation

M1	M0	Function	Modes
0	0	Single Pulse Generator	Mode 0
0	1	Rate Generator, Pulse Output	Mode 1
1	0	Square Wave Output	Mode 2
1	1	Retriggerable One Shot	Mode 3

MODE 0: SINGLE PULSE GENERATOR

When the timer is in this mode the output will be initially low if the Timer Start/$\overline{\text{Stop}}$ bit is low (stopped). When this mode is initiated the timer output will go high on the next falling edge of the prescaler's input clock, the contents of the

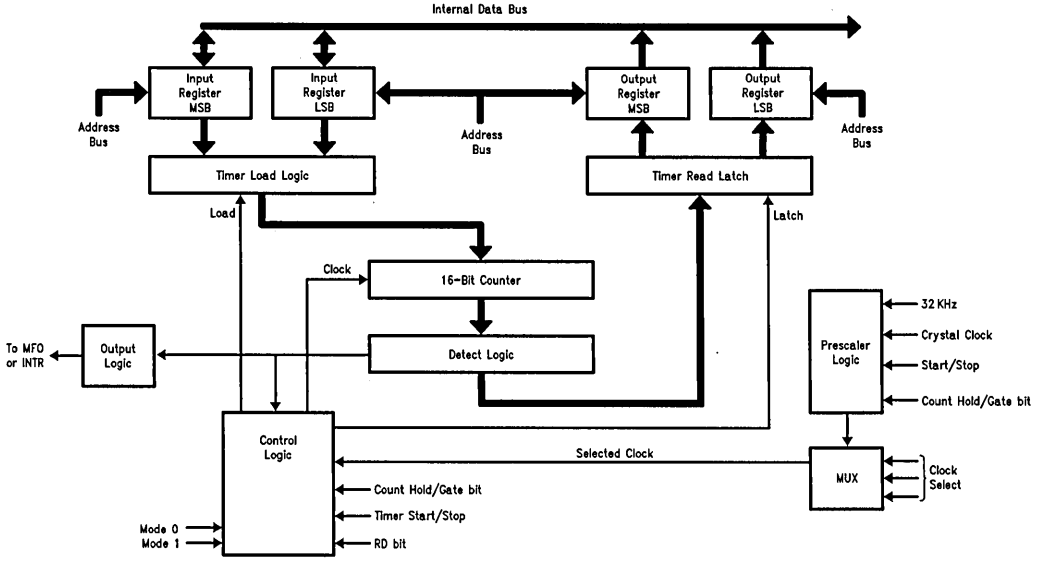

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FIGURE 7. DP8571A Timer Block Diagram

Functional Description (Continued)

input data registers are loaded into the timer. The output will stay high until the counter reaches zero. At zero the output is reset. The result is an output pulse whose duration is equal to the input clock period times the count value (N) loaded into the input data register. This is shown in *Figure 8*.

Pulse Width = Clock Period × N

An interrupt is generated when the zero count is reached. This can be used for one-time interrupts that are set to occur a certain amount of time in the future. In this mode the Timer Start/$\overline{\text{Stop}}$ bit (TSS) is automatically reset upon zero detection. This removes the need to reset TSS before starting another operation.

The count down operation may be temporarily suspended either under software control by setting the Count Hold/Gate bit in the timer register high, or in hardware by setting the G0 or G1 pin high.

The above discussion assumes that the MFO output is programmed to be non-inverting outputs (active high). If the polarity of the output waveform is wrong for the application the polarity can be reversed by configuring the Output Mode Register. The drive configuration can also be programmed to be push pull or open drain.

MODE 1: RATE GENERATOR

When operating in this mode the timer will operate continuously. Before the timer is started its output is low. When the timer is started the input data register contents are loaded into the counter on the negative clock edge and the output is set high (again assuming the Output Mode Register is programmed active high). The timer will then count down to zero. Once the zero count is reached the output goes low for one clock period of the timer clock. Then on the next clock the counter is reloaded automatically and the countdown repeats itself. The output, shown in *Figure 9*, is a waveform whose pulse width and period is determined by N, the input register value, and the input clock period:

Period = (N + 1) (Clock Period)

Pulse Width = Clock Period

Again, the output polarity is controllable as in mode 0. If enabled, an interrupt is generated whenever the zero count is reached. This can be used to generate a periodic interrupt.

MODE 2: SQUARE WAVE GENERATOR

This mode is also cyclic but in this case a square wave rather than a pulse is generated. The output square wave period is determined by the value loaded into the timer input register. This period and the duty cycle are:

Period = 2(N + 1) (Clock Period) Duty Cycle = 0.5

When the timer is stopped the output will be low, and when the Start/$\overline{\text{Stop}}$ bit is set high the timer's counter will be loaded on the next clock falling transition and the output will be set high.

The output will be toggled after the zero count is detected and the counter will then be reloaded, and the cycle will continue. Thus, every N + 1 counts the output gets toggled, as shown in *Figure 10*. Like the other modes the timer operation can be suspended by setting the count hold/gate bit (CHG) in the Timer Control Register. An interrupt will be generated every falling edge of the timer output, if enabled.

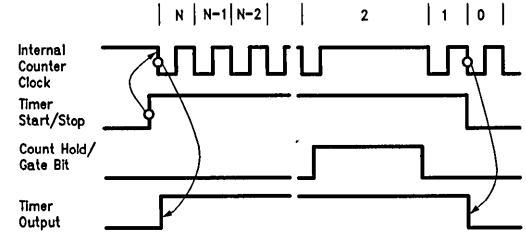

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FIGURE 8. Typical Waveforms for Timer Mode 0 (MFO Output Programmed Active High)

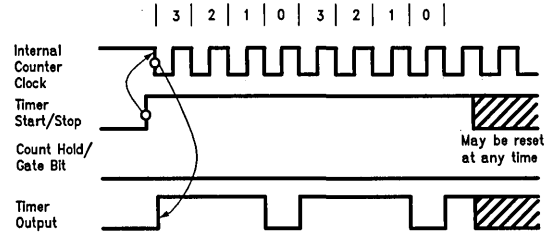

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FIGURE 9. Timing Waveforms for Timer Mode 1 (MFO Output Programmed Active High)

Functional Description (Continued)

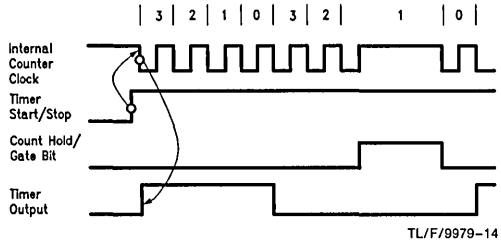


FIGURE 10. Timing Waveforms for Timer Mode 2 (MFO Output Programmed Active High)

MODE 3: RETRIGGERABLE ONE SHOT

Once the timer Start/$\overline{\text{Stop}}$ bit is set the output stays inactive, and nothing happens until the Count Hold/Gate (CHG) bit is set in the timer control register. When a transition ocurs the one shot output is set active immediately; the counter is loaded with the value in the input register on the next transition of the input clock and the countdown begins. If a retrigger occurs, regardless of the current counter value, the counters will be reloaded with the value in the input register and the counter will be restarted without changing the output state. See *Figure 11*. A trigger count can occur at any time during the count cycle. In this mode the timer will output a single pulse whose width is determined by the value in the input data register (N) and the input clock period.

$$\text{Pulse Width} = \text{Clock Period} \times N$$

The timer will generate an interrupt only when it reaches a count of zero. This timer mode is useful for continuous "watch dog" timing, line frequency power failure detection, etc.

READING THE TIMERS

Normally reading the timer data register addresses, 0FH and 10H for Timer 0 and 11H and 12H for Timer 1 will result in reading the input data register which contains the preset value for the timers. During timer operation it is often useful to read the contents of the 16-bit down counter. This reading may be an erroneous value of FFFFH.

To read a timer, the μP first sets the timer read bit in the appropriate Timer Control Register high. This will cause the counter's contents to be latched to 2–8 bit output registers, and will enable these registers to be read if the μP reads the timer's input data register addresses. On reading the LSB byte the timer read bit is internally reset and subsequent reads of the timer locations will return the input register values.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 32 locations at one time. An internal switching scheme provides a total of 67 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table VII. They show the name, address and page locations for the DP8571A.

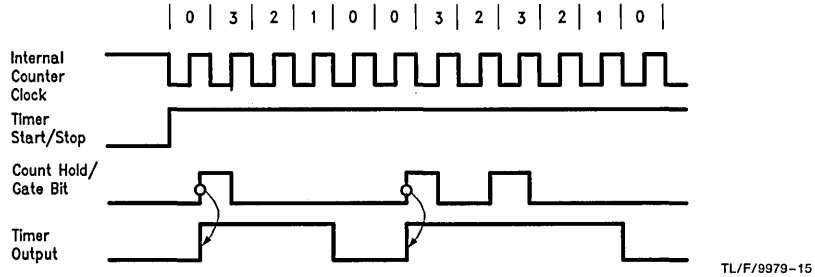


FIGURE 11. Timing Waveforms for Timer Mode 3, MFO Output Programmed Active High

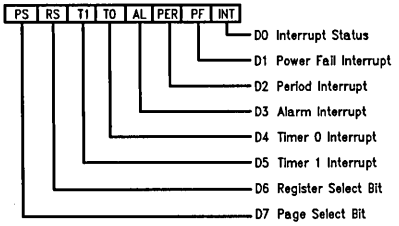
Functional Description (Continued)

TABLE VII. Register/Counter/RAM Addressing for DP8571A

A0-4	PS (Note 1)	RS (Note 2)	Description
CONTROL REGISTERS			
00	X	X	Main Status Register
01	0	0	Timer 0 Control Register
02	0	0	Timer 1 Control Register
03	0	0	Periodic Flag Register
04	0	0	Interrupt Routing Register
01	0	1	Real Time Mode Register
02	0	1	Output Mode Register
03	0	1	Interrupt Control Register 0
04	0	1	Interrupt Control Register 1
COUNTERS (CLOCK CALENDAR)			
05	0	X	1/100, 1/10 Seconds (0-99)
06	0	X	Seconds (0-59)
07	0	X	Minutes (0-59)
08	0	X	Hours (1-12, 0-23)
09	0	X	Days of Month (1-28/29/30/31)
0A	0	X	Months (1-12)
0B	0	X	Years (0-99)
0C	0	X	Julian Date (LSB) (1-99)
0D	0	X	Julian Date (0-3)
0E	0	X	Day of Week (1-7)
TIMER DATA REGISTERS			
0F	0	X	Timer 0 LSB
10	0	X	Timer 0 MSB
11	0	X	Timer 1 LSB
12	0	X	Timer 1 MSB
TIMER COMPARE RAM			
13	0	X	Sec Compare RAM (0-59)
14	0	X	Min Compare RAM (0-59)
15	0	X	Hours Compare RAM (1-12, 0-23)
16	0	X	DOM Compare RAM (1-28/29/30/31)
17	0	X	Months Compare RAM (1-12)
18	0	X	DOW Compare RAM (1-7)
TIME SAVE RAM			
19	0	X	Seconds Time Save RAM
1A	0	X	Minutes Time Save RAM
1B	0	X	Hours Time Save RAM
1C	0	X	Day of Month Time Save RAM
1D	0	X	Months Time Save RAM
1E	0	1	RAM
1F	0	X	RAM/Test Mode Register
01-1F	1	X	2nd Page General Purpose RAM

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block or the page selected.

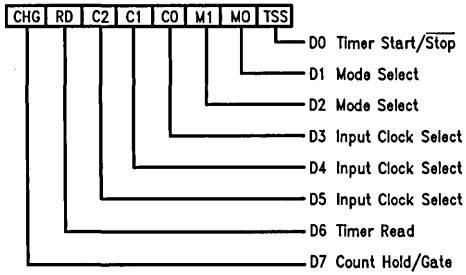
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3-D5 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1-D5: These five bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1, D3-D5 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

Functional Description (Continued)

TIMER 0 AND 1 CONTROL REGISTER



TL/F/9979–17

These registers control the operation of the timers. Each timer has its own register.

D0: This bit will Start (1) or Stop (0) the timer. When the timer is stopped the timer's prescaler and counter are reset, and the timer will restart from the beginning when started again. In mode 0 on time out the TSS bit is internally reset.

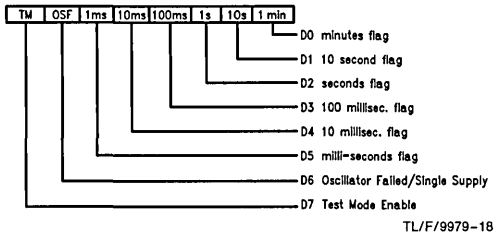
D1 and D2: These control the count mode of the timers. See Table VI.

D3–D5: These bits control which clock signal is applied to the timer's counter input. Refer to Table IV for details.

D6: This is the read bit. If a one is written into this location it will cause the contents of the timer to be latched into a holding register, which can be read by the μP at any time. Reading the least significant byte of the timer will reset the RD bit. The timer read cycle can be aborted by writing RD to zero.

D7: The CHG bit has two mode dependent functions. In modes 0 through 2 writing a one to this bit will suspend the timer operation (without resetting the timer prescaler). However, in mode 3 this bit is used to trigger or re-trigger the count sequence as with the gate pins. If retriggering is desired using the CHG bit, it is not necessary to write a zero to this location prior to the re-trigger. The action of further writing a one to this bit will re-trigger the count.

PERIODIC FLAG REGISTER



TL/F/9979–18

The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

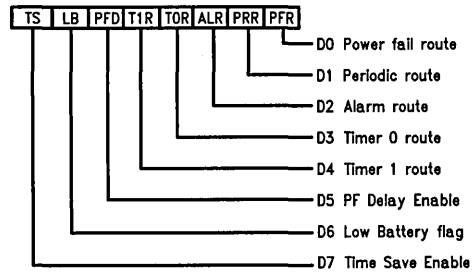
D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. This bit is automatically set on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/$\overline{\text{stop}}$ bit in the Real Time Mode Register, with the crystal oscillating.

When D6 is written to, it defines whether the TCP is being used in battery standby (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single supply mode applications. This bit is automatically set on initial power-up or an oscillator fail event. This disables the oscillator reference circuit, and requires that V_{BB} is connected to ground, and the single supply mode connected to V_{CC}. When this bit is set to zero, the oscillator reference is enabled. This allows operation in standard battery standby application.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table VII). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

INTERRUPT ROUTING REGISTER



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D0–D4: The lower 5 bits of this register are associated with the main interrupt sources created by this chip. The purpose of this register is to route the interrupts to either the MFO (multi-function pin), or to the main interrupt pin. When any bit is set the associated interrupt signal will be sent to the MFO pin, and when zero it will be sent to the INTR pin.

Functional Description (Continued)

D5: The Delay Enable bit is used when a power fail occurs.

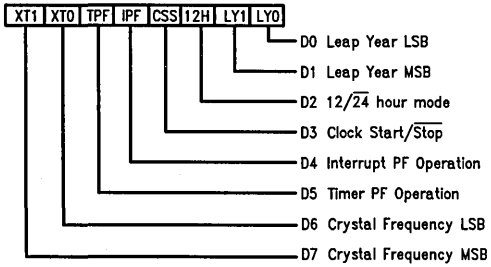
If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



TL/F/9979–20

D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the TCP is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Timer interrupts will also be functional provided that bit D5 is also set. Note that the MFO and INTR pins are configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register 0 and bits D6 and D7 of interrupt control register 1 will be reset when the TCP enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5: This bit controls the operation of the timers in standby mode. If set to a one the timers will continue to function when the TCP is in standby mode. The input pins TCK, G0, G1 are locked out in standby mode, and cannot be used.

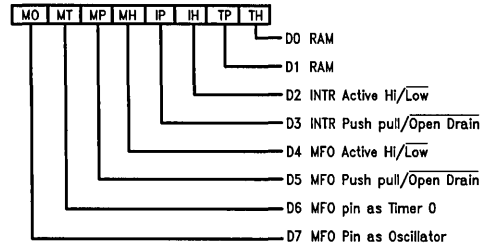
Therefore external control of the timers is not possible in standby mode. Note also that MFO and T1 pins are automatically reconfigured open drain during standby.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



TL/F/9979–21

Functional Description (Continued)

D0 and D1: These bits are available as general purpose RAM.

D2: This bit, when set to a one makes the INTR output pin active high, and when set to a zero, it makes this pin active low.

D3: This bit controls whether the INTR pin is an open drain or push-pull output. A one indicates push-pull.

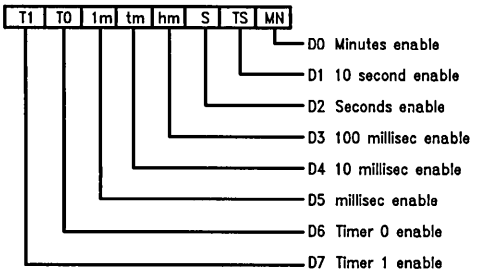
D4: This bit, when set to a one makes the MFO output pin active high, and when set to a zero, it makes this pin active low.

D5: This bit controls whether the MFO pin is an open drain or push-pull output. A one indicates push-pull.

D6 and D7: These bits are used to program the signal appearing at the MFO output, as follows:

D7	D6	MFO Output Signal
0	0	2nd Interrupt
0	1	Timer 0 Waveform
1	X	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0

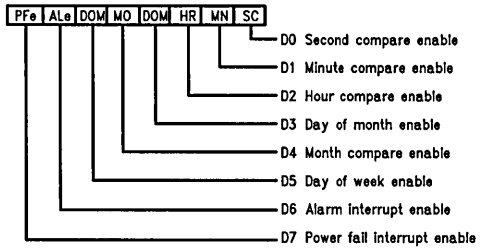


TL/F/9979–22

D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: These are individual timer enable bits. A one written to these bits enable the timers to generate interrupts to the μP.

INTERRUPT CONTROL REGISTER 1



TL/F/9979–23

D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $\overline{\text{PFAIL}} = 0$.

This bit also enables the low battery detection analog circuitry.

If the user wishes to mask the power fail interrupt, but utilize the analog circuitry, this bit should be enabled, and the Routing Register can be used to route the interrupt to the MFO pin. The MFO pin can then be left open or configured as the Timer 0 or buffered oscillator output.

Control and Status Register Address Bit Map

Main Status Register PS = 0 RS = 0 ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R[1]	R[1]	R[1]	R[1]	R[2]	R[3]
Page Select	Register Select	Timer 1 Interrupt	Timer 0 Interrupt	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed.

Timer 0 Control Register PS = 0 RS = 0 Address = 01H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Timer 1 Control Register PS = 0 RS = 0 Address = 02H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Interrupt Routing Register PS = 0 RS = 0 Address = 04H

R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	Timer 1 Int. Route MFO/$\overline{INT}$	Timer 0 Int. Route MFO/$\overline{INT}$	Alarm Int. Route MFO/$\overline{INT}$	Periodic Int. Route MFO/$\overline{INT}$	Power Fail Int. Route MFO/$\overline{INT}$

6. Set and reset by V_{BB} voltage.

Real Time Mode Register PS = 0 RS = 1 Address = 01H

Crystal Freq. XT1	Crystal Freq. XT0	Timers EN on Back-Up	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	MFO as Timer 0	MFO PP/$\overline{OD}$	MFO Active HI/$\overline{LO}$	INTR PP/$\overline{OD}$	INTR Active HI/$\overline{LO}$	RAM	RAM

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

Timer 1 Interrupt Enable	Timer 0 Interrupt Enable	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

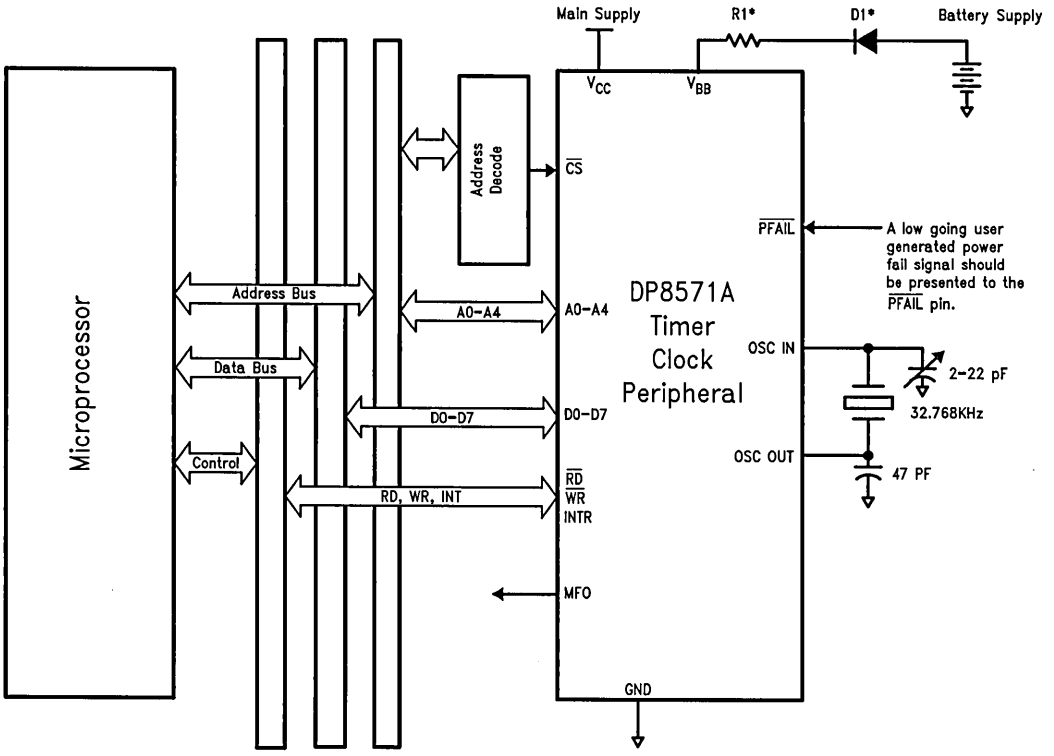
All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

Typical Application



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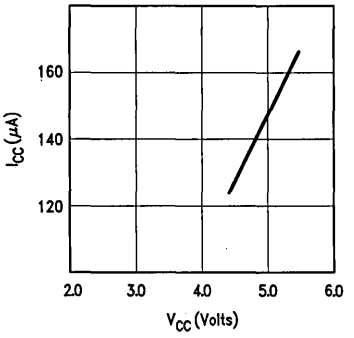
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode F_{OSC} = 32.768 kHz)



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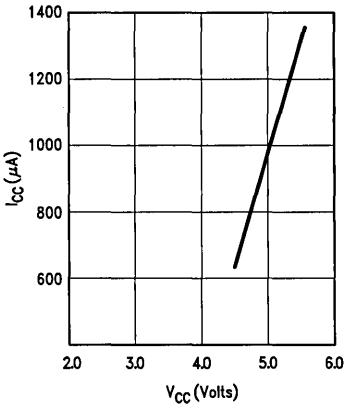
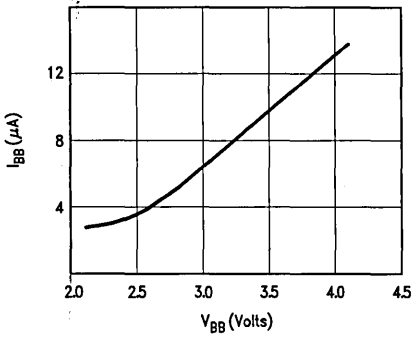
Operating Current vs Supply Voltage (Battery Backed Mode F_{OSC} = 32.768 kHz)



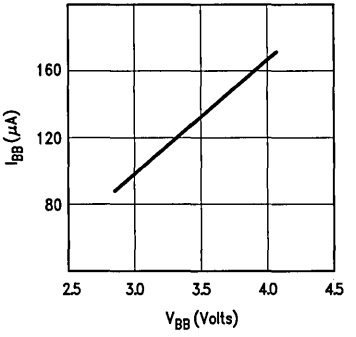
TL/F/9979–26

Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



TL/F/9979–27

Standby Current vs Power Supply Voltage F_{OSC} = 4.194304 MHz



TL/F/9979–28

National Semiconductor

PRELIMINARY

DP8572A Real Time Clock (RTC)

General Description

The DP8572A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

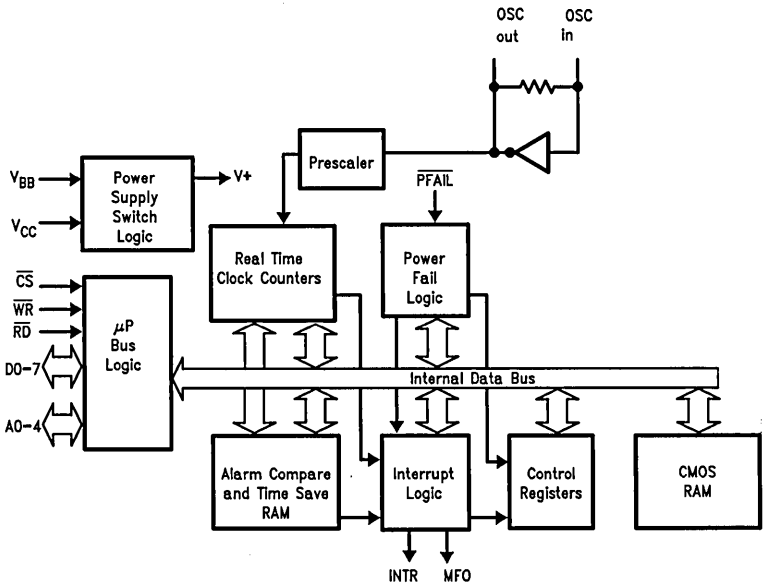
Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Power failure logic and control functions have been integrated on chip. This logic is used by the RTC to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided, and upon power failure detection, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel resonant oscillator
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, and power fail interrupts
- Up to 44 bytes of CMOS RAM

Block Diagram



TL/F/9980–1

FIGURE 1

1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	4.5	5.5	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV

DC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} −0.1		V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock		0.8 0.1	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −4.0 mA	V_{CC} −0.1 3.5		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 4.0 mA		0.1 0.25	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5.0	μA
I_{LKG}	Output High Leakage Current T1, MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5.0	μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		250 1.0 12.0	μA mA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		8 20	mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		40 7.5	μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 7)	V_{CC} = GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		10 400	μA μA
I_{BLK}	Battery Supply Leakage	2.2V ≤ V_{BB} ≤ 4.0V	−5	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, V_{BB} ≤ V_{CC} −0.4V.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 4.5V ≤ V_{CC} ≤ 5.5V.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	20		ns
t_{RW}	Read Strobe Width (Note 8)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 9)	3		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		60	ns
t_{RCH}	Chip Select Hold after Read Strobe	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	50		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	20		ns
t_{WAH}	Address Hold after Write Strobe (Note 9)	3		ns
t_{CW}	Chip Select to End of Write Strobe	90		ns
t_{WW}	Write Strobe Width (Note 10)	80		ns
t_{DW}	Data Valid to End of Write Strobe	50		ns
t_{WDH}	Data Hold after Write Strobe (Note 9)	3		ns
t_{WCH}	Chip Select Hold after Write Strobe	0		ns

Note 8: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 9: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

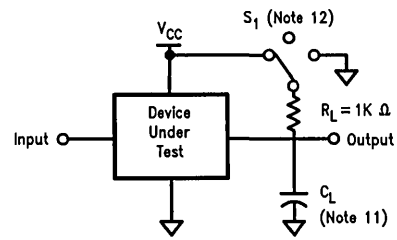
Note 10: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 12)	Active High +0.5V Active Low −0.5V

Note 11: C_L = 100 pF, includes jig and scope capacitance.

Note 12: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



TL/F/9980–2

Capacitance (T_A = 25°C, f = 1 MHz)

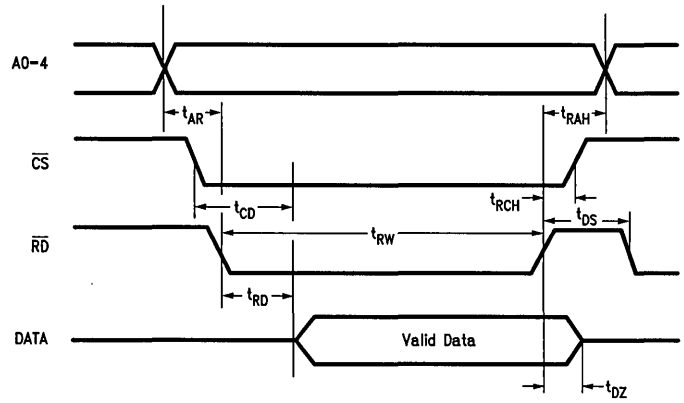
Symbol	Parameter (Note 13)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

Note 13: This parameter is not 100% tested.

Note 14: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

Timing Waveforms

Read Timing Diagram



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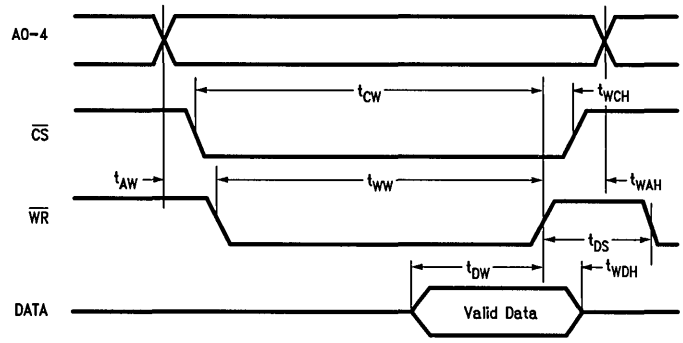
Write Timing Diagram



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General Description (Continued)

The DP8572A's interrupt structure provides three basic types of interrupts: Periodic, Alarm/Compare, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the RTC. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input); OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator. The MFO output is configured as push-pull, active high for normal or single power supply operation and as an open drain during standby mode. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output is permanently configured active low, open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the RTC. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the RTC goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

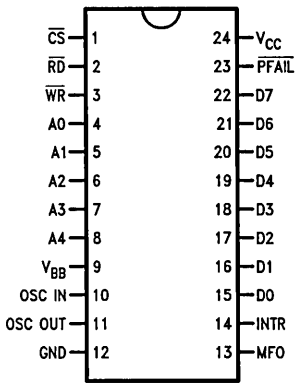
V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the RTC programmed for single power supply only, and power applied to the V_{CC} pin.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line



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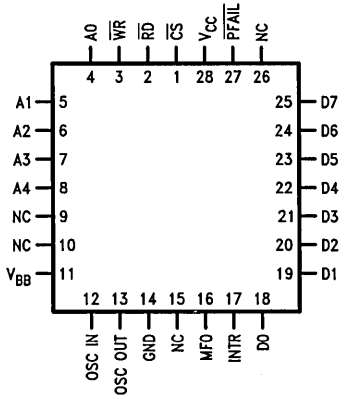
Top View

Order Number DP8572AN
See NS Package Number N24C

Plastic Chip Carrier



TL/F/9980–6

Top View

Order Number DP8572AV
See NS Package Number V28A

Functional Description

The DP8572A contains a fast access real time clock, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the RTC are controlled by a set of seven registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1*.

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management

The memory map of the RTC is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.

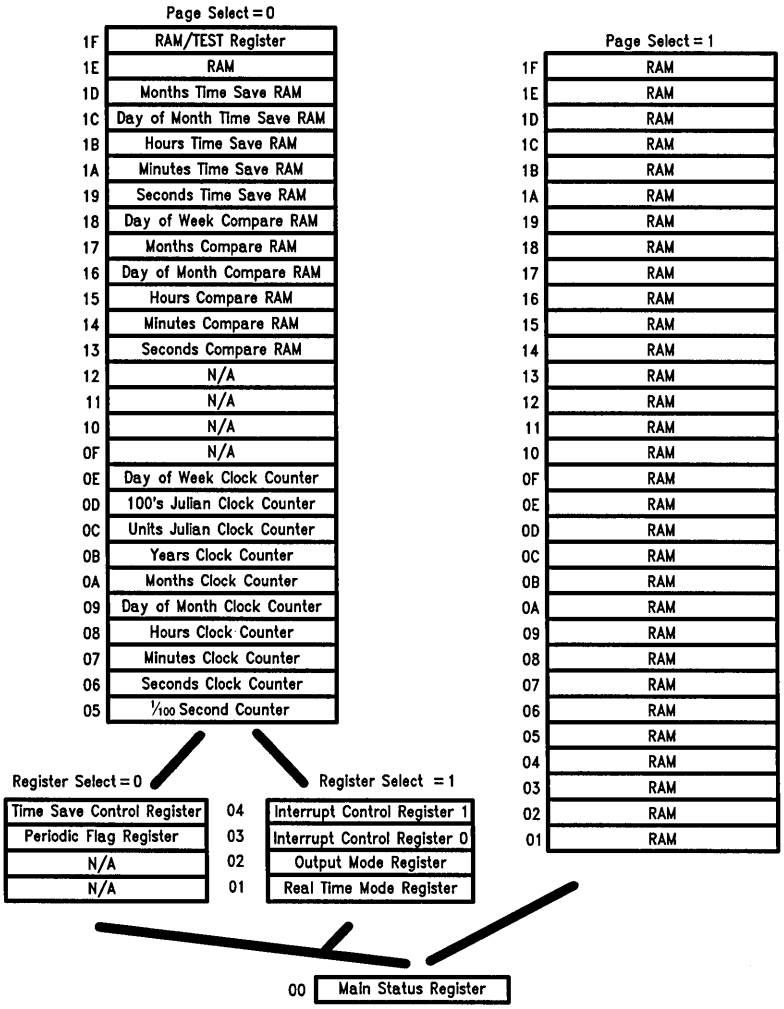


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FIGURE 2. DP8572A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the DP8572A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the RTC is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Time Save Control Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the RTC or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.768 kHz, 4.9152 MHz, and 4.194304 MHz.

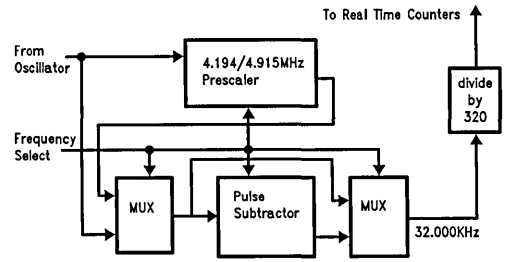

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FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

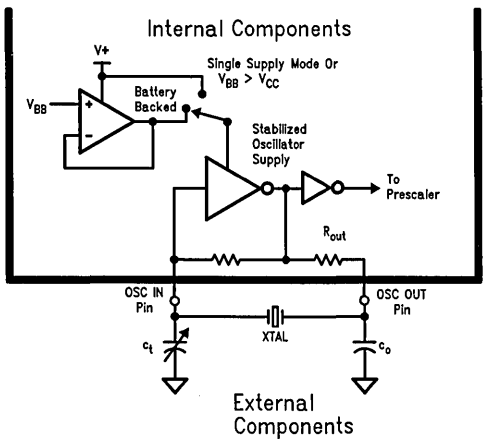

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FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The RTC has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all RTC interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the RTC to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system. (The Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.)

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm comparisons that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the Alarm interrupt enable bit is set (see *Figure 5*).

Disabling the periodic interrupts will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2 and D3 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Three Categories:

1. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
2. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
3. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The RTC then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the RTC when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the DP8572A provides circuitry to simplify design in battery backed systems. This switches over to the back up supply, and isolates itself from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{\text{PFAIL}}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{\text{PFAIL}}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

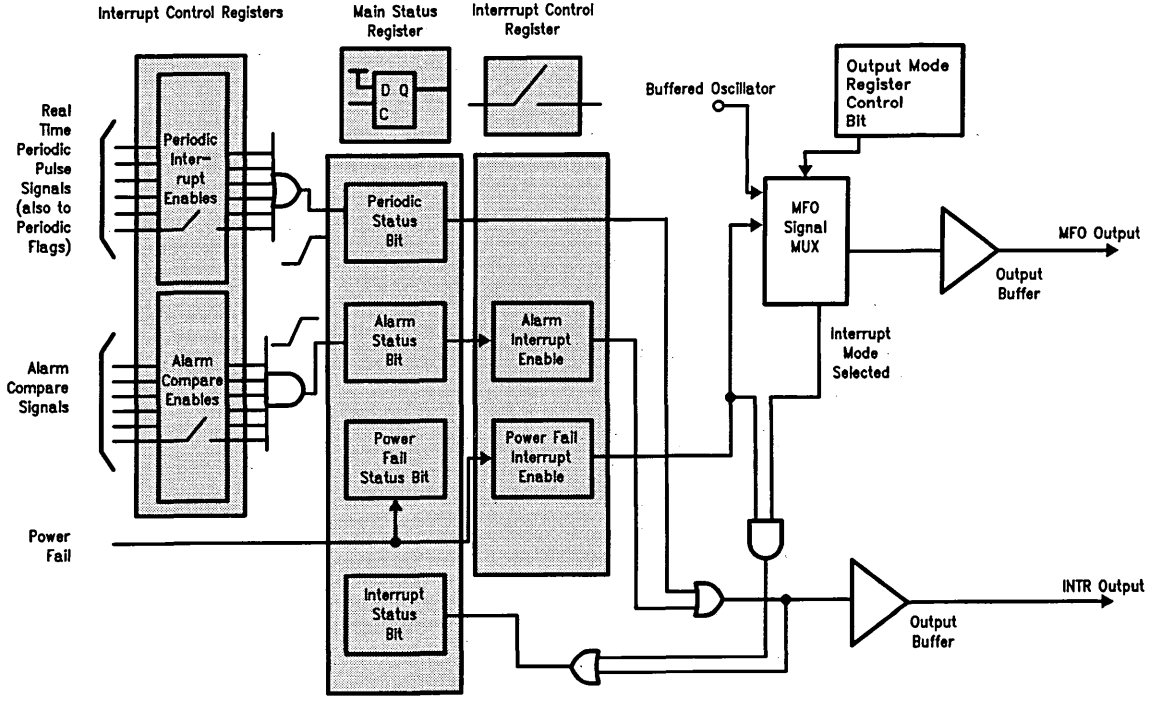

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FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

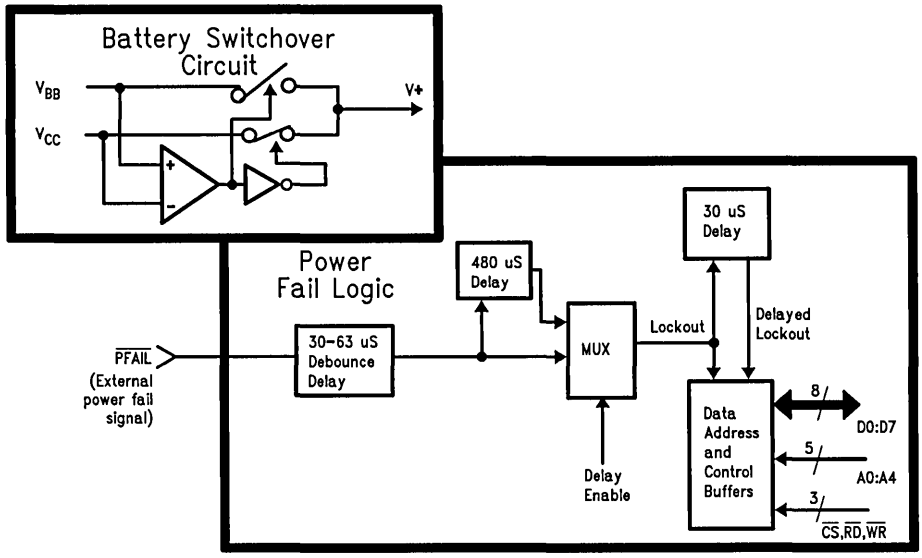

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the DP8572A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the RTC it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{PFAIL}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the RTC will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the RTC will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{PFAIL}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
$\overline{PFAIL}$	Not Isolated	Not Isolated
INTR, MFO	Not Isolated	Open Drain

The Interrupt Power Fail Operation bit in the Real-Time Mode Register determine whether or not the interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{PFAIL}$ = 0. When $\overline{PFAIL}$ = 1

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the DP8572A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The DP8572A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC}. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the DP8572A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 28 locations at one time. An internal switching scheme provides a total of 61 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table III. They show the name, address and page locations for the DP8572A.

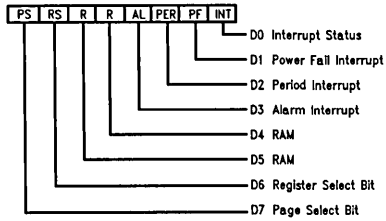
TABLE III. Register/Counter/RAM Addressing for DP8572A

A0-4	PS (Note 1)	RS (Note 2)	Description
CONTROL REGISTERS			
00	X	X	Main Status Register
01	0	0	Timer 0 Control Register
02	0	0	Timer 1 Control Register
03	0	0	Periodic Flag Register
04	0	0	Interrupt Routing Register
01	0	1	Real Time Mode Register
02	0	1	Output Mode Register
03	0	1	Interrupt Control Register 0
04	0	1	Interrupt Control Register 1
COUNTERS (CLOCK CALENDAR)			
05	0	X	1/100, 1/10 Seconds (0-99)
06	0	X	Seconds (0-59)
07	0	X	Minutes (0-59)
08	0	X	Hours (1-12, 0-23)
09	0	X	Days of Month (1-28/29/30/31)
0A	0	X	Months (1-12)
0B	0	X	Years (0-99)
0C	0	X	Julian Date (LSB) (1-99)
0D	0	X	Julian Date (0-3)
0E	0	X	Day of Week (1-7)
TIMER DATA REGISTERS			
0F	0	X	Timer 0 LSB
10	0	X	Timer 0 MSB
11	0	X	Timer 1 LSB
12	0	X	Timer 1 MSB
TIMER COMPARE RAM			
13	0	X	Sec Compare RAM (0-59)
14	0	X	Min Compare RAM (0-59)
15	0	X	Hours Compare RAM (1-12, 0-23)
16	0	X	DOM Compare RAM (1-28/29/30/31)
17	0	X	Months Compare RAM (1-12)
18	0	X	DOW Compare RAM (1-7)
TIME SAVE RAM			
19	0	X	Seconds Time Save RAM
1A	0	X	Minutes Time Save RAM
1B	0	X	Hours Time Save RAM
1C	0	X	Day of Month Time Save RAM
1D	0	X	Months Time Save RAM
1E	0	1	RAM
1F	0	X	RAM/Test Mode Register
01-1F	1	X	2nd Page General Purpose RAM

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

Functional Description (Continued)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block or the page selected.

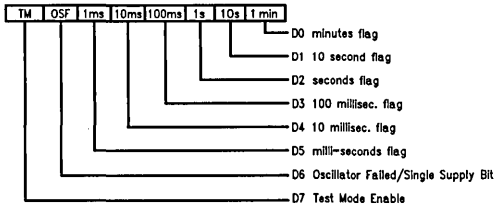
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1–D3: These three bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1 and D3 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D4–D5: General purpose RAM bits.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

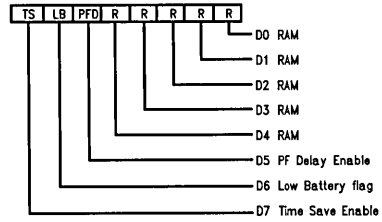
D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. This bit is automatically set on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/$\overline{\text{stop}}$ bit in the Real Time Mode Register, with the crystal oscillating.

When D6 is written to, it defines whether the RTC is being used in battery standby (normal) or in a single supply mode application. When set to a one this bit configures the RTC for single supply mode applications. This bit is automatically set on initial power-up or an oscillator fail event. This disables the oscillator reference circuit, and requires that V_{BB} is connected to ground, and the single supply mode connected to V_{CC}. When this bit is set to zero, the oscillator reference is enabled. This allows operation in standard battery standby application.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table III). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

TIME SAVE CONTROL REGISTER



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D0–D4: General purpose RAM bits.

Functional Description (Continued)

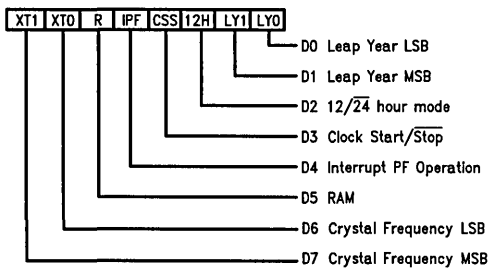
D5: The Delay Enable bit is used when a power fail occurs. If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



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D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the RTC is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Note that the MFO pin is configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register and the periodic interrupt flag will be reset when the RTC enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

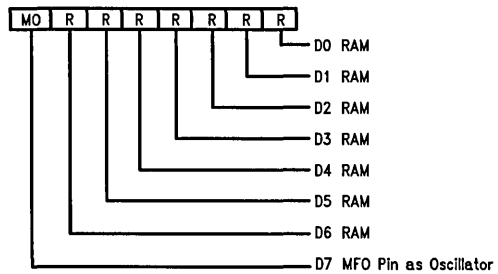
D5: General purpose RAM.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



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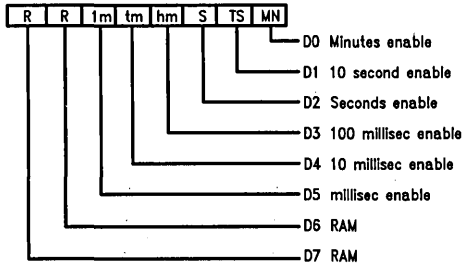
D0–D6: General Purpose RAM

Functional Description (Continued)

D7: This bit is used to program the signal appearing at the MFO output, as follows:

D7	MFO Output Signal
0	Power Fail Interrupt
1	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0



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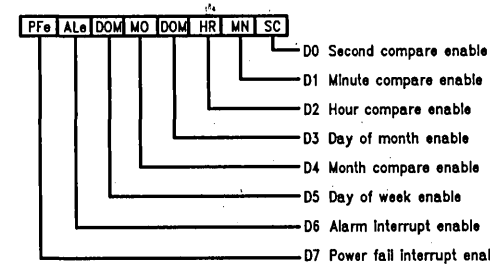
D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: General Purpose RAM.

INTERRUPT CONTROL REGISTER 1



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D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $\overline{\text{PFAIL}}$ = 0.

This bit also enables the low battery detection analog circuitry.

Control and Status Register Address Bit Map

Main Status Register PS = X RS = X ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R[1]	R[1]	R[2]	R[3]
Page Select	Register Select	RAM	RAM	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed.

Periodic Flag Register PS = 0 RS = 0 Address = 03H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Time Save Control Register PS = 0 RS = 0 Address = 04H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	RAM	RAM	RAM	RAM	RAM

6. Set and reset by V_{BB} voltage.

Real Time Mode Register PS = 0 RS = 1 Address = 01H

D7	D6	D5	D4	D3	D2	D1	D0
Crystal Freq. XT1	Crystal Freq. XT0	RAM	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

D7	D6	D5	D4	D3	D2	D1	D0
MFO as Crystal	RAM	RAM	RAM	RAM	RAM	RAM	RAM

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

D7	D6	D5	D4	D3	D2	D1	D0
RAM	RAM	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

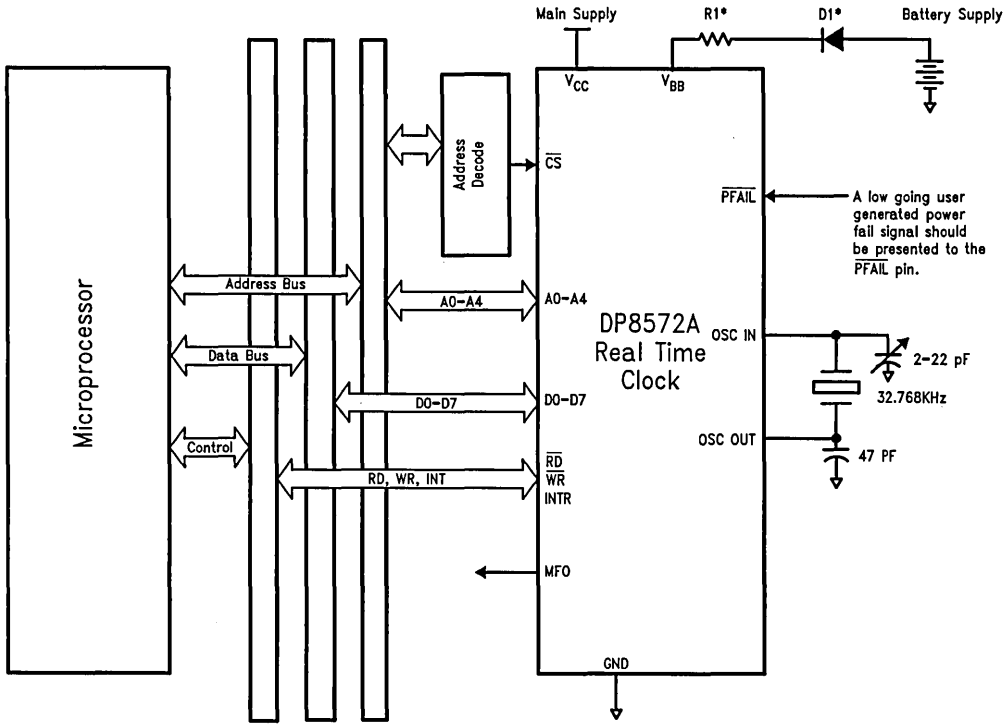
All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

D7	D6	D5	D4	D3	D2	D1	D0
Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

Typical Application



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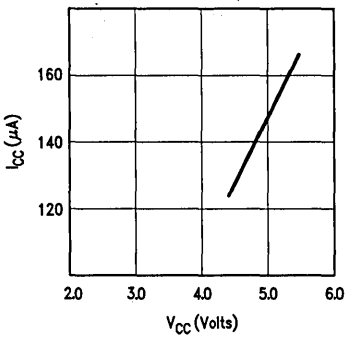
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode F_{OSC} = 32.768 kHz)



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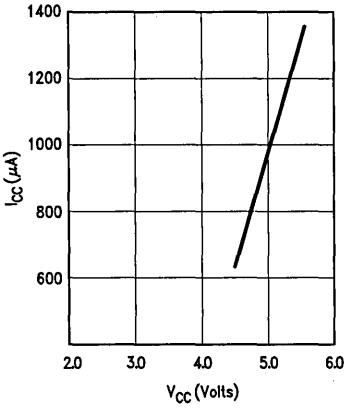
Operating Current vs Supply Voltage (Battery Backed Mode F_{OSC} = 32.768 kHz)



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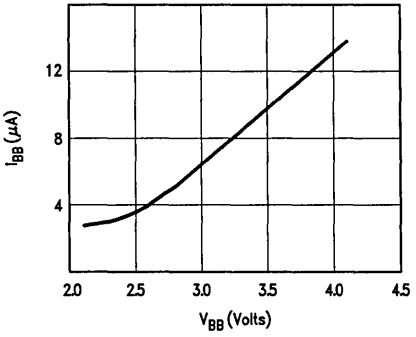
Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



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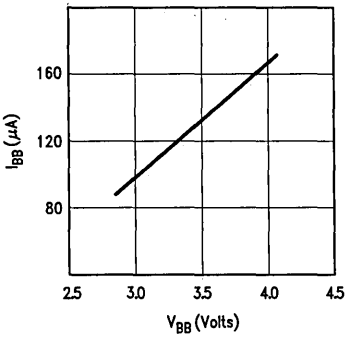
Standby Current vs Power Supply Voltage F_{OSC} = 4.194304 MHz



TL/F/9980–23

National Semiconductor

PRELIMINARY

DP8573A Real Time Clock (RTC)

General Description

The DP8573A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports organized as one block of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, and the Time Save RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week and day of month counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the 32.768 kHz crystal and two capacitors.

Power failure logic and control functions have been integrated on chip. This logic is used by the RTC to issue a power fail interrupt, and lock out the μP interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided, and upon power failure detection, internal circuitry will automatically switch from the main supply to the battery supply.

The DP8573A's interrupt structure provides three basic types of interrupts: Periodic, Alarm/Compare, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

Features

- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week counter
  - Parallel resonant oscillator
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, and power fail interrupts

Block Diagram

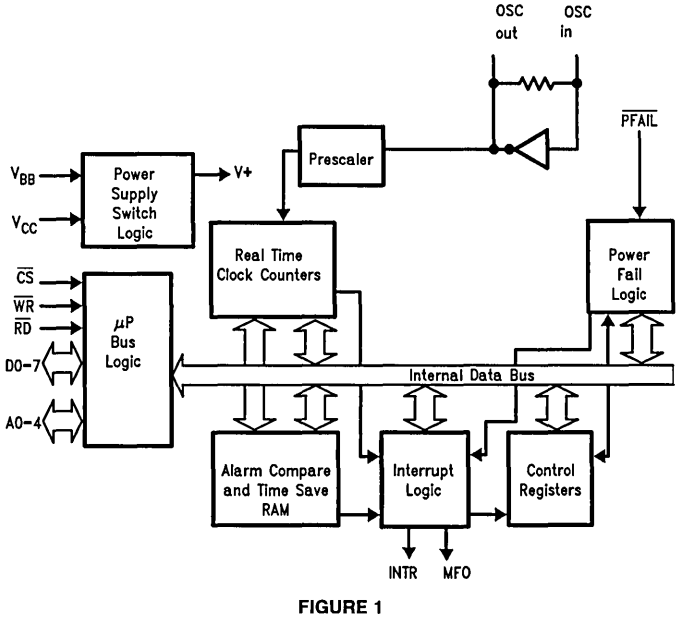


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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	4.5	5.5	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC}−0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating		1	kV

DC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} −0.1		V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock		0.8 0.1	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −4.0 mA	V_{CC} −0.1 3.5		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 4.0 mA		0.1 0.25	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5.0	μA
I_{LKG}	Output High Leakage Current T1, MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5.0	μA
I_{CC}	Quiescent Supply Current (Note 6)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		 250 1.0 12.0	 μA mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz		40	μA
I_{BB}	Standby Mode Battery Supply Current (Note 7)	V_{CC} = GND F_{OSC} = 32.768 kHz		10	μA
I_{BLK}	Battery Supply Leakage	2.2V ≤ V_{BB} ≤ 4.0V	−5	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: In battery backed mode, $V_{BB} \leq V_{CC} - 0.4V$.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) $4.5V \leq V_{CC} \leq 5.5V$.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out.

AC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, $V_{\overline{PFAIL}} > V_{IH}$, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	20		ns
t_{RW}	Read Strobe Width (Note 8)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 9)	3		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		60	ns
t_{RCH}	Chip Select Hold after Read Strobe	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	50		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	20		ns
t_{WAH}	Address Hold after Write Strobe (Note 9)	3		ns
t_{CW}	Chip Select to End of Write Strobe	90		ns
t_{WW}	Write Strobe Width (Note 10)	80		ns
t_{DW}	Data Valid to End of Write Strobe	50		ns
t_{WDH}	Data Hold after Write Strobe (Note 9)	3		ns
t_{WCH}	Chip Select Hold after Write Strobe	0		ns

Note 8: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 9: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

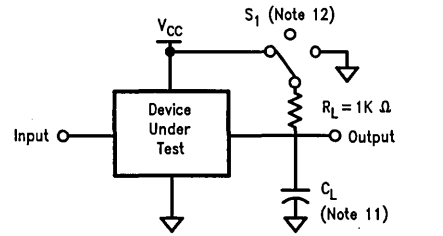
Note 10: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 12)	Active High +0.5V Active Low −0.5V

Note 11: C_L = 100 pF, includes jig and scope capacitance.

Note 12: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



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Capacitance (T_A = 25°C, f = 1 MHz)

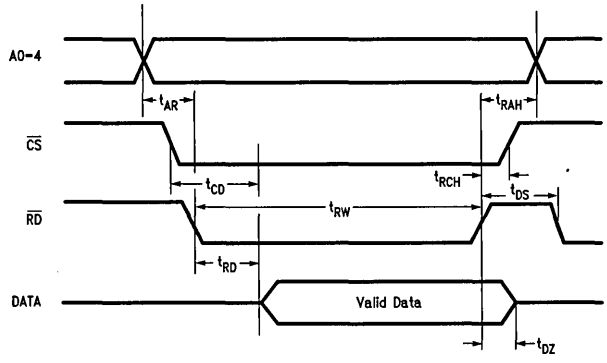
Symbol	Parameter (Note 14)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

Note 13: This parameter is not 100% tested.

Note 14: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

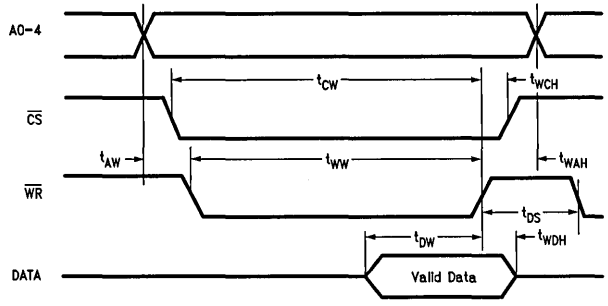
Timing Waveforms

Read Timing Diagram



TL/F/9981-3

Write Timing Diagram



TL/F/9981-4

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the RTC. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0-A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input): OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator. The MFO output is configured as push-pull, active high for normal or single power supply operation and as an open drain during standby mode. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output is permanently configured active low, open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0-D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the RTC. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the RTC goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

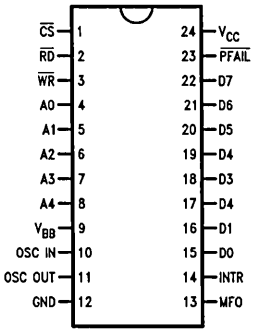
V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the RTC programmed for single power supply only, and power applied to the V_{CC} pin.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line

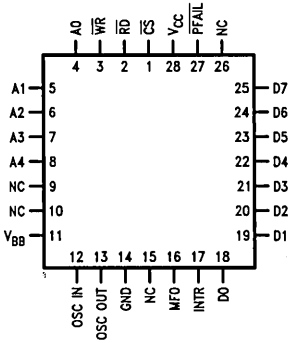


TL/F/9981–5

Top View

Order Number DP8573AN
See NS Package Number N24C

Plastic Chip Carrier



TL/F/9981–6

Top View

Order Number DP8573AV
See NS Package Number V28A

Functional Description

The DP8573A contains a fast access real time clock, interrupt control logic, and power fail detect logic. All functions of the RTC are controlled by a set of seven registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1.*

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management

The memory map of the RTC is shown in the memory addressing table *(Figure 2).* A control bit in the Main Status Register is used to select either control register block.

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the DP8573A is configured for single supply mode, an extra 50 μA may be consumed until the crystal select bits are programmed. The user should also ensure that the RTC is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 8 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Upon initial application of power the counters will contain random information.

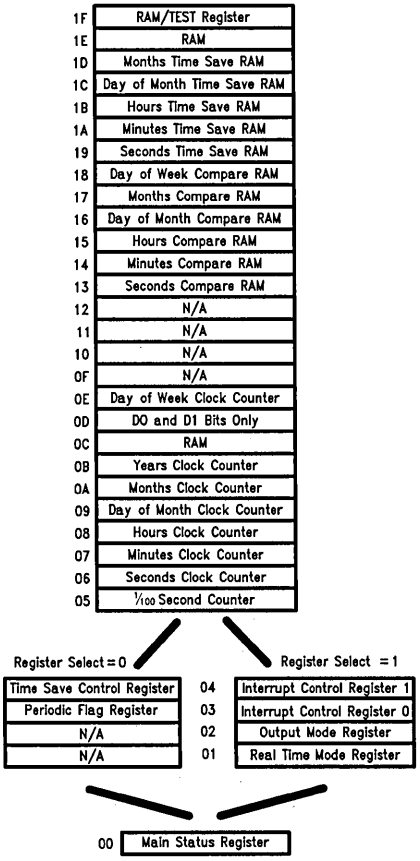


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FIGURE 2. DP8573A Internal Memory Map

Functional Description (Continued)

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Time Save Control Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM if the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register a second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hours for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 μs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*).

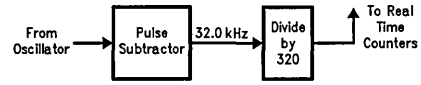

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FIGURE 3. Programmable Clock Prescaler Block

In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the **load capacitance** specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).

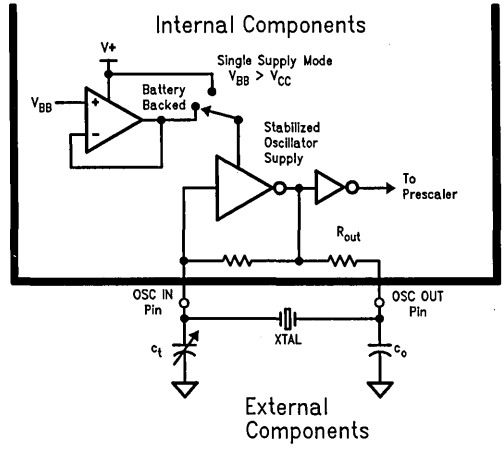

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FIGURE 4. Oscillator Circuit Diagram

Functional Description (Continued)

XTAL	C_O	C_t	R_{OUT}
32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The RTC has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Address
Main Status Register	X	00H
Periodic Flag Register	0	03H
Interrupt Control Register 0	1	03H
Interrupt Control Register 1	1	04H
Output Mode Register	1	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all RTC interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the RTC to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system. (The Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.)

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm comparisons that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the Alarm interrupt enable bit is set (see *Figure 5*).

Disabling the periodic interrupts will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2 and D3 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Interrupts Fall Into Three Categories:

1. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
2. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
3. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{\text{PFAIL}}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The RTC then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

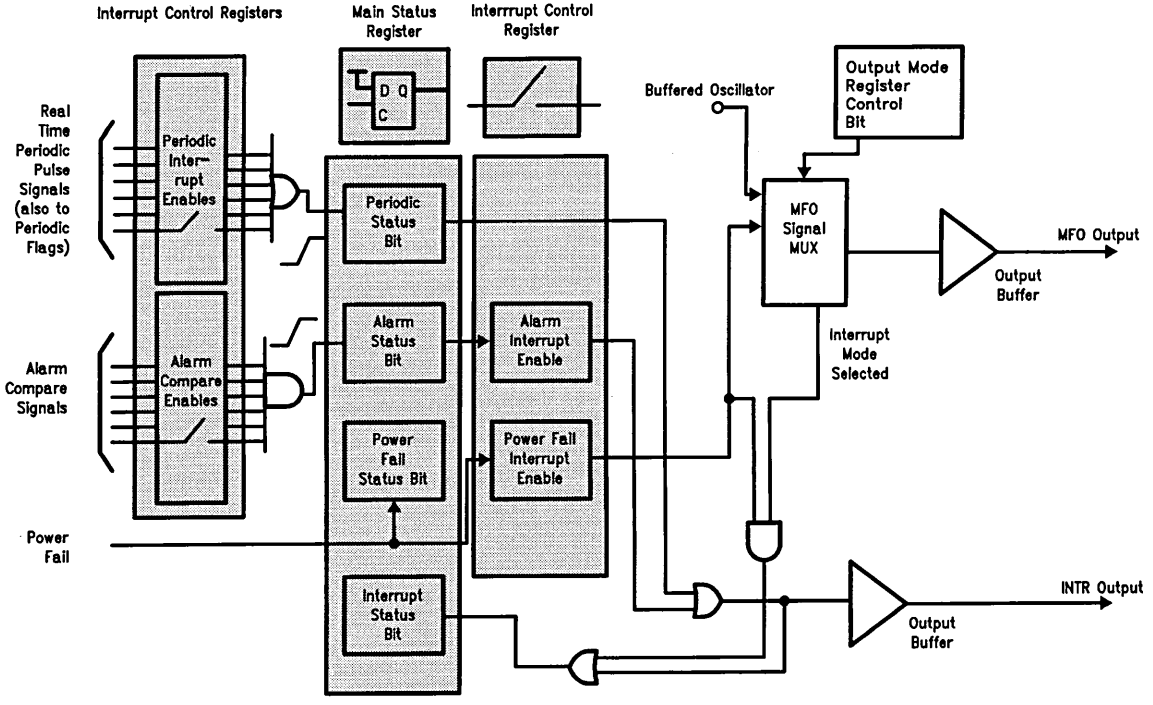

FIGURE 5. Interrupt Control Logic Overview

Functional Description (Continued)

POWER FAIL INTERRUPTS DESCRIPTION

The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the RTC when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

Since the clock must be operated from a battery when the main system supply has been turned off, the DP8573A provides circuitry to simplify design in battery backed systems. This switches over to the back up supply, and isolates itself from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic: 2) battery switch over logic: and 3) isolation logic.

Detection of power loss occurs when $\overline{PFAIL}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{PFAIL}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.

If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced.

The battery switch over circuitry is completely independent of the $\overline{PFAIL}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the RTC will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the RTC will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{PFAIL}$ = Logic 0	Standby Mode $V_{BB} > V_{CC}$
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	Locked Out	Locked Out
A0–A4	Locked Out	Locked Out
D0–D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
$\overline{PFAIL}$	Not Isolated	Not Isolated
INTR, MFO	Not Isolated	Open Drain

The Interrupt Power Fail Operation bit in the Real-Time Mode Register determines whether or not the interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{PFAIL}=0$. When $\overline{PFAIL}=1$ the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no ex-

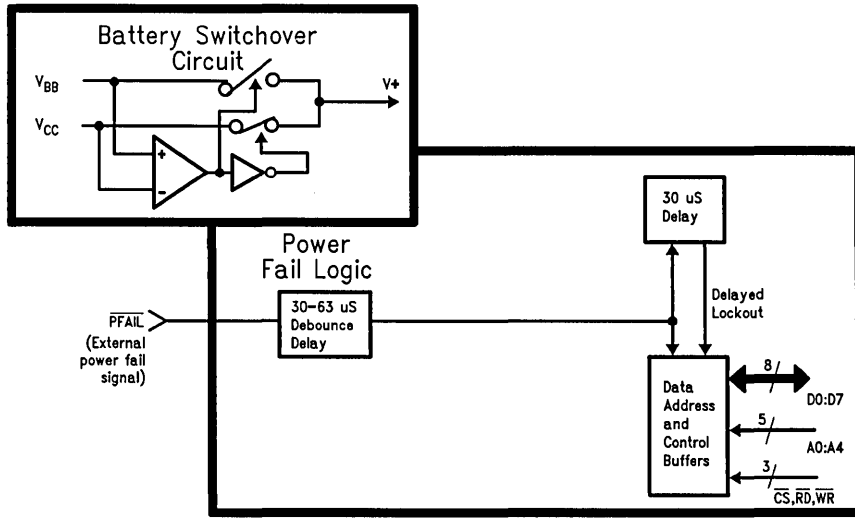

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FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

Functional Description (Continued)

ternal interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

INITIAL POWER ON DETECT AND POWER FAIL TIME SAVE

There are two other functions provided on the DP8573A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The DP8573A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC}. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 28 locations at one time. An internal switching scheme provides a total of 30 locations.

The only register that does not get switched is the Main Status Register. It contains the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table III. They show the name, address and page locations for the DP8573A.

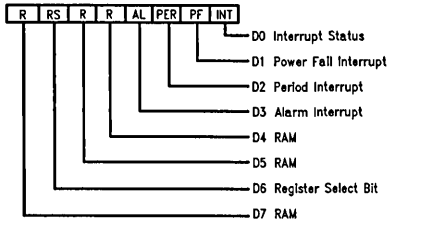
TABLE III. Register/Counter/RAM Addressing for DP8573A

A0-4	RS (Note 1)	Description	
CONTROL REGISTERS			
00	X	Main Status Register	
01	0	N/A	
02	0	N/A	
03	0	Periodic Flag Register	
04	0	Time Save Control Register	
01	1	Real Time Mode Register	
02	1	Output Mode Register	
03	1	Interrupt Control Register 0	
04	1	Interrupt Control Register 1	
COUNTERS (CLOCK CALENDAR)			
05	X	1/100, 1/10 Seconds	(0–99)
06	X	Seconds	(0–59)
07	X	Minutes	(0–59)
08	X	Hours	(1–12, 0–23)
09	X	Days of Month	(1–28/29/30/31)
0A	X	Months	(1–12)
0B	X	Years	(0–99)
0C	X	RAM	
0D	X	D0, D1 bits only	
0E	X	Day of Week	(1–7)
0F	X	N/A	
10	X	N/A	
11	X	N/A	
12	X	N/A	
TIME COMPARE RAM			
13	X	Sec Compare RAM	(0–59)
14	X	Min Compare RAM	(0–59)
15	X	Hours Compare RAM	(1–12, 0–23)
16	X	DOM Compare RAM	(1–28/29/30/31)
17	X	Months Compare RAM	(1–12)
18	X	DOW Compare RAM	(1–7)
TIME SAVE RAM			
19	X	Seconds Time Save RAM	
1A	X	Minutes Time Save RAM	
1B	X	Hours Time Save RAM	
1C	X	Day of Month Time Save RAM	
1D	X	Months Time Save RAM	
1E	1	RAM	
1F	X	RAM/Test Mode Register	

Note 1: RS—Register Select (Bit D6 of Main Status Register)

Functional Description (Continued)

MAIN STATUS REGISTER



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The Main Status Register is always located at address 0 regardless of the register block selected.

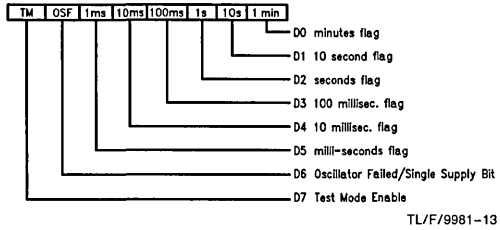
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1–D3: These three bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{\text{PFAIL}}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1 and D3 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D4, D5 and D7: General purpose RAM bits.

D6: Bit D6 controls the register block to be accessed (see memory map).

PERIODIC FLAG REGISTER



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The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0–D5 are read only bits, D6 and D7 are read/write.

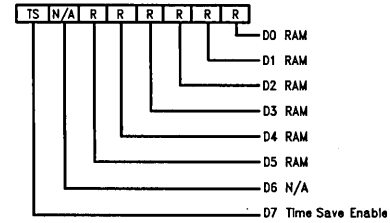
D0–D5: These bits are set by the real time rollover events: (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. This bit is automatically set on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/$\overline{\text{stop}}$ bit in the Real Time Mode Register, with the crystal oscillating.

When D6 is written to, it defines whether the RTC is being used in battery standby (normal) or in a single supply mode application. When set to a one this bit configures the RTC for single supply mode applications. This bit is automatically set on initial power-up or an oscillator fail event. This disables the oscillator reference circuit, and requires that V_{BB} is connected to ground, and the single supply mode connected to V_{CC}. When this bit is set to zero, the oscillator reference is enabled. This allows operation in standard battery standby application.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table III). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

TIME SAVE CONTROL REGISTER



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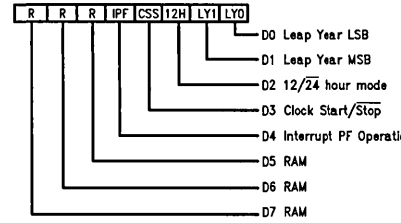
D0–D5: General purpose RAM bits.

D6: Not Available, appears as logic 0 when read.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



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Functional Description (Continued)

D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

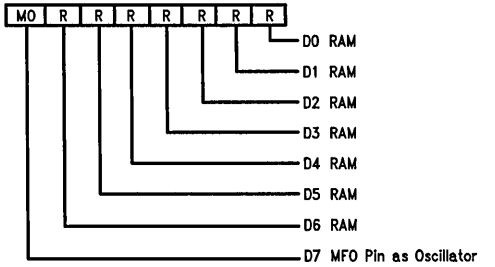
D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the RTC is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Note that the MFO pin is configured as open drain in standby mode.

If bit D4 is set to a zero then the interrupt control register and the periodic interrupt flag will be reset when the RTC enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5–D7: General purpose RAM bits.

OUTPUT MODE REGISTER



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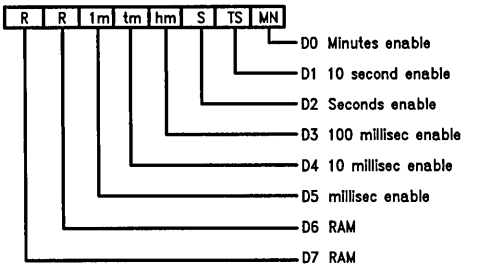
D0–D6: General purpose RAM bits.

D7: This bit is used to program the signal appearing at the MFO output, as follows:

D7	MFO Output Signal
0	Power Fail Interrupt
1	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0



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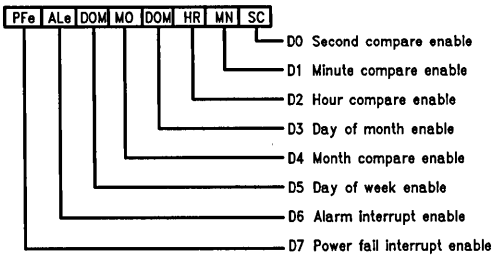
D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: General purpose RAM.

INTERRUPT CONTROL REGISTER 1



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D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when a $\overline{\text{PFAIL}}$ = 0.

Control and Status Register Address Bit Map

Main Status Register PS = X RS = X ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R^1	R^1	R^2	R^3
RAM	Register Select	RAM	RAM	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed.

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W^4	R^5	R^5	R^5	R^5	R^5	R^5
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fail Write 0 Batt-Backed Mode Write 1 Single Supply Mode
5. Reset by positive edge of read.

Time Save Control Register PS = 0 RS = 0 Address = 04H

Time Save Enable	N/A	RAM	RAM	RAM	RAM	RAM	RAM	All Bits R/W

Real Time Mode Register PS = 0 RS = 1 Address = 01H

RAM	RAM	RAM	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB	All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	RAM	RAM	RAM	RAM	RAM	RAM	RAM	All Bits R/W

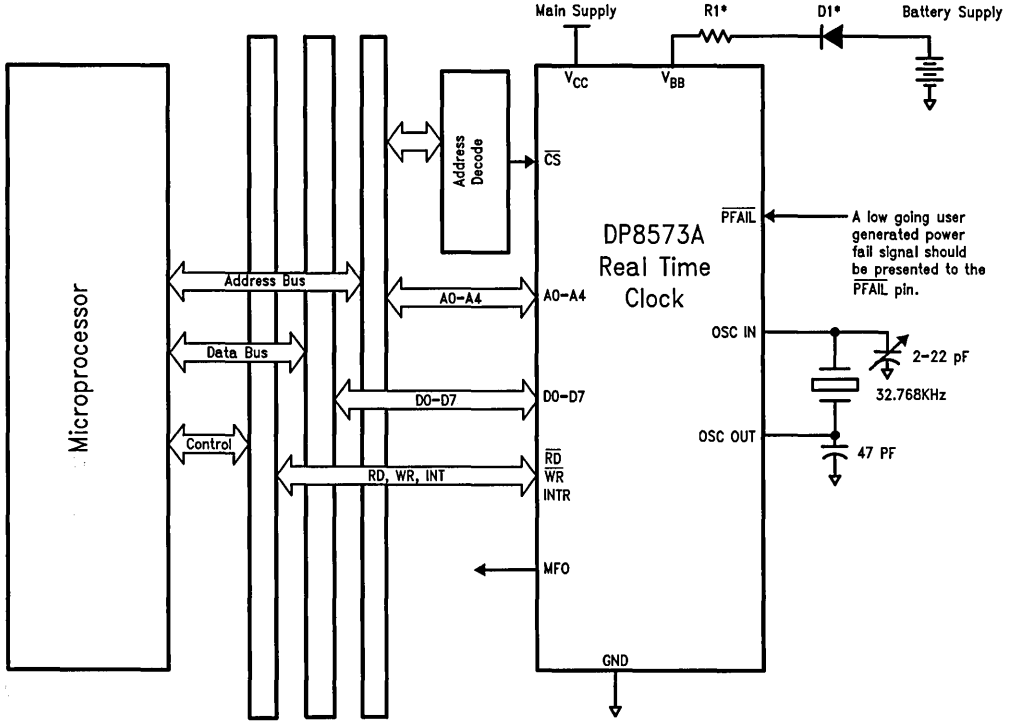
Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

RAM	RAM	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable	All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable	All Bits R/W

Typical Application



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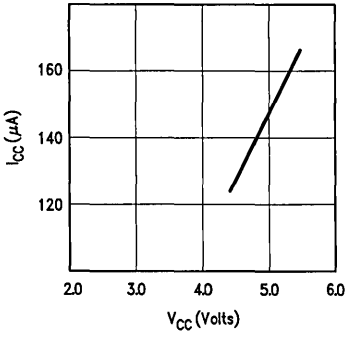
*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode F_{OSC} = 32.768 kHz)



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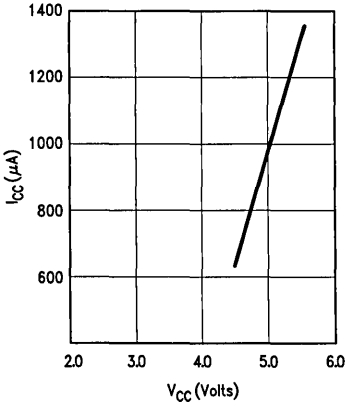
Operating Current vs Supply Voltage (Battery Backed Mode F_{OSC} = 32.768 kHz)



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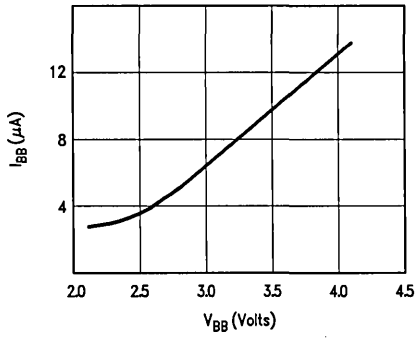
Typical Performance Characteristics (Continued)

Standby Current vs Power Supply Voltage (F_{OSC} = 32.768 kHz)



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National Semiconductor

MM58274C Microprocessor Compatible Real Time Clock

General Description

The MM58274C is fabricated using low threshold metal gate CMOS technology and is designed to operate in bus oriented microprocessor systems where a real time clock and calendar function are required. The on-chip 32.768 kHz crystal controlled oscillator will maintain timekeeping down to 2.2V to allow low power standby battery operation. This device is pin compatible with the MM58174B but continues timekeeping up to tens of years. The MM58274C is a direct replacement for the MM58274 offering improved Bus access cycle times.

Applications

- Point of sale terminals
- Teller terminals
- Word processors
- Data logging
- Industrial process control

Features

- Same pin-out as MM58174A and MM58274B
- Timekeeping from tenths of seconds to tens of years in independently accessible registers
- Leap year register
- Hours counter programmable for 12 or 24-hour operation
- Buffered crystal frequency output in test mode for easy oscillator setting
- Data-changed flag allows simple testing for time rollover
- Independent interrupting time with open drain output
- Fully TTL compatible
- Low power standby operation (10μA at 2.2V)
- Low cost 16-pin DIP and 20-pin PCC

Block Diagram

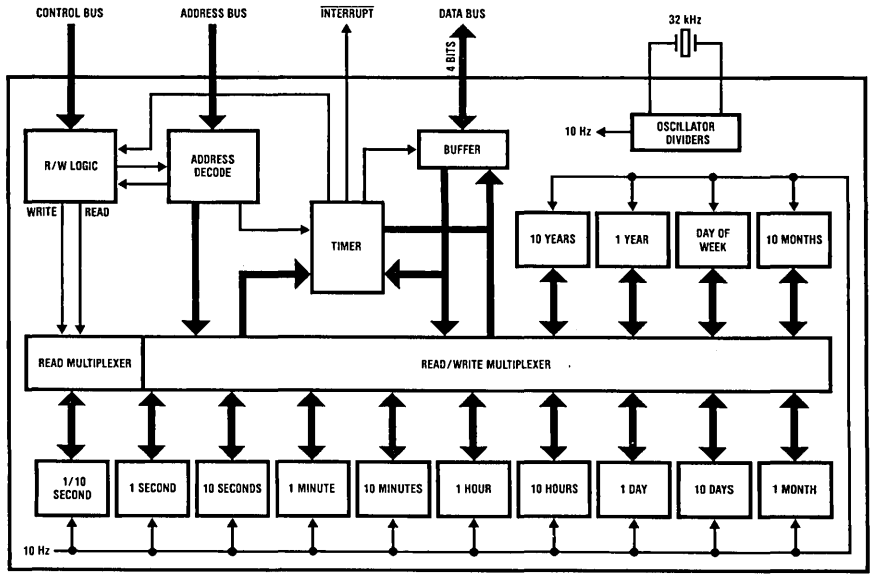

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FIGURE 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Input or Output Voltage	$-0.3V$ to $V_{DD} + 0.3V$
DC Input or Output Diode Current	± 5.0 mA
Storage Temperature, T_{STG}	$-65°C$ to $+150°C$
Supply Voltage, V_{DD}	6.5V
Power Dissipation, P_D	500 mW
Lead Temperature (Soldering, 10 seconds)	260°

Operating Conditions

	Min	Max	Units
Operating Supply Voltage	4.5	5.5	V
Standby Mode Supply Voltage	2.2	5.5	V
DC Input or Output Voltage	0	V_{DD}	V
Operating Temperature Range	-40	85	°C

Electrical Characteristics $V_{DD} = 5V \pm 10\%$, $T = -40°C$ to $+85°C$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage (except XTAL IN)		2.0			V
V_{IL}	Low Level Input Voltage (except XTAL IN)				0.8	V
V_{OH}	High Level Output Voltage (DB0–DB3)	$I_{OH} = -20\ \mu A$ $I_{OH} = -1.6$ mA	$V_{DD} - 0.1$ 3.7			V V
V_{OH}	High Level Output Voltage (INT)	$I_{OH} = -20\ \mu A$ (In Test Mode)	$V_{DD} - 0.1$			V
V_{OL}	Low Level Input Voltage (DB0–DB3, $\overline{INT}$)	$I_{OL} = 20\ \mu A$ $i_{OL} = 1.6$ mA			0.1 0.4	V V
I_{IL}	Low Level Input Current (AD0–AD3, DB0–DB3)	$V_{IN} = V_{SS}$ (Note 2)	-5		-80	μA
I_{IL}	Low Level Input Current ($\overline{WR}$, $\overline{RD}$)	$V_{IN} = V_{SS}$ (Note 2)	-5		-190	μA
I_{IL}	Low Level Input Current ($\overline{CS}$)	$V_{IN} = V_{SS}$ (Note 2)	-5		-550	μA
I_{OZH}	Ouput High Level Leakage Current ($\overline{INT}$)	$V_{OUT} = V_{DD}$			2.0	μA
I_{DD}	Average Supply Current	All $V_{IN} = V_{CC}$ or Open Circuit $V_{DD} = 2.2V$ (Standby Mode) $V_{DD} = 5.0V$ (Active Mode)		4	10 1	μA mA
C_{IN}	Input Capacitance			5	10	pF
C_{OUT}	Output Capacitance	(Outputs Disabled)		10		pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. All voltages referenced to ground unless otherwise noted.

Note 2: The DB0–DB3 and AD0–AD3 lines all have active P-channel pull-up transistors which will source current. The $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ lines have internal pull-up resistors to V_{DD}.

AC Switching Characteristics

READ TIMING: DATA FROM PERIPHERAL TO MICROPROCESSOR $V_{DD} = 5V \pm 0.5V$, $C_L = 100\ pF$

Symbol	Parameter	Commercial Specification $T_A = -40°C$ to $+85°C$			Units
		Min	Typ	Max	
t_{AD}	Address Bus Valid to Data Valid		390	650	ns
t_{CSD}	Chip Select On to Data Valid		140	300	ns
t_{RD}	Read Strobe On to Data Valid		140	300	ns
t_{RW}	Read Strobe Width (Note 3, Note 7)			DC	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	0			ns
t_{CSH}	Chip Select Hold Time from Trailing Edge of Read Strobe	0			ns
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	70	160		ns
t_{HZ}	Time from Trailing Edge of Read Strobe Until O/P Drivers are TRI-STATE®			250	ns

WRITE TIMING: DATA FROM MICROPROCESSOR TO PERIPHERAL $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Commercial Specification $T_A = -40°C$ to $+85°C$			Units
		Min	Typ	Max	
t_{AW}	Address Bus Valid to Write Strobe ↓ (Note 4, Note 6)	400	125		ns
t_{CSW}	Chip Select On to Write Strobe ↓	250	100		ns
t_{DW}	Data Bus Valid to Write Strobe ↓	400	220		ns
t_{WW}	Write Strobe Width (Note 6)	250	95		ns
t_{WCS}	Chip Select Hold Time Following Write Strobe ↓	0			ns
t_{WA}	Address Bus Hold Time Following Write Strobe ↓	0			ns
t_{WD}	Data Bus Hold Time Following Write Strobe ↓	100	35		ns
t_{AWS}	Address Bus Valid Before Start of Write Strobe	70	20		ns

Note 3: Except for special case restriction: with interrupts programmed, max read strobe width of control register (ADDR 0) is 30 ms. See section on Interrupt Programming.

Note 4: All timings measured to the trailing edge of write strobe (data latched by the trailing edge of $\overline{WR}$).

Note 5: Input test waveform peak voltages are 2.4V and 0.4V. Output signals are measured to their 2.4V and 0.4V levels.

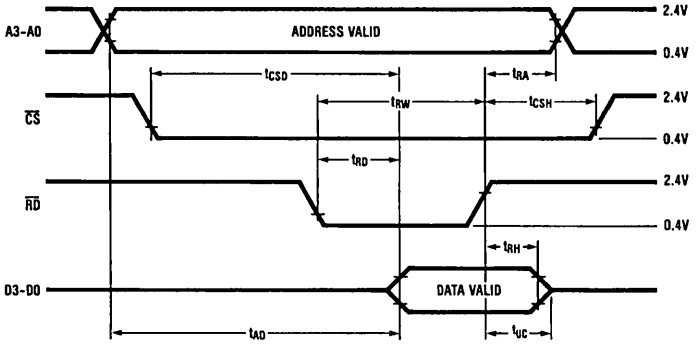
Note 6: Write strobe as used in the Write Timing Table is defined as the period when both chip select and write inputs are low, ie., $\overline{WS}$, = $\overline{CS}$ + $\overline{WR}$. Hence write strobe commences when both signals are low, and terminates when the first signal returns high.

Note 7: Read strobe as used in the Read Timing Table is defined as the period when both chip select and read inputs are low, ie., $\overline{RS}$ = $\overline{CS}$ + $\overline{RD}$.

Note 8: Typical numbers are at $V_{CC} = 5.0V$ and $T_A = 25°C$.

Switching Time Waveforms

Read Cycle Timing (Note 5)



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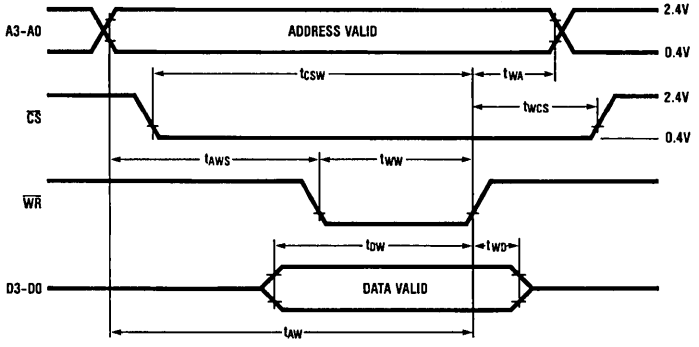
Write Cycle Timing (Note 5)



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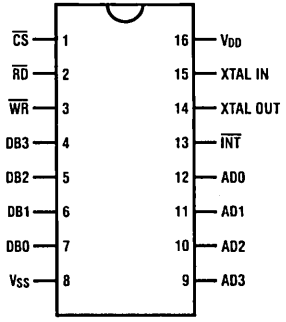
Connection Diagrams

Dual-In-Line Package



Top View

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PCC Package

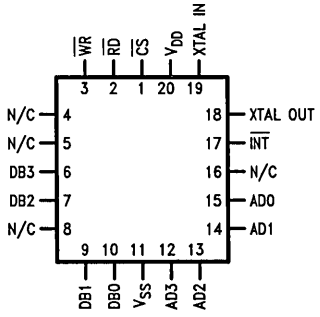

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FIGURE 2

Order Number MM58274CJ, MM58274CN or MM58274CV
See NS Package J16A, N16A, or V20A

Functional Description

The MM58274C is a bus oriented microprocessor real time clock. It has the same pin-out as the MM58174A while offering extended timekeeping up to units and tens of years. To enhance the device further, a number of other features have been added including: 12 or 24 hours counting, a testable data-changed flag giving easy error-free time reading and simplified interrupt control.

A buffered oscillator signal appears on the interrupt output when the device is in test mode. This allows for easy oscillator setting when the device is initially powered up in a system.

The counters are arranged as 4-bit words and can be randomly accessed for time reading and setting. The counters output in BCD (binary coded decimal) 4-bit numbers. Any register which has less than 4 bits (e.g., days of week uses only 3 bits) will return to a logic 0 on any unused bits. When written to, the unused inputs will be ignored.

Writing a logic 1 to the clock start/stop control bit resets the internal oscillator divider chain and the tenths of seconds counter. Writing a logic 0 will start the clock timing from the nearest second. The time then updates every 100 ms with all counters changing synchronously. Time changing during a read is detected by testing the data-changed bit of the control register after completing a string of clock register reads.

Interrupt delay times of 0.1s, 0.5s, 1s, 5s, 10s, 30s or 60s can be selected with single or repeated interrupt outputs. The open drain output is pulled low whenever the interrupt timer times out and is cleared by reading the control register.

CIRCUIT DESCRIPTION

The block diagram in *Figure 1* shows the internal structure of the chip. The 16-pin package outline is shown in *Figure 2*.

Crystal Oscillator

This consists of a CMOS inverter/amplifier with an on-chip bias resistor. Externally a 20 pF capacitor, a 6 pF–36 pF trimmer capacitor and a crystal are required to complete the 32.768 kHz timekeeping oscillator circuit.

The 6 pF–36 pF trimmer fine tunes the crystal load impedance, optimizing the oscillator stability. When properly adjusted (i.e., to the crystal frequency of 32.768 kHz), the circuit will display a frequency variation with voltage of less than 3 ppm/V. When an external oscillator is used, connect to oscillator input and float (no connection) the oscillator output.

When the chip is enabled into test mode, the oscillator is gated onto the interrupt output pin giving a buffered oscillator output that can be used to set the crystal frequency when the device is installed in a system. For further information see the section on Test Mode.

Divider Chain

The crystal oscillator is divided down in three stages to produce a 10 Hz frequency setting pulse. The first stage is a non-integer divider which reduces the 32.768 kHz input to 30.720 kHz. This is further divided by a 9-stage binary ripple counter giving an output frequency of 60 Hz. A 3-stage Johnson counter divides this by six, generating a 10 Hz output. The 10 Hz clock is gated with the 32.768 kHz crystal frequency to provide clock setting pulses of 15.26 μs duration. The setting pulse drives all the time registers on the

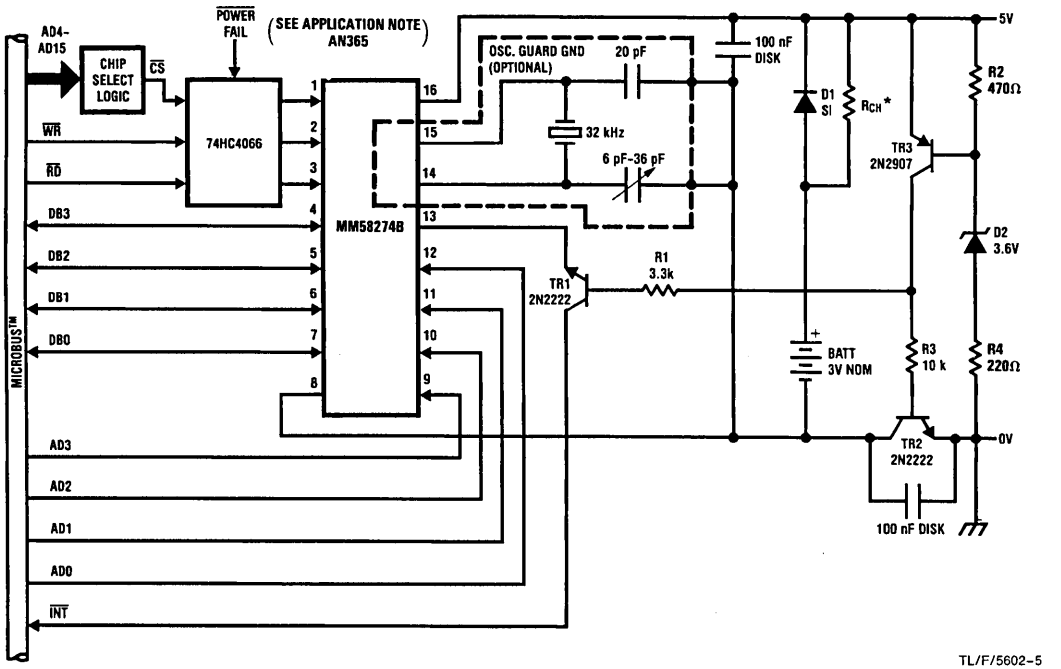

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FIGURE 3. Typical System Connection Diagram

Functional Description (Continued)

device which are synchronously clocked by this signal. All time data and data-changed flag change on the falling edge of the clock setting pulse.

Data-Changed Flag

The data-changed flag is set by the clock setting pulse to indicate that the time data has been altered since the clock was last read. This flag occupies bit 3 of the control register where it can be tested by the processor to sense data-changed. It will be reset by a read of the control register. See the section, "Methods of Device Operation", for suggested clock reading techniques using this flag.

Seconds Counters

There are three counters for seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds.

The registers are accessed at the addresses shown in Table I. The tenths of seconds register is reset to 0 when the clock start/stop bit (bit 2 of the control register) is set to logic 1. The units and tens of seconds are set up by the processor, giving time setting to the nearest second. All three registers can be read by the processor for time output.

Minutes Counters

There are two minutes counters:

a) units of minutes

b) tens of minutes.

Both registers may be read to or written from as required.

Hours Counters

There are two hours counters:

a) units of hours

b) tens of hours.

Both counters may be accessed for read or write operations as desired.

In 12-hour mode, the tens of hours register has only one active bit and the top three bits are set to logic 0. Data bit 1 of the clock setting register is the AM/PM indicator; logic 0 indicating AM, logic 1 for PM.

When 24-hour mode is programmed, the tens of hours register reads out two bits of data and the two most significant bits are set to logic 0. There is no AM/PM indication and bit 1 of the clock setting register will read out a logic 0.

In both 12/24-hour modes, the units of hours will read out four active data bits. 12 or 24-hour mode is selected by bit 0 of the clock setting register, logic 0 for 12-hour mode, logic 1 for the 24-hour mode.

Days Counters

There are two days counters:

a) units of days

b) tens of days.

The days counters will count up to 28, 29, 30 or 31 depending on the state of the months counters and the leap year counter. The microprocessor has full read/write access to these registers.

Months Counters

There are two months counters:

a) units of months

b) tens of months.

Both these counters have full read/write access.

Years Counters

There are two years counters:

a) units of years

b) tens of years.

Both these counters have full read/write access. The years will count up to 99 and roll over to 00.

TABLE I. Address Decoding of Real-Time Clock Internal Registers

Register Selected	Address (Binary)				(Hex)	Access
	AD3	AD2	AD1	AD0		
0 Control Register	0	0	0	0	0	Split Read and Write
1 Tenths of Seconds	0	0	0	1	1	Read Only
2 Units Seconds	0	0	1	0	2	R/W
3 Tens Seconds	0	0	1	1	3	R/W
4 Units Minutes	0	1	0	0	4	R/W
5 Tens Minutes	0	1	0	1	5	R/W
6 Unit Hours	0	1	1	0	6	R/W
7 Tens Hours	0	1	1	1	7	R/W
8 Units Days	1	0	0	0	8	R/W
9 Tens Days	1	0	0	1	9	R/W
10 Units Months	1	0	1	0	A	R/W
11 Tens Months	1	0	1	1	B	R/W
12 Units Years	1	1	0	0	C	R/W
13 Tens Years	1	1	0	1	D	R/W
14 Day of Week	1	1	1	0	E	R/W
15 Clock Setting/ Interrupt Registers	1	1	1	1	F	R/W

Functional Description (Continued)

Day of Week Counter

The day of week counter increments as the time rolls from 23:59 to 00:00 (11:59 PM to 12:00 AM in 12-hour mode). It counts from 1 to 7 and rolls back to 1. Any day of the week may be specified as day 1.

Clock Setting Register/Interrupt Register

The interrupt select bit in the control register determines which of these two registers is accessible to the processor at address 15. Normal clock and interrupt timing operations will always continue regardless of which register is selected onto the bus. The layout of these registers is shown in Table II.

The clock setting register is comprised of three separate functions:

a) leap year counter: bits 2 and 3

b) AM/PM indicator: bit 1

c) 12/24-hour mode set: bit 0 (see Table IIA).

The leap year counter is a 2-stage binary counter which is clocked by the months counter. It changes state as the time rolls over from 11:59 on December 31 to 00:00 on January 1.

The counter should be loaded with the 'number of years since last leap year' e.g., if 1980 was the last leap year, a clock programmed in 1983 should have 3 stored in the leap year counter. If the clock is programmed during a leap year, then the leap year counter should be set to 0. The contents of the leap year counter can be read by the μP.

The AM/PM indicator returns a logic 0 for AM and a logic 1 for PM. It is clocked when the hours counter rolls from 11:59 to 12:00 in 12-hour mode. In 24-hour mode this bit is set to logic 0.

The 12/24-hour mode set determines whether the hours counter counts from 1 to 12 or from 0 to 23. It also controls the AM/PM indicator, enabling it for 12-hour mode and forcing it to logic 0 for the 24-hour mode. The 12/24-hour mode bit is set to logic 0 for 12-hour mode and it is set to logic 1 for 24-hour mode.

IMPORTANT NOTE: *Hours mode and AM/PM bits cannot be set in the same write operation. See the section on* Initialization (Methods of Device Operation) *for a suggested setting routine.*

All bits in the clock setting register may be read by the processor.

The interrupt register controls the operation of the timer for interrupt output. The processor programs this register for single or repeated interrupts at the selected time intervals.

The lower three bits of this register set the time delay period that will occur between interrupts. The time delays that can be programmed and the data words that select these are outlined in Table IIB.

Data bit 3 of the interrupt register sets for either single or repeated interrupts; logic 0 gives single mode, logic 1 sets for repeated mode.

Using the interrupt is described in the Device Operation section.

TABLE IIA. Clock Setting Register Layout

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 Indicates a Leap Year	R/W
AM/PM Indicator (12-Hour Mode)			X		0 = AM 1 = PM 0 in 24-Hour Mode	R/W
12/24-Hour Select Bit				X	0 = 12-Hour Mode 1 = 24-Hour Mode	R/W

TABLE IIB. Interrupt Control Register

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt output cleared, start/stop bit set to 1.	X	0	0	0
0.1 Second	DB3 = 0 for single interrupt DB3 = 1 for repeated interrupt	0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second		0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1

Timing Accuracy: single interrupt mode (all time delays): ±1 ms
Repeated Mode: ±1 ms on initial timeout, thereafter synchronous with first interrupt (i.e., timing errors do not accumulate).

Functional Description (Continued)

Control Register

There are three registers which control different operations of the clock:

a) the clock setting register

b) the interrupt register

c) the control register.

The clock setting and interrupt registers both reside at address 15, access to one or the other being controlled by the interrupt select bit; data bit 1 of the control register.

The clock setting register programs the timekeeping of the clock. The 12/24-hour mode select and the AM/PM indicator for 12-hour mode occupy bits 0 and 1, respectively. Data bits 2 and 3 set the leap year counter.

The interrupt register controls the operation of the interrupt timer, selecting the required delay period and either single or repeated interrupt.

The control register is responsible for controlling the operations of the clock and supplying status information to the processor. It appears as two different registers; one with write only access and one with read only access.

The write only register consists of a bank of four latches which control the internal processes of the clock.

The read only register contains two output data latches which will supply status information for the processor. Table III shows the mapping of the various control latches and status flags in the control register. The control register is located at address 0.

The write only portion of the control register contains four latches:

A logic 1 written into the test bit puts the device into test mode. This allows setting of the oscillator frequency as well as rapid testing of the device registers, if required. A more complete description is given in the Test Mode section. For normal operation the test bit is loaded with logic 0.

The clock start/stop bit stops the timekeeping of the clock and resets to 0 the tenths of seconds counter. The time of day may then be written into the various clock registers and the clock restarted synchronously with an external time source. Timekeeping is maintained thereafter.

A logic 1 written to the start/stop bit halts clock timing. Timing is restarted when the start/stop bit is written with a logic 0.

The interrupt select bit determines which of the two registers mapped onto address 15 will be accessed when this address is selected.

A logic 0 in the interrupt select bit makes the clock setting register available to the processor. A logic 1 selects the interrupt register.

The interrupt start/stop bit controls the running of the interrupt timer. It is programmed in the same way as the clock start/stop bit; logic 1 to halt the interrupt and reset the timer, logic 0 to start interrupt timing.

When no interrupt is programmed (interrupt control register set to 0), the interrupt start/stop bit is automatically set to a logic 1. When any new interrupt is subsequently programmed, timing will not commence until the start/stop bit is loaded with 0.

In the single interrupt mode, interrupt timing stops when a timeout occurs. The processor restarts timing by writing logic 0 into the start/stop bit.

In repeated interrupt mode the interrupt timer continues to count with no intervention by the processor necessary.

Interrupt timing may be stopped in either mode by writing a logic 1 into the interrupt start/stop bit. The timer is reset and can be restarted in the normal way, giving a full time delay period before the next interrupt.

In general, the control register is set up such that writing 0's into it will start anything that is stopped, pull the clock out of test mode and select the clock setting register onto the bus. In other words, writing 0 will maintain normal clock operation and restart interrupt timing, etc.

The read only portion of the control register has two status outputs:

Since the MM58274C keeps real time, the time data changes asynchronously with the processor and this may occur while the processor is reading time data out of the clock.

Some method of warning the processor when the time data has changed must thus be included. This is provided for by the data-changed flag located in bit 3 of the control register. This flag is set by the clock setting pulse which also clocks the time registers. Testing this bit can tell the processor whether or not the time has changed. The flag is cleared by a read of the control register but not by any write operations. No other register read has any effect on the state of the data-changed flag.

Data bit 0 is the interrupt flag. This flag is set whenever the interrupt timer times out, pulling the interrupt output low. In a polled interrupt routine the processor can test this flag to determine if the MM58274C was the interrupting device. This interrupt flag and the interrupt output are both cleared by a read of the control register.

TABLE III. The Control Register Layout

Access (addr0)	DB3	DB2	DB1	DB0
Read From:	Data-Changed Flag	0	0	Interrupt Flag
Write To:	Test 0 = Normal 1 = Test Mode	Clock Start/Stop 0 = Clock Run 1 = Clock Stop	Interrupt Select 0 = Clock Setting Register 1 = Interrupt Register	Interrupt Start/Stop 0 = Interrupt Run 1 = Interrupt Stop

Functional Description (Continued)

Both of the flags and the interrupt output are reset by the trailing edge of the read strobe. The flag information is held latched during a control register read, guaranteeing that stable status information will always be read out by the processor.

Interrupt timeout is detected and stored internally if it occurs during a read of the control register, the interrupt output will then go low only after the read has been completed.

A clock setting pulse occurring during a control register read will *not* affect the data-changed flag since time data read out before or after the control read will not be affected by the time change.

METHODS OF DEVICE OPERATION

Test Mode

National Semiconductor uses test mode for functionally testing the MM58274C after fabrication and again after packaging. Test mode can also be used to set up the oscillator frequency when the part is first commissioned.

Figure 4 shows the internal clock connections when the device is written into test mode. The 32.768 kHz oscillator is gated onto the interrupt output to provide a buffered output for initial frequency setting. This signal is driven from a TRI-STATE output buffer, enabling easy oscillator setting in systems where interrupt is not normally used and there is no external resistor on the pin.

If an interrupt is programmed, the 32.768 kHz output is switched off to allow high speed testing of the interrupt timer. The interrupt output will then function as normal.

The clock start/stop bit can be used to control the fast clocking of the time registers as shown in *Figure 4*.

Initialization

When it is first installed and power is applied, the device will need to be properly initialized. The following operation steps are recommended when the device is set up (all numbers are decimal):

1) Disable interrupt on the processor to allow oscillator setting. Write 15 into the control register: *The clock and interrupt start/stop bits are set to 1, ensuring that the clock and interrupt timers are both halted. Test mode and the interrupt register are selected.*

2) Write 0 to the interrupt register: *Ensure that there are no interrupts programmed and that the oscillator will be gated onto the interrupt output.*

3) Set oscillator frequency: *All timing has been halted and the oscillator is buffered out onto the interrupt line.*

4) Write 5 to the control register: *The clock is now out of test mode but is still halted. The clock setting register is now selected by the interrupt select bit.*

5) Write 0001 to all registers. This ensures starting with a valid BCD value in each register.

6) Set 12/24 Hours Mode: *Write to the clock setting register to select the hours counting mode required.*

7) Load Real-Time Registers: *All time registers (including Leap Years and AM/PM bit) may now be loaded in any order. Note that when writing to the clock setting register to set up Leap Years and AM/PM, the Hours Mode bit must not be altered from the value programmed in step 5.*

8) Write 0 to the control register: *This operation finishes the clock initialization by starting the time. The final control register write should be synchronized with an external time source.*

In general, timekeeping should be halted before the time data is altered in the clock. The data can, however, be altered at any time if so desired. Such may be the case if the user wishes to keep the clock corrected without having to stop and restart it; i.e., winter/summer time changing can be accomplished without halting the clock. This can be done in software by sensing the state of the data-changed flag and only altering time data just after the time has rolled over (data-changed flag set).

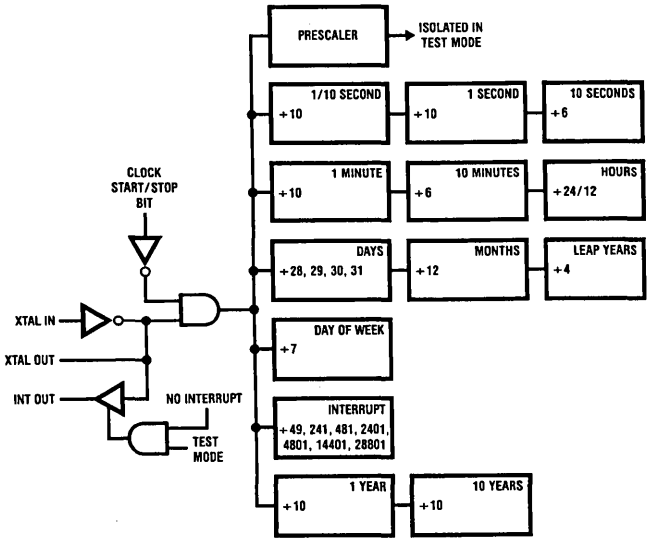

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FIGURE 4. Test Mode Organization

Functional Description (Continued)

Reading the Time Registers

Using the data-changed flag technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1) Read the control register, address 0: *This is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.*

2) Read time registers: *All desired time registers are read out in a block.*

3) Read the control register and test DCF: *If DCF is cleared (logic 0), then no clock setting pulses have after occurred since step 1. All time data is guaranteed good and time reading is complete.*

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may not be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

Interrupt Programming

The interrupt timer generates interrupts at time intervals which are programmed into the interrupt register. A single interrupt after delay or repeated interrupts may be programmed. Table IIB lists the different time delays and the data words that select them in the interrupt register.

Once the interrupt register has been used to set up the delay time and to select for single or repeat, it takes no further part in the workings of the interrupt system. All activity by the processor then takes place in the control register.

Initializing:

1) Write 3 to the control register (AD0): *Clock timing continues, interrupt register selected and interrupt timing stopped.*

2) Write interrupt control word to address 15: *The interrupt register is loaded with the correct word (chosen from Table IIB) for the time delay required and for single or repeated interrupts.*

3) Write 0 or 2 to the control register: *Interrupt timing commences. Writing 0 selects the clock setting register onto the data bus; writing 2 leaves the interrupt register selected. Normal timekeeping remains unaffected.*

On Interrupt:

Read the control register and test for Interrupt Flag (bit 0).

If the flag is cleared (logic 0), then the device is not the source of the interrupt.

If the flag is set (logic 1), then the clock did generate an interrupt. The flag is reset and the interrupt output is cleared by the control register read that was used to test for interrupt.

Single Interrupt Mode:

When appropriate, write 0 or 2 to the control register to restart the interrupt timer.

Repeated Interrupt Mode:

Timing continues, synchronized with the control register write which originally started interrupt timing. No further intervention is necessary from the processor to maintain timing.

In either mode interrupt timing can be stopped by writing 1 into the control register (interrupt start/stop set to 1). Timing for the full delay period recommences when the interrupt start/stop bit is again loaded with 0 as normal.

IMPORTANT NOTE: Using the interrupt timer places a constraint on the maximum Read Strobe width which may be applied to the clock. Normally all registers may be read from with a t_{RW} down to DC (i.e., $\overline{CS}$ and $\overline{RD}$ held continuously low). When the interrupt timer is active however, the maximum read strobe width that can be applied to the control register (Addr 0) is 30 ms.

This restriction is to allow the interrupt timer to properly reset when it times out. Note that it only affects reading of the control register—all other addresses in the clock may be accessed with DC read strobes, regardless of the state of the interrupt timer. Writes to any address are unaffected.

NOTES ON AC TIMING REQUIREMENTS

Although the Switching Time Waveforms show Microbus control signals used for clock access, this does not preclude the use of the MM58274C in other non-Microbus systems. *Figure 5* is a simplified logic diagram showing how the control signals are gated internally to control access to the clock registers. From this diagram it is clear that $\overline{CS}$ could be used to generate the internal data transfer strobes, with $\overline{RD}$ and $\overline{WR}$ inputs set up first. This situation is illustrated in *Figure 6*.

The internal data busses of the MM58274C are fully CMOS, contributing to the flexibility of the control inputs. When determining the suitability of any given control signal pattern for the MM58274B the timing specifications in AC Switching Characteristics should be examined. As long as these timings are met (or exceeded) the MM58274C will function correctly.

When the MM58274C is connected to the system via a peripheral port, the freedom from timing constraints allows for very simple control signal generation, as in *Figure 7*. For reading (*Figure 7a*), Address, $\overline{CS}$ and $\overline{RD}$ may be activated simultaneously and the data will be available at the port after t_{AD}-max (650 ns). For writing (*Figure 7b*), the address and data may be applied simultaneously; 70 ns later $\overline{CS}$ and $\overline{WR}$ may be strobed together.

Functional Description (Continued)

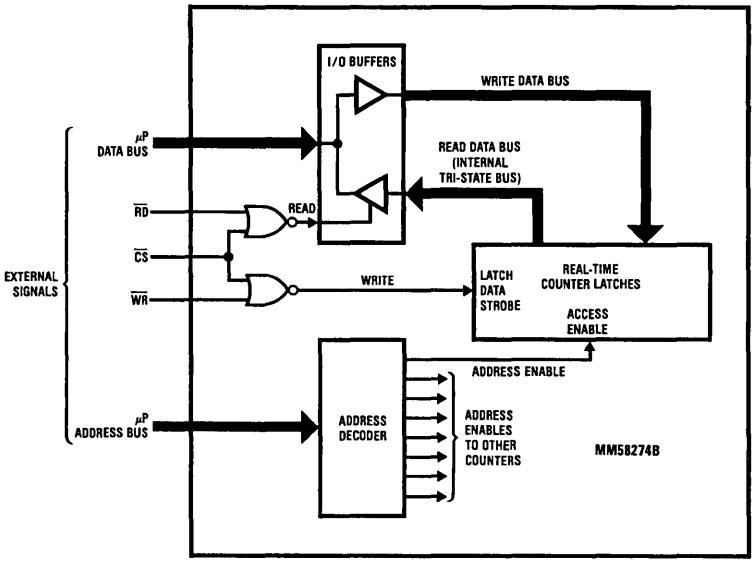

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FIGURE 5. MM58274C Microprocessor Interface Diagram

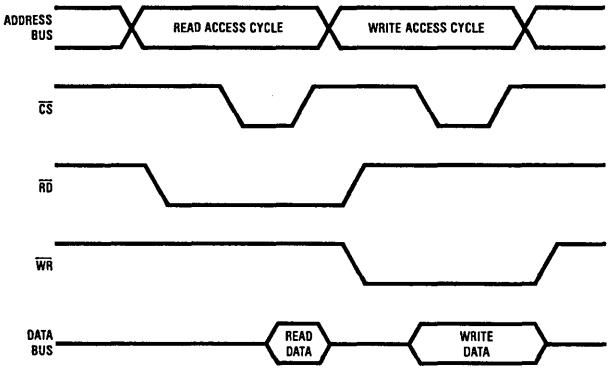

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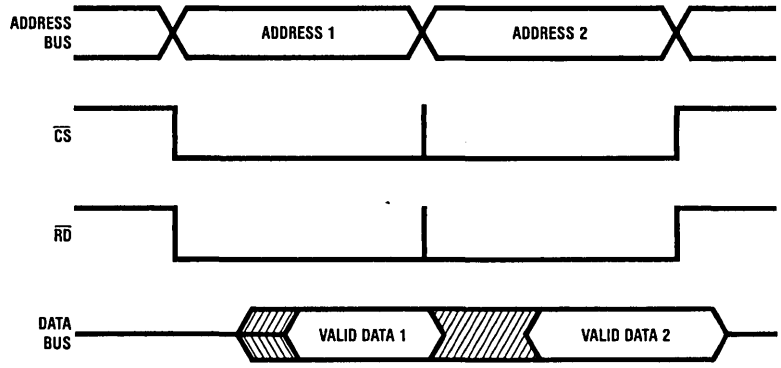
FIGURE 6. Valid MM58274C Control Signals Using Chip Select Generated Access Strobes

Functional Description (Continued)



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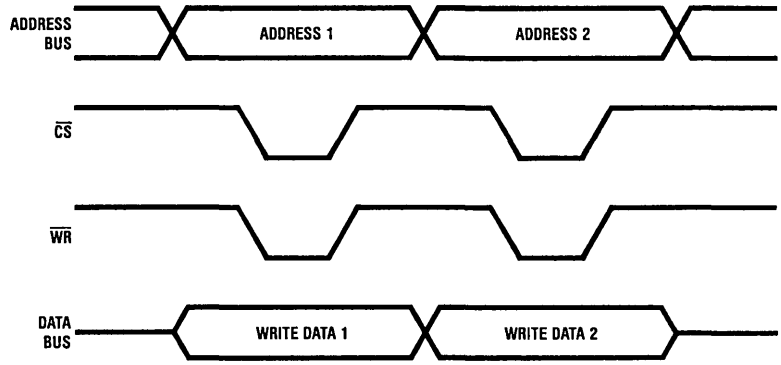
a. Port Generated Read Access—2 Addresses Read Out



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b. Port Generated Write Access—2 Addresses Written To

FIGURE 7. Simple Port Generated Control Signals

Functional Description (Continued)

APPLICATION HINTS

Time Reading Using Interrupt

In systems such as point of sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined in the section on methods of operation is ideal for this type of system. Some systems, however, need to sense a change in real time; e.g., industrial timers/process controllers, TV/VCR clocks, any system where real time is displayed.

The interrupt timer on the MM58274C can generate interrupts synchronously with the time registers changing, using software to provide the initial synchronization.

In single interrupt mode the processor is responsible for initiating each timing cycle and the timed period is accurate to ±1 ms.

In repeated interrupt mode the period from the initial processor start to the first timeout is also only accurate to ±1 ms. The following interrupts maintain accurate delay periods relative to the first timeout. Thus, to utilize interrupt to control time reading, we will use repeated interrupt mode.

In repeated mode the time period between interrupts is exact, which means that timeouts will always occur at the same point relative to the internal clock setting pulses. The case for 0.1s interrupts is shown in *Figure A-1*. The same is true for other delay periods, only there will be more clock setting pulses between each interrupt timeout. If we set up the interrupt timer so that interrupt always times out just after the clock setting pulse occurs (*Figure A-2*), then there is no need to test the data-changed flag as we know that the time data has just changed and will not alter again for another 100 ms.

This can be achieved as outlined below:

1) Follow steps 1 and 2 of the section on interrupt programming. In step 2 set up for repeated interrupt.

2) Read control register AD0: *This is a dummy read to reset the data-changed flag.*

3) Read control register AD0 until data-changed flag is set.

4) Write 0 or 2 to control register. Interrupt timing commences.

Time Reading with Very Slow Read Cycles

If a system takes longer than 100 ms to complete reading of all the necessary time registers (e.g., when CMOS processors are used) or where high level interpreted language routines are used, then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

The technique below will detect both time changing *between* read strobes (i.e., between reading tens of minutes and units of hours) and also time changing *during* read, which can produce invalid data.

1) Read and store the value of the *lowest* order time register required.

2) Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.

3) Read the lowest order register and compare it with the value stored previously in step 1. If it is still the same, then all time data is good. If it has changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads *must* both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no higher order register has changed either.

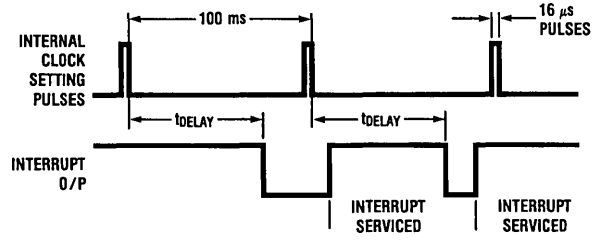

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FIGURE A-1. Time Delay from Clock Setting Pulses to Interrupt is Constant

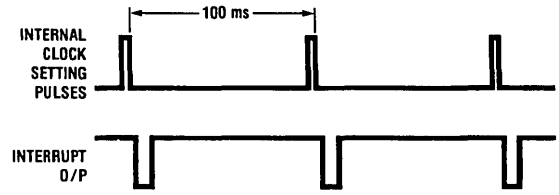

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FIGURE A-2. Interrupt Timer Synchronized with Clock Setting Pulses

National Semiconductor

MM58167A
Microprocessor Real Time Clock

General Description

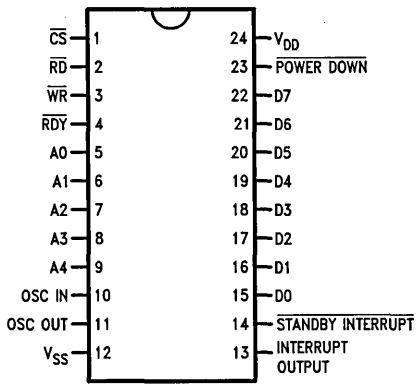
The MM58167A is a low threshold metal gate CMOS circuit that functions as a real time clock in bus oriented microprocessor systems. The device includes an addressable real time counter, 56 bits of RAM, and two interrupt outputs. A $\overline{\text{POWER DOWN}}$ input allows the chip to be disabled from the rest of the system for standby low power operation. The time base is a 32.768 Hz crystal oscillator.

Features

- Microprocessor compatible (8-bit data bus)
- Milliseconds through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- $\overline{\text{POWER DOWN}}$ input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32.768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock

Connection Diagrams

Dual-In-Line Package



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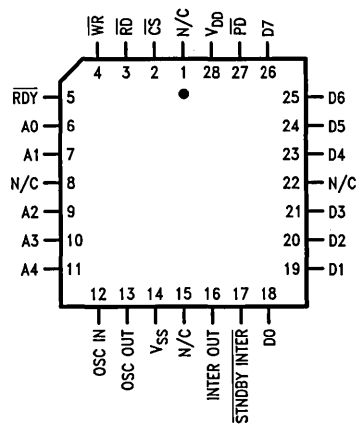
Top View

Order Number MM58167AN
See NS Package Number N24A

PCC Package



TL/F/6148–2

Top View

Order Number MM58167AV
See NS Package Number V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at All Pins	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
$V_{DD} - V_{SS}$	6.0V
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Electrical Characteristics $V_{SS} = 0V, 0°C \le T_A \le 70°C$

Parameter	Conditions	Min	Max	Units
Supply Voltage				
V_{DD}	Outputs Enabled	4.5	5.5	V
V_{DD}	$\overline{\text{POWER DOWN}}$ Mode	2.2	5.5	V
Supply Current				
I_{DD}, Dynamic	Outputs TRI-STATE® $f_{IN} = 32.768$ kHz, $V_{DD} = 5.5V$ $V_{IH} \ge V_{DD} - 0.3V$ $V_{IL} \le V_{SS} + 0.3V$		20	μA
I_{DD}, Dynamic	Outputs TRI-STATE $f_{IN} = 32.768$ kHz, $V_{DD} = 5.5V$ $V_{IH} = 2.0V$, $V_{IL} = 0.8V$		5	mA
Input Voltage				
Logical Low		0.0	0.8	V
Logical high		2.0	V_{DD}	V
Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	−1	1	μA
Output Impedance	I/O and INTERRUPT OUT			
Logical Low	$V_{DD} = 4.5V$, $I_{OL} = 1.6$ mA		0.4	V
Logical High	$V_{DD} = 4.5V$, $I_{OH} = -400$ μA	2.4		V
	$I_{OH} = -10$ μA	0.8 V_{DD}		V
TRI-STATE	$V_{SS} \le V_{OUT} \le V_{DD}$	−1	1	μA
Output Impedance	$\overline{\text{RDY}}$ and $\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$ (Open Drain Devices)			
Logical Low, Sink	$V_{DD} = 4.5V$, $I_{OL} = 1.6$ mA		0.4	V
Logical High, Leakage	$V_{OUT} \le V_{DD}$		10	μA

Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table I. Any unused bits are held at a logical zero during a read and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example tens of hours cannot legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table I as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60 μs above 4.5V and 300 μs at 2.2V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones, then this RAM location will always compare. The rule of thumb for an "alarm" interrupt is: All nibbles of higher order than specified are set to C hex (always compare). All nibbles lower than specified are set to "zero". As an example, if an alarm is to occur everyday at 10:15 a.m., configure the bits in RAM as shown in Table II.

The RAM is formatted the same as the real time counter, 4 bits per digit, 14 digits, however there are no unused bits.

The unused bits in the real time counter will compare only to zeros in the RAM.

An address map is shown in Table III.

Interrupts and Comparator

There are two interrupt outputs. The first is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, once per second, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (*Figure 1*). Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to its reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupting frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the $\overline{\text{STANDBY INTERRUPT}}$ (open drain output, active low). This interrupt occurs when enabled and when a RAM/real time counter comparison occurs. The $\overline{\text{STANDBY INTERRUPT}}$ is enabled by writing a one on the D0 line at address 16_H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the $\overline{\text{STANDBY INTERRUPT}}$ is enabled, the interrupt will turn on immediately.

TABLE I. Real Time Counter Format

Counter Addressed		Units				Max BCD Code	Tens				Max BCD Code
		D0	D1	D2	D3		D4	D5	D6	D7	
Milliseconds	(00_H)	—	—	—	—	0	D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	—	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	—	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	—	—	2
Day of the Week	(05_H)	D0	D1	D2	—	7	—	—	—	—	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	—	—	3
Month	(07_H)	D0	D1	D2	D3	9	D4	—	—	—	1

(—) indicates unused bits

Functional Description (Continued)

TABLE II. Clock RAM Bit Map for Alarm Interrupt Everyday at 10:15 a.m.

Function	Address					Data							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	0	1	0	1	0	1
Hours	0	1	1	0	0	0	0	0	1	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	1	1	X	X	1	1	X	X
Months	0	1	1	1	1	1	1	X	X	1	1	X	X

TABLE III. Address Codes and Function

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter—Milliseconds
0	0	0	0	1	Counter—Hundredths and Tenths of Seconds
0	0	0	1	0	Counter—Seconds
0	0	0	1	1	Counter—Minutes
0	0	1	0	0	Counter—Hours
0	0	1	0	1	Counter—Day of Week
0	0	1	1	0	Counter—Day of Month
0	0	1	1	1	Counter—Month
0	1	0	0	0	RAM—Milliseconds
0	1	0	0	1	RAM—Hundredths and Tenths of Seconds
0	1	0	1	0	RAM—Seconds
0	1	0	1	1	RAM—Minutes
0	1	1	0	0	RAM—Hours
0	1	1	0	1	RAM—Day of Week
0	1	1	1	0	RAM—Day of Month
0	1	1	1	1	RAM—Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counters Reset
1	0	0	1	1	RAM Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	GO Comand
1	0	1	1	0	$\overline{\text{STANDBY INTERRUPT}}$
1	1	1	1	1	Test Mode

All others unused

The comparator is a cascaded exclusive NOR. Its output is latched 61 μs after the rising edge of the 1 kHz clock signal (input to the milliseconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.5V, the thousandths of seconds counter should not be included in a compare because of the possibility of having a ripple delay greater than 61 μs. (For output timing see Interrupt Timing.)

Power Down Mode

The $\overline{\text{POWER DOWN}}$ input is essentially a second chip select. It disables all inputs and outputs except for the $\overline{\text{STANDBY INTERRUPT}}$. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain timekeeping and turn on the $\overline{\text{STANDBY INTERRUPT}}$ if programmed to do so. (The programming must be done before the $\overline{\text{POWER DOWN}}$ input goes to a

Functional Description (Continued)

logical zero.) When switching V_{DD} to the standby or power down mode, the $\overline{\text{POWER DOWN}}$ input should go to a logical zero at least 1 μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between V_{SS} − 0.3V and V_{DD} + 0.3V. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the $\overline{\text{POWER DOWN}}$ input back to a logical one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing all 1's (FF) at address 12_H or 13_H respectively.

A write pulse at address 15_H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This GO command is used for precise starting of the clock. The data on the data bus is ignored during the write. If the seconds counter is at a value greater than 39 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute.

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The status bit is set if this 1 kHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14_H is read. All the other data lines will zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14_H will reset the status bit.

Using the Rollover Status Bit

If a single read of any clock counter is made, it should be followed by reading the rollover status bit.

Example: Read months, then read rollover status.

If a sequential read of the clock counters is made, then the rollover status bit should be read after the last counter is read.

Example: Read hours, minutes, seconds, then read the rollover status.

Oscillator

The oscillator used in the standard Pierce parallel resonant oscillator. Externally, 2 capacitors, a 20 MΩ resistor and the crystal are required. The 20 MΩ resistor is connected between OSC IN and OSC OUT to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200 kΩ. The capacitor values should be typically 20 pF–25 pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the oscillator output should be left floating and the oscillator input levels should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to reduce interference of the oscillator by the A4 address.

Control Lines

The $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, AND $\overline{\text{CHIP SELECT}}$ signals are active low inputs. The $\overline{\text{READY}}$ signal is an open drain output. At the start of each read or write cycle the $\overline{\text{READY}}$ line (open drain) will pull low and will remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a write. $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ must be accompanied by a $\overline{\text{CHIP SELECT}}$ (see *Figures 3* and *4* for read and write cycle timing).

During a read or write, address bits must not change while chip select and control strobes are low.

Test Mode

The test mode is for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32.768 kHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at $1F_H$.

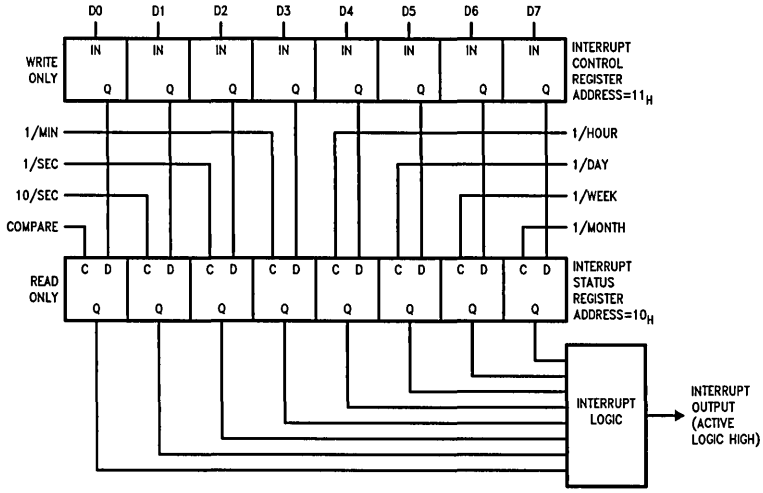


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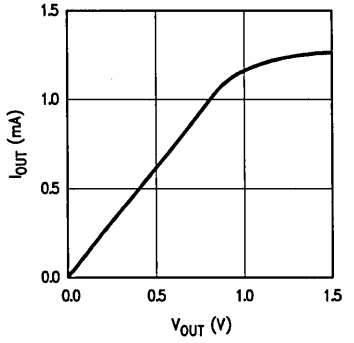
FIGURE 1. Interrupt Register Format

Functional Description (Continued)

Standby Interrupt Typical Characteristics



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Typical Supply Current vs Supply Voltage during Power Down

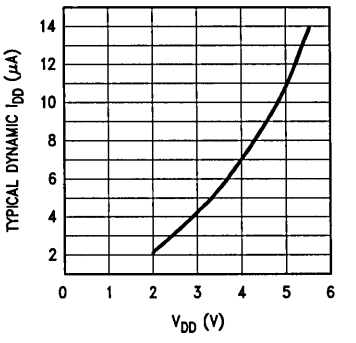

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FIGURE 2

Interrupt Timing $0°C \le T_A \le 70°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Symbol	Parameter	Min	Max	Units
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	μs
t_{SBYON}	Compare Valid to $\overline{\text{STANDBY INTERRUPT}}$ (Pin 14) Low (Note 1)		5	μs
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	μs
t_{SBYOFF}	Trailing Edge of Write Cycle (D0 = 0; Address = 16_H) to $\overline{\text{STANDBY INTERRUPT}}$ Off (High Impedance State)		5	μs

Note 1: The status register clocks are: the corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61 μs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing $0°C \le T_A \le 70°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Symbol	Parameter	Min	Max	Units
t_{AR}	Address Bus Valid to Read Strobe (Note 3)	100		ns
t_{CSR}	Chip Select to Read Strobe (Note 2)	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns
t_{RYDV}	Rising Edge of Ready to Data Valid		100	ns

Note 2: When reading, a deselect time of 500 ns minimum must occur between counter reads. Deselect is: $\overline{CS} = 1$ or $(\overline{WR}) \bullet (\overline{RD}) = 1$.

Note 3: If $t_{AR} = 0$ and Chip Select, Address Valid or Read are coincident then they must exist for 1050 ns.

Write Cycle Timing $0°C \le T_A \le 70°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Symbol	Parameter	Min	Max	Units
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready Strobe Width		800	ns
t_{RYH}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	110		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Note 4: If data changes while $\overline{CS}$ and $\overline{WR}$ are low, then they must remain coincident for 1050 ns after the data change to ensure a valid write. Data bus loading is 100 pF. Ready output loading is 50 pF and 3 kΩ pull-up.

Input and output AC timing levels:
Logical one = 2.0V
Logical zero = 0.8V

Read and Write Cycle Timing Diagrams

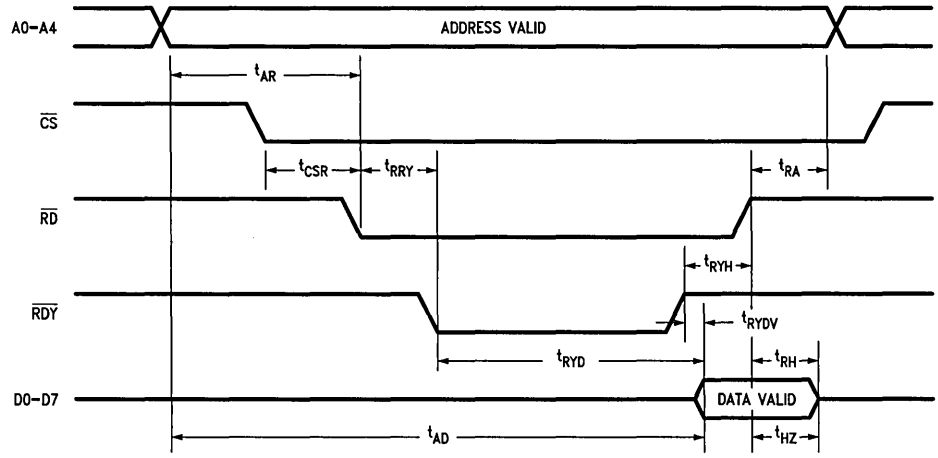

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FIGURE 3. Read Cycle Timing

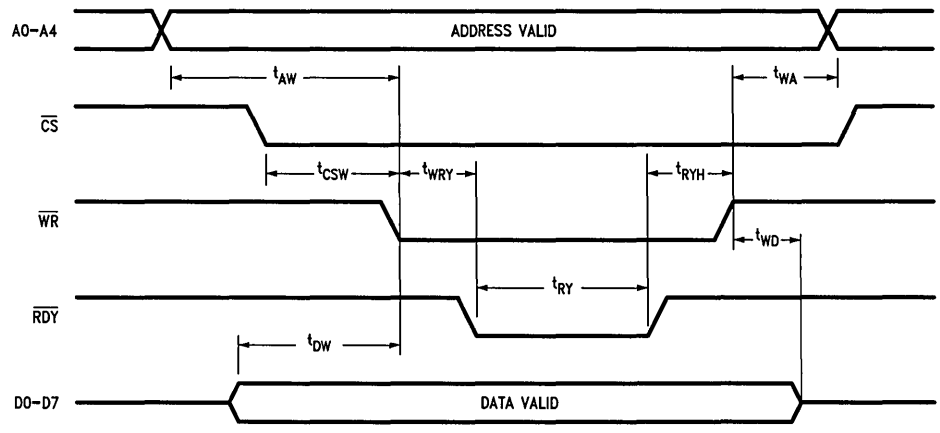

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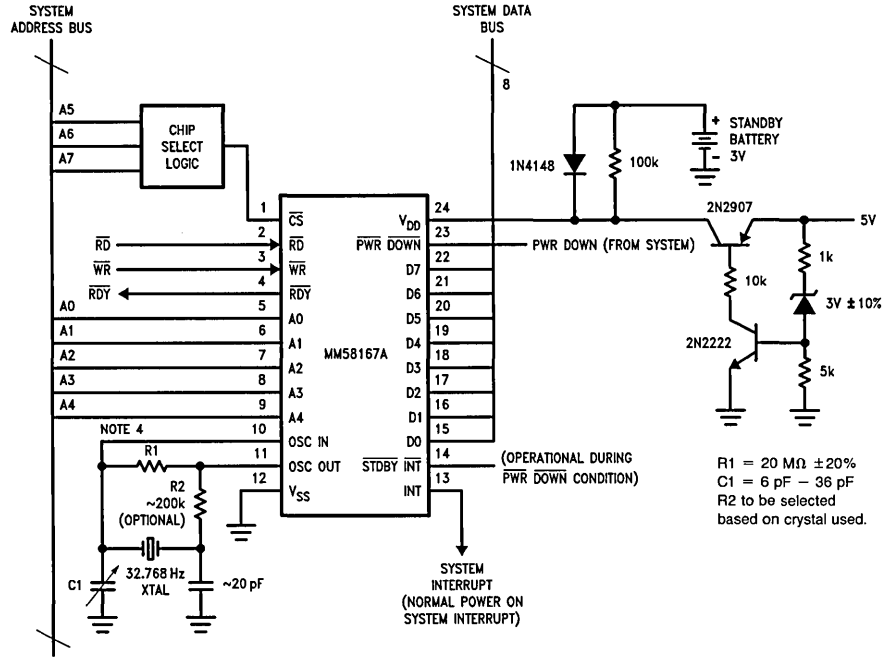
FIGURE 4. Write Cycle Timing

Typical Applications



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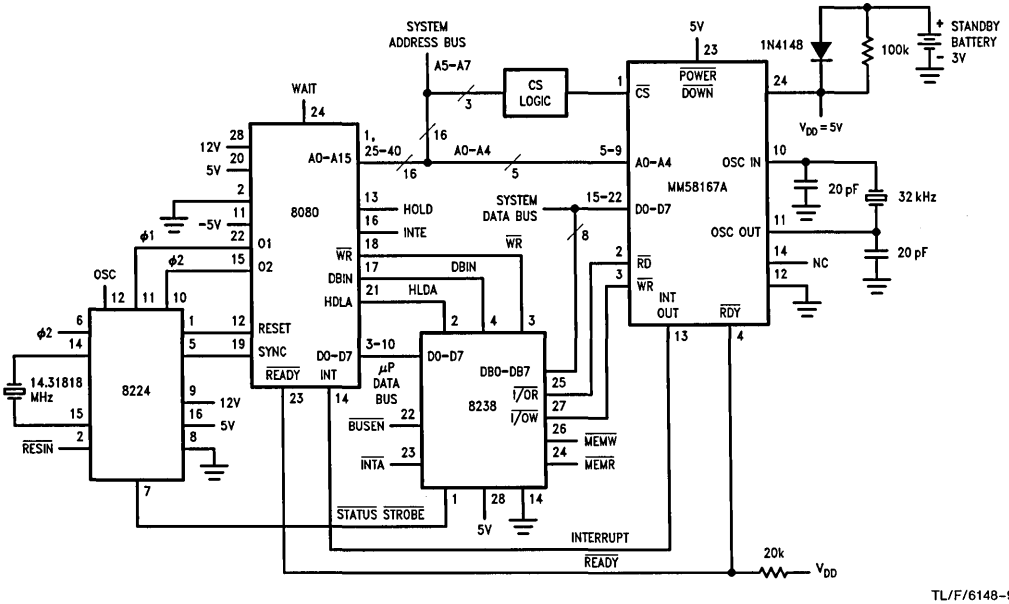
Note 5: A ground line or ground plane guard trace should be included between pins 9 and 10 to insure the oscillator is not disturbed by the address line.

FIGURE 5. Typical Connection Diagram



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Note 6: Must use 8238 or equivalent logic to insure advanced I/OW pulse; so that the ready output of the MM58167A is valid by the end of $\phi 2$ during the T2 microcycle.

Note 7: $t_{\phi 2} \geq t_{RS8080} + t_{DL8238} + t_{WRY58167A}$.

FIGURE 6. 8080 System Interface with Battery Backup

Block Diagram

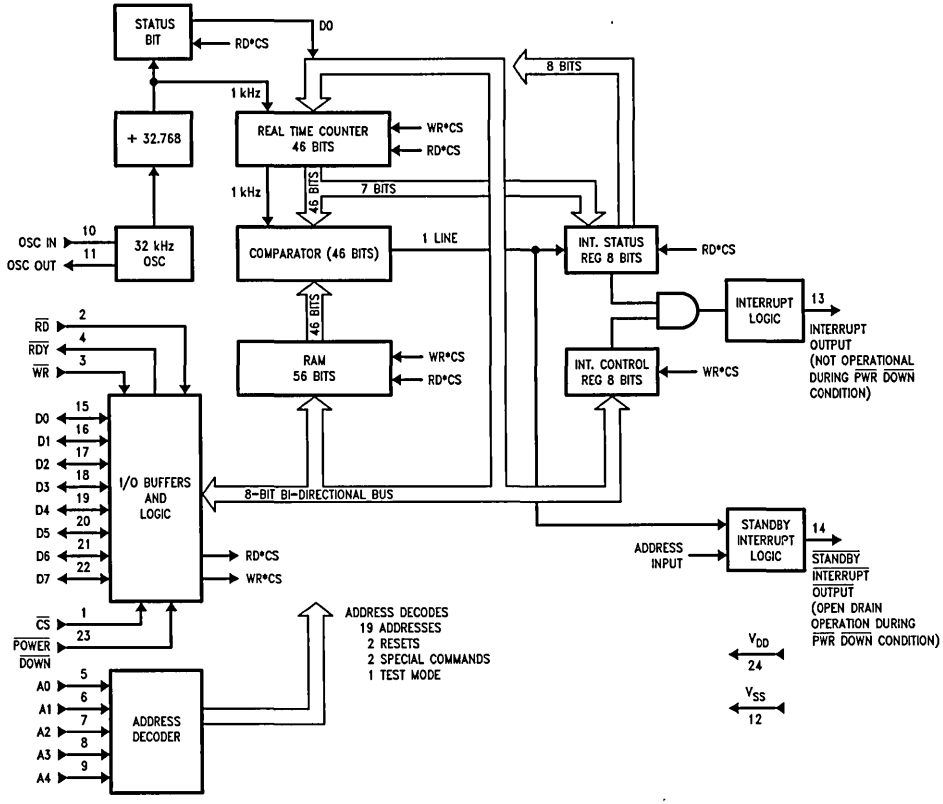

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FIGURE 7

Section 2

Application Notes

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MM58167A Real Time Clock Design Guide

National Semiconductor
Application Note 353
Milt Schwartz

The MM58167A is a real-time 24-hour format clock with input/output structure and control lines that facilitate interfacing to microprocessors. It provides a reliable source of calendar data from milliseconds through months, as well as 6 bytes plus 2 nibbles of RAM, which are available to the user if the alarm (compare) interrupt is not used. The MM58167A features low power consumption (typically 4.5 microamperes at 3-volt supply) during battery backed mode, flexible interrupt structure (alarm and repetitive), and a fast internal update rate (1 kHz). Systems utilizing this device include, personal computers, process control, security, and data acquisition.

This application note covers hardware interface to microprocessors, clock interrupts, oscillator operation, accuracy, calibration techniques, software, and battery back-up considerations.

Hardware Description Overview

1.0 *Figure 1* is a functional block diagram of the MM58167A. It can be subdivided into the following sections:

1.1 Oscillator

The oscillator consists of an internal inverter to which the user connects a 32.768 kHz crystal, bias resistor and capacitors, to form a Pierce parallel resonant circuit.

1.2 Prescaler

The prescaler divides the 32.768 kHz oscillator down to 1 kHz using pulse swallowing techniques. The 1 kHz pulse rate is the incrementing signal for the timekeeping counters.

Block Diagram

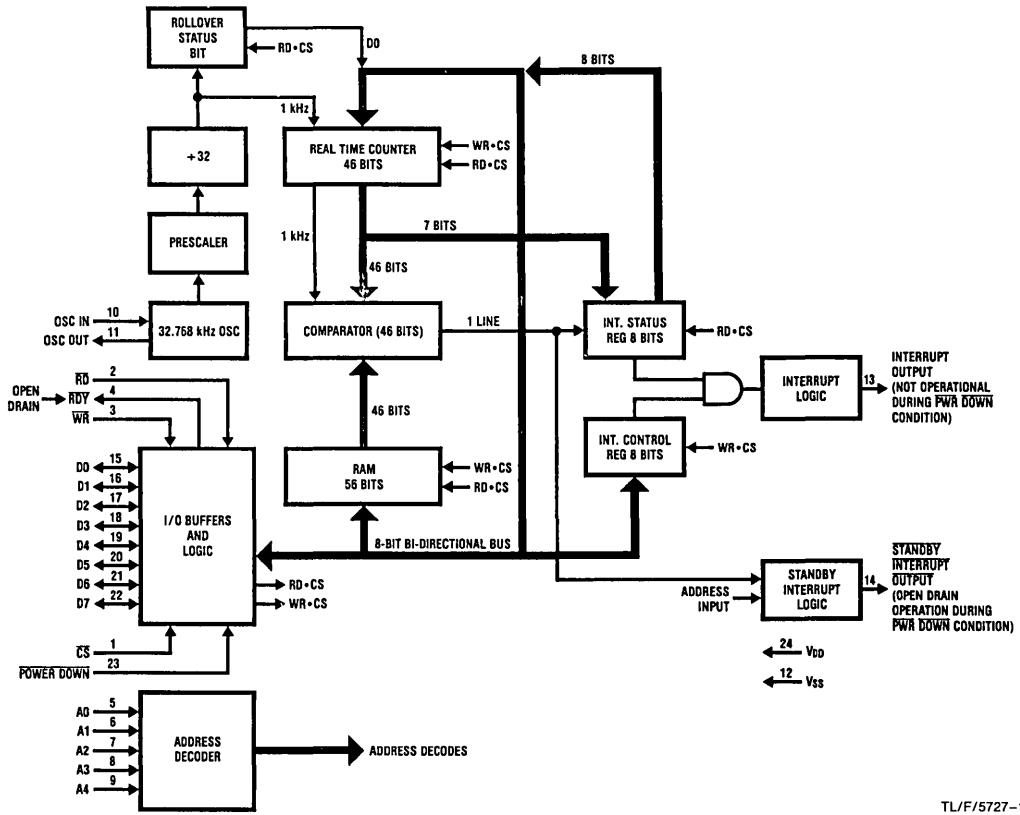


FIGURE 1

Hardware Description Overview (Continued)

1.3 Timekeeping Counters

The timekeeping section consists of a 14-stage BCD counter, each stage having read/write capability. The counters keep time in a 24-hour format. *Figure 6* shows the counter detail of calendar-date-time format.

1.4 Rollover Status

A rollover status bit (read only) informs the user that invalid data may have been read, due to the counters being incremented during a counter read or between successive counter reads. This situation occurs because the counters are clocked asynchronously with respect to the microprocessor.

1.5 RAM

14 nibbles of RAM are provided for alarm (compare) interrupt or general storage. The nibbles are packed 2 per address except for 2 locations, address 08 and 0D (HEX). The nibble at address 08 appears in the high order 4 bits, while the nibble at address 0D appears in the low order 4 bits. See memory map *Figure 2* for details.

Address In HEX	D7 D6 D5 D4	D3 D2 D1 D0
8	Milliseconds	No RAM Exists
9	Tenths of Seconds	Hundredths of Seconds
A	Tens of Seconds	Units of Seconds
B	Tens of Minutes	Units of Minutes
C	Tens of Hours	Units of Hours
D	No RAM Exists	Day of Week
E	Tens Day of Month	Units Day of Month
F	Tens of Months	Units of Months

FIGURE 2. RAM Memory Map

1.6 Comparator

A 46-bit comparator compares values in RAM against the counters to provide an alarm (compare) interrupt. When a compare occurs, the main interrupt will be activated if the D0 bit of the interrupt control register was set. The standby interrupt will be activated if a "1"was written to address 16 hex.

1.7 Interrupt Hardware

Interrupt hardware consists of two interrupt outputs. The main interrupt and the standby interrupt. The main interrupt is an active high push-pull output. The standby interrupt is an active low open drain output. For the main interrupt, an 8-bit control register allows the user to select from 1 to 7 interrupt rates, as well as an alarm. An 8-bit status register informs the user which of the 8 interrupts occurred. A one-bit control register enables/disables the standby interrupt. The standby interrupt is activated only for the alarm condition. A 46-bit comparator matches the timekeeping counters against RAM for the alarm interrupt.

1.8 Input/Output and Control Lines

The input/output structure consists of a 5-bit address bus and 8-bit bidirectional data bus. The control lines are chip select, power down, read and write. In addition, a ready output is provided for those microprocessors that have wait-state capability and meet the timing requirements of the ready signal. The power down input acts as a chip select of opposite polarity. It differs from the chip select in that it will TRI-STATE® the main interrupt output while the chip select does not TRI-STATE the interrupt. The power down input is intended to facilitate deselecting the chip for battery backed operation. Chip select, read and write are active low controls. The ready output is active low open drain and is caused by chip select and the negative-going-edge of read or write (it is an internal one-shot). If the ready output is not used as a control line when interfacing to a microprocessor, it may be left open circuit.

Detail Descriptions

OSCILLATOR

Figure 3 represents the internal and external circuitry that comprise the oscillator. The inverter, which is the heart of the oscillator, is designed to consume minimum power. The inverter has a typical gain of 30 at 1 kHz and 4 at 30 kHz. The oscillator input may be driven from an external source. If this is desired, the input should swing rail-to-rail and be approximately a 50% duty cycle. The oscillator output pin is open circuit for this case. The external oscillator circuit may be constructed using a CMOS inverter or N-FET (see *Figures 4a* and *4b*). Referring to *Figure 3*, the external 20 MΩ resistor biases the inverter in its active region. The internal feedback resistor may be too large in value to guarantee reliable biasing.

The external series resistor is to protect the crystal from being overdriven and possibly damaged. Manufacturers of these crystals specify maximum power that the crystal can dissipate. It is this rating which determines what value of series resistor should be used. The two external capacitors are effectively in series with each other (from an A.C. viewpoint). This total value comprises the load capacitance (typically 9 to 13 picofarad) specified by the crystal manufacturer at the crystal's oscillating frequency. The rule of thumb in choosing these capacitors is:

$$1/\text{load capacitance} = 1/C1 + 1/C2$$

C2 is greater than C1 (typically two to four times)

C1 is usually trimmed to obtain the 32768 Hertz frequency.

The start-up time of this oscillator may vary from two to seven seconds (empirical observation) and is due to the high "Q" of the crystal. Typical waveform values monitored at the oscillator output are observed to be 3 volts peak to peak riding on a 2.5 volt D.C. level (for V+ = 5 volts).

CHOOSING THE CRYSTAL

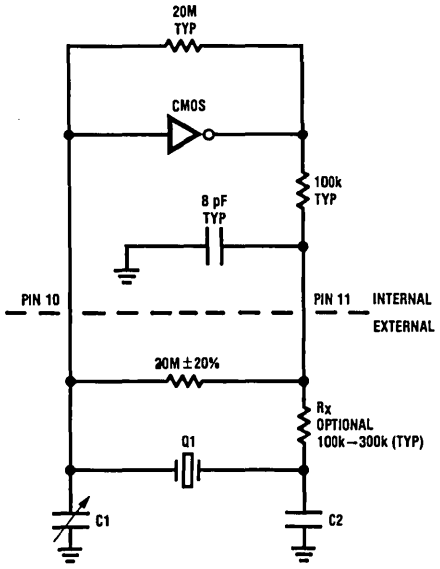
The below parameters describe the crystal to be used

Parallel Resonant, tuning fork (N cut) or XY Bar

$Q >= 35{,}000$

Load Capacitance (CL)	9 to 13 Picofarad
Power Rating	20 Microwatt Max.
Accuracy	User Choice
Temperature Coefficient	User Choice

Detail Descriptions (Continued)



Q1 = 32,768 Hz

Mnfg.	Tel.#
RCD	800-228-8108
Saronix	415-856-6900
Reeves-Hoffman	717-243-5929

C1 = 5 → 30 pf
Circuit Specialists
Part# 275-0430-005
Tel.# 1-800-528-1417
Johanson #9613 or #9410-3 pc.
Tel.# 201-334-2676
C2 = 15 → 20 pf mica

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FIGURE 3. Oscillator Circuit and Recommended Connections

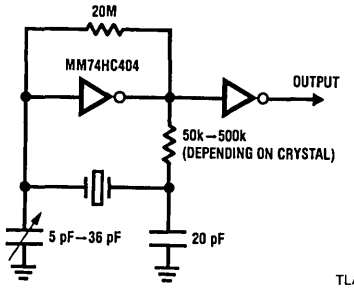

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FIGURE 4a

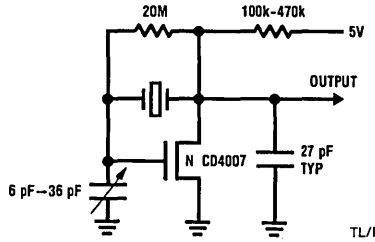

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FIGURE 4b

When used with a crystal, the accuracy of the oscillator circuit over voltage and temperature is about +/− 10 PPM. Voltage variations cause about 50% of the inaccuracy and temperature variations account for the other half. This inaccuracy results in an error of about 5 minutes per year. Errors due to external components must be taken into account by the user. If an external oscillator is used, then it determines the accuracy of the clock. The oscillator input pin (pin 10), is a high impedance node that is susceptible to 'noise'. The usual result is the clock gains time at a high rate (on the order of seconds per hour or greater). This noise is usually the result of coupling from pin 9 which is a low order address bit if tied directly to a microprocessor bus. Suggestions to alleviate this condition are:

1. Gate pin 9 with chip select.
2. Use a slow rise and fall time non inverting buffer such as a CMOS to drive pin 9. If this choice is made, similar CMOS should drive the write and read strobes to avoid timing conflicts.
3. Use an external oscillator and drive pin 10 with a low impedance device (CMOS or transistor), leave pin 11 open circuit.
4. Connect all oscillator components as close as possible to pins 10 and 11.

CALIBRATION

To calibrate the oscillator the following method is suggested. The one second repetitive interrupt is activated. This is done by first connecting the interrupt (pin 13) of the clock to the interrupt of the microprocessor. Next a short program is written that sets bit D2 of the interrupt control register, and then enters a loop that wastes time while awaiting an interrupt. The interrupt service routine only needs to read the interrupt status register, which clears the interrupt, and then returns. The result is a 1 second periodic signal at pin 13.

The flow chart of *Figure 5* is an example of the detail steps. A time event meter is used to measure the time interval between successive positive going edges of the interrupt output while adjusting the variable capacitor C1. This period will be 1 second when the oscillator is at 32,768 Hertz.

Detail Descriptions (Continued)

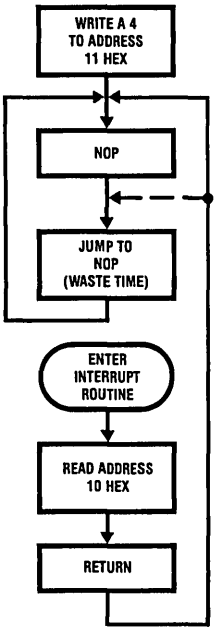

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FIGURE 5. Flow Chart for Calibration Using the 1 Hz Repetitive Interrupt

If the 32,768 Hertz is to be measured directly, then a HI impedance LO capacitance amplifier or comparator or CMOS gate should be connected to the oscillator output pin to prevent the measuring instrument from offsetting the frequency of the oscillator. This addition is permanently a part of the oscillator circuit and must be battery backed if the clock is battery backed. The reason for battery backing this buffer is to ensure that its input impedance does not change during the power down operation which could result in the oscillator stopping or being offset in frequency.

PRESCALER OPERATION

The 32,768 Hertz signal is divided to an even 32,000 Hertz using pulse swallowing techniques. This is accomplished by dropping three pulses every 128 counts of the 32,768 Hertz signal. The resulting 32 kHz is then divided to produce 1 kHz which is the internal incrementer for the rest of the timekeeper. This 1 kHz waveform is nonmonotonic with respect to individual periods. As a result, there are 750 short and 250 long periods within a one second interval.

The short period is 1/1024 seconds, and the long period is [1/1024 +3/32768] seconds. As a result, the milliseconds, hundredths and tenths of seconds "jitter". The inaccuracy on an individual period basis is about 91 microseconds. The period and number of clock edges are correct over one second within the accuracy of the crystal oscillator. The ten thousandths of seconds counter referred to in the data sheet counts milliseconds. The 1 second and slower signals are jitter free. Refer to *Figure 6* for counter block diagram.

TIMEKEEPING COUNTERS

The timekeeping counters are intended to work with valid BCD values. In general, if illegal codes are entered then no guarantee is given for recovery. As shown in *Figure 6*, the timekeeping stages are arranged as a ripple counter. The month, day of month, and day of week counters count 1 through N. The milliseconds through hours counters count 0 through N. The rollover of a counter stage increments the next higher order counter. This rollover takes place when the highest allowed value plus one is decoded. For example, in a 30-day month, the day of month counter would decode the value 31, reset to one and increment the month counter. If the highest allowed value plus one is written to a counter, the counter will reset when the write is removed and "may" increment the next higher order counter.

For example, if February 29 is written to the clock, the read back will be a "1" in the day of month counter and the month may read "3". However, for leap year use, February 31 may be written. If this is done on Mar 1 at 0 (hours through milliseconds), then the clock will read March 1 after 24 hours. In this way, the value Feb 31 could be used as an indication that the date is really Feb 29. Refer to *Figures 7A 7B,* and *7C* for flowcharts of a program and alarm interrupt bit map that take leap year into account. Note that the software implemented leap year counter is accurate at least through the year 2048. For a perpetual calendar, a more sophisticated algorithm would be needed.

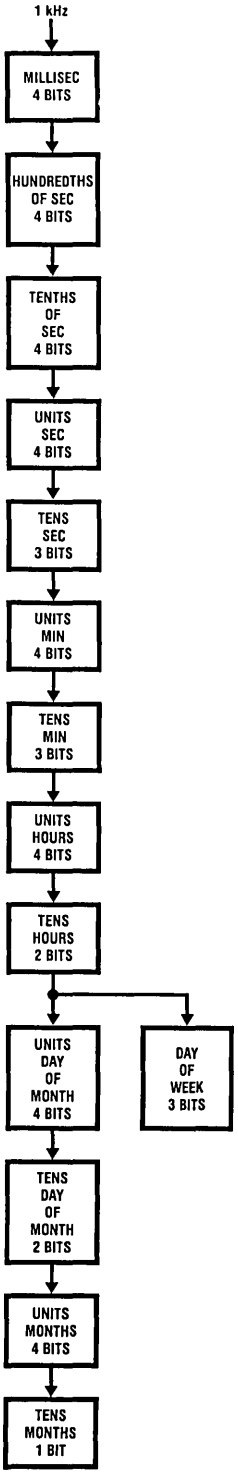

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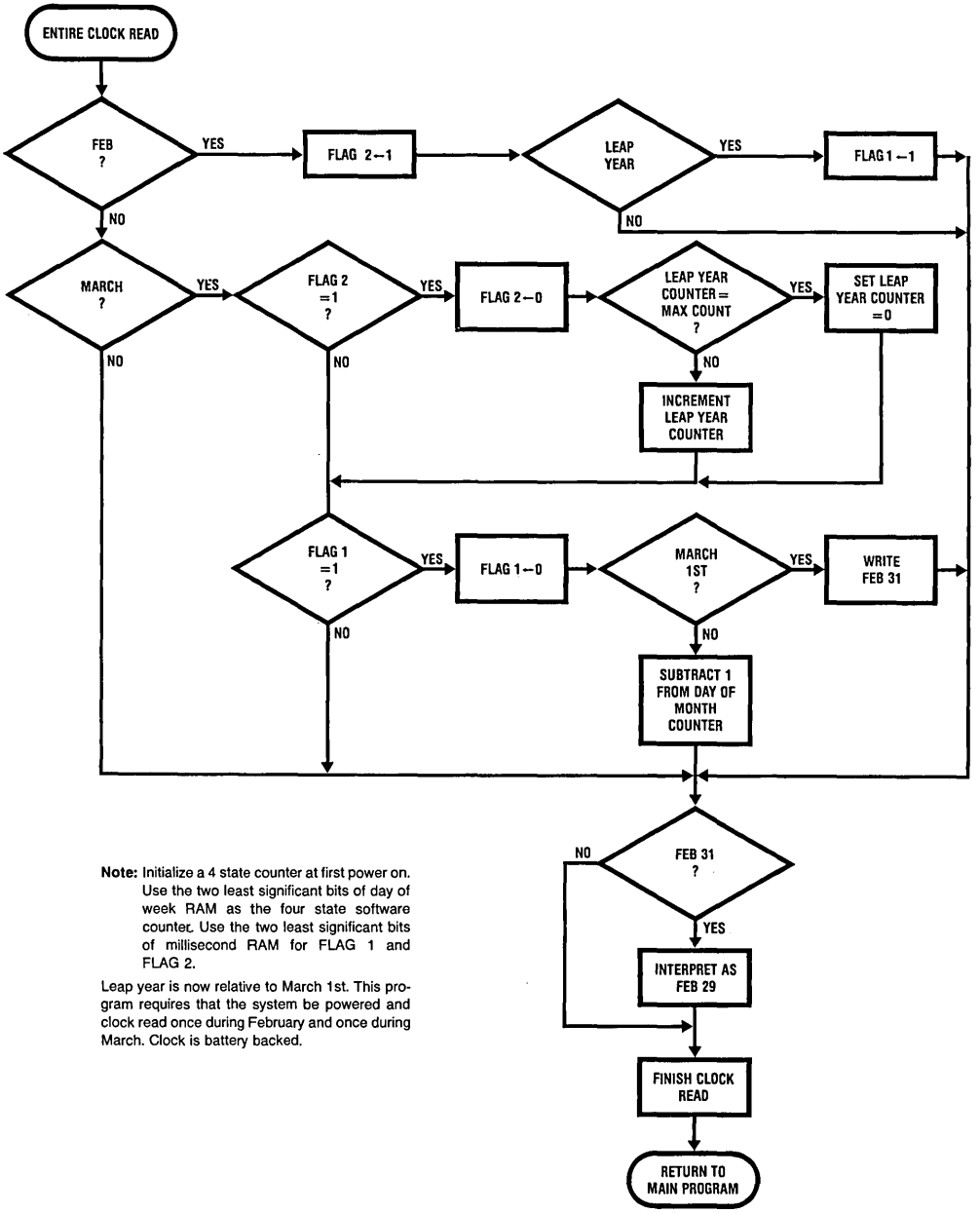
FIGURE 6. BCD Timekeeping Counters



Note: Initialize a 4 state counter at first power on. Use the two least significant bits of day of week RAM as the four state software counter. Use the two least significant bits of millisecond RAM for FLAG 1 and FLAG 2.

Leap year is now relative to March 1st. This program requires that the system be powered and clock read once during February and once during March. Clock is battery backed.

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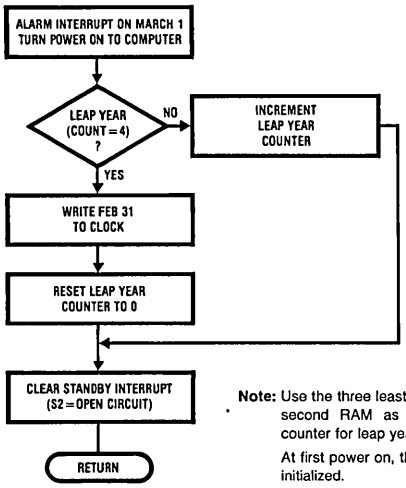
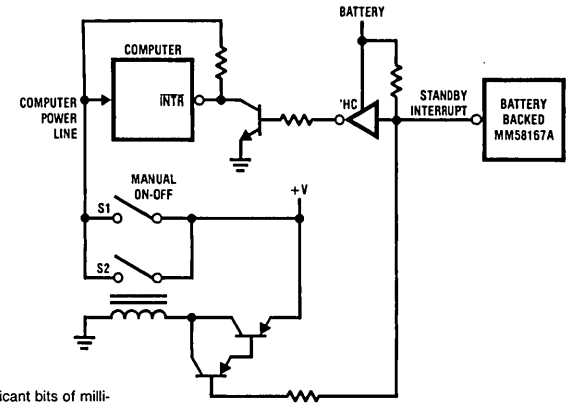
FIGURE 7A. Leap Year Flow Chart





Note: Use the three least significant bits of milli-second RAM as a five-state software counter for leap year.

At first power on, the leap year counter is initialized.

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FIGURE 7B. Leap Year Flow Chart and Hardware

Function	Address					DATA							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	0	0	0	0	0	0
Hours	0	1	1	0	0	0	0	0	0	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	0	0	0	0	0	0	0	1
Months	0	1	1	1	1	0	0	0	0	0	0	1	1

FIGURE 7C. Clock RAM Bit Map For Alarm Interrupt on March 1@ 0 Hrs

INTERRUPTS

The 58167 has two interrupt output pins. The main interrupt (pin 13) is active "high", and is active when the power down pin is "high". When power down (pin 23) is low, the main interrupt output is TRI-STATE. The second interrupt is the "standby interrupt" and is an active low open drain requiring a pull up resistor to VDD. This interrupt is always powered. Refer to *Figure 8* for typical sink current versus voltage out characteristics. Separate control bits exist for the two interrupts. The main interrupt offers two modes of operation which may be combined. Mode 1 is the interactive repetitive interrupt. For this case, a logic 1 is written to one or more bits in the control register (address 11 hex) from D1 through D7, a logic 0 is written into the D0 position. Refer to *Figure 9* for bit configuration of the interrupt control and status registers.

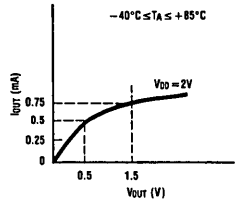

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FIGURE 8. Typical Curve of I vs V of Standby Interrupt

As a result, the clock chip provides an interactive repetitive interrupt, that occurs when the selected counter rolls over. That is, the user must clear the interrupt so the next one can be recognized. This is done by reading the interrupt status register (address 10 hex). This read results in the user obtaining the interrupt status (which interrupt occurred) and the clearing of the interrupt output as well as the status register. It is the positive-going-edge of the read strobe which causes the preceding. This clearing action precludes polling the status register. For precision timing, the positive-going-edge of the repetitive interrupt should be used as a trigger. The one-per-second through one-per-month repetitive interrupts will be as accurate as the setting of the crystal oscillator. The ten-per-second interrupt will be accurate to about 91 microseconds. Refer to prescaler description for more detail.

The second mode of main interrupt is the "compare" or "alarm". In this case, a specific value is entered in the RAM of the clock. When the time keeping counter(s) match that value, the interrupt becomes active. Refer to *Figure 11* for a typical example. *Figures 9* and *10* show internal interrupt logic and waveforms. In addition to a specific one time interrupt (alarm), a repetitive interrupt can be achieved by reprogramming the selected RAM location with a future event value. The rule of thumb for an "alarm" interrupt is: All nibbles of higher order than specified are set to C hex (always compare). All nibbles lower than specified are set to "zero".

A programming example of the fastest interrupt rate obtainable (500 per second) is given in *Figure 12*. This program written in NSC800™ code (Z80) sets "always compare" conditions (CC hex) in RAM locations 9 through C, E and F. RAM location D which corresponds to the day of the week counter (a single digit), is set to C. RAM location 8 is set to 0. When the first interrupt occurs, the service routine reads the status register and sets the value 2 into RAM location 8. At succeeding interrupts, the values 4, 6, 8 are set into location 8 and the sequence repeats.

If an interrupt is activated and the interrupt occurs during battery backed operation (power down), the main interrupt output will be active high when system power returns.

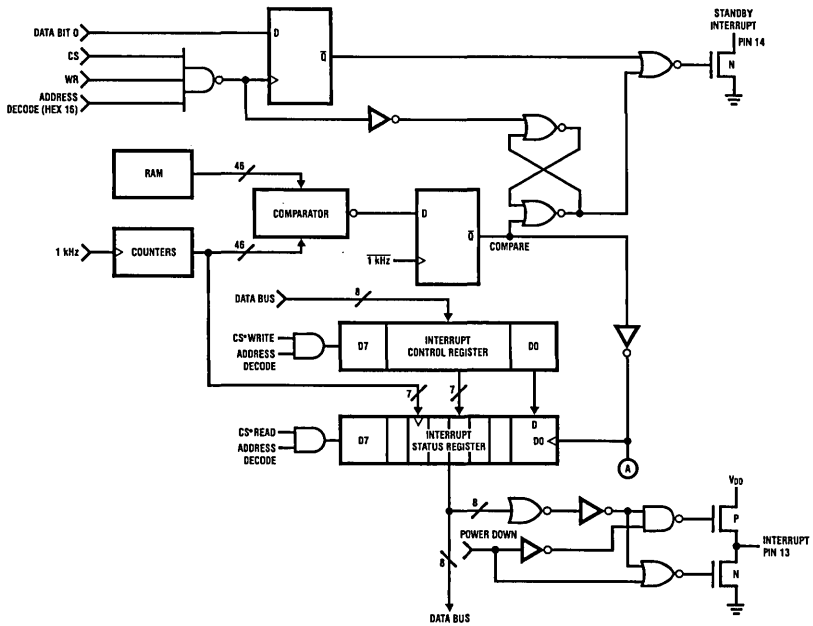

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FIGURE 9. Interrupt Registers and Logic

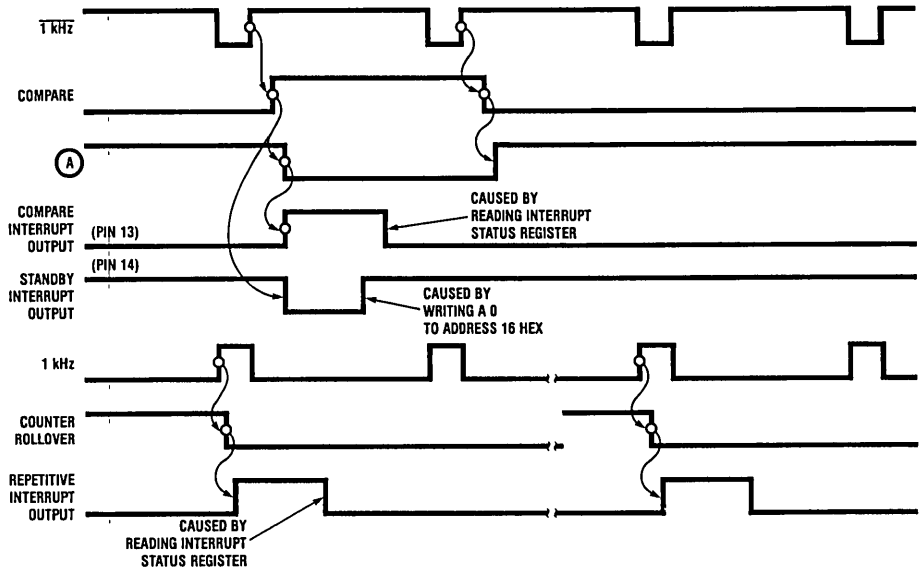

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FIGURE 10. Internal Interrupt Timing

Function	Address					DATA							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	1	0	0	0	1	0
Hours	0	1	1	0	0	0	0	0	1	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	1	1	X	X	1	1	X	X
Months	0	1	1	1	1	1	1	X	X	1	1	X	X

FIGURE 11. Ram Mapping for Alarm Interrupt at 10:22:00 Every Day

```
                NAME ('I500Hz')
                TITLE 58167 500HZ REPETITIVE INTERRUPT (10/13/83)

                ;THIS PROGRAM IS FOR USE WITH THE 58167 POWER DOWN BOARD
                ;INTERFACED TO THE NSC888 BOARD. CODE IS NSC800.
                ;A 500HZ SIGNAL IS GENERATED AT THE INTERRUPT PIN (13).
                ;THIS SIGNAL IS GENERATED USING THE COMPARE INTERRUPT
                ;AND UPDATING THE ''RAM'' FOR THE NEXT INTERRUPT


                                        ORG 0800H

4092                            RESET EQU 04092H
4091                            CONT  EQU 04091H
4090                            STAT  EQU 04090H
408F                            MON   EQU 0408FH
408E                            DOM   EQU 0408EH
408D                            DOW   EQU 0408DH
408C                            HRS   EQU 0408CH
408B                            MIN   EQU 0408BH
408A                            SEC   EQU 0408AH
4089                            HT    EQU 04089H
4088                            MIL   EQU 04088H
101C                            VEC1  EQU 0101CH
101D                            VEC2  EQU 0101DH


0800'  3E 00                    INIT:   LD      A,0             ;SET UP INTRPT FOR NSC888
0802'  32 101C                          LD      (VEC1),A        ;         *
0805'  3E 09                            LD      A,009H          ;         *
0807'  32 101D                          LD      (VEC2),A        ;         *
080A'  3E 08                            LD      A,8             ;         *
080C'  D3 BB                            OUT     (0BBH),A        ;         *
080E'  31 1FFF                          LD      SP,01FFFH       ;INIT STACK POINTER
0811'  3E FF                            LD      A,0FFH
0813'  32 4092                          LD      (Reset),A       ;RESET ALL CLOCK COUNTERS
0816'  3E 00                            LD      A,0
0818'  32 4091                          LD      (CONT),A        ;CLEAR INTRPT CONTROL
081B'  3A 4090                          LD      A,(STAT)        ;CLEAR ANY PENDING INTRPT
081E'  3E CC                            LD      A,0CCH          ;SET RAM FOR INTRPT
0820'  32 408F                          LD      (MON),A
0823'  32 408E                          LD      (DOM),A
0826'  32 408D                          LD      (DOW),A
0829'  32 408C                          LD      (HRS),A
082C'  32 408B                          LD      (MIN),A
082F'  32 408A                          LD      (SEC),A
0832'  32 4089                          LD      (HT),A
0835'  3E 00                            LD      A,0
0837'  32 4088                          LD      (MIL),A
083A'  3E 01                            LD      A,1
083C'  32 4091                          LD      (CONT), A       ;SET COMPARE INTRPT
083E'  FB                               EI
0840'  00                       NOP:    NOP
0841'  C3 0840                         JP      NOP             ;WASTE TIME AWAITING
                                                                ;INTERRUPT
                                ;INTERRUPT SERVICE ROUTINE GETS THE VALUE IN THE
                                ;MILLISECOND RAM, TEST FOR 8. IF YES THEN SET RAM
                                ;EQUAL TO 0, CLEAR INTERRUPT AND RETURN.
                                ;IF NO, ADD 2 TO RAM MILLISECOND,
                                ;CLEAR INTERRUPT AND RETURN.
                                ;''REMEMBER'' RAM MILLISECONDS IS ''HIGH'' ORDER NIBBLE
                                ;ONLY

                                        ORG 0900H

0900'  3A 4088                  ZERO:   LD      A,(MIL)         ;GET RAM MILLSEC
0903'  E6 F0                            AND     0F0H            ;MASK
0905'  FE 80                            CP      080H            ;? RAM=8
0907'  CA 0912'                         JP      Z,ZERO
090A'  C6 20                            ADD     A,020H
090C'  32 4088                          LD      (MIL),A
090F'  C3 0917'                         JP      RETRN
0912'  3E 00                            LD      A,0
0914'  32 4088                          LD      (MIL),A
0917'  3A 4090                  RETRN:  LD      A,(STAT)        ;CLEAR INTRPT
091A'  FB                               EI
091B'  C9                               RET

                                                END
```

FIGURE 12. NSC800 Assembly Code for 500 Hz Interrupt

STANDBY INTERRUPT

A "1" written to address 16 hex enables the standby interrupt and a "0" disables it. This interrupt also becomes active when a match exists between time keeping counter(s) and a value written into RAM. The standby interrupt can be cleared as soon as it is recognized. The user should ensure that a delay of one millisecond or greater exists prior to reenabling the standby interrupt. This delay is necessary because of the internal signal level which causes the interrupt. If this delay does not occur, then the standby interrupt becomes reactivated until the internal latched compare goes away, which occurs at the next 1 kHz clock. *Figure 10* illustrates interrupt timing.

RAM

RAM is organized as shown in *Figure 2*. There are 4 bits of RAM for each BCD counter. The RAM may be used as general purpose or for an alarm interrupt. It is possible under certain conditions to perform the compare interrupt and use selected bits of the RAM for general purpose storage. Any RAM position that is set for the 'always compare' condition allows the user to manipulate the 2 LO order bits in each nibble. However, the 2 high order bits in each nibble position must be maintained as logic 1'S. For example, the user may have an alarm interrupt that does not use the day of the week as a condition for interrupt. Therefore the 2 low order bits might be used as a 4 state software counter to keep track of leap year. Reading and writing the RAM is the same as any standard RAM.

HARDWARE INTERFACE CONSIDERATIONS

There are four basic methods of interfacing the 58167A to a microprocessor. They are memory mapped, microprocessor ports (for single chip microprocessors like the 8048), peripheral adapter, and separate latches. The advantage of memory mapped interface is use of all memory reference instructions. The disadvantages are the processor may need to be "wait-stated" and the environment is noisier with respect to the crystal oscillator. Refer to *Figure 13* for typical bus interface.

Microprocessors that have separate ports (16 are sufficient) offer the capability to interface directly without "wait-stating", or additional device count. Eight of the port bits (data) need to be bidirectional for this interface. *Figure 14* indicates port interface. Programmable peripheral interface devices such as the 8255A or NSC810 afford the user the advantage of timing control by data bit manipulation, as well as a less noisy environment with respect to the oscillator circuit. *Figure 15* depicts the 8255A and NSC810 interface.

External latches may be used in place of the programmable peripheral interface device. This results in higher package count but easier troubleshooting. Also, the latches do not have to be manipulated through a control register. *Figure 16* illustrates the external latch approach. For the peripheral approaches, address, data, chip select, read and write strobes are manipulated by controlling the data bus bits via program execution. The peripheral interface approach facilitates calibration of the oscillator because the chip select, read strobe, and address lines can be set to steady state logic levels. Refer to calibration techniques for more detail.

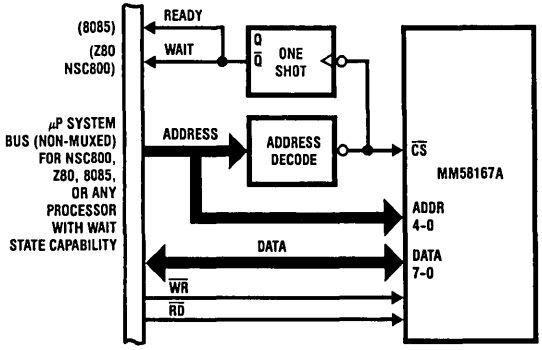

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FIGURE 13. Typical μP Bus Interface

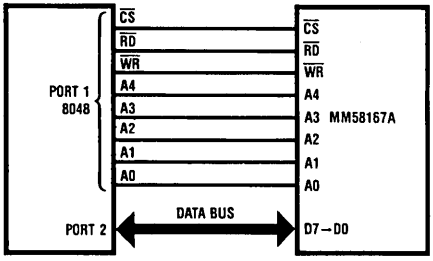

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FIGURE 14. MM58167A Interfaced to Single Chip Microcomputer

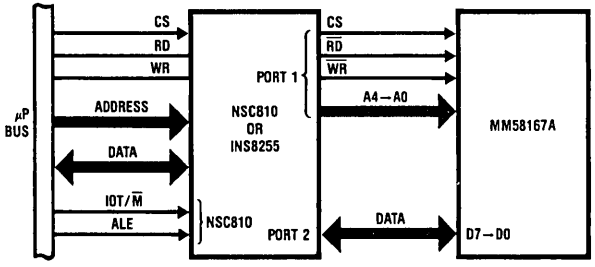

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FIGURE 15. MM58167A Interfaced to μP Through Peripheral Adapter

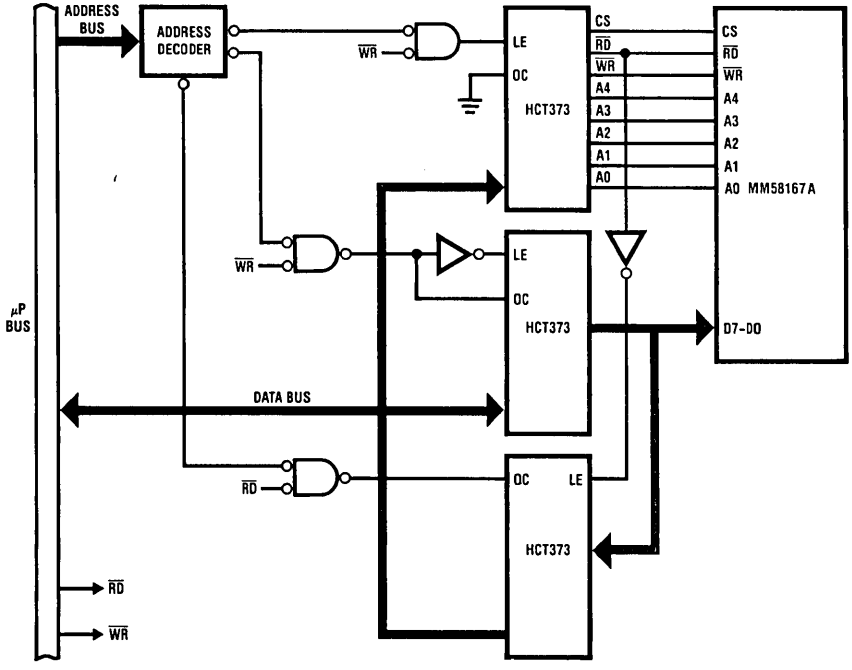

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FIGURE 16. MM58167A Interfaced to μp Using TRI-STATE Latches

POWER DOWN/BATTERY BACKED CONSIDERATIONS

Battery back up of the clock may be considered by the user to maintain time during power failure, provide a "wake-up" alarm, save the time that power failure occurred, calculate how long power failure lasted. The first step in providing a battery backed system is to isolate the system supply from the battery. This is to ensure that the battery is not discharged by the system supply when power failure occurs. *Figure 17* shows two techniques to achieve isolation. *Figure 17A* is implemented using diodes to isolate. In one case a Schottky diode is used to guarantee minimum voltage drop loss, while in the other case an adjustable voltage regulator (LM317) is used from a higher voltage and regulated to about 5.7 volts. A 1N914 diode in series with the regulator achieves the 5 volts for the clock. The Schottky diode has a drop of about 0.3 volts. Thus the V+ of the clock is typically at 4.7 volts. The user must be cautious about input signals not exceeding the 4.7 volt V+, since the clock is a CMOS device. This situation could arise if the devices driving the inputs of the clock were CMOS and received power from the 5 volt system supply. *Figure 17B* makes use of the low saturation of a PNP transistor (0.1 volt) to take care of the above situation. The NPN transistor is used to achieve isolation. The zener diode ensures that the circuit stops conducting and appears open circuit before the battery switches in.

Some basic considerations must be adhered to in a power down situation where the real time clock is battey backed. One is to ensure no spurious write strobes accompanied by a chip select occur during power down or power up. Another is to guarantee the system is stable when selecting/deselecting the clock. Also, any legitimate write-in-progress should be completed. To accomplish this, hardware is implemented such that early power failure is detected (usually a comparator detects DC failure, a retriggerable one-shot detects AC failure) See *Figures 18* and *19*. At this point the clock chip is deselected. The worst case is the power fails faster than the detection circuit can cause deselection. When power returns, the hardware detects power on, but the system must be stable before communication is allowed with the real-time-clock.

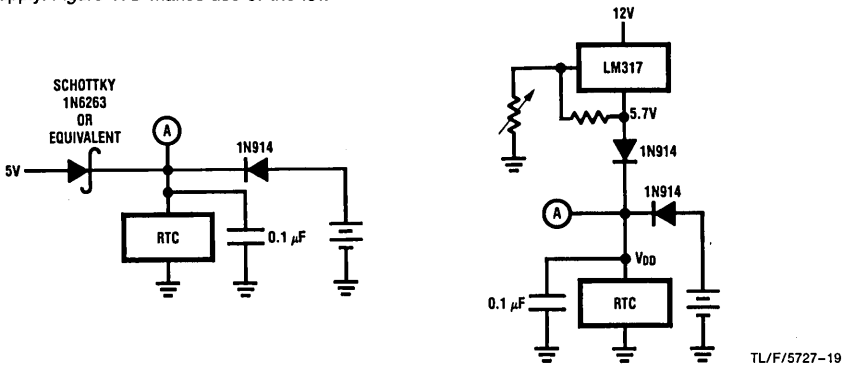

FIGURE 17. Isolating System Supply from Battery

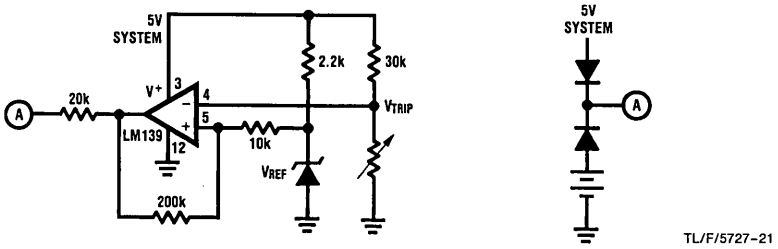

FIGURE 18. Sensing D.C. Failure Using a Comparator

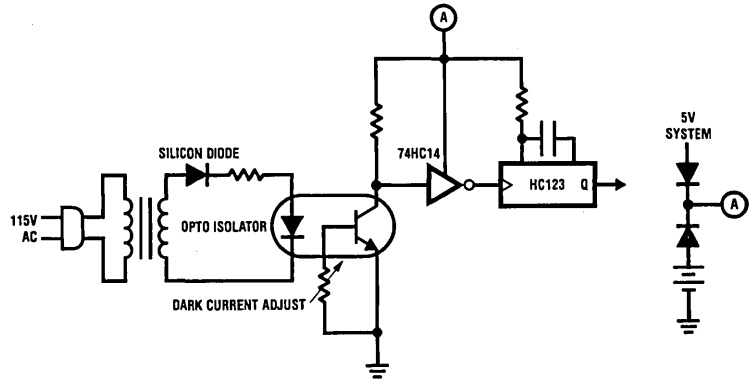

FIGURE 19. Sensing AC Line Failure Using Retriggerable One Shot

The 5-volt system supply rise and fall time characteristics during power turn on and power failure must be known. Care should be taken to allow a legitimate write in progress to be completed. This is necessary because a "short write" could cause erroneous data to be entered to the clock. If the clock is used as a "read only" device (except for initialization of calendar and time), the circuitry to allow a write in progress to be completed does not have to be considered. For this situation, a switch in series with the write strobe could be implemented such that the write line to the clock is "tied high" after initialization.

To sense system DC power failure a comparator and voltage reference may be used. *Figure 20*, detail 1, shows the comparator and voltage reference configured such that the comparator output is "low" when 5-volt system power is greater than 4.6 volts. If possible, the power fail trip point should be referenced to a lightly loaded (fast collapse) DC supply, preferably higher than the 5-volt system. This would allow early sense of power failure. When using comparators, the output may oscillate as the trip point is approached. The oscillation is caused by noise on the DC line appearing at the input to the comparator when at or near the trip voltage. The cleaner the supply, the less chance of oscillation. In all cases, hysteresis should be used to minimize oscillations. Note that the 20 kohm pull-up resistor is connected to the battery backed node, while the LM139 V+ pin is connected to the 5-volt system supply. Used this way, the comparator does not draw any current except leakage from the battery and the output remains high during power down.

To sense AC failure, a retriggerable one-shot may be used. The RC time out may be adjusted to allow for one or more cycles of 60 Hertz to be missed. Using this approach, the Q output of the one-shot is always high while 60 Hertz is present. When a cycle is missed the one-shot times out and Q goes low. *Figure 19* shows AC sensing. This technique could cause a spurious deselect of the clock if a "glitch" occurs on the AC line resulting in a missed cycle.

For this application, the circuit shown in *Figure 20* was implemented. The MM58167A was interfaced to the NSC800 in memory mapped locations. A demo program was written to exercise the clock, and display time, date and calendar. Power was switched on and off at irregular intervals, to test the battery backed circuitry. The results were that the clock kept correct time. Battery backed current for all circuitry was 10 microamp. For general consideration, this circuitry allows a chip select in progress to be completed.

FUNCTIONAL OPERATION OF *FIGURE 22*

Power up sequencing consists of the LM139 (comparator) making a high to low transition when the 5-volt system supply exceeds 4.6 volts. This transition triggers the 0.5 second one-shot causing its output to be low and removes the low reset on the D flip-flop through nand gate J. The output of the 2 microsecond one-shot is "don't care" once the comparator switches from high to low. After 0.5 seconds, the system is assumed to be stable, and the D flip-flop output which was reset is clocked high by the low to high transition of the 0.5 second one-shot. Thus, the clock chip is enabled allowing normal communication with the microprocessor.

The power down sequence consists of the comparator making a low to high transition when the 5-volt supply is less than 4.6 volts. If no chip select is present, the D flip-flop is reset through nand gate J, causing pin 23 of the clock to be low (deselected). If a legitimate chip select was in progress, the reset action through nand gate J would be delayed by the low level of the 2-microsecond one-shot.

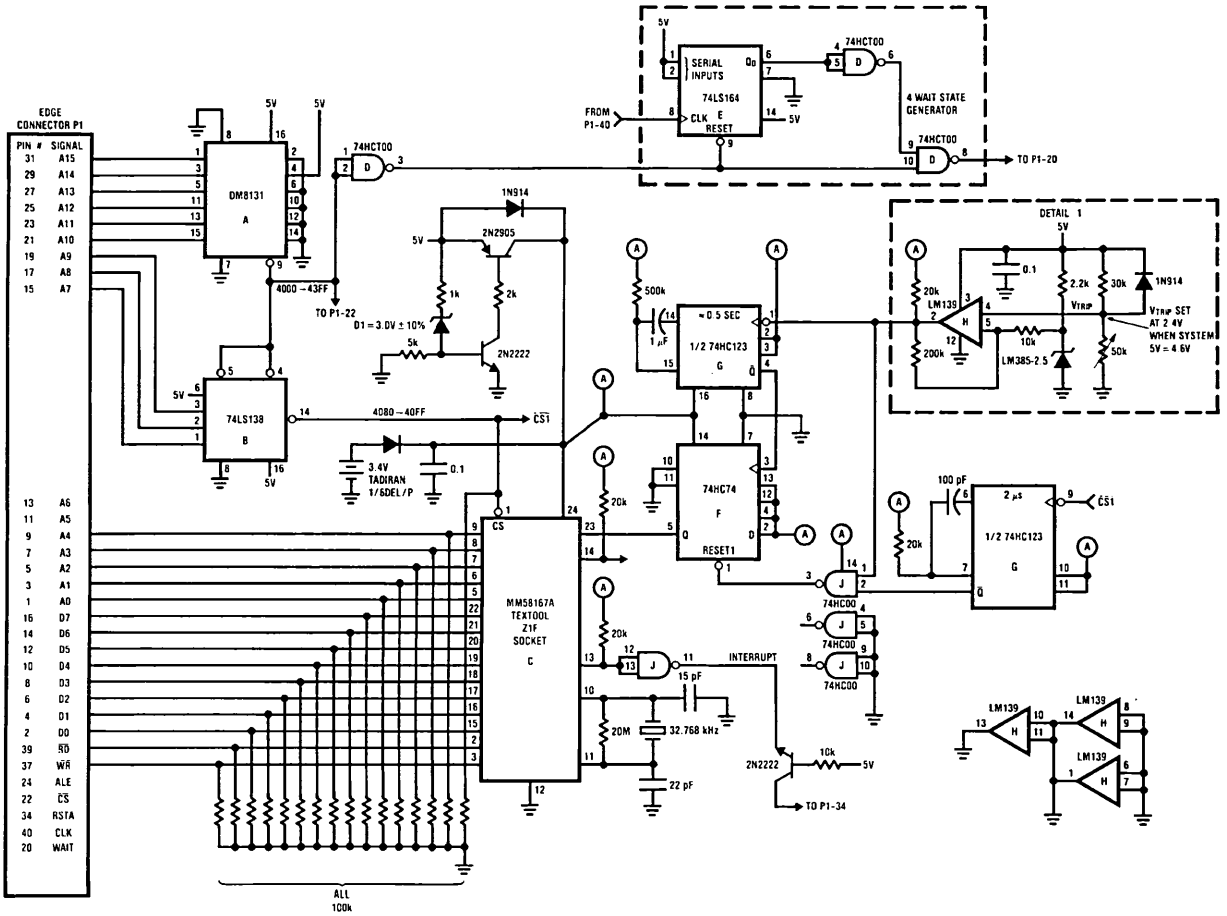

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FIGURE 20. Detailed Schematic of Power Down Circuitry, and Interface to NSC888 Board

A wait state generator was implemented using the chip select as the sensing signal. This was necessary to comply with NSC800 wait state timing. The wait generator provides 2 microseconds of access time, which is more than adequate to meet clock chip timing requirements. Pull-down resistors were added to all clock input pins to guarantee no floating inputs during power down. This ensures that the CMOS clock does not draw excessive current from the battery during power down. A diode isolates 5-volt system from the battery (A 3.4-volt Tadiran nonrechargeable lithium cell was used in this application). The battery is isolated from the 5-volt supply using a circuit comprised of PNP and NPN transistors along with a zener diode. The zener diode value was selected such that the combined voltage drop of the zener and the base emitter of the NPN transistor was greater than the battery voltage. This ensures no current will be drawn from the battery by the 5-volt supply when power failure occurs.

The battery is non rechargeable, but allows up to 10 microamps of charge current without damaging the cell. An LM139 voltage comparator and LM385-2.5 voltage reference were used to sense the 5-volt system supply. The trip point was adjusted such that when the 5-volt supply dropped to 4.6 volts, the comparator switched from low to high. Observation of the comparator output showed oscillation, but caused no malfunction. The duration of the oscillation was about 100 microseconds. Burst noise on the 5-volt supply was about 0.5 volts peak to peak. For the circuitry implemented, the 5-volt supply should fall no faster than 1 volt per millisecond. This rate allows 100 microseconds for deselect to take place while the supply is falling from 4.6 volts to 4.5 volts. Thus, deselect occurs while the system is stable.

Miscellaneous

TEST MODE

The test mode applies the oscillator output to the input of the millisecond counter. This affords faster testing of the chip. This mode is intended for factory testing, where a programmable pulse generator is used. A pulse rate of 50 kHz may be used in this mode. The pulse should swing rail to rail and be a square wave. Apply the pulses to the oscillator input pin, leaving the oscillator output pin open circuit. The basic sequence would be to write values to the counters, enter test mode and apply a known number of pulses. Next, read the counters using normal read sequence.

GO COMMAND

A write to address 15 hex (data is a "don't care") will clear the seconds through milliseconds counters. If the value in the seconds counter is equal to or greater than 40 when the GO command is executed, then the minute counter will be incremented.

RESET COMMAND

Writing the value FF hex to address 12 hex causes the hours through milliseconds counters to be reset to zero. The day of week, day of month, and month counters are set to 1.

Writing the value FF hex to address 13 hex causes the RAM to be cleared.

GENERAL TIMING CONSIDERATIONS:

To guarantee a valid read/write without using the ready output, the following criteria must be met.

Read Operation

When reading, a deselect time of 500 nanoseconds must occur between counter reads. Read strobe width must not exceed 800 microseconds. The deselect condition is: $\overline{CS}$ = 1 or $(\overline{RD}) \bullet (\overline{WR}) = 1$.

1. Address setup before RD = 100 ns min
2. CS to RD = 0 min
3. Read strobe width = 950 ns min
4. Address hold after read = 50 ns min
5. Deselect time = 500 ns min

Write Operation

1. Address set up before WR = 100 ns min
2. CS to WR = 0 ns min
3. WR and data must be coincident for 950 ns min
4. Data hold after WR = 110 ns min
5. Address hold after WR = 50 ns min

If the ready output is used to guarantee read write operation, then the following recommendations are made. Referencing the April 1982 data sheet, during a read, the ready line makes its positive transition 100 nanoseconds before data is valid. (Not shown in the data sheet.) The user should not use this signal to latch data into an external latch. If this signal is used to wait state a microprocessor, then a critical examination of the microprocessor timing with respect to when it terminates its wait stated cycle must be made. This examination must also include any set-up time the processor needs prior to reading data. Also, note that the ready output (per the data sheet) negative-going-edge occurs 150 nanoseconds after the read or write strobe has gone low. Check microprocessor timing to ensure that the ready signal would be recognized as a "wait-signal".

It is not advised to perform sequential reading by connecting chip select and read low and cycling through the counters by changing address lines. The reason is that it is possible to cause an internal latch to "flip," the result being an error in timekeeping.

SOFTWARE CONSIDERATIONS

Reading the Counters

A read of one counter plus the rollover status bit or all the counters plus the rollover bit must be done within 800 microseconds. If the rollover status bit is a "1" then a complete read of counter(s) must be performed again. The 800 microsecond value is conservative. If the time between the read of any counter(s) and the rollover status bit exceeds 800 microseconds, then the status bit will always be set. The order of reading must be counter(s) first, then rollover status bit. This is because the positive going edge of the read strobe clears the status bit. Refer to *Figure 23.* The status bit is enabled for a period of 150 microsecond maximum at a rate of 1 kHz. If during this 150 microsecond period a counter(s) read occurs, the status bit will be set. This is true no matter how often the rollover status is read during that time period. Each rollover status read resets the status bit, but any counter read within the 150 microsecond period will set the rollover status bit. If the counters are read after a repetitive interrupt, then allow 150 microseconds (conservative) from the sense of the interrupt to the read of the counters (ripple delay time) and the data will be valid. If the counters are read after a compare interrupt, the read can occur immediately and will be valid.

Writing the Counters

The counters may be written to in any order, because the write overrides the internal increment. If it is desired to write all the counters without increments occurring in between writes, then the complete write operation must be performed within 800 microseconds. As long as valid BCD values (with respect to the specific counter) are written, no other counter is affected by the write. In general, writing the high order to low order counters is the conservative approach. This method is less susceptible to increments between writes for cases where the writing takes greater than 800 microseconds. For initialization of time, if the "GO" command is issued prior to any write, then 10 milliseconds are available to write from months through tenths and hundredths of seconds without any effect due to internal incrementing.

BIBLIOGRAPHY

MM58167A Microprocessor Real Time Clock Data Sheet April 1982.

"Crystal Oscillator Design And Temperature Compensation" By Marvin E. Frerking.

National Semiconductor Application Note AN-313 D.C. Electrical Characterization Of High Speed CMOS Logic.

LM-139 Quad Voltage Comparator Data Sheet.

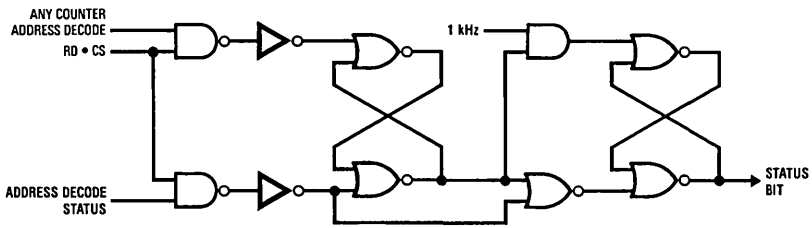

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FIGURE 21. Rollover Status Bit Logic

The MM58274C Adds Reliable Real-Time Keeping to Any Microprocessor System

National Semiconductor
Application Note 365
Peter K. Thomson

INTRODUCTION

When a Real-Time Clock (RTC) is to be added into a digital system, the designer will face a number of design constraints and problems that do not usually occur in normal systems. Attention to detail in both hardware and software design is necessary to ensure that a reliable and trouble free product is implemented.

The extra circuitry required for an RTC falls into three main groups: a precise oscillator to control real-time couting; a backup power source to maintain time-keeping when the main system power is removed; power failure detection and write protection circuitry. The MM58274C in common with most RTC devices uses an on-chip oscillator circuit and an external watch crystal (frequency 32.768 kHz) as the time reference. A battery is the usual source of backup power, along with circuitry to isolate the battery-backed clock from the rest of the system. Like any CMOS component, the RTC must be protected against data corruption when the main system power fails; a problem that is very often not fully appreciated.

Rather than dealing strictly with any one particular application, this applications note discusses all of the aspects involved in adding a reliable RTC function to a microprocessor system, with descriptions of suitable circuitry to achieve this. Hardware problems, component selection, and physical board layout are examined. The software examples given in the data sheet are explained and clarified, and some other software suggestions are presented. Finally a number of otherwise unrelated topics are lumped together under "Miscellany"; including a discussion on how the MM58274C may be used directly to upgrade an existing MM58174A installation.

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    - Alkaline
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APPENDIX A-1 Reading Valid Real-Time Data (Reprinted from the MM58274C Data Sheet)

APPENDIX A-2 MM58274C Functional Truth Tables

1.0 HARDWARE

Selecting the correct components for the job and implementing a good board layout is crucial to developing an accurate and reliable Real-Time Clock function. The range of component choices available is large and the suitability of different types depends on the demands of the system.

1.1 COMPONENT SELECTION

With reference to *Figure 1*, the oscillator components and the battery are examined and the suitability of different types is discussed.

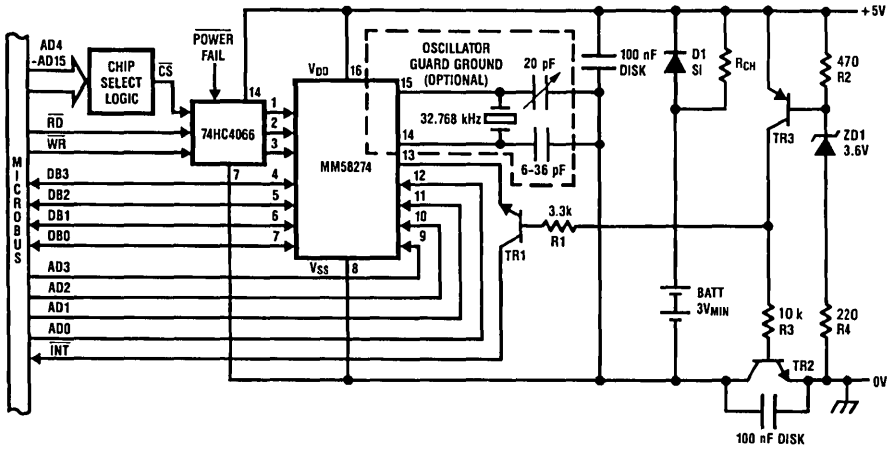

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FIGURE 1. MM58274C System Installation

1.1.1 Crystal

The oscillator is designed to work with a standard low power NT cut or XY Bar clock crystal of 32.768 kHz frequency. The circuit is a Pierce oscillator and is shown complete in *Figure 2*. The 20 MΩ resistor biases the oscillator into its linear region and ensures oscillator start-up. The 200 kΩ resistor prevents the oscillator amplifier from overdriving the crystal. If very low power crystals are used (i.e., less than 1 μW) an external resistor of around 200 kΩ may have to be added to reduce the drive to the crystal.

The oscillator will drive most normal watch crystals, with up to 20 μW drive available from the on-chip oscillator.

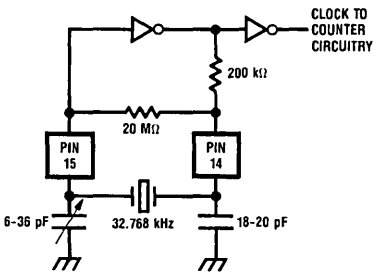

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FIGURE 2. Complete Oscillator Diagram

1.1.2 Loading Capacitors

Two capacitors are used to provide the correct output loading for the crystal. One is a fixed value capacitor in the range 18 pF–20 pF and the other is a variable 6 pF–36 pF trimmer capacitor. Adjusting the trimmer allows the crystal loading (and hence the oscillator frequency) to be fine tuned for optimal results.

The capacitors are the components most likely to affect the overall accuracy of the oscillator and care must be exercised in selection. Ceramic capacitors offer good operating temperature range with close tolerance and low temperature coefficients (typically ±3 ppm/K, for good quality examples). If trimming is undesirable a pair of close tolerance (±5% or better) capacitors in the range 18 pF–20 pF may be used. The average time-keeping accuracy for this configuration is within ±20 seconds per month.

1.1.3 Backup Battery

There are a number of different cell types available that can be used for time-keeping retention. Some cells are more suitable than others, and the way in which the system is used also influences the choice of cell. Ideally the standby voltage of the RTC should be kept as low as possible, as the supply current increases with increasing voltage *(Figure 3)*. Four different power sources are discussed: capacitors, nickel-cadmium rechargeable cells, alkaline and lithium primary cells.

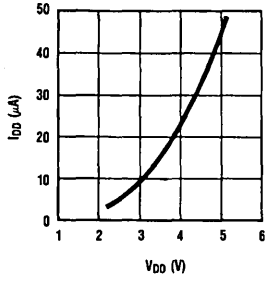

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FIGURE 3. Typical I_{DD} (μA) vs V_{DD} (V) for MM58274C in Standby Mode (T_A = 25°C)

Capacitors

When the system is permanently powered, and any long term removal of system power (i.e., more than a few hours) requires complete restarting, then a 1–2 Farad capacitor may be sufficient to run the clock during the power down. This can keep the clock running for 48–72 hours.

Nickel-Cadmium Cells

Nickel-cadmium (Ni-Cad) cells can be trickle-charged from the system power supply using a resistor as shown in *Figure 1*. The exact value of resistor used depends on the capacity and number of cells in the battery. Consult the manufacturers data for information on charging rates and times.

A 3- or 4-cell battery should be used to power the clock (the nominal battery voltages are 3.6V for 3 cells in series and 4.8V for 4 cells), with 3 cells preferable. PCB mounting batteries of 100 mAh capacity are available and these will give around 6 months data retention (at normal room temperature). For this cell type to be used the system must spend a large proportion of its time turned on to keep the battery charged (i.e., used daily).

Alkaline

Alkaline cells are among the least expensive primary cells which are suitable for use in real-time clock applications. They are available in a large range of capacities and shapes and have a very good storage (shelf) life.

Two cells in series will provide a nominal 3V, which is adequate to power the clock (via the isolating diode). The main problem with the alkaline system is that the cell terminal voltage drops slowly over the life of the cell. When the voltage at the clock supply pin drops to 2.2V, the cells must be replaced (battery voltage around 2.6V–2.7V). With present alkaline cells, this point is usually reached when the cells are only ½ to ⅔ discharged.

Provisions must be made either to check the battery voltage at regular intervals or to replace the cells regularly enough to avoid the danger of using discharged cells. Once again the manufacturers data regarding capacity and cell voltage against time must be examined to determine a suitable cell selection. A good alkaline system will supply 1–2 years continuous time-keeping.

Lithium

Lithium cells are the most suitable for real-time clock applications. A single cell with 3V potential is sufficient to power the system. The cell potential is very stable over use and the storage life is excellent. The energy density of lithium cells is very high, giving enough capacity in a physically small cell to power the clock continuously for at least 5 years (at room temperature using a 1,000 mAh cell).

Several cells which are recommended for RTC use are D2/3A*, D2A*, and 1/6DEL/P*. Each have 1,000 mAh capacity. These cells are available with solder pin connections for PCB mounting, giving a reliable backup supply.

Other Cells and Notes

There are many other types of cells, both primary and secondary, which may be adapted for RTC use. When selecting a cell type, attention must be paid to:

a. Cell capacity and physical size.
b. Storage (shelf) life.
c. Voltage variation over use.
d. Operating temperature range.
e. The method of battery connection and mounting.

In general, soldered cells are preferable to connector mounted cells. With replaceable batteries, the battery and connector contacts must be kept thoroughly clean. Dirty or corroded contacts can cause the clock to be starved of power, giving erratic and unreliable performance. The ease of operator access for cell replacement should also be considered.

Temperature Range

The performance of any cell will be satisfactory for most office or domestic environments. When "ruggedized" equipment is to be used (i.e., field portable equipment, automotive, etc.) the temperature specification of different cell types should be taken into account when selecting a cell. Lithium cells offer good performance over 0°C–70°C with little loss in capacity. Once again, the manufacturer's data should be examined to determine suitability, especially since different cells of the same type can have markedly different characteristics.

Few types of cells will offer any useful capacity at temperatures in or below the range 0°C–10°C, and fewer still will operate over the full military temperature range (−55°C to +125°C). Solid lithium cells and mercury-cadmium cells are two systems which can cover this range.

1.2 BOARD LAYOUT

1.2.1 Oscillator Connection

The oscillator components must be built as close to the pins of the clock chip as is physically possible. The ideal configuration is shown in *Figure 4*. From *Figure 2*, the oscillator circuit, it can be seen that both Osc In and Osc Out are high impedance nodes, susceptible to noise coupling from adjacent lines. Hence the oscillator should, as far as is practicable, be surrounded by a guard ground. The absolute maximum length of PCB tracking on either pin is 2.5 cm (1 inch). Longer tracks increase the parasitic track to track capacitances, increasing the risk of noise coupling and hence reducing the overall oscillator stability.

Where the system operates in humid or very cold environments (below 5°C), condensation or ice may form on the PCB. This has the effect of adding parasitic resistances and capacitances between pins 14 and 15, and also to ground. This variation in loading adversely affects the stability of the oscillator and in extreme cases may cause the oscillator to stop.

*Duracell Trade Number.
**Tadiran Trade Number.

Keeping the PCB tracks as short as possible will help to minimize the problem, and on its own this may be sufficient. Where the operating conditions are particularly severe, the PCB and oscillator components should be coated with a suitable water repellent material, such as lacquer or silicon grease (suitability being determined by the electrical properties of the materials—high impedance and low dielectric constant).

Figures 2 and *4* show the trimmer placed on Osc Out. The placement of the trimmer capacitor on either Osc In or Osc Out is not critical. Placing the trimmer on Osc Out yields a smaller trim range, but less susceptibility to changes in trimmer capacitance. Placement of the trimmer capacitor on Osc In gives a wider trim span, but slightly greater susceptibility to capacitance changes.

1.2.2 Battery Placement

For the battery, placement is less critical than with the oscillator components. Practical considerations are of greater importance now; i.e., accessibility. The battery should be placed where it is unlikely to be accidentally shorted or disconnected during routine operation and servicing of the equipment.

When replaceable cells are used, connecting a 100 μF capacitor across the RTC supply lines will keep the clock operating for 30–40 seconds with the battery disconnected *(Figure 5)*. This allows the battery to be replaced regardless of whether or not the main supply is active.

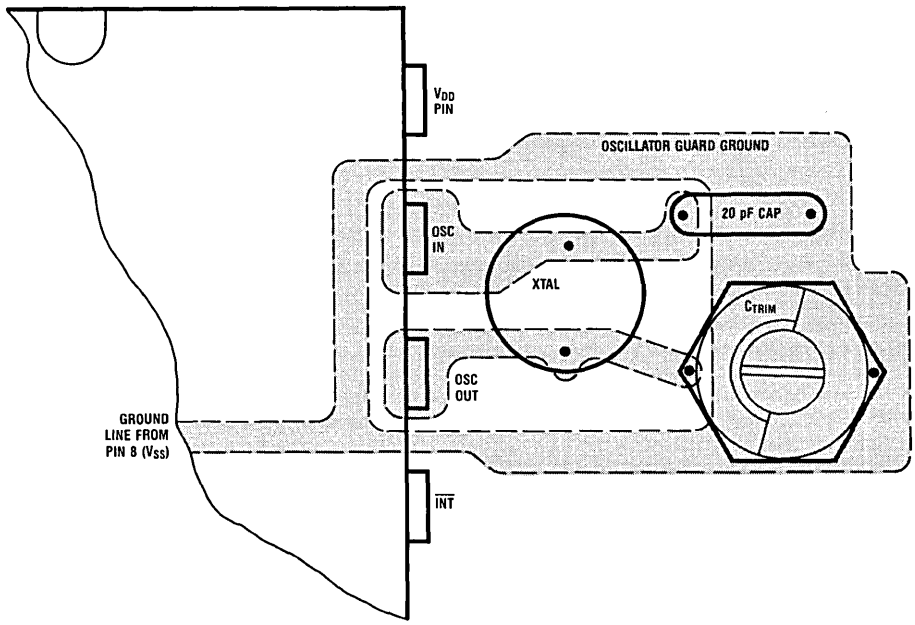

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FIGURE 4. Oscillator Board Layout

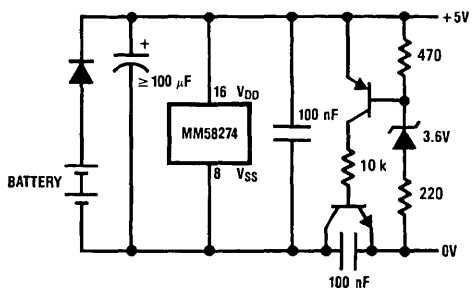

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FIGURE 5. Simplified Power Supply Diagram with 100 μF Capacitor Added

1.2.3 Other Components

The placement of the other RTC dedicated components (e.g., supply disconnection and power failure protection components) is not particularly critical. However, the same guidelines as applied to the battery should be followed when the PCB layout is designed.

1.3 POWER SUPPLY ISOLATION SCHEMES

1.3.1 The Need for Isolation

There are two reasons for disconnecting the clock circuit from the rest of the system:

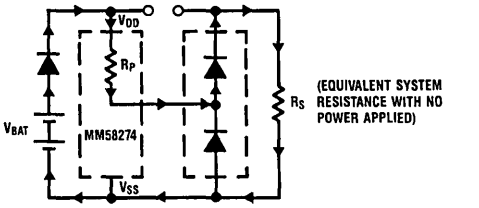
1. To prevent the backup battery from trying to power the whole system when the main power fails.
2. To minimize the battery current (and extend battery life) by preventing current leakage out of the RTC input pins.

The MM58274C inputs have internal pull-up devices which pull the inputs to V_{DD} in power down mode. This turns off the internal TTL input buffers and causes the μP interface functions of the clock to go to full CMOS logic levels, drawing no supply current (except for the unavoidable leakage current of the internal MOS transistors). For the MM58274C this is achieved by isolating the ground (V_{SS}) supply line from the rest of the system.

Figures 6a and *6b* show the two cases where first V_{DD} *(6a)* and then V_{SS} *(6b)* are open-circuited. The line out from the MM58274C represents any of the Control, Address, or Data lines on the RTC, with the internal pull-up resistor shown. The two diodes and resistor R_S represent the logic device connected to the RTC input and the resistance of the rest of the system with no power applied.

When V_{DD} is open-circuit as in *Figure 6a*, there is a complete current path, shown by the arrows, out of the RTC input and through the external circuitry. This battery current is a complete waste and serves only to reduce the cell life. Depending on the value of R_S, the voltage level at the pin may fall low enough to turn on the internal TTL level buffer, wasting further current as the buffer is no longer fully CMOS.

With V_{SS} disconnected *(Figure 6b)*, there is no return path to the battery and the pin is pulled completely up to V_{DD}. The TTL buffer is switched off and no power is lost.



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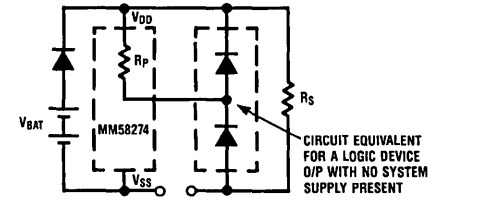
a) V_{DD} Disconnection



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b) V_{SS} Disconnection

FIGURE 6. Current Leakage Prevention by Proper Supply Disconnection

1.3.2 Isolation Techniques I—5V Supply Only

Figure 7 shows the isolation circuit suggested in the MM58274C data sheet. This circuit provides complete disconnection where only the system +5V is available for switching control.

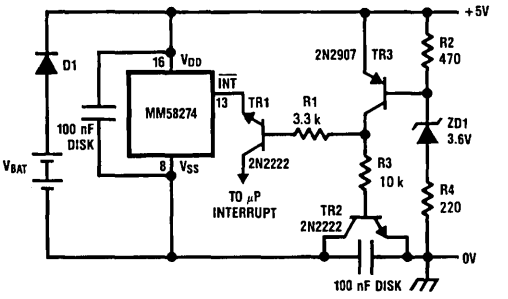

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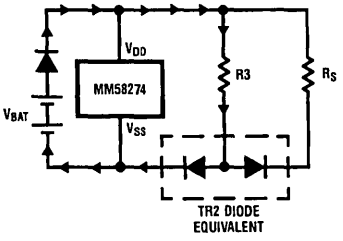
FIGURE 7. 5V Isolation Circuit

TR2 is the disconnecting device, which is controlled by TR3 and its associated circuitry. TR3 is turned on by its bias chain R2, ZD1, R4 as the system supply rises up to 4.2V. TR3 and R3 then turn on TR2 to connect the clock to the system supply. D1 isolates the backup battery when the system supply is active. The 100 nF disk capacitors decouple the supply during R/W operations and should be included in any disconnection scheme.

TR3 is necessary to prevent R3 and TR2 from leaking battery current in the power down condition. The circuit without TR3 is shown in *Figure 8* where TR2 has been replaced by equivalent diodes to clearly show the problem. The circuitry could be simplified by replacing TR3 with a Zener diode *(Figure 9)*. There will be a small loss of current down through TR2 however, as the Zener will pass a small leakage current at below its "knee" voltage. Thus the Zener should be selected for its low current capability.



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R_S = System Resistance with No Power Applied

FIGURE 8. Current Leakage in Simplified Disconnection Schemes

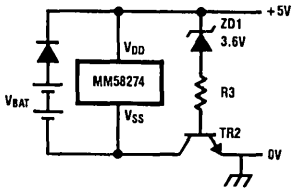

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FIGURE 9. Alternative Supply Disconnection Scheme Sensing 5V (Decoupling Capacitors Omitted for Clarity)

Finally TR1 and R1 *(Figure 7)* are optional components which are only required when the interrupt output is used. If interrupts are left programmed when the power fails, the interrupt timer will still time-out setting the interrupt output. Since this is an active low pull-down transistor it effectively shorts directly across TR2, destroying the RTC isolation and discharging the battery into the rest of the system *(Figure 10)*. In order to prevent this from occurring, TR1 and R1 are added.

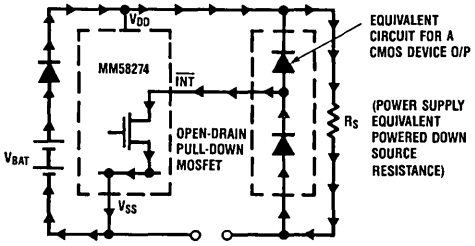

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FIGURE 10. Battery Discharge Path via Unisolated Interrupt Output

None of the disconnection components are at all critical, with general purpose transistors being completely adequate for the task. D1 should be a small-signal silicon or germanium diode.

1.3.3 Isolation Techniques II— Negative Supply Switched

Where a negative voltage supply is available (either regulated or unregulated) the circuit of *Figure 11* may be used. This is similar in operation to its diode equivalent shown in *Figure 12*, where the voltage drops across the diodes provide the correct potential to the clock. *Figure 11* has the advantage, however, that the clock power is supplied from the ground line by transistor action, rather than via the resistor as in *Figure 12*. Less lower is dissipated in the resistor as only transistor bias current need be drawn.

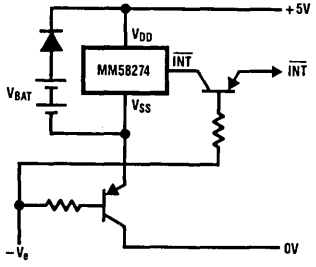

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FIGURE 11. Negative Voltage Driven Supply Disconnection Scheme (Decoupling Capacitors Omitted for Clarity)

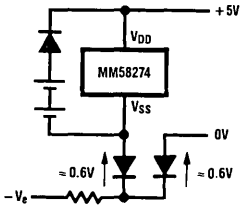

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FIGURE 12. Diode Equivalent Circuit of *Figure 11*

1.3.4 Other Methods

There are many other possibilities for supply disconnection schemes, i.e., relay disconnection. When designing a disconnection scheme, the performance must be analyzed both with the system power applied and with system power absent. Check for leakage paths and undue voltage drops and try to set up so that disconnection and reconnection will take place as near to the backup voltage as possible.

1.4 POWER FAIL PROTECTION

One of the major causes of unreliability in RTC designs is due to inadequate power failure protection. As the system is powered up and down, the μP and surrounding logic can produce numerous spurious signals, including spurious writes and illegal control signals (i.e., RD and WR both active together).

Bipolar logic devices can produce spikes and glitches as the internal biasing switches off around 3V–3.5V, and the transistors operate in their linear region for a short time. Any such spurious signals, if applied to the RTC, could cause the time data to be corrupted. Systems using 74HC logic and CMOS processors are less stringent in their power failure requirements as the devices tend to work right down to around 2V. Some form of write protection is still required, however.

In order to protect the time data, the system must be physically prevented from writing to the clock when the power supply is not stable. The ideal situation is to ban Write access to the clock before the system +5V starts to fail, and then keep the chip "locked-out" until the power is restored and stabilized. This ideal access control signal is illustrated in *Figure 13*.

Three methods of power fail protection are discussed, although there are also many other possibilities.

1.4.1 Write Protect Switch

By far the simplest and potentially the most hazard-free method is to use a switch on the WR control line to the clock *(Figure 14)*. This is completely adequate, but requires the intervention of an operator to alter time data or program interrupts.

Some thought must be given to ensuring that the operator cannot accidentally leave the WR line switched in. This may be achieved by the physical access method used (i.e., the machine is impossible to operate or switch off when in the time setting mode, because of the placement of access hatches, etc.) or with software. The switch state could be sensed by trying to alter the data in the Tens of Years counter or Interrupt register just prior to leaving the clock setting routine, and refusing to leave the routine until the WR switch has been opened. The switch condition should similarly be checked whenever the system is initialized or reset.

The physical location of the switch should also be considered for ease of accessibility. How easy the switch is to reach will depend on the system; i.e., in some cases a "tamper proof" clock may be required.

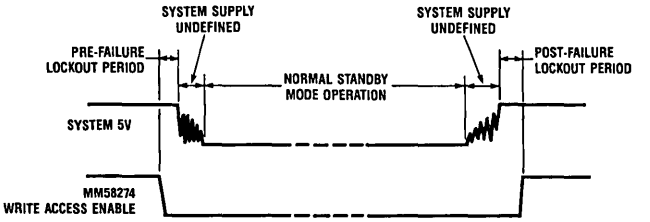

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FIGURE 13. RTC Access Lockout Definition

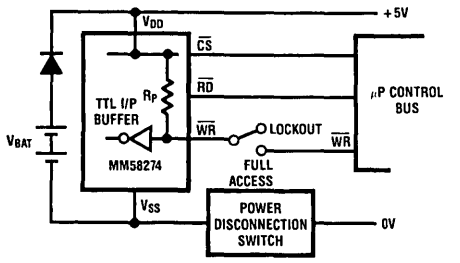

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FIGURE 14. Write Protection by Manually Switching WR

1.4.2 5V Sensing

The circuit of *Figure 15* senses the system 5V supply and prevents access to the clock if the supply falls below 4.2V–4.3V. This circuit should be used where only the system 5V is available for reference. The LM139 comparator and associated components sense the 5V supply and generate the power fail signal (P.Fail). The 74HC75 and components disconnect the WR line.

R3 and ZD1 provide a reference voltage of 2V–3V for the comparator. R4 and VR1 form a potential divider chain sensing the 5V line, and VR1 is adjusted to switch the comparator output at 4.2V–4.3V. An alternative to VR1 would be to use a pair of close tolerance resistors (±2%) with values selected to suit the Zener diode reference used. The combination of R4, D3 and C2 provide an RC time constant to delay the comparator when sensing the return of 5V (to provide the post-failure delay in *Figure 13*). The LM139 has an open-collector output which is held low when 5V is present and is switched off when 5V fails. This line is pulled high by R5 to flag power failure (P.Fail). Since the comparator is a linear device drawing a bias current, it is powered by the system 5V supply to avoid consuming battery power.

One 74HC75 package contains four latches, of which two are used. These are transparent latches controlled by the "G" input. With G high, the latch is transparent and the Q and $\overline{Q}$ outputs follow the Data input. When G is low, the state of Q and $\overline{Q}$ on the falling edge is latched. In this way, F2 prevents P.Fail from locking out the clock if there is a Write cycle in progress. F1 isolates the WR input on the clock when F2 passes the P.Fail signal. C1, R2 and D1 do not slow the advent of P.Fail, but they cause a delay in the release of the function to mask any comparator noise or oscillation as the comparator switches off or on (i.e., during the undefined supply periods).

D2, C3 and R6 smooth the comparator supply and help it to function effectively. The time constants of the RC networks should be selected to suit the power supply of the system that is used. Comparing the functioning of this circuit with the ideal case of *Figure 13* shows that most of the conditions can be satisfied, except that there is no real pre-failure lock-out period. This cannot be achieved without some form of look ahead power failure.

As an alternative to F1 a permanently powered 74HC4066 analog switch could be used as the isolating component *(Figure 16)*. The 74HC4066 does not require pull-up resistors on its inputs as there are no internal CMOS buffers inside this device which must be controlled. The resistor on the WR line is for the benefit of the 74HC75.

Note that both of the devices mentioned must be permanently powered from the battery to be useful in this way. Unused gates in any such device must *NOT* be used in combinational logic that is not permanently powered. All unused inputs should be tied to V_{DD} or V_{SS} to render them inactive.

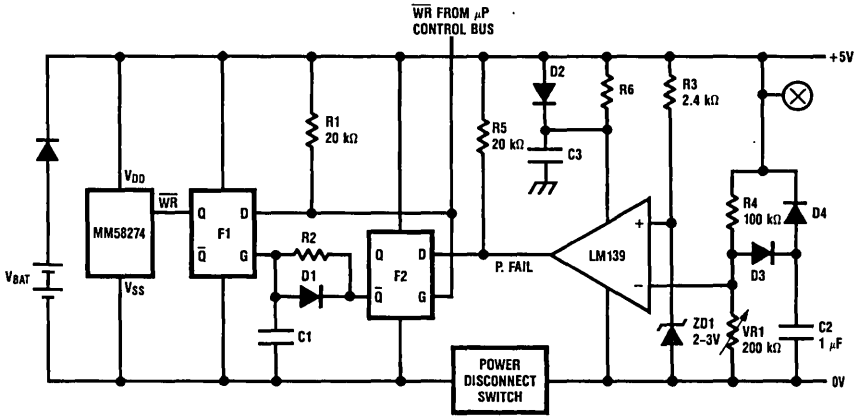

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FIGURE 15. Power Supply Failure Detection and Write Protection Circuitry

1.4.3 Supply Pre-Sense

The same circuit of *Figure 15* can be used with unregulated supplies or other voltage lines which will fail before the 5V line. To achieve this, point X is connected to the sensed voltage instead of 5V, and the R4/VR1 ratio is adjusted to suit. The major benefit here is that advance warning of an impending 5V failure can be detected, allowing a pre-failure lockout signal to be generated.

Less precision is required to sense the unregulated supply than the system 5V supply. Consequently less complex circuitry can be used to do the detection and this is reflected in the circuit of *Figure 17*. Most 5V regulators will operate with an input voltage from 7V to 25V. Typically the input voltage is around 9V to 12V, giving some headroom. In *Figure 17* this voltage is high enough to drive a current through the Zener diode and turn on transistor TR1, holding P.Fail low. R_{LIM} limits the Zener current. The Zener voltage is selected to switch off before the regulator fails, around 7.5V–8.5V depending on the time constant of the supply. With no current, TR1 switches off and R_P pulls P.Fail high.

When power is re-applied the 5V supply will stabilize before the Zener switches on, removing P.Fail. To provide a longer post-failure lockout period R_{LIM} could be replaced with two resistors and a diode/capacitor delay as in *Figure 15*.

Figure 18 is another extension of the same basic idea to provide an advance interrupt signal to allow μP housekeeping before the RTC (and CMOS RAM) is locked out. The extra rectifying components D1, C_t and R_t keep $\overline{NMI}$ off as long as input power is present. Time constant τ_2 is selected to be at 2–3 times faster than τ_1, the supply time constant. The interrupt signal is thus asserted before P.Fail.

1.4.4 Switching Power Supplies

Switching power supplies are available which generate power failure signals. This signal may be adequate for direct use as a P.Fail line, but the manufacturer's information should be consulted to determine the suitability of a given power unit. P.Fail must still be gated with the Write signal for the clock, regardless of the actual detection method employed.

1.4.5 Summary

The general guidelines for power fail protection are:

1. Physically isolate the WR input to the clock. The μP cannot be relied upon to logically operate the isolation mechanism.
2. The clock should be isolated before the 5V power line starts to fail, and stay isolated until after it has reestablished.
3. Consider the action of the sensing and protection circuitry if the supplies oscillate or if a momentary glitch occurs.
4. The Power Fail signal must be gated with Write strobes to the RTC. A foreshortened Write may also cause data corruption.
5. Logic components (and ICs in general) should be avoided when designing power failure schemes. Discrete components are far more predictable in their performance when the power supplies are not well defined. The exception to this general rule is when using permanently powered HCMOS logic devices. They will function in a reliable manner down to 2V.

System-powered logic devices cannot be relied on for power failure or Write isolation (not even CMOS).

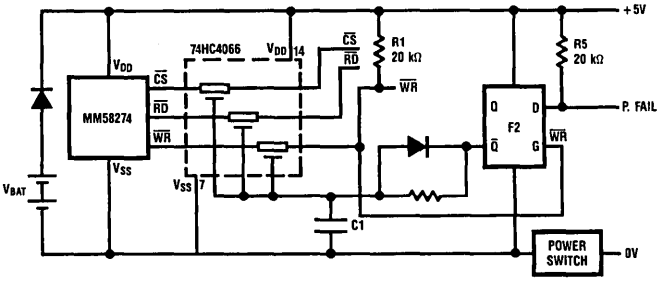

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FIGURE 16. F1 Replaced by a 74HC4066 Analog Switch (Pull-Up Resistors Not Required on $\overline{CS}$ or $\overline{RD}$ Inputs)

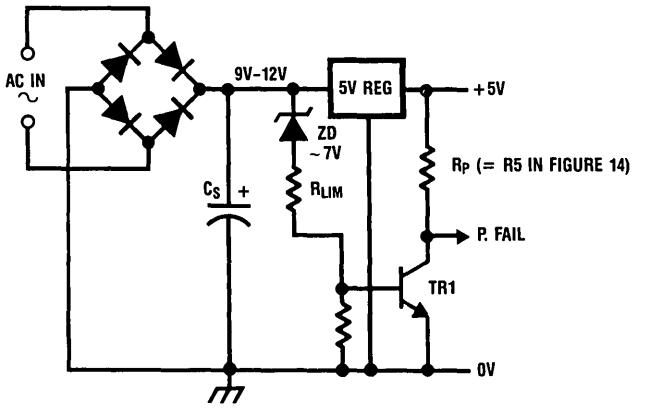

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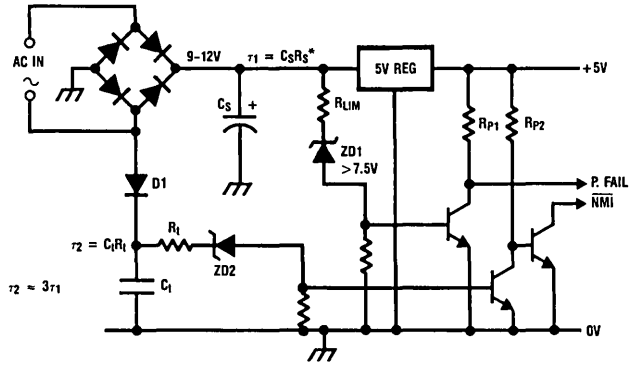
FIGURE 17. Power Fail Signal Generation from Unregulated Supplies



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*R_S = Equivalent Resistance of the System.

FIGURE 18. Power Fail Circuit with μP Housekeeping Interrupt

2.0 SOFTWARE

2.1 DATA VALIDATION

The MM58274C data sheet describes in some detail three different methods of reading the clock and validating the real-time data. These techniques are reproduced in Appendix A-1. Rather than repeating the data sheet examples, this applications note examines the principles that lie behind the techniques suggested.

The basic problem is that the μP must somehow be synchronized with the changes in real-time in order to read valid data. This synchronization can either be done prior to reading the time data (pre-read), or after reading the data (post-read synchronization).

2.1.1 Post-Read Synchronization

Using the Data-Changed Flag (DCF) or the lowest order time register as outlined in the appendix: Time Reading using DCF and Time Reading with very slow Read cycles; are both examples of post-read synchronization.

What this means is that the data is read out first, and then verified. This is achieved by defining a random time-slot, started by the first DCF or low order register read, and ended by the second such read. If DCF has not been set during the time-slot or the lowest order register has not changed, then no real-time change occurred during that time-slot. All real-time reads during the time-slot are thus guaranteed.

2.1.2 Pre-Read Synchronization

The Interrupt Timer technique uses pre-read synchronization. Once it has been initialized as described, the interrupt timer times out just after the real-time data has changed. Thus the μP is guaranteed a full 100 ms period in which to read the time counters before the next change occurs.

The interrupt timer has to be synchronized with the real-time counters because it is an independent unit which may be started and stopped at any time by the μP. This software synchronization is achieved by using another pre-read technique. The timer is set up and ready to go, but then the μP waits for DCF to occur before issuing the start command. The same technique could be used to actually read the time-data, but post-read synchronization is faster.

2.2 INTERRUPT AS A "DATA-CHANGED" FLAG

DCF is set every 100 ms when the 1/10ths of seconds counter is changed. When the time is only being read to the nearest second or minute, it would be useful to have a flag which is only set by a change in the lowest order counter being used.

If the interrupt output from the clock is not being used, the timer can be used as a programmable data-changed flag. To achieve this, the timer is set up and started in exactly the same way as described for interrupt time reading (Appendix A-1). The interrupt output, however, should be left unconnected. When reading the real-time data, the technique used is the same as for the normal Data-Changed Flag except that the Interrupt Flag is tested instead of DCF.

Note that the lowest order real-time register which is to be read out should be used to initially synchronize the counter. The interrupt timer is started when the real-time counter value is seen to change.

2.3 WRITING WITHOUT HALTING TIME-KEEPING

For most purposes the RTC should be halted when the time is being set, especially if large numbers of counters are being updated. The clock can also then be re-started in synchronism with an external time reference. If only a few counters are to be altered and the clock is already synchronized, then this can be done without stopping the clock. An example of a minor change which may be undertaken in this way is daylight savings (winter/summer change of hour).

The problem to be overcome when writing in this way is that the write strobe may coincide with a time change pulse. As the time counters are synchronous, the 100 ms clock pulse is fed to each one. Writing to one counter may cause a spurious carry to be generated from that counter, causing the next one up the chain to be incremented.

Since a spurious carry will only affect the next counter if it coincides with a time update pulse, the solution is once again to synchronize clock access with the real-time change. The most suitable method for this is pre-read synchronization. In other words, the μP must wait for DCF to be set before starting to write data to the clock, giving a guaranteed 100 ms period for writing.

2.4 THE CLOCK AS A μP WATCHDOG

The interrupt timer can be used as a μP watchdog circuit, operating on a non-maskable interrupt input to the μP. The timer is set up in either single or repeat interrupt mode for the watchdog period required: 0.1s, 0.5s or 1 second are probably the most useful times for this. Synchronization with real-time is not required.

In the main program loop the μP writes to the clock, stopping and then re-starting the interrupt timer. The timer period selected will depend on how long the main loop takes to execute. As long as the μP continues to execute the loop, no time-outs occur and no interrupts are generated. If the μP fails for some reason to reset the timer, it eventually times out, generating the initializing interrupt to restore operations.

2.5 THE JAPANESE CALENDAR

Because the MM58274C has a programmable leap year counter, this allows the possibility of programming for the Japanese Showa calendar. The Japanese calender counts years from the time that the present Japanese Emperor comes to power.

The normal procedure for the MM58274C is to program "the number of years since last leap year." This remains the same whether the clock is loaded with the Gregorian or Showa year. When software is used to calculate the leap year count value from the year, then the formula used must be modified.

The formula for the Gregorian year is:

Leap Year Value = [Gregorian Year/4] REMAINDER

Whereas for the Showa year the formula is:

Leap Year Value = [(Showa Year + 1)/4] REMAINDER

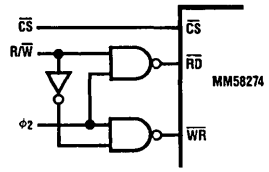
Leap Year Value is the number from 0 to 3 which is written into the leap year counter, and is the REMAINDER of the integer calculations shown above.

3.0 MISCELLANY

3.1 CONNECTION TO NON Microbus™ SYSTEMS

Adding the MM58274C to non Microbus processors is made fairly straightforward because of the flexibility of the control signal timing. *Figure 19* shows two examples of logic to connect to clock to a 6502/6800 microprocessor bus.

Figure 19a the $\overline{RD}$ and $\overline{WR}$ inputs are strobed, generating reasonably typical Microbus type control signals. In *Figure 19b*, CS is used as the strobe signal. There is no particular advantage to either circuit, they are just variations on the same theme. This circuit flexibility may be used to advantage to save SSI packages in the board design.



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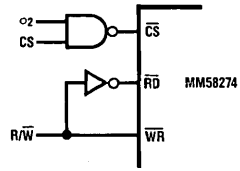
a)



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b)

FIGURE 19. 6800/6502 μP Bus Interface

3.2 TEST MODE

Test Mode is used by National Semiconductor when the MM58274C is tested during manufacture. It enables the real-time counters to be clocked rapidly through their full count sequence.

The MM58274C counters are clocked synchronously to simplify μP access, with ripple carry signals from each counter to the next. In Test Mode some of these carries are intercepted and permanently asserted causing the counters to count each clock pulse. The prescaler is also bypassed so that the counters count every clock applied to the Osc In pin. The Test Mode counter connection is shown in *Figure 20*.

If Test Mode is to be used for incoming inspection or device verification, then the clock waveform of *Figure 21* should be applied to the oscillator input (Osc In, pin 15). The MM58274C uses semi-dynamic flip-flops in the counters which are only fully static when the oscillator input is high. Thus *Figure 21* shows that the oscillator waveform is normally high, pulsing low to clock the real-time counters. The time data in the counters changes on the rising edge of Osc In.

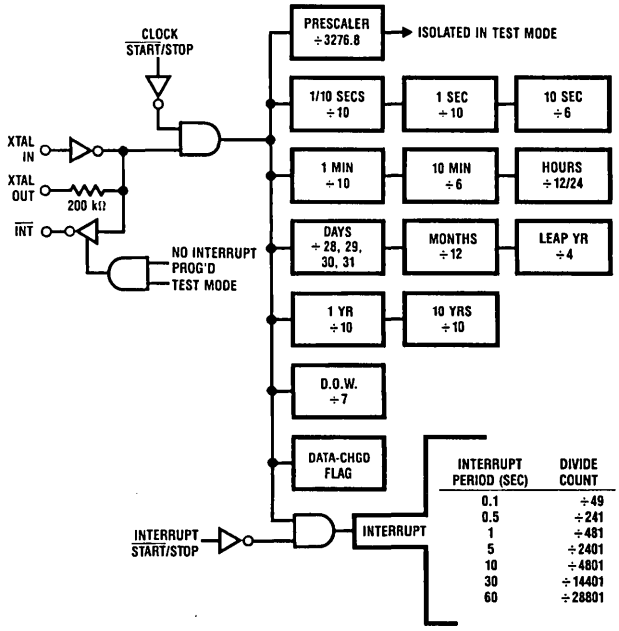

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FIGURE 20. Test Mode Interconnection Diagram of Internal Counter Stages

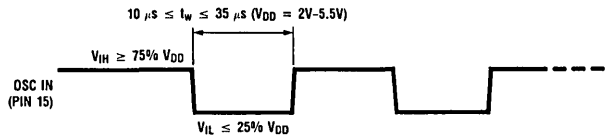

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FIGURE 21. Oscillator Waveform for Counter Clocking in Test Mode

The pulse width limits for reliable clocking are shown on the diagram. When running with a 32 kHz crystal, the normal pulse width is 15.26 μs. With no forcing input, the oscillator will self bias to around 2.5V (V_{DD} = 5V). While a few hundred mV swing above and below this level is sufficient to drive the oscillator, for guaranteed test clocking the input should swing between $V_{IH} \geq 75\%\ V_{DD}$ and $V_{IL} \leq 25\%\ V_{DD}$.

3.3 TEST MODE AND OSCILLATOR SETTING

When Test Mode is used to set the oscillator frequency, the interrupt timer must be disabled (interrupt register programmed with all 0s) for the oscillator frequency to appear on the interrupt output. No test equipment should be connected directly to either oscillator pin, as the added loading will alter the characteristics of the oscillator making precise tuning impossible.

Note that oscillator frequency will vary slightly as the supply varies between operating and standby voltages. Typically this variation will be around ±6 seconds per month ($V_{STANDBY}$ = 2.4V), slowing at standby voltage. When the clock will spend the greater part of its working life in standby mode, it may prove worthwhile to correct for this in the tuning. This can be done by tuning at standby voltage (by writing the RTC into test mode, then disconnecting it from the system to tune on battery backup). Alternatively, the clock can be slightly overtuned at operational voltage, tuning to 32.7681 kHz.

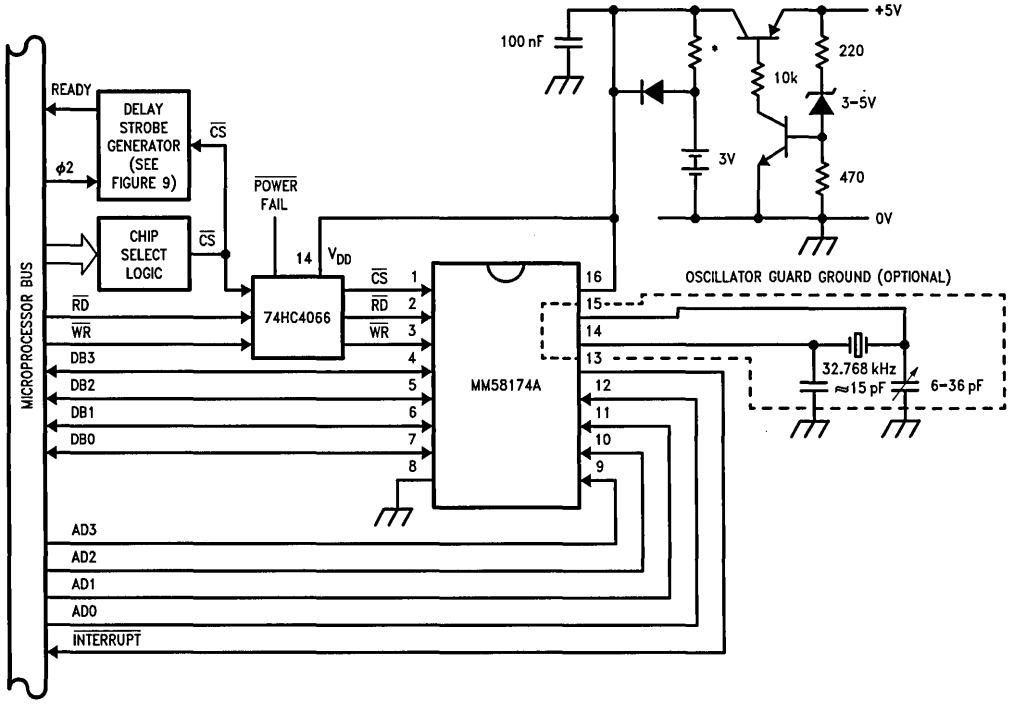
In a similar way, where the RTC spends equal amounts of time in both operational and standby modes (i.e., powered by day, standby at night), the oscillator may be tuned somewhere between the two conditions. Following these tuning suggestions will not eliminate time-keeping errors, but they will help in minimizing them.

Time-keeping accuracy cannot be exactly specified. It depends on the quality of the components used in the oscillator circuit and their physical layout, also the stability of the supply voltage, the variations in ambient temperture, etc. With good components and a reasonably stable environment however, time-keeping accuracy to within 4 seconds/month can be achieved, although 8 seconds/month is somewhat more typical in practical systems.

3.4 UPGRADING AN MM58174A SYSTEM WITH THE MM58274C

The MM58274C has the same pin-out as the MM58174A and can be used as a direct replacement, with certain reservations. The two devices are not quite the same in their external circuit appearances, and this is reflected in their applications circuits. In addition, the MM58274C is not software compatible with the MM58174A, requiring a change in the operating system to use the MM58274C.

Figure 22 shows the circuit diagram for the MM58174A system connection. There are two major differences between this and the MM58274C diagram *(Figure 1);* a) the oscillator circuit and b) the supply disconnection scheme.



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*Use resistor with Ni-Cad cells only.

FIGURE 22. MM58174A System Installation

a) The Oscillator Circuit

The MM58274C normally operates with an 18 pF–20 pF fixed loading capacitor as opposed to the 15 pF of the MM58174A. This is a reflection of the greater internal capacitance of the MM58174A, rather than any change in the characteristics of the oscillator itself. The MM58274C will operate using a 15 pF capacitor, but the oscillator will probably need to be retrimmed.

Operating with a 15 pF capacitor will make the oscillator more sensitive to change in the environment, i.e., temperature, voltage, moisture, etc. This will result in lower accuracy in time-keeping. The oscillator is more prone to stopping at low voltage. Oscillation would normally be maintained down to 1.8V–1.9V (although not guaranteed); with a 15 pF load it may only oscillate down to 2.0V–2.1V. It is thus important to check the battery regularly and replace it before the RTC voltage falls below 2.2V.

Where possible the 15 pF capacitor should be replaced by an 18 pF–20 pF capacitor (anywhere in the range 18 pF–20 pF is adequate), or a second 3 pF–5 pF capacitor may be added in parallel with the 15 pF.

Note: When components have been soldered into the oscillator circuit, allow the circuit to cool to room temperature before attempting to retune the oscillator.

The change of pin of the tuning capacitor (from OSC Out to Osc In) is not critical.

b) The Supply Disconnection Scheme

The MM58174A uses mostly pull-down devices on its μP inputs to pull the inputs to CMOS levels, and so the 5V power line is disconnected on this device. The two exceptions to this are the $\overline{CS}$ and $\overline{WR}$ inputs which have pull-up resistors to inactivate the internal write strobe. As *Figure 5a* shows, there is a leakage path through these pins, which in most MM58174A installations are individually isolated.

The largest penalty in inserting an MM58274C into an MM58174A circuit is the battery current that is lost through the pull-up devices. This will increase the typical supply current from 4 μA to 50–100 μA and it is up to the individual user to decide whether or not this drain is tolerable in a particular application.

The most important requirement is that the $\overline{WR}$ input should be electrically isolated or current leakage through pin inputs may force the inputs low enough to cause spurious writes to occur. Since it is already customary to isolate these inputs for the MM58174A, this may not be a problem. Where this has not been done, either the circuit will have to be modified or the $\overline{WR}$ PCB track can be cut and a switch or some extra circuitry added to allow isolation.

Note that power fail disconnection and input isolation may be achieved using the same components. In *Figure 22* the MM74HC4066 analog switch will do both jobs.

The current drained by the input pull-ups may be minimized with some attention to the data/address driving devices. It is often possible to replace LSTTL devices with standard 7400 series devices and reduce the leakage (at the cost of some increase in operating current). Many 7400 series device outputs lack diodes in the right places to pass leakage currents. LSTTL devices will, for the main part, have these diodes. CMOS devices will always have diodes to both power rails on inputs and outputs.

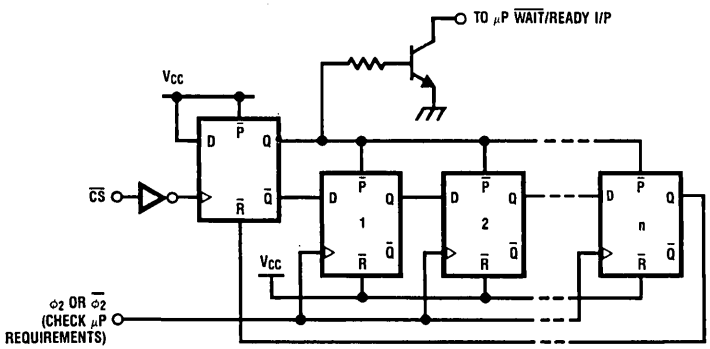
There is no hard and fast rule for this. Where devices from one manufacturer work, the same part from a different one may not. Some trial and error experimentation may prove worthwhile in selected devices.

3.5 WAIT STATE GENERATION FOR FAST μPs

Although the MM58274C has faster access times than the MM58174A, in many cases, the μP will be too fast to directly access the RTC. *Figure 23* shows a circuit which will produce wait states of any length required to enable the RTC to be accessed, using the 74HC74 dual D-type flip-flop.

The RTC $\overline{CS}$ signal clocks up a logic 1 on the Q output of the first F/F, removing the Preset from all the other F/Fs and pulling the μP WAIT line low, via the transistor. The other F/Fs 1 to n, form a shift register clocked by the ϕ_2 system clock.

After n ϕ_2 clocks (where n is the number of flip-flops in the shift register) a logic 0 shifts out from the nth F/F, resetting the main flip-flop. The main F/F then presets the shift register and clears the WAIT signal, ready for the next $\overline{CS}$ edge to repeat the cycle. On power-up the delay generator will initialize itself after a maximium of n system clocks have occurred so no reset signal is required. Some μPs demand that a $\overline{WAIT}$/READY input is synchronized with ϕ_2 of the system clock. This can readily be achieved by selecting the correct ϕ_2 edge as the clock signal for the shift register chain.



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Flip-Flop—MM74HC74 D-Type Latch

FIGURE 23. Access Delay Generator (Clocked Wait State Generator)

APPENDIX A-1. READING VALID REAL-TIME DATA

TIME READING USING DCF

Using the Data-Changed Flag (DCF) technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1. Read the control register, address 0: *This is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.*
2. Read time registers: *All desired time registers are read out in a block.*
3. Read the control register and test DCF: *If DCF is still clear (logic 0), then no clock setting pulses have occurred since step 1. All time data is guaranteed good and time reading is complete.*

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may not be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

TIME READING USING AN INTERRUPT

In systems such as point-of-sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined above is ideal for this type of system. Where the μP must respond to any change in real-time (e.g., industrial timers/process controllers, TV/VCR clocks or any system where real-time is displayed) then the interrupt timer may be for time reading. Software is used to synchronize the interrupt timer with the time changing as outlined below:

1. Select the interrupt register (write 2 or 3 to ADDR0).
2. Program for repeated interrupts of the desired time interval (see Table IIb in Appendix A-2): *Do not start the timer yet.*
3. Read control register AD0: *This is a dummy read to reset the data-changed flag.*
4. Read control register AD0 repeatedly until data-changed flag is set.
5. Write 0 or 2 to control register. Interrupt timing commences.

When interrupt occurs, read out all required time data. There is no need to test DCF as the interrupt "pre-synchronizes" the time reading already. The interrupt flag is automatically reset by reading from ADDR0 to test it. In repeat interrupt mode, the timer continues to run with no further μP intervention necessary.

TIME READING WITH VERY SLOW READ CYCLES

If a system takes longer than 100 ms to complete reading of all the necessary time registers (e.g., when CMOS processors are used or where high level interpreted language routines are used) then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

The technique below will detect both time changing *between* read strobes (i.e., between reading tens of minutes and units of hours) and also time changing *during* read, which can produce invalid data.

1. Read and store the value of the *lowest* order time register required.
2. Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.
3. Re-read the lowest order register and compare it with the value stored previously in step 1. If it is still the same, then all time data is good. If it has changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads *must* both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no other register has changed either.

APPENDIX A-2. FUNCTIONAL TRUTH TABLES FOR MM58274C

TABLE I. Address Decoding for Internal Registers

Register Selected	Address Bits				Access
	AD3	AD2	AD1	AD0	
0 Control Register	0	0	0	0	Split Read and Write
1 Tenths of Secs	0	0	0	1	Read Only
2 Units Seconds	0	0	1	0	R/W
3 Tens Seconds	0	0	1	1	R/W
4 Units Minutes	0	1	0	0	R/W
5 Tens Minutes	0	1	0	1	R/W
6 Units Hours	0	1	1	0	R/W
7 Tens Hours	0	1	1	1	R/W
8 Units Days	1	0	0	0	R/W
9 Tens Days	1	0	0	1	R/W
10 Units Months	1	0	1	0	R/W
11 Tens Months	1	0	1	1	R/W
12 Units Years	1	1	0	0	R/W
13 Tens Years	1	1	0	1	R/W
14 Day of Week	1	1	1	0	R/W
15 Clock Setting/Interrupt Registers	1	1	1	1	R/W

TABLE IIa. Clock Setting Register Layout

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 Indicates a Leap Year	R/W
AM/PM Indicator (12 Hour Mode)			X		0 = AM 1 = PM 0 in 24 Hour Mode	R/W
12–24 Hour Select Bit				X	0 = 12 Hour Mode 1 = 24 Hour Mode	R/W

TABLE IIb. Interrupt Control Register

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt Output Cleared, Start/Stop Bit Set to 1.	X	0	0	0
0.1 Second		0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second		0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1

Timing Accuracy:
Single Interrupt Mode (all time delays): ±1 ms
Repeated Mode: ±1 ms on initial timeout, thereafter synchronous with first interrupt (i.e., timing errors do not accumulate).

DB3 = 0 for Single Interrupt DB3 = 1 for Repeated Interrupt

TABLE III. The Control Register Layout

Access (ADDR0)	DB3	DB2	DB1	DB0
Reaf From:	Data Changed Flag	0	0	Interrupt Flag
Write To:	Test 0 = Normal 1 = Test Mode	Clock Start/Stop 0 = Clock Run 1 = Clock Stop	Interrupt Select 0 = Clk. Set Reg. 1 = Int. Reg.	Interrupt Start/Stop 0 = Int. Run 1 = Int. Stop

Calibration of the DP8570A Family

National Semiconductor
Application Note 588
James Petrie

This application note applies to the DP8570A, DP8571A, DP8572A, and DP8573A. With respect to the DP8573A, only the discussion of the 32.768 kHz oscillator applies.

The intrinsic properties of quartz make it a uniquely simple device for highly accurate and stable frequency generation. Crystals are not a primary frequency standard but used with care can provide stability far in excess of most requirements. Various configurations of oscillator circuits exist to enable the designer to implement such a source. Its performance, however, is largely dependant on the environment and its associated electrical components. Firstly, consider the basic element—the crystal itself.

A quartz crystal is a mechanically moving system and is very dependant on the environment in which it is operating. The encapsulation will therefore critically affect the long term stability and is a major cause of crystal aging. The choice of crystal holder is important; there are four main types:

TABLE I. Crystal Types

Crystal Type	Aging
Solder Sealed	100 ppm/year
Resistance Welded	4 ppm/year
Cold Welded	2 ppm/year
Glass Enclosed	1 ppm/year

The solder seal units have relatively poor aging characteristics and have now been superceded by resistance welded units. The other three types offer good aging characteristics.

The exact frequency of oscillation is also dependent on the ambient temperature, therefore another important feature to bear in mind when choosing a crystal is the Frequency/Temperature characteristic. If a typical manufacturer's specification is consulted it can easily be seen that there is quite a variation in stability for different temperatures; stabilities of ±20 ppm over a range of −20°C to +70°C are not uncommon.

The capacitors are the components that are most likely to affect the accuracy of the oscillator and care must also be exercised in selection. Since the oscillator plays such an important part in the accuracy of the DP8570A (both timers and real-time selection) it is vital to use good quality examples. There are various types of capacitors available which offer close tolerances and good temperature coefficients. Any of these would be suitable in this application.

TABLE II. Capacitor Types

Capacitor	Typical Tolerance	Typical Temp Coef.
Polycarbonate	5%	50 ppm/°C
Ceramic	10%	30 ppm/°C
Silver Mica	1%	35 ppm/°C

Trimmer capacitors with polypropolene dielectrics give a poorer temp coefficient when compared with those above (typically 300 ppm/°C approx). However, they offer the benefit of allowing the oscillator to be tuned for optimum results.

The oscillator components must be built as close as possible to the pins of the device so as to minimize stray capacitance. The oscillator circuit pins are high impedance nodes and are susceptible to noise coupling from adjacent lines, hence the oscillator should also be surrounded by a guard ground. The maximum length of PCB tracks on either pin is 2.5 cm, longer tracks will reduce oscillator stability.

The accuracy and stability of the oscillator is dependent on various factors; principally external components used, ambient temperature and aging. The information given above is included as a guide to the problems encountered in designing a stable oscillator circuit. Manufacturers specifications should be consulted for more comprehensive data before embarking on designs.

Figures 4a and *4b* show typical curves of frequency temperature characteristics of tuning fork and A-T cut crystals.

DP8570 OSCILLATORS

For the DP8570A, the configuration of the crystal oscillator is the standard Pierce parallel resonant oscillator arrangement which has been designed for low power consumption and high stability, this is shown in *Figure 1*. The external components required are a crystal and two capacitors to provide the correct output loading. The configuration recommended is that of a fixed capacitor and a variable trimmer capacitor, adjusting the trimmer allows the crystal loading (and hence the oscillator frequency) to be fine tuned for optimum results. All other components are on-chip.

The DP8570A has three selectable oscillator frequencies which can be used as a clock source, these are split into two groups, there is the high frequency oscillator and the low frequency oscillator. When programmed for low frequency operation, a small low power inverter is selected along with the relevant bias and feedback resistors, similarly for high frequency operation a larger inverter with a different pair of resistors is selected, *Figure 1* illustrates the basic concept.

A fourth option is available, but this is for driving the OSC IN pin with an external 32.768 kHz signal. In this mode the OSC OUT pin is not connected.

The three different crystals frequencies are; 32.768 kHz, 4.194304 MHz or 4.9152 MHz, see data sheet for full explanation of crystal selection. The recommended capacitance values for these crystals are shown in Table 3.

TABLE III. Oscillator Capacitors

	Variable (Osc In)	Fixed (Osc Out)
32.768 KHz	2 pF–22 pF	47 pF
4.194304 MHz	0 pF–80 pF	68 pF
4.9152 MHz	29 pF–49 pF	68 pF

For optimum performance it is recommended that the variable capacitance is placed on OSC IN. The typical value quoted for the trimmer capacitor is the value that the manufacturer quotes for these commercially available types and which will allow accurate tuning of the oscillator. It is not meant to show the range or tolerance of an equivalent fixed value.

This range is also based on a typical circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases the load capacitance specified by the manufacturer is what determines proper oscillation. This load capacitance is the series combination of capacitance on each side of the crystal with respect to ground.

It is perfectly feasible to use two fixed values, however this will not allow optimum setting of the oscillator frequency. For example a 12 pF fixed capacitor with a tolerance of ±10% is a good substitute for the trimmer capacitor in a 32.768 kHz application.

The HF oscillator has been designed primarily for 4 MHz operation therefore greater care should be exercized when choosing external components for 5 MHz operation. The best configuration for the 5 MHz operation is to use a fixed capacitor in parallel with a trimmer capacitor on the OSC IN pin. Note the small variation of the OSC IN capacitance required to ensure correct start-up and oscillation.

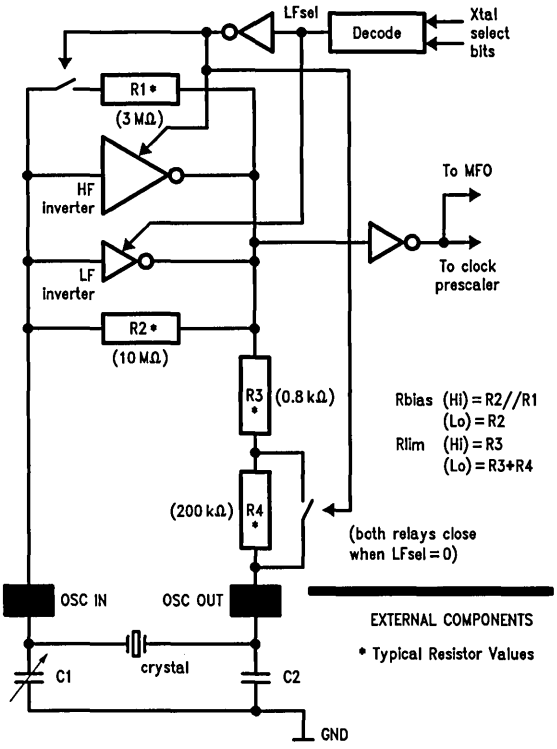

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FIGURE 1. DP8570A Oscillator

CALIBRATION ROUTINE

A calibration routine is necessary to maintain the oscillator output at the desired accuracy and thus optimize time keeping accuracy. The problem with calibrating these types of circutis is accessing the oscillator frequency. No test equipment should be connected directly to either oscillator pin, as the added loading will alter the characteristics of the oscillator making accurate tuning impossible.

For the DP8570A, the calibration can be accomplished using the Multi-Function Output (MFO) pin of the device. The MFO pin can be programmed for several different functions.

1. Buffered Crystal Output
2. Second Interrupt Pin
3. Timer 0 Output

The crystal frequency can be made available at this pin. Since it is buffered a measuring device can be connected directly to it and the oscillator will remain unaffected. Further, this task can be accomplished under software control and without entering test mode.

Adjustment of the oscillator can be carried out using the setup shown in *Figure 2*, by tuning the capacitance C1 the user can see what effect this variation has on the frequency value.

The following sequence of operations is the calibration routine that is required when setting up the oscillator.

1. Main Status Register. Write 01xx xxxx. Select RS = 1, PS = 0.
2. Output Mode Register. Write 1011 xxxx. Select MFO as buffered oscillator with push/pull and active high configuration.
3. Real Time Mode Register. Write 0000 0000. Select desired crystal frequency (32.768 kHz).
4. Main Status Register. Write 00xx xxxx. Select RS = 0, PS = 0.
5. Periodic Flag Register. Write 00xx xxxx. Select Battery backed mode and ensure not in test mode (bit D6 = 1 for single supply mode).
6. Monitor the MFO pin with an oscilloscope and observe that the oscillator is functioning at approximately its correct frequency.
7. Connect a frequency measuring instrument to the MFO pin.

   Care should be exercised when choosing an instrument with which to measure the frequency. To achieve accuracies of 10 ppm or greater high resolution high accuracy instruments only should be used. Instruments recommended are HP 5334A or PHILLIPS PM 6654.
8. Adjust the trimmer capacitor until the desired accuracy is obtained (2 ppm should be achievable). *Figure 5* shows the relationship between frequency error or in ppm vs time gained/lost in minutes/year.

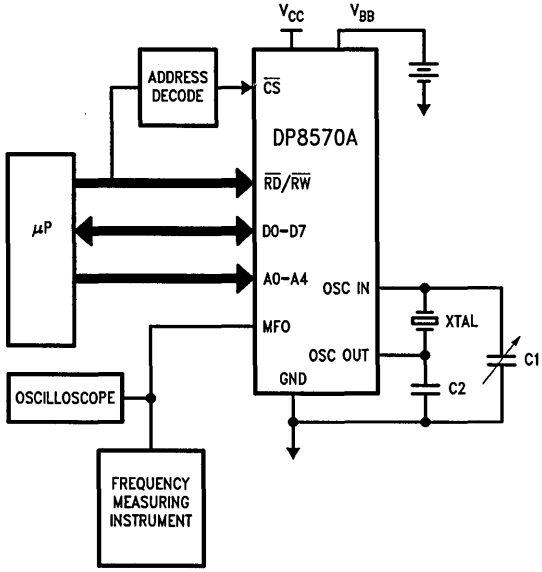

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FIGURE 2. Calibration Setup

TEST CONSIDERATIONS

Under test conditions a crystal cannot be used as there is no control over its output, a pulse generator must be used to clock the device in a controlled manner. This presents correlation problems when measuring I_{DD}/I_{BB} because the clock signal used in testing is a square wave and the values for current consumption will be different. The graphs in *Figure 3* show the values of operating current (I_{DD}) and standby current (I_{BB}) for different temperatures, voltage and crystal.

The graph that is the most important is I_{BB} at 32.768 kHz, the data sheet states that no more than 10 μA of standby current will be consumed across temperature for V_{BB} = 3V. Typical values at T = 25°C (V_{BB} = 3V) as measured on the tester are approximately 4 μA, this compares with 6 μA as measured with a crystal. If a user wishes to use the 10 μA specification, he must limit the battery supply to approximately 3.5V, (see Graph 3a). Graph 3b shows that the standby current does not vary a great deal with temperature.

For the I_{CC} measurement a typical value at V_{CC} = 5.5V, T = 25°C is 160 μA as measured with a tester as opposed to a value of 162 μA with a crystal. There is little difference between the two values. The same cannot be said for the high frequency crystals, the tester figure of 210 μA for V_{CC} = 3V, T = 25°C compared to only 97 μA for a crystal. The reason for this is as follows, when forcing with a clock source the current is largely dependent on the capacitance at the OSC OUT pin, the larger the value the larger the current drawn.

During testing the OSC OUT pin cannot be bent out of the test socket therefore there will aways be some value of stray capacitance connected to OSC OUT. Hence, increased current will always be expected.

For the lower frequency crystal the stray capacitance on OSC OUT does not play a major part so the current is greater because of the greater rate of change of the square wave compared to the sine wave output of a crystal.

CONCLUSION

The calibration of crystal oscillators is fairly straight forward but is of prime importance and as can be seen this task can be accomplished very easily. Regular monitoring of the oscillator frequency can thus be performed with no major disruption to the device's operation.

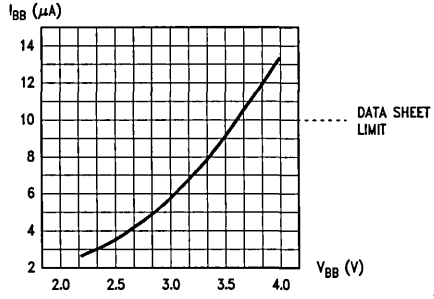

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FIGURE 3a. Standby Current against Battery Voltage T = 25°C (32.768 kHz)

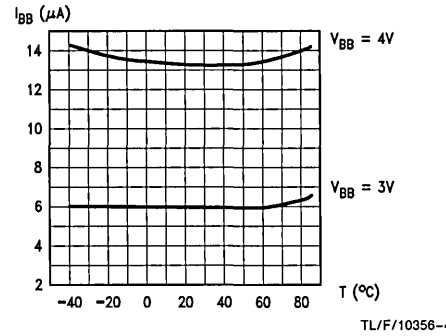

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FIGURE 3b. Standby Current against Temperature (32.768 kHz)

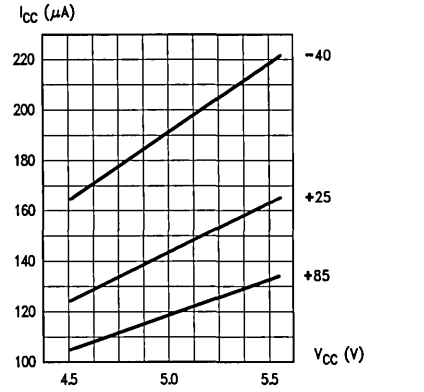

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FIGURE 3c. Operating Current against Supply Voltage (32.768 kHz)

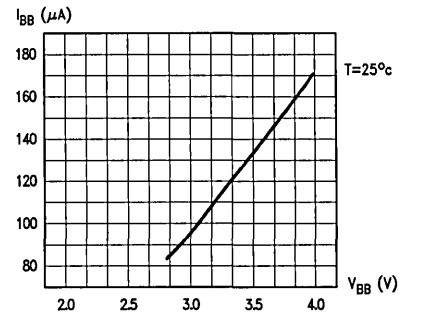

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FIGURE 3d. Standby Current against Battery Voltage (4.194304 MHz)

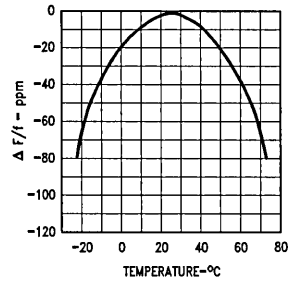

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FIGURE 4a. Frequency Temperature Characteristic for a Typical 32.768 kHz Tuning Fork Crystal

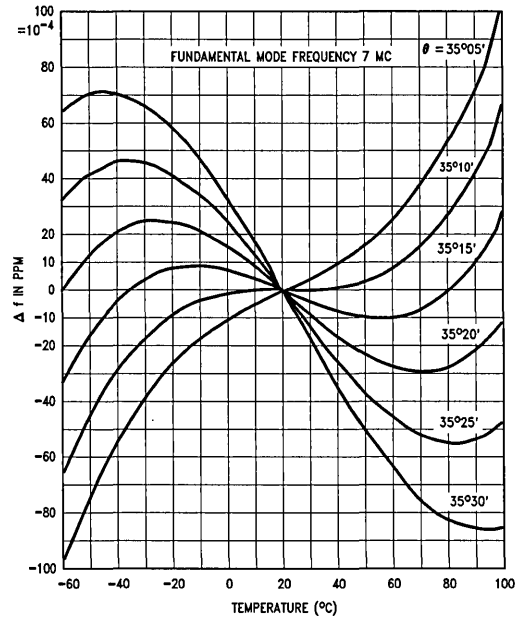

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FIGURE 4b. Frequency-Temperature-Angle Characteristics of Plated AT-Type Natural Quartz Crystal Resonators (from "Crystal Oscillator Design and Temperature Compensation")

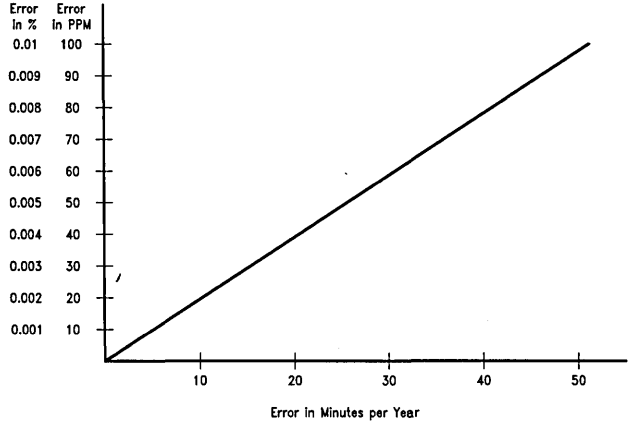

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FIGURE 5. Oscillator Error in % or PPM vs Error in Time

DP8570A Timer Clock Peripheral Test Mode and Test Considerations

National Semiconductor
Application Note 589
James Petrie

Primarily the test mode is used by National Semiconductor to ease the testing of device at manufacture. However, some users may wish to implement testing of devices prior to being used in designs. The purpose of this application note is to give the user insight into what is involved when testing the DP8570A Timer Clock Peripheral (TCP). The complete range of test mode features is presented here along with notes on how to use them. General testing guidelines are also given which should help the user to avoid some of the pitfalls at the design-in stage.

INTRODUCTION

The real-time clock section of the DP8570A is a series of cascaded registers. To test the correct roll-over of each register in this configuration would take a very long time. For example, if clocked in real-time (100 Hz), testing would take 100 years to complete, obviously this is unacceptable.

Similar problems exist when testing the timers. Each timer is 16 bits wide. If it were to be tested in normal operation, 65536 (2^{16}) pulses are required to produce a cycle in the 16th bit in the chain. This will result in an intolerable increase of testing time.

There are further test considerations with the timer prescaler section of the device. These sections contain frequency divider circuits. The easiest way to test these dividers is to measure the frequency of the output and relate it to the frequency of the input. However, with some standard production machines it is difficult to measure frequency. Therefore it will be difficult to check the various outputs of the timer prescaler.

The actual method of testing these prescalers is to apply a set number of pulses to the input of the divider and monitor the output for a change of state. For example, to test the divide by 32000 counter, that number of pulses would have to be applied to produce an output pulse. If the normal timer prescaler configuration is used it will take one full second waiting for the divide by 32000 counter to cycle.

TEST MODE FEATURES

To overcome testing difficulties of the types discussed a test configuration has been designed into the device, which can be implemented via software. Due to the complex nature of the TCP a complete register is required to control the various test functions. This register is situated at RAM location 1F (hex) on page 0 (see datasheet for details of addressing).

The byte associated with this address is normally a general purpose RAM location. When in test mode, the register can be programmed to implement various test configurations. To enable these functions the test mode enable bit (D7) in the Periodic Flag Register (PFR) must be programmed high. For normal operation this bit must be programmed low. The Test Mode Register configuration is shown in *Figure 1*.

D7	D6	D5	D4	D3	D2	D1	D0
OSF DISABLE	CRB1	CRB0	SRB1	SRB0	EMC	CTR TEST	DIR CLOCK

FIGURE 1. Test Mode Register

The functions of the various bits in the test mode register are outlined below. Bits D0,D1 are for the real time and associated sections, while bits D2 to D6 are dedicated for timer use. D7 is for general use.

DIR CLOCK: This is the Direct Clock bit. When programmed high, the oscillator dividers (32 kHz and 1 kHz) and the pulse subtractor in the clock prescaler are bypassed. Thus the counters in the real-time section may be clocked directly from a signal presented to the OSC IN pin. To implement the by-pass correctly, the frequency select bits D6,D7 in the Real-Time Mode Register, must be programmed such that the 4 MHz and 5 MHz divider chains are also disabled (see *Figure 2*). The correct programming for this is D6,D7 = 0 or D6,D7 = 1.

The 4 MHz and 5 MHz dividers can be tested in isolation using the following:

DIR CLOCK = 1 and D6 = 1 for 4 MHz,
DIR CLOCK = 1 and D7 = 1 for 5 MHz.

The output of these dividers will then be connected directly to the 1/100 second counter.

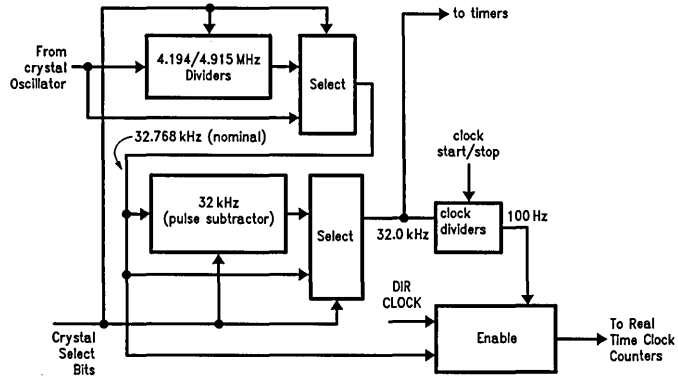

FIGURE 2. Clock Prescaler (with Test Bit)

CTR TEST: This is the Counter Test bit. When programmed high this bit re-configures the real-time counters into the test mode configuration (see *Figure 3*). These counters can then be clocked in parallel thus reducing the test time.

Note that the normal maximum operating frequency of these counters is 100 Hz and the low frequency oscillator is designed to work at approximately 32 kHz. Therefore if fast clocking via the OSC IN pin is attempted serious signal degradation will occur, making testing impossible. For these reasons it is recommended that for a V_{BB} = 3V, a maximum clock rate of 200 kHz (2.5 μs pulse width) is used on all tests where the OSC IN pin provides the clock source. When testing the device using clock bursting, the clock must be a return-to-one signal. It is not recommended that the OSC OUT pin be used as a clock source, and must not be connected.

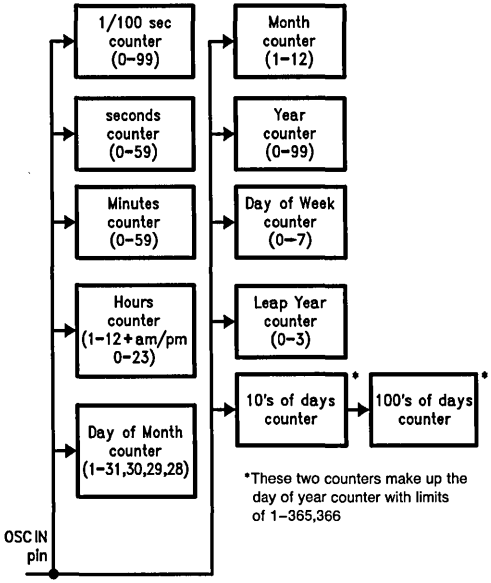

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FIGURE 3. Real Time Counters, Test Mode Configuration

EMC: This is the Enable MSB Clock bit. When programmed high it enables the most significant bytes (MSBs) of both 16-bit counters to be clocked directly. Note that the LSB's of the counters must contain 00(hex) for this to be accomplished correctly. This allows the timers to be tested in two halves, which will give a total of 2 × (2^8) possible states instead of 2^{16} significantly reducing the test time.

SRB0: This is the Signal Route Bit for timer 0 prescaler. When programmed high this bit routes the selected clock to the timer 0 output.

SRB1: This is the Signal Route Bit for timer 1 prescaler. When programmed high this bit routes the selected clock to the timer 1 output.

The inclusion of the "SRB" bits means that a more modular approach to timer testing is achieved because the timer prescalers can be tested in isolation.

The clock select bits in the Timer Control Register are used to route the required clock to the multiplexer output "selected clock", of the prescaler, see *Figure 4*. Note that timer 0 output is accessed using the Multifunction Output (MFO) pin, see datasheet for details. However, timer 1 output can be accessed directly using the Timer 1 Output (T1) pin.

CRB0: This is the Crystal Route Bit for timer 0 prescaler. When programmed high this bit routes the external crystal frequency to the dividing counters in timer 0 prescaler which are normally driven by the internal 32.0 kHz signal. See *Figure 2*.

CRB1: This is the Crystal Route Bit for timer 1 prescaler. When programmed high, this bit routes the external crystal frequency to the dividing counters in timer 1 prescaler which are normally driven by the internal 32.0 kHz signal.

The "CRB" bits allow all the timer prescaler dividers to be clocked directly from the OSC IN pin. This allows fast clocking of these circuits plus allowing a known number of pulses to be input. Note that the frequency select bits in the Real Time Mode register need to be programmed correctly for this section as well (D6,D7 = 0).

OSF DISABLE: This is the OSC Fail Disable bit. When programmed high this bit causes the OSC FAIL detect circuitry in the clock prescaler to be disabled.

One of the features of the DP8570A is its ability to detect when an oscillator fail has occurred. Oscillator failure is indicated by reading bit D6 in the Periodic Flag Register. When an oscillator fail is detected four functions are performed.

1. The OSC fail flag is set.
2. The clock start/stop bit (CSS) in the Real Time Mode register is reset, preserving the time that the oscillator stopped.
3. Overrides the lockout circuitry ensuring that the processor interface is not locked out when an oscillator fail has occurred.
4. Presets battery bit (D6) in PFR (selects the single power supply mode).

Under test conditions a crystal cannot be used because there is no control over its output. A pulse generator must be used to clock the device in a controlled manner. Obviously, under these single-step conditions the oscillator fail circuitry will detect a lack of oscillation and perform the functions mentioned. Therefore for certain tests it will be necessary to disable the effect of OSC fail (where CSS must remain active for example), this is accomplished using the OSC Fail Disable bit.

To get access to the OSF Disable bit, the test mode enable bit (D7 in the PFR) must be written high first. The order is important. The OSF Disable bit must also be programmed back to zero when testing is complete. This is to avoid drawing excess current in standby mode. When initial power is applied, this bit has been designed to power-up in the inactive state, ensuring that the TCP will not enter a state of permanent lockout when power is applied.

The implications of function 4 are also important when considering the fact that a pulse generator is used to provide the clock source. The amplitude of the output signal should be equal to the power supply of the oscillator (V_{OSC}).

In battery backed mode	$V_{OSC} = V_{BB}$
In single power supply mode	$V_{OSC} = V_{CC}$

When testing the device in battery backed mode, and using single pulses, the following steps are necessary to ensure that the device is in the correct mode.

MSR	00	RS = 0
PFR	80	Test Mode Enable
TST	80	OSC Fail Disable Bit
PFR	80	Battery Bit and Test Mode

The reason the PFR has to be written twice is that the OSC FAIL signal will preset the single supply bit (D6) and has to be disabled before D6 can be written to.

Read/Write Considerations

In the DP8570 the bits in the address space consist not only of normal read/write bits but also flags, read-reset flags, write-1 reset flags and a dual function bit. The user should be aware of these when attempting to read/write to the device.

Read/Write Bits

MSR	D6,D7 Only
TCR0, TCR1	D0–D7
PFR	D7 Only
IRR	D0–D5, D7
RTMR	D0–D7

(Bit D3 will remain at 0 unless in test mode or the oscillator is running)

OMR	D0–D7
ICR0, ICR1	D0–D7
1/100 sec	D0–D7
SECONDS	D0–D6 (D7 Always 0)
MINUTES	D0–D6 (D7 Always 0)
HOURS 24 hr	D0–D5 (D6,D7 Always 0)
HOURS 12 hr	D0–D4

(D5,D6 Always 0, D7 = am/pm Bit)

DAY of MONTH	D0–D5 (D6, D7 Always 0)
MONTH	D0–D4 (D5–D7 Always 0)
YEAR	D0–D7
DAY of YEAR	D0–D7
100's DOY	D0, D1 (D2–D7 Always 0)
DAY of WEEK	D0–D2 (D3–D7 Always 0)

The rest of the address locations are all read/write but certain precautions need to be observed to get a correct response. It is recommended that the control section is reset to all zeros before attempting to write to the rest of page 0 locations.

Flags

The flags are read only and are set and reset by events inside the device. They are situated at the following locations.

Batt Low Flag	D6 of IRR
Power Fail Flag	D1 of MSR
Interrupt Status Flag	D0 of MSR
Dual Function	D6 of PFR

When READ, D6 of the PFR will give the contents of the OSC FAIL flag. When WRITTEN, D6 sets up the power supply mode of the DP8570A. Writing a "1" selects single power supply mode, writing a "0" selects the battery backed mode.

The implications of this are quite important because there is no direct way the user can tell which power supply mode is selected. The only way of determining the mode is by monitoring the OSC OUT pin. The amplitude of this signal will be approximately equal to the value of V_{OSC}.

In battery backed mode the amplitude will be V_{BB}, in single supply mode the amplitude will be V_{CC}. Most of the time, the OSC OUT pin may be measured using a 10 MΩ, 10 pF probe. However, when the high frequency oscillator, the oscillator may stop. For this case a higher impedance, lower capacitance probe may be needed.

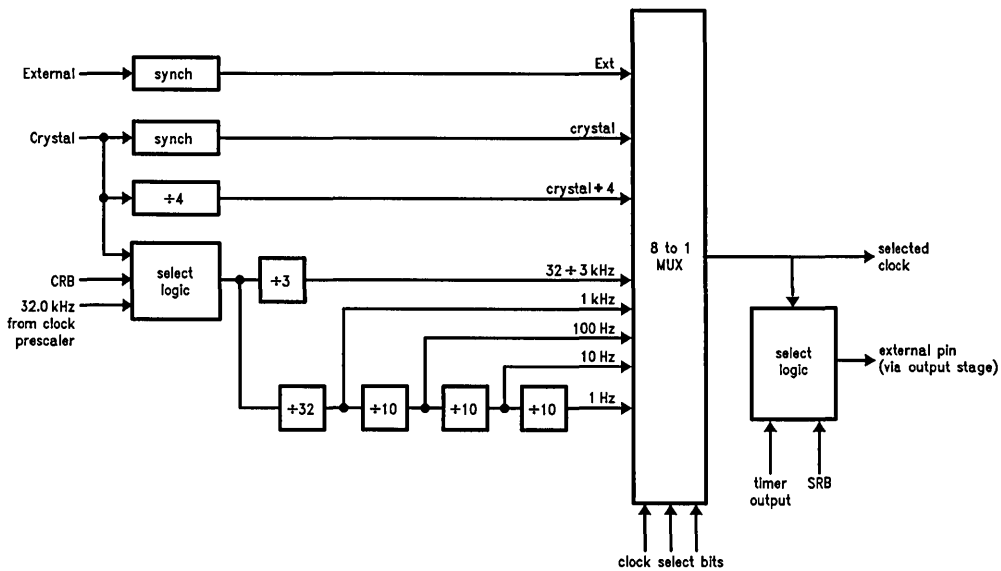

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FIGURE 4. Timer Prescaler (with test bits)

The only way of determining the mode is by monitoring the OSC OUT pin. The amplitude of this signal will be approximately equal to the value of V_{OSC}.

In battery backed mode the amplitude will be V_{BB}, in single supply mode it will be V_{CC}. This technique is helpful when using either a pulse generator or crystal as the clock source. However, care should be taken if probing OSC OUT when a crystal is used, as the probe capacitance could stop the oscillation. As a minimum, a 10 Meg, 10 pF probe is recommended.

The read-reset flags are situated at D0–D5 of the PFR and are read only. Internal events inside the device set the flags and they are reset when read.

The write-1 reset flags are situated at D2–D5 of the MSR. They can be read as a 1 or 0, and are set by internal events inside the device. Writing a 0 to these bits will have no effect. Writing a 1 will reset these flags.

CONCLUSION

The purpose of this note is to provide some insight into the complexities of testing the DP8570A. It shows how various tests can be carried out efficiently by designing testability into a device. The actual testing implemented by the user can be simple or comprehensive and only those features required need be utilized.

Flexible Timers on the DP8570A and DP8571A

National Semiconductor
Application Note 595
Jim Mitchell

1.0 INTRODUCTION

The DP8570A/71A/72A/73A family are Real Time Clock devices for use in microprocessor based systems. They are fast access low power devices with power fail protection, standby battery operation, multiple interrupts and RAM. In addition, the DP8570A and DP8571A "Timer Clock Peripherals" have two independent 16-bit binary countdown timers.

This application note deals primarily with using the timers on the DP8570A. It has dedicated timer pins; an external clock pin with up to 10 MHz operation, a hardware gate/hold pin per timer and a timer output pin. Further information is given on the DP8571A which does not have these pins, hence reducing the pin-count, but has the additional feature of being able to cascade the timers. This gives use of a timer of up to 32 bits.

The timers of both Timer Clock Peripherals have four modes of operation, seven crystal derived internal clock frequencies, programmable output/interrupts and standby operation.

2.0 DP8570A TIMERS *(Figure 1)*

Each timer, T0 and T1, has two 8-bit registers (MSB/LSB) accessed in page 0 of the DP8570A internal memory. The number in these registers is loaded into a 16-bit counter when the timer is started and the counter is decremented by the selected input clock, hence controlling the timer output. Resetting the timer start/$\overline{\text{stop}}$ bit stops the timer and puts its output into its inactive state (high or low depending on how the output is programmed). Every time the start/$\overline{\text{stop}}$ bit is set the initial value in the MSB/LSB registers is reloaded by the next selected timer input clock. A gate signal, however, is also required in mode3 before loading occurs.

Normally when accessing the data at the address of the MSB/LSB registers, only the initial load value will be read. However, if the timer read bit is set, the MSB/LSB of the counter itself will be read. This allows the user to read the counters *on-the-fly*, without disturbing timing.

The user might encounter a problem when the timer read bit is set just as the counter is reloading. In this case there is a possibility of erroneously reading a value FFhex. The user should choose initial register values other than FFhex, reject any FFhex read on-the-fly and try the read operation again.

The T0 and T1 timer start/$\overline{\text{stop}}$ bit and timer read bit are in their respective timer control registers. Each timer control register contains the following bits:

D0 Timer Start/Stop
D1 Mode Select M0
D2 Mode Select M1
D3 Input Clock Select C0
D4 Input Clock Select C1
D5 Input Clock Select C2
D6 Timer Read
D7 Count Hold/Gate

The programming of this and other timer related registers is described in Section 3.0.

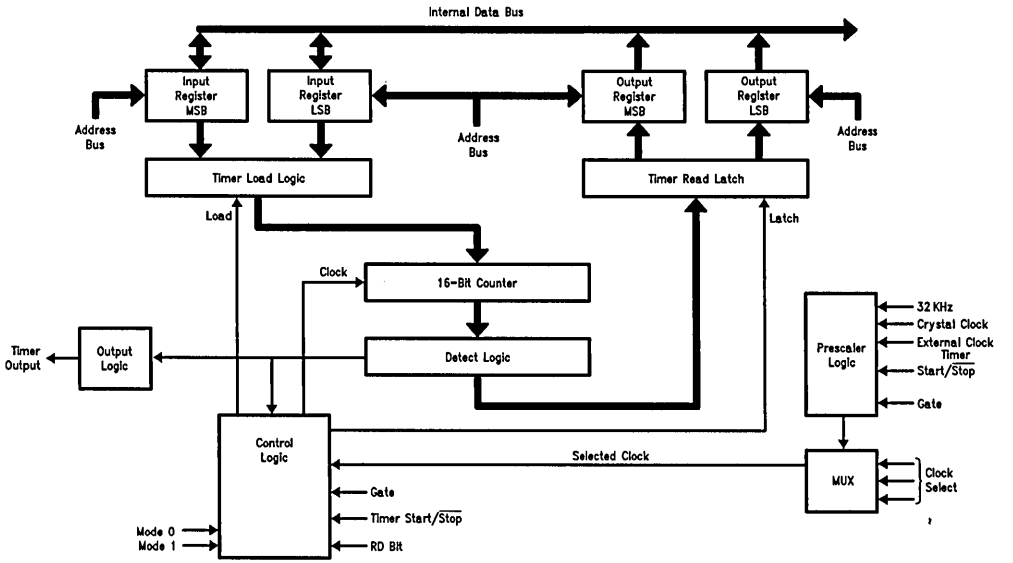

FIGURE 1. DP8570A Timer

3.0 USING DP8570A TIMERS

The following steps should be considered when using the DP8570A timers.

a) Mode selection to give desired output waveform.

b) Input and frequency selections to give countdown rate of timer.

c) Output and interrupt selections.

d) Standby conditions (if backed up).

3.1 Mode Selection

Four output waveforms are obtainable from the DP8570A, selected by two bits in the timer control registers (Table I).

TABLE I. Timer Control Registers Mode Bits D2, D1

M1	M0	Mode
0	0	0
0	1	1
1	0	2
1	1	3

3.1.1 MODE 0: Single Pulse Generator *(Figure 2)*

In this mode, a timer output will become active and its counter will decrement once its start/$\overline{\text{stop}}$ bit is set. As soon as the count reaches zero, the start/$\overline{\text{stop}}$ bit is automatically reset and the output returns to its inactive state. Hence the active time (pulse width) is

Timer Clock Period × Number in Counter.

The pulse width can be increased by temporarily stopping the clock in two ways. One is to set the timer count hold/gate bit and the other is to put the respective G Input pin to a logic one state. The count-down is resumed once the count hold/gate bit is reset or G input is returned to logic zero.

3.1.2 MODE 1: Rate Generator *(Figure 3)*

In this mode, a timer output will become active and its counter will decrement once its start/$\overline{\text{stop}}$ bit is set. When the count reaches zero, the output goes inactive for one timer clock period. The counter is reloaded with the number in the registers. On the next clock the output goes active again and the sequence continues until the start/$\overline{\text{stop}}$ bit is reset. The period is

Timer Clock Period × (Number In Counter + 1)

and the (inactive) pulse width is the timer clock period. As in mode 0, the count-down can be suspended by setting the count hold/gate bit or using the G input pin.

3.1.3 MODE 2: Square Wave generator *(Figure 4)*

In this mode, a timer output will become active and its counter will decrement once its start/$\overline{\text{stop}}$ bit is set. On the clock after the count reaches zero, the output goes inactive. The counter is reloaded with the number in the registers and the counter will decrement to zero again before returning to the active state. The sequence continues until the start/$\overline{\text{stop}}$ bit is reset. The period is

2 × Timer Clock Period × (Number In Counter + 1)

with a 50% duty cycle. As in mode 0, the count-down can be suspended by setting the count hold/gate bit or using the G input pin.

3.1.4 MODE 3: Retriggerable One Shot *(Figure 5)*

In mode 3, a timer output will not become active as soon as its start/$\overline{\text{stop}}$ bit is set. A trigger is also required to start a pulse. The trigger is either setting the count hold/gate bit or the rising edge of a pulse on the respective G input pin. (A trigger pulse as short as 25 ns can be used.) This trigger puts the timer output in the active state and initiates the timer count-down sequence. When the count reaches zero, the output goes inactive until another trigger is given. The pulse width is

Timer Clock Period × Number in Counter.

If another trigger is given while the timer is still decrementing, the initial number from the timer registers is reloaded thus extending the pulse. The DP8570A remains operational in this mode until the start/$\overline{\text{stop}}$ bit is reset.

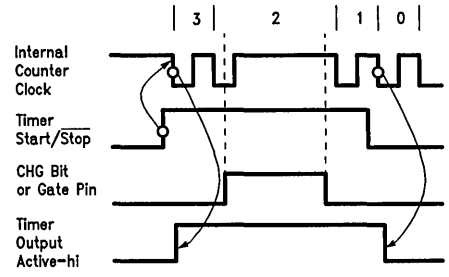

FIGURE 2. Mode 0—Single Pulse Generator

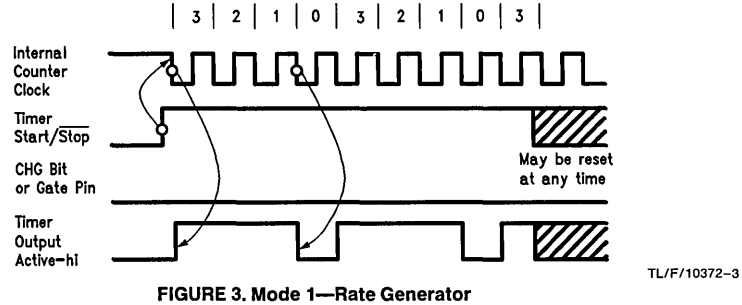

FIGURE 3. Mode 1—Rate Generator

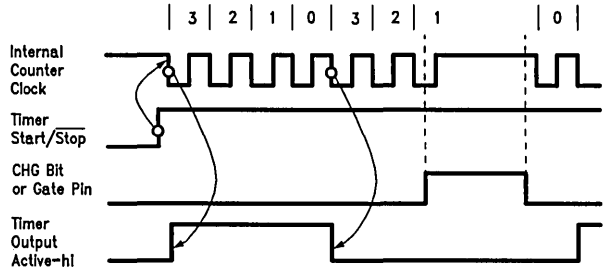

FIGURE 4. Mode 2—Square Wave Generator

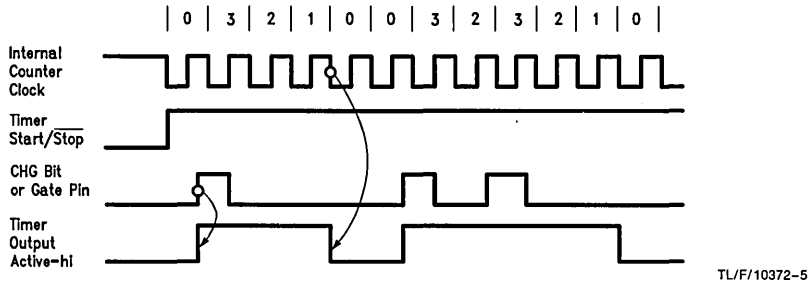

FIGURE 5. Mode 3—Retriggerable One Shot

3.2 Input and Frequency Selection

The DP8570A has a real time clock which can operate from any of four different crystal frequencies. The crystal frequency is selected in the real time mode register (Table II).

TABLE II. Real Time Mode Register Crystal Select Bits, D7, D6

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

This crystal frequency or a lower frequency derived from it can be used to clock the timers by programming the C2, 1, 0 bits in the timer control registers (Table III) to values 001 to 111 inclusive.

TABLE III. Timer Control Registers Input Select Bits, D5, D4, D3

C2	C1	C0	Timer Clock
0	0	0	External
0	0	1	Crystal Frequency
0	1	0	(Crystal/Freq.)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	0.1s (10 Hz)
1	1	1	1s (1 Hz)

Alternatively, the DP8570A timers can be clocked externally via the TCK pin by writing 000 to these input clock select bits. Falling edges of a 50% duty cycle input on the TCK pin clock the timer(s) at up to 10 MHz.

The other DP8570A timer input pins are G0 and G1 for timers T0 and T1 respectively. Their action depends on the mode selected and is described above.

3.3 Output and Interrupt Selections

The T1 pin on the DP8570A is a dedicated output from timer 1, whereas the MFO pin can be configured as the timer 0 output by programming the output mode register (Table IV).

TABLE IV. Output Mode Register Output Pin Configurations

D7	D6	MFO
0	0	INTR
0	1	T0
1	X	OSC

MFO	D7	0 (For Timer/INTR Output)
	D6	T0/2nd-INTR
MFO	D5	Push-Pull/Open-Drain
	D4	Active-Hi/Active-Lo
INTR	D3	Push-Pull/Open-Drain
	D2	Active-Hi/Active-Lo
T1	D1	Push-Pull/Open-Drain
	D0	Active-Hi/Active-Lo

The output mode register also sets up the T1, MFO and INTR pins as active high or low, push-pull or open-drain outputs individually. Care should be taken not to connect an open drain output to a voltage above the supply voltage in use at the time (i.e., normally V_{DD}, but V_{BB} in standby).

Whenever a timer goes to its inactive state (except when the start/$\overline{\text{stop}}$ bit is reset), it generates an interrupt, setting a bit in the main status register *(Figure 6)*. Interrupt control register 0 includes one bit for each timer (D6, 7 for T0, 1 respectively) to enable the interrupt at an output. The interrupt routing register has one bit per timer (D3, 4 for T0, 1 respectively) to route the interrupt to either the INTR pin or MFO pin (if programmed as a second interrupt pin). The interrupt status bit (D0 of the main status register) is also set when an interrupt (timer, alarm, powerfail or periodic) is pending at an output pin. Writing 1's to the main status register resets interrupts.

3.4 Standby Operation

The DP8570A power supply mode should be programmed on initial power-up by writing to bit D6 of the periodic flag register. Write 1 for single supply mode (hence no standby features) or 0 for battery backed-up mode. If thus configured, the device will enter "standby" mode if $V_{BB} > V_{DD}$. (See datasheet for hardware configurations.)

In standby the timers are still operational if bit D5 of the real time mode register is set, and if so, timer (and other) interrupts can be operational in standby if bit D4 is set. The TCK and G input pins, however, are locked out. In standby, MFO, INTR and T1 outputs are automatically configured in as open-drain outputs. When power is restored ($V_{DD} > V_{BB}$) they return to the output mode register configuration.

3.5 Power-Fail Operation

If a low going power loss signal is detected at the $\overline{\text{PFAIL}}$ pin, timer operation is unaffected, but the databus will be locked out.

4.0 PROGRAMMING STEPS

The following steps are recommended for setting-up DP8570A timer(s) after initial power-up.

a) **Main Status Register:** PS = 0, RS = 1.

b) **Real Time Mode Register:** Set crystal bits (Table II) and standby operation bits.

c) **Main Status Register:** PS = 0, RS = 0.

d) **Periodic Flag Register:** Set bit D6 for single-supply mode or reset it for backed-up mode and reset D7 so that the device is not in test mode.

e) **T0 and/or T1 Control Register:** Reset start/$\overline{\text{stop}}$ bit (D7) to ensure timers are not running.

f) **Interrupt Routing Register:** Route T0/1 interrupts (0 to INTR, 1 to MFO) if required.

g) **Main Status Register:** PS = 0, RS = 1.

h) **Output Mode Register:** Configure T1, INTR and MFO Outputs (Table IV).

i) **Interrupt Control Register 0:** Set T0/1 interrupt enable bits if required.

j) **MSB/LSB T0/1 Registers:** Load values for timer counter(s).

k) **READ:** main status register to clear old interrupts.

l) **Main Status Register:** PS = 0, RS = 0.

m) **T0 and/or T1 Control Registers:** start timer(s) with bits set for mode (Table I) and input clock (Table III).

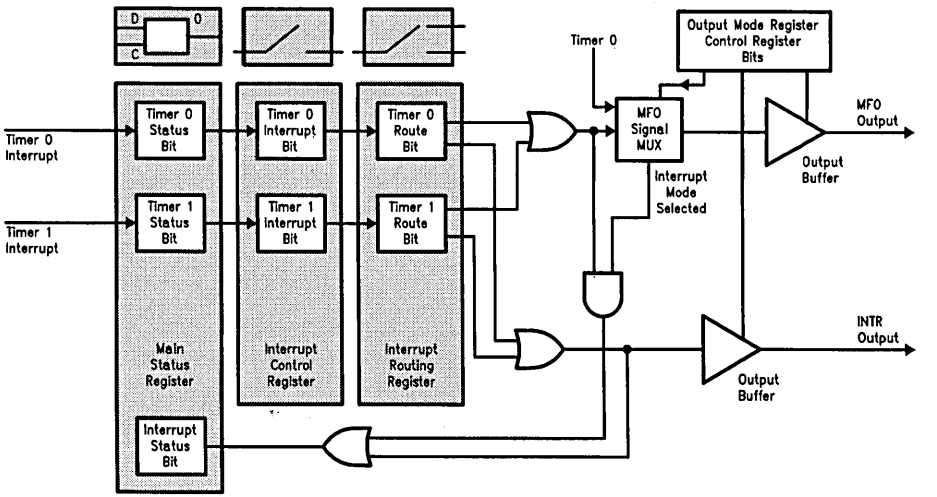

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FIGURE 6. DP8570A Timer Interrupts

If operating timers in a device already powered-up and in a known state, the above order need not be adhered to. Table V gives an example of programming a DP8570A which is already powered-up and operating correctly as a real time clock from some crystal frequency, with power supply configured and not in test mode. This example produces a 10 ms high pulse output (push-pull) every one minute using timer 1.

TABLE V. Programming Example

Write D7–0	Addr.	Reg.	Action
00000000	00000	MSR	PS=RS=0
00000000	00010	TCR1	T1 Stopped
00000010	00000	MSR	RS=1
0xxxxxxx	00011	ICR0	Disable T1 Intr.
00010111	10010	MSB1	} Timer
01101111	10001	LSB1	} Counter = 5999
xxxxxx10	00010	OMR	T1 = p–p, act.hi
00000000	00000	MSR	RS = 0
00101011	00010	TCR1	Start T1: Mode 1, 10 ms Input Clock

(x = Don't care in this example, but may affect other DP8570A operations.)

5.0 SYNCHRONIZATION ERRORS

As the operation of starting and stopping timers is normally asynchronous to the timer input clock, an error of up to one timer input clock period may occur. Similarly, when using the G input pins or count hold/gate bits, the following synchronization errors can occur depending on timer input clock selected:

External (TCK) +Up to One External Clock Period.

Crystal or Crystal/4 +Up to One Crystal Clock Period.

Other Selections +0 to 32 μs.

6.0 DP8571A

The DP8571A differs from the DP8570A in the following ways.

a) It has no G0 or G1 input pins. The count hold/gate bits are fully functional however.

b) It has no T1 timer output pin. The T1 timer read bit can be used as in the DP8570A to read the value in the timer counter and interrupts are fully functional also.

c) The T1 bits in the output mode register (D1, 0) are RAM bits.

d) It has no TCK input pin.

e) An added feature of the DP8571A is it cascade mode, activated by programming T0 control register C2–0 input clock select bits to 000.

The C2–0 bits in the T1 control register are programmed to select its input clock (000 is not allowed).

6.1 DP8571A Cascade Operation

In the cascade mode, the output of timer T1 is the input clock for T0 *(Figure 7)*. The T1 bits in the output mode register have no effect on T1 and in this mode T1 output should be considered as active-low with falling edges clocking T0.

This mode gives the DP8571A 32-bit counter capability, raising the maximum counter value from 65,535 to 4,294,967,295 (Table VI). If used, for example, as a large hundredths of seconds countdown timer (with 10 ms input clock selected for T1), full range is increased from about 10.9 minutes to over 71 weeks. Also a larger variety of output waveforms can be realised by varying the values in the counters.

TABLE VI. Some Powers of 2 for Reference

Power of 2	Decimal Value
0	1
4	16
8	256
12	4,096
16	65,536
20	1,048,576
24	16,777,216
28	268,435,456
32	4,294,967,296

In cascade mode, timers cannot count down in binary from numbers greater than 65,535 if T1 contains any number other than FFFFhex. This is because T1's MSB/LSB register values are reloaded instead of FFFF when T1's count reaches 0000. The following example shows one way of working around this problem.

For countdown from 65,540 (00010004 hex) with cascaded timers:

a) Reset Timer Control Registers.

b) Write 00hex to T0 MSB, 01hex to T0 LSB registers and 00hex to T1 MSB, 04hex to T1 LSB registers.

c) Setup operating conditions for timers (outputs, interrupts, etc.).

d) Start T0 cascaded from T1, in mode 0–3 as required.

e) Start T1 with required input, in mode 1–3 as required.

f) After first T1 input clock (which loads T1 counter) and before the T1 count decrements to 0000hex, write FFhex to both LSB and MSB T1 registers.

The cascaded counters will continue to count down in effect as a single binary counter.

However, in modes 1 and 2, when T0 and T1 both reach 0000hex, the last values written to their LSB/MSB registers will be loaded (i.e. T0 = 0001hex, T1 = FFFFhex) unless action is taken to restore T1's original values (0004hex in this case) beforehand. One method would be for T0 to generate an interrupt on reaching 0000hex, which initiates a software routine to write the required values to T1 LSB/MSB registers before T1 decrements to 0000.

7.0 TEST MODES

Several features are available on the DP8570A/71A to ease testing by setting the test mode enable bit (D7) of the periodic flag register and programming the test register in page 0 as follows.

a) Set the enable MSB clock bit (D2): allows the two MSB halves of the timer counters to be clocked instead of the LSB halves (LSB must be 00).

b) Set signal route bits 0 and 1 (D3, 4): routes the T0 and T1 selected input clock signal (inverted) to the output and interrupt logic of the device instead of the timer outputs. The DP8571A, timer 1 signal route bit does not affect the output of T1 clocking T0, but allows T1 interrupt logic to be driven from its (inverted) clock instead of its output.

c) Set crystal route bits 0 and 1 (D5, 6): The timer input clocks 10.7 kHz to 1 Hz inclusive (Table III) come from prescalers driven from an internal 32 kHz signal. If the crystal route bit is set for a timer, then its prescaler is instead driven directly by the crystal oscillator. Hence, an external signal generator faster than 32 kHz can be used to speed up testing of the timer. Real time mode register crystal select bits should be set to 32 kHz or 32.768 kHz in this case.

(Test modes are featured in detail on National Semiconductor Application Note 589.)

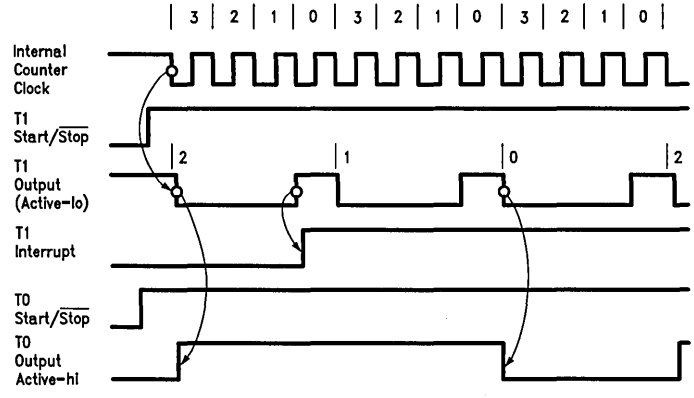

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FIGURE 7. DP8571A Cascade Mode, T0 Mode = T1 Mode = 1, Value in Counters: T1 = 3, T0 = 2

Typical DP8570A Interface to the IBM PC/XT for the Purpose of Engineering Evaluation

National Semiconductor
Application Brief 43
Milt Schwartz

The following information has been provided to assist the reader in developing an evaluation setup for the DP8570A family of Real Time Clocks. This interface was prototyped and debugged for use in an IBM PC/XT or compatible bus computer with an accompanying program written in the C language.

Hardware Used

The interface consists of:

DP8570A Timer Clock Peripheral
74ALS521 Address Decoder (I/O Hex 300 to 31F)
74ALS245 Transceiver (Data Bus Buffer)
Lithium Battery (3.4V Nominal)
Standard Pierce Parallel Resonant Crystal
(32.768 kHz, ±20 ppm)
Various Capacitors (±10%)
Various Resistors (1/8W ±10%)

Refer to the complete schematic provided. *(Figure 1)*

As shown on the schematic, T1, G1, G0 MFO, INTR, and TCK are available for monitoring purposes.

Pins T1, MFO, INTR, and TCK have 3.9k pull-up resistors to V_{BB}. These resistors allow operation of T1, MFO, and INTR outputs during power down when in the battery backed mode. The resistor on TCK guarantees this input will not be floating.

Pins G0 and G1 have 10k pull-down resistors to ground. These resistors ensure that Timer 0 and Timer 1 are enabled by the hardware.

A resistor divider was placed at the $\overline{\text{PFAIL}}$ pin in place of an external power fail signal (as suggested in the data sheet). This facilitates bus lockout during a power fail/return. The user may wish to simulate standby mode by changing the voltage at the $\overline{\text{PFAIL}}$ pin. For example, this may be accomplished by connecting a resistor (fixed or variable) in parallel with the 3.4k resistor.

Separate power supplies for V_{CC} and V_{BB} may be used in place of the system 5V supply and battery for the purpose of monitoring the supply currents.

Software

A demo program, TCP, was written in C language and designed to run on MS-DOS or PC-DOS. The program TCP consists of several pop up menus with the initial display as the main menu. This menu lists the available functions which may be called. Each pop up menu prompts for an entry and provides on-screen documentation.

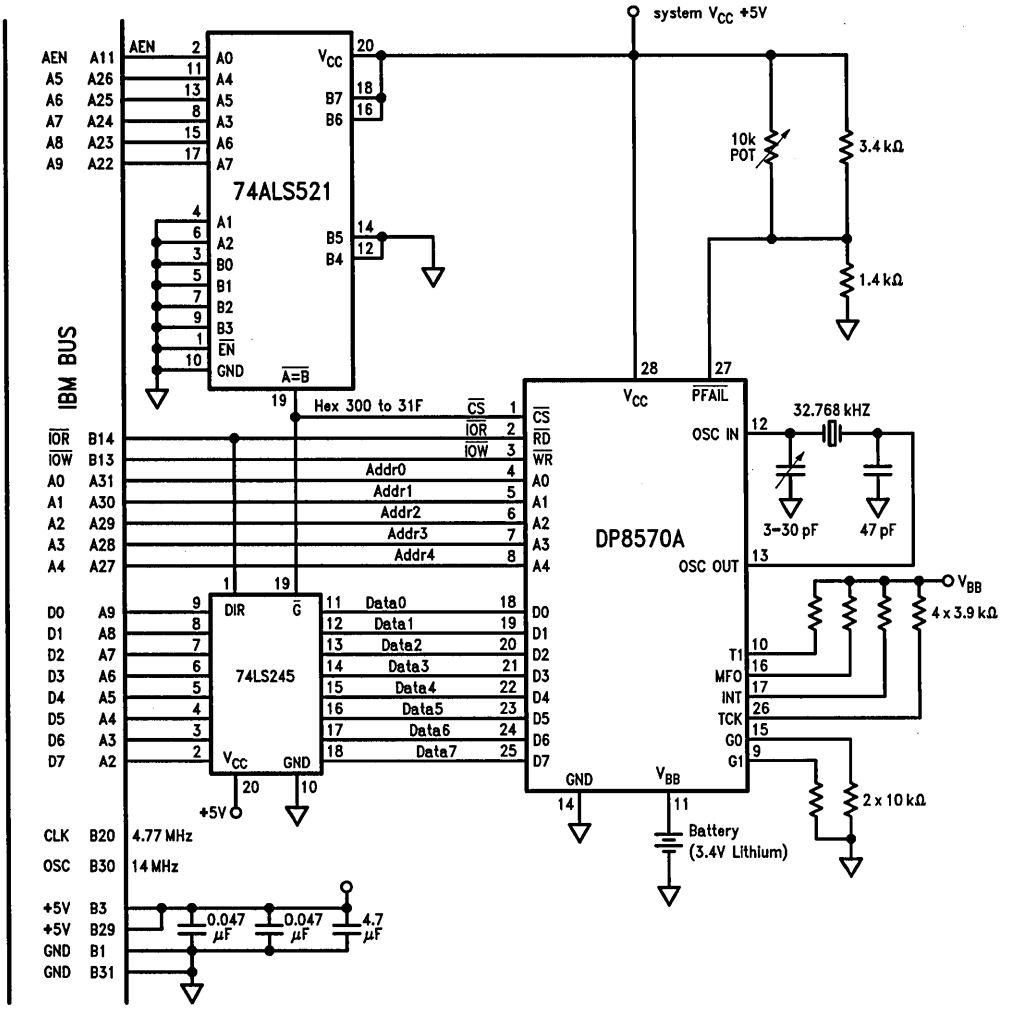

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FIGURE 1. DP8570A Timer Clock Peripheral Interface to IBM/XT

Section 3

Appendices/ Physical Dimensions

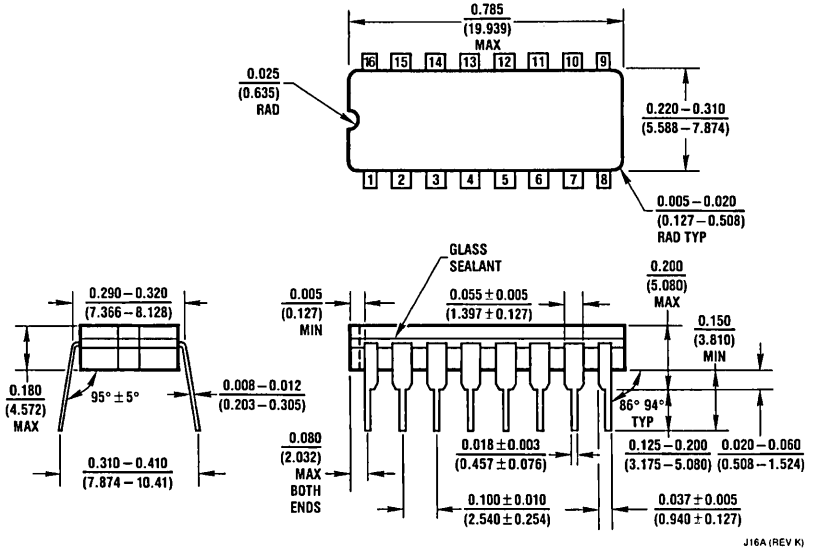
Section 3 Contents

Physical Dimensions 3-3
Bookshelf
Distributors

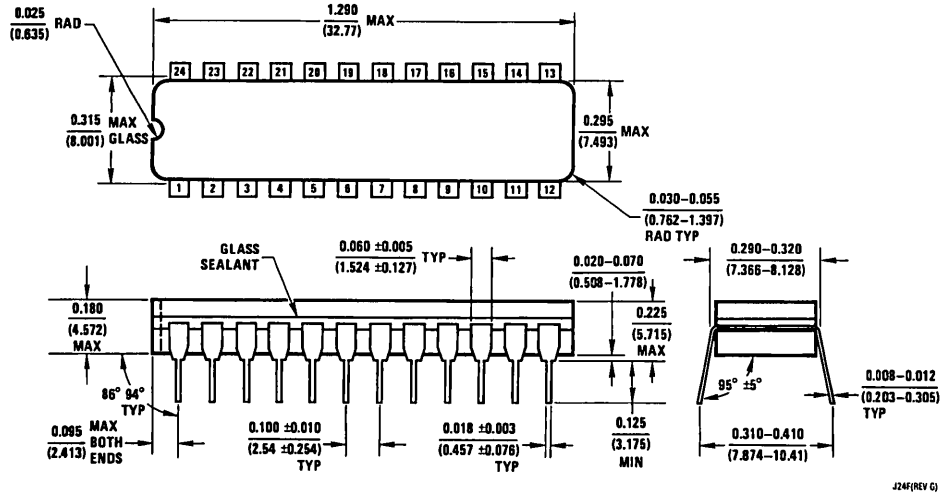
National Semiconductor

All dimensions are in inches (millimeters)

16 Lead Ceramic Dual-In-Line Package
NS Package Number J16A



24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package
NS Package Number J24F



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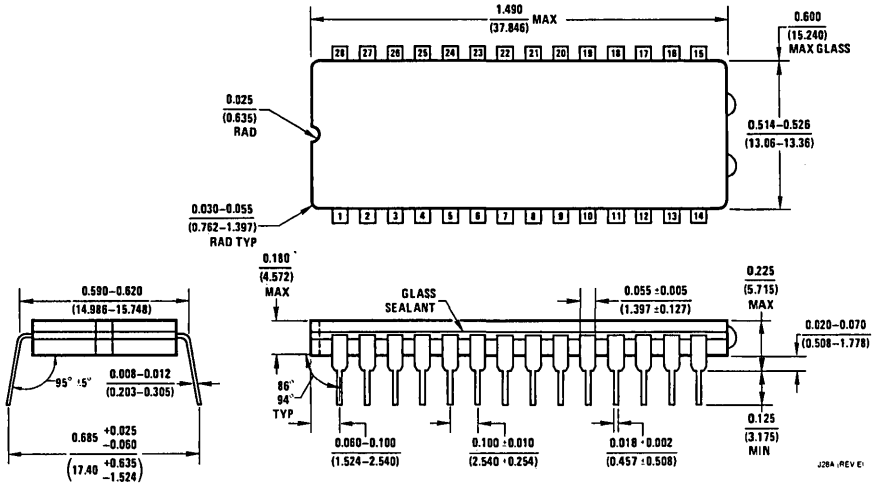
28 Lead Ceramic Dual-In-Line Package
NS Package Number J28A



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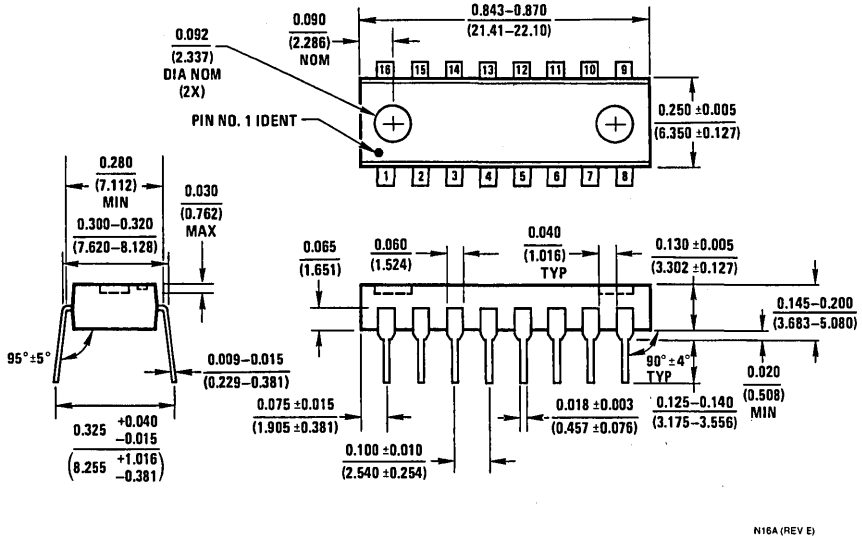
NS Package Number N16A



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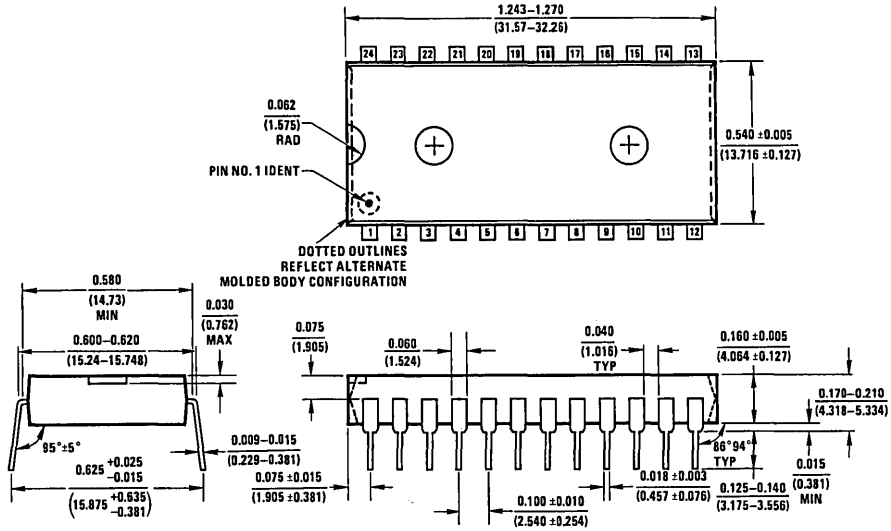
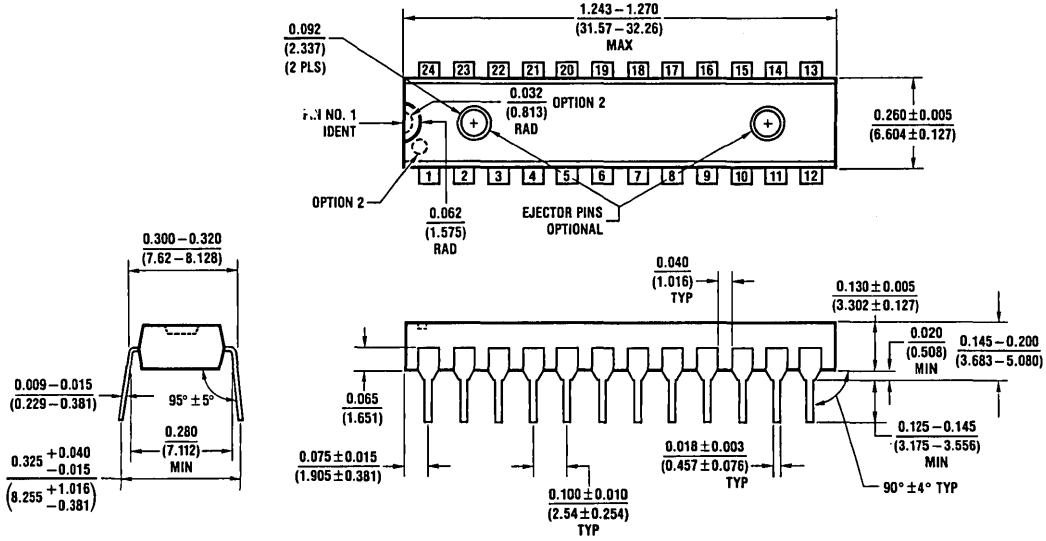


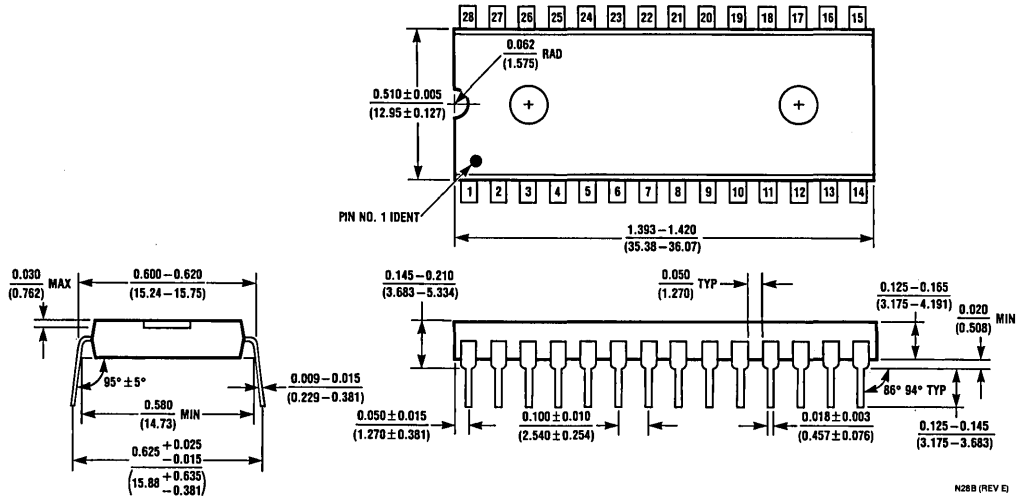
N24A (REV E)

24 Lead Plastic Slim (0.300″ Wide) Dual-In-Line Package
NS Package Number N24C

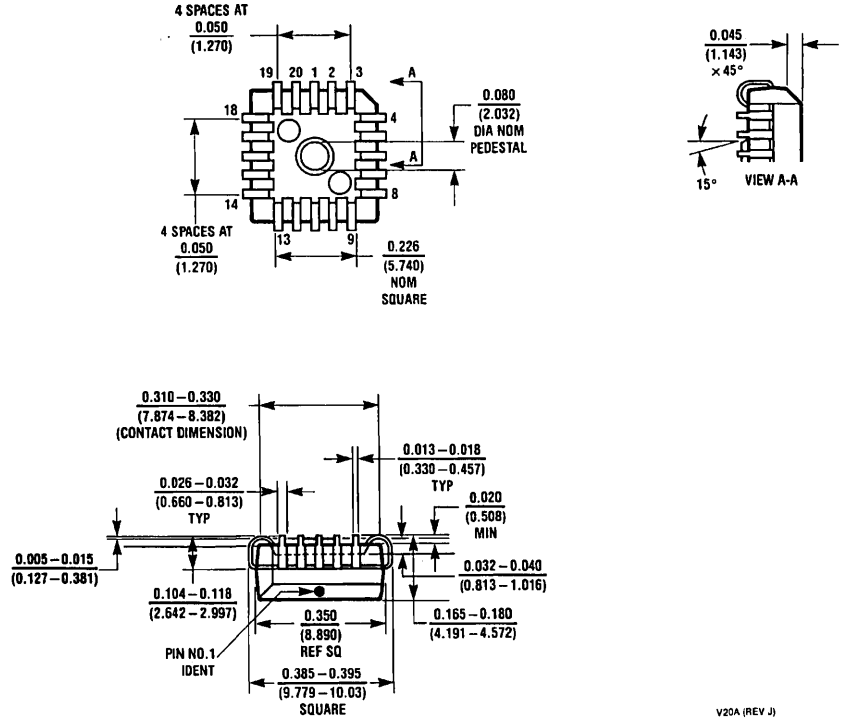


N24C (REV F)

28 Lead Plastic Dual-In-Line Package
NS Package Number N28B



20 Lead Plastic Chip Carrier
NS Package Number V20A



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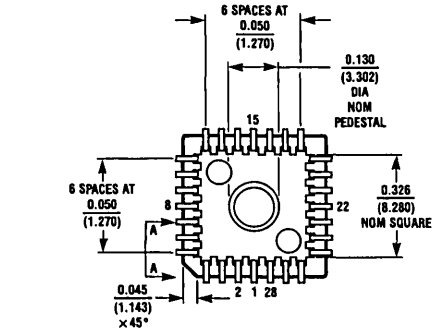

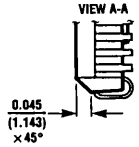

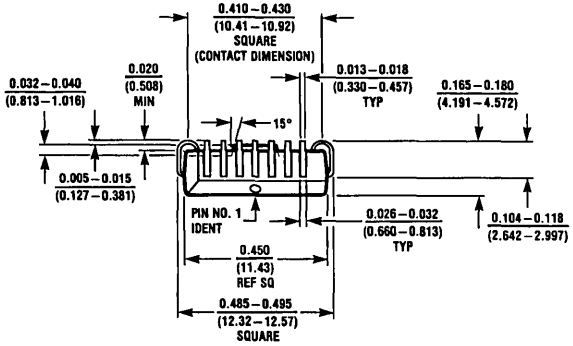

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