400069

National Semiconductor

Memory Databook

MEMORY
DATABOOK

1992 Edition

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New Products for 1992

EPROMs

68040 Compatible EPROM

Brief Description: This device can interface directly with Motorola's 68040 Microprocessor to allow for speed maximization while reducing the number of glue logic devices, thus reducing system cost.

Low Voltage EPROMs

Brief Description: These devices operate at 3V for low power consumption, and have JEDEC standard pinouts. These devices are ideal for handheld applications.

2 Megabyte EPROM

Brief Description: This device is a high performance device that possesses two megabytes of NV memory, and has JEDEC standard pinout.

EEPROMs

16K MICROWIRE™ EEPROM

Brief Description: The NM93C86A can be configured either x8 or x16 and offers 16K of NV memory. This device will be offered in an 8-pin small-outline (SO) package for minimal space usage.

16K MICROWIRE EEPROM

Brief Description: The NM59C16 can be configured either x8 or x16, can be monitored for programming status by monitoring the RDY/BUSY pin and offers 16K of NV memory. This device will be offered in an 8-pin small-outline (SO) package for minimal space usage.

2K/4K Extended Low Voltage I²C EEPROM

Brief Description: These devices operate on an I²C 2-wire bus and operate in an extended voltage range of 2.5V to 5.5V.

4K SPI™ EEPROM

Brief Description: These devices are designed for data storage in applications requiring both non-volatile memory and in-system data updates.

Note: For device status and availability, contact your local sales office.

Memory Databook Introduction

National Semiconductor's Memory Databook is a comprehensive collection of information on advanced memory products intended to meet the needs of virtually every electronic system. We are committed to designing and providing state-of-the-art non-volatile EPROM and EEPROM solutions. National's EPROM families—Standard Products, Processor Oriented ePROMs, 5V Low Current and Low Voltage (3V), along with our EEPROM families—MICROWIRE™ and I²C, are designed to do just that.

National Semiconductor's EPROM families are suited to meet a variety of customer needs. The Standard Product EPROMs are industry compliant JEDEC parts. Yet, a standard EPROM does not meet the needs of every electronic system. To meet these needs, National provides other families such as the Low Current 5V family which has low I_{CC} for power sensitive applications, Low Voltage EPROMs for newly emerging portable hand-held markets, and Processor Oriented ePROMs (POP™) which are designed to fully utilize microprocessor features which increase data throughput.

National Semiconductor's EEPROM families are also suited to provide any solution in serial EEPROM. Different microcontrollers provide various serial interfaces. National, the industry leader, is setting the standard again! The MICROWIRE interface is the industry standard. We have expanded our offering to also include the I²C interface for consumer electronics, and SPI™ for automotive and telecommunication.

National Semiconductor is committed to excellence in design, manufacturing, reliability, and service to our customers through the continuing development of new products and technologies. As new information and devices become available, individual new datasheets will be issued. For the most current information, please contact your local National Semiconductor sales office or distributor.

Look to National for long term support for your memory needs!

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Section 1

CMOS EPROMs

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National Semiconductor

CMOS EPROM Selection Guide
Standard Products

General Description

National Semiconductor's family of high performance CMOS EPROMs offer the following shared features: pin compatibility with byte-wide JEDEC EPROMs; "Don't Care" feature during read operations; high speed operation with high performance CPUs such as the 80186, 68020, 80386; single chip solutions for the code storage requirements of 100% firmware based equipment.

A feature not shared by all family members is found in the NMC87C257—address latches for direct interfacing with address/data multiplexed microprocessors. Other differences are memory size, speed, packaging and operating temperature range.

Features

- High performance CMOS
  - 100 ns access time
- Fast programming
- EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection exceeds 2000V
- Compatible with JEDEC EPROM configurations
- Simplified upgrade path
  - V_{PP} and PGM are "Don't Care" during normal read operation
- Single 5V power supply

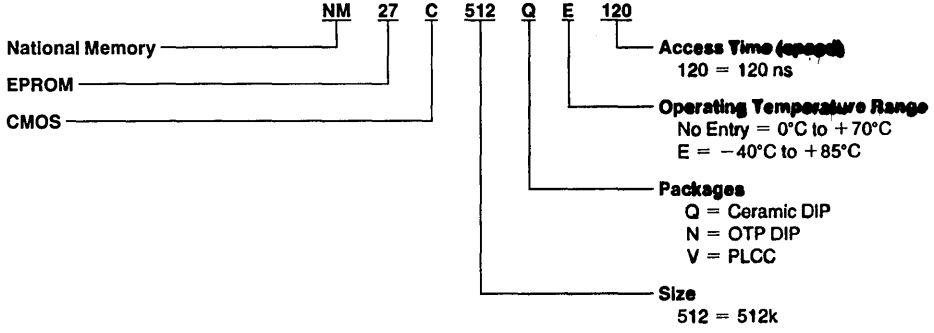
Available Product

	Packages	Temperature Ranges	Speed
NMC27C16B	Q	C, E	150 ns, 200 ns
NMC27C32B	Q	C, E	200 ns
NMC27C64	Q, N	C, E, M*	150 ns, 200 ns
NM27C128	Q, N	C, E	200 ns, 250 ns
NM27C256	Q, V, N	C, E	100 ns, 120 ns, 150 ns, 200 ns
NM27C512	Q, V, N	C, E	120 ns, 150 ns, 200 ns
NM27C010	Q, V, N	C, E	120 ns, 150 ns, 200 ns
NM27C210	Q, V	C, E	120 ns, 150 ns, 200 ns
NM27C040	Q	C, E	150 ns, 170 ns, 200 ns

*N package available only in commercial temperature range (0°C to +70°C).

Note: All products will operate at speeds slower than those listed.

Ordering Information



National Semiconductor

NMC27C16B 16,384-Bit (2048 x 8) CMOS EPROM

General Description

The NMC27C16B is a high performance 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

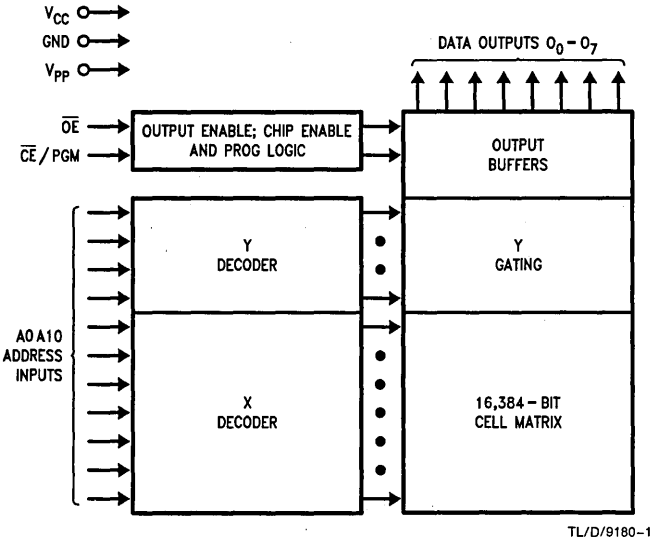
The NMC27C16B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  Active power: 55 mW max
  Standby power: 0.55 mW max (99% savings)
- Optimal EPROM for total CMOS systems
- Extended temperature range available,
  −40°C to +85°C
- Fast and reliable programming (100 μs for most bytes)
- TTL compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming equipment
- High current CMOS level output drivers
- Upgrade for NMOS 2716

Block Diagram



TL/D/9180–1

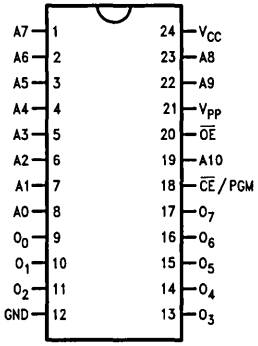
Pin Names

A0–A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
PGM	Program
NC	No Connect

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C16B
Dual-In-Line Package



TL/D/9180–2

Top View

27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$	V_{CC} A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16B pins.

Order Number NMC27C16BQ
See NS Package Number J24AQ

Commercial Temp. Range (0°C to 70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQ150	150
NMC27C16BQ200	200

Extended Temp. Range (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQE150	150
NMC27C16BQE200	200

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	
Commercial Parts	−10°C to +80°C
Extended Temp. Parts	−40°C to +85°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply and A9 Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C

Operating Conditions (Note 8)

Temperature Range	
NMC27C16BQ150, 200	0°C to +70°C
NMC27C16BQE150, 200	−40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 11)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.1	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.1	1	μA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	V_{PP} = 5.5V			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 mA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C16BQ				Units
			Q150, QE150		Q200, QE200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{OE} = \overline{OE} = V_{IL}$	0		0		ns

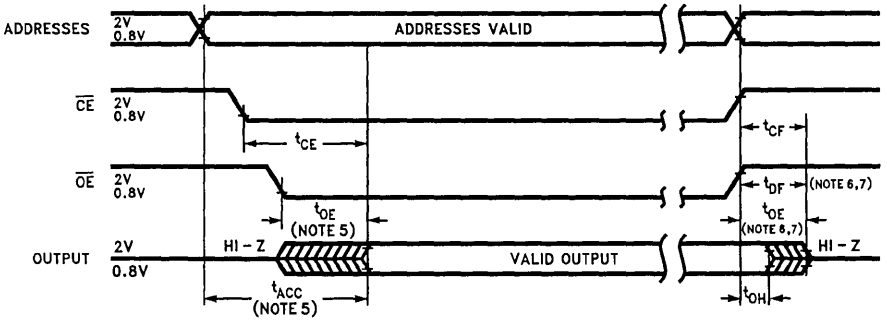
Capacitance $T_A = +25°C, f = 1$ MHz (Note 4)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load (Note 12)	1 TTL Gate and $C_L = 100$ pF	Timing Measurement Reference Level	
Input Rise and Fall Times	≤ 5 ns	Inputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms (Notes 2 & 9)



TL/D/9180-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} ≤ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: This parameter is only sampled and is not 100% tested.

Note 5: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 6: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 7: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 8: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 9: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns maximum.

Note 11: Typical values are for $T_A = 25°C$ and nominal supply voltages.

Note 12: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = 400$ μA.
C_L: 100 pF inlcudes fixture capacitance.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$/PGM = V_{IL}	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}$/PGM = V_{IL}			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IH}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		3.0	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

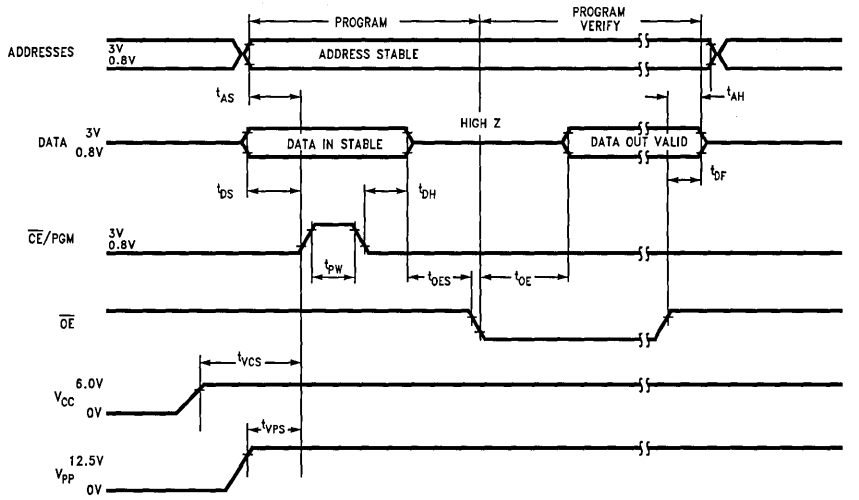
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

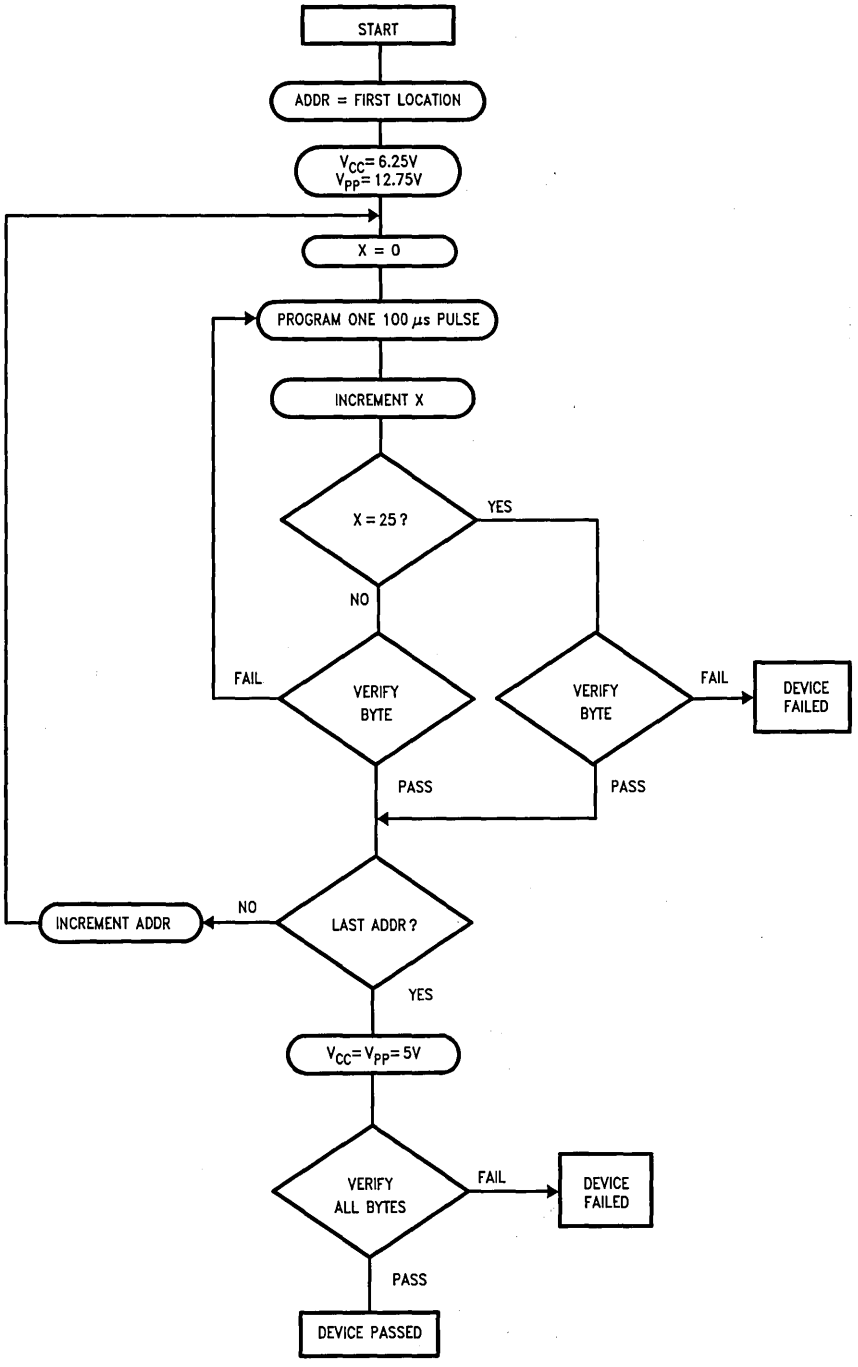
Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms



TL/D/9180-4

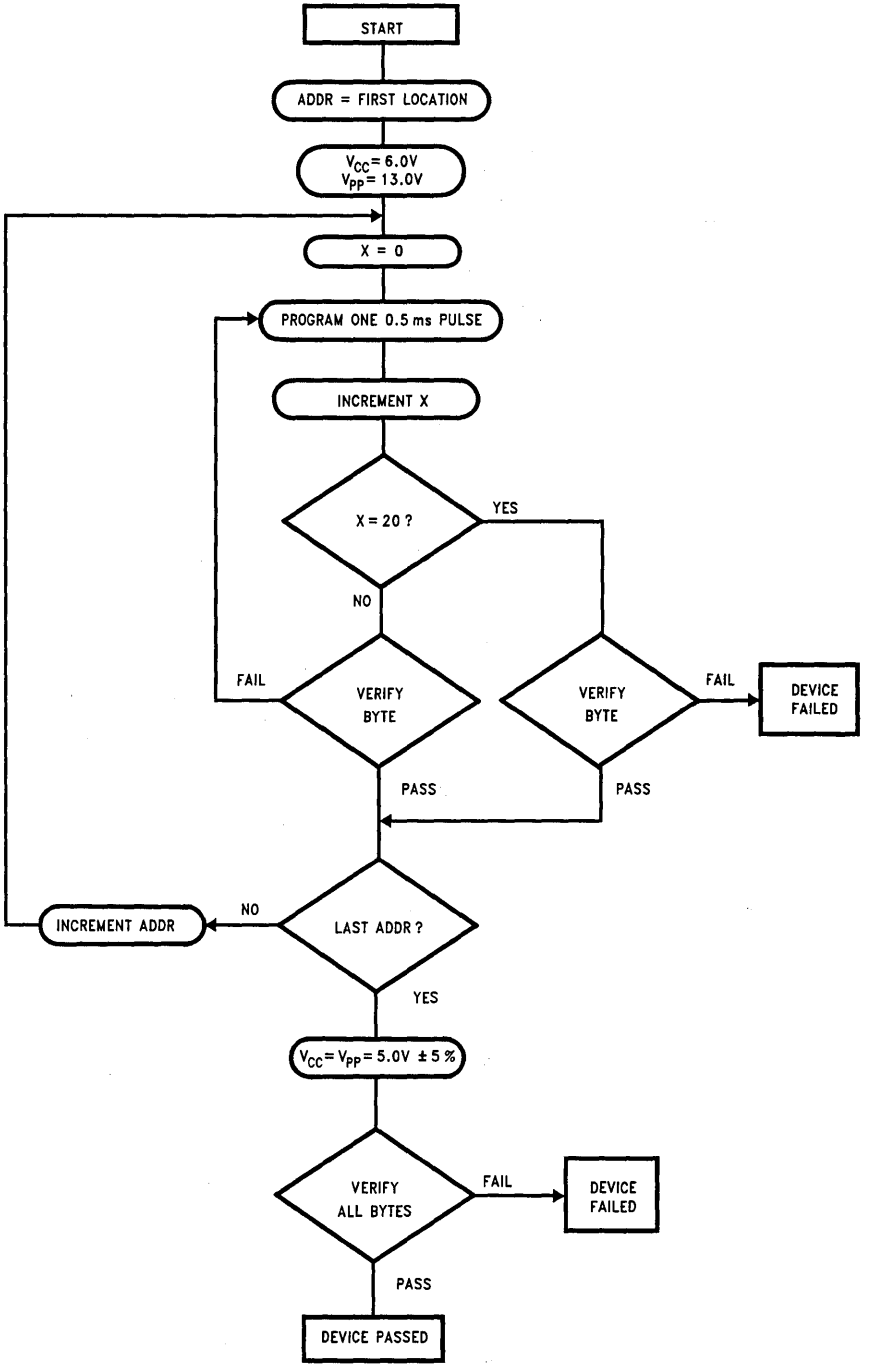
Fast Programming Algorithm Flow Chart (Note 4)



TL/D/9180–5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)



TL/D/9180–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C16B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC27C16B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C16B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C16B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 21 (V_{PP}) will damage the NMC27C16B.

Initially, and after each erasure, all bits of the NMC27C16B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins.

When the address and data are stable, an active high, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C16B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

The NMC27C16B must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming multiple NMC27C16Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16Bs may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled NMC27C16Bs.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11), (13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{CC}	5	Hi-Z
Program	V_{IH}	V_{IH}	12.75V	6.25	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	12.75V	6.25	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C16Bs in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM all like inputs (including $\overline{OE}$) of the parallel NMC27C16Bs may be common. A TTL high level program pulse applied to an NMC27C16B's $\overline{CE}$/PGM input with V_{PP} at 12.75V will program that NMC27C16B. A TTL low level $\overline{CE}$/PGM input inhibits the other NMC27C16Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. Except during programming and program verify, V_{PP} must be at V_{CC}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C16B has a manufacturer's identification code to aid in programming. The code, shown in Table III, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C16B is, "8F80", where "8F" designates that it is made by National Semiconductor, and "80" designates a 16k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C16B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a mimimum of 15 W-sec/cm^2.

The NMC27C16B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C16B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C16B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

TABLE III. Manufacturer's Identification Code

Pins	A_0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

National Semiconductor

NMC27C32B
32,768-Bit (4096 x 8)
CMOS EPROM

General Description

The NMC27C32B is a 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance.

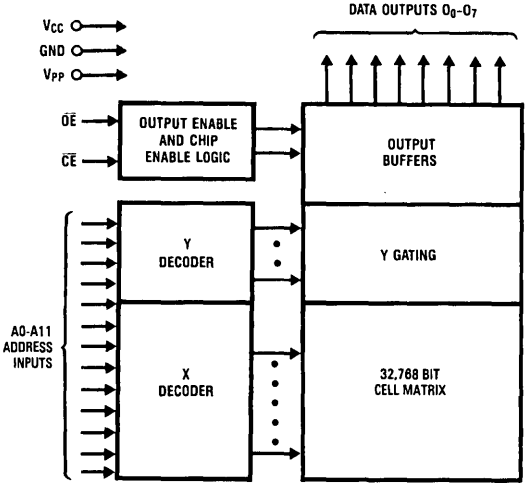
The NMC27C32B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  - — Active Power 55 mW Max
  - — Standby Power 0.55 mW Max
- Extended temperature range, −40°C to +85°C, available
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers
- Compatible with NMOS 2732

Block Diagram



TL/D/6827-1

Pin Names

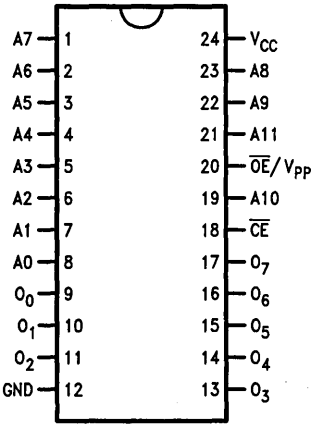
A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O_0–O_7	Outputs
V_{CC}	Power Supply
GND	Ground

1

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32B
Dual-In-Line Package



TL/D/8827–2

27C16 2716	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
V_{PP}	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pins.

Order Number NMC27C32BQ
See NS Package Number J24AQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ150	150
NMC27C32BQ200	200
NMC27C32BQ250	250

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−40°C to +85°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}$ V_{PP} Supply and A9 Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	
NMC27C32BQ150, 200, 250	0°C to +70°C
NMC27C32BQE200	−40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{PP}	$\overline{OE}/V_{PP}$ Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B						Units
			Q150		Q200, QE200		Q250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	0	70	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

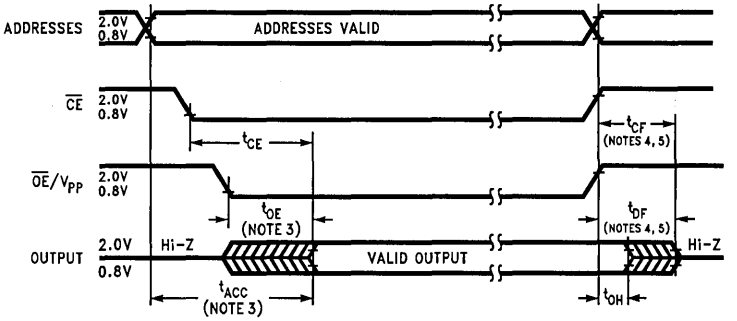
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	16	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

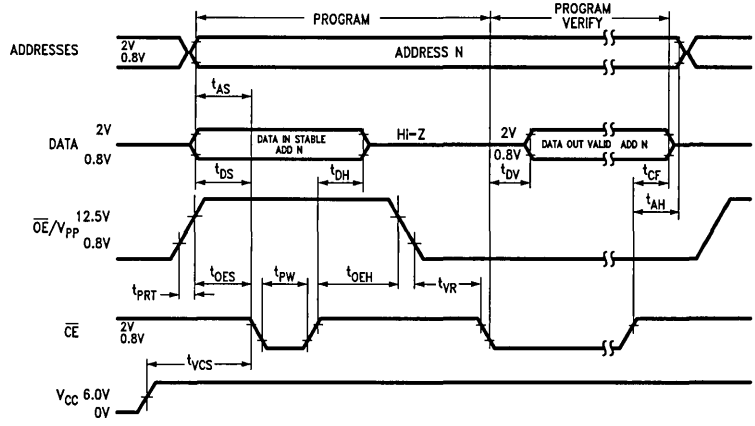
Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max, except for $\overline{OE}/V_{PP}$ which cannot exceed −0.2V.

Note 10: Typical values are for $T_A = 25°C$ and nominal supply voltages.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms



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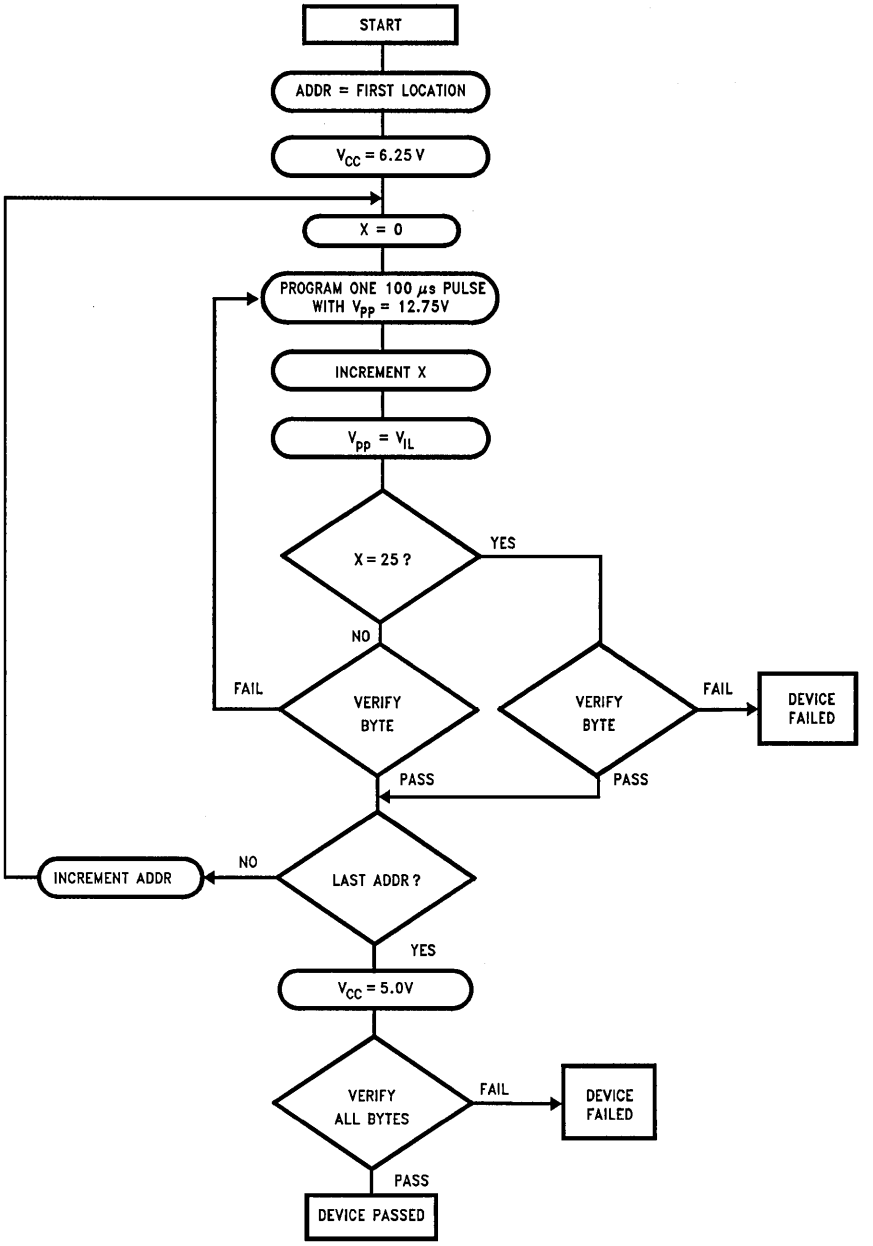
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 4)



TL/D/8827–5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

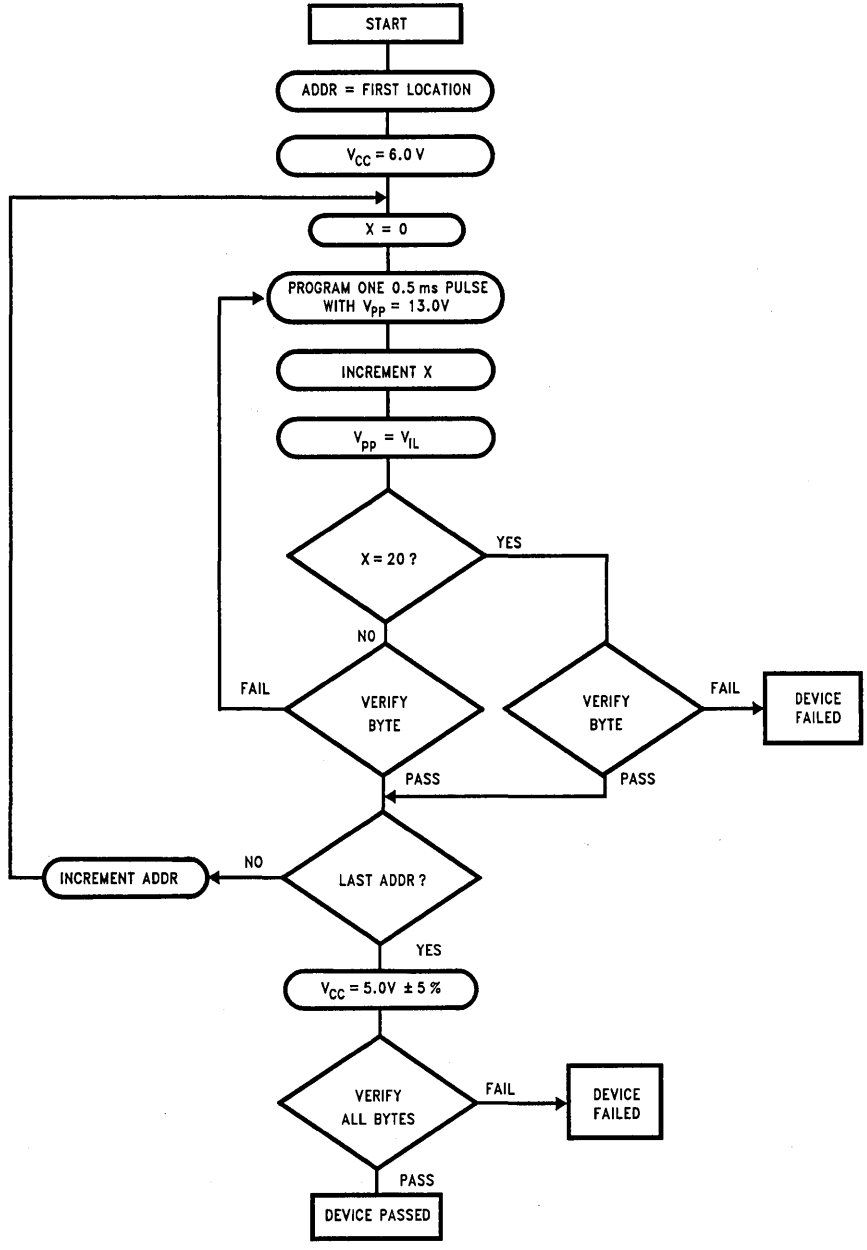


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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C32B are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a. The lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 20 $\overline{OE}/V_{PP}$ will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C32B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

The NMC27C32B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32B.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C32B may be common. A TTL low level program pulse applied to an NMC27C32B's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C32B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C32B from being programmed.

Program Verify

A verify should be performed on the programmed bit to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F01", where "8F" designates that it is made by National Semiconductor, and "01" designates a 32k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C32B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	0	1	01

TABLE III. Minimum NMC27C32B Erasure Time

Light Intensity (μW/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NMC27C64
65,536-Bit (8192 x 8) CMOS EPROM

General Description

The NMC27C64 is a 64K UV erasable, electrically reprogrammable and one-time programmable (OTP) CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

The NMC27C64Q is packaged in a 28-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

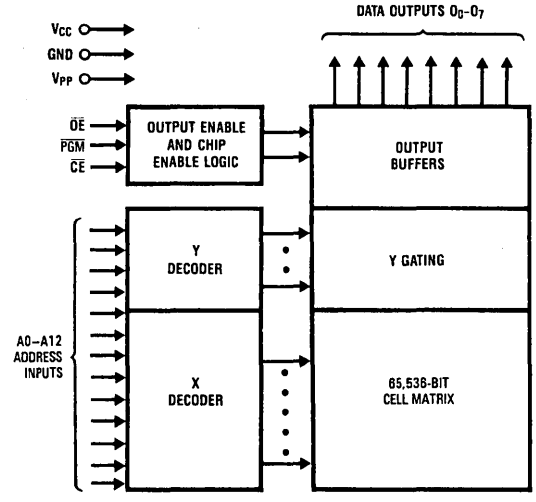
The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be one once.

This family of EPROMs are fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- High performance CMOS
  - 120 ns access time
- High reliability with EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection exceeds 2000V
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier
- Drop-in replacement for 27C64 or 2764
- Manufacturers identification code

Block Diagram



TL/D/8634-1

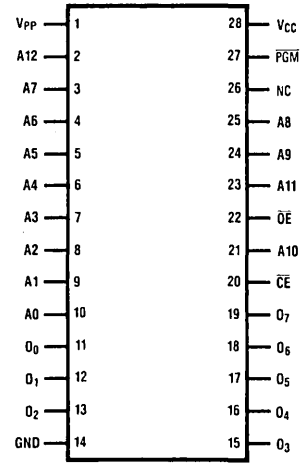
Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power Supply
GND	Ground

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C64Q/N
Dual-In-Line Package



TL/D/8634-2

27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

Commercial Temperature Range
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q, N150	150
NMC27C64Q, N200	200
NMC27C64Q, N250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE150	150
NMC27C64QE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QM200	200
NMC27C64QM250	250

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q15, Q150, 200, 250	0°C to +70°C
NMC27C64N150, 200, 250	
NMC27C64QE150, 200	−40°C to +85°C
NMC27C64QM200, M250	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64Q/N						Units
			15, 150, E150		200, E200, M200		250, M250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 2) NMC27C64Q

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

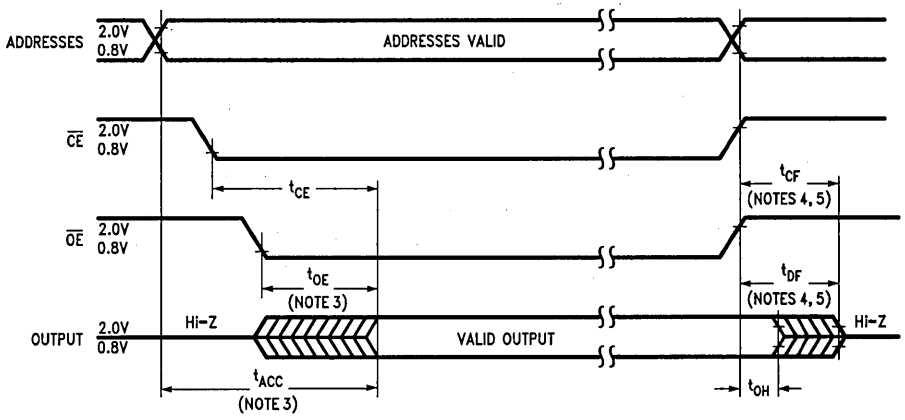
Capacitance T_A = +25°C, f = 1 MHz (Note 2) NMC27C64N

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

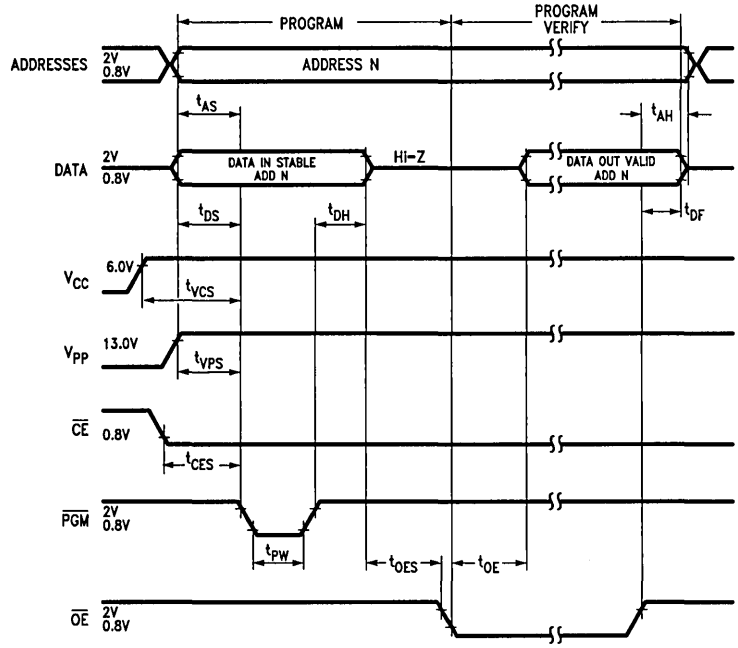
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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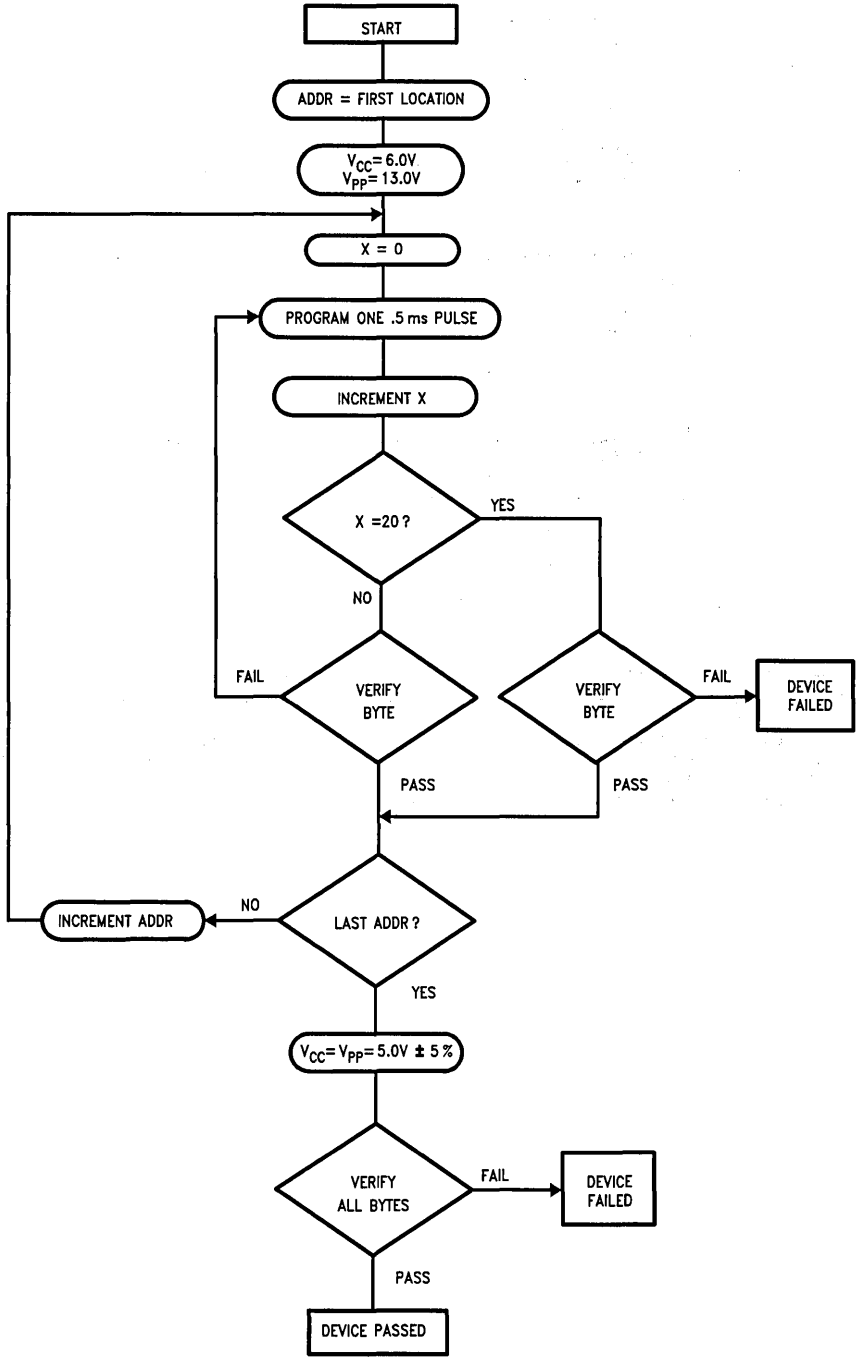
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

Interactive Programming Algorithm Flow Chart



TL/D/8634–5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s. If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's PGM input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C64 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NM27C128
131,072-Bit (16K x 8) High Performance CMOS EPROM

General Description

The NM27C128 is a high performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with National's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 100 ns access time over the full operating range. (If faster speeds are required, contact your National sales representative.)

The NM27C128 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 100ns access time provides high speed operation with high-performance CPUs. The NM27C128 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

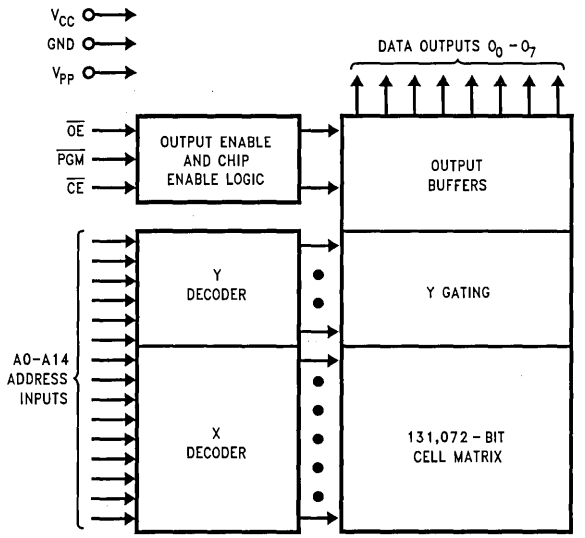
The NM27C128, is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C128 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - 100 ns access time
- Fast turn-off for microprocessor compatibility
- EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection exceeds 2000V
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier
- Drop-in replacement for 27C128 or 27128

Block Diagram

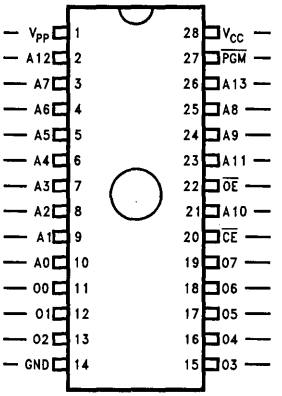


TL/D/11329-1

Connection Diagrams

27C080	27C040	27C020	27C010	27C512	27C256
A19	V_{PP}	V_{PP}	V_{PP}		
A16	A16	A16	A16		
A15	A15	A15	A15	A15	V_{PP}
A12	A12	A12	A12	A12	A12
A7	A7	A7	A7	A7	A7
A6	A6	A6	A6	A6	A6
A5	A5	A5	A5	A5	A5
A4	A4	A4	A4	A4	A4
A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2
A1	A1	A1	A1	A1	A1
A0	A0	A0	A0	A0	A0
O0	O0	O0	O0	O0	O0
O1	O1	O1	O1	O1	O1
O2	O2	O2	O2	O2	O2
GND	GND	GND	GND	GND	GND

DIP
NM27C128



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27C256	27C512	27C010	27C020	27C040	27C080
		V_{CC}	V_{CC}	V_{CC}	V_{CC}
		PGM	PGM	A18	A18
V_{CC}	V_{CC}	XX	A17	A17	A17
A14	A14	A14	A14	A14	A14
A13	A13	A13	A13	A13	A13
A8	A8	A8	A8	A8	A8
A9	A9	A9	A9	A9	A9
A11	A11	A11	A11	A11	A11
OE	OE/V_{PP}	OE	OE	OE	OE/V_{PP}
A10	A10	A10	A10	A10	A10
CE	CE/PGM	CE	CE	CE/PGM	CE/PGM
O7	O7	O7	O7	O7	O7
O6	O6	O6	O6	O6	O6
O5	O5	O5	O5	O5	O5
O4	O4	O4	O4	O4	O4
O3	O3	O3	O3	O3	O3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C128 pins.

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 Q, N, V 100	100
NM27C128 Q, N, V 120	120
NM27C128 Q, N, V 150	150
NM27C128 Q, N, V 200	200

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 QE, NE, VE 120	120
NM27C128 QE, NE, VE 150	150
NM27C128 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Military Temp. Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 QM 120	120
NM27C128 QM 150	150

Package Types: NM27C128 Q, N, V XXX

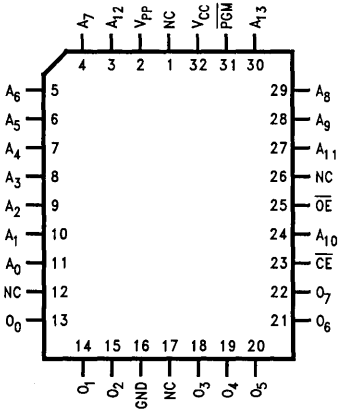
Q = Quartz-Windowed Ceramic DIP
N = Plastic OTP DIP
V = Surface-Mount PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

Symbol	Description
A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
NC	No Connect

PLCC



Top

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5		V
$I_{CC}SB1$	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ V_{IL} = GND ± 0.3V, $V_{IH} = V_{CC} \pm 0.3V$		100	μA
$I_{CC}SB2$	V_{CC} Standby Current (T^2L)	$\overline{CE} = V_{IH}$		1	mA
I_{CC1}	V_{CC} Active Current, T^2L Inputs	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz I/O = 0 mA		40	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA C,I Temp. Range		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	ns
t_{CF} (Note 2)	$\overline{CE}$ High to Output Float		30		45		55	ns
t_{DF} (Note 2)	$\overline{OE}$ High to Output Float		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

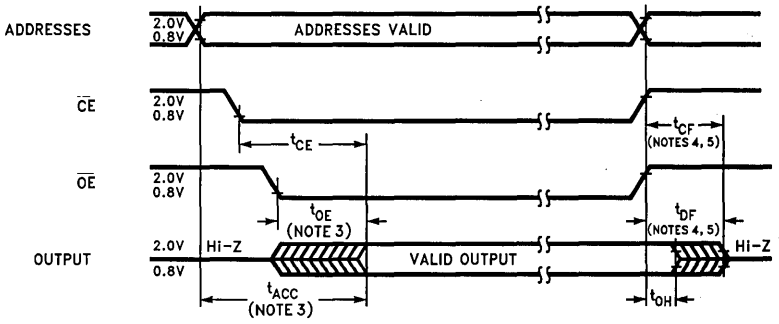
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45 to 2.4V
		Timing Measurement Reference Level	(Note 10)
Input Rise and Fall Times	≤ 5 ns	Inputs	0.8V and 2.0V
		Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

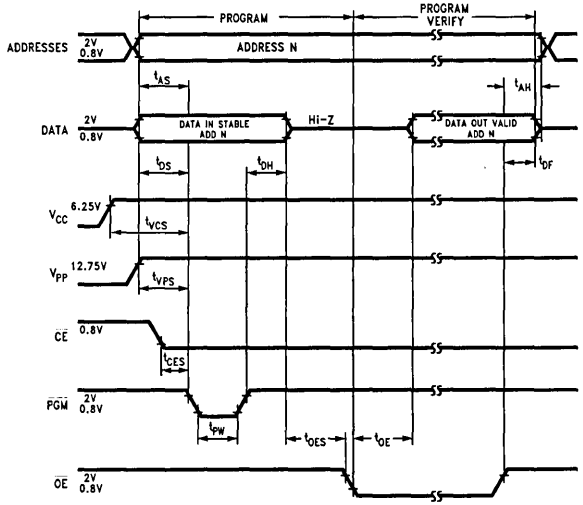
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart (Note 4)

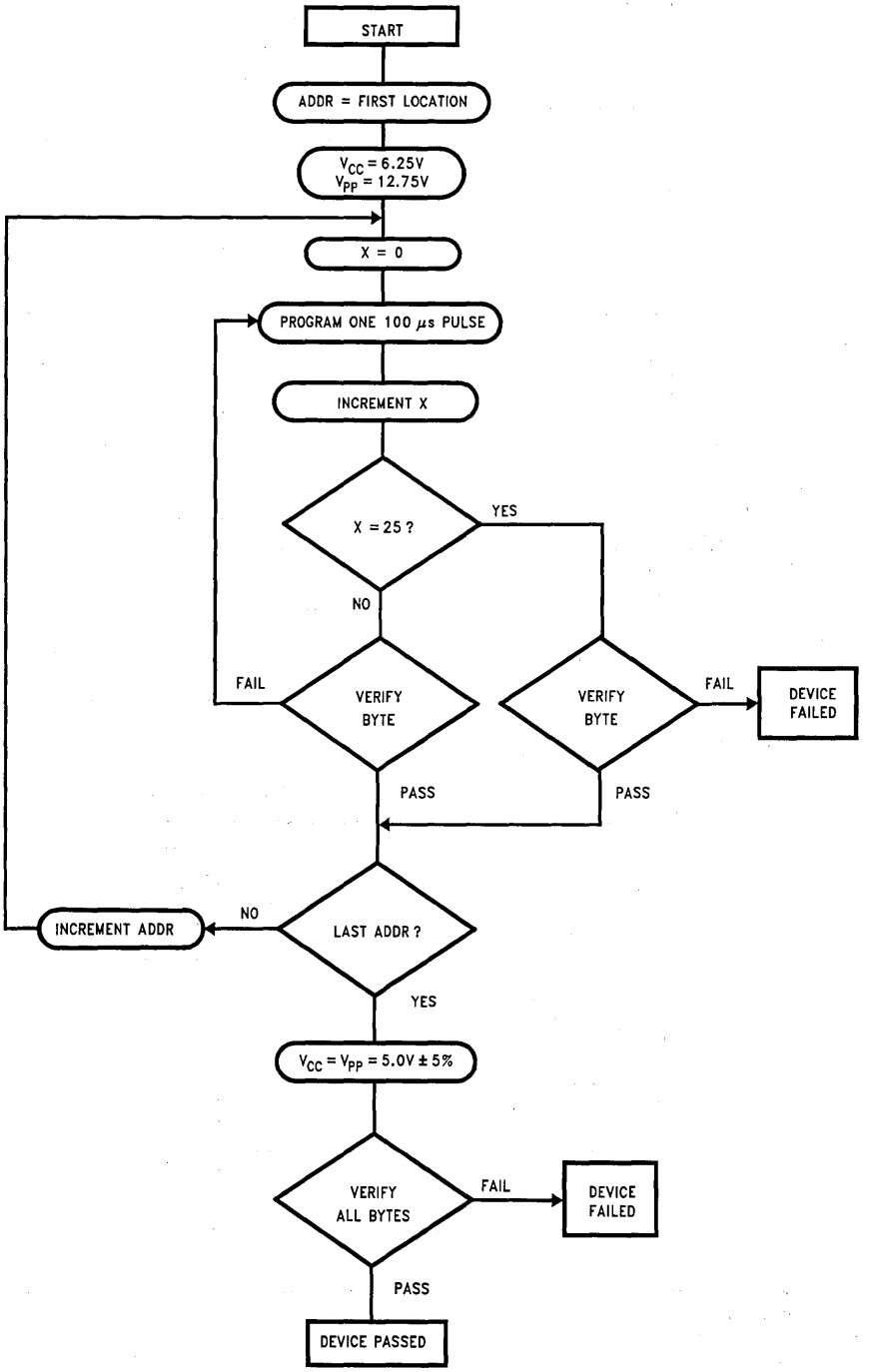

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

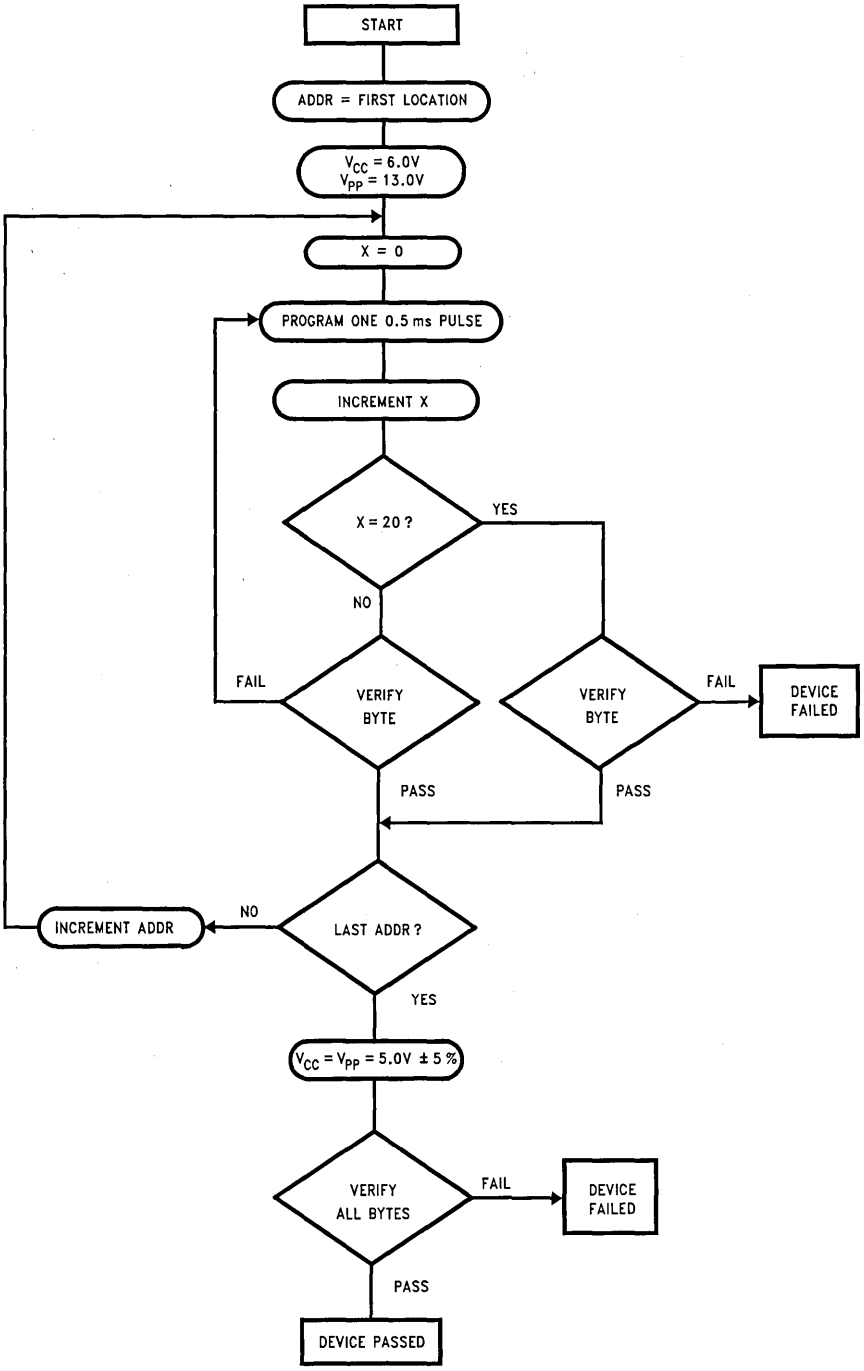

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V, $\overline{CE}$ is A7 V_{IL}, and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacture and device type. The code for NM27C128 is "8F83", where "8F" designates that it is made by National Semiconductor, and "83" designates a 128K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of NM27C128 listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5.0V	D_{OUT}
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High-Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	0	1	1	83

National Semiconductor

NM27C256
262,144-Bit (32K x 8) High Performance CMOS EPROM

General Description

The NM27C256 is a 256K Electrically Programmable Read Only Memory. It is manufactured in National's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 120 ns access time over the full operating range.

The NM27C256 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120 ns access time provides high speed operation with high-performance CPUs. The NM27C256 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

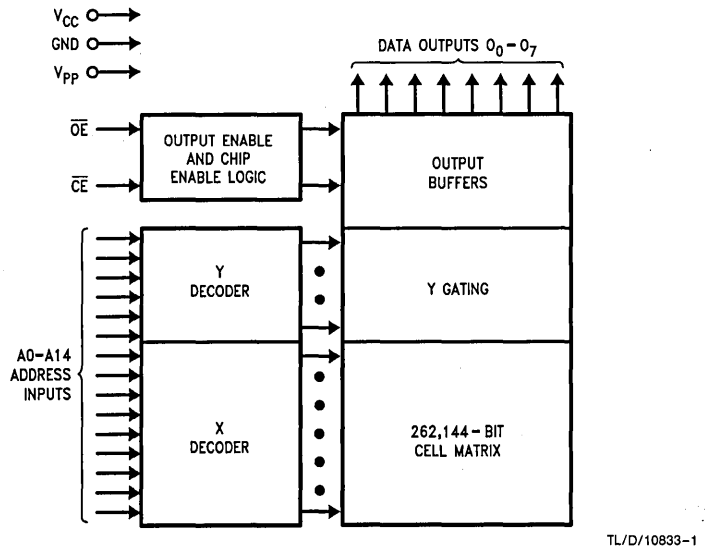
The NM27C256, is configured in the standard EPROM pin-out which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C256 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - 100 ns access time
- High reliability with EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection exceeds 2000V
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier
- Drop-in replacement for 27C256 or 27256
- Manufacturer's identification code

Block Diagram



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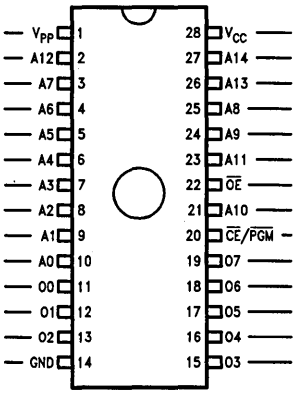
Connection Diagrams

27C080	27C040	27C020	27C010	27C512
A19	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A16	A16	A16	A16	
A15	A15	A15	A15	A15
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O0	O0	O0	O0	O0
O1	O1	O1	O1	O1
O2	O2	O2	O2	O2
GND	GND	GND	GND	GND

DIP
NM27C256



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27C512	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18	A18
V_{CC}	XX	A17	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}
A10	A10	A10	A10	A10
$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$/$\overline{PGM}$
O7	O7	O7	O7	O7
O6	O6	O6	O6	O6
O5	O5	O5	O5	O5
O4	O4	O4	O4	O4
O3	O3	O3	O3	O3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C256 pins.

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 Q, N, V 120	120
NM27C256 Q, N, V 150	150
NM27C256 Q, N, V 200	200

Military Temp. Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QM 150	150
NM27C256 QM 250	250

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QE, NE, VE 120	120
NM27C256 QE, NE, VE 150	150
NM27C256 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package Types: NM27C256 Q, N, V XXX

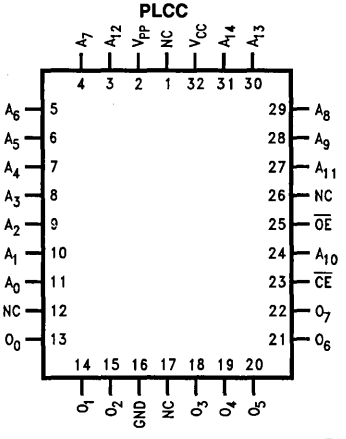
Q = Quartz-Windowed Ceramic DIP
N = Plastic OTP DIP
V = Surface-Mount PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

PLCC



Top

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	− 0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	3.5		V
I_{SB1} (Note 11)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$		100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}		40	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz, Inputs = V_{CC} or GND, I/O = 0 mA C, I Temperature Ranges		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	100		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		30		35		45		55	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

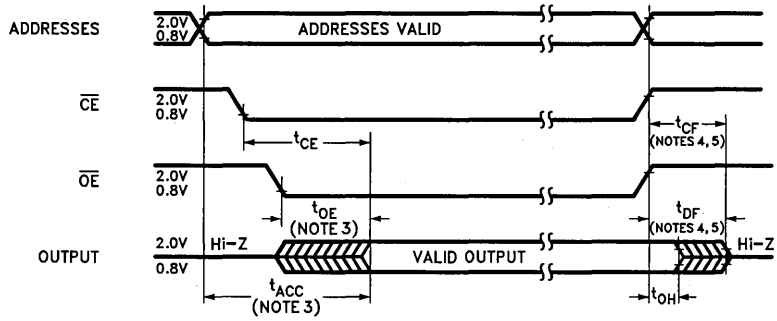
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45 to 2.4V
Timing Measurement Reference Level	(Note 10)
Inputs	0.8V and 2.0V
Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

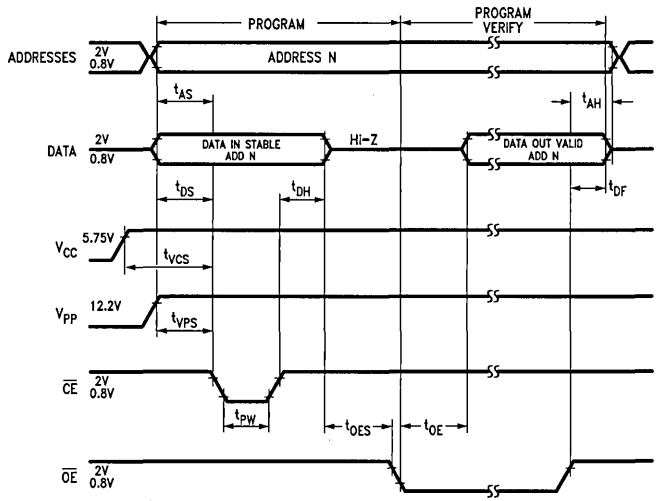
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS inputs: V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart (Same as NMC27C256B)

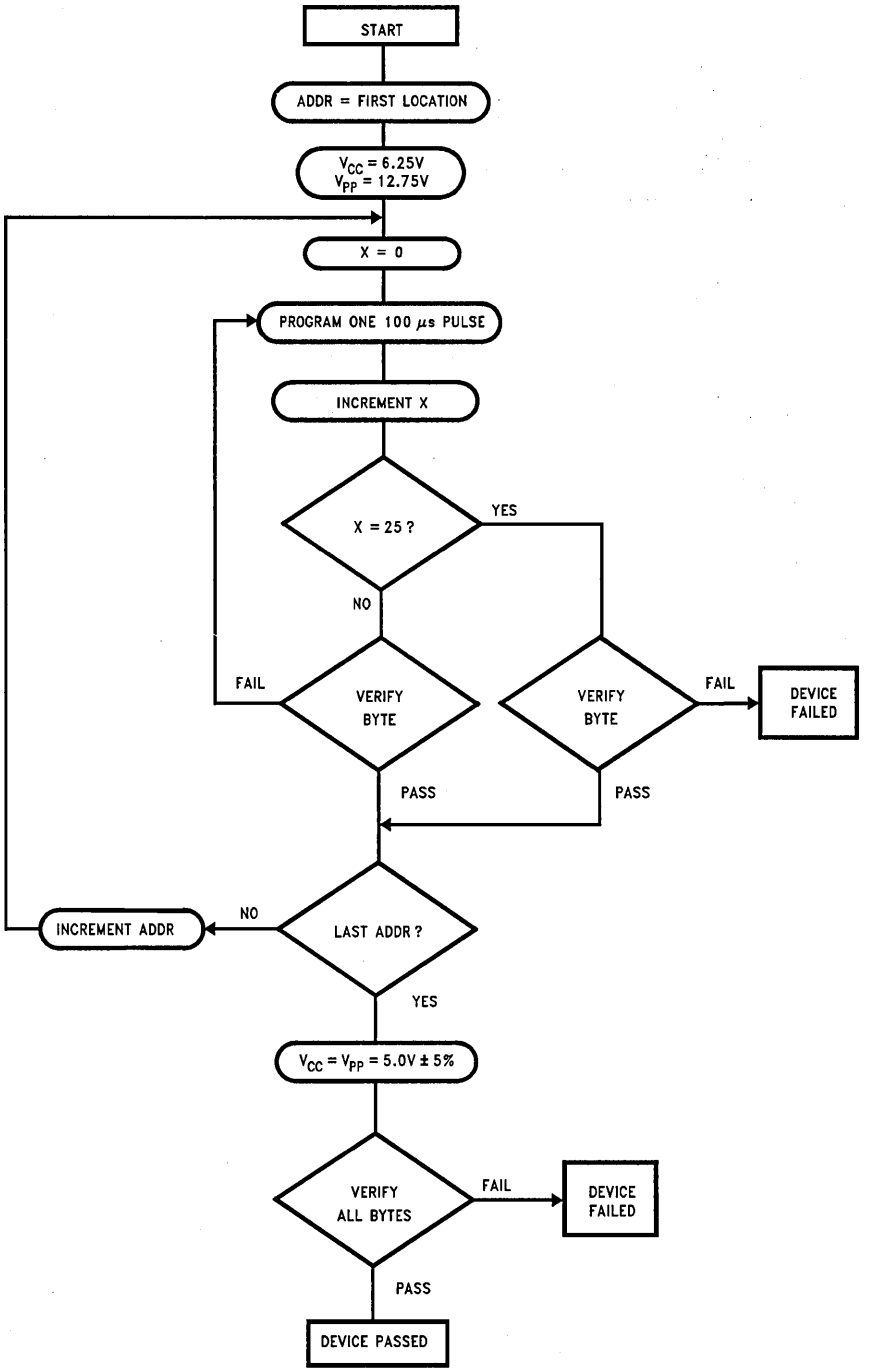

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

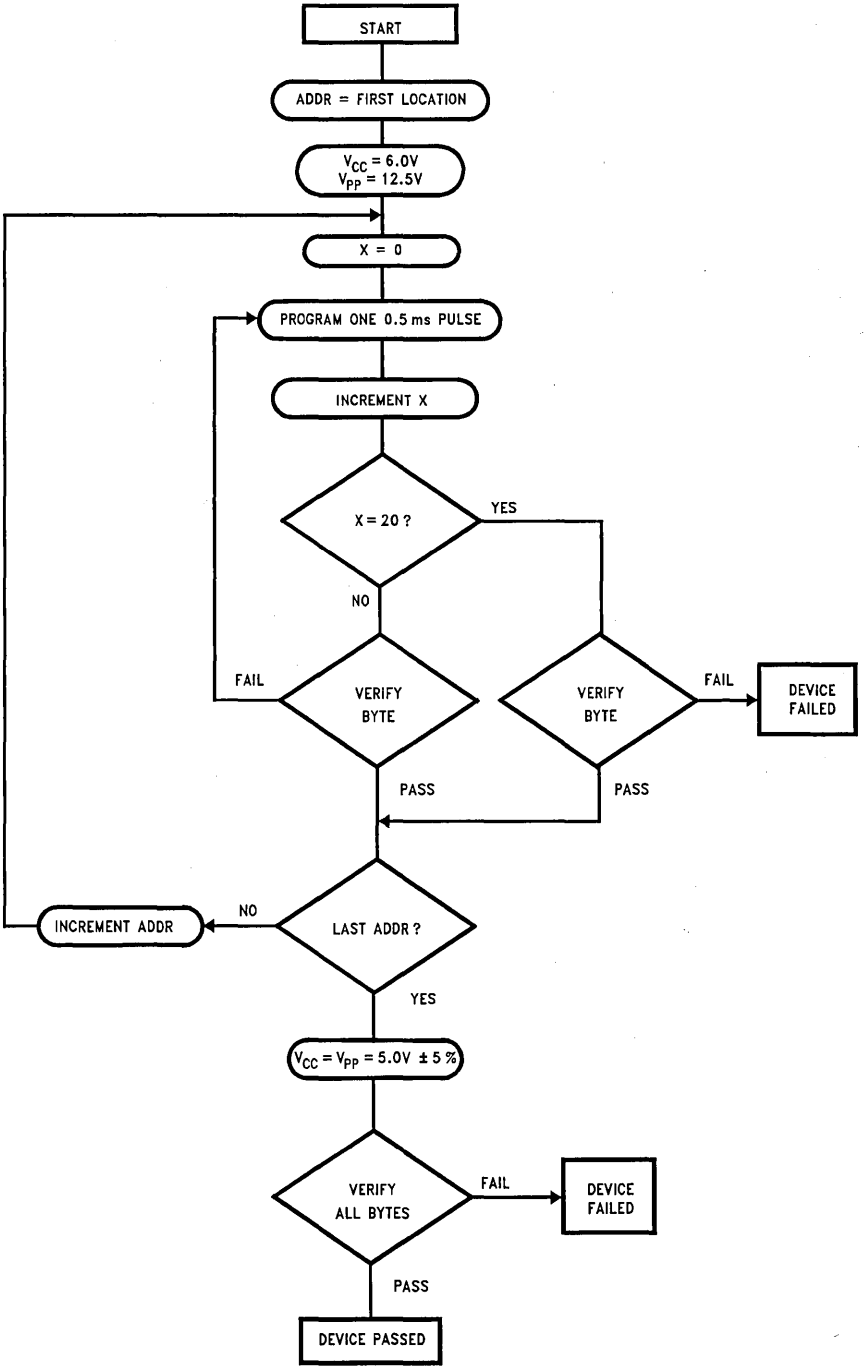

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE/PGM has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (including OE) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C256 is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of NM27C256 listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	V_{IH}X	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High-Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	0	0	04

National Semiconductor

NM27C512
524,288-Bit (64K x 8) High Performance CMOS EPROM

General Description

The NM27C512 is a high performance 512K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in National's latest CMOS split gate EPROM technology, which enables it to operate at speeds as fast as 120 ns access time over the full operating range.

The NM27C512 provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 120 ns access time provides no-wait-state operation with high-performance CPUs. The NM27C512 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

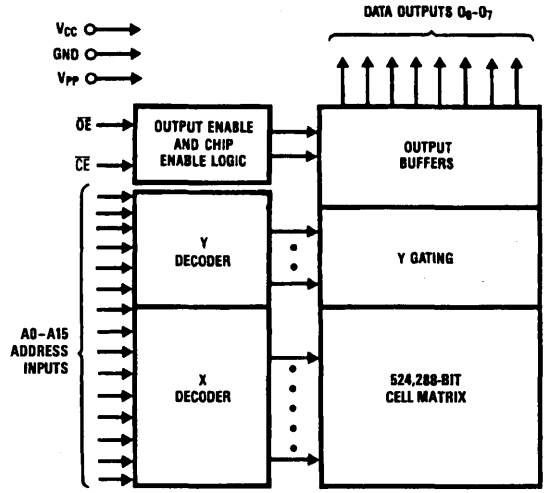
The NM27C512 is configured in the standard JEDEC EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C512 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - 120 ns access time
- Fast turn-off for microprocessor compatibility
- High reliability with EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection exceeds 2000V
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier
- Manufacturers identification code

Block Diagram



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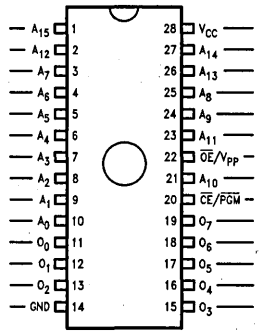
Connection Diagrams

27C080	27C040	27C020	27C010	27C256
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27C512



27C256	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/PGM	XX/PGM	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C512 pins.

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)*
NM27C512 Q, N, V 120	120
NM27C512 Q, N, V 150	150
NM27C512 Q, N, V 200	200

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Access Time (ns)*
NM27C512 QM 200	200

Extended Temp Range (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)*
NM27C512 QE, NE, VE 120	120
NM27C512 QE, NE, VE 150	150
NM27C512 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

*All versions are guaranteed to function for slower speeds.

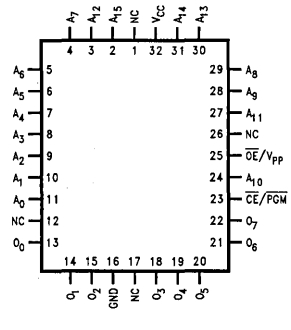
Package Types: NM27C512 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP Package
N = Plastic OTP DIP Package
V = PLCC Package

- All packages conform to the JEDEC standard.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PLCC



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature −65°C to +150°C

All Input Voltages Except A9 with Respect to Ground −0.6V to +7V

V_{PP} and A9 with Respect to Ground −0.7V to +14V

V_{CC} Supply Voltage with Respect to Ground −0.6V to +7V

ESD Protection (MIL Std. 883, Method 3015.2) >2000V

All Output Voltages with Respect to Ground V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	08	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V		100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}		1	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5 MHz		40	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz, Inputs = V_{CC} or GND, I/O = 0 mA, C, I Temp Ranges		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	μA
V_{PP}	V_{PP} Read Voltage		V_C − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics

Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF}	Output Disable to Output Float		25		45		55	
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

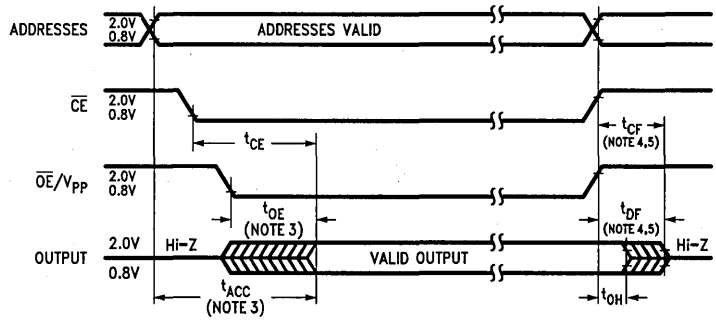
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 9)	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

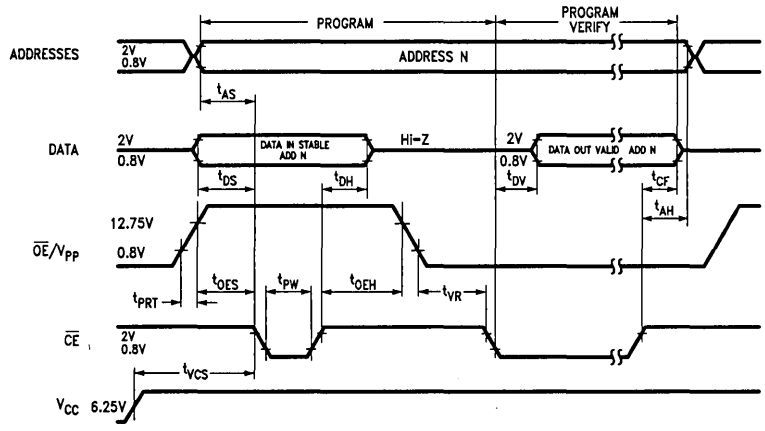
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1 and 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



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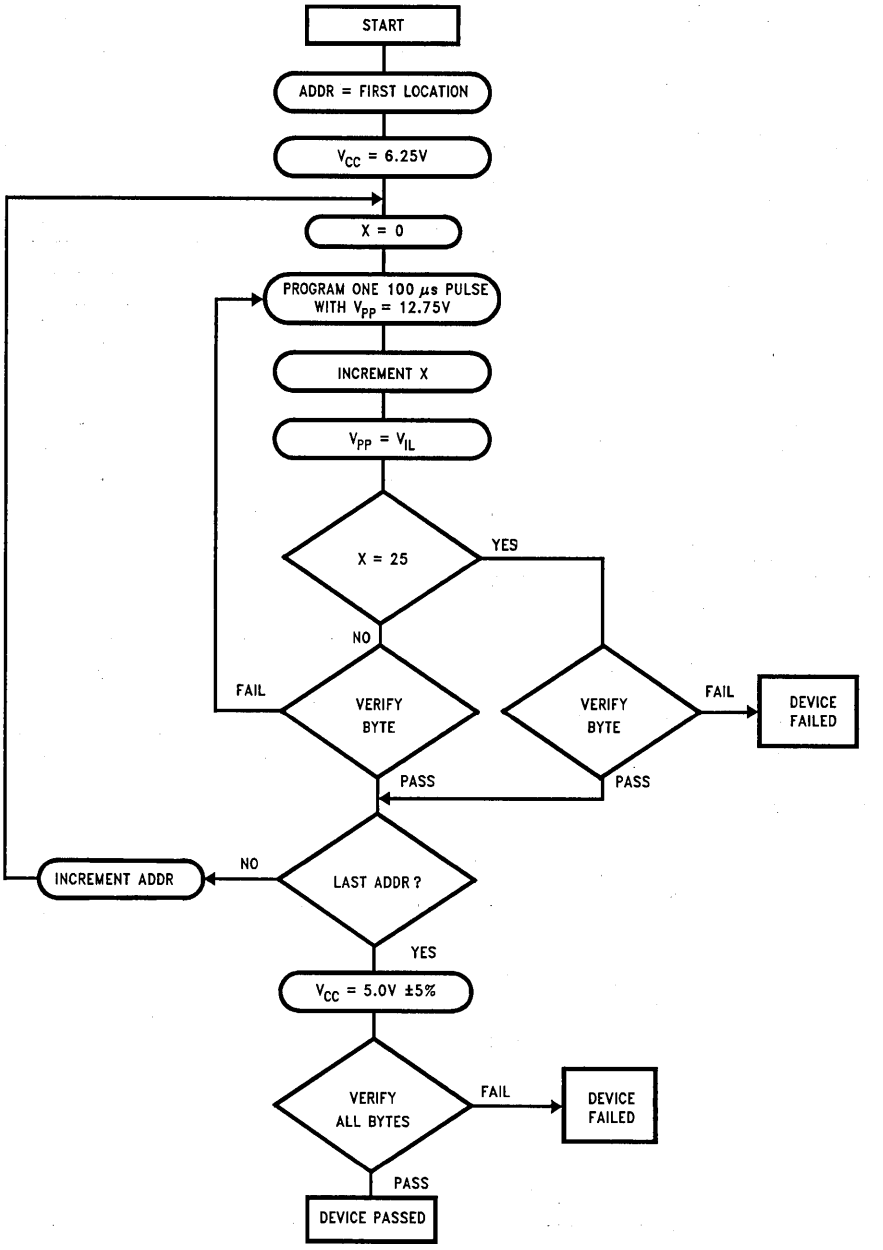
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Same as NMC27C512A)



TL/D/10834–6

FIGURE 1

Interactive Programming Algorithm Flow Chart

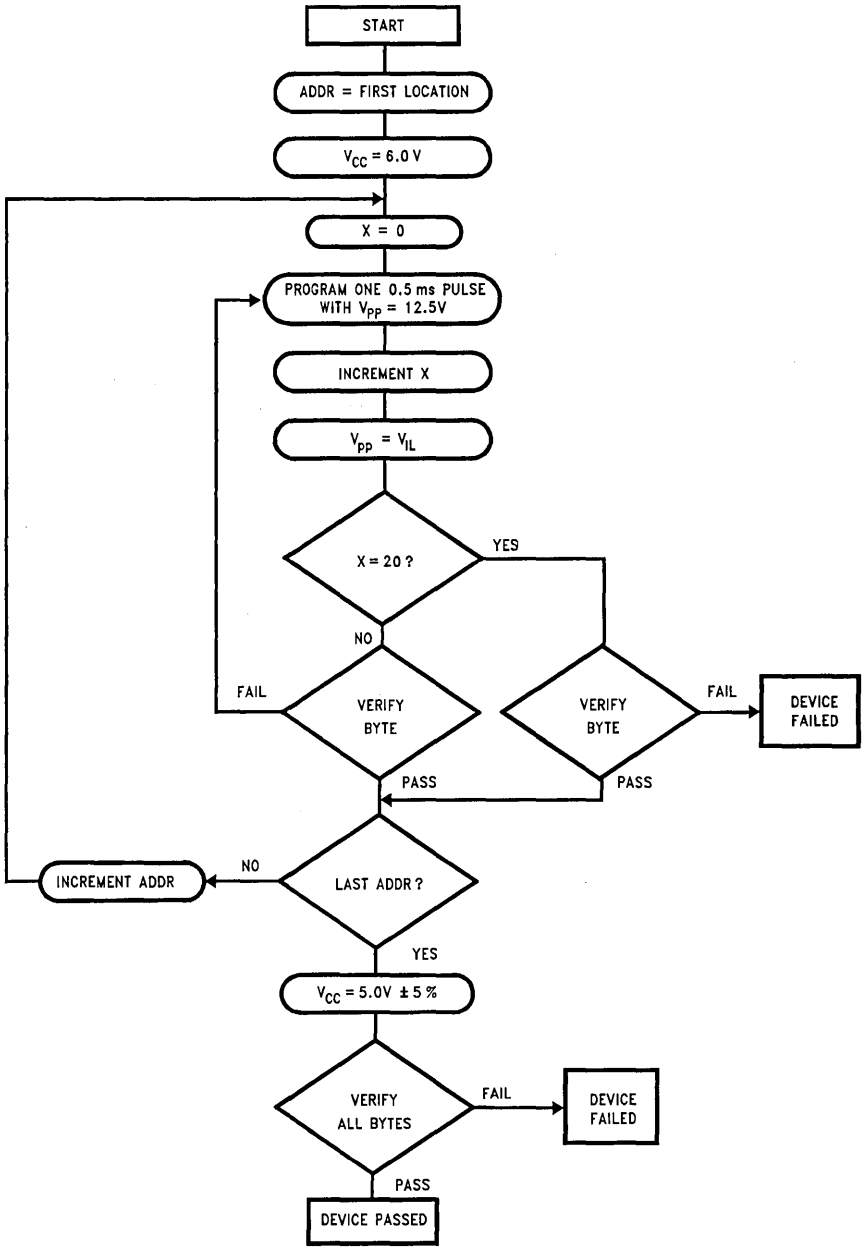


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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and OE/V_{PP}. The OE/V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE/V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (OE/V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE/V_{PP}) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with OE/V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with OE/V_{PP} and CE at V_{IL}. Data should be verified T_{DV} after the falling edge of CE.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C512 is "8F85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	V_{PP}(2)	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(2)	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

National Semiconductor

NM27C010
1,048,576-Bit (128K x 8) High Performance CMOS EPROM

General Description

The NM27C010 is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature during read operations allows memory expansions from 1M to 8M bits with no printed circuit board changes.

The NM27C010 can directly replace lower density 28-pin EPROMs by adding an A16 address line and V_{CC} jumper. During the normal read operation PGM and V_{PP} are in a "Don't Care" state which allows higher order addresses, such as A17, A18, and A19 to be connected without affecting the normal read operation. This allows memory upgrades to 8M bits without hardware changes. The NM27C010 is also offered in a 32-pin plastic DIP with the same upgrade path.

The NM27C010 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 100 ns access time provides no-wait-state operation with high-performance CPUs. The NM27C010 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

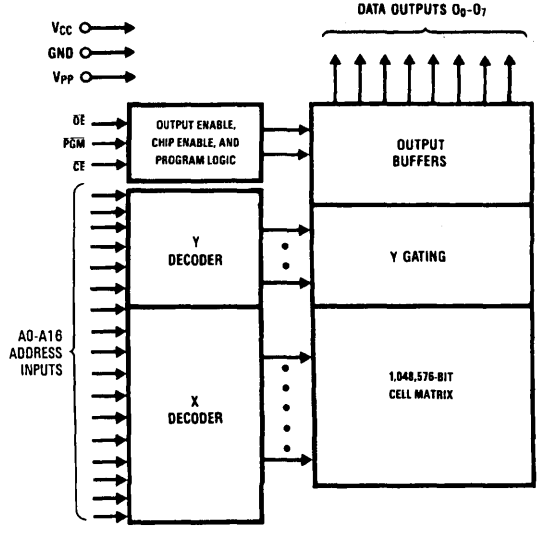
The NM27C010 is manufactured using National's advanced CMOS SVG EPROM technology.

The NM27C010 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - 100 ns access time
- Fast turn-off for microprocessor compatibility
- High reliability with EPI processing
  - Latch-up immunity
  - ESD protection
- Simplified upgrade path
  - V_{PP} and PGM are "Don't Care" during normal read operation
- Compatible with 27010 and 27C010 EPROMs
- JEDEC standard pin configurations
  - 32-pin DIP package
  - 32-pin chip carrier
- Manufacturers identification code
- Fast programming

Block Diagram



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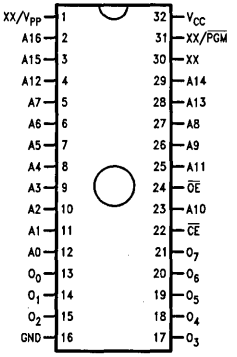
Connection Diagrams

DIP PIN CONFIGURATIONS

27C080	27C040	27C020	27C512	27C256
A19	XX/V_{PP}	XX/V_{PP}		
A16	A16	A16		
A15	A15	A15	A15	V_{PP}
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27C010



27C256	27C512	27C020	27C040	27C080
		V_{CC}	V_{CC}	V_{CC}
		XX/PGM	A18	A18
V_{CC}	V_{CC}	A17	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
OE	OE/V_{PP}	OE	OE	OE/V_{PP}
A10	A10	A10	A10	A10
CE/PGM	CE/PGM	CE	CE/PGM	CE/PGM
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C010 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 Q, V, N 100	100
NM27C010 Q, V, N 120	120
NM27C010 Q, V, N 150	150
NM27C010 Q, V, N 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 QE, VE, NE 120	120
NM27C010 QE, VE, NE 150	150
NM27C010 QE, VE, NE 200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 QM 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

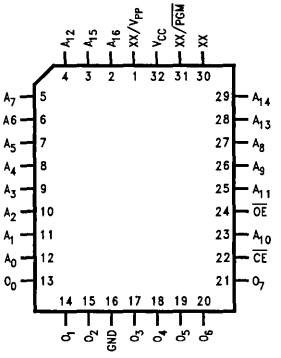
Package Types: NM27C010 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP package
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function at slower speeds.

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages Except A_9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A_9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	f = 5 MHz		50	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	100		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		45		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		35		35		45		55	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

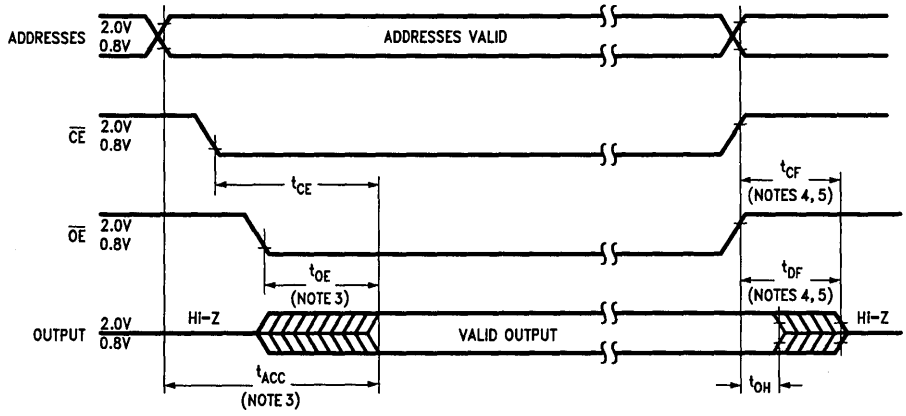
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

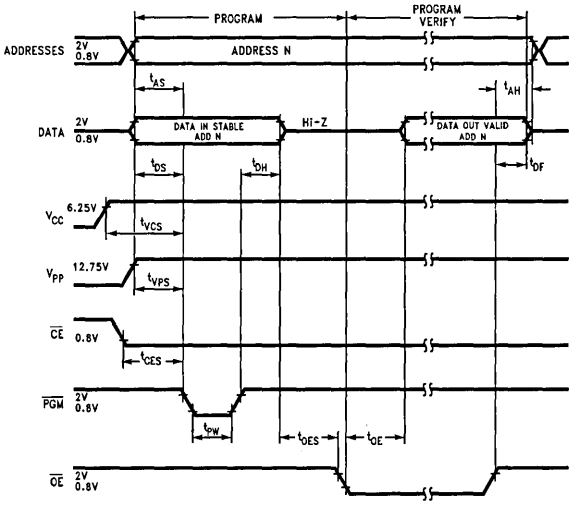
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4, & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

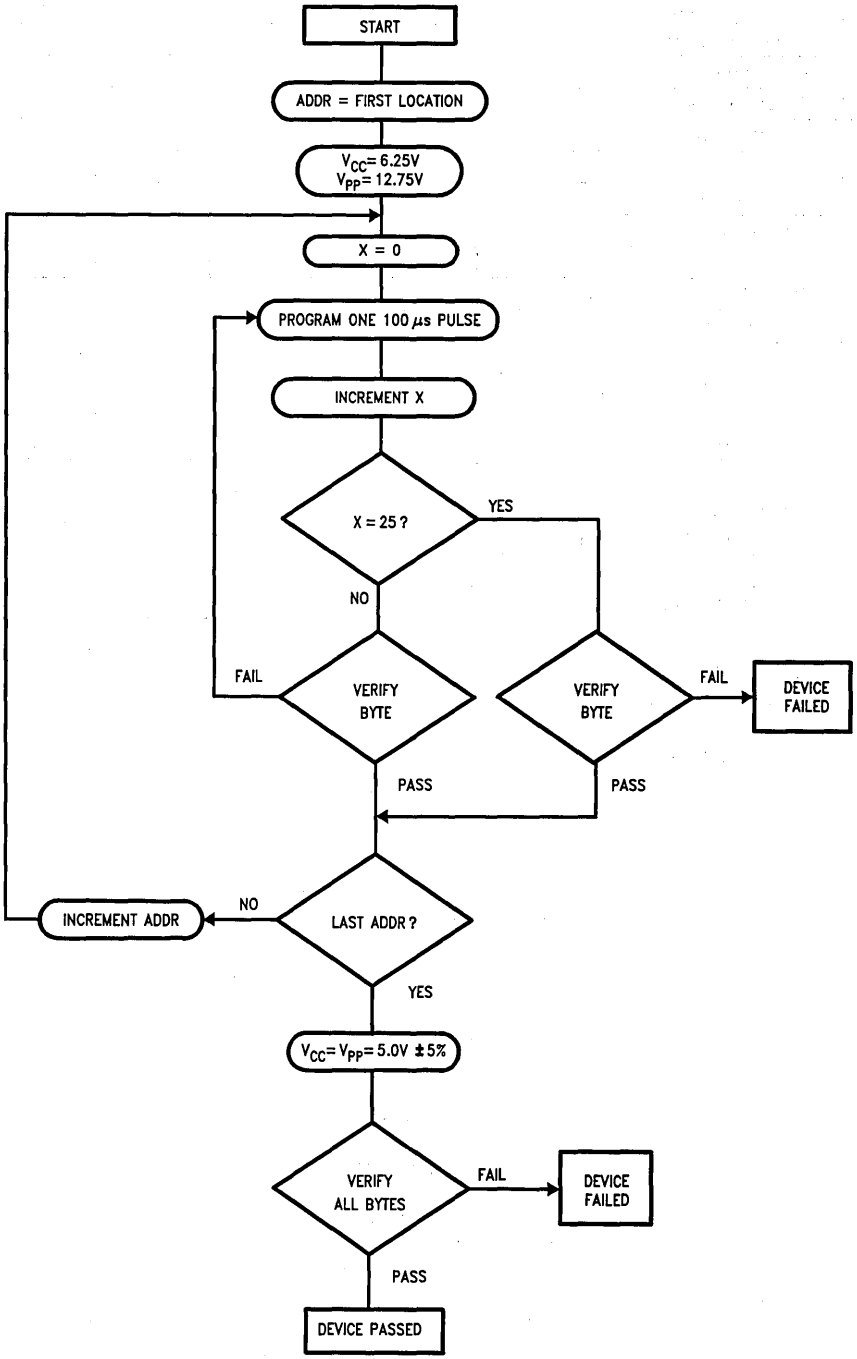
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart (Same as NMC27C010)



TL/D/10798–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 275 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's indentification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27C010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1 Megabit (128K $\times$ 8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–07. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C210 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O_7 (21)	O_6 (20)	O_5 (19)	O_4 (18)	O_3 (17)	O_2 (15)	O_1 (14)	O_0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

National Semiconductor

NM27C210
1,048,576-Bit (64K x 16) High Performance CMOS EPROM

General Description

The NM27C210 is a high performance Electrically Programmable UV erasable ROM (EPROM). It contains 1,048,576 bits configured as 64K x 16 bit. It is offered in both erasable versions for prototyping and early production applications as well as non-erasable, plastic packaged versions that are ideal for high volume and automated assembly applications.

The NM27C210 operates from a single 5 volt ±10% supply in the read mode.

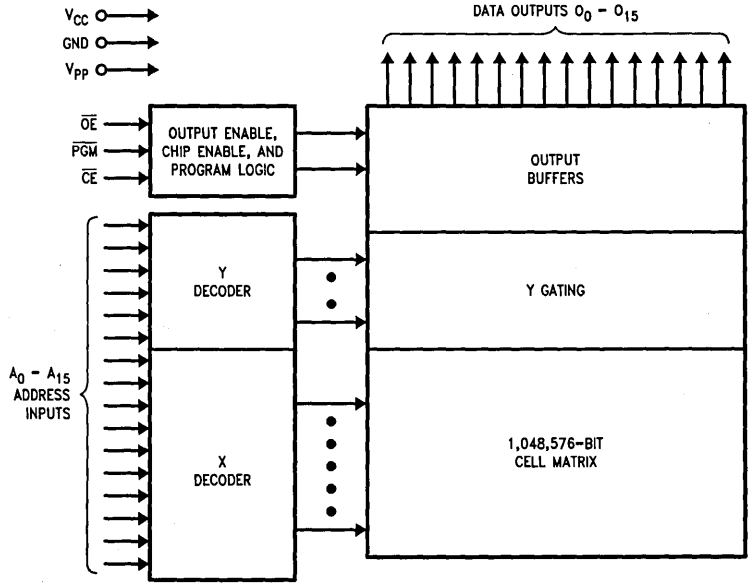
The NM27C210 is offered in both DIP and surface mount packages. The DIP package is a 40-pin dual-in-line ceramic with a quartz window to allow erasing. The surface mount package is a 44-pin PLCC that is offered in OTP.

This EPROM is manufactured using National's proprietary 1.2 micron CMOS SVG EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

Features

- High performance CMOS
  - 120 ns access time
- Fast turn-off for microprocessor compatibility
- High reliability with EPI processing
  - Latch-up immunity
  - ESD protection exceeds 2000V
- Simplified upgrade path
  - V_{PP} and PGM are "Don't Care" during normal read operation
- Compatible with 27210 and 27C210 EPROMs
- JEDEC standard pin configuration
  - 40-pin DIP package
  - 44-pin PLCC package
- Manufacturer's identification code
- Fast programming

Block Diagram



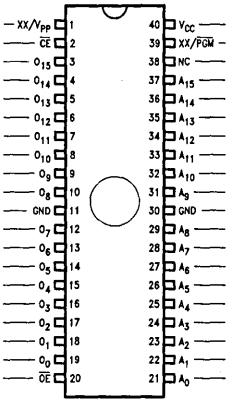
TL/D/11093-1

Connection Diagrams

DIP PIN CONFIGURATIONS

27C280	27C240	27C220
A_{18}	XX/V_{PP}	XX/V_{PP}
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_{15}	O_{15}	O_{15}
O_{14}	O_{14}	O_{14}
O_{13}	O_{13}	O_{13}
O_{12}	O_{12}	O_{12}
O_{11}	O_{11}	O_{11}
O_{10}	O_{10}	O_{10}
O_9	O_9	O_9
O_8	O_8	O_8
GND	GND	GND
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3
O_2	O_2	O_2
O_1	O_1	O_1
O_0	O_0	O_0
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$

DIP
NM27C210



27C220	27C240	27C280
V_{CC}	V_{CC}	V_{CC}
XX/$\overline{PGM}$	A_{17}	A_{17}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_{12}	A_{12}	A_{12}
A_{11}	A_{11}	A_{11}
A_{10}	A_{10}	A_{10}
A_9	A_9	A_9
GND	GND	GND
A_8	A_8	A_8
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C210 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 N, Q, V 120	120
NM27C210 N, Q, V 150	150
NM27C210 N, Q, V 200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 QM 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 NE, QE, VE 120	120
NM27C210 NE, QE, VE 150	150
NM27C210 NE, QE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

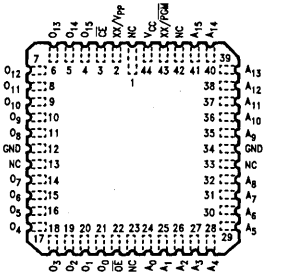
Package Types: NM27C210 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP package
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	f = 5 MHz		50	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		35		45		55	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

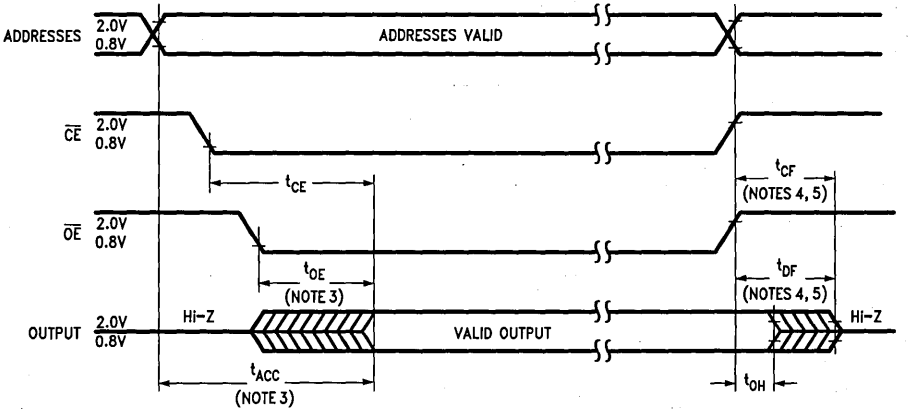
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



TL/D/11093–4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

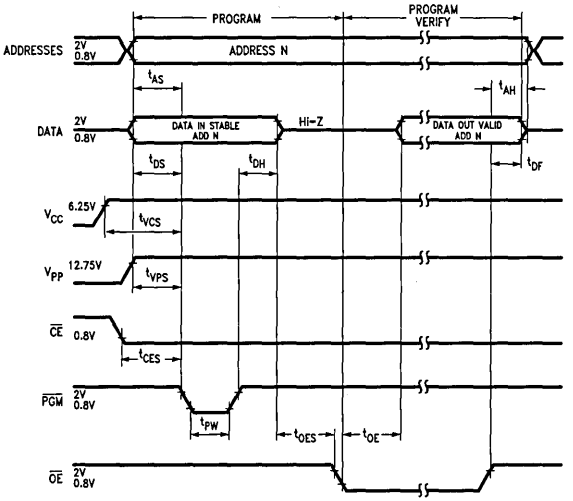
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/11093–5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

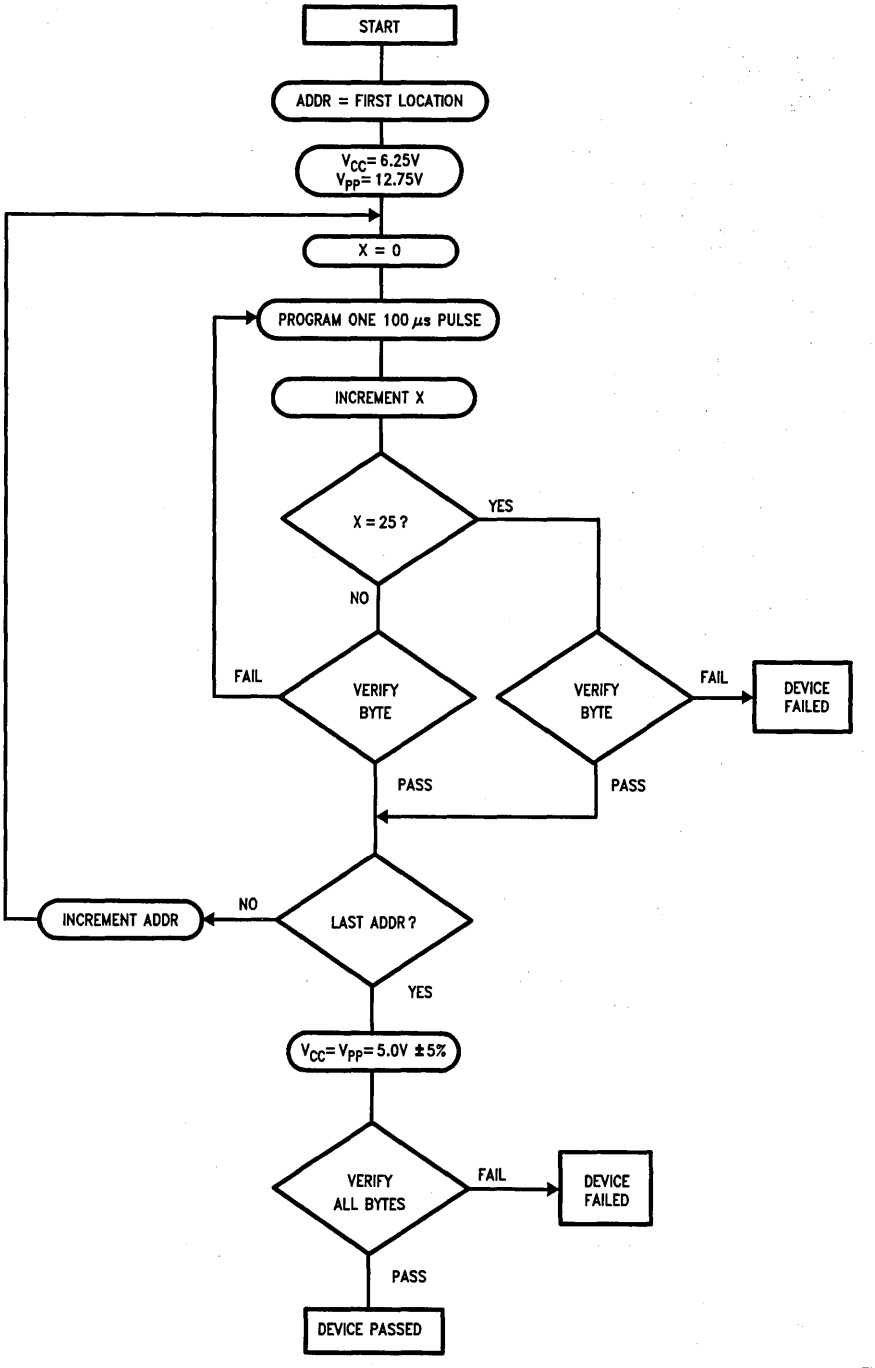
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11093–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 275 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27C210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A_9. Addresses A_1-A_8, $A_{10}-A_{15}$, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0-O_7. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C210 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

National Semiconductor

NM27C040
4,194,304-Bit (512K x 8) High Performance CMOS EPROM

General Description

The NM27C040 is a high performance, 4,194,304-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 512K words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature on V_{PP} during read operations allows memory expansions from 1M to 8 Mbits with no printed circuit board changes.

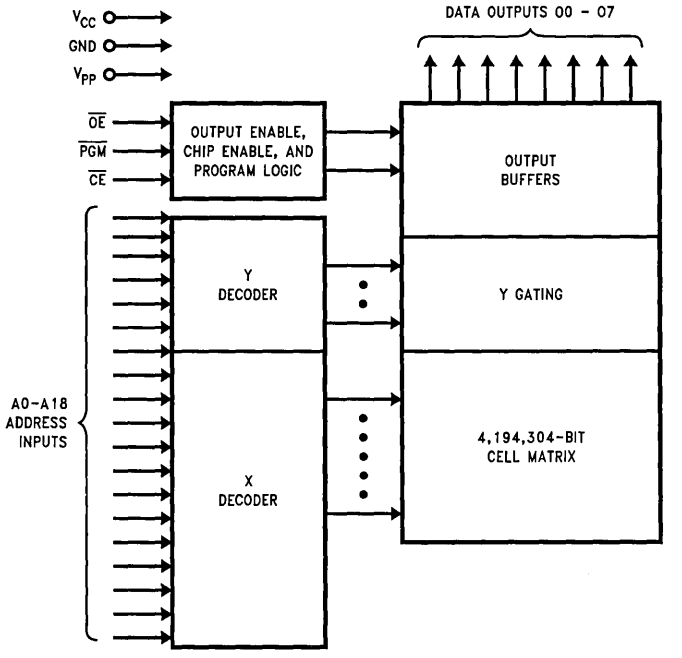
The NM27C040 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 150 ns access time provides high speed operation with high-performance CPUs. The NM27C040 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The NM27C040 is manufactured using National's advanced CMOS SVG EPROM technology.

Features

- High performance CMOS
  - 150 ns access time
- High reliability with EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection exceeds 2000V
- Simplified upgrade path
  - V_{PP} is a "Don't Care" during normal read operation
- JEDEC standard pin configuration
  - 32-pin DIP package
- Manufacturer's identification code

Block and Connection Diagrams



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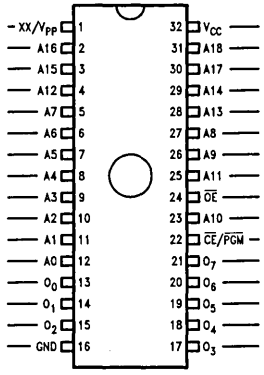
Block and Connection Diagrams (Continued)

27C080	27C020	27C010
A19	XX/V_{PP}	XX/V_{PP}
A16	A16	A16
A15	A15	A15
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND

DIP
NM27C040



TL/D/10836-2

27C010	27C020	27C080
V_{CC}	V_{CC}	V_{CC}
XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18
XX	A17	A17
A14	A14	A14
A13	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C040 pin.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 Q 150	150
NM27C040 Q 170	170
NM27C040 Q 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 QE 150	150
NM27C040 QE 170	170
NM27C040 QE 200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 QM 200	200

Package Types: NM27C040 Q,VXXX
Q = Quartz-Windowed Ceramic DIP

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} +10V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	±5V	±10%
Military	−55°C to +125°C	±5V	±10%

Read Operation

DC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	f = 5 MHz		60	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	150		170		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		170		200	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF} (Note 2)	Output Disable to Output Float		35		45		55	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	9	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	15	pF

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF (Note 8)

Input Rise and Fall Times: ≤5 ns

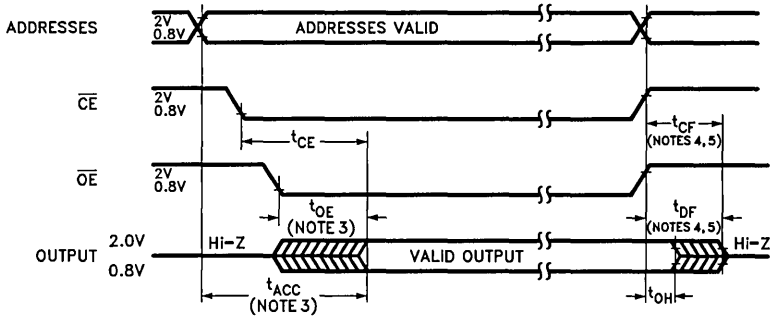
Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level (Note 10)

Inputs: 0.8V and 2V

Outputs: 0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

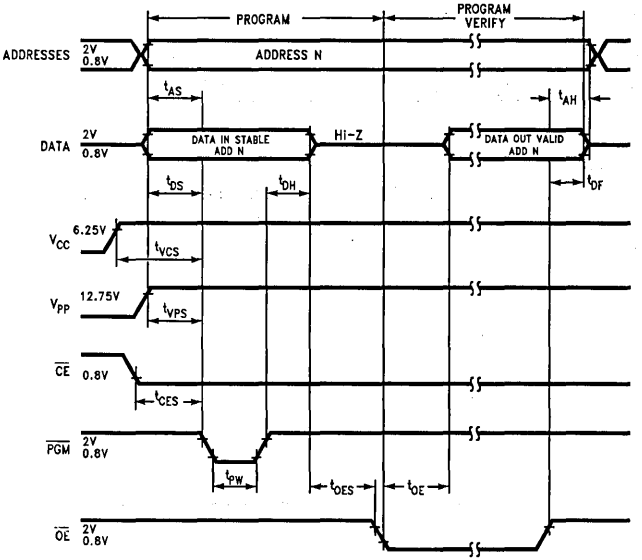
Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Waveform (Note 3)



TL/D/10836–5

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM}$ = X	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM}$ = X			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage		−0.1	0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

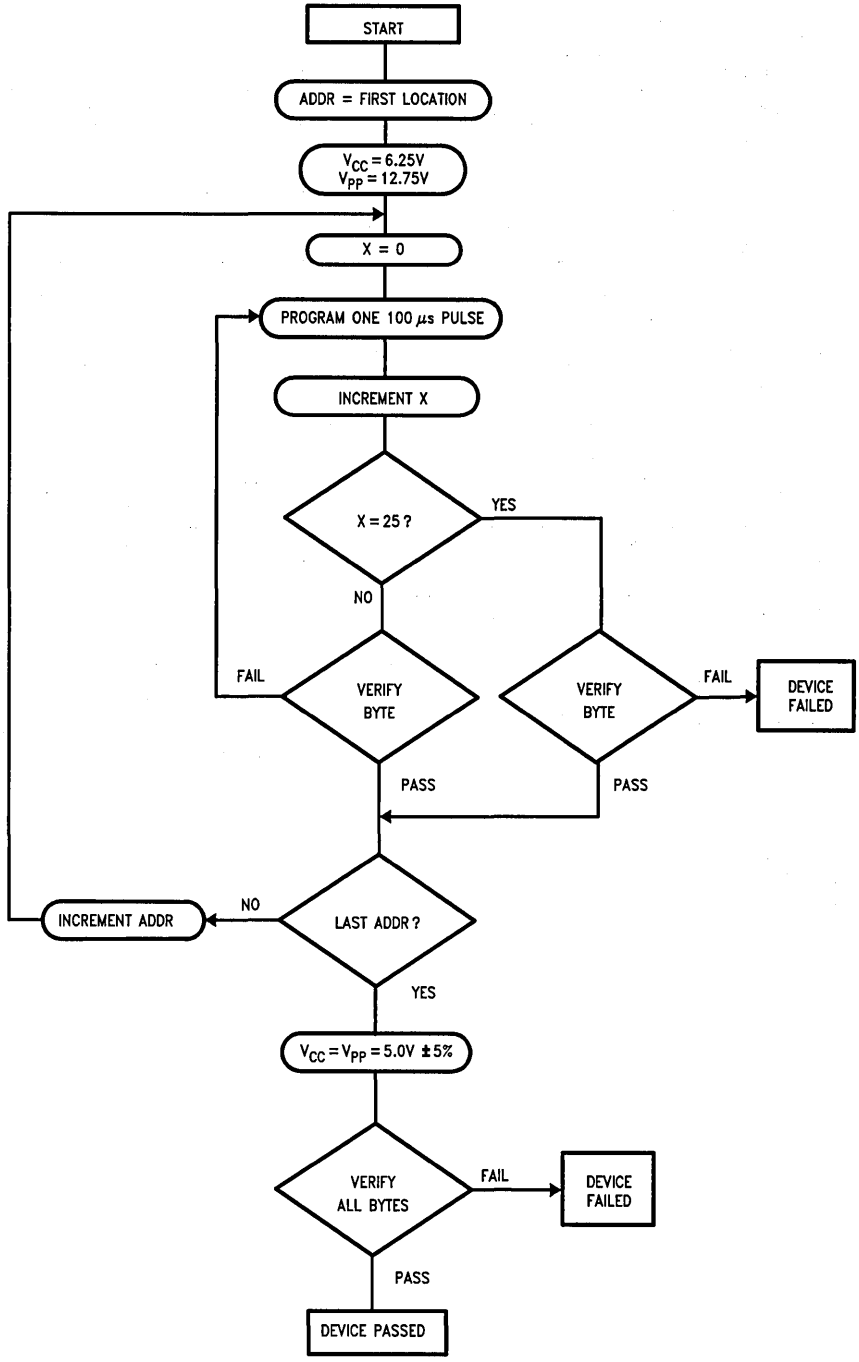
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Progam Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/10836–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE/PGM has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from of 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Functional Description (Continued)

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C040 is "8F08", where "8F" designates that it is made by National Semiconductor, and "08" designates a 4 Megabit (512K x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C040 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_H

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	1	0	0	0	08

National Semiconductor

Processor Oriented EPROM Selection Guide

General Description

National Semiconductor's family of Processor Oriented EPROMs are devices with features or functions to enhance their operation with various microprocessors and microcontrollers. There are 3 devices with specification improvements to help eliminate wait states and glue logic. These are the NM27P512, NM27P210, and NM27P040. There is one device that has address latches to facilitate multiplexed data/address busses without the use of external address latches, the NMC87C257.

Available Product

	Packages	Temperature Ranges*	Improved t_{DF}/t_{OH}	Latches
NM27P512	Q, N, V	C, E, M	Y	
NM27P210	Q, N, V	C, E, M	Y	
NM27P040	Q, N, V	C, E, M	Y	
NMC87C257	Q, V	C, E, M		Y

*Contact your National Semiconductor sales representative for military operating temperature range devices.

Ordering Information

NM 27 P 512 Q E 120

National Memory

EPROM

Processor Oriented

Memory Configuration
257 = 32k x 8 w/Latches
512 = 64k x 8
210 = 64k x 16
040 = 512k x 8

Package
Q = Quartz Window Ceramic
N = Plastic DIP (OTP)
V = PLCC (OTP)

Operating Temperature Range
No Entry = 0°C to +70°C
E = −40°C to +85°C
M = −55°C to +125°C

Speed

National Semiconductor

NM27P512
524,288-Bit (64K x 8) Processor Oriented CMOS EPROM

General Description

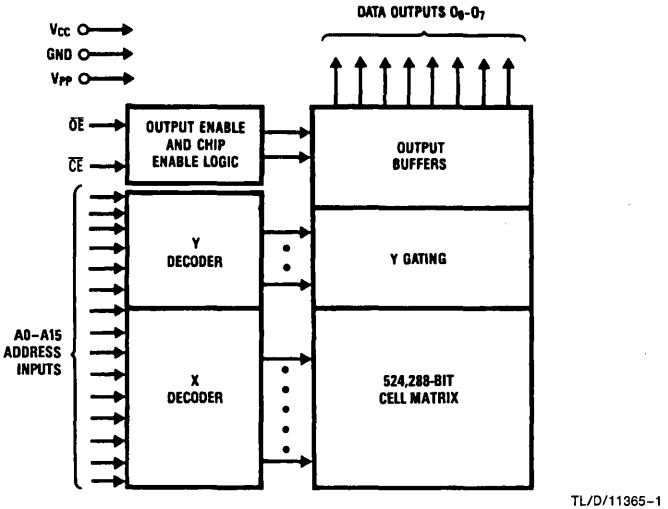
The NM27P512 is a 512K Processor Oriented EPROM configured as 64k x 8. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P512 is implemented in National's advanced CMOS EPROM process to provide a reliable solution and access times as fast as 120 ns.

The interface improvements address two areas to eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P512 remains compatible with industry standard JEDEC pinout EPROMs. The time from CE or OE being negated until the outputs are guaranteed to be in the high impedance state has been reduced to eliminate the need for wait states at the termination of the memory cycle and the data-out hold time has been extended to eliminate the need to provide data hold time for the microprocessor by delaying control signals or latching and holding the data in external latches.

Features

- Fast output turn off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  — 120 ns access time
- High reliability with EPI processing
  — Latch-up immunity to 200 mA
  — ESD protection exceeds 2000V
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram

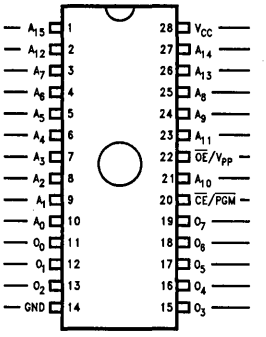


TL/D/11365-1

Connection Diagrams

27C080	27C040	27C020	27C010	27C256
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27P512



27C256	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	$XX/\overline{PGM}$	$XX/\overline{PGM}$	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P512 pins.

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)*
NM27P512 Q, N, V 120	120
NM27P512 Q, N, V 150	150

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Access Time (ns)*
NM27P512 QM 200	200

Extended Temp Range (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)*
NM27P512 QE, NE, VE 120	120
NM27P512 QE, NE, VE 150	150

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

*All versions are guaranteed to function for slower speeds.

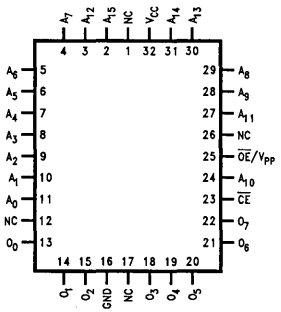
Package Types: NM27P512 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP Package
N = Plastic OTP DIP Package
V = PLCC Package

- All packages conform to the JEDEC standard.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PLCC



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature −65°C to +150°C

All Input Voltages Except A9 with Respect to Ground −0.6V to +7V

V_{PP} and A9 with Respect to Ground −0.7V to +14V

V_{CC} Supply Voltage with Respect to Ground −0.6V to +7V

ESD Protection (MIL Std. 883, Method 3015.2) >2000V

All Output Voltages with Respect to Ground V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	08	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		3.5		V
I_{SB1}(10)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	f = 5 MHz		40	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_C − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Electrical Characteristics

Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF}(2)	Output Disable to Output Float		25		25		25	
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	7		7		7		

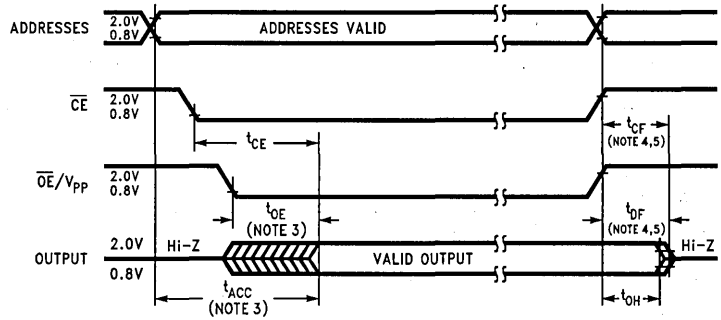
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 9)	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



TL/D/11365–4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

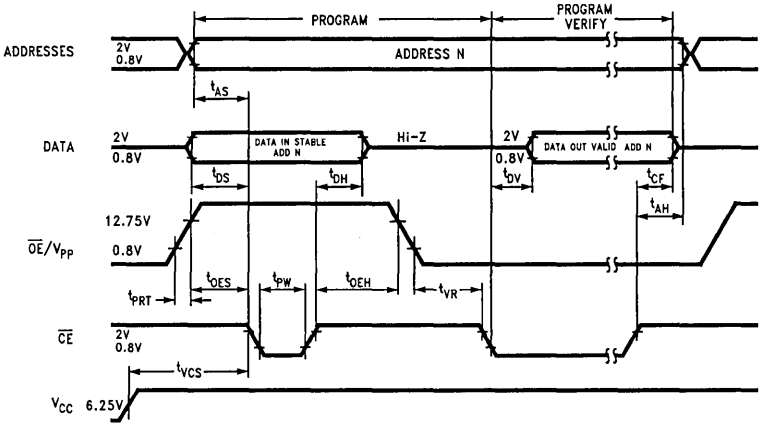
Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 10: CMOS inputs; V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Characteristics (Notes 1 and 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



TL/D/11365–5

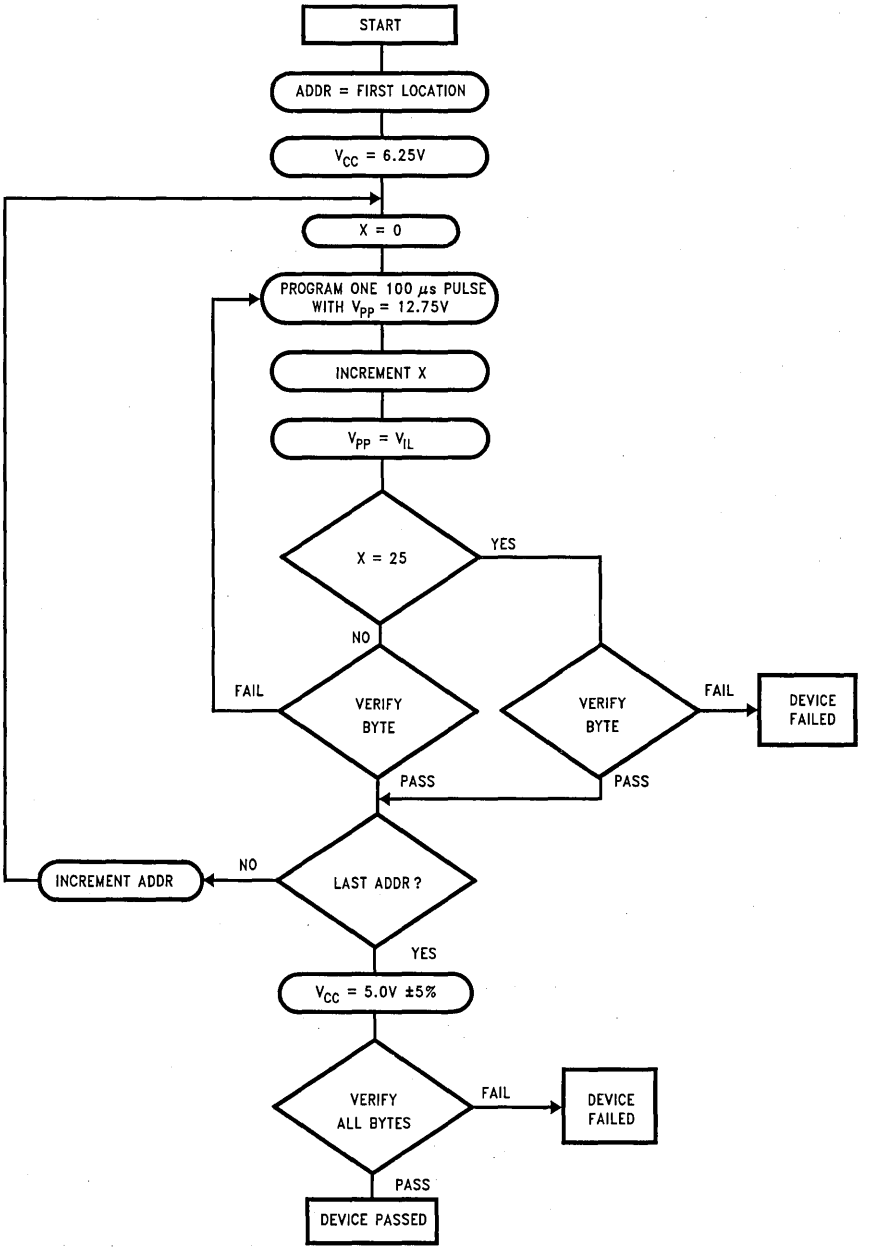
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

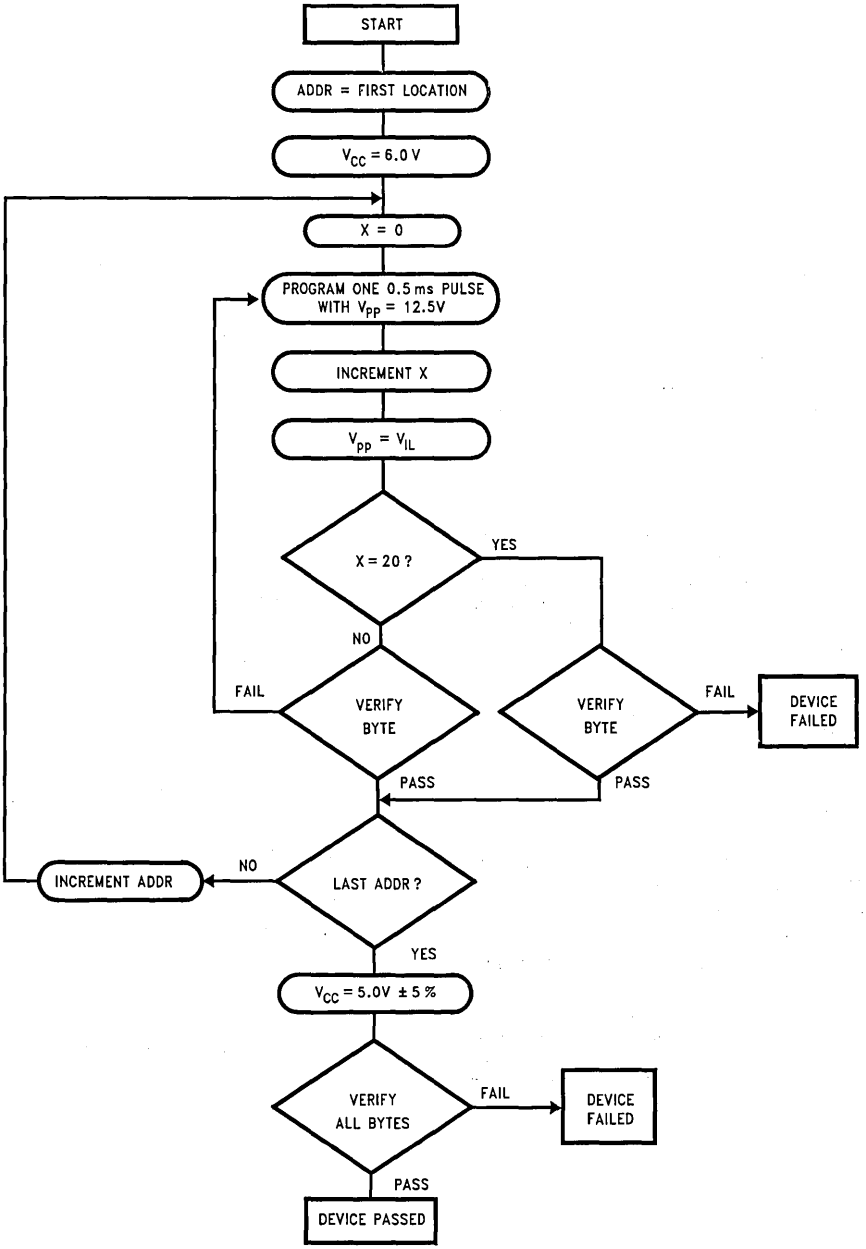
Fast Programming Algorithm Flow Chart



TL/D/11365–6

FIGURE 1

Interactive Programming Algorithm Flow Chart



TL/D/11365–7

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and OE/V_{PP}. The OE/V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE/V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (OE/V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE/V_{PP}) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with OE/V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with OE/V_{PP} and CE at V_{IL}. Data should be verified T_{DV} after the falling edge of CE.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27P512 is "8F85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27P512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	V_{PP}(2)	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(2)	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

National Semiconductor

NM27P210
1,048,576-Bit (64K x 16) Processor Oriented CMOS EPROM

General Description

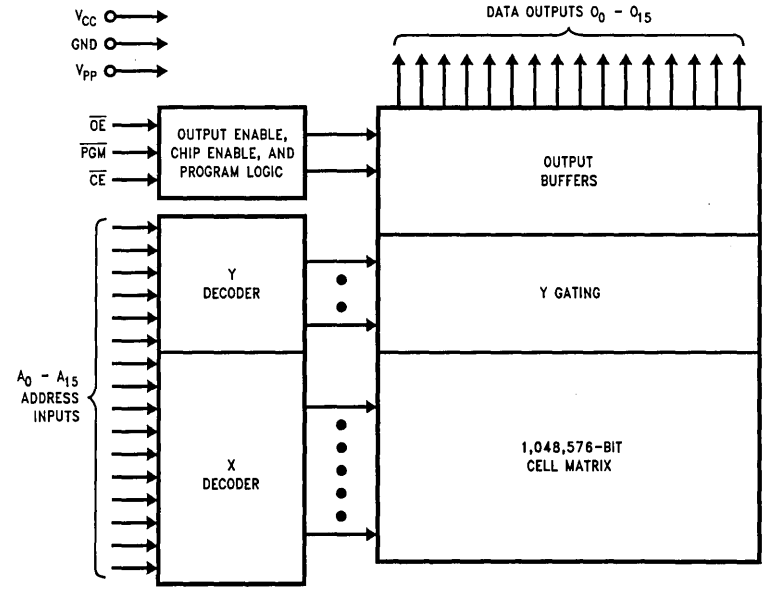
The NM27P210 is a 1024K Processor Oriented EPROM configured as 64K x 16. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P210 is implemented in National's advanced CMOS EPROM process to provide a reliable solution and access times as fast as 120 ns.

The interface improvements address two areas to eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P210 remains compatible with industry standard JEDEC pinout EPROMs. The time from CE or OE being negated until the outputs are guaranteed to be in the high impedance state has been reduced to eliminate the need for wait states at the termination of the memory cycle and the data-out hold time has been extended to eliminate the need to provide data hold time for the microprocessor by delaying control signals or latching and holding the data in external latches.

Features

- Fast output turn-off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  — 120 ns access time
- High reliability with EPI processing
  — Latch-up immunity to 200 mA
  — ESD protection exceeds 2000V
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram



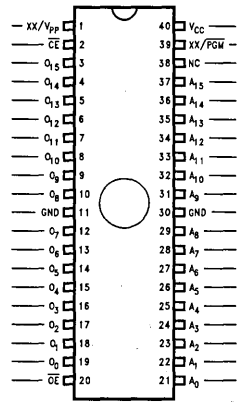
TL/D/11366-1

Connection Diagrams

DIP PIN CONFIGURATIONS

27C280	27C240	27C220
A_{18}	XX/V_{PP}	XX/V_{PP}
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_{15}	O_{15}	O_{15}
O_{14}	O_{14}	O_{14}
O_{13}	O_{13}	O_{13}
O_{12}	O_{12}	O_{12}
O_{11}	O_{11}	O_{11}
O_{10}	O_{10}	O_{10}
O_9	O_9	O_9
O_8	O_8	O_8
GND	GND	GND
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3
O_2	O_2	O_2
O_1	O_1	O_1
O_0	O_0	O_0
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$

DIP
NM27P210



27C220	27C240	27C280
V_{CC}	V_{CC}	V_{CC}
$XX/\overline{PGM}$	A_{17}	A_{17}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_{12}	A_{12}	A_{12}
A_{11}	A_{11}	A_{11}
A_{10}	A_{10}	A_{10}
A_9	A_9	A_9
GND	GND	GND
A_8	A_8	A_8
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P210 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P210 Q, V 120	120
NM27P210 Q, V 150	150

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P210 QM 200	150

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P210 QE, VE 120	120
NM27P210 QE, VE 150	150

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

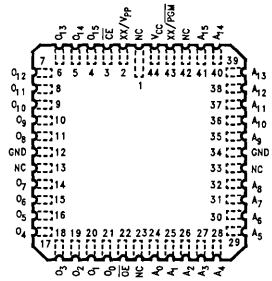
Package Types: NM27P210 Q, V XXX
Q = Quartz-Windowed Ceramic DIP package
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



TL/D/11366–3

Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		3.5		V
I_{SB1} (Note 11)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	f = 5 MHz		50	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150	
t_{OE}	$\overline{OE}$ to Output Delay		50		50	
t_{DF}/t_{CF} (Note 2)	Output Disable to Output Float		25		25	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	7		7		

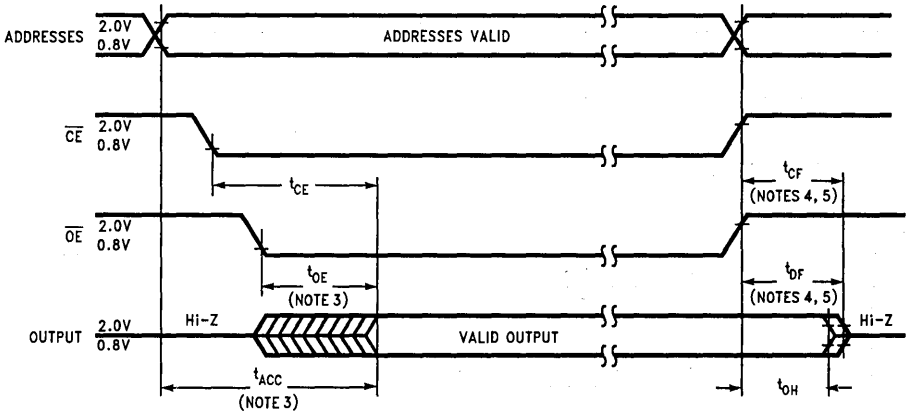
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

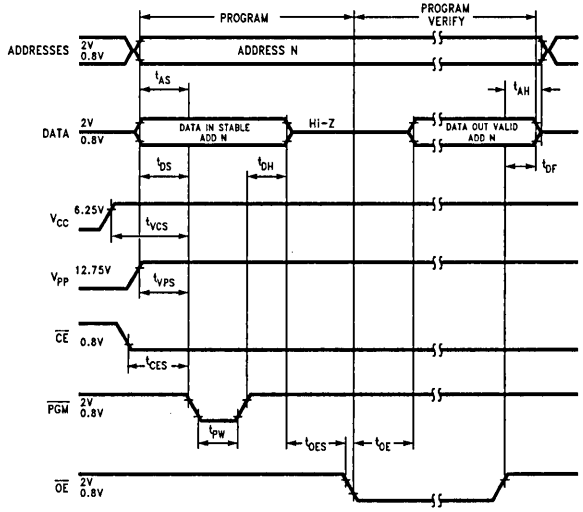
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS inputs; V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Characteristics (Notes 1, 2, 3, 4 & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/11366–5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

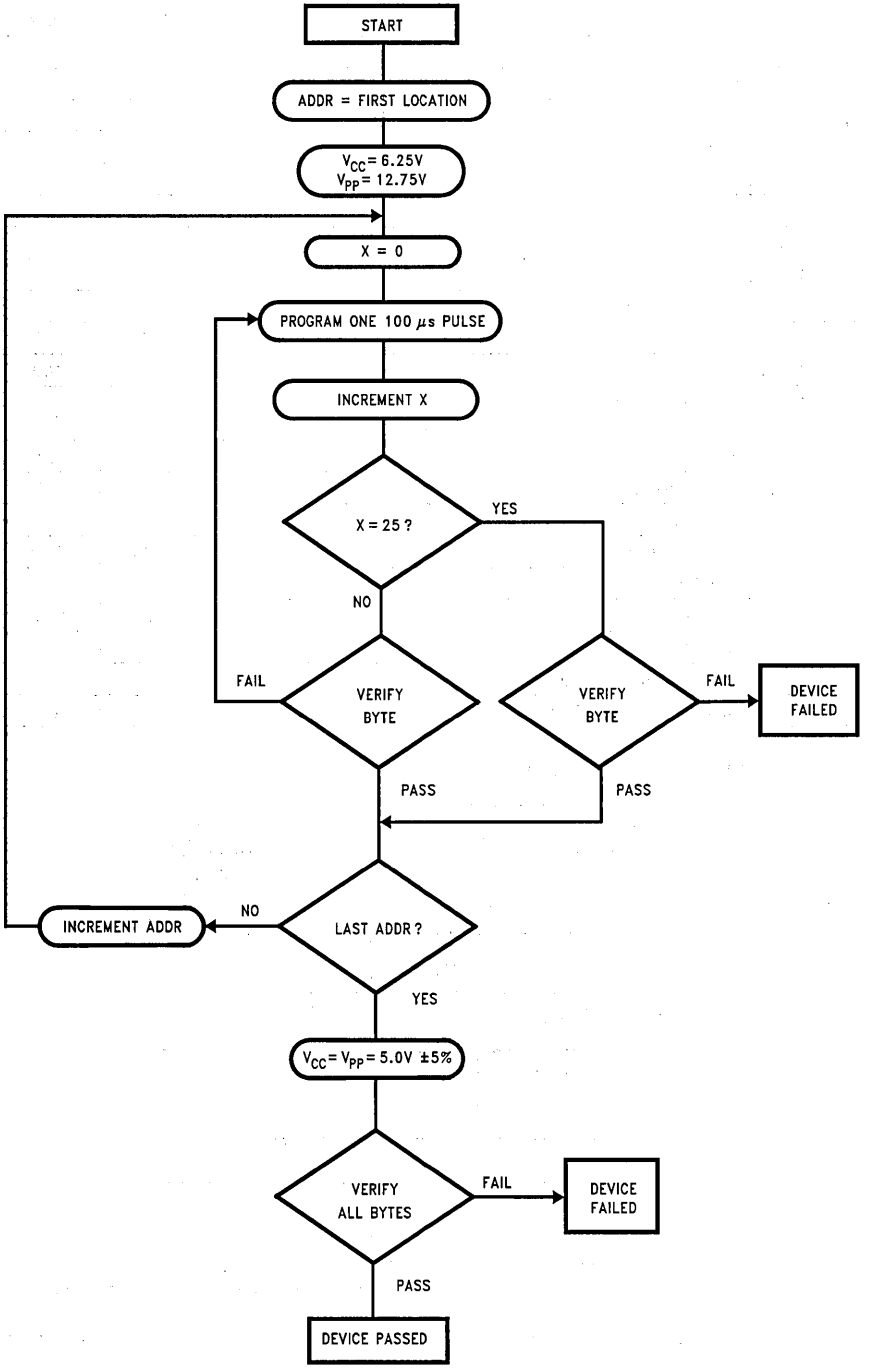
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11366–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 275 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27P210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V ±0.5V to address pin A_9. Addresses A_1-A_8, $A_{10}-A_{15}$, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0-O_7. Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27P210 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

National Semiconductor

NM27P040
4,194,304-Bit (512K x 8) Processor Oriented CMOS EPROM

General Description

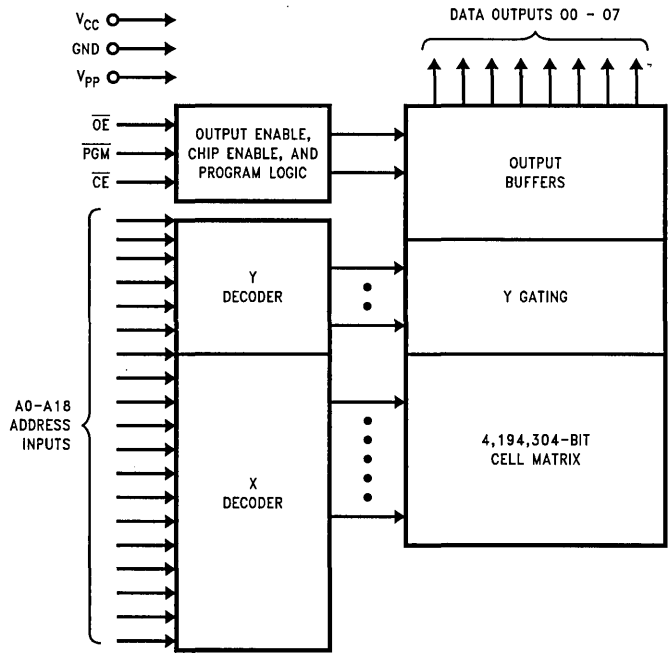
The NM27P040 is a 4096K Processor Oriented EPROM configured as 512K x 8. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P040 is implemented in National's advanced CMOS EPROM process to provide a reliable solution and access times as fast as 150 ns.

The interface improvements address two areas to eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P040 remains compatible with industry standard JEDEC pinout EPROMs. The time from CE or OE being negated until the outputs are guaranteed to be in the high impedance state has been reduced to eliminate the need for wait states at the termination of the memory cycle and the data-out hold time has been extended to eliminate the need to provide data hold time for the microprocessor by delaying control signals or latching and holding the data in external latches.

Features

- Fast output turn off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  — 150 ns access time
- High reliability with EPI processing
  — Latch-up immunity to 200 mA
  — ESD protection exceeds 2000V
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram

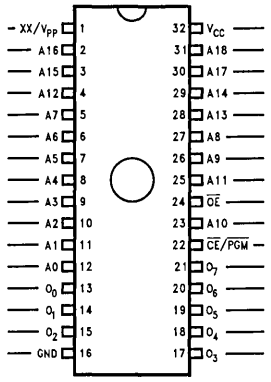


TL/D/11367–1

Connection Diagrams

27C080	27C020	27C010
A19	XX/V_{PP}	XX/V_{PP}
A16	A16	A16
A15	A15	A15
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND

DIP
NM27P040



TL/D/11367–2

27C010	27C020	27C080
V_{CC}	V_{CC}	V_{CC}
XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18
XX	A17	A17
A14	A14	A14
A13	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P040 pin.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P040 Q 150	150
NM27P040 Q 170	170

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P040 QE 150	150
NM27P040 QE 170	170

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P040 QM 200	250

Package Types: NM27P040 QXXX
Q = Quartz-Windowed Ceramic DIP

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} +10V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	±5V	±10%
Military	−55°C to +125°C	±5V	±10%

Read Operation

DC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS) (Note 11)	$\overline{CE} = V_{CC} \pm 0.3V$		100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5 MHz		60	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	150		170		250		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		170		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		170		250	
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	
t_{DF}/t_{CF} (Note 2)	Output Disable to Output Float		25		25		25	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	7		7		7		

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

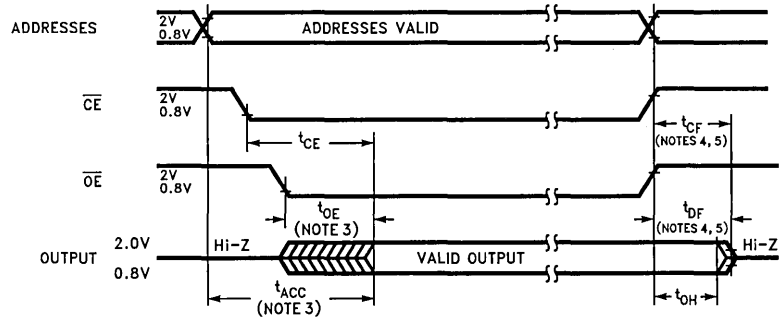
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level (Note 10)

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

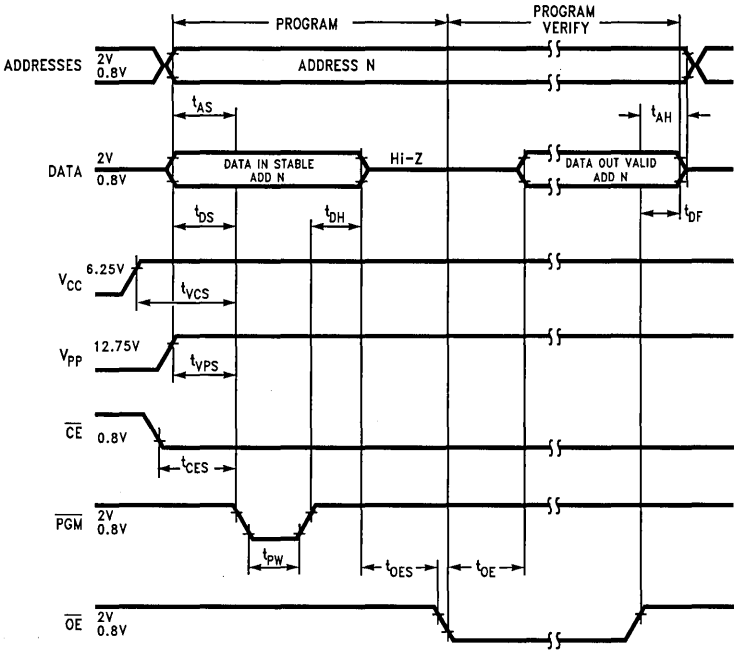
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS input: V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Waveform (Note 3)



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Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM}$ = X	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM}$ = X			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage		−0.1	0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Progam Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart

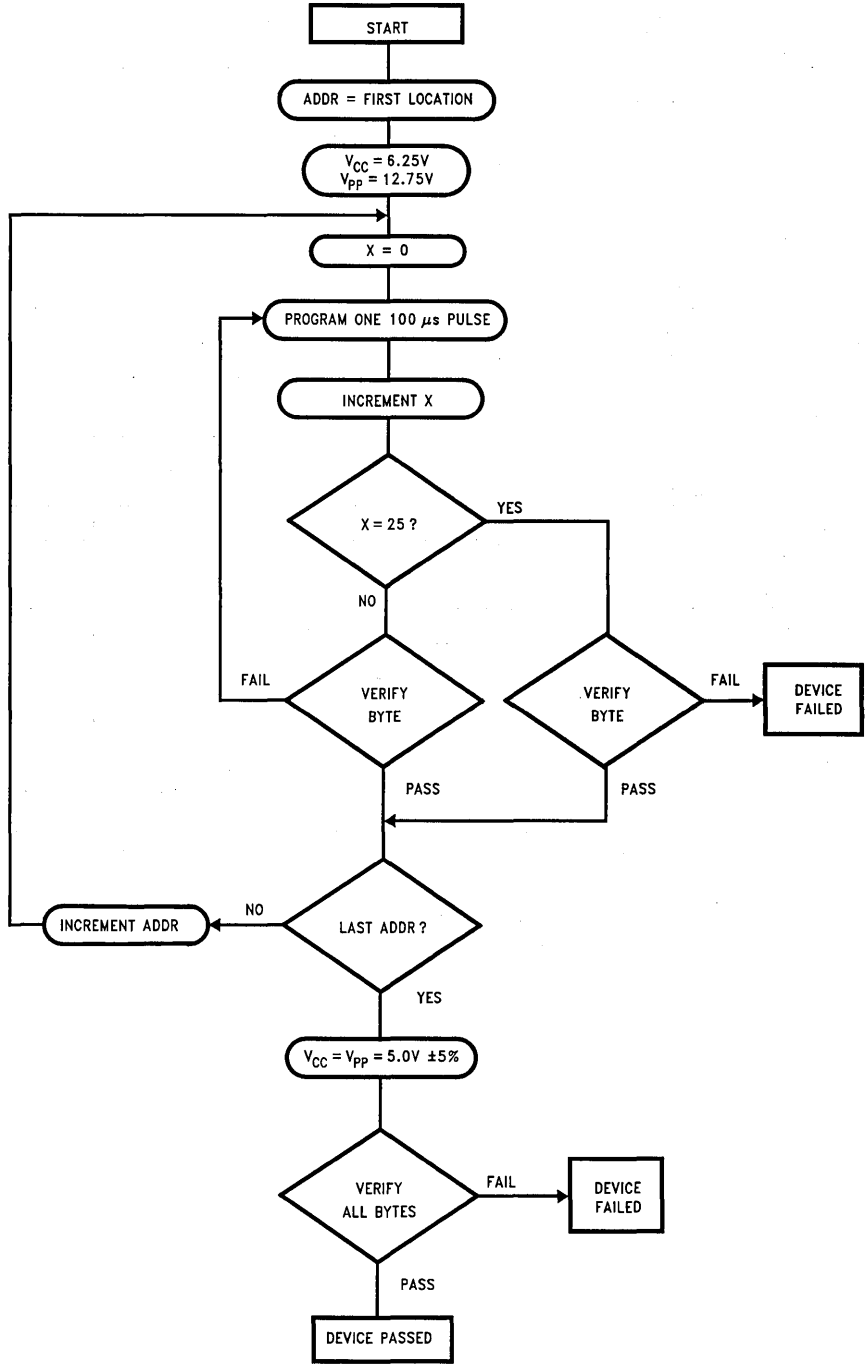

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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE/PGM has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from of 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27P040 is "8F08", where "8F" designates that

Functional Description (Continued)

it is made by National Semiconductor, and "08" designates a 4 Megabit (512K x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27P040 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_H

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	1	0	0	0	08

National Semiconductor

NMC87C257
262,144-Bit (32K x 8) CMOS EPROM with On-Chip Address Latches

General Description

The NMC87C257 is a CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC87C257 has latched addresses for direct interfacing with address/data multiplexed microprocessors and microcontrollers. The A0–A7 pins can be tied to the respective O0–O7 pins and then bused to the microprocessor or microcontroller directly. No latch device is needed for interfacing.

The part is designed to operate with a single +5V power supply with ±10% tolerance.

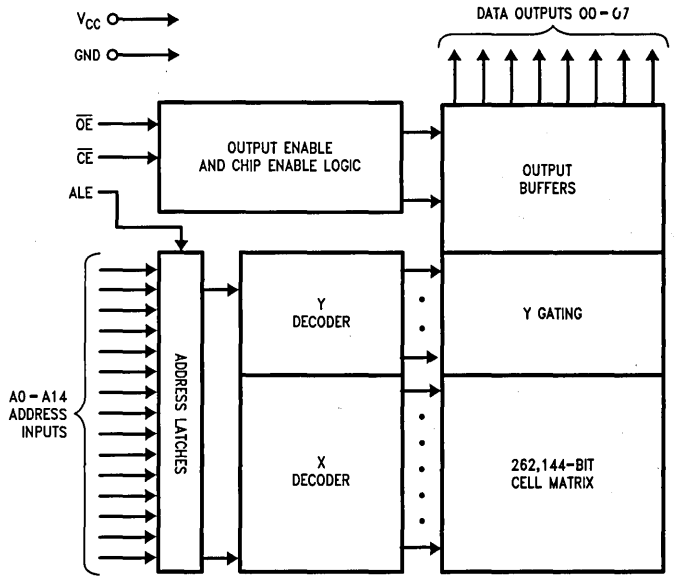
The part is packaged in a 28-pin dual-in-line package with a quartz window or PLCC. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure. The PLCC is not erasable.

This EPROM is fabricated with National's proprietary CMOS double-poly silicon gate technology.

Features

- Address latches for direct interfacing with address/data multiplexed microprocessors
- Low CMOS power consumption:
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Pin compatible with standard 256K EPROM
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control use NMC27C256B PGM Algorithm
- High current CMOS level output drivers

Block Diagram



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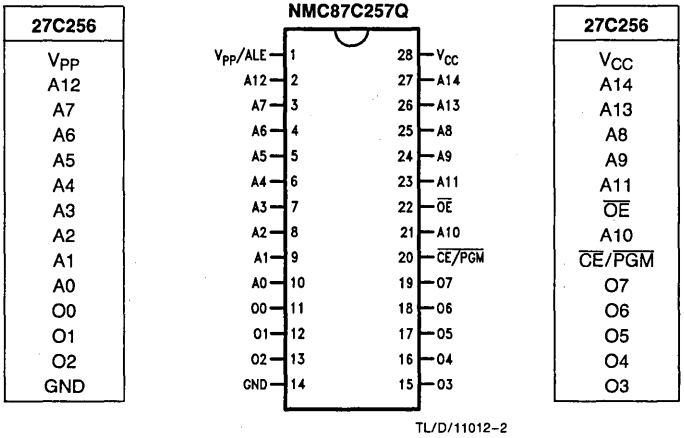
Connection Diagram



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Note: Socket compatible 27C256 EPROM pin configuration is shown in the block adjacent to the NMC87C257 pins.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
ALE	Address Latch Enable
V_{PP}	Programming Supply
V_{CC}	Power Supply
GND	Ground
NC	No Connection

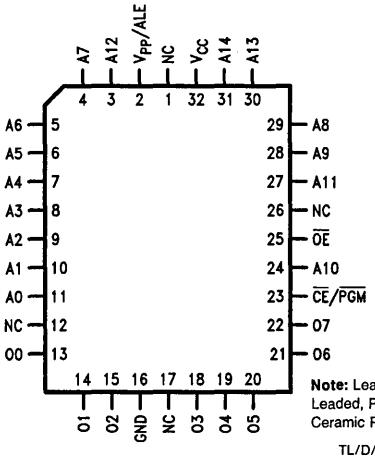
Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC87C257Q150, V150	150
NMC87C257Q200, V200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC87C257QE150	150
NMC87C257QE200	200

PLCC Pin Configuration



Note: Leadless or Leaded, Plastic or Ceramic Package

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Top

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias	−65°C to +150°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 2)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 2)	V_{CC} + 1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 Seconds)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	1700V

Operating Conditions (Note 3)

V_{CC} Power Supply	5V ±10%
Temperature Range	
Commercial	0°C to +70°C
Extended	−40°C to +85°C

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current		$V_{IN} = V_{CC}$ or GND		0.01	1.0	μA
I_{LO}	Output Leakage Current		$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1.0	μA
I_{CC1} (Note 4)	V_{CC} Current (Active) TTL Inputs		ALE = V_{IH}, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 4)	V_{CC} Current (Active) CMOS Inputs		ALE = V_{CC}, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	Switching	$\overline{CE} = V_{IH}$, ALE = V_{IH}		10	12	mA
		Stable	$\overline{CE} = V_{IH}$, ALE = V_{IL}		0.3	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	Switching	$\overline{CE} = V_{CC}$, ALE = V_{CC}		8	10	mA
		Stable	$\overline{CE} = V_{CC}$, ALE = GND		0.5	100	μA
I_{PP}	V_{PP} Load Current		$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage			−0.2		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage		I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.1			V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 3: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 4: V_{PP} may be connected to V_{CC} except during programming.

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC87C257				Units
			150		200		
			Min	Max	Min	Max	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	Chip Enable Access Time	$\overline{OE} = V_{IL}$		150		200	ns
t_{LL}	Chip Deselect Width		30		50		ns
t_{AL}	Address to ALE Latch Set-Up		5		15		ns
t_{LA}	Address Hold from ALE Latch		20		30		ns
t_{OE}	Output Enable to Output Valid	$\overline{CE} = V_{IL}$		50		75	ns
t_{LOE}	ALE to Output Enable		20		30		ns
t_{CF} (Note 1)	Chip Disable to Output in High Z	$\overline{OE} = V_{IL}$	0	50	0	55	ns
t_{DF} (Note 1)	Output Disable to Output in High Z	$\overline{CE} = V_{IL}$	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

Note 1: This parameter is only sampled and is not 100% tested.

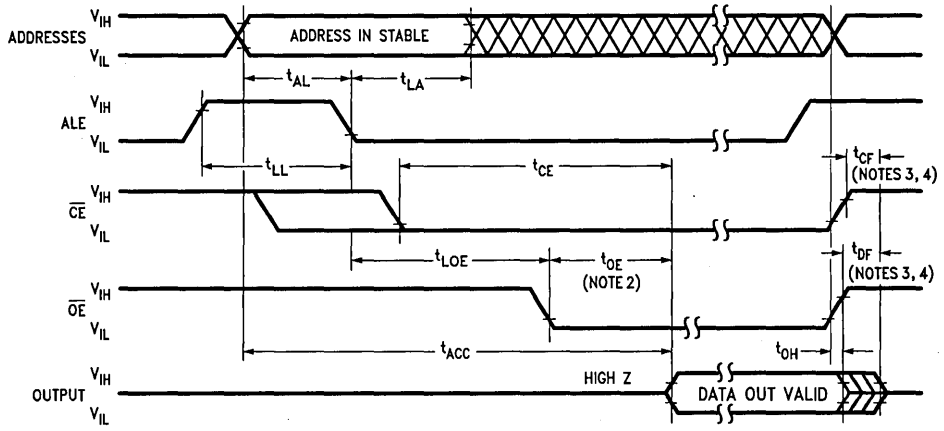
Capacitance $T_A = +25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 7)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 5, 6 and 8)



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Note 1: This parameter is only sampled and is not 100% tested.

Note 2: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 3: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 4: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 5: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 6: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

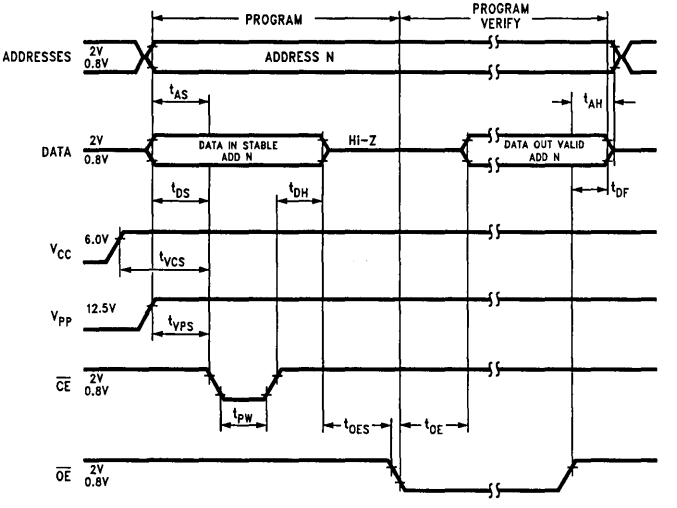
Note 7: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 8: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms



TL/D/11012–4

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 1) (Same as NMC27C256B)

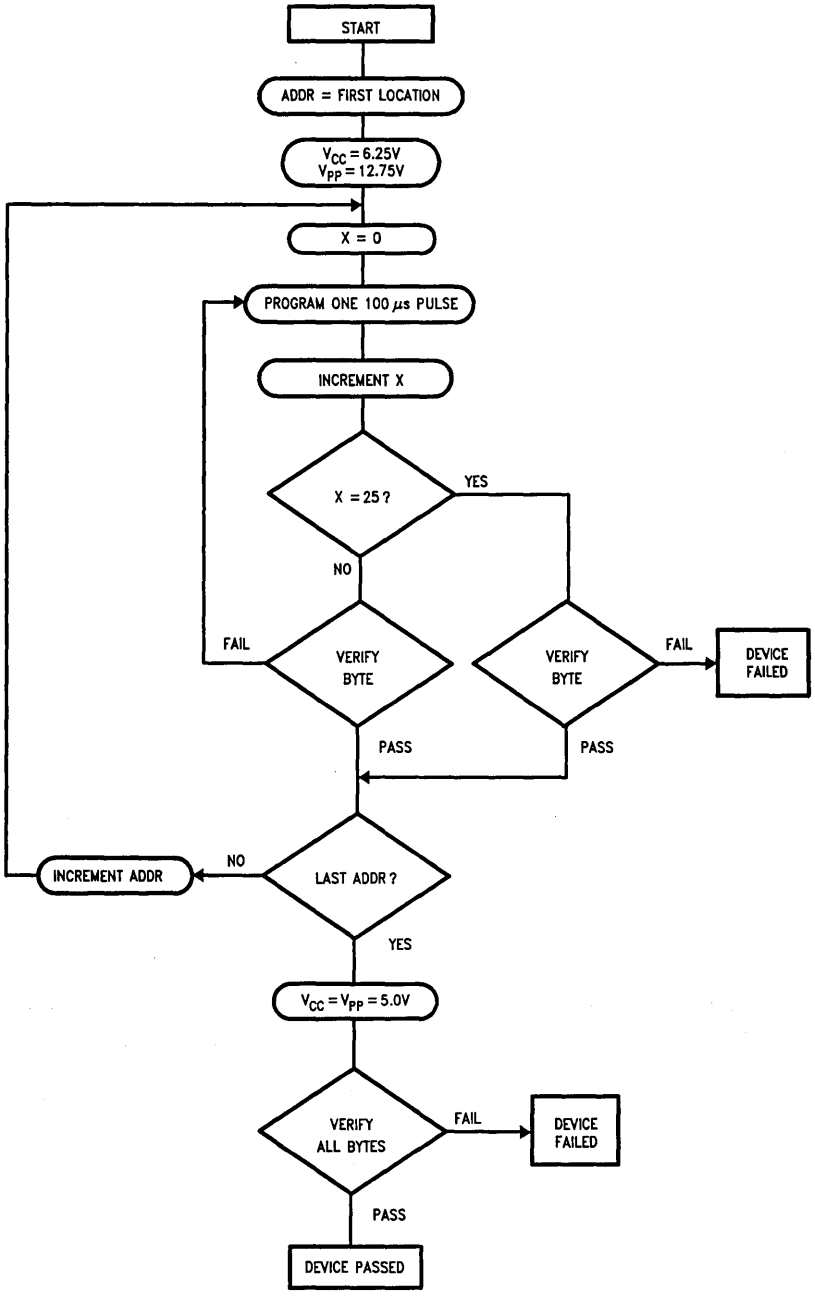


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FIGURE 1

Note 1: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Functional Description

DEVICE OPERATION

The seven modes of operation of the NMC87C257 are listed in Table I. It should be noted that all inputs for the seven modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC87C257 has a chip enable (CE) and an output enable (OE), both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}), is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Address Latch Operation

The NMC87C257 has an Address Latch Enable (ALE) pin which latches the address inputs on a negative transition. Addresses must be stable for the address setup time (t_{AL}) before the ALE transition, and they must hold for the address hold time (t_{LA}) after the transition. After the hold time has transpired the address drive can be removed from the address input pins and the bus can be used for other signals. The ALE pin is a feed-through latch and the part will operate as a normal unlatched device when the ALE pin is held high.

An important application for the NMC87C257 is memory in an address/data multiplexed microprocessor system. In an 8 bit system the low order memory address pins, A0–A7, can be tied to the respective memory output pins, O0–O7 and run on an 8-bit bus to the AD0–AD7 pins of the microprocessor. This reduces the bus width and it can be done without adding an address latch interface device. In this application the Output Enable ($\overline{OE}$) pin should be held high until after the address hold time (t_{LA}) has transpired, to avoid bus contention.

Standby Mode

The NMC87C257 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input and a CMOS low signal to the ALE input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC87C257s are usually used in larger memory arrays, National has provided a 3-line control function that accommodates this use of multiple memory connections. The 3-line control function allows for:

a. the lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these control lines, it is recommended that $\overline{CE}$ and ALE be decoded and used as the primary device selecting functions while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC87C257.

Initially, and after each erasure, all bits of the NMC87C257 are in the "1" state. Data is introduced by selectively programmings "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by untraviolet light erasure.

The NMC87C257 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC87C257 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC87C257 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Functional Description (Continued)

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP}/ALE (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	D_{OUT}
Latched	V_{IL}	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	V_{IL}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Programming multiple NMC87C257s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC87C257 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC87C257.

Program Inhibit

Programming multiple NMC87C257s in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC87C257s may be common. A TTL low level program pulse applied to an NMC87C257 $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC87C257. A TTL high level $\overline{CE}$ input inhibits the other NMC87C257 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC87C257 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC87C257 is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256K part.

The code is accessed by applying 12.0V ± 0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL} and V_{PP}/ALE is held at V_{IH}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC87C257 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC87C257 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC87C257 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC87C257 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC87C257 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Functional Description (Continued)

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

TABLE III. Minimum NMC87C257 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NM27LC256
262,144-Bit (32k x 8) Low Current CMOS EPROM

General Description

The NM27LC256 is a 32k x 8 EPROM manufactured on a proven, manufacturable CMOS process, consuming extremely low current in both the active and standby modes. The NM27LC256 consumes a mere 17.5 mW, (typical) making it ideal for battery powered portable and hand held systems, and for systems using "in-line" power.

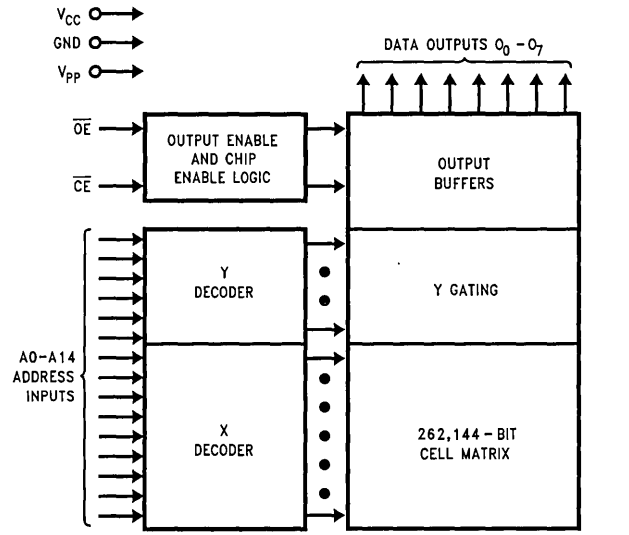
The NM27LC256 is one among a family of Power Miser products from National Semiconductor catering to the increasing low current demands of the market.

Offered in the JEDEC Pinout, the NM27LC256 offers a viable alternative to the user as a replacement for existing high power devices, while also providing an upgrade path to higher densities.

Features

- Low power consumption
  - — 5V operation
  - — 4.5 mA (max) active
  - — 100 μA (max) standby
- 170 ns access time
- Latch-up immunity to 200 mA
- ESD protection exceeds 2000V
- JEDEC standard pinout
- Manufacturer's identification code

Block Diagram



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Pin Names

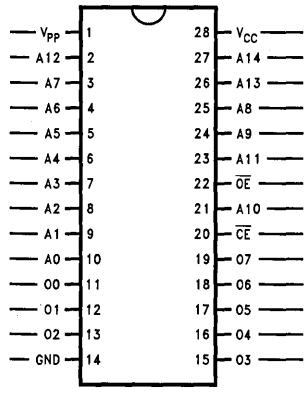
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

1

Connection Diagrams

27LC010	27LC512	27LC64
XX/V_{PP}		
A16		
A15	A15	V_{PP}
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O0	O0	O0
O1	O1	O1
O2	O2	O2
GND	GND	GND

DIP
NM27LC256



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27LC64	27LC512	27LC010
		V_{CC}
		XX/PGM
V_{CC}	V_{CC}	XX
$\overline{PGM}$	A14	A14
NC	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O7	O7	O7
O6	O6	O6
O5	O5	O5
O4	O4	O4
O3	O3	O3

Note: Compatible EPROM plan configurations are shown in the blocks adjacent to the NM27LC256 plan

Commercial Temperature Range
(0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC256 Q, N, 170	170
NM27LC256 Q, N, 200	200
NM27LC256 Q, N, 250	250

Extended Temperature Range
(−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC256 QE, NE, 170	170
NM27LC256 QE, NE, 200	200
NM27LC256 QE, NE, 250	250

Ordering Information

NM 27 LC 256 Q E 170

- National Memory
- EPROM
- Low Current
- Access Time
  - 170 = 170 ns
  - 200 = 200 ns
  - 250 = 250 ns
- Operating Temperature Range
  - E = Extended Temperature
- Blank—Commercial Temperature
  - Q = Ceramic DIP
  - N = Plastic DIP, OTP
- Package Size
  - 64 = 64k
  - 256 = 256k
  - 512 = 512k

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
All Input Voltages Except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

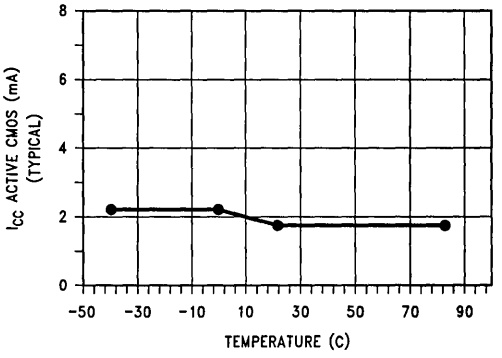
Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Level			−0.1		0.8	V
V_{IH}	Input High Level			2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		2.4			V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			0.5	100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			0.1	1.0	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE} = \overline{OE} V_{IL}$, F = 3 MHz Inputs V_{IH} or V_{IL}	Com'l		7.0	9.0	mA
			Ind'l		7.0	10.0	
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, F = 3 MHz Inputs = V_{CC} or GND, I/O = 0 mA (See *Figures 1, 2*)	Com'l		3.5	4.5	mA
			Ind'l		3.5	5.0	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$				10	
V_{PP}	V_{PP} Read Voltage			V_{CC}−0.7		V_{CC} + 0.7	
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1		1	
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10		10	

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	170		200		250		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250	
t_{OE}	$\overline{OE}$ to Output Delay		75		75		100	
t_{DF} (Note 2)	Output Disable to Output Float		60		60		60	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First		0		0		0	



TL/D/11405-3

FIGURE 1. I_{CC} ACTIVE CMOS vs Temperature $V_{CC} = V_P = 5.0V$, Frequency 1 MHz

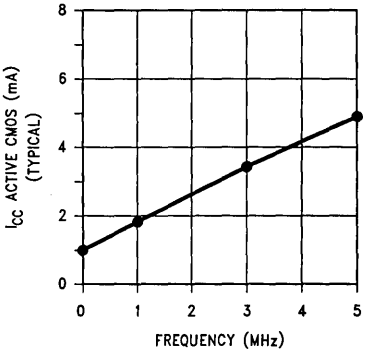


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FIGURE 2. I_{CC} ACTIVE CMOS vs Temperature vs Frequency $V_{CC} = V_{PP} = 5.0V$, Temperature = 25°C

Capacitance $T_A = +25°C$, 1 = 1 MHz (Note 2)

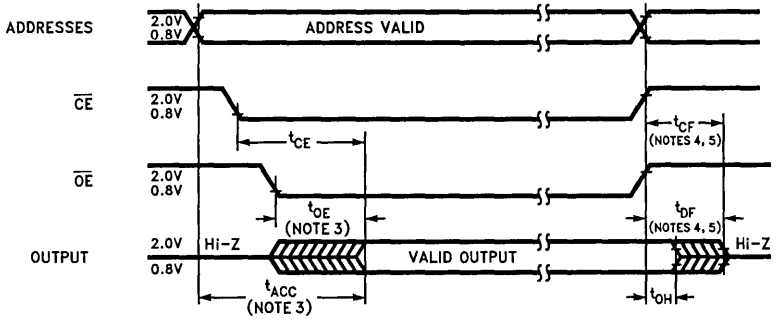
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Pulse Levels	≤ 5 ns

Input Pulse Level	0.45V to 2.4V
Timing Measurement Level (Note 10)	(Note 10)
Inputs	0.8V to 2V
Outputs	0.8V to 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/11405–5

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The T_{DF} and T_{CF} compare level is determined as follows:
High to TRI-STATE®, the measure V_{CH1} (DC) − 0.10V;
Low to TRI-STATE, the measure V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at last a 0.2 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA, C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

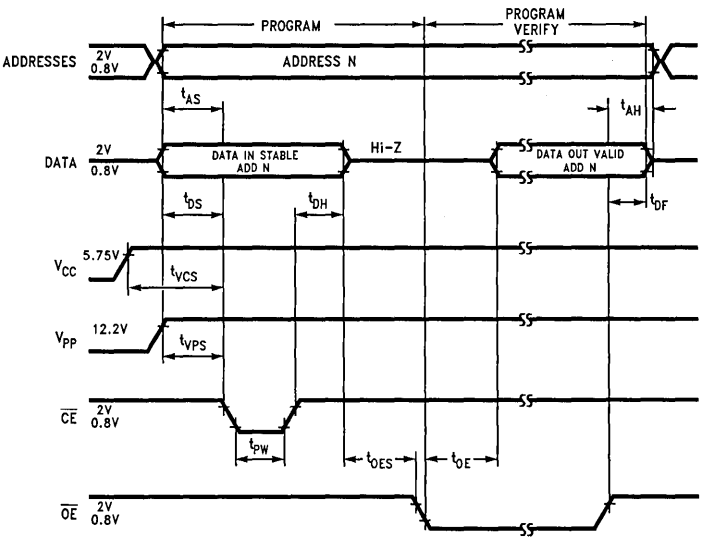
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS inputs V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ± 0.3V.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
$t_{\overline{OE}}$	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

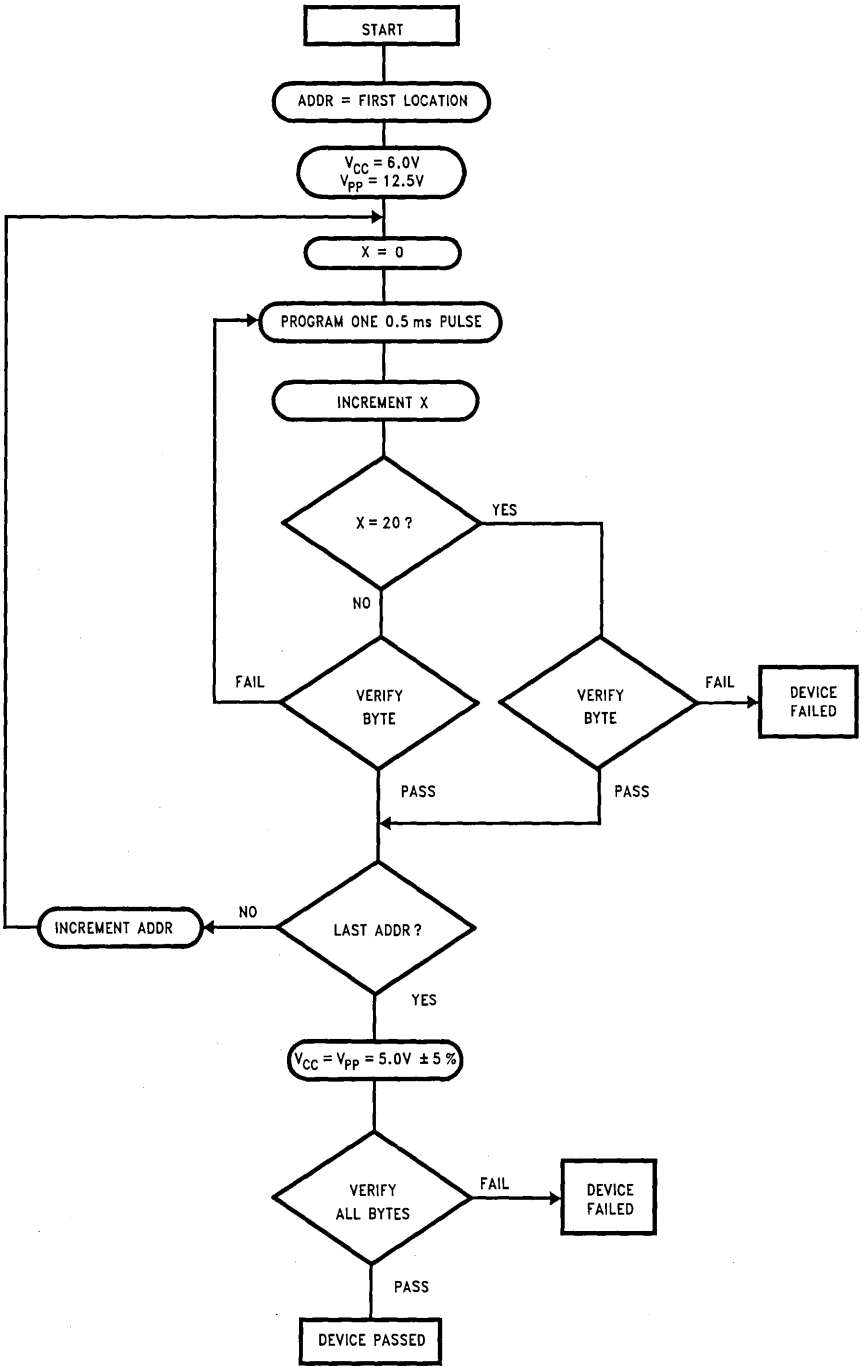
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the spurious V_{PP} voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Interactive Programming Algorithm Flow Chart



TL/D/11405–7

FIGURE 3

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.0V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 97%, from 24.75 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming; Interactive Algorithm

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Interactive Programming Algorithm shown in *Figure 3*. Each Address is programmed with a series of 500 μs pulses until it verifies good, up to a maximum of 20 pulses. Most memory cells will program with a single 500 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROMs $\overline{CE}$ input with V_{PP} at 13.0V will program that EPROM. A TTL high level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROM from being programmed.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	X	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27LC256 is "8FC4", where "8F" designates that it is made by National Semiconductor, and "C4" designates a 256k (32k8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IH}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristic of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	0	0	C4

National Semiconductor

PRELIMINARY

NM27LC512
524,288-Bit (64k x 8) Low Current CMOS EPROM

General Description

The NM27LC512 is a 64k x 8 EPROM manufactured on a proven, manufacturable CMOS process, consuming extremely low current in both the active and standby modes. The NM27LC512 consumes a mere 30 mW, making it ideal for portable and hand held computers, data acquisition and medical equipment, and for systems using in-line power.

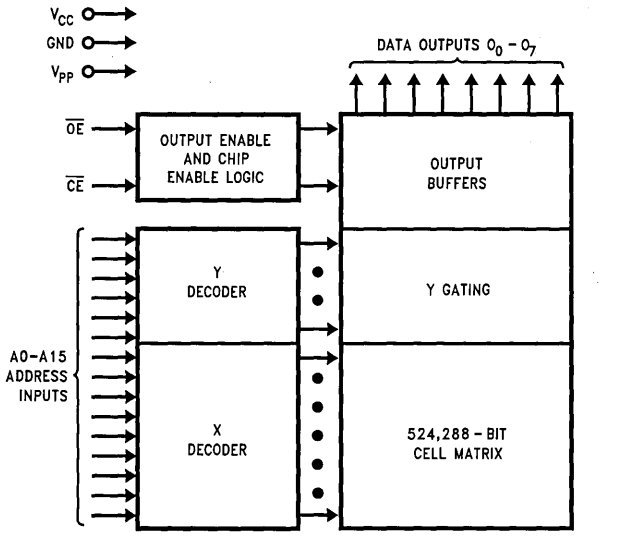
The NM27LC512 is one among a family of Power Miser products from National Semiconductor catering to the increasing low current demands of the market.

Offered in a JEDEC Standard Pinout, the NM27LC512 offers a viable alternative to the user as a replacement for existing high power devices, while also providing an upgrade path from lower densities.

Features

- Low CMOS power consumption
  - — 5V operation
  - — 8.0 mA (Max) active
  - — 100 μA (Max) standby
- 150 ns access time
- Latch-up immunity to 200 mA
- ESD protection exceeds 2000V
- JEDEC standard pinout
- Manufacturer's identification code

Block Diagram



TL/D/11406-1

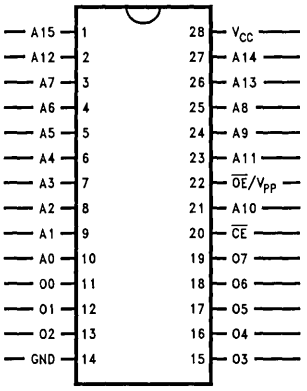
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Connection Diagram

27LC010	27LC256
XX/V_{PP}	
A16	
A15	V_{PP}
A12	A12
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O0	O0
O1	O1
O2	O2
GND	GND

DIP
NM27LC512



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27LC256	27LC010
	V_{CC}
	XX/$\overline{PGM}$
V_{CC}	XX
A14	A14
A13	A13
A8	A8
A9	A9
A11	A11
$\overline{OE}$	$\overline{OE}$
A10	A10
$\overline{CE}$	$\overline{CE}$
O7	O7
O6	O6
O5	O5
O4	O4
O3	O3

Note: Compatible EPROM plan configurations are shown in the blocks adjacent to the NM27LC256 plan.

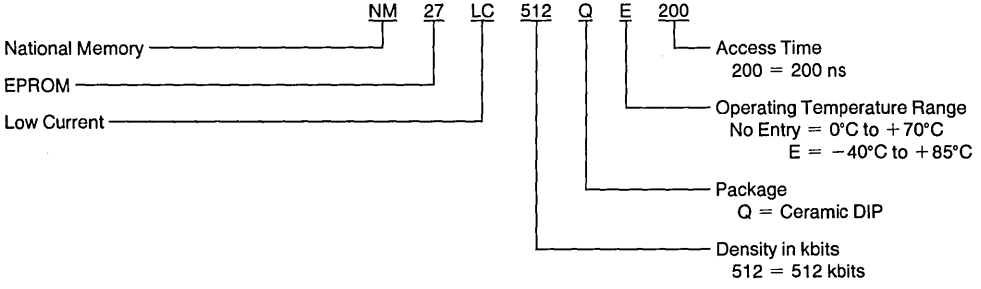
Commercial Temperature Range
(0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC256 Q, N 150	150
NM27LC256 Q, N 200	200
NM27LC256 Q, N 250	250

Extended Temperature Range
(−40°C to +85°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NM27LC256 QE, NE 150	150
NM27LC256 QE, NE 200	200
NM27LC256 QE, NE 250	250

Ordering Information



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages Except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

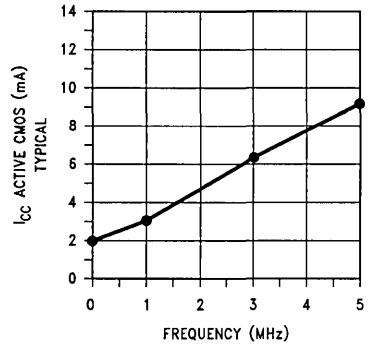
Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Level		−0.2		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
I_{SB1}	V_{CC} Standby Current CMOS Inputs	$\overline{CE} = V_{CC} \pm 0.3V$	0.5	0.5	100	μA
I_{SB2}	V_{CC} Standby Current TTL Inputs	$\overline{CE} = V_{IH}$	0.1	0.1	1.0	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE} = \overline{OE} = V_{IL}$, f = 3 MHz Inputs = V_{IH} or V_{IL}		16.0	12.5	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 3 MHz Inputs = V_{CC} or GND, I/O = 0 mA (Refer to *Figures 1, 2*)	5.0	6.0	8.0	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1		1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10		10	μA

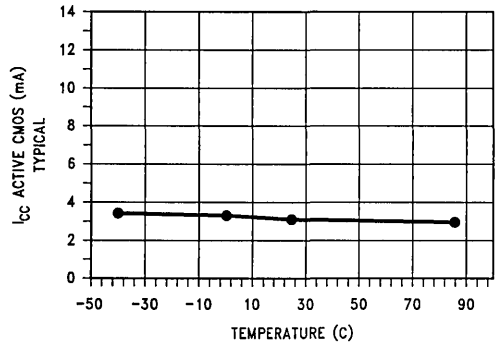
AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	150		200		250		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250	
t_{OE}	$\overline{OE}$ to Output Delay		60		75		100	
t_{DF} (Note 2)	Output Disable to Output Float		50		55		60	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First		0		0		0	



TL/D/11406-3

FIGURE 1. I_{CC}—ACTIVE—CMOS vs Frequency
V_{CC} = V_P = 5.0V, Temperature = 25°C



TL/D/11406-4

FIGURE 2. I_{CC}—ACTIVE—CMOS vs Temperature
V_{CC} = V_{PP} = 5.0V, Frequency = 1 MHz

1

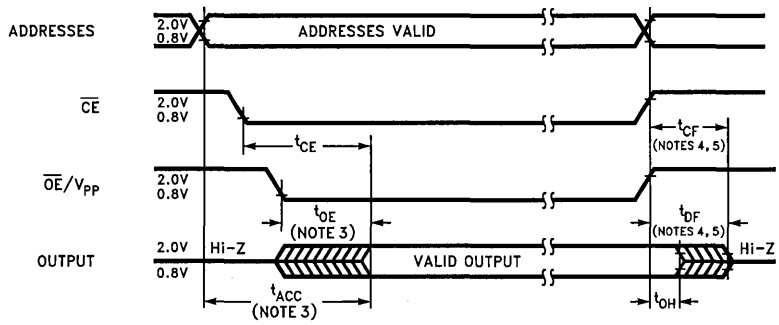
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	(Note 9)
Inputs	0.8V to 2V
Outputs	0.8V to 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/11406–5

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The T_{DF} and T_{CF} compare level is determined as follows:
High to TRI-STATE®, the measure V_{CH1} (DC) − 0.10V;
Low to TRI-STATE, the measure V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.

C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 10: CMOS inputs V_{IL} = GND ±0.3V, V_{IH} = V_{CC} ± 0.3V.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{cf}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2	V

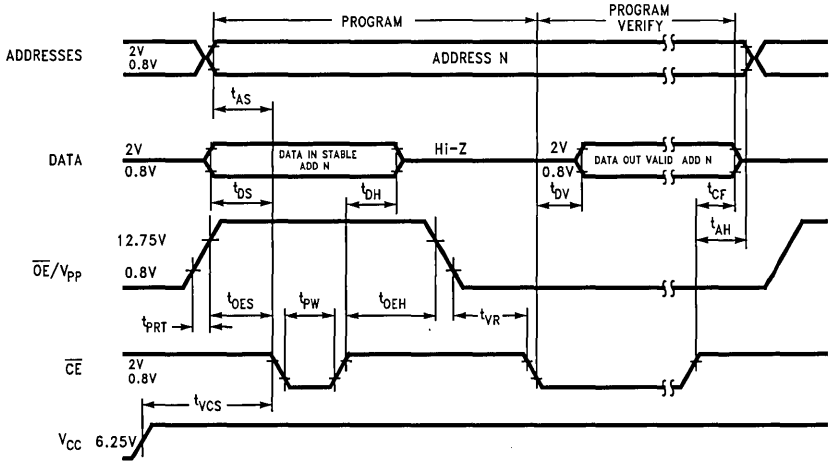
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

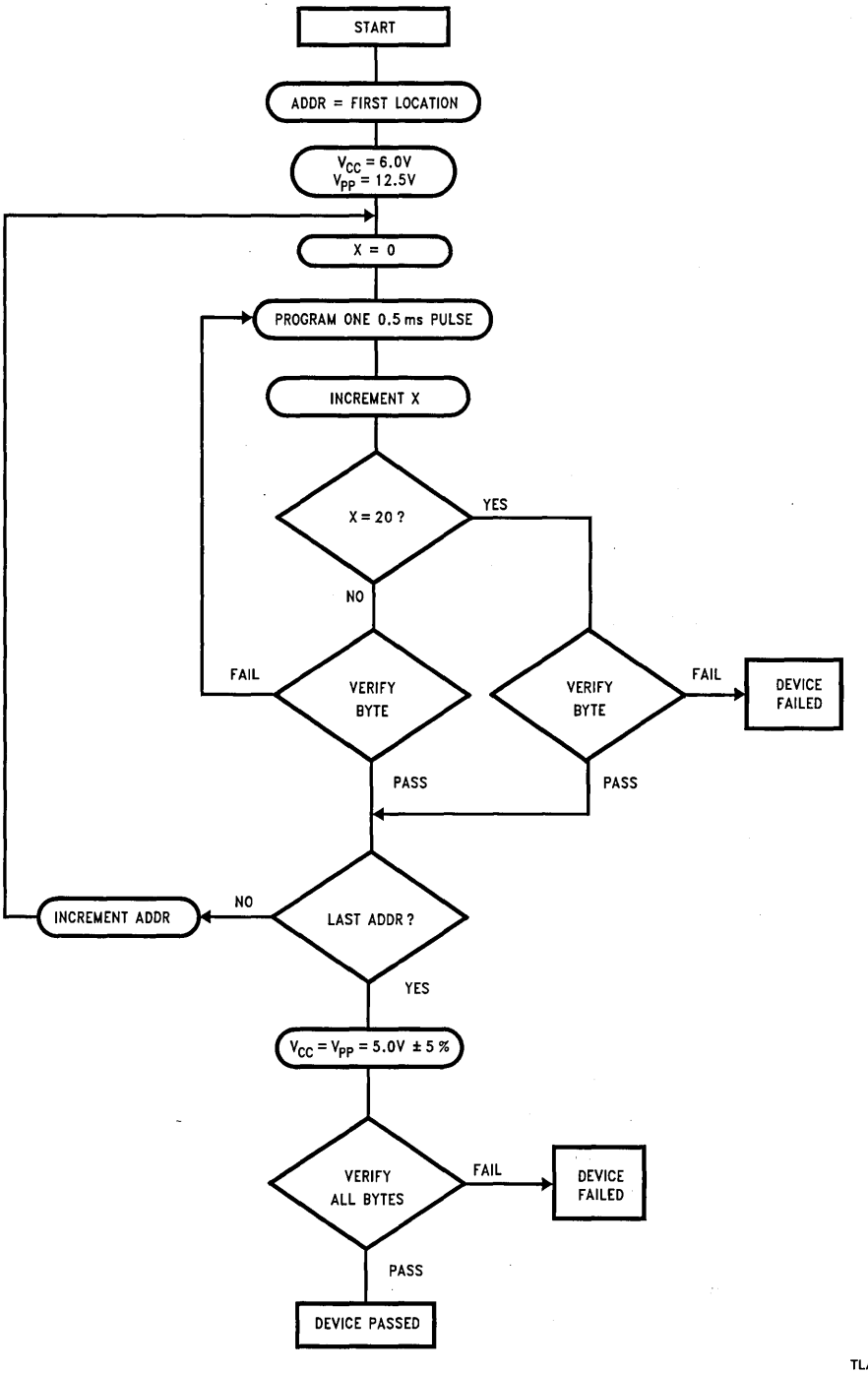
Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Programming Waveforms



TL/D/11406–6

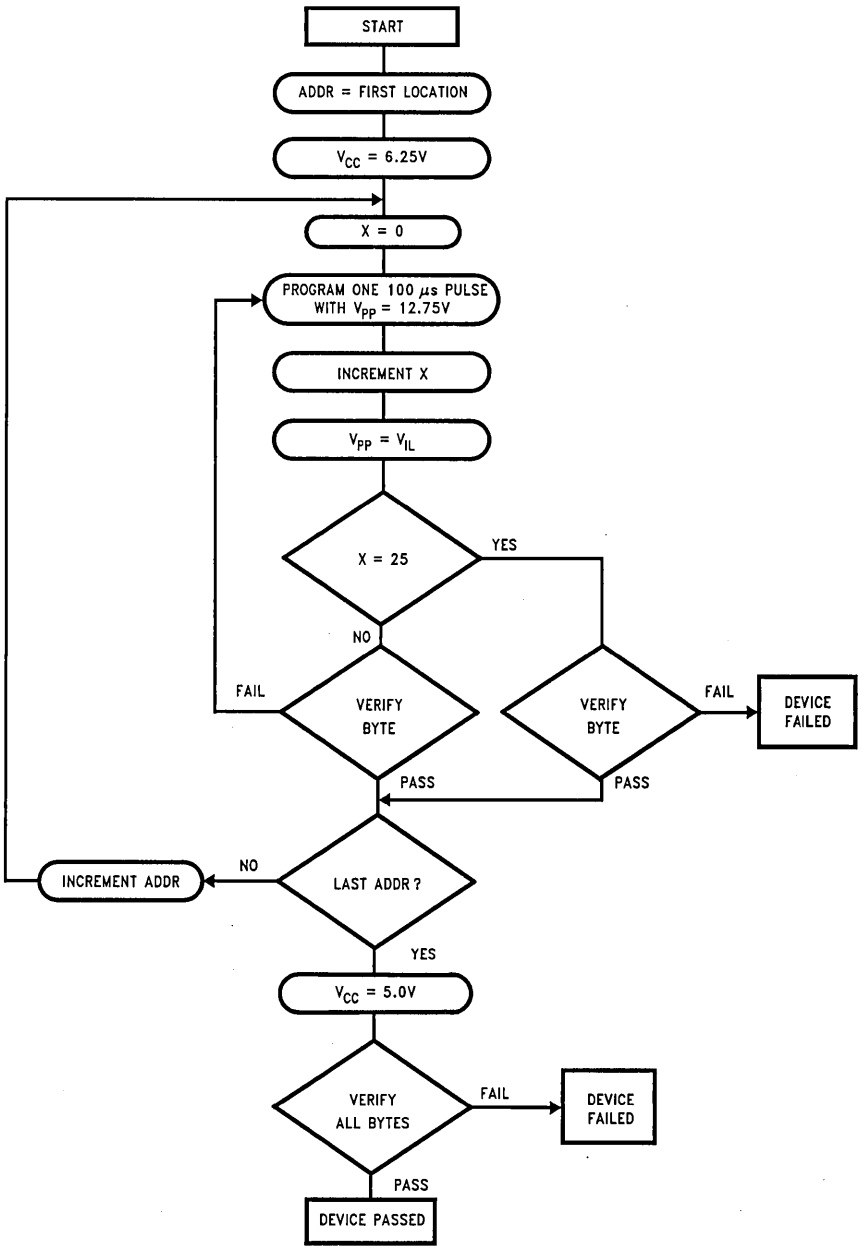
Interactive Programming Algorithm Flow Chart



TL/D/11406–8

FIGURE 3

Fast Programming Algorithm Flow Chart



TL/D/11406–7

FIGURE 4

Functional Description

DEVICE OPERATION

The six modes of operation of the NM27LC512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NM27LC512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NM27LC512 has a standby mode which reduces the active power dissipation by over 99%, from 44 mW to 0.55 mW. The NM27LC512 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Typing

Because the NM27LC512 is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the NM27LC512.

Initially, and after each erasure, all bits of the NM27LC512 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NM27LC512 is in the programming mode when the $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed.

The NM27LC512 is programmed with the Fast Programming Algorithm shown in *Figure 4*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The NM27LC512 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NM27LC512 in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NM27LC512 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NM27LC512.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 3*).

Mode Selection

The modes of operation of the NM27LC512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	X	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

Functional Description (Continued)

Program Inhibit

Programming multiple NM27LC512 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NM27LC512 may be common. A TTL low level program pulse applied to an NM27LC512's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NM27LC512. A TTL high level $\overline{CE}$ input inhibits the other NM27LC512 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Manufacturer's Identification Code

The NM27LC512 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NM27LC512 is , "8F 85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NM27LC512 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NM27LC512 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NM27LC512 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NM27LC512 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NM27LC512 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	0	0	04

TABLE III. Minimum NM27LC512 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

ADVANCE INFORMATION

NM27LV512
524,288-Bit (64k x 8) Low Voltage EPROM

General Description

The NM27LV512 is a high performance Low Voltage Electrical Programmable Read Only Memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over commercial temperature (0°C to 70°C), and 250 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive handheld and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its' commitment to high quality and reliability with EPI processing on the NM27LV512. Latch-up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is guaranteed 2000V.

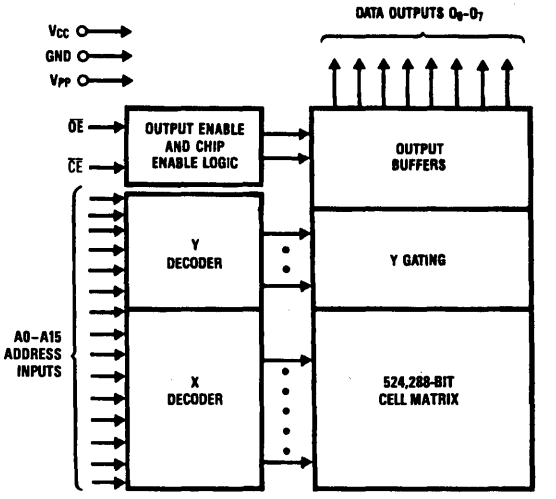
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has forseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive users.

The NM27LV512 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 5.5V operation
- 200 ns access time
- Low current operation
  - — 12 mA I_{CC} Active Current @ 5 MHz
  - — 20 μA I_{CC} Standby Current @ 5 MHz
- Ultra Low Power operation
  - — 50 μW Standby Power @ 3.3V
  - — 50 mW Active Power @ 3.3V
- High reliability EPI processing
  - — Latch up immunity up to 200 mA
  - — 2000V ESD protection
- Surface mount package options
  - — 28-pin CERPACK
  - — 28-pin PLCC
  - — 28-pin TSOP

Block Diagram



TL/D/11375–1

National Semiconductor

PRELIMINARY

NM27LV010
1,048,576-Bit (128k x 8) Low Voltage EPROM

General Description

The NM27LV010 is a high performance Low Voltage Electrically Programmable Read Only Memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over Industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its commitment to high quality and reliability with EPI processing on the NM27LV010. Latch-up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is guaranteed for 2000V.

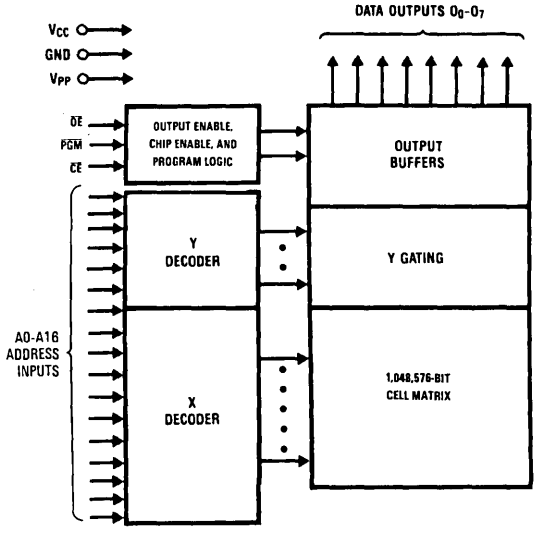
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive applications.

The NM27C010 is one member of National's growing Low Voltage product Family.

Features

- 3.0V to 5.5V operation
- 200 ns access time
- Low current operation
  - 15 mA I_{CC} active current @ 5 MHz
  - 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - 33 μW standby power @ 3.3V
  - 50 mW active power @ 3.3V
- High reliability EPI processing
  - Latch-up immunity up to 200 mA
  - 2000V ESD protection
- Surface mount package options
  - TSOP package
  - 32-pin PLCC

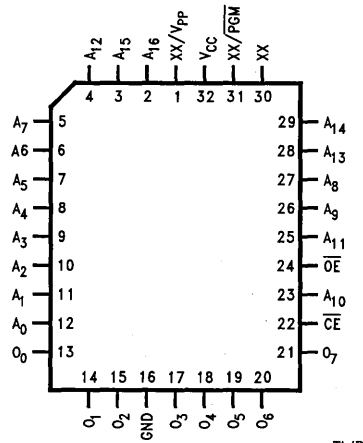
Block Diagram



TL/D/11377–1

Connection Diagram

PLCC and CLCC Pin Configuration



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Top View

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 3.3 ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV010 L, V, T 200	200
NM27LV010 L, V, T 250	250
NM27LV010 L, V, T 300	300

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
V_{PP}	Programming Voltage

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 3.3 ± 0.3

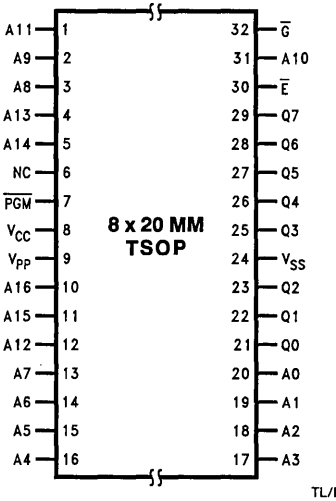
Parameter/Order Number	Access Time (ns)
NM27LV010 LE, VE, TE	250
NM27LV010 LE, VE, TE	300

Note: Surface mount PLCC available for commercial and extended temperature ranges only.

Package Types: NM27LV010 L, V, T
L = Quartz-Windowed LCC Package
T = TSOP
V = PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

TSOP Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3V	±0.3
Industrial	−40°C to +85°C	3.3V	±0.3

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.3	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.0 mA			0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = −2.0 mA		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 100 μA			0.2	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = −100 μA		V_{CC} − 0.3		
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			20	μA
I_{SB2}	V_{CC} Standby Current(TTL)	$\overline{CE}$ = V_{IH}			100	μA
I_{CC}	V_{CC} Active Current	$\overline{CE}$ + $\overline{OE}$ = V_{IL}	f = 5 MHz		15	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 3.0V or GND			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 3.0V or GND		−1	1	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		300		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	200			120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay	200			120		150	
t_{OE}	$\overline{OE}$ to Output Delay	70		70		75		
t_{DF} (Note 2)	Output Disable to Output Float	50		50		60		
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		

Capacitance $T_A = +25°C$, 1 = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

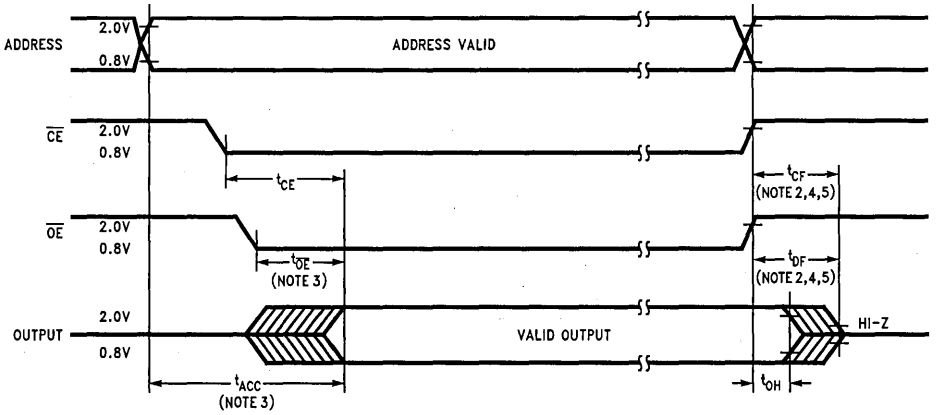
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/11377–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.2 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

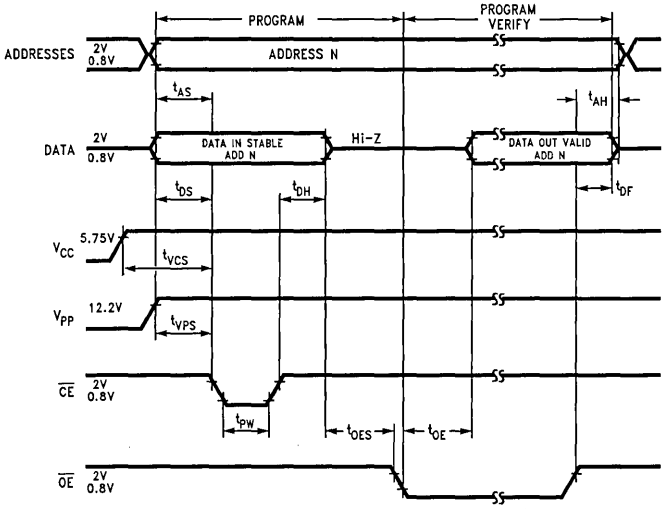
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveform (Note 3)



TL/D/11377–4

Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

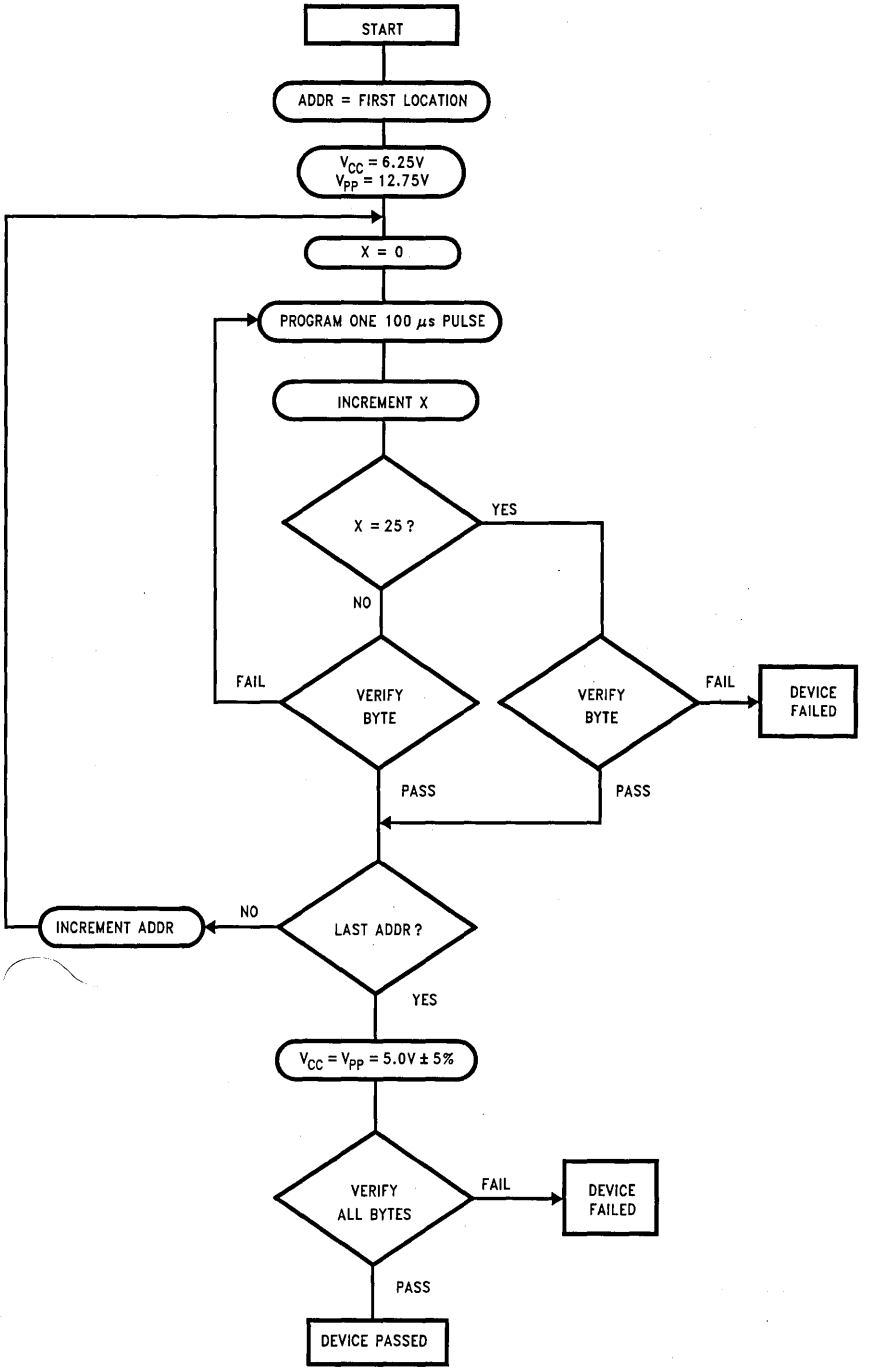
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11377–5

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 50 mW to 33 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP} and V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27LV010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1 Megabit (128k x 8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0–07. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV010 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	3.3V	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	3.3V	High Z
Standby	V_{IH}	X	V_{CC}	3.3V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

National Semiconductor

ADVANCE INFORMATION

NM27LV210
1,048,576-Bit (64K x 16) Low Voltage EPROM

General Description

The NM27LV210 is a high performance Low Voltage Electrical Programmable read only memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over commercial temperature (0°C to +70°C) and 250 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its commitment to High Quality and Reliability with EPI processing on the NM27LV210. Latch up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is also guaranteed up to 2000V.

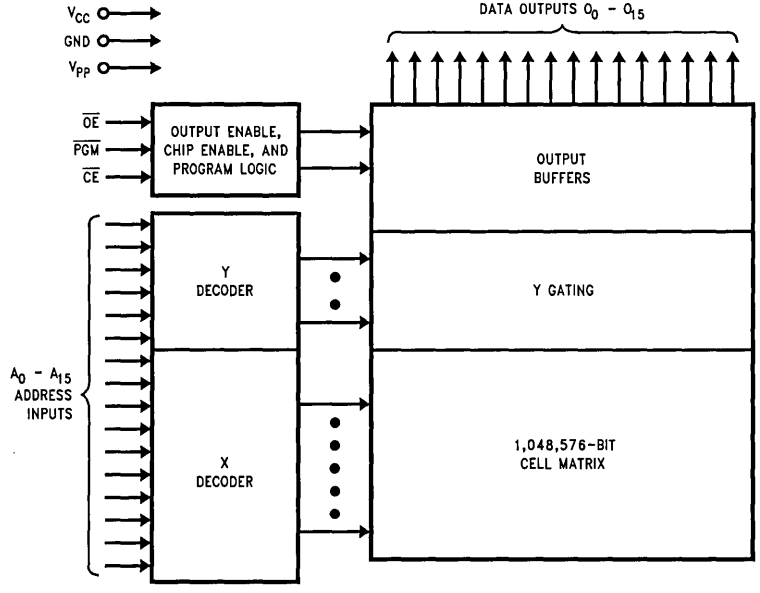
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive users.

The NM27LV010 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 5.5V operation
- 200 ns maximum access time
- Low current operation
  - — 15 mA I_{CC} active current @ 5 MHz
  - — 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - — 60 μA standby power @ 3.3V
  - — 50 mW active power @ 3.3V
- High reliability EPI processing
  - — Latch up immunity up to 200 mA
  - — 2000V ESD protection
- Surface mount package options
  - — TSOP package
  - — 44-Pin PLCC

Block Diagram



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Section 2

CMOS EEPROMs

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I²C CMOS EEPROM Selection Guide

General Description

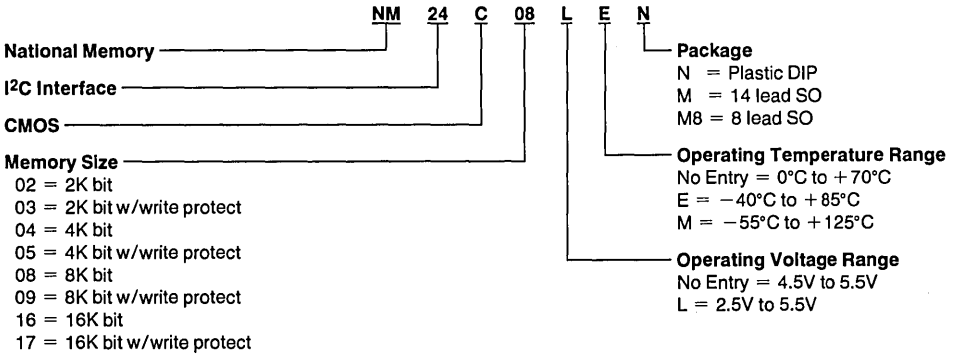
National Semiconductor's family of I²C CMOS EEPROMs share the following features: A serial interface and software protocol allowing operation on a two wire bus. Also, programming of the upper half of the memory can be disabled by connecting the WP pin to V_{CC} on certain members of the family.

National Semiconductor EEPROMs offer 100,000 write cycles guaranteed—500,000 typical with data retention greater than 40 years. The I²C CMOS EEPROMs are all available in DIP and SO packaging.

Features

- Low power CMOS
  - 2 mA active current typical
  - 60 μA standby current typical
- Hardwire write protect for upper half of memory
- 2 wire serial interface
- Bidirectional data transfer protocol
- Sixteen byte page write mode
  - Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 5 ms
- Data retention greater than 40 years
- 8-pin mini-DIP, 8-pin SO or 14-pin SO package

Available Product	Packages	Temperature Ranges	4.5V–5.5V	2.5V–5.5V	Security
NM24C02	N, M, M8	C, E, M	Y	Y	
NM24C03	N, M, M8	C, E, M	Y	Y	Y
NM24C04	N, M, M8	C, E, M	Y	Y	
NM24C05	N, M, M8	C, E, M	Y	Y	Y
NM24C08	N, M	C, E, M	Y		
NM24C09	N, M	C, E, M	Y		Y
NM24C16	N, M	C, E, M	Y		
NM24C17	N, M	C, E, M	Y		Y



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MICROWIRE™ CMOS EEPROM Selection Guide

General Description

National Semiconductor offers a family of CMOS EEPROMs which share the following features: MICROWIRE Serial Interface, floating gate M²CMOS™ technology, 5V only operation, 100,000 cycle operation, Directwrite†, and self-timed programming cycle with programming status on the data out pin. All of these devices are offered in compatible packages and pinouts.

There are also several features not shared by all family members, which separate the family into three groups. These features are **operating voltage range, write protection,** and **sequential register read.** Other differences are memory size, packaging, and operating temperature range. Although, for the purpose of this selection guide, the family will not be separated by these differences, as each individual device is available with all of these variants.

Features

- 40 year data retention
- Extended voltage operation
- Endurance: 10^6 data changes
- Reliable CMOS floating gate technology
- Single voltage operation in all modes
- MICROWIRE compatible serial interface
- Directwrite†, no erase cycles required
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential Register Read*
- User configurable write protection*

*Features available on NM93CS only.

Available Product

	Packages	Temperature Ranges	4.5V–5.5V	2.0V–5.5V*
NM93CS06	N, M8	C, E, M	Y	Y
NM93CS46	N, M8	C, E, M	Y	Y
NM93CS56	N, M8	C, E, M	Y	Y
NM93CS66	N, M	C, E, M	Y	Y
NM93C06	N, M8	C, E, M	Y	Y
NM93C46	N, M8	C, E, M	Y	Y
NM93C56	N, M8	C, E, M	Y	Y
NM93C66	N, M8	C, E, M	Y	Y

*Extended Voltage (2.0–5.5) operation is not available on the M Temperature Range (−55°C to +125°C)

NOTE: For 14-Pin SO availability, contact local sales office.

NM 93 C S 06 L E M8

National Memory

Microwire Interface

CMOS

Features
- No Entry = Standard
- S = User programmable write protection and sequential read

Memory Size
- 06 = 256 bit
- 46 = 1024 bit
- 56 = 2048 bit
- 66 = 4096 bit

Operating Voltage Range
- L = 2.0V to 5.5V
- No Entry = 4.5V to 5.5V

Operating Temperature Range
- No Entry = 0°C to +70°C
- E = −40°C to +85°C
- M = −55°C to +125°C

Package
- N = Plastic DIP
- J = Ceramic DIP
- M = 14 Lead SO
- M8 = 8 Lead SO

†Directwrite allows directly writing over existing data, without erasing.

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Specialty Products CMOS EEPROM Selection Guide

General Description

National Semiconductor offers a full line of CMOS EEPROMs. Some share the MICROWIRE™ Serial Interface such as the NM93C06 and the NM93CS06; others share the I²C (2 wire) Interface such as the NM24C02 and the NM24C08. In addition to the above EEPROMs, we also offer some specialty EEPROMs.

These include the NM95C12, NM93C46A and the NM59C11 EEPROMs.

Features

- No erase necessary
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Compatible with COPS™ Microcontroller
- Reliable CMOS floating gate technology

The **NM95C12** is a 976-bit CMOS EEPROM with 8 programmable outputs that can be used as DIP switches. The 976 bits of memory are divided into 61 registers of 16 bits each with each register individually accessible. Registers 61–63 are dedicated for DIP switch functions. The NM95C12 contains 8 individually programmable outputs which can be used as switches.

The **NM93C46A** and the **NM59C11** are both 1024 bits of CMOS EEPROM which can be organized as either 64 16-bit registers or as 128 8-bit registers. The NM93C46A and the NM59C11 share the MICROWIRE Interface and the x8 and x16 configuration. The differentiating feature is in the pin configuration: The NM93C46A's Program/Erase status is output on the Data-Out (DO) pin; the NM59C11's on a separate RDY/BUSY pin. Both devices use a low to high transition on the clock (SK) to clock all data into or out of the device, except device programming status which is independent of the clock.

Available Product

	Packages	Temperature Ranges	4.5V–5.5V	2.0V–5.5V
NM95C12	N, M	C, E, M	Y	
NM93C46A	N, M8	C, E, M	Y	Y
NM59C11	N, M8	C, E, M	Y	

National Semiconductor

NM24C02/C04/C08/C16
2K-/4K-/8K-/16K-Bit Serial EEPROM (I²C Synchronous 2-Wire Bus)

General Description

The NM24C02/C04/C08/C16 devices are 2048/4096/8192/16,384 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements.

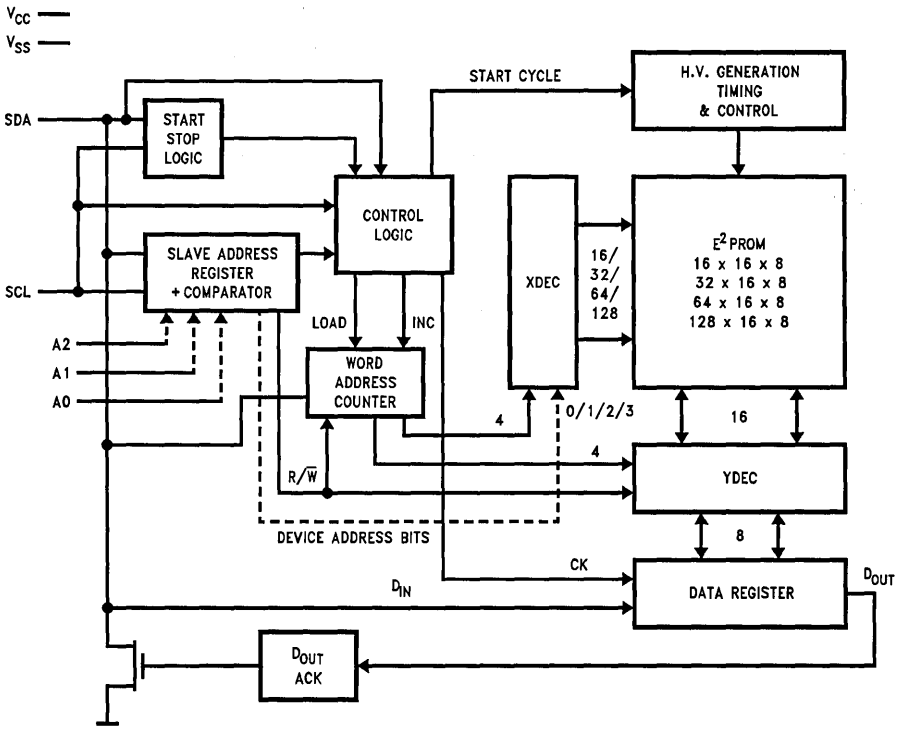
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Low Power CMOS
  - 2 mA active current typical
  - 60 μA standby current typical
- 2-wire I²C serial interface
  - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 14 pin SO package

Functional Diagram



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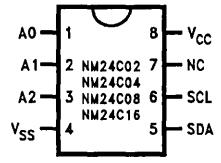
Connection Diagrams

Dual-In-Line Package (N)



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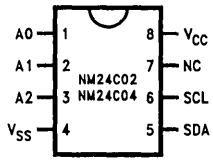
Top View

See NS Package Number N08E (N)

SO Package (M8)



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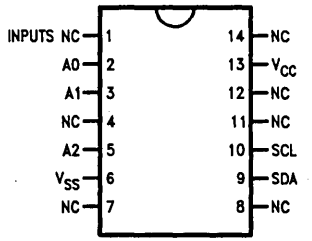
Top View

See NS Package Number M08A (M8)

SO Package (M)



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Top View

See NS Package Number M14B (M)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
V_{CC}	+5V

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C02N/NM24C04N/NM24C08N/NM24C16N NM24C02M/NM24C04M/NM24C08M/NM24C16M NM24C02M8/NM24C04M8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C02EN/NM24C04EN/NM24C08EN/NM24C16EN NM24C02EM/NM24C04EM/NM24C08EM/NM24C16EM NM24C02EM8/NM24C04EM8

Military Temperature Range (−55°C to +125°C)

Order Number
NM24C02MN/NM24C04MN/NM24C08MN/NM24C16MN NM24C02MM/NM24C04MM/NM24C08MM/NM24C16MM NM24C02MM8/NM24C04MM8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C02/C04/C08/C16	0°C to +70°C
NM24C02E/C04E/C08E/C16E	−40°C to +85°C
NM24C02M/C04M/C08M/C16M (Mil. Temperature)	−55°C to +125°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

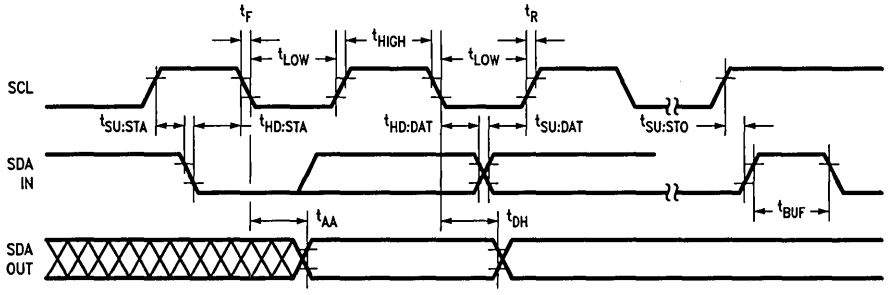
Note 2: This parameter is periodically sampled and not 100% tested.

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMS on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

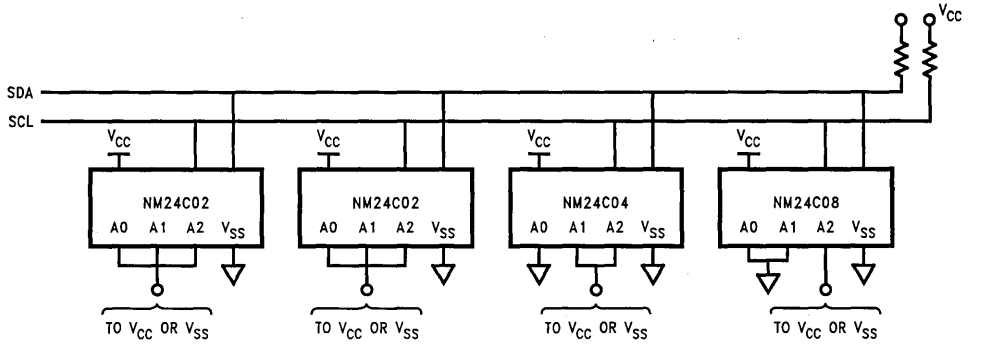
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16K (Maximum Size) of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note: It is recommended that the total line capacitance be less than 400 pF.

Note: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02	DA	DA	DA	2048 Bits	1
NM24C04	V_{SS}	DA	DA	4096 Bits	2
NM24C08	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C16	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02	ADR	ADR	ADR	$2^3 = 8$ (8) x (2K) = 16K
NM24C04	X	ADR	ADR	$2^2 = 4$ (4) x (4K) = 16K
NM24C08	X	X	ADR	$2^1 = 2$ (2) x (8K) = 16K
NM24C16	X	X	X	$2^0 = 1$ (1) x (16K) = 16K

ADR: Denotes an active pin used for device addressing
X: Not used for addressing (Must be tied to Ground/V_{SS})

Device Operation

The NM24Cxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

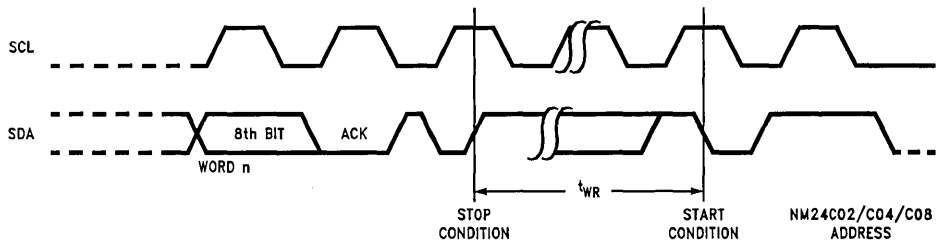
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

Write Cycle Timing



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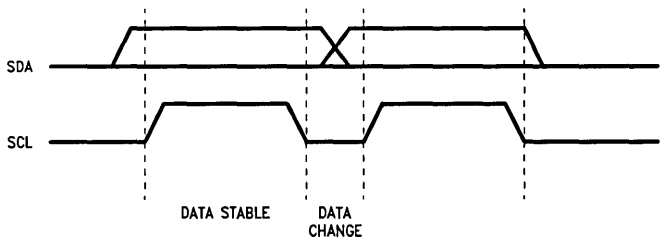

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FIGURE 1. Data Validity

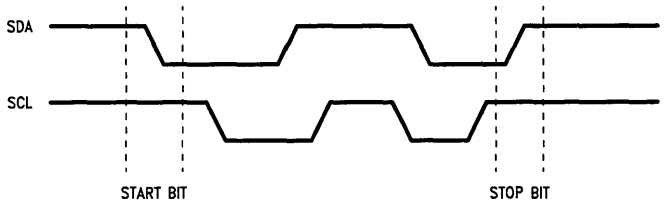

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FIGURE 2. Definition of Start and Stop

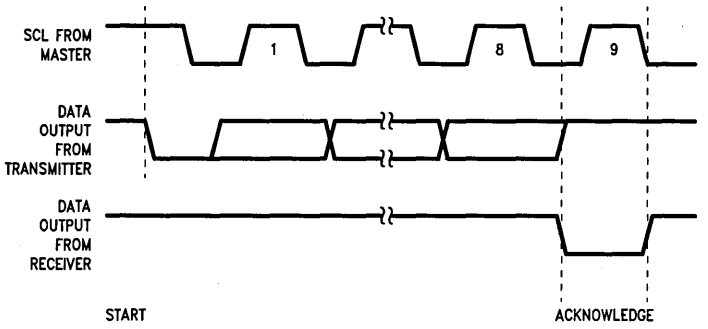


FIGURE 3. Acknowledge Response from Receiver

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3.*

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C02, NM24C04, NM24C08 and NM24C16.

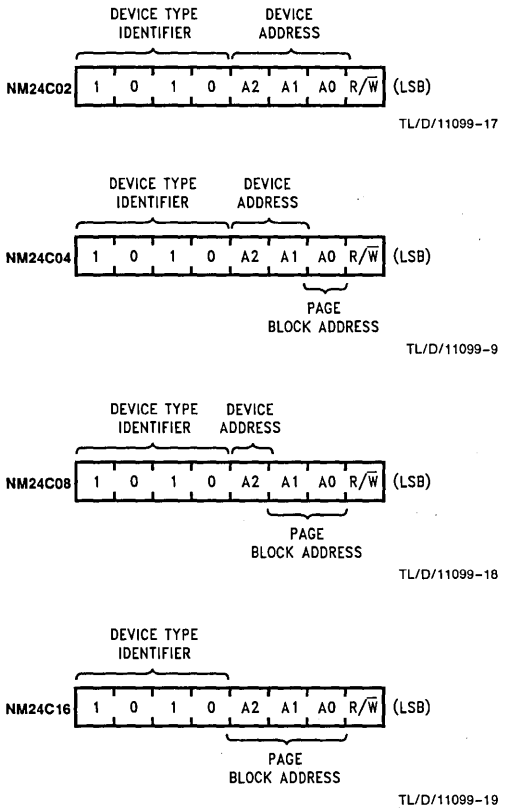


FIGURE 4. Slave Addresses

DEVICE ADDRESSING

Refer to the following table for Slave Addresss string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02	A	A	A	1 (2K)	(NONE)
NM24C04	P	A	A	2 (4K)	0 1
NM24C08	P	P	A	4 (8K)	00 01 10 11
NM24C16	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment

All I^2C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed, and a "0" initiates the write mode.

A simple review: After the NM24C02/C04/C08/C16 recognizes the start condition, the devices interfaced to the I^2C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

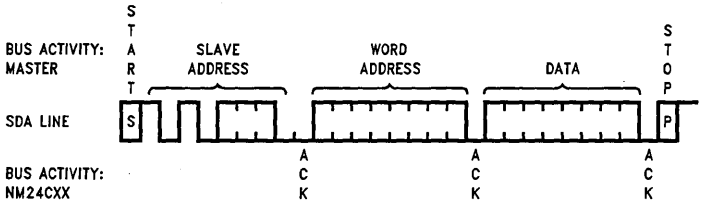
PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

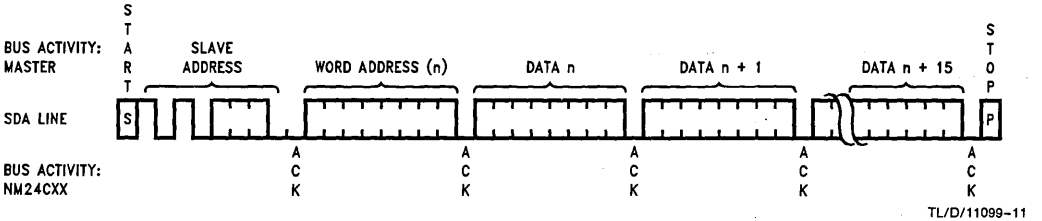
ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is still busy with the write operation no ACK will be returned. If the NM24Cxx has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.



TL/D/11099–10

FIGURE 5. Byte Write



TL/D/11099–11

FIGURE 6. Page Write

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

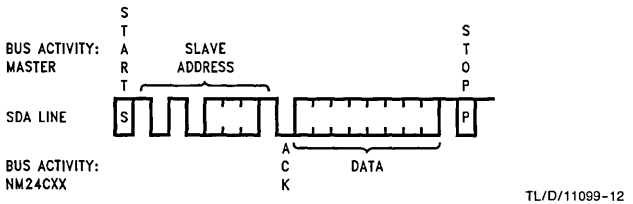


FIGURE 7. Current Address Read

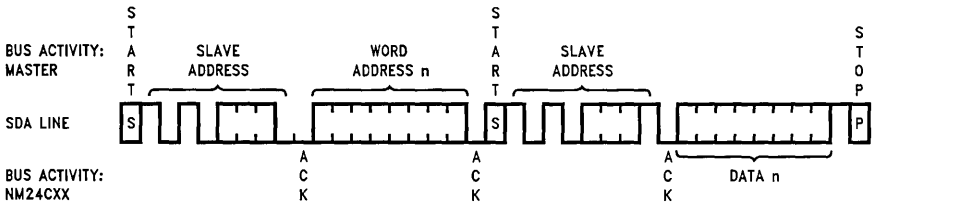


FIGURE 8. Random Read

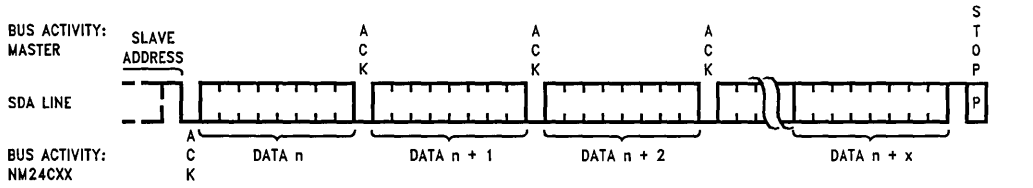


FIGURE 9. Sequential Read

Read Operations (Continued)

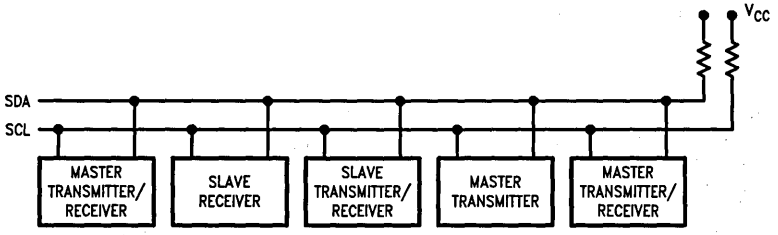


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FIGURE 10. Typical System Configuration

Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7 kΩ)

National Semiconductor

NM24C03/C05/C09/C17
2K-/4K-/8K-/16K-Bit Serial EEPROM with Write Protect (I²C Synchronous 2-Wire Bus)

General Description

The NM24C03/C05/C09/C17 devices are 2048/4096/8192/16,834 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol, and are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

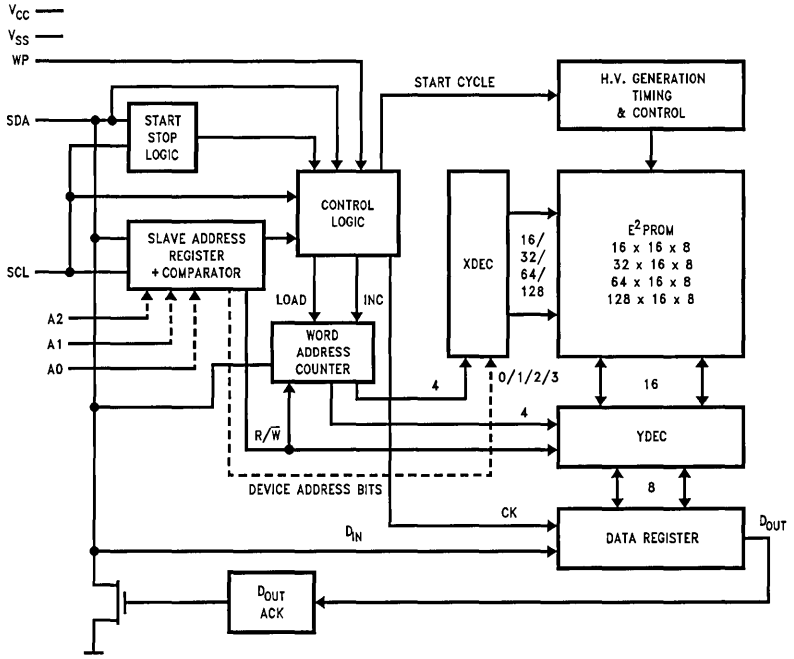
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features

- Hardwire write protect for upper block
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I²C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 14 pin SO package

Functional Diagram



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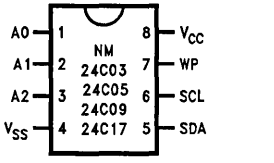
Connection Diagrams

Dual-In-Line Package (N)



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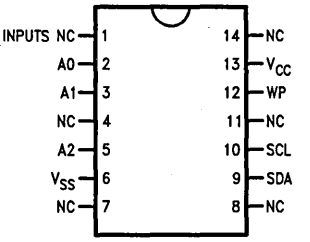
Top View

See NS Package Number N08E

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
V_{CC}	+5V
WP	Write Protect
NC	No Connection

SO Package (M)



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Top View

See NS Package Number M14B

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C03N/NM24C05N/NM24C09N/NM24C17N NM24C03M/NM24C05M/NM24C09M/NM24C17M

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C03EN/NM24C05EN/NM24C09EN/NM24C17EN NM24C03EM/NM24C05EM/NM24C09EM/NM24C17EM

Military Temperature Range (−55°C to +125°C)

Order Number
NM24C03MN/NM24C05MN/NM24C09MN/NM24C17MN NM24C03MM/NM24C05MM/NM24C09MM/NM24C17MM

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM24C03/C05/C09/C17	0°C to +70°C
NM24C03E/C05E/C09E/C17E	−40°C to +85°C
NM24C03M/C05M/C09M/C17M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ. (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A_0, A_1, A_2, SCL, WP)	V_{IN} = 0V	6	pF

A.C. Conditions of Test

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

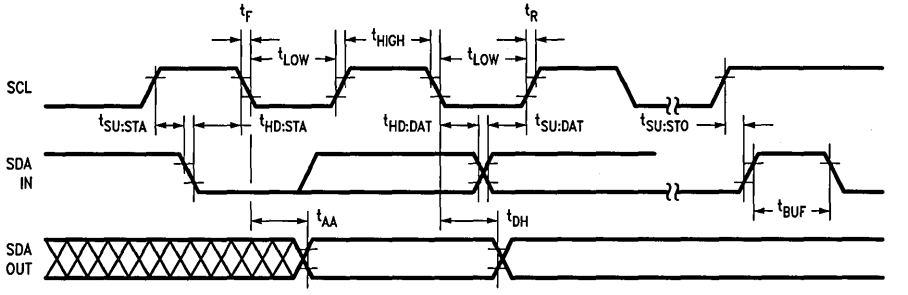
Note 2: This parameter is periodically sampled and not 100% tested.

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In additon, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

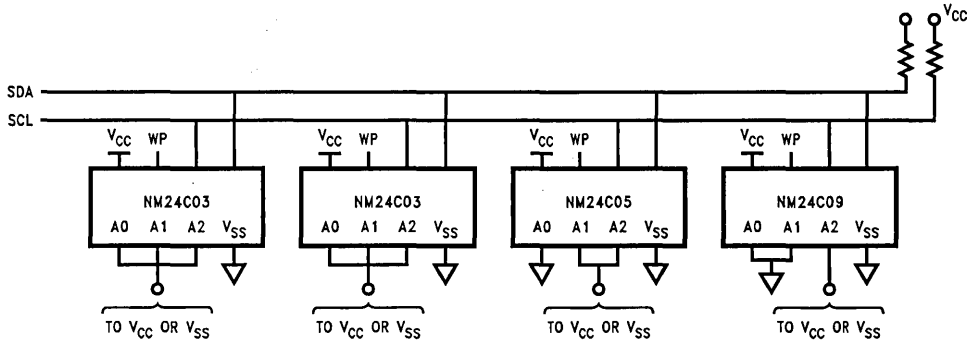
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string)

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16k (Maximum Size) of Memory on 2-Wire Bus



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Note:

The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.
It is recommended that the total line capacitance be less than 400 pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C03	DA	DA	DA	2048 Bits	1
NM24C05	V_{SS}	DA	DA	4096 Bits	2
NM24C09	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C17	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C04	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K
NM24C08	X	X	ADR	$2^1 = 2$ (2) × (8K) = 16K
NM24C16	X	X	X	$2^0 = 1$ (1) × (16K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

WP WRITE PROTECTION

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible.

If tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C03/C05/C09/C17 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx is considered a slave in all applications.

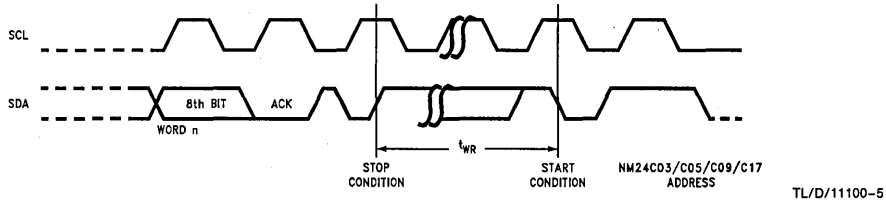
CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Write Cycle Timing



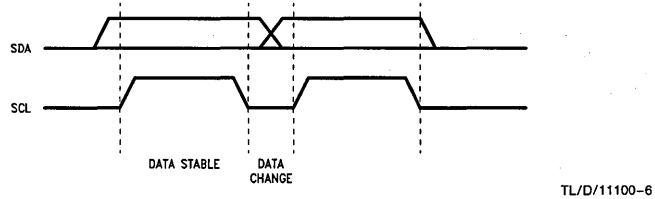


FIGURE 1. Data Validity

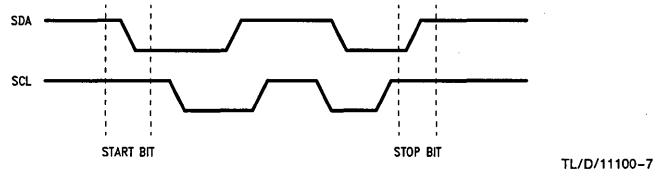


FIGURE 2. Definition of Start and Stop

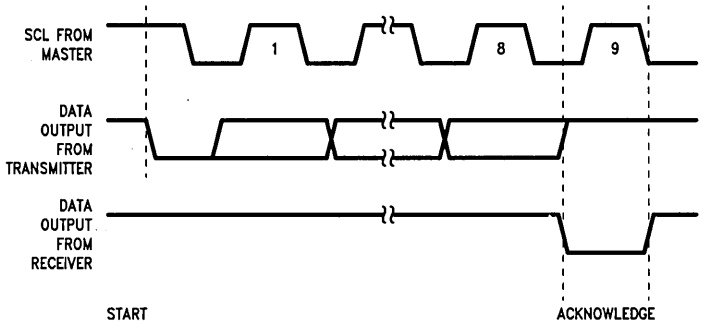


FIGURE 3. Acknowledge Response from Receiver

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C03, NM24C05, NM24C09 and NM24C17.

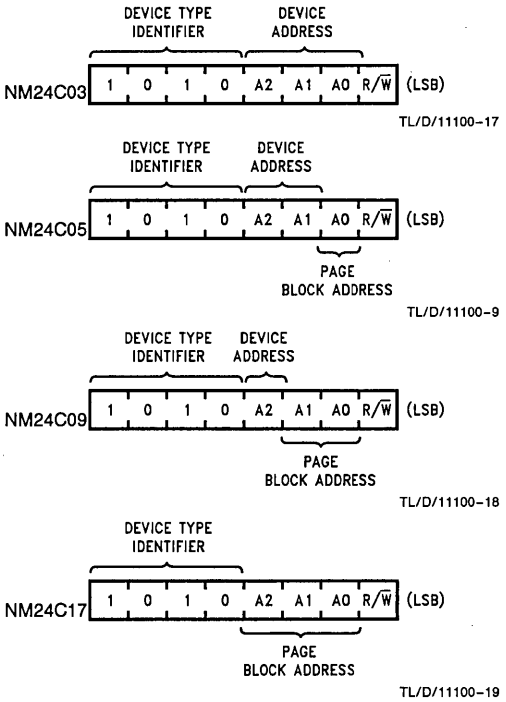


FIGURE 4. Slave Addresses

2

Device Addressing (Continued)

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02	A	A	A	1 (2K)	(None)
NM24C04	P	A	A	2 (4K)	0 1
NM24C08	P	P	A	4 (8K)	00 01 10 11
NM24C16	P	P	P	1 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C03/C05/C09/C17 recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

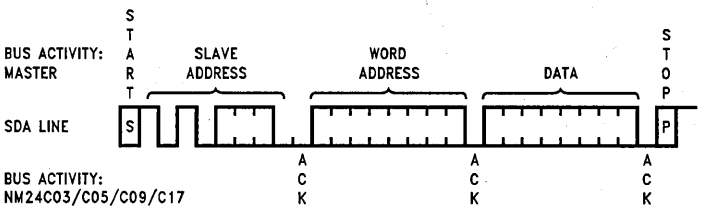


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FIGURE 5. Byte Write

Write Operations (Continued)

PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is still busy with the write operation, no ACK will be returned. If the NM24Cxx has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the NM24Cxx is connected to V_{CC} (+5V). The NM24Cxx will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24Cxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

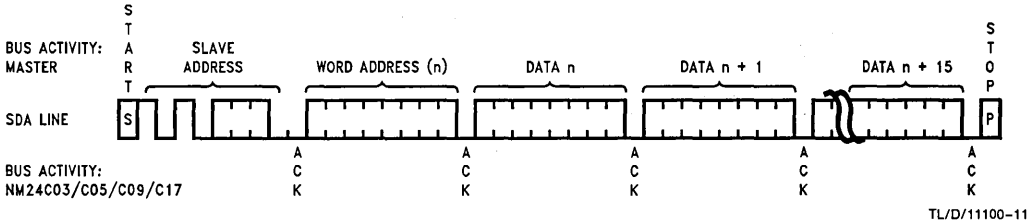

FIGURE 6. Page Write

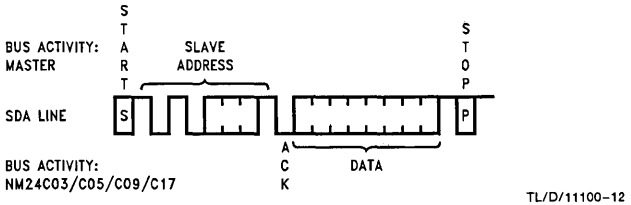

FIGURE 7. Current Address Read

Read Operations (Continued)

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

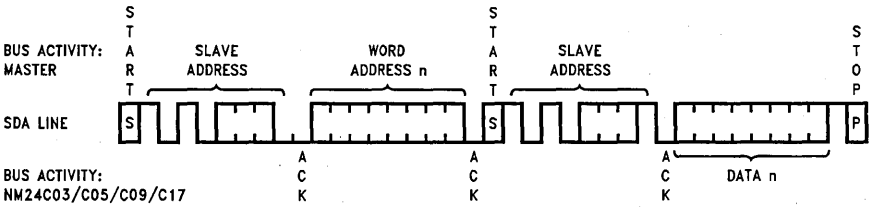

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FIGURE 8. Random Read

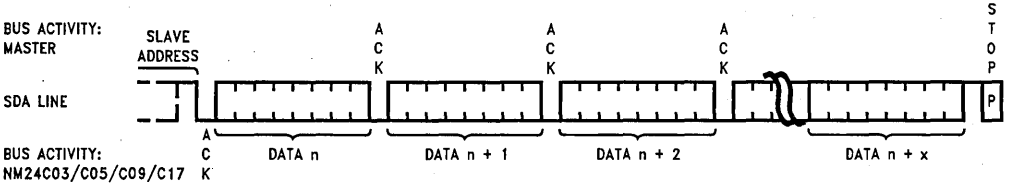

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FIGURE 9. Sequential Read

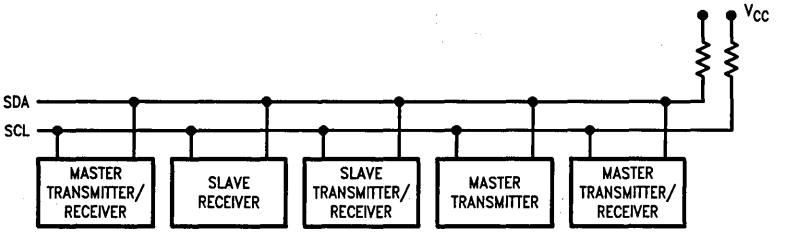

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FIGURE 10. Typical System Configuration

National Semiconductor

NM24C02L/C04L
2K-/4K-Bit Serial EEPROM with Extended Voltage (I^2C Synchronous 2-Wire Bus)

General Description

The NM24C02L/04L devices are 2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I^2C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements. National EEPROMs are designed and tested for applications requiring high reliability, high endurance and low power consumption.

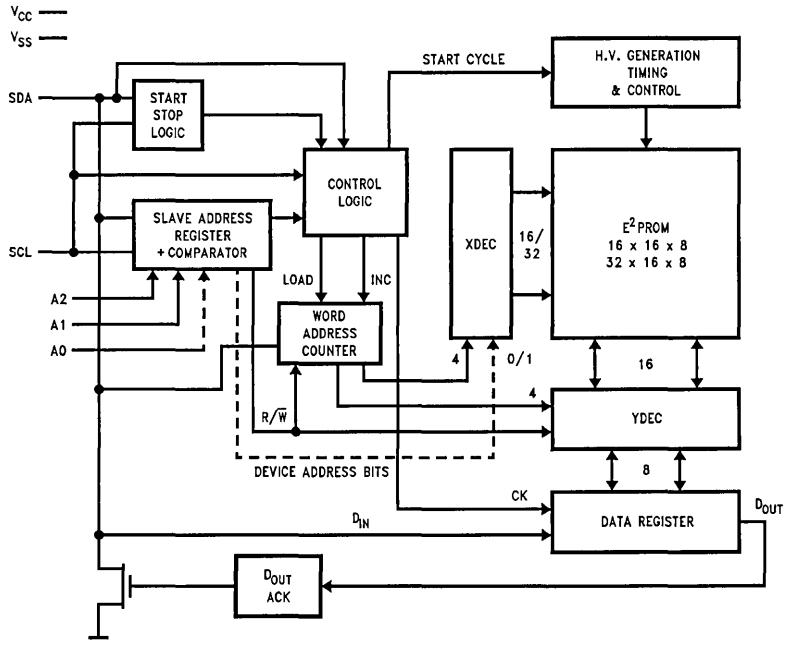
These devices have an operating voltage range of 2.5V to 5.5V and are offered in an 8-pin small outline (SO) package, making these devices perfectly suited for low power applications that require minimal board space usage.

This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

Features

- Extended operating voltage, 2.5V–5.5V
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I^2C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 8 pin SO package

Functional Diagram



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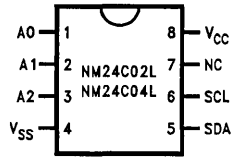
Connection Diagrams

Dual-In-Line Package (N) and SO Package (M8)



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Top View

See NS Package Number M08A (M8) and N08E (N)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
V_{CC}	+5V

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C02LN/NM24C04LN NM24C02LM/NM24C04LM

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C02LEN/NM24C04LEN NM24C02LEM/NM24C04LEM

LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM2402L/C04L	0°C to +70°C
NM24C02EL/04EL	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.5V to 4.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 200 μA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

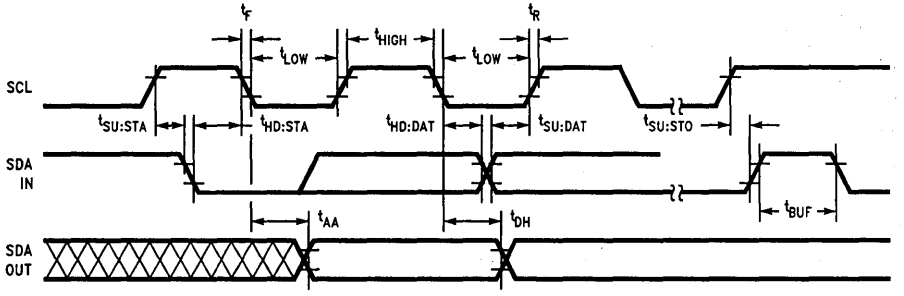
LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C02L/C04L	0°C to +70°C
NM24C02EL/C04EL	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

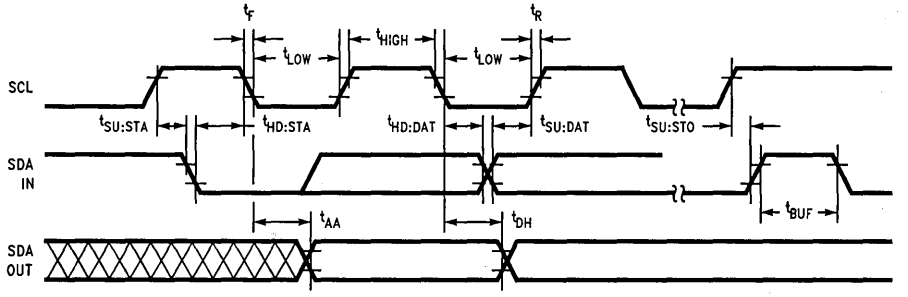
STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

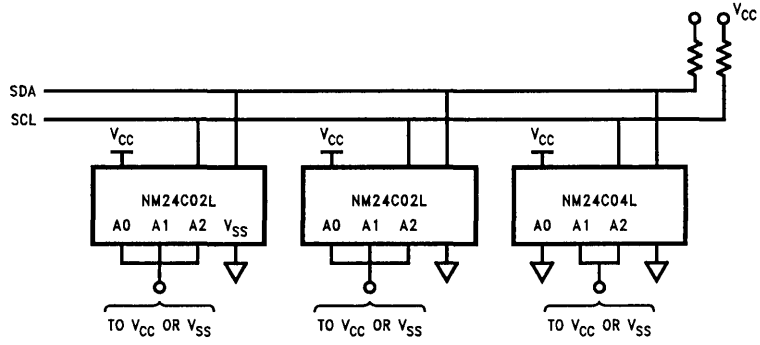
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 8K (½ of Maximum Size) of Memory on 2-Wire Bus



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Note 1: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note 2: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note 3: It is recommended that the total line capacitance be less than 400 pF.

Note 4: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02L	DA	DA	DA	2048 Bits	1
NM24C04L	V_{SS}	DA	DA	4096 Bits	2

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C04	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K
NM24C08	X	X	ADR	$2^1 = 2$ (2) × (8K) = 16K
NM24C16	X	X	X	$2^0 = 1$ (1) × (16K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

Device Operation

The NM24C02L/C04L supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the NM24C02L/C04L will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

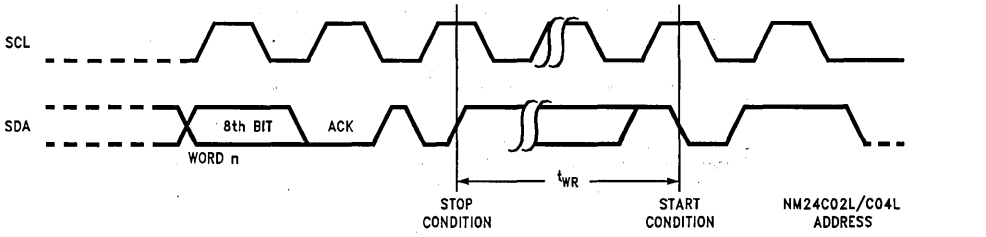
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24CxxL continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

Write Cycle Timing



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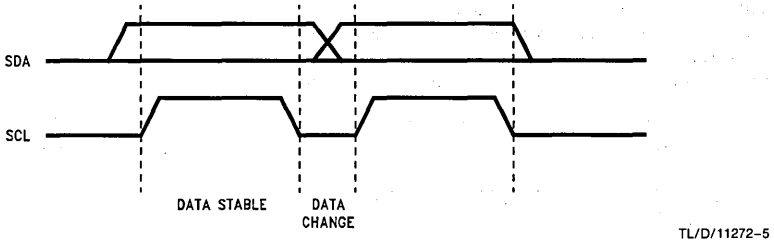

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FIGURE 1. Data Validity

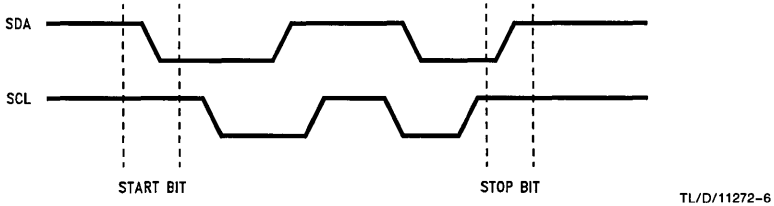

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FIGURE 2. Definition of Start and Stop

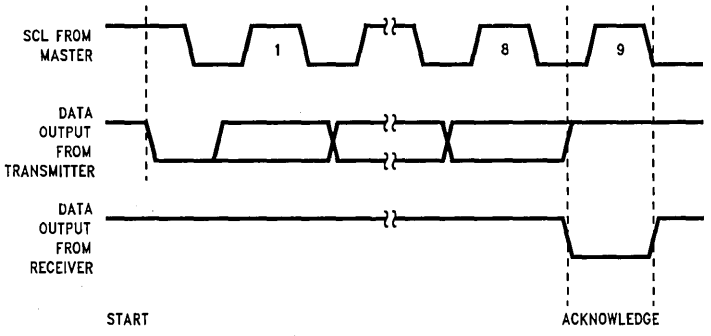

FIGURE 3. Acknowledge Response from Receiver

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24CxxL will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24CxxL will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24CxxL will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for both devices: NM24C02L and NM24C04L.

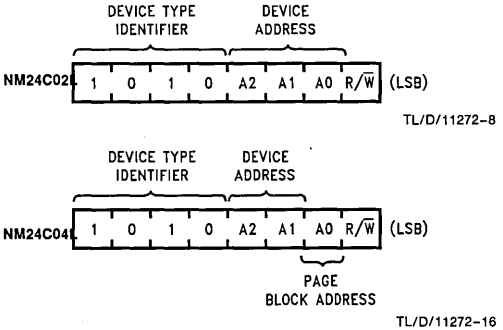

FIGURE 4. Slave Addresses

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02	A	A	A	1 (2K)	(NONE)
NM24C04	P	A	A	2 (4K)	0 1
NM24C08	P	P	A	4 (8K)	00 01 10 11
NM24C02	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

Device Addressing (Continued)

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C02L/C04L recognizes the start condition, the devices interfaced to the I^2C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24C02L/C04L responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24CxxL begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24CxxL inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24CxxL is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24CxxL will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

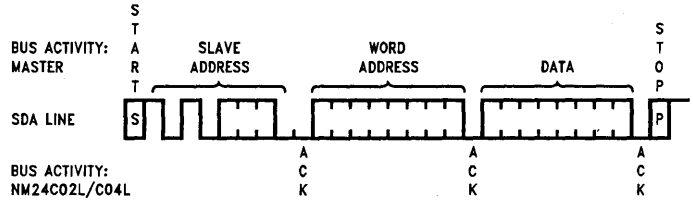

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FIGURE 5. Byte Write

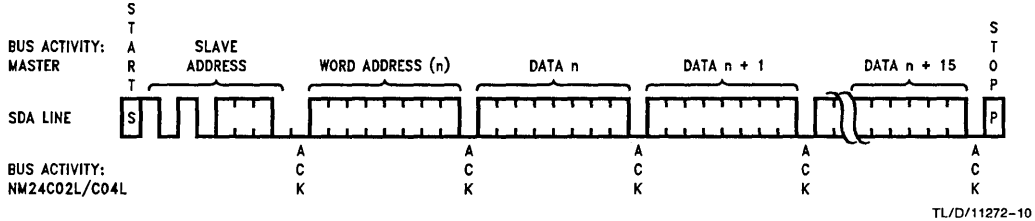

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FIGURE 6. Page Write

Write Operations (Continued)

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24CxxL initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24CxxL is still busy with the write operation, no ACK will be returned. If the NM24CxxL has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24CxxL contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24CxxL issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24CxxL discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24CxxL and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and the NM24CxxL discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24CxxL continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24CxxL continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

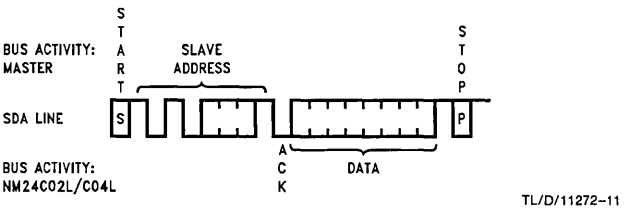

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FIGURE 7. Current Address Read

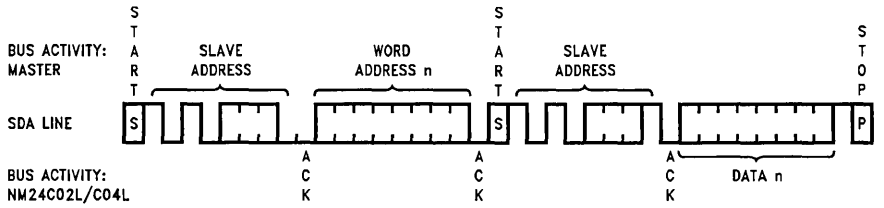

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FIGURE 8. Random Read

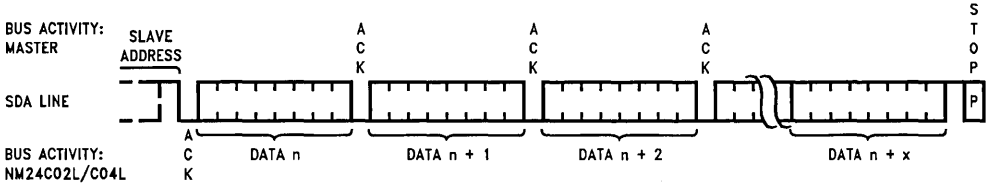

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FIGURE 9. Sequential Read

Write Operations (Continued)

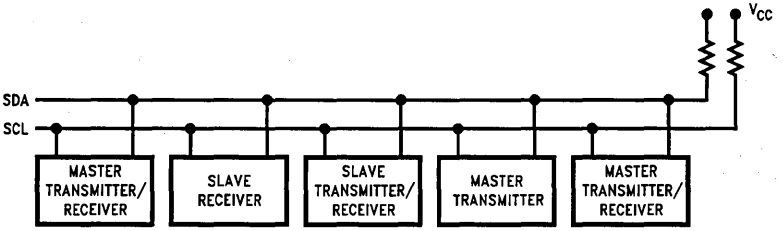

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FIGURE 10. Typical System Configuration

National Semiconductor

NM24C03L/C05L
2K-/4K-Bit Serial EEPROM with Write Protect and Extended Voltage (I^2C Synchronous 2-Wire Bus)

General Description

The NM24C03L/C05L devices are 2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I^2C 2-wire protocol, and are designed to minimize device pin count and simplify PC board layout requirements. National EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

The upper half of the memory can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

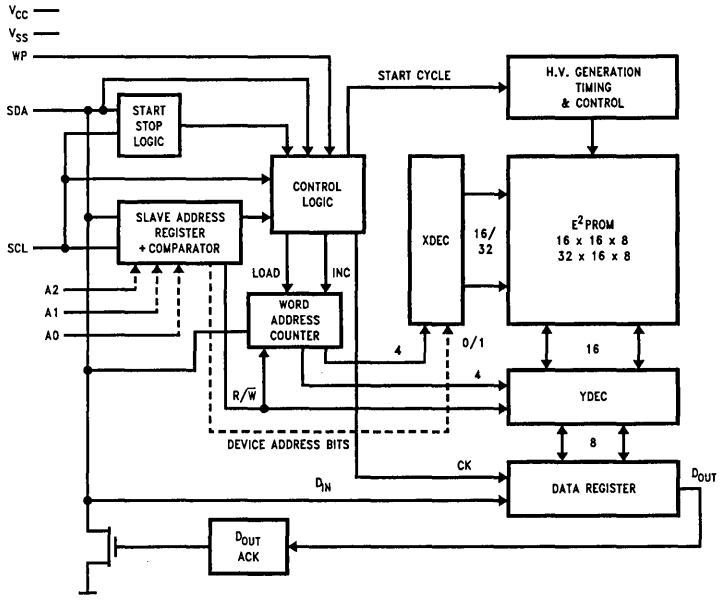
These devices have an operating voltage range of 2.5V to 5.5V and are offered in an 8-pin small outline (SO) package, making these devices perfectly suited for low power applications that require minimal board space usage.

This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

Features

- Hardwire write protect for upper block
- Low Power CMOS
  - 2 mA active current typical
  - 60 μA standby current typical
- 2-wire I^2C serial interface
  - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - Minimizes total write time per byte
- Self timed write cycle
  - Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin mini-DIP or 14-pin SO package

Functional Diagram



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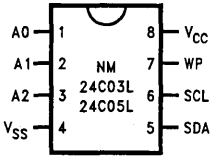
Connection Diagram

Dual-In-Line Package (N)



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Top View

See NS Package Number N08E (N) and M08A (M8)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
V_{CC}	+5V
WP	Write Protect

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C03LN/NM24C05LN NM24C03LM8/NM24C05LM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C03LEN/NM24C05LEN NM24C03LEM8/NM24C05LEM8

LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C03L/C05L	0°C to +70°C
NM24C03LE/C05LE	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.5V to 4.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 200 μA			0.4	V

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0V	6	pF

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

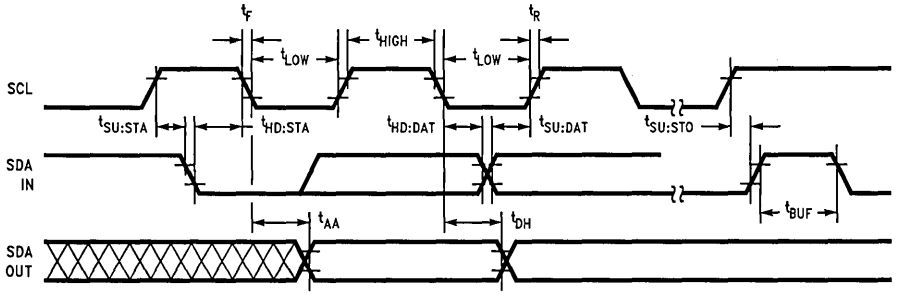
LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C03L/C05L	0°C to +70°C
NM24C03LE/C05LE	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	µA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Note 2: This parameter is periodically sampled and not 100% tested.

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

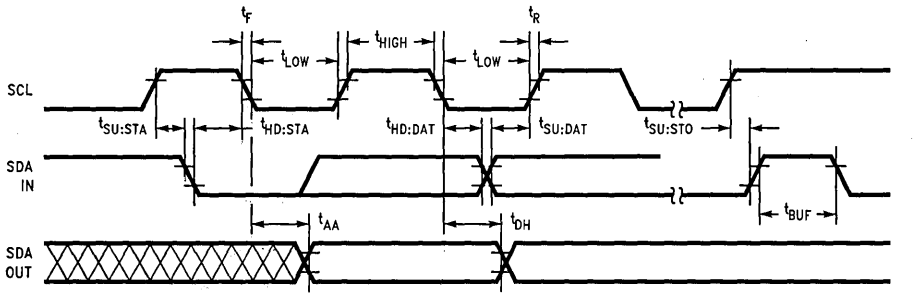
STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I^2C Bus)

As mentioned, the I^2C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In additon, since the I^2C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I^2C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

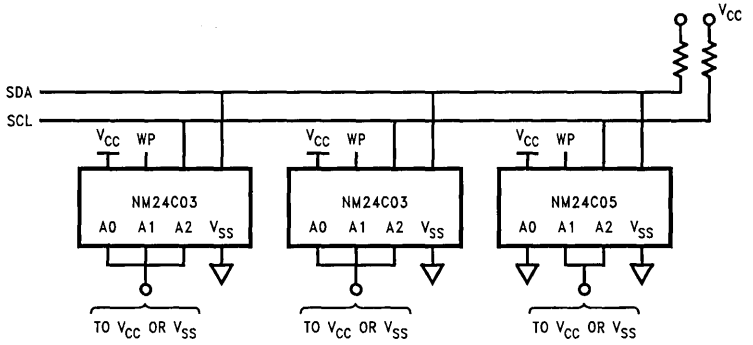
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string)

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I^2C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 8k (½ Maximum Size) of Memory on 2-Wire Bus



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Notes:

The SDA pull-up resistor is required due to the open-drain/open-collector output of I^2C bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.
It is recommended that the total line capacitance be less than 400 pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C03L	DA	DA	DA	2048 Bits	1
NM24C05L	V_{SS}	DA	DA	4096 Bits	2

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C03L	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C05L	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

WP WRITE PROTECTION

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible.

If tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C03L/C05L supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx is considered a slave in all applications.

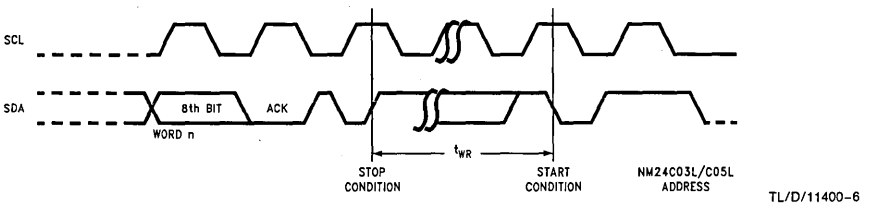
CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Write Cycle Timing



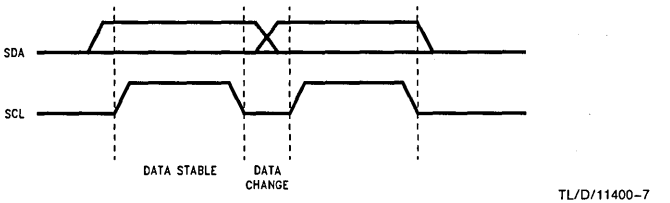


FIGURE 1. Data Validity

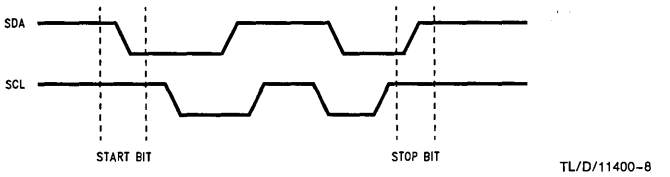


FIGURE 2. Definition of Start and Stop

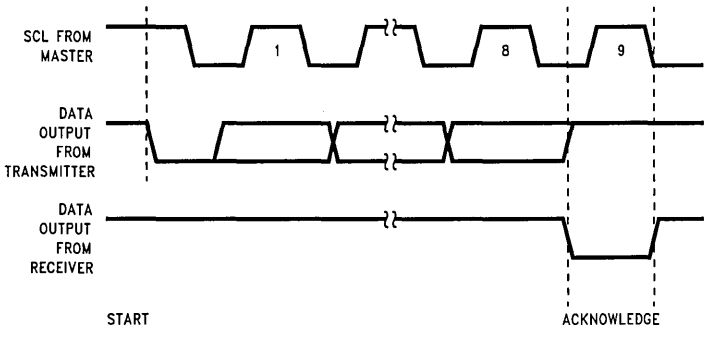


FIGURE 3. Acknowledge Response from Receiver

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for both devices: NM24C03L and NM24C05L.

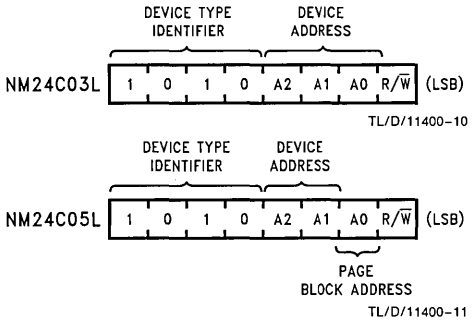


FIGURE 4. Slave Addresses

Device Addressing (Continued)

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C03L	A	A	A	1 (2K)	(None)
NM24C05L	P	A	A	2 (4K)	0 1

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C03L/C05L recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

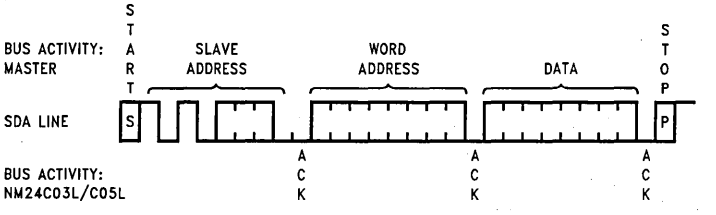


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FIGURE 5. Byte Write

Write Operations (Continued)

PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is still busy with the write operation, no ACK will be returned. If the NM24Cxx has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the NM24Cxx is connected to V_{CC} (+5V). The NM24Cxx will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24Cxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

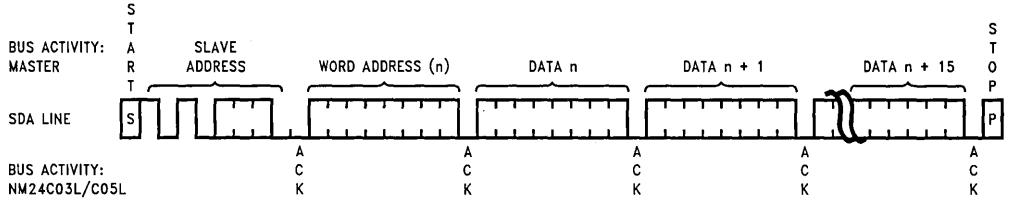

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FIGURE 6. Page Write

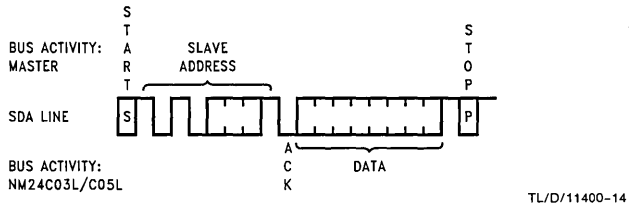

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FIGURE 7. Current Address Read

Read Operations (Continued)

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

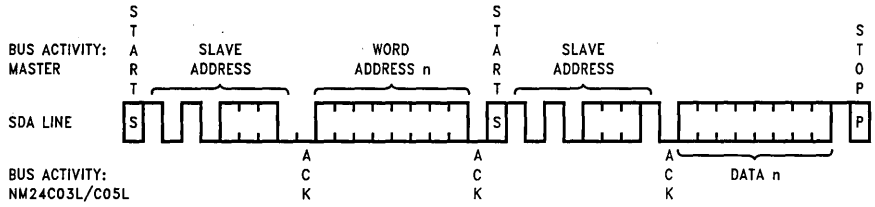

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FIGURE 8. Random Read

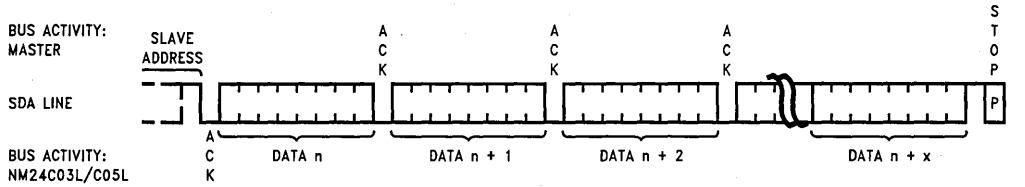

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FIGURE 9. Sequential Read

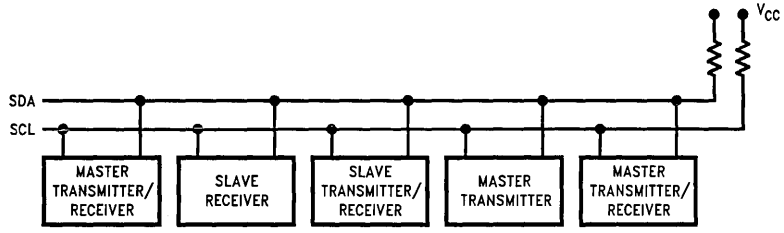

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FIGURE 10. Typical System Configuration

National Semiconductor

NM59C11 1024-Bit Serial EEPROM 64 x 16-Bit or 128 x 8-Bit Configurable with Programming Status

General Description

The NM59C11 is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or as 128 8-bit registers. The organization is determined by the status of the ORG input. This memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM59C11 is available in an SO package for small space considerations.

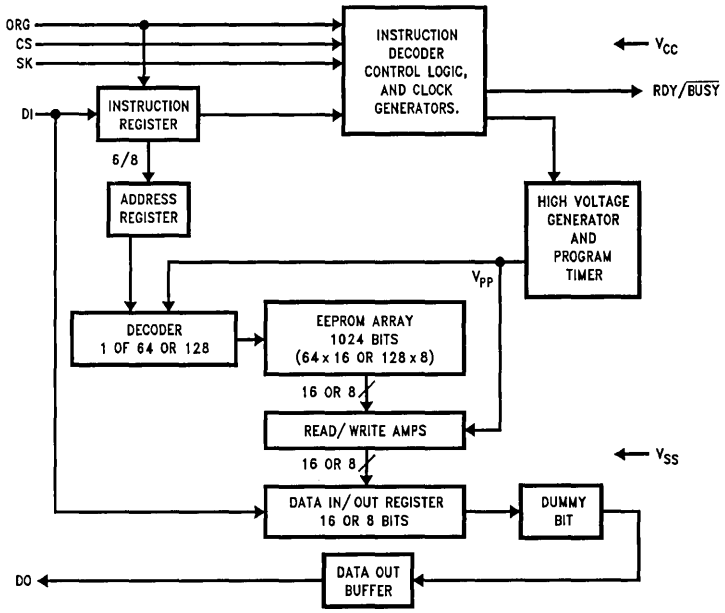
The interface that controls the EEPROM is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 6 instructions that operate the NM59C11: Read, Erase/Write Enable, Write, Erase/Write Disable, Write All, and Erase All. The device programming status is output on the RDY/$\overline{\text{BUSY}}$ output.

The NM59C11 has programming status in adddition to the functions found in the NM93C46A.

Features

- Device status during programming mode
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct Write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes (also available with 3.0V to 5.5V)
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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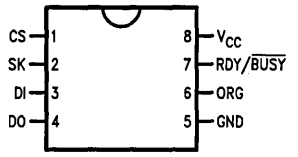
Connection Diagram

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization
RDY/$\overline{BUSY}$	Programming Status

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM59C11N
NM59C11M8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM59C11EN
NM59C11EM8

Military Temp. Range (−55°C to +125°C)

Order Number
NM59C11MN
NM59C11MM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM59C11	0°C to +70°C
NM59C11E	−40°C to +85°C
NM59C11M	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified)

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM59C11 NM59C11E MN59C11M	CS = V_{IH}, SK = 1 MHz SK = 1.0 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM59C11 NM59C11E MN59C11M	CS = V_{IH}, SK = 1 MHz SK = 1.0 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM59C11 NM59C11E NM59C11M	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NM59C11 NM59C11E NM59C11M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM59C11 NM59C11E NM59C11M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM59C11 NM59C11E NM59C11M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM59C11 NM59C11E NM59C11M		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM59C11 NM59C11E NM59C11M	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM59C11 NM59C11E NM59C11M	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM59C11 NM59C11E NM59C11M	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM59C11 NM59C11E NM59C11M	(Note 4) (Note 4) (Note 5)	250 250 500		ns
t_{CSS}	CS Setup Time	NM59C11 NM59C11E NM59C11M	Relative to SK	50 50 100		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DH}	DO Hold Time		Relative to SK	10		ns
t_{DIS}	DI Setup Time	NM59C11A NM59C11AE NM59C11AM	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		
t_{PD1}	Output Delay to "1"	NM59C11A NM59C11AE NM59C11AM	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM5911A NM59C11AE NM59C11AM	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM59C11A NM59C11AE NM59C11AM	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specfication is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in a SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SLK} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the mimimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM59C11 has 6 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8/9 bits carry the op code and the 6/7-bit address for register selection.

Read (READ)

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into an 8- or 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 8- or 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

RDY/BUSY

The NM59C11 has a separate output that indicates if the device is in the programming mode. It enters the programming mode when the last data bit is clocked in. When it enters the programming mode, the NM59C11 drives the RDY/BUSY output low. After it completes the programming mode, it drives the RDY/BUSY output high. The RDY/BUSY output remains at a high level at all times except while the device is in the programming mode.

Program (PROGRAM)

The program instruction is used to write data into an 8- or 16-bit register at the specified address. When the last data bit is clocked in, the NM59C11 automatically enters the programming mode. While the device is in the programming mode it cannot accept any other instructions and the RDY/BUSY output is driven low to indicate BUSY. When the device has completed the internally timed programming cycle, the RDY/BUSY output is driven high to indicate it is ready to accept the next instruction.

The Chip Select (CS) input does not need to be driven low to initiate the programming cycle, but it must be driven low for the minimum CS low timer (t_{CS} = 250 μs) before a new cycle can be initiated.

Erase All (ERAL)

The ERAL instruction will erase all memory registers simultaneously (all bits set to a logical "1"). To initiate the internal programming mode, an 8- or 16-bit data field must be clocked in, although the contents of the data field are "don't care" in this instruction. The internally timed programming cycle will be initiated when the last data bit is clocked in. As with the Program mode, the RDY/BUSY line will indicate when the device is able to accept the next instruction.

The Chip Select (CS) input does not need to be driven low to initiate the internal programming cycle, but it must be driven low for the minimum chip select low time (t_{CS} = 250 ns) before a new cycle can be initiated.

Write All (WRAL)

The WRAL instruction will write the same data into all memory registers simultaneously. The address field is "don't care" in this instruction, although must be clocked in. The internal programming cycle is initiated when the last data bit is clocked in. As with the Program mode, the RDY/BUSY output indicates when the device is ready to accept the next instruction.

The Chip Select (CS) input does not need to be driven low to initiate the internal programming cycle, but it must be driven low for the minimum chip select low time (t_{CS} = 250 ns) before a new cycle can be initiated.

Erase/Write Disable (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

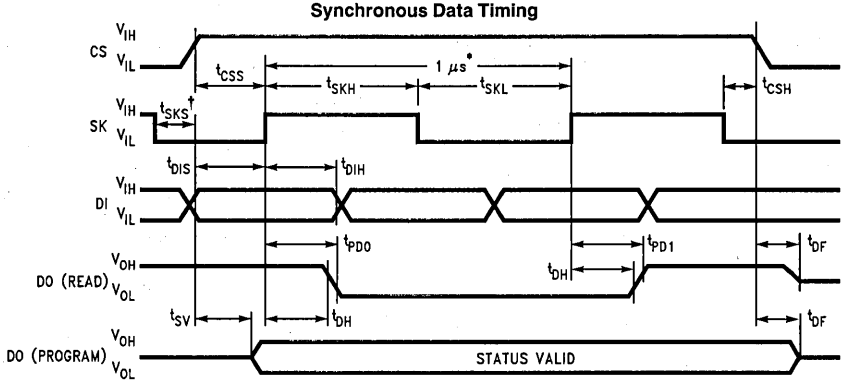
Instruction Set

Instruction	Start Bit	Opcode	Address*		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A6–A0	A5–A0			Read Address AN–A0
PROGRAM	1	0100	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0011	XXXXXXX	XXXXXX			Program Enable
EWDS	1	0000	XXXXXXX	XXXXXX			Program Disable
ERAL	1	0010	XXXXXXX	XXXXXX			Erase All Addresses
WRAL	1	0001	XXXXXXX	XXXXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" address bits.

Timing Diagrams

Synchronous Data Timing



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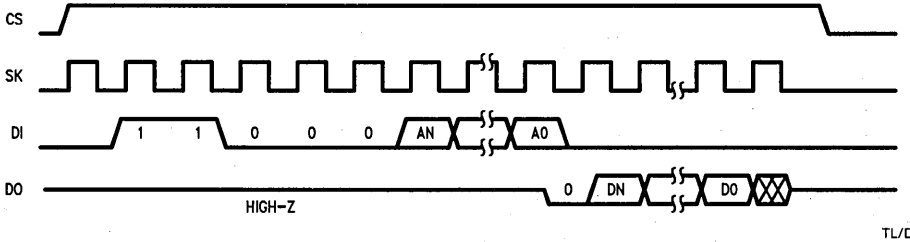
*This is the minimum SK period (Note 2).

†t_{SKS} is not needed if D1 = V_{IL} when CS is going active (HIGH).

READ



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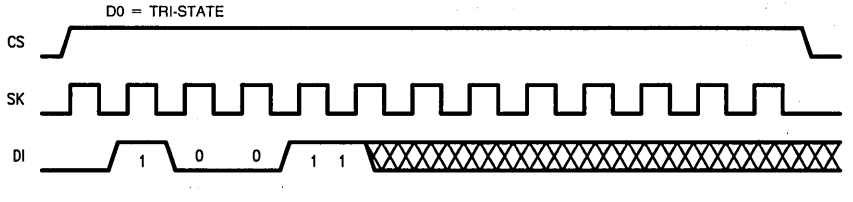
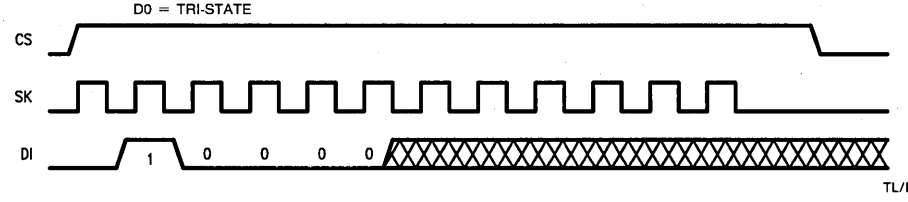
EWEN



TL/D/11051–5

EWDS†

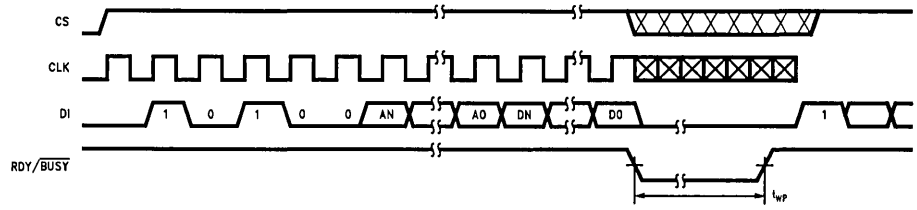


TL/D/11051–6

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a number of clock cycles after the last bit of opcode is clocked in. In the 64 x 16 configuration, 6 additional clock cycles are required. In the 128 x 8 configuration, 7 additional clock cycles are required.

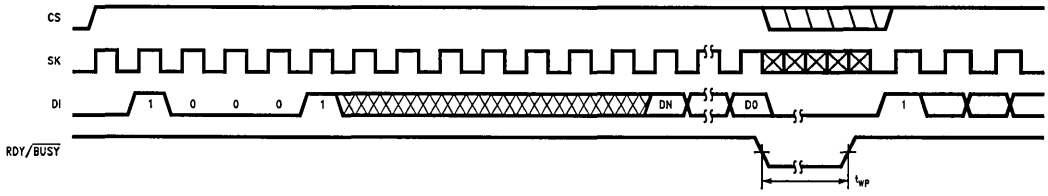
Timing Diagrams (Continued)

WRITE



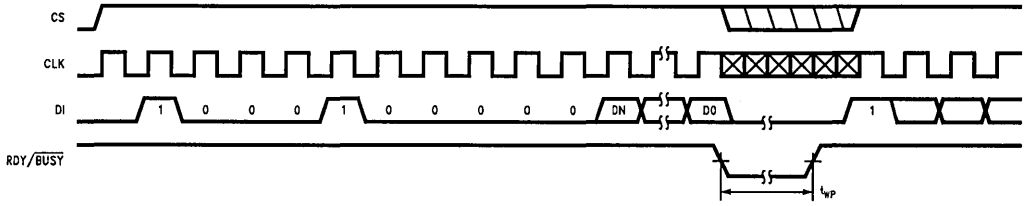
TL/D/11051–7

WRAL (128 x 8 Organization)



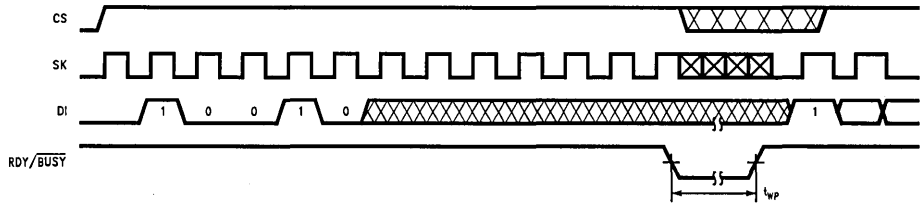
TL/D/11051–8

WRAL (64 x 16 Organization)



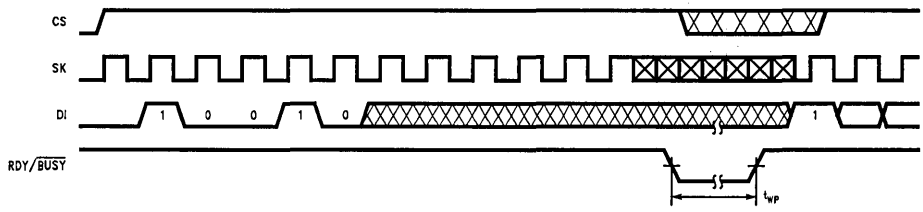
TL/D/11051–9

ERAL† (128 x 8 Organization)



TL/D/11051–11

ERAL† (64 x 16 Organization)



TL/D/11051–12

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a number of clock cycles after the last bit of opcode is clocked in. In the 64 x 16 configuration, 6 additional clock cycles are required. In the 128 x 8 configuration, 7 additional clock cycles are required.

National Semiconductor

NM93C06/C46/C56/C66
256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™)

General Description

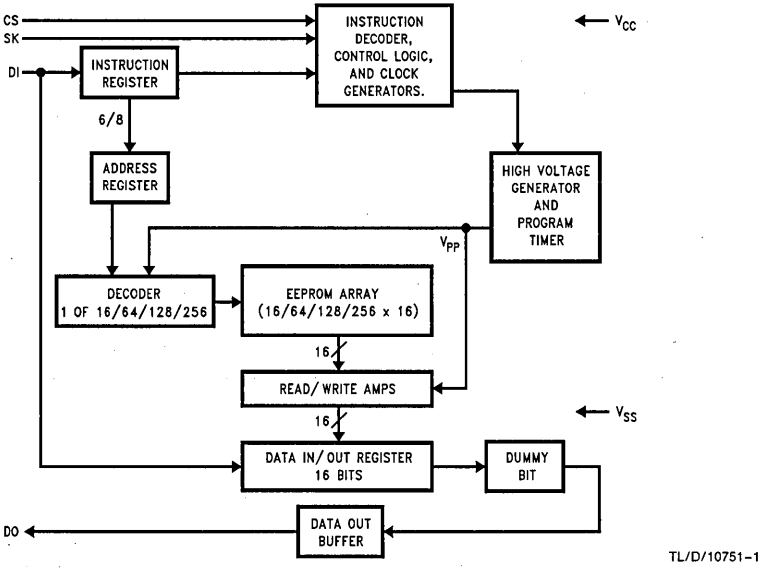
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 400 μA; Typical standby current of 25 μA
- Direct Write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

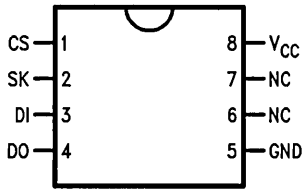
Block Diagram



TL/D/10751–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/10751-2

Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93C06N/NM93C46N
NM93C56N/NM93C66N
NM93C06M8/NM93C46M8
NM93C56M8/NM93C66M8

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93C06MN/NM93C46MN
NM93C56MN/NM93C66MN
NM93C06MM8/NM93C46MM8
NM93C56MM8/NM93C66MM8

Extended Temp. Range (−40°C to +85°C)

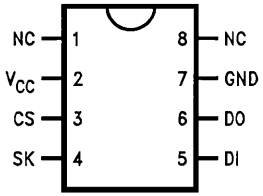
Order Number*
NM93C06EN/NM93C46EN
NM93C56EN/NM93C66EN
NM93C06EM8/NM93C46EM8
NM93C56EM8/NM93C66EM8

Alternate (Turned) SO Pinout

Order Number
NM93C46TM8 Commercial Temp.
NM93C46TEM8 Extended Temp.

*For 14-Pin SO availability contact your local National Semiconductor Sales Office.

Alternate SO Pinout (TM8)



TL/D/10751-12

See NS Package M08A

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06–NM93C66	0°C to +70°C
NM93C06E–NM93C66E	−40°C to +85°C
NM93C06M–NM93C66M	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified)

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	CS = 0V		50 50 100	μA
I_{IL}	Input Leakage	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	NM93C06E-NM93C66E NM93C06M-NM93C66M	I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M		0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	(Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	(Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	(Note 4) (Note 5)	250 250 500		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	Relative to SK	50 50 100		ns
t_{DH}	D0 Hold Time		Relative to SK	10*		ns
t_{DIS}	DI Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

*t_{DH} = 70 ns for the NM93C06 and NM93C46

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The ERASE ALL instruction is not required, see note below.

Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Erase/Write Disable (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

NOTE: The NM93C06/C46/C56/C66 devices do not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

Instruction Set for the NM93C06 and NM93C46

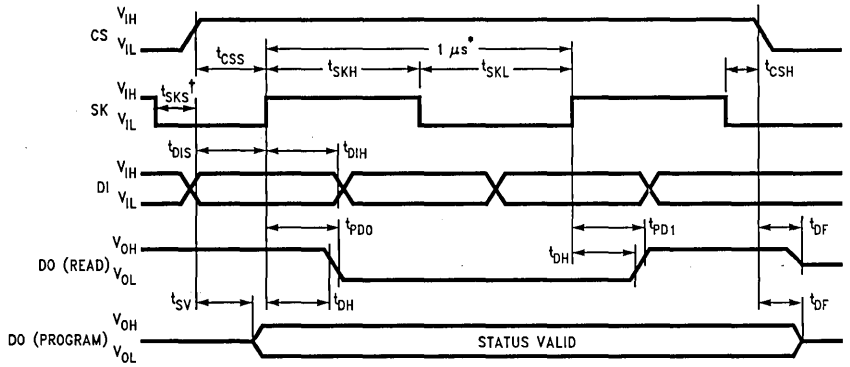
Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Instruction Set for the NM93C56 and NM93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
ERAL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7–A0	D15–D0	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

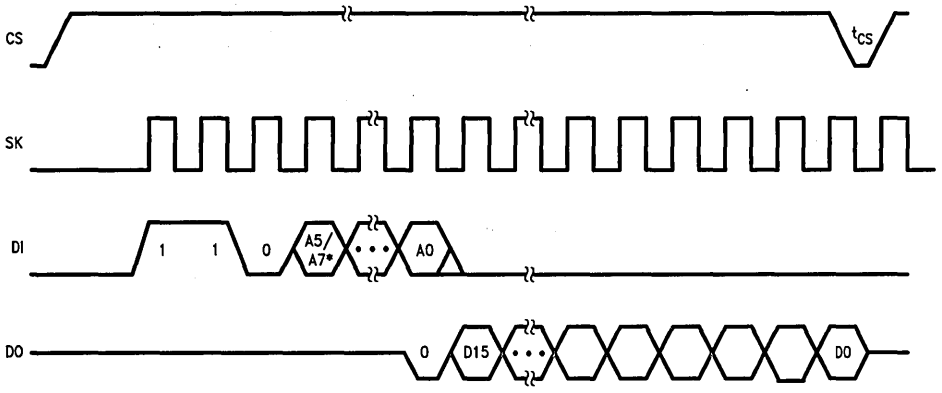
Synchronous Data Timing



*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

TL/D/10751–4

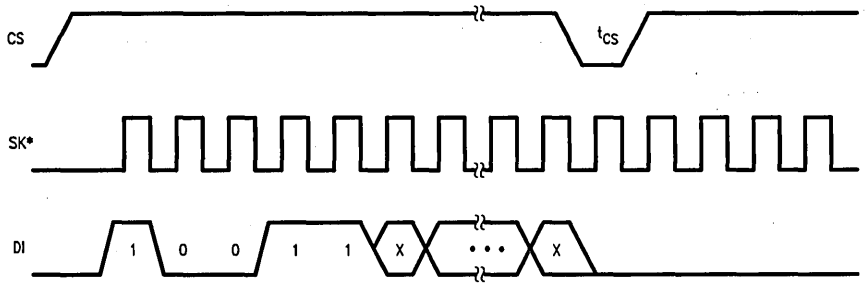
READ:



*Address bits A_5 and A_4 become "don't care" for NM93C06.
*Address bit A_7 becomes a "don't care" for NM93C56.

TL/D/10751–5

EWEN:

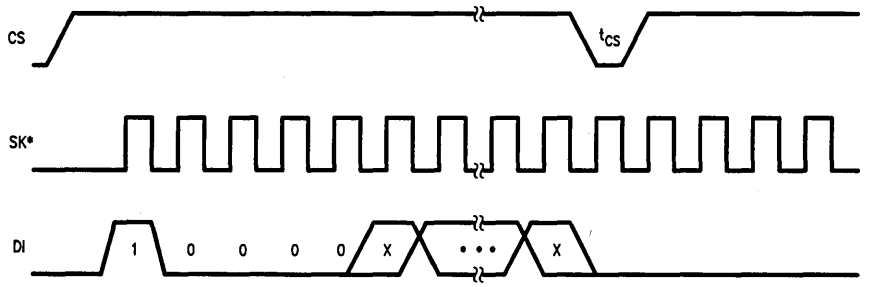


*The NM93C56 and NM93C66 require a minimum of 11 clock cycles. The NM93C06 and NM93C46 require a minimum of 9 clock cycles.

TL/D/10751–6

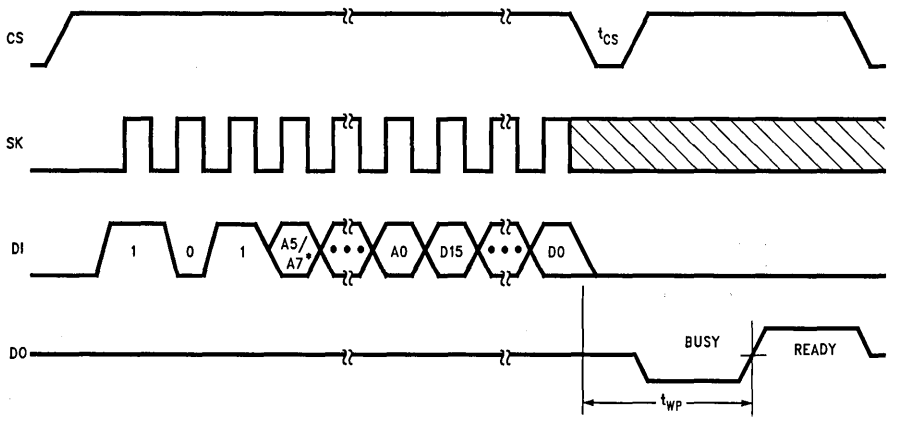
Timing Diagrams (Continued)

EWDS:



*The NM93C56 and NM93C66 require a minimum of 11 clock cycles. The NM93C06 and NM93C46 require a minimum of 9 clock cycles. TL/D/10751–7

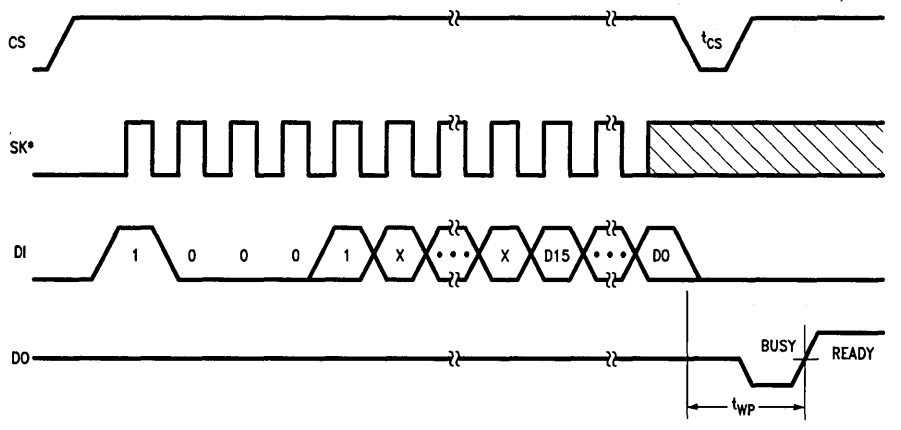
WRITE:



*Address bit A_5 and A_4 become "don't care" for NM93C06. TL/D/10751–8

*Address bit A_7 becomes a "don't care" for NM93C56.

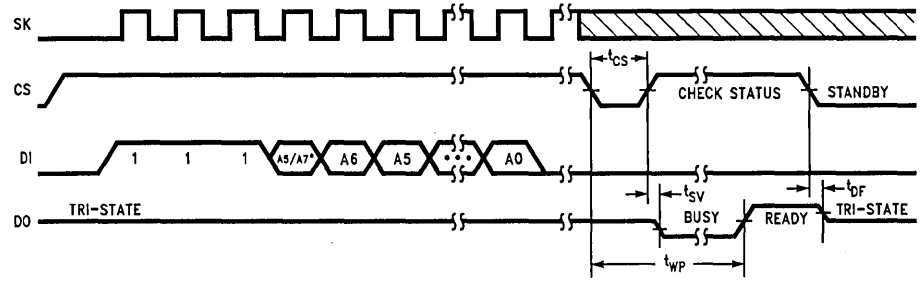
WRAL:†



*The NM93C56 and NM93C66 require a minimum of 11 clock cycles. The NM93C06 and NM93C46 require a minimum of 9 clock cycles. TL/D/10751–9

Timing Diagrams (Continued)

ERASE:

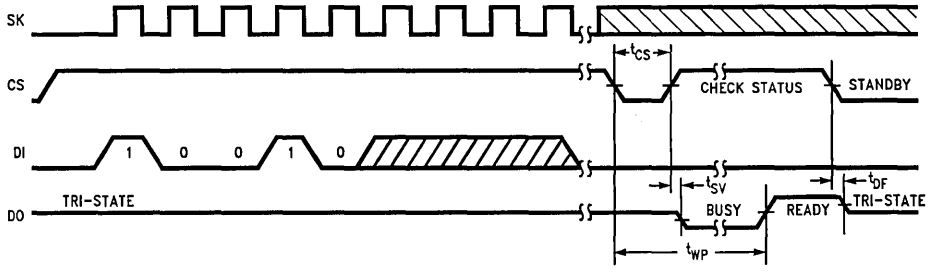


TL/D/10751–10

*Address bits A5 and A4 are "don't care" for NM93C06.

*Address bits A7 is "don't care" for NM93C56.

ERAL:



TL/D/10751–11

National Semiconductor

NM93CS06/CS46/CS56/CS66 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

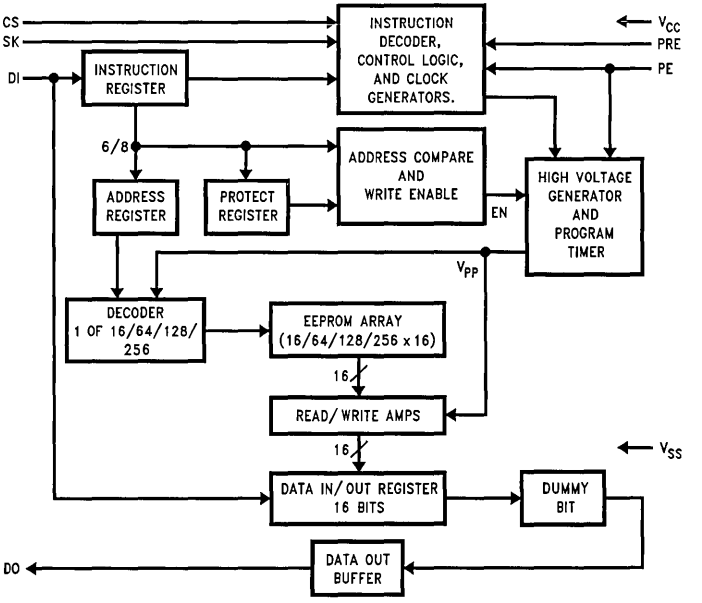
The NM93CS06/CS46/CS56/CS66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 registers of 16 bits each. N registers ($N \leq 16$, $N \leq 64$, $N \leq 128$, $N \leq 256$) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CSXX Family is offered in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE™ compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PREN, PRCLEAR, and PRDS.

Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 400 μA and standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram

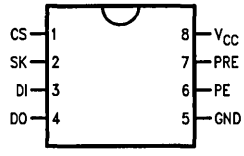


TL/D/10750–1

Connection Diagrams

PIN OUT:

Dual-In-Line Package (N) and 8-Pin SO (M8)*



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Top View

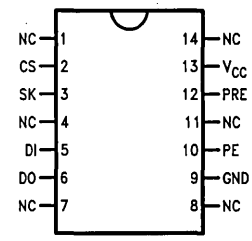
See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



TL/D/10750–3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93CS06N/NM93CS46N/NM93CS56N/NM93CS66N
NM93CS06M8/NM93CS46M8/NM93CS56M8/NM93CS66M*

Extended Temp. Range (−40°C to +85°C)

Order Number*
NM93CS06EN/NM93CS46EN/NM93CS56EN/NM93CS66EN
NM93CS06EM8/NM93CS46EM8/NM93CS56EM8/NM93CS66EM*

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93CS06MN/NM93CS46MN/NM93CS56MN/NM93CS66MN
NM93CS06MM8/NM93CS46MM8/NM93CS56MM8

*The NM93CS66 is available in 8-Pin DIP and 14-Pin SO only.

Note: For 14-pin SO availability on the 93CS06, CS46 and CS56, contact your local National Semiconductor Sales Office.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxx	0°C to +70°C
NM93CSxxE	−40°C to +85°C
NM93CSxxM	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	CS = 0V		50 50 100	μA
I_{IL}	Input Leakage	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93CS06E-NM93CS66E NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage	NM93CS06M-NM93CS66M	I_{OH} = −400 μA	2.4		V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	(Note 4) (Note 4) (Note 5)	250 250 500		ns
t_{CSS}	CS Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	Relative to SK	50 50 100		ns
t_{PRES}	PRE Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	Relative to SK	50 50 100		ns

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DH}	DO Hold Time		Relative to SK	10		ns
t_{PES}	PE Setup Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	Relative to SK	50 50 100		ns
t_{DIS}	DI Setup Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	Relative to CS Relative to CS Relative to CS	250 250 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended parts specifies a minimum SK clock period of 1 microsecond; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 microseconds; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial and Extended parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93CSxx EEPROM Family has 10 instructions as described below. Note that there is a difference in the length of the instruction for the NM93CS06 and NM93CS46 vs. the NM93CS56 and NM93CS66. This is due to the fact that the two larger devices require 2 additional address bits which are not required for the smaller devices. Within the two groups of devices the number of address bits remain constant even though in some cases the most significant bit(s) are not used. In every instruction, the first bit is always a "1" and is viewed as a start bit. The next 8 or 10 bits (depending on device size) carry the op code and address. The address is either 6 or 8 bits depending on the device size.

Read and Sequential Register Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **sequential register read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address sto in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction. The contents of the Protect Register will be read as 0's after a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06 and NM93CS46

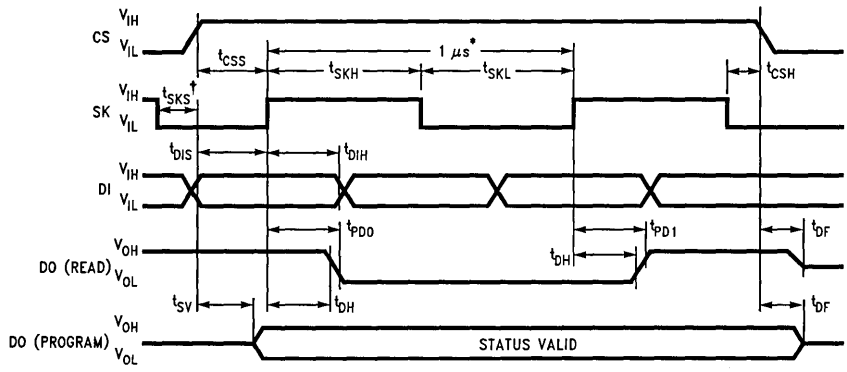
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE. Protect Register equals 0's.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Instruction Set for the NM93CS56 and NM93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE. Protect Register equals 0's.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

Synchronous Data Timing



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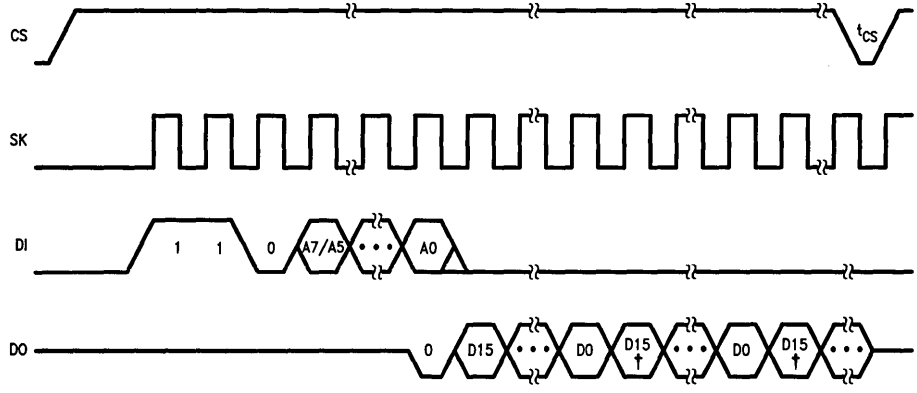
*This is the minimum SK period (Note 2).

†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:
PRE = 0, PE = X



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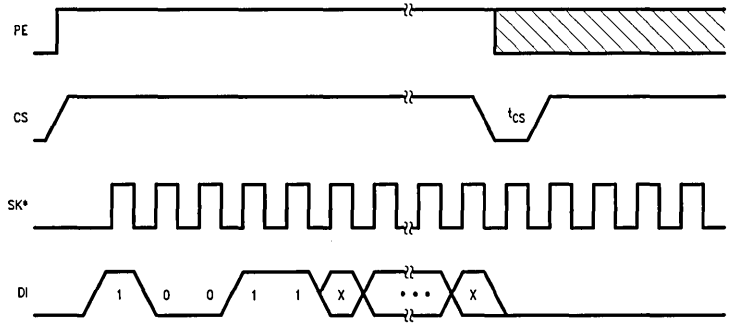
*Address bit A7 becomes "don't care" for NM93CS56.
*Address bits A5 and A4 become "don't cares" for NM93CS06.

†The memory automatically cycles to the next register.

Timing Diagrams (Continued)

WEN:
PRE = 0, DO = TRI-STATE



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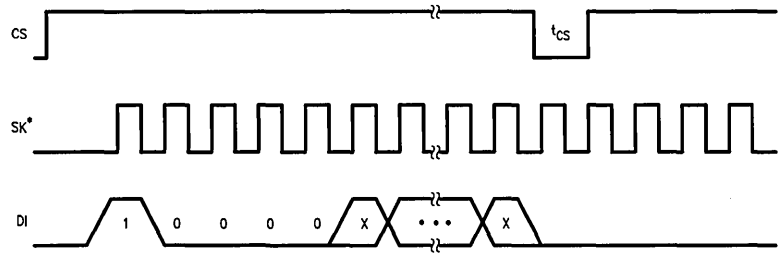
*The NM93CS56 and NM93CS66 require a minimum of 11 clocks cycles. The NM93CS06 and NM93CS46 require a minimum of 9 clock cycles.

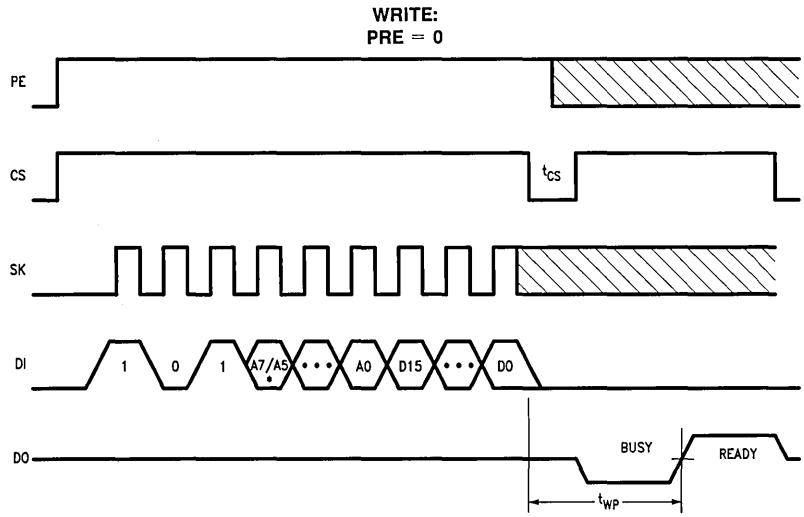
WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/10750–6

*The NM93CS56 and NM93CS66 require a minimum of 11 clocks cycles. The NM93CS06 and NM93CS46 require a minimum of 9 clock cycles.

WRITE:
PRE = 0



*Address bit A7 becomes a "don't care" for NM93CS56.
*Address bits A5 and A4 become "don't cares" for NM93CS06.

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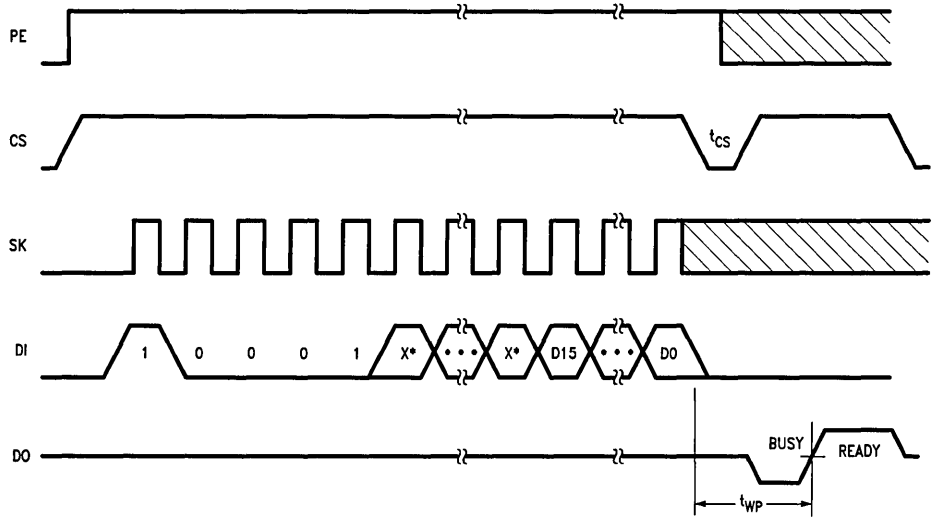
Timing Diagrams (Continued)

WRALL†:
PRE = 0



*Don't care

†Protect Register **MUST** be cleared.

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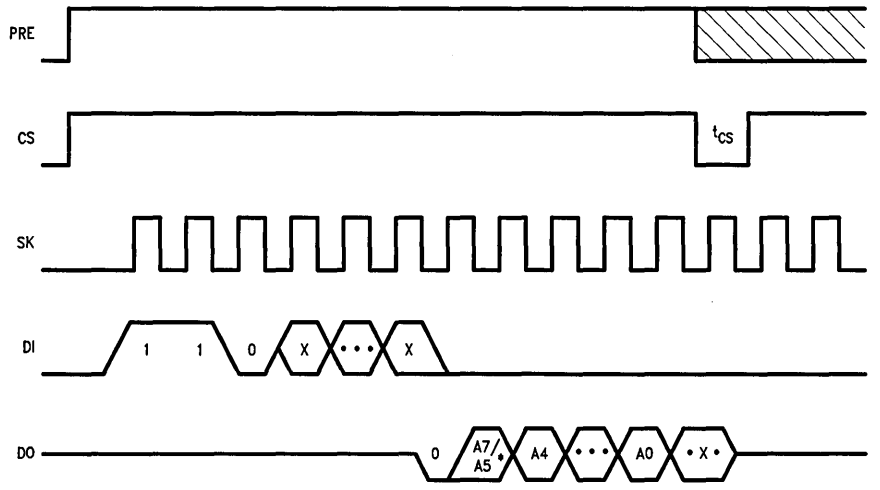
PRREAD:
PE = X



*Address bits A5 and A4 become "don't cares" for NM93CS06.

*Address bit A7 becomes "don't care" for NM93CS56.

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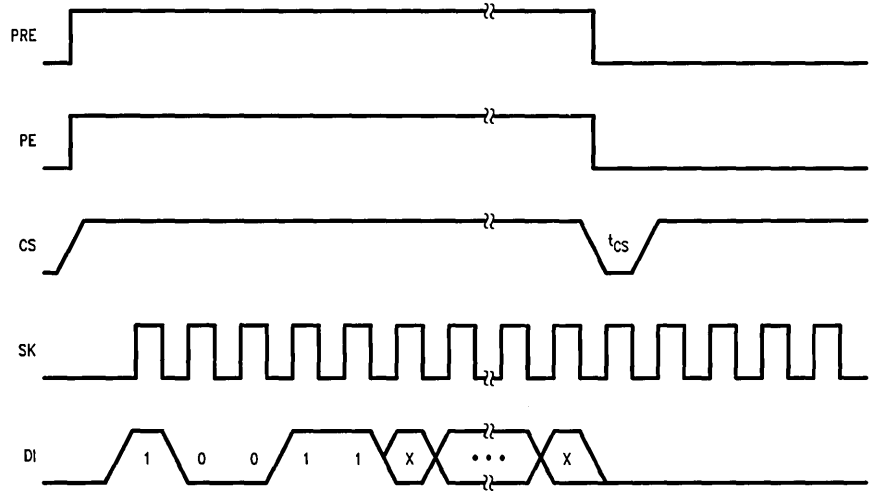
Timing Diagrams (Continued)

PREN*:
DO = TRI-STATE



*A WEN cycle must precede a PREN cycle.

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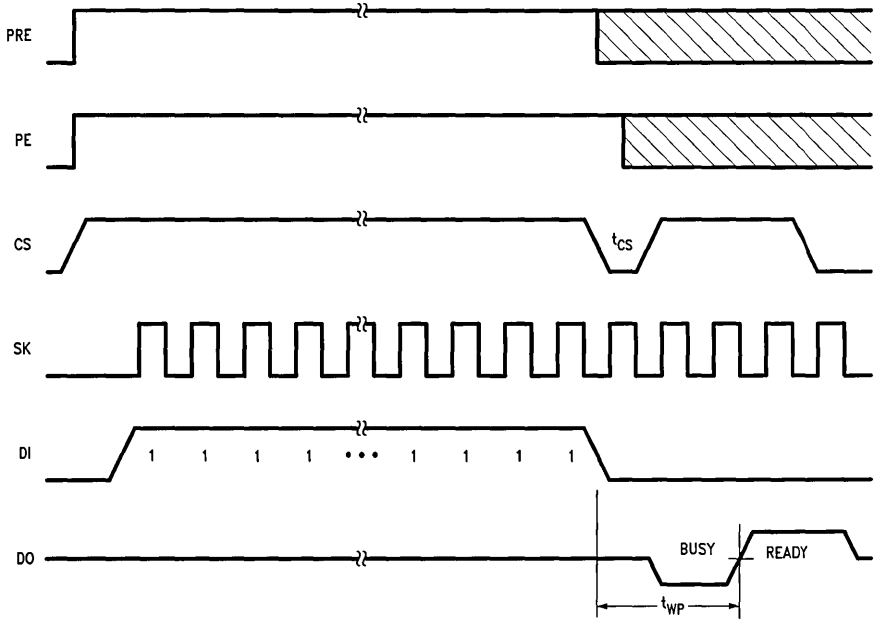
PRCLEAR*:

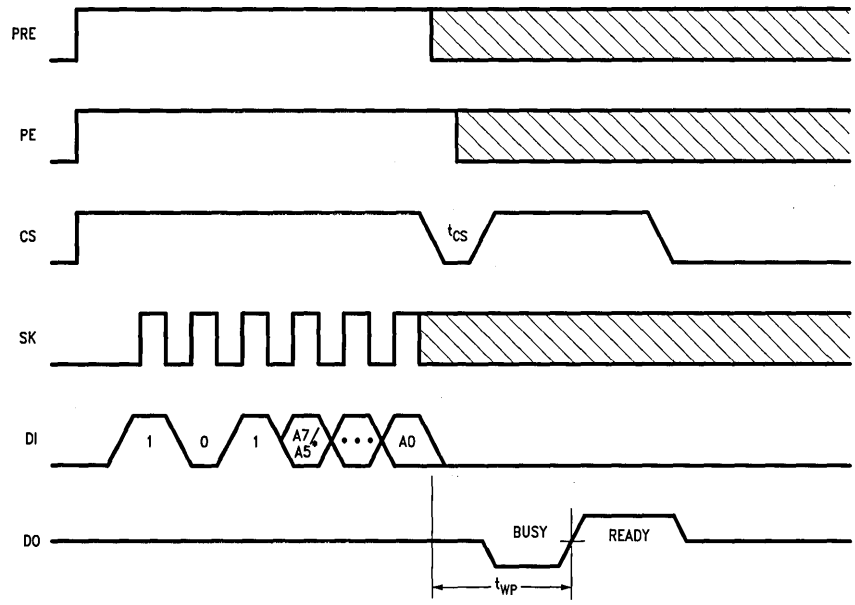


*A PREN cycle must **immediately** precede a PRCLEAR cycle.

TL/D/10750–11

Timing Diagrams (Continued)

PRWRITE†:



*Address bit A7 becomes a "don't care" for NM93CS56.
*Address bits A5 and A4 become "don't cares" for NM93CS06.

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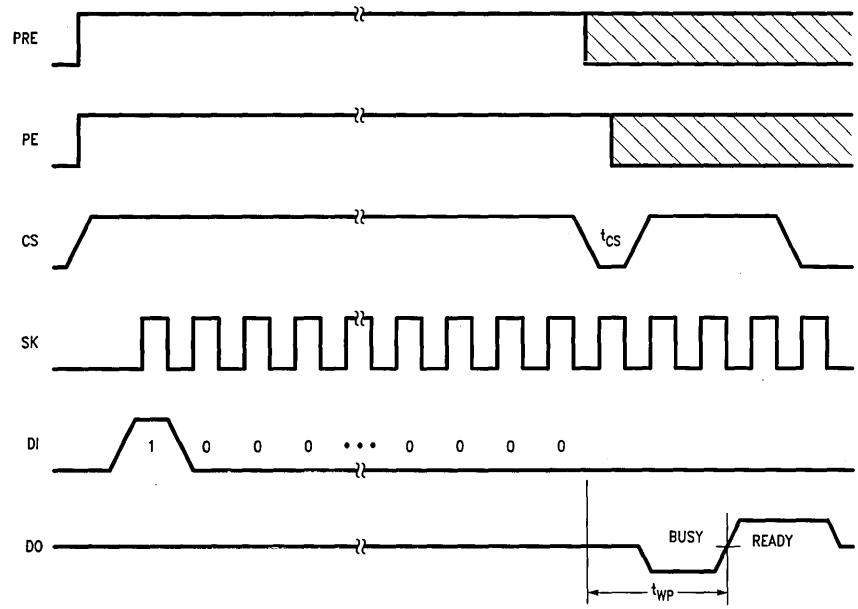
†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:



***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

TL/D/10750–13

National Semiconductor

NM93C06L/C46L/C56L/C66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V t0 5.5V)

General Description

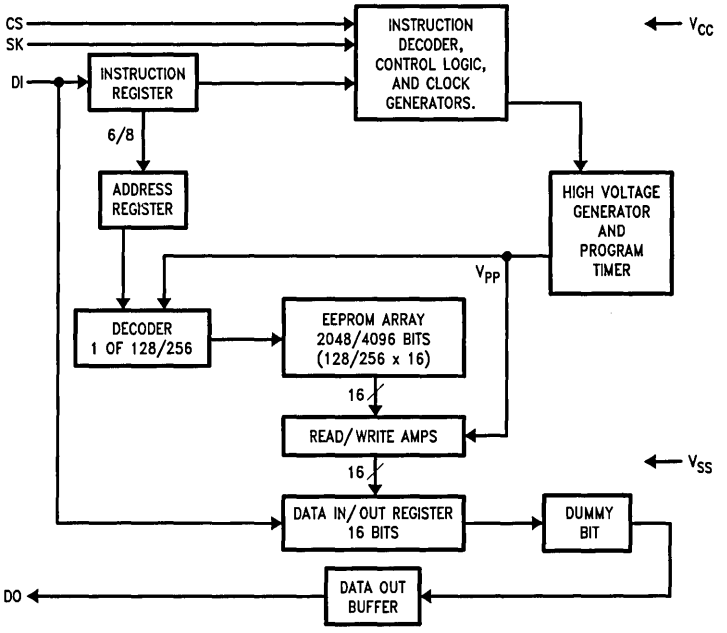
The NM93C06L/C46L/C56L/C66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CxxL Family functions in an extended voltage operating range, requires only a single power supply and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. These devices are available in an SO package for small space considerations.

The NM93CxxL Family interfaces to microprocessors and microcontrollers via a single 4-wire MICROWIRE™ bus which possesses the following parameters: SK (Serial Clock), CS (Chip Select), DI (Data Input) and DO (Data-Output). DI includes: instruction, address and data to be written. DO offers data read and programming status information. Serial interfacing allows 8-pin DIP or 8-pin SO packaging to minimize board space. The following seven instructions (op codes) control device operation: EWEN (Erase/Write Enable), EWDS (Erase/Write Disable), READ (Read), ERAL (Erase all registers), ERASE (Erase a register/address), WRAL (Write all registers with 16 bits of data) and WRITE (Write a register/address).

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; Typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

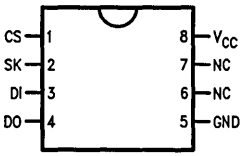
Block Diagram



TL/D/10045–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/10045-2

Top View

See NS Package Number N08E or M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C06LN/NM93C46LN
NM93C56LN/NM93C66LN
NM93C06LM8/NM93C46LM8
NM93C56LM8/NM93C66LM8

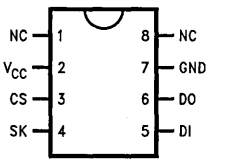
Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C06LEN/NM93C46LEN
NM93C56LEN/NM93C66LEN
NM93C06LEM8/NM93C46LEM8
NM93C56LEM8/NM93C66LEM8

Alternate (Turned) SO Pinout

Order Number
NM93C46TLM8/NM93C46TLEM8

Alternate SO Pinout (TM8)



TL/D/10045-12

See NS Package Number M08A

LOW VOLTAGE (<4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 250 kHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		2V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2)	1 1		μs
t_{SKS}	SK Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 3)	1 1		μs
t_{CSS}	CS Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	0.2 0.2		μs
t_{DH}	DO Hold Time		Relative to SK	10		ns

LOW VOLTAGE (<4.5V) SPECIFICATIONS

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms

Capacitance (Note 4)

T_A = 25°C f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF		
V_{CC} Range	**AC Test Conditions**	
4.5V < V_{CC} < 5.5V	Input Pulse Levels	0.8V and 2.0V
	Timing Measurement Level (V_{IL}/V_{IH})	0.9V and 1.9V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 2.0V
	(TTL Load Conditions: I_{OL} = 2.1 mA, I_{OH} = −0.4 mA)	
2.0V < V_{CC} < 4.5V	Input Pulse Levels	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH})	0.4V and 1.6V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 1.6V
	(CMOS Load Conditions: I_{OL} = 10 μA, I_{OH} = −10 μA)	

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The above SK frequency specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		3 3	mA
I_{CC3}	Standby Current	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage	NM93C06LE-NM93C66LE	I_{OL} = 10 μA		0.2	V
f_{SK}	SK Clock Frequency	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		0 0	1 1	MHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2) (Note 3)	250 300		ns
t_{SKL}	SK Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2) (Note 3)	250 250		ns
t_{CS}	Minimum CS Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 4) (Note 5)	250 250		ns
t_{CSS}	CS Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	50 50		ns
t_{DH}	DO Hold Time		Relative to SK	10		ns

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{PD0}	Output Delay to "0"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{SV}	CS to Status Valid	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{DF}	CS to DO in TRI-STATE	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test CS = V_{IL}		100 100	ns
t_{WP}	Write Cycle Time				10	ms

Note: Throughout this table "M" refers to temperature range (−55°C to +125°C), not package.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93CxxL Family has seven instruction sets as described below. Note that each instruction set is broken down into the Start Bit (SB), Op code, Address (if applicable) and Data (if applicable). As shown in the timing diagrams and INSTRUCTION SET tables, address bits will have 6 bits for the NM93C06 and NM93C46 and 8 bits for the NM93C56 and NM93C66 devices. All instruction bits are entered into the device on the SK low-to-high transitions.

Programming is enabled by bringing CS to a Logical 0 state for the required t_{CS} period. After this t_{CS} period the self-timed operation may be monitored by bringing CS to a logical 1 and observing the DO status: Logical 1 = READY (Ready for the next instruction) and Logical 0 = BUSY (Programming in progress).

Erase/Write Enable (EWEN):

When V_{CC} is applied to the device, it powers up in the programming Erase/Write disabled state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once this instruction is executed, programming remains enabled until the Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data disturbance, the Erase/Write Disable instruction disables all programming modes and should follow the end of all programming cycles.

Read (READ):

The READ instruction outputs the specified address data on the DO pin. After the READ instruction is received, the instruction and address are decoded and data is transferred from the address to a 16-bit shift register output buffer. A dummy bit (logical 0) precedes all 16-bit data out strings. The READ instruction may be executed from either the enabled or disabled state.

Erase (ERASE):

This instruction, when followed by an address location, programs all bits in the selected register/address to a 1 state (Register erase).

Erase All (ERAL):

This instruction programs all registers/addresses in the memory array to a 1 state, (Bulk erase).

Write (WRITE):

This instruction, when followed by an address location and 16 bits of data, programs the selected register/address.

Write All (WRAL):

This instruction, when followed by 16 bits of data, programs all registers/addresses in the memory array with the specified data pattern, (Bulk write).

Instruction Set for the NM93C06L and NM93C46L

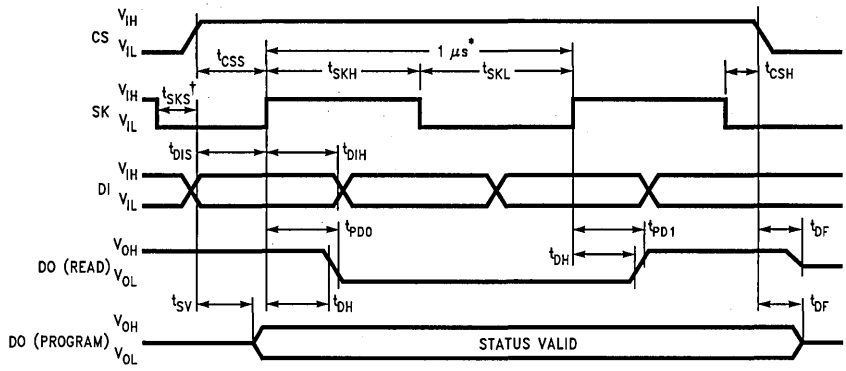
Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Instruction Set for the NM93C56L and NM93C66L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
WRITE	1	01	A7–A0	D15–D0	Writes register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing

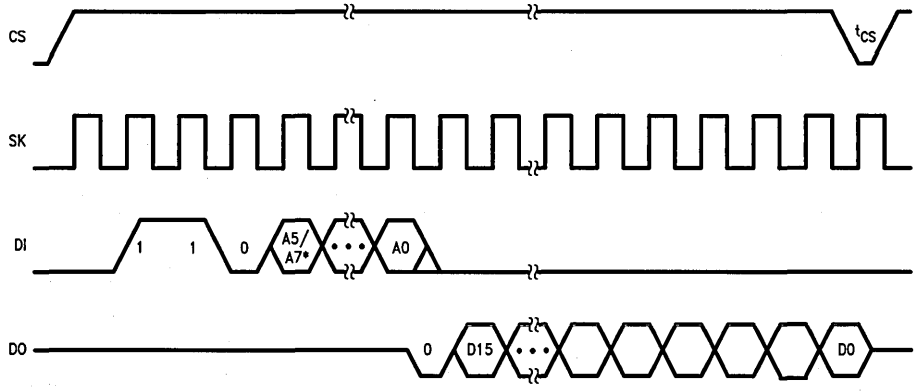


TL/D/10045–13

*This is the minimum SK period (Note 2).

†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:

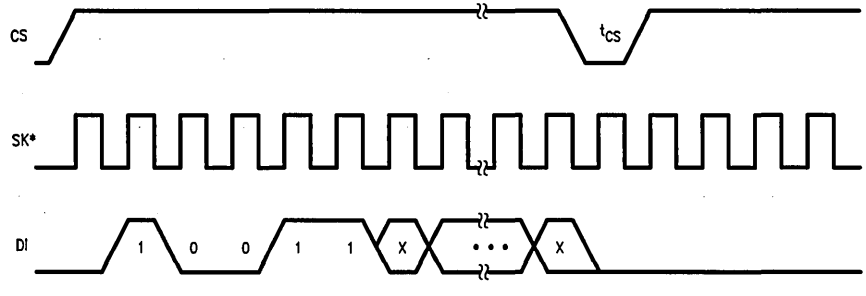


TL/D/10045–5

*Address bits A_5 and A_4 become "don't care" for NM93C06L.

*Address bit A_7 becomes a "don't care" for NM93C56L.

EWEN:

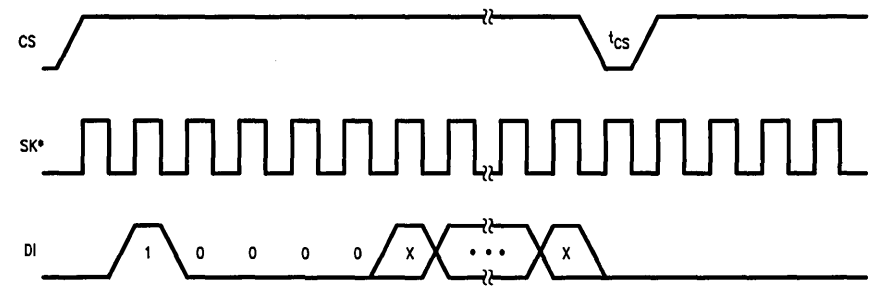


TL/D/10045–6

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

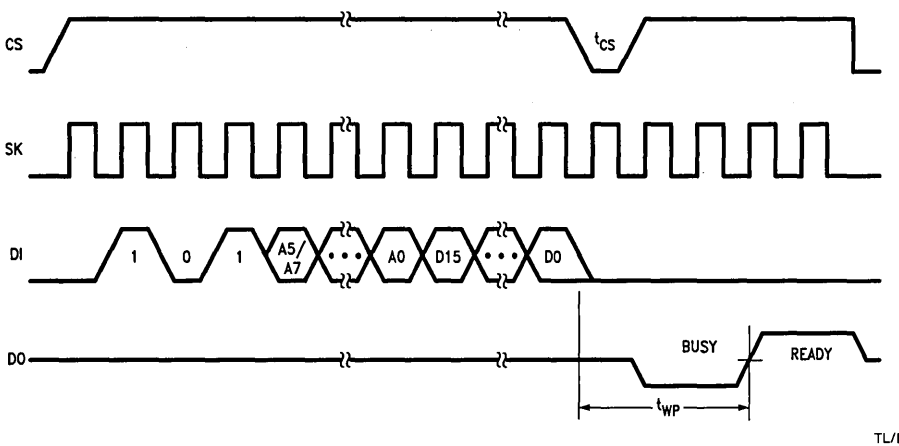
EWDS:



TL/D/10045–7

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

WRITE:

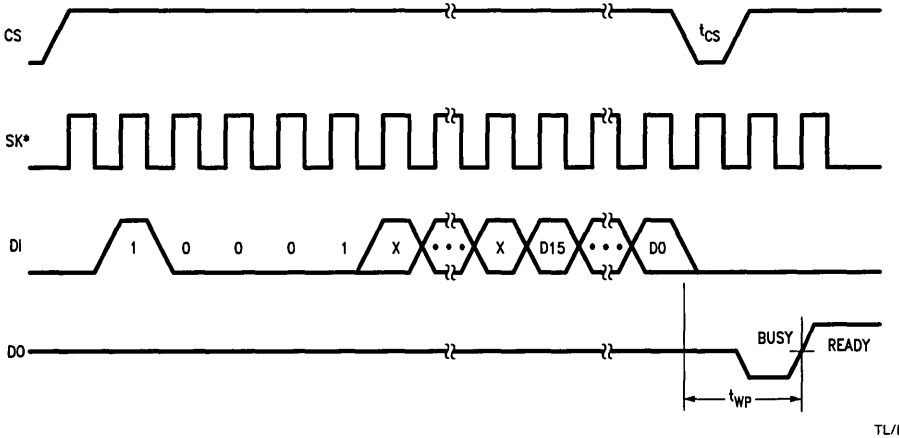


TL/D/10045–8

*Address bit A_5 and A_4 become "don't care" for NM93C06L.

*Address bit A_7 becomes a "don't care" for NM93C56L.

WRAL:

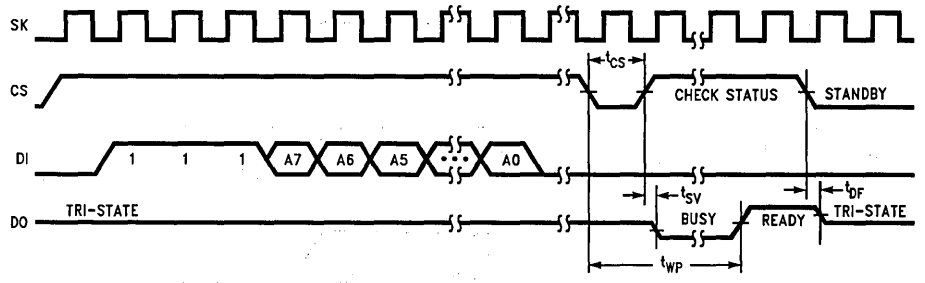


TL/D/10045–9

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

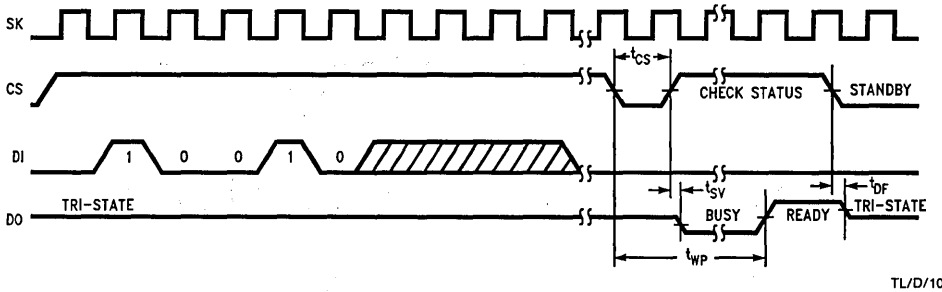
Timing Diagrams (Continued)

ERASE:



TL/D/10045–10

ERAL:



TL/D/10045–11

National Semiconductor

NM93CS06L/CS46L/CS56L/CS66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V to 5.5V) and Data Protect

General Description

The NM93CS06L/CS46L/CS56L/CS66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CSxxL Family functions in an extended voltage operating range and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. N registers ($N \leq 16$, $N \leq 64$, $N \leq 128$, $N \leq 256$) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

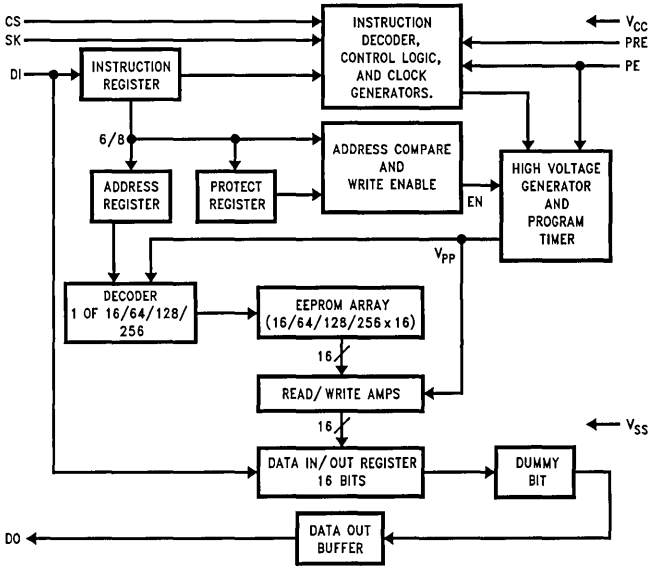
These devices are available in an SO package for small space considerations.

The serial interface that control these EEPROMs is MICROWIRE™ compatible, providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PREN, PRCLEAR, and PRDS.

Features

- Sequential register read
- Write protection in a user defined section of memory
- 2.0V to 5.5V operating range in read mode
- 2.5V to 5.5V operating range in other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct Write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- Packages Available: 8-pin SO, 8-pin DIP

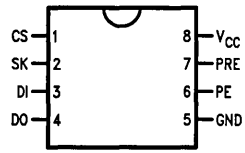
Block Diagram



TL/D/10044–1

Connection Diagrams

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



TL/D/10044–2

Top View

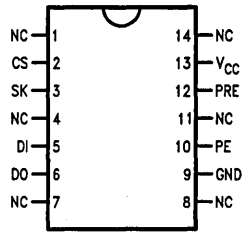
See NS Package Number N08E (N)
See NS Package Number M08A (M8)

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



TL/D/10044–3

Top View

See NS Package Number M14A (M)

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93CS06LN/NM93CS46LN/NM93CS56LN/NM93CS66LN NM93CS06LM8/NM93CS46LM8/NM93CS56LM8/NM93CS66LM*

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93CS06LEN/NM93CS46LEN/NM93CS56LEN/NM93CS66LEN NM93CS06LEM8/NM93CS46LEM8/NM93CS56LEM8/NM93CS66LEM*

*The NM93CS66 is available in 8-pin DIP and 14-pin SO only.

Note: 14-pin SO availability on the 93CS06, CS46 and CS56, contact your local National Semiconductor Sales Office.

LOW VOLTAGE (<4.5) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxxL	0°C to +70°C
NM93CSxxLE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
V_{RPP}	Power Supply Ripple		Peak-to-Peak (Note 5)		0.1 V_{CC}	V
I_{CC1}	Operating Current CMOS Input Levels	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93CS06L–NM93CS66L NM93CS06LE–NM93CSS66LE	CS = V_{IH}, SK = 250 kHz 4.5V≤V_{CC}≤5.5V		3 3	mA
I_{CC3}	Standby Current	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93CS06L–NM93CS66L NM93CS06LE–NM93CSS66LE	V_{OUT} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V≤V_{CC}≤5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V≤V_{CC}≤4.5V	−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V≤V_{CC}≤5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		2V≤V_{CC}≤4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V
f_{SK}	SK Clock Frequency	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	(Note 2)	1 1		μs
t_{SKS}	SK Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	(Note 3)	1 1		μs
t_{CSS}	CS Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to SK	0.2 0.2		μs
t_{PRES}	PRE Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	0.2 0.2		μs

LOW VOLTAGE (<4.5) SPECIFICATIONS (Continued)

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to SK	0.2 0.2		μs
t_{DIS}	DI Setup Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to SK	0.4 0.4		μs
t_{DH}	DO Hold Time		Relative to SK	10		ns
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{PEH}	PE Hold Time	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	Relative to CS Relative to CS	0.4 0.4		μs
t_{PREH}	PRE Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93CS06L–NM93CS66L NM93CS06LE–NM93CS66LE	CS = V_{IL} AC Test		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms

Capacitance (Note 4)

T_A = 25°C, f = 1MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF

V_{CC} Range	AC Test Conditions	
4.5V < V_{CC} < 5.5V	Input Pulse Levels	0.8V and 2.0V
	Timing Measurement Level (V_{IL}/V_{IN}):	0.9V and 1.9V
	Timing Measurement Level (V_{OL}/V_{OH}):	0.8V and 2.0V
	(TTL Load Conditions: I_{OL} = 2.1 mA; I_{OH} = −0.4 mA)	
2.0V < V_{CC} < 4.5V	Input Pulse Levels:	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH}):	0.4V and 1.6V
	Timing Measurement Level (V_{OL}/V_{OH}):	0.8V and 1.6V
	(CMOS Load Conditions: I_{OL} = 10 μA; I_{OH} = − 10 μA)	

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The above SK frequency specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Note 5: Rate of voltage change must be less than 0.5 V/ms.

STANDARD VOLTAGE (4.5 ≤ V ≤ 5.5) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 second)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxxL	0°C to +70°C
NM93CSxxLE	−40°C to +85°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table "M" refers to temperature range (−55°C to +125°C) not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz		3 3	mA
I_{CC3}	Standby Current	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	V_{OUT} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC}+1	V
V_{OL1}	Output Low Voltage	NM93CS06LE-NM93CS66LE NM93CS06LE-NM93CS66LE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OL} = −10 μA	 V_{CC}−0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE		0 0	1 1	MHz
t_{SKH}	SK High Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	(Note 2) (Note 2)	250 300		ns
t_{SKL}	SK Low Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	(Note 2) (Note 2)	250 250		ns
t_{CS}	Minimum CS Low Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	(Note 4) (Note 4)	250 250		ns
t_{CSS}	CS Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	50 50		ns
t_{PRES}	PRE Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	50 50		ns
t_{DH}	DO Hold Time		Relative to SK	10		ns

STANDARD VOLTAGE (4.5 ≤ V ≤ 5.5) SPECIFICATIONS (Continued)

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table "M" refers to temperature range (−55°C to +125°C) not package. (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	50 50		ns
t_{DIS}	DI Setup Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to SK	100 100		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	Relative to CS Relative to CS	250 250		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test		500 500	ns
t_{PD0}	Output Delay to "0"	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test		500 500	ns
t_{SV}	CS to Status Valid	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test		500 500	ns
t_{DF}	CS to DO in TRI-STATE®	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE	AC Test CS = V_{IL}		100 100	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended parts specifies a minimum SK clock period of 1 microsecond; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 microseconds; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial and Extended parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6.: This parameter is periodically sampled and not 100% tested.

Functional Description

The extended voltage EEPROMs of the NM93CSxxL Family have 10 instructions as described below. Note that there is a difference in the length of the instruction for the NM93CS06L and NM93CS46L vs. the NM93CS56L and NM93CS66L since the two larger devices require 2 additional address bits which are not required for the smaller devices. Within the two groups of devices the number of address bits remain constant even though in some cases the most significant bit(s) are not used. In every instruction, the first bit is always a "1" and is viewed as a start bit. The next 8 or 10 bits, depending on device size, carry the op code and address. The address is either 6 or 8 bits, depending on the device size.

Read and Sequential Register Read (READ):

The Read (READ) instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **Sequential Read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is allocated to the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and that the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and therefore enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRCLEAR instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction. The Protect Register will be read as 0s after it is cleared.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register which is the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction, the Protect Register must first be cleared by executing a PRCLEAR operation and the PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06L and NM93CS46L

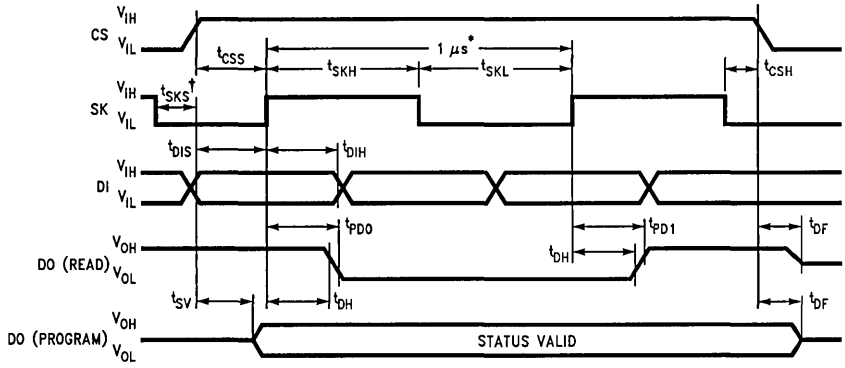
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE. Cleared state is read as 0's.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Instruction Set for the NM93CS56L and NM93CS66L

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE. Cleared state is read as 0's.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

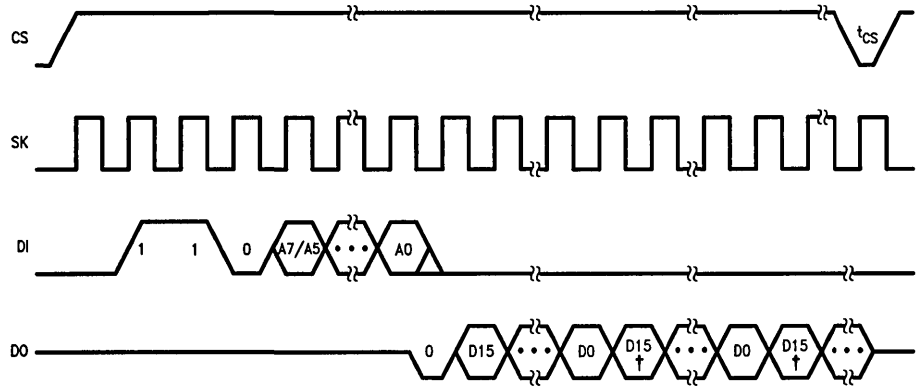
Synchronous Data Timing



TL/D/10044–15

*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:
PRE = 0, PE = X

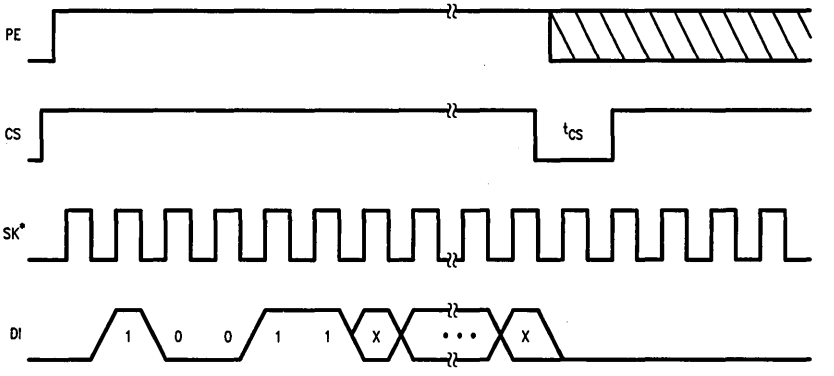


TL/D/10044–5

*Address bit A7 becomes "don't care" for NM93CS56L.
*Address bits A5 and A4 become "don't cares" for NM93CS06L.
†The memory automatically cycles to the next register.

Timing Diagrams (Continued)

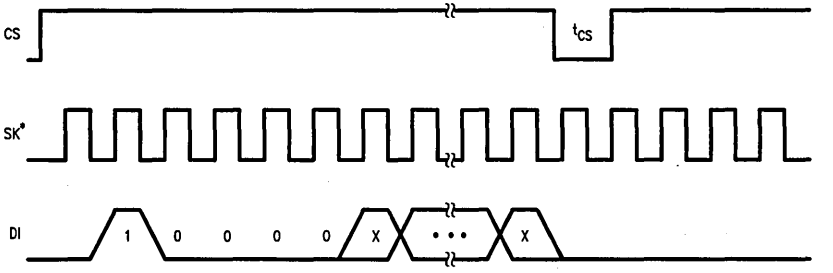
WEN:
PRE = 0, D0 = TRI-STATE



TL/D/10044–6

*The NM93CS56L and NM93CS66L require a minimum of 11 clock cycles. The NM93CS06L and NM93CS46L require a minimum of 9 clock cycles.

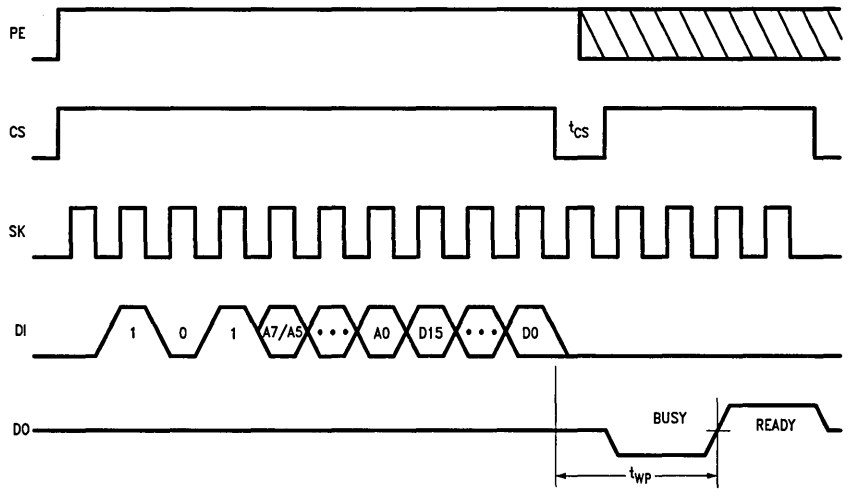
WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/10044–7

*The NM93CS56L and NM93CS66L require a minimum of 11 clock cycles. The NM93CS06L and NM93CS46L require a minimum of 9 clock cycles.

WRITE:
PRE = 0

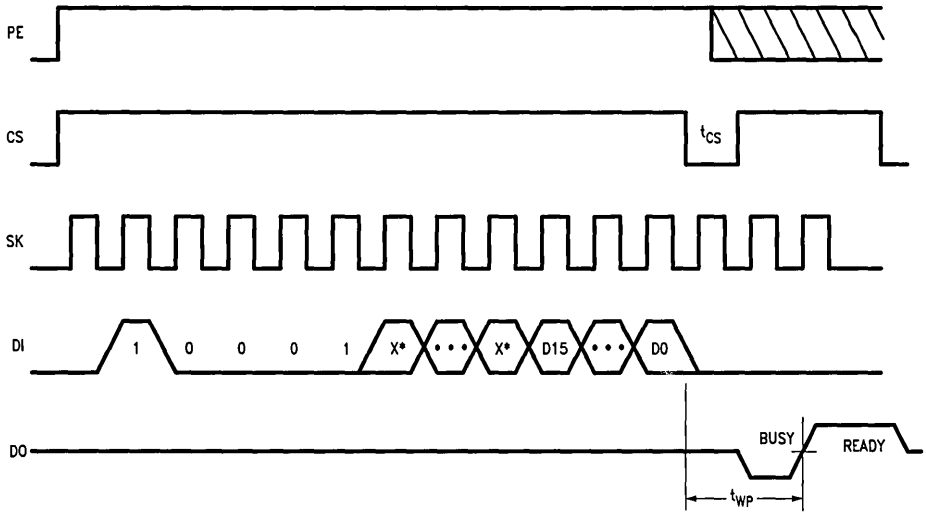


TL/D/10044–8

- Address bit A7 becomes a "don't care" for NM93CS56L.
- Address bits A5 and A4 become "don't cares" for NM93CS06L.

Timing Diagrams (Continued)

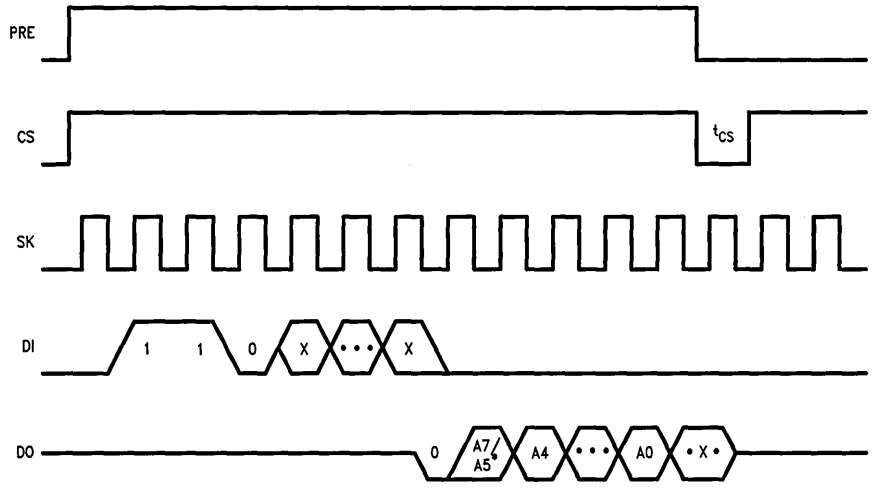
WRALL:
PRE = 0



*Don't care
†Protect Register **MUST** be cleared.

TL/D/10044–9

PRREAD:
PE = X

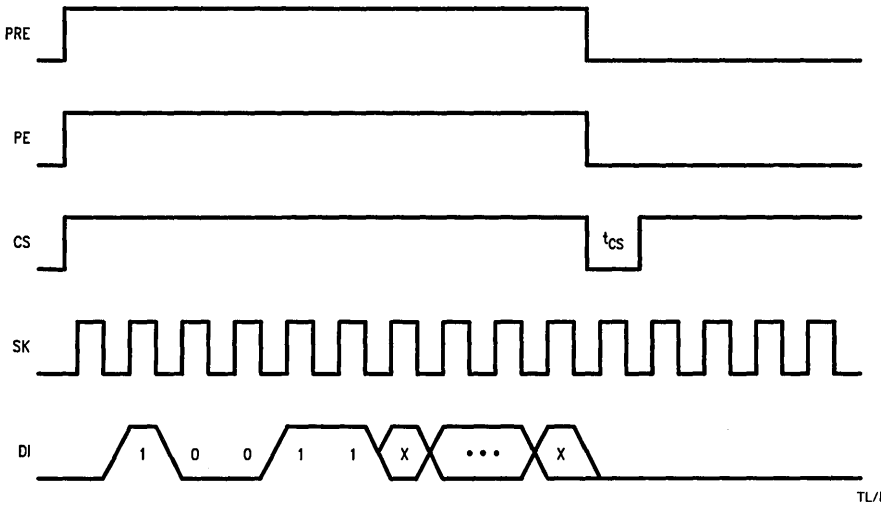


TL/D/10044–10

•Address bits A5 and A4 become "don't cares" for NM93CS06L.
•Address bit A7 becomes "don't care" for NM93CS56L.

Timing Diagrams (Continued)

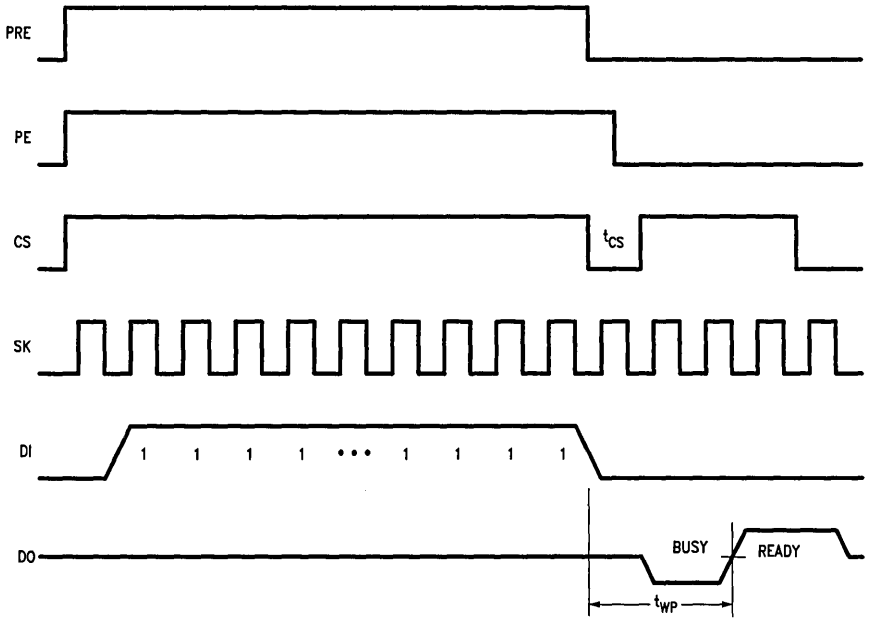
PREN*:
DO = TRI-STATE



TL/D/10044–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR*:

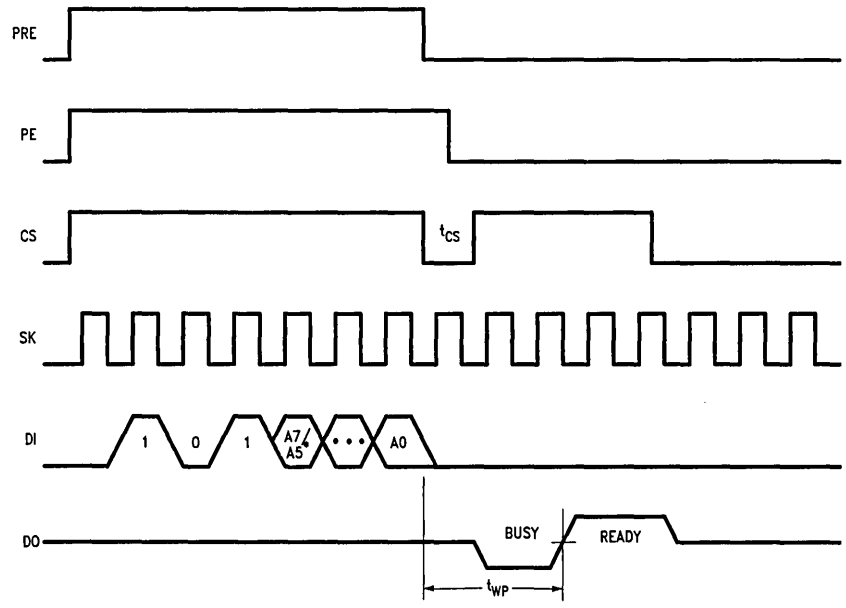


*A PREN cycle must **immediately** precede a PRCLEAR cycle.

TL/D/10044–12

Timing Diagrams (Continued)

PRWRITE†:

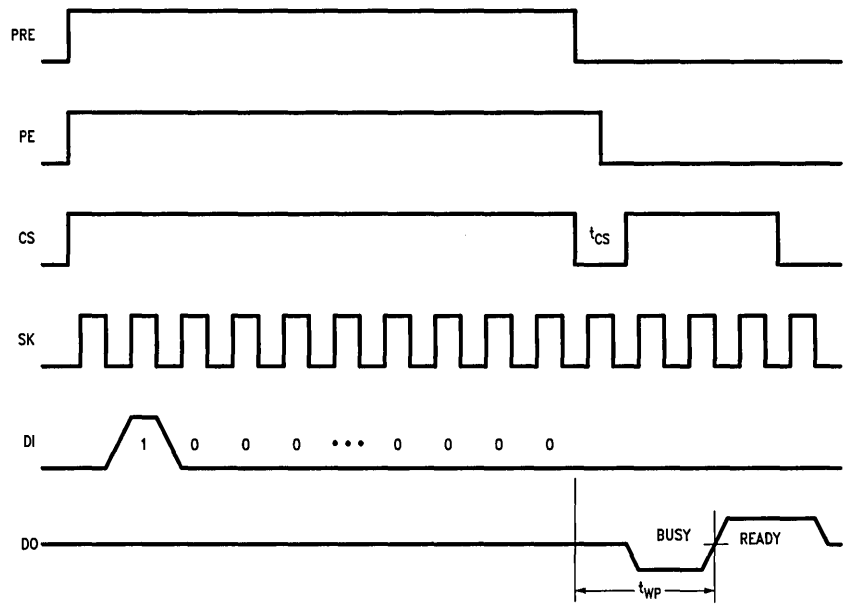


TL/D/10044–13

*Address bit A7 becomes a "don't care" for NM93CS56L.
*Address bits A5 and A4 become "don't cares" for NM93CS06L.

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:



TL/D/10044–14

***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor

NM93C46A
1024-Bit Serial EEPROM
64 x 16-Bit or 128 x 8-Bit Configurable

General Description

The NM93C46A is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C46A is available in an SO package for space considerations.

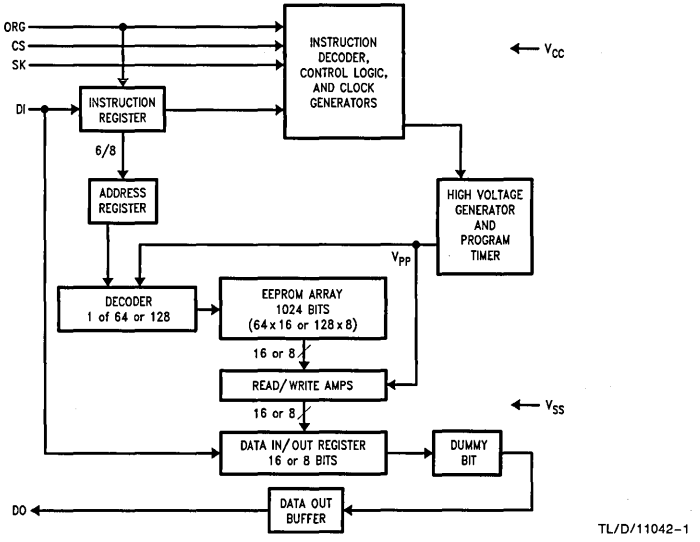
The interface that controls the EEPROM is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46A is compatible with National Semiconductor's NM93C46 if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

- Device status during programming mode
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

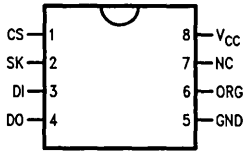
Block Diagram



TL/D/11042–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11042-2

Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46AN
NM93C46AM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46AEN
NM93C46AEM8

Military Temp. Range (−55°C to +125°C)

Order Number
NM93C46AMN
NM93C46AMM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
EDS Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46A	0°C to +70°C
NM93C46AE	−40°C to +85°C
NM93C46AM	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% Unless Otherwise Specified

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46A NM93C46AE NM93C46AM	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46A NM93C46AE NM93C46AM	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93C46A NM93C46AE NM93C46AM	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NM93C46A NM93C46AE NM93C46AM	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM93C46A NM93C46AE NM93C46AM	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC}+1	V
V_{OL1}	Output Low Voltage	NM93C46A NM93C46AE NM93C46AM	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM93C46A NM93C46AE NM93C46AM		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C46A NM93C46AE NM93C46AM	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM93C46A NM93C46AE NM93C46AM	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93C46A NM93C46AE NM93C46AM	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C46A NM93C46AE NM93C46AM	(Note 4) (Note 4) (Note 5)	250 250 500		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% Unless Otherwised Specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46A NM93C46AE NM93C46AM	Relative to SK	50 50 100		ns
t_{DIS}	DI Setup Time	NM93C46A NM93C46AE NM93C46AM	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C46A NM93C46AE NM93C46AM	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C46A NM93C46AE NM93C46AM	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C46A NM93C46AE NM93C46AM	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C46A NM93C46AE NM93C46AM	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms
t_{DH}	D0 Hold Time		Relative to SK	20		ns

Capacitance (Note 6)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46A has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8/9 bits carry the op code and the 6/7-bit address for register selection.

Read (READ)

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into an 8- or 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 8- or 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE)

The Write (WRITE) instruction is followed by 8 or 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The ERASE ALL instruction is not required, see note below.

Write All (WRAL)

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Erase/Write Disable (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Note: The NM93C46A device does not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

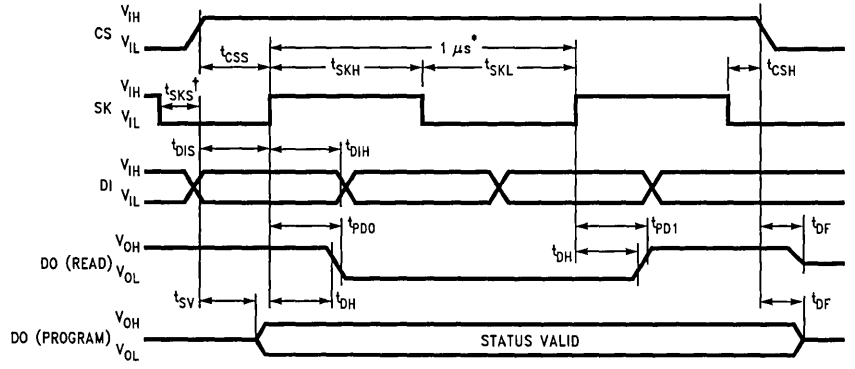
Instruction Set

Instruction	Start Bit	Opcode		Address*		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1	1	A6–A0	A5–A0			Erase Address AN–A0
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0	0	11XXXXX	11XXXX			Program Enable
EWDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" Address Bits.

Timing Diagrams

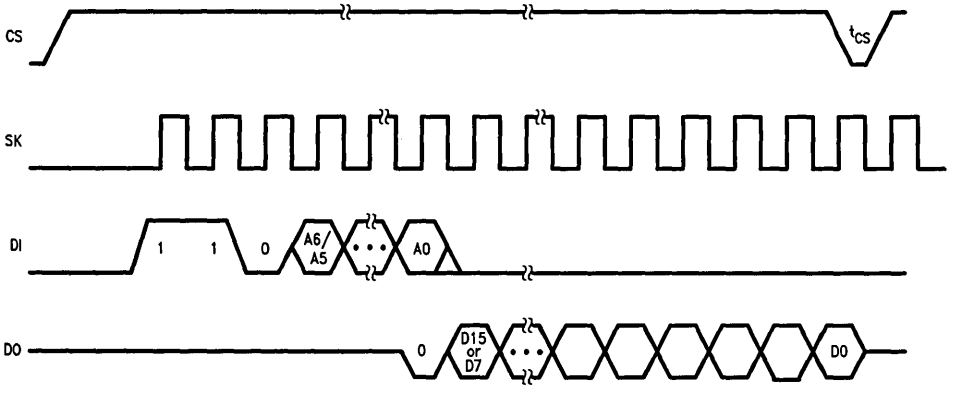
Synchronous Data Timing



TL/D/11042-3

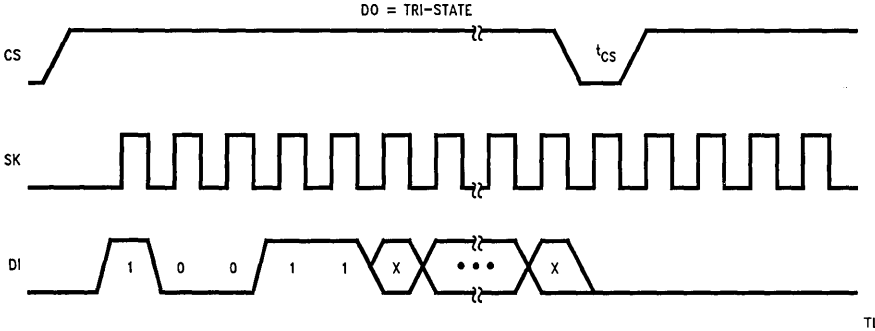
*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ



TL/D/11042-4

EWEN†

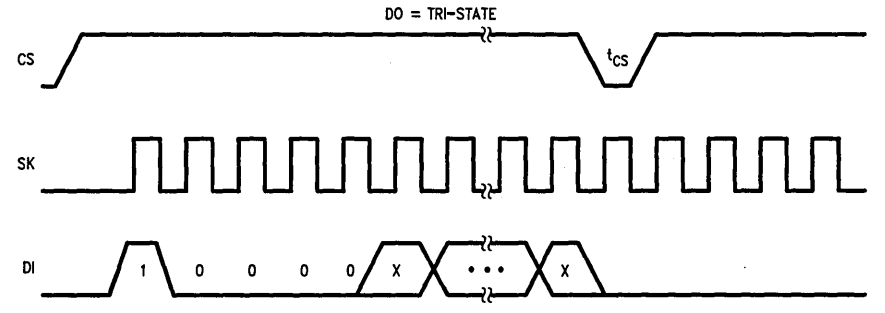


TL/D/11042-5

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

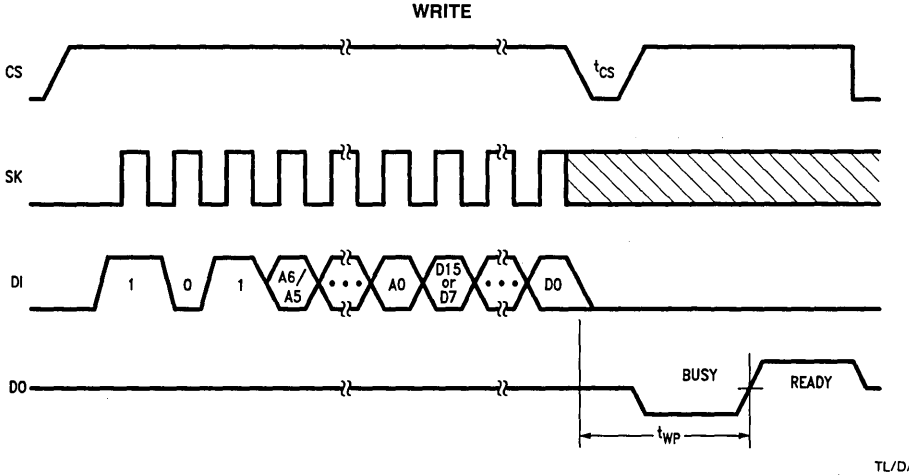
Timing Diagrams (Continued)

EWDS†



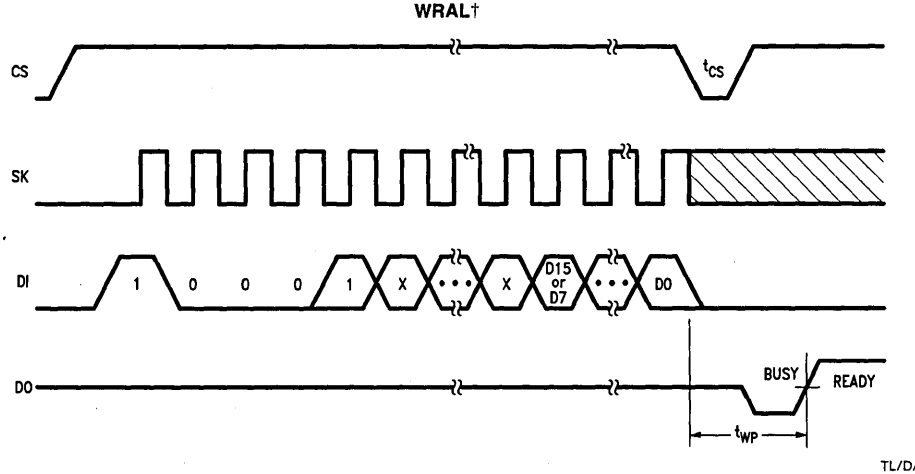
TL/D/11042–6

WRITE



TL/D/11042–7

WRAL†

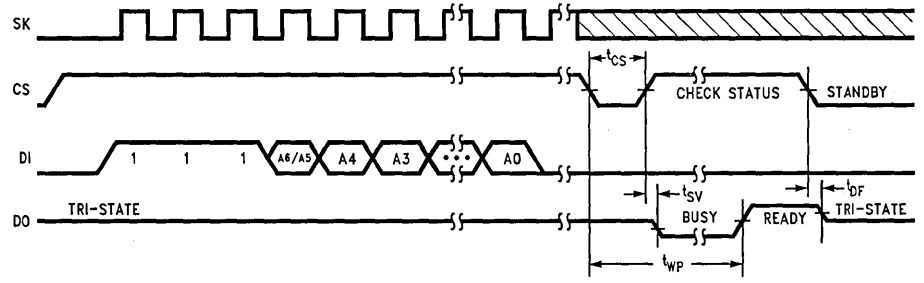


TL/D/11042–8

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

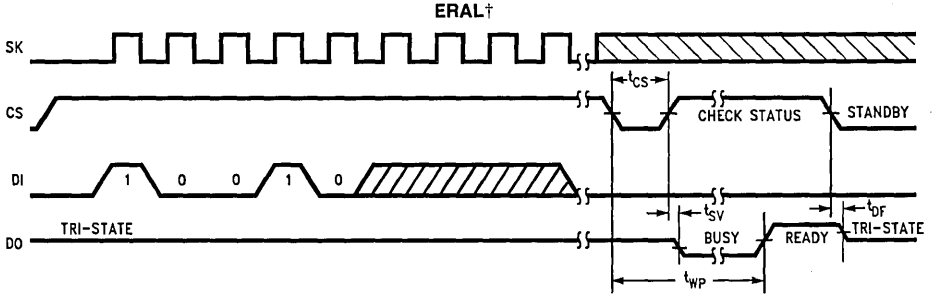
Timing Diagrams (Continued)

ERASE



TL/D/11042–9

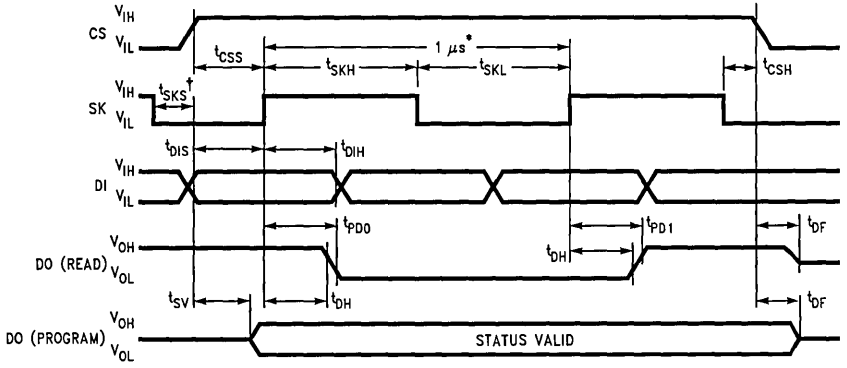
ERAL†



TL/D/11042–10

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Synchronous Data Timing



TL/D/11042–11

*This is the minimum SK period (Note 2).

††t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

National Semiconductor

NM93C46AL
1024-Bit Serial EEPROM
64 x 16-Bit or 128 x 8-Bit Configurable

General Description

The NM93C46AL is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, low power consumption and a wide operating voltage range.

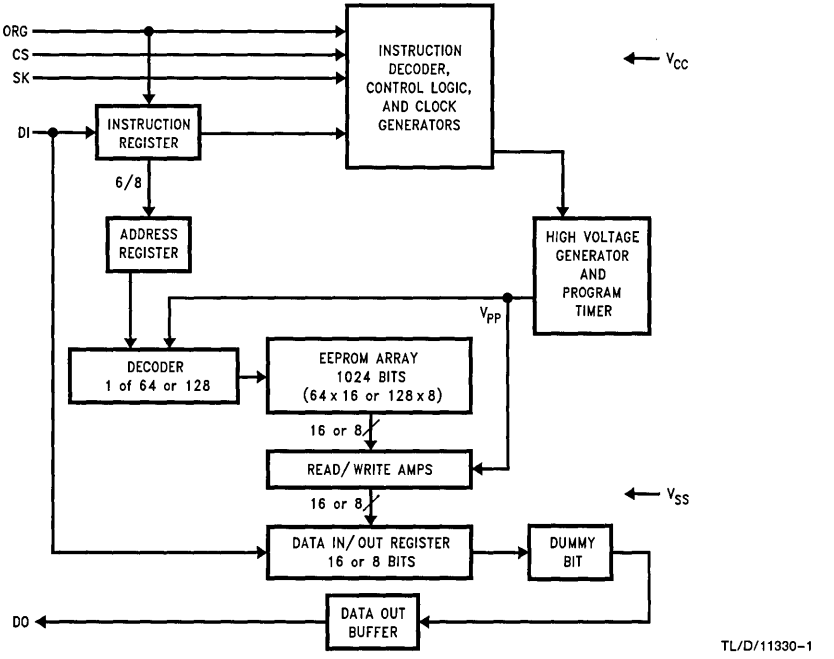
The interface is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46AL: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46AL is compatible with National Semiconductor's NM93C46L if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

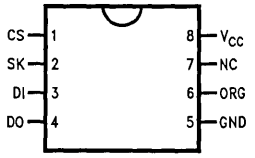
Block Diagram



TL/D/11330–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11330-2

Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46ALN
NM93C46ALM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46ALEN
NM93C46ALEM8

LOW VOLTAGE (<4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Power Supply Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 250 kHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NM93C46AL NM93C46ALE	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
	Pin 6			−10	10	
I_{OL}	Output Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1 0.8 V_{CC}	0.2 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	NM93C46AL NM93C46ALE	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2}	Output Low Voltage		2V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA		0.1 V_{CC}	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	0.9 V_{CC}		V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C46AL NM93C46ALE	(Note 2)	1 1		μs
t_{CS}	Minimum CS Low Time	NM93C46AL NM93C46ALE	(Note 3)	1 1		μs

LOW VOLTAGE (<4.5V) SPECIFICATIONS

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46AL NM93C46ALE	Relative to SK	0.2 0.2		μs
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C46AL NM93C46ALE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C46AL NM93C46ALE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C46AL NM93C46ALE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C46AL NM93C46ALE	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms
t_{DH}	D0 Hold Time		Relative to SK	10		ns

Capacitance (Note 4)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions (>4.5V)

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: For Commercial parts, CS must be brought low for a minimum of 1 μs between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHZ SK = 0.5 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz		3 3	mA
I_{CC3}	Standby Current	NM93C46AL NM93C46ALE	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC}+1	V
V_{OL1}	Output Low Voltage	NM93C46AL NM93C46ALE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE	(Note 2) (Note 3)	250 500		ns
t_{SKL}	SK Low Time	NM93C46AL NM93C46ALE	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NM93C46AL NM93C46ALE	(Note 4) (Note 5)	250 500		ns

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$) (Continued)

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46AL NM93C46ALE	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NM93C46AL NM93C46ALE	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE	NM93C46AL NM93C46ALE	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions (>4.5V)

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46AL has seven instruction sets as described below. Note that each instruction set is broken down into the Start Bit (SB), Op code, Address (if applicable) and Data (if applicable). As shown in the timing diagrams and INSTRUCTION SET tables, address bits will have 6/7 bits and 8/16 bits for the data. All instruction bits are entered into the device on the SK low-to-high transitions.

Programming is enabled by bringing CS to a Logical 0 state for the required t_{CS} period. After this t_{CS} period the self-timed operation may be monitored by bringing CS to a logical 1 and observing the DO status: Logical 1 = READY (Ready for the next instruction) and Logical 0 = BUSY (Programming in progress).

Erase/Write Enable (EWEN):

When V_{CC} is applied to the device, it powers up in the programming Erase/Write disabled state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once this instruction is executed, programming remains enabled until the Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data disturbance, the Erase/Write Disable instruction disables all programming modes and should follow the end of all programming cycles.

Read (READ):

The Read instruction outputs the specified address data on the DO pin. After the READ instruction is received, the instruction and address are decoded and data is transferred from the address to an 8-/16-bit shift register output buffer. A dummy bit (logical 0) precedes all 8-/16-bit data out strings. The READ instruction may be executed from either the enabled or disabled state.

Erase (ERASE):

This instruction, when followed by an address location, programs all bits in the selected register/address to a 1 state (Register erase).

Erase All (ERAL):

This instruction programs all registers/addresses in the memory array to a 1 state (Bulk erase).

Write (WRITE):

This instruction, when followed by an address location and 8/16 bits of data, programs the selected register/address.

Write All (WRAL):

This instruction, when followed by 8/16 bits of data, programs all registers/addresses in the memory array with the specified data pattern (Bulk write).

Note: The NM93C46AL device does not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

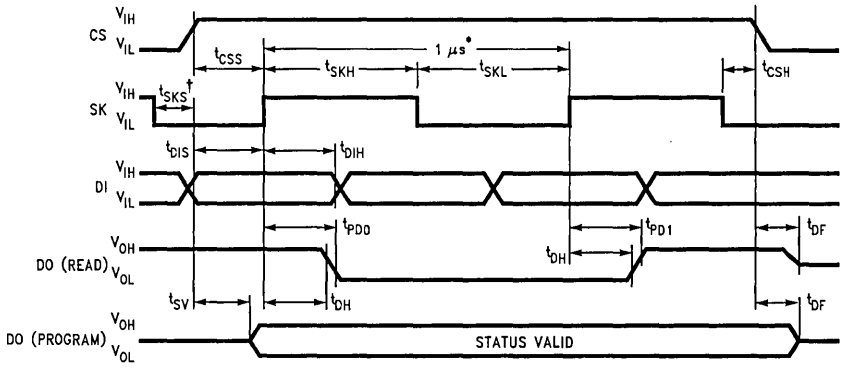
Instruction Set

Instruction	Start Bit	Opcode		Address*		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1	1	A6–A0	A5–A0			Erase Address AN–A0
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0	0	11XXXXX	11XXXX			Program Enable
EWDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" Address Bits.

Timing Diagrams

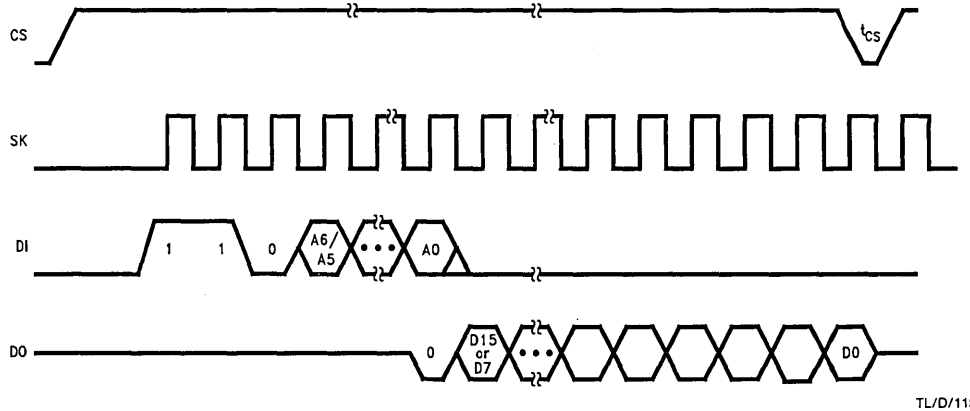
Synchronous Data Timing



TL/D/11330–3

*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

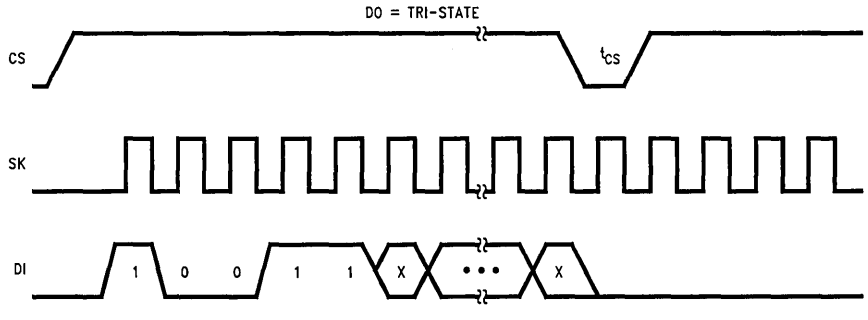
READ



TL/D/11330–4

EWEN†

DO = TRI-STATE

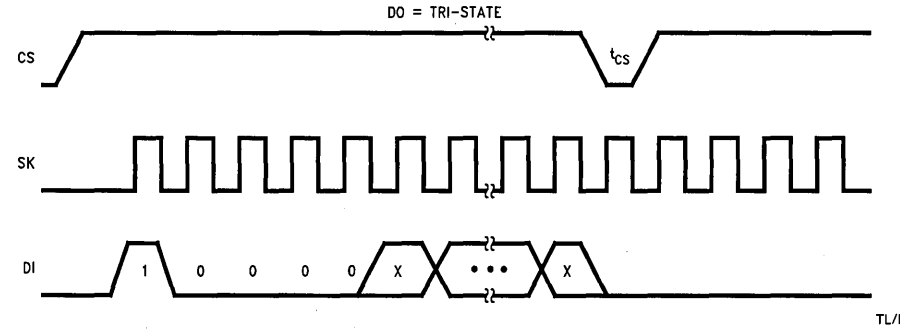


TL/D/11330–5

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

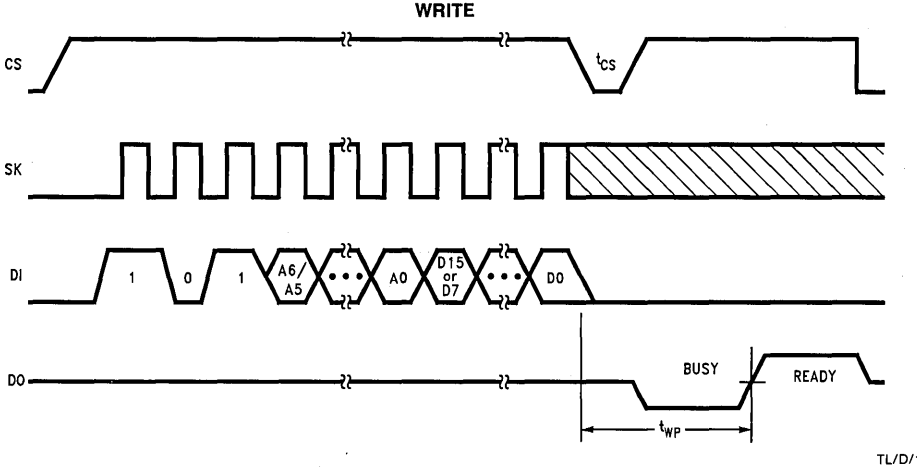
Timing Diagrams (Continued)

EWDS†



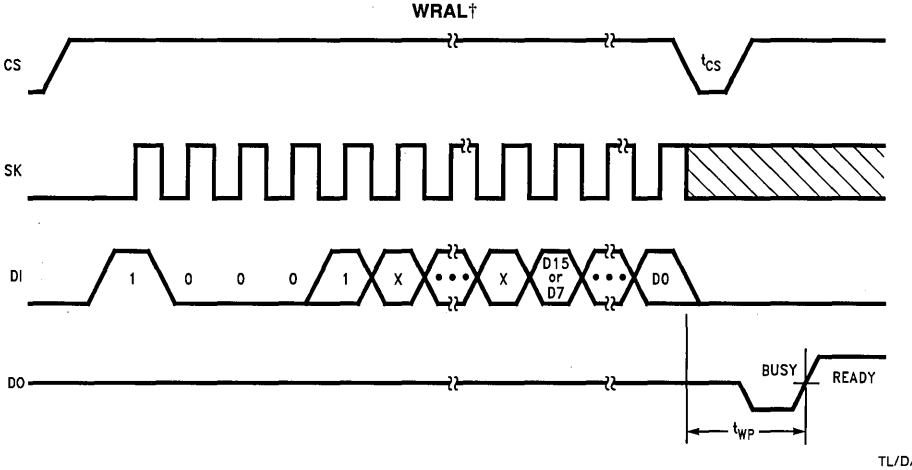
TL/D/11330–6

WRITE



TL/D/11330–7

WRAL†

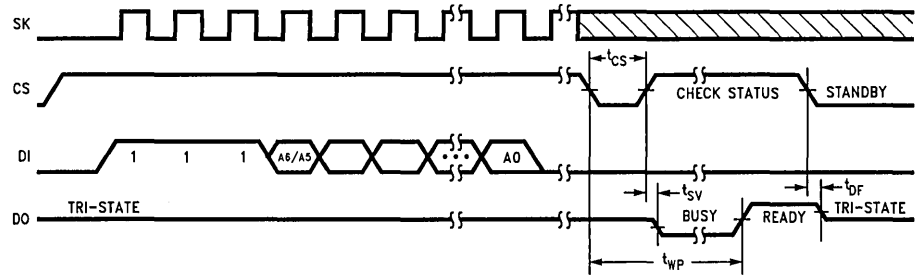


TL/D/11330–8

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

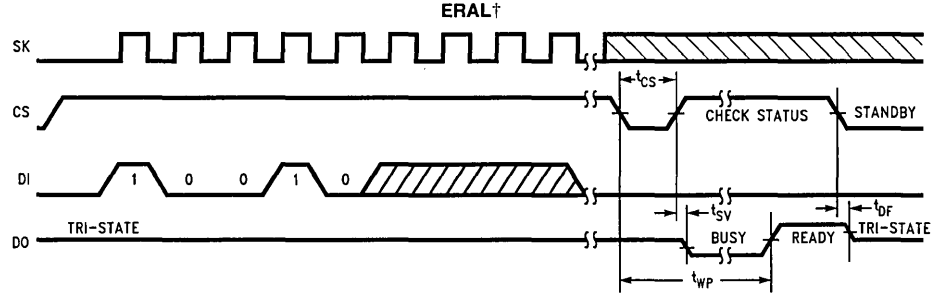
Timing Diagrams (Continued)

ERASE



TL/D/11330–9

ERAL†



TL/D/11330–10

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

National Semiconductor

NM95C12 1K-Bit CMOS EEPROM with Programmable Switches

General Description

The NM95C12 is a 976-bit, CMOS EEPROM with 8 non-volatile programmable outputs that can be used as DIP switches. The 976 bits of memory are divided into 61 registers of 16 bits each and each register can be individually accessed. Registers 61–63 are dedicated to storing the switch settings.

In addition to the 976 bits of EEPROM memory, the NM95C12 contains eight individually programmable outputs which can be used as switches and two additional registers used in conjunction with the switch logic which are volatile. Each switch output may be programmed to provide either a High or Low level. These outputs may also be programmed to form four individual pairs of SPST switches.

The switch configuration information is obtained from a non volatile register whenever power is first applied to the device. This ensures the switches will always have a user determined state upon power-up.

Features

- 8 DIP switch positions or 4 SPST switch positions
- 976 bits of CMOS EEPROM memory available
- 4 mA (max) operating current, 50 μA (max) standby current
- Software write protection
- Serial I/O interface fully MICROWIRE compatible
- Single +5V ±10% operation
- 14-pin DIP or SO package availability
- 100,000 write cycles guaranteed, 500,000 typical
- 40 year data retention
- Reliable floating gate technology
- Sequential register read
- Self-timed write cycle
- Erase cycles not necessary
- Compatible with COPS™ microcontrollers

Block Diagram

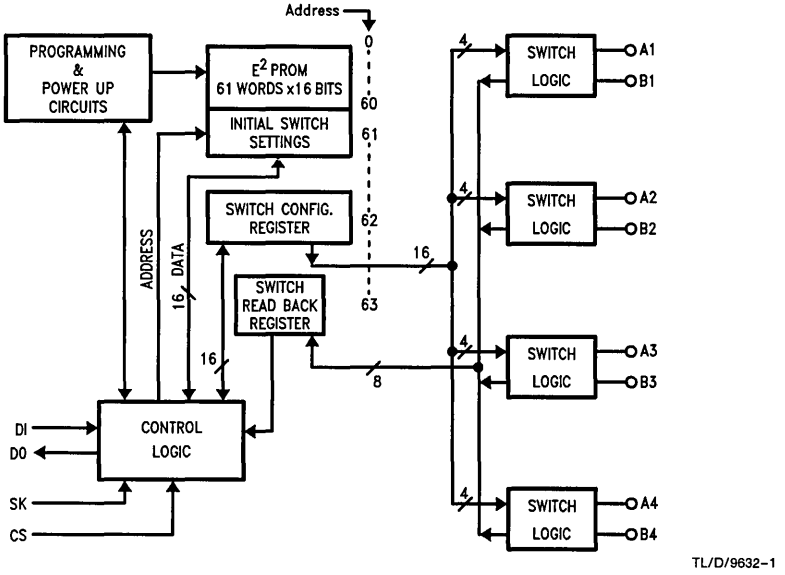


FIGURE 1. Block Diagram

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	6.5V
Voltage at Any Pin	−0.3 to +6.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @25°C	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM95C12	0°C to +70°C
NM95C12E	−40°C to +85°C
NM95C12M*	−55°C to +125°C
Power Supply Voltage (V_{CC})	4.5V to 5.5V

*Contact factory for availability

DC Electrical Characteristics V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	$C_S = V_{IH}$, SK = 1 MHz		4	mA
I_{CC2}	Operating Current TTL Input Levels	$C_S = V_{IH}$, SK = 1 MHz		6	mA
I_{CC3}	Standby Current CMOS Input Levels on Switches	C_S = 0V		50	μA
I_{CC4}	Standby Current TTL Input Levels on Switches	C_S = 0V		800	μA
I_{iL}	Input Leakage	V_{IN} = 0V to V_{CC}	−2.5	+2.5	μA
I_{oL}	Output Leakage	V_{OUT} = 0V to V_{CC}	−2.5	2.5	μA
V_{IL}	Input Low Voltage		−0.1	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	2.4		V
R_{ON}	Switch On Resistance			200	Ω
R_{OFF}	Switch Off Resistance		10		MΩ
V_S	Maximum Voltage Allowed on any Switch Terminal			V_{CC} + 1	V
I_S	Max Current Allowed through Switch Terminals			10	mA

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency	NM95C12		0	1	MHz
		NM95C12E		0	1	
		NM95C12M		0	0.5	
t_{SKH}	SK High Time	NM95C12	(Note 2)	250		ns
		NM95C12E	(Note 2)	300		
		NM95C12M	(Note 3)	500		
t_{SKL}	SK Low Time	NM95C12	(Note 2)	250		ns
		NM95C12E	(Note 2)	250		
		NM95C12M	(Note 3)	500		
t_{SKS}	SK Setup	NM95C12		50		ns
		NM95C12E		50		ns
		NM95C12M		100		ns
t_{CS}	Minimum CS Low Time	NM95C12	(Note 4)	250		ns
		NM95C12E	(Note 4)	250		
		NM95C12M	(Note 5)	500		
t_{CSS}	CS Setup Time	NM95C12	Relative to SK	50		ns
		NM95C12E		50		
		NM95C12M		100		

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PUSR}	Power Up Slew Rate			1		ms
t_{DIS}	DI Setup Time	NM95C12 NM95C12E NM95C12M	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM95C12 NM95C12E NM95C12M	$CS = V_{IL}$ AC Test		100 100 200	ns
t_{ISWD}	Switch Delay from Switch Input	NM95C12 NM95C12E NM95C12M	AC Test		250 250 500	ns
t_{SWPD0}	Switch Delay to 0 from Config. Change	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{SWPD1}	Switch Delay to 1 from Config. Change	NM95C12 NM95C12E NM95C12M	AC Test		500 500 1000	ns
t_{SWS}	A1–A4, B1–B4 Setup Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{SWH}	A1–A4, B1–B4 Hold Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{WP}	Write Cycle Time				10	ms
t_{DH}	DO Hold Time		Relative to SK	10		ns

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

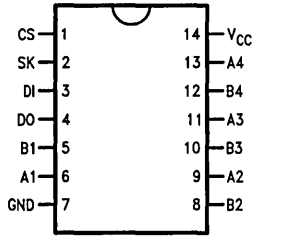
Note 5: For Military parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from +65°C to +85°C.

Connection Diagrams

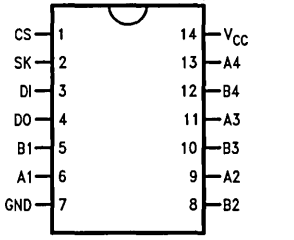
SO Package



TL/D/9632-3

Top View
Order Number NM95C12M, NM95C12EM and NM95C12MM
See NS Package M14A

Dual-In-Line Package



TL/D/9632-2

Top View
Order Number NM95C12N, NM95C12EN and NM95C12MN
See NS Package N14A

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
A1–A4	Switch Terminals
B1–B4	Switch Terminals

Pin Descriptions

Pin Name	Description
CS	Chip Select, Input—This input must be high while communicating with the NM95C12. When this input is LOW, the chip is powered down into the standby mode. It should be noted that the CS does not control the A1 through A4 and B1 through B4 outputs and hence has no effect on them. The CS input must be made LOW after completing an instruction to prepare the control logic to accept the next instruction. If the CS input becomes LOW prematurely, the operation in progress is aborted. If programming the E^2 memory is in progress and the CS goes LOW, the programming is not aborted but will proceed to its normal completion.
SK	Serial Clock, Input—This input is used for clocking the serial I/O. The CS input must be high for clocking to have any effect. Information presented on the DI input will be shifted into the device on the LOW to HIGH transition of the clock. Information from the device will be available on the DO output serially, in response to the LOW to HIGH transition of the clock.
DI	Serial Data In, Input—All information needed for the operation of the device is entered serially from this input. HIGH represents logic '1' and LOW represents logic '0'. The entry order is most significant bit first and least significant bit last.
DO	Serial Data Out, Output, 3-state—When data is read, data from the addressed location will be available on this output serially, in sync with the LOW to HIGH transitions on the SK input. Normally the DO pin is in high impedance state. During a read instruction, when the last bit of the address is shifted in, the DO will go LOW indicating that data will follow. The data will follow in response to the clock transitions. The data will come out most significant bit first and least significant bit last. During E^2 programming operations, this output is also used as the status indicator. During programming operations, LOW indicates Busy (programming in progress) and HIGH indicates Ready. The DO output will be in the high impedance state if the CS input is LOW unconditionally.
A1–A4 B1–B4	Switch Terminals—These pins provide the simulated DIP switch features and hence are called terminals. The behavior of these pins is determined by the settings in the Switch Configuration Register and are independent of the CS input.
V_{CC}	+5V Power Supply.
GND	Ground.

Functional Description

Figure 1 is a block diagram of the NM95C12. It consists of a 62-word X 16-bit E²PROM array, a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and the necessary control logic. It may be noted that only eight bit positions of the SRR are used in the NM95C12.

ADDRESS SPACE

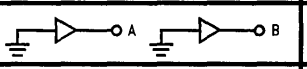
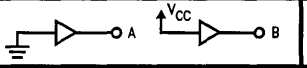
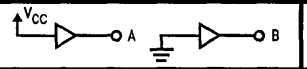
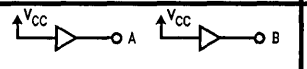
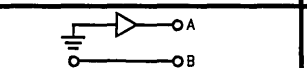
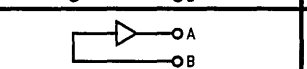
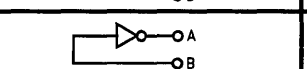
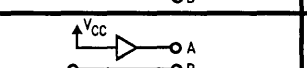
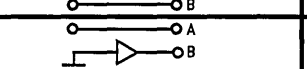
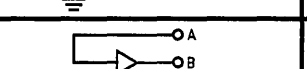
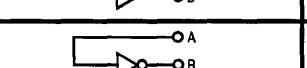
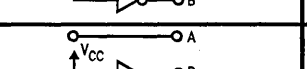
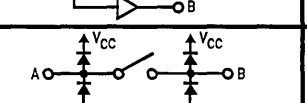
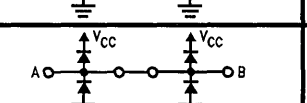
Registers 0–60 of the E²PROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions. Address location 61 is an E² location which also can be read or programmed like any other E² location. However, address 61 is used in the NM95C12 to provide the initial switch configuration information automatically on power-up.

The SCR is located at address 62. The SCR is not an E² location and hence is volatile. It does not have endurance limits or programming time requirements associated with it, allowing the switches to be reconfigured an unlimited number of times.

The SCR is automatically loaded from address 61 on power-up. The SCR controls the switch logic and hence the behavior of the terminals A1 through A4 and B1 through B4.

Located at address 63 is the Switch Readback Register (SRR). This is a read only register.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\overline{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\overline{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

Functional Description (Continued)

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y, and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals. It should be remembered that the CS input has no effect on the behavior of the terminals.

SWITCH READBACK REGISTER

The SRR allows the current logic level present at the switch terminals to be read back via the Microwire bus. The SRR is loaded by the rising edge of SK immediately after the last instruction bit is clocked in (The same clock edge that loads A0). The SRR is loaded on this clock edge only when register 63 (Switch Readback Register) is being read. In the case of switch mode 13 (Analog switch mode), the SRR will not report the actual levels present at the terminals due to this mode being analog levels. In mode 13, bits 15–8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the analog switch mode.

The bit assignments and conceptual function of the SRR is shown in *Figure 3*. As shown, only bits 15 thru 8 are used, and bits 7 thru 0 are always read as logical 0. The SRR is a Read-Only register and if it is written, the device will not perform a write or generate a Ready/Busy status. The SRR is not implemented in EEPROM, allowing an infinite number of cycles in the register.

INSTRUCTION SET

The NM95C12 instruction set contains five instructions, and each instruction is ten bits long. The first 2 bits of the instruction are the start bits (SB) and are always a logical "01", followed by the op code (2 bits) and the address field (6 bits). The WRITE and WRALL instructions are followed by sixteen bits of data (D15–D0) which is written into the memory. Table II is a list of the instructions and their format.

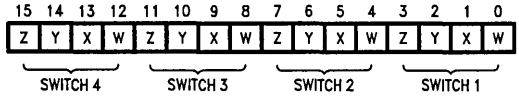

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FIGURE 2. Switch Configuration Register (SCR)

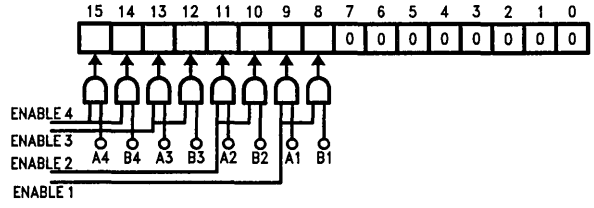

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FIGURE 3. Switch Readback Register (SRR)

TABLE II. NM95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10	A5–A0		Reads data stored in memory, starting at specified address.
WEN	01	00	11XXXX		Write enable must precede all programming modes.
WRITE	01	01	A5–A0	D15–D0	Writes register.
WRALL	01	00	01XXXX	D15-D0	Writes all registers.
WDS	01	00	00XXXX		Disables all programming instructions.

Functional Description (Continued)

WDS (Write Disable): When this instruction is issued, all subsequent writing into the NM95C12 is locked out. Any attempt to write into a locked device is ignored. The NM95C12 powers up in the locked state. The WEN is the only instruction that unlocks the device. The write disable operation has no effect on read operations. Thus reading will occur normally even from a locked device.

WRALL (Write All): When this instruction is executed, the NM95C12 bulk-programs the same 16-bit data pattern into all of its E^2 memory locations (address 0 through 61). The SCR is unaffected since it is not an E^2 location. The data pattern must follow immediately after the last bit of this instruction. The chip enters into the self-timed program mode after CS is brought low, before the next rising edge of SK.

WEN (Write Enable): This instruction is used to unlock the write circuits. The circuits will remain unlocked until the WDS instruction locks them. The NM95C12 powers up in the locked state and hence WEN must be executed prior to any programming instructions.

WRITE (Write/Program): This instruction writes a 16-bit data word into the address location specified by the A_0–A_5 bits of the instruction. The 16 data bits must follow the last bit of the instruction. After loading the WRITE instruction and the 16-bit data, the chip enters into the self-timed program mode when CS is brought low before the next rising edge of the SK clock. If the addressed location is the SCR, then the chip does not enter into the self-timed E^2 programming mode (the SCR is not an E^2 location) but loads the switch configuration data into the SCR. The WRITE instruction can only be aborted by deselecting the chip (CS LOW) before entering all the instruction bits. The NM95C12 does not require erasing prior to writing.

READ (Read): This instruction reads the data from the addressed location. As before, the instruction also contains the address. The data will come out serially on the D0 output on the rising edge of the clock. A logical '0' precedes the 16-bit data (dummy bit).

The NM95C12 has a convenient feature called sequential register read. Normally, the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the D0 pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. It should be noted that in the sequential register read mode, address wrap-around will occur.

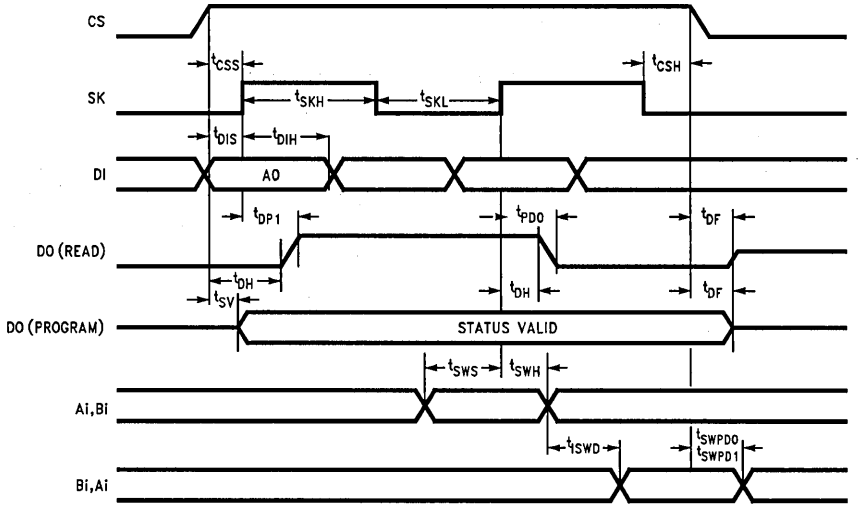
During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bits separating the data words.

Ready/Busy Indication

Programming an E^2 memory takes several milliseconds. Unlike some devices which require the user to keep track of the elapsed time to ensure completion of the programming cycle, the NM95C12 contains an on-chip timer. The timer starts when the CS input goes LOW after the last data bit is entered. After entering a programming cycle (CS forced LOW), the timer status may be observed by forcing the CS input back HIGH. The timer status is available on the D0 pin if the CS input is forced HIGH within one ms of starting the programming cycle. LOW on the D0 pin indicates that the programming is still in progress while HIGH indicates the device is READY for the next instruction. It should be noted that if the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

Timing Diagrams

Synchronous Data Timing



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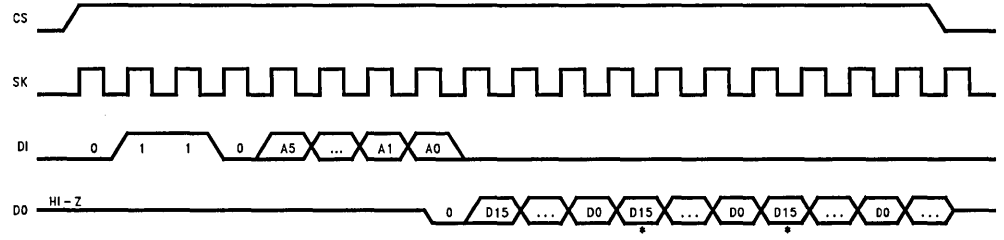
Timing Diagrams (Continued)

Instruction Sequence

READ:



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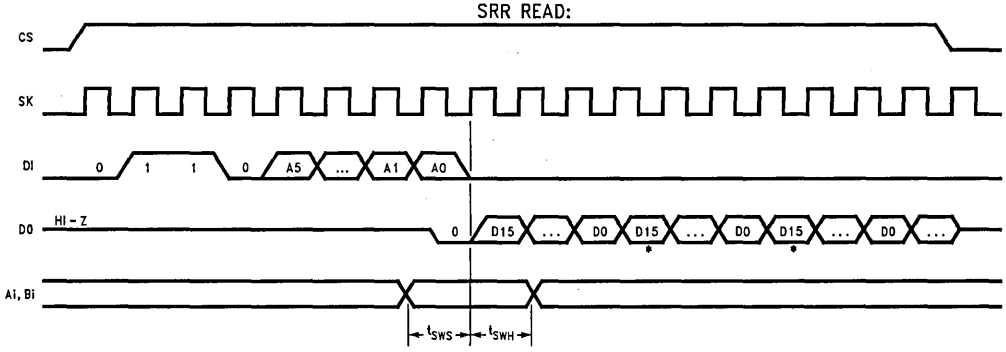
SRR READ:



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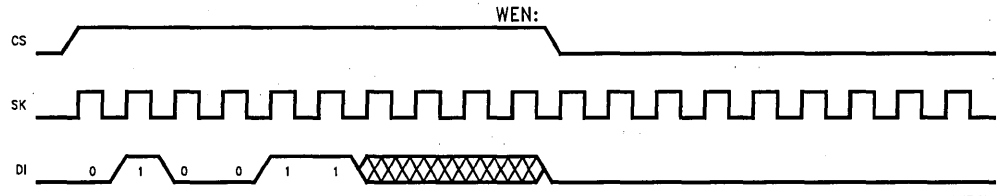
WEN:



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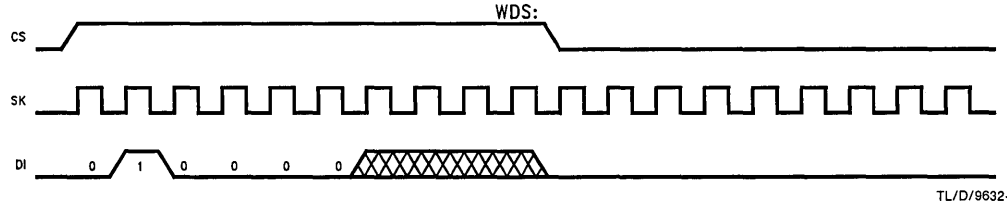
WDS:



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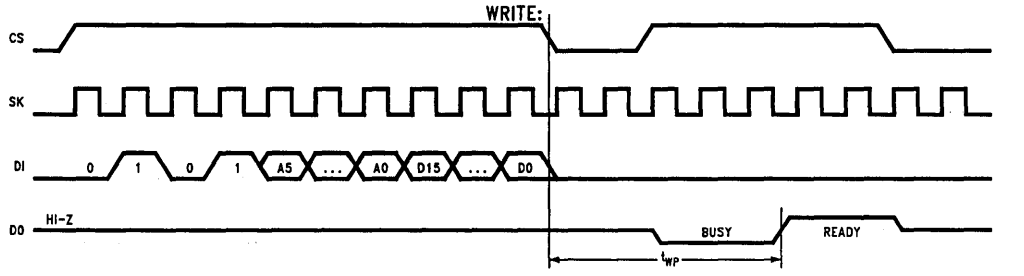
*The memory automatically cycles to the next register.

Timing Diagrams (Continued)

Instruction Sequence (Continued)



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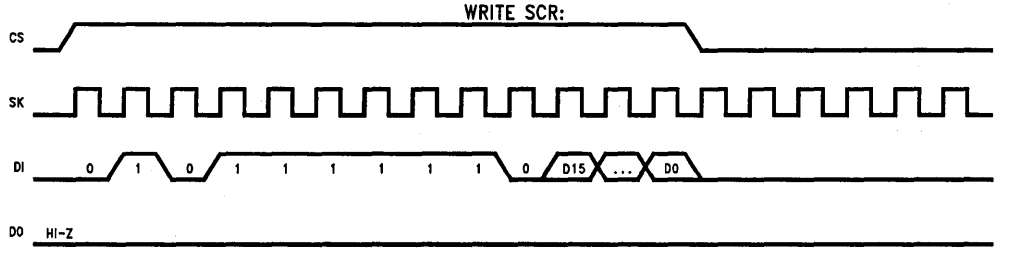

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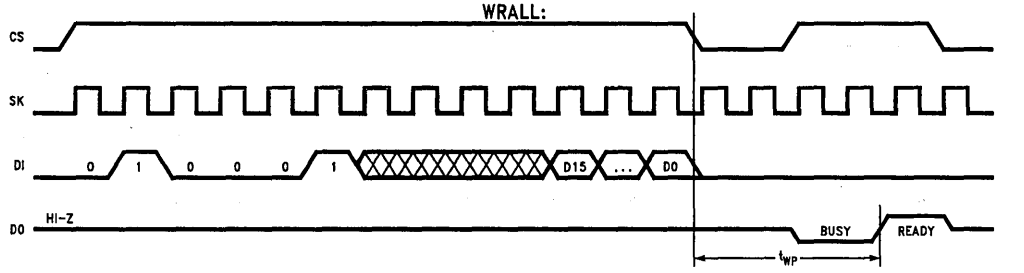

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Section 3
PROMs

Section 3 Contents

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NON-REGISTERED BIPOLAR PROMS

DM74S188 (32 x 8) 256-Bit TTL PROM 3-4
DM74S288 (32 x 8) 256-Bit TTL PROM 3-8
DM74S287 (256 x 4) 1024-Bit TTL PROM 3-12
DM74S387 (256 x 4) 1024-Bit TTL PROM 3-16
DM74LS471 (256 x 8) 2048-Bit TTL PROM 3-20
DM74S472 (512 x 8) 4096-Bit TTL PROM 3-24
DM74S473 (512 x 8) 4096-Bit TTL PROM 3-28
DM74S570 (512 x 4) 2048-Bit TTL PROM 3-32
DM74S571 (512 x 4) 2048-Bit TTL PROM 3-36
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DM74S573 (1024 x 4) 4096-Bit TTL PROM 3-44

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Bipolar PROM Selection Guide

Non-Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) in ns	t_{EA} (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
256	32 x 8 OC	16	DM74S188	35	20	110	0°C to +70°C
	32 x 8 TS	16	DM74S288	35	20	110	0°C to +70°C
	32 x 8 OC	16	DM74S188A	25	20	110	0°C to +70°C
	32 x 8 TS	16	DM74S288A	25	20	110	0°C to +70°C
1024	256 x 4 OC	16	DM74S387	50	25	130	0°C to +70°C
	256 x 4 TS	16	DM74S287	50	25	130	0°C to +70°C
	256 x 4 OC	16	DM74S387A	30	20	130	0°C to +70°C
	256 x 4 TS	16	DM74S287A	30	20	130	0°C to +70°C
2048	512 x 4 OC	16	DM74S570	55	30	130	0°C to +70°C
	512 x 4 TS	16	DM74S571	55	30	130	0°C to +70°C
	512 x 4 OC	16	DM74S570A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM74S571A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM74S571B	35	25	130	0°C to +70°C
	256 x 8 TS	20	DM74LS471	60	30	100	0°C to +70°C
4096	512 x 8 OC	20	DM74S473	60	30	155	0°C to +70°C
	512 x 8 TS	20	DM74S472	60	30	155	0°C to +70°C
	512 x 8 OC	20	DM74S473A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM74S472A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM74S472B	35	25	155	0°C to +70°C
	512 x 8 OC	24	DM74S475	65	35	170	0°C to +70°C
	1024 x 4 OC	18	DM74S572	60	35	140	0°C to +70°C
	1024 x 4 TS	18	DM74S573	60	35	140	0°C to +70°C
	1024 x 4 OC	18	DM74S572A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM74S573A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM74S573B	35	25	140	0°C to +70°C

National Semiconductor

DM74S188
(32 x 8) 256-Bit TTL PROM

General Description

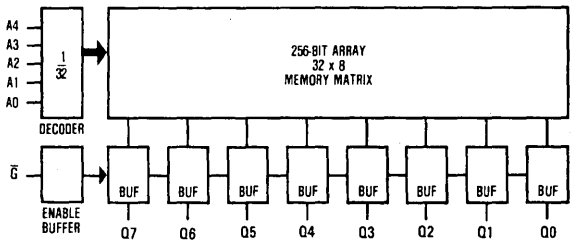
This Schottky memory is organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—25 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



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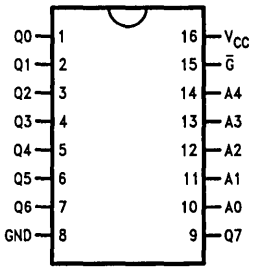
Pin Names

A0–A4	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package



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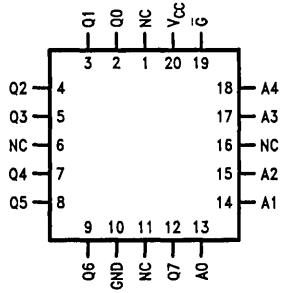
Top View

Order Number DM74S188J, 188AJ, DM74S188N or 188AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9187-3

Top View

Order Number DM74S188V or 188AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S188N	35
DM74S188J	35
DM74S188V	35
DM74S188AN	25
DM74S188AJ	25
DM74S188AV	25

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM74S188			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110	mA

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S188			DM74S188A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	35		17	25	ns
TEA	TEVQV	Enable Access Time		15	20		15	20	ns
TER	TEXQX	Enable Recovery Time		15	25		15	20	ns
TZX	TEVQX	Output Enable Time		15	20		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	20	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S288 (32 x 8) 256-Bit TTL PROM

General Description

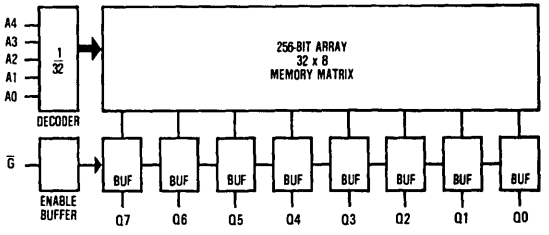
This Schottky memory is organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—25 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

Block Diagram



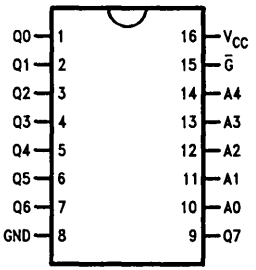
TL/D/8360–1

Pin Names

A0–A4	Addresses
$\overline{G}$	Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

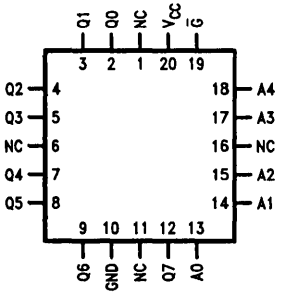


TL/D/8360-2

Top View

Order Number DM74S288J, 288AJ or DM74S288N, 288AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/8360-7

Top View

Order Number DM74S288V or 288AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S288N	35
DM74S288J	35
DM74S288V	35
DM74S288AN	25
DM74S288AJ	25
DM74S288AV	25

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM74S288			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50	μA
					−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA				V
		I_{OH} = −6.5 mA	2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMPERATURE RANGE (0°C to +70°C)

Symbol	Parameter	JEDEC Symbol	DM74S288			DM74S288A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		22	35		17	25	ns
TEA	Enable Access Time	TEVQV		15	20		15	20	ns
TER	Enable Recovery Time	TEXQX		15	25		15	20	ns
TZX	Output Enable Time	TEVQX		15	25		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	25		15	20	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S287
(256 x 4) 1024-Bit TTL PROM

General Description

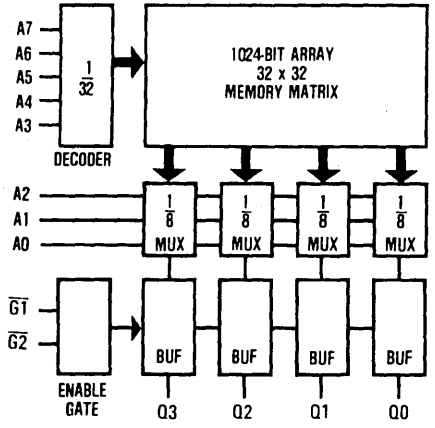
This Schottky memory is organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 30 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- >2000V input protection for electrostatic discharge
- TRI-STATE® outputs

Block Diagram



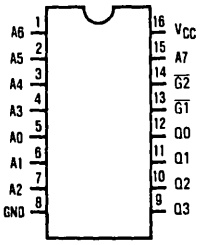
TL/D/8359–1

Pin Names

A0–A7	Addresses
$\overline{G1}$, $\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

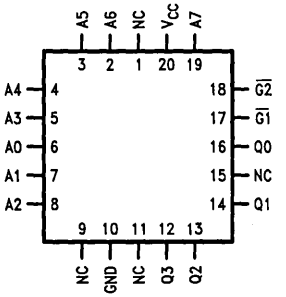


TL/D/8359-2

Top View

Order Number DM74S287J, 287AJ, 287N or 287AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/8359-7

Top View

Order Number DM74S287V or 287AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S287AJ	30
DM74S287J	50
DM74S287AN	30
DM74S287N	50
DM74S287AV	30
DM74S287V	50

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM74S287			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC}=Max, V_{IN}=0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC}=Max, V_{IN}=2.7V			25	μA
		V_{CC}=Max, V_{IN}=5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC}=Min, I_{OL}=16 mA		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			V
V_C	Input Clamp Voltage	V_{CC}=Min, I_{IN}=−18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC}=5.0V, V_{IN}=2.0V T_A=25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC}=5.0V, V_O=2.0V T_A=25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC}=Max, Inputs Grounded All Outputs Open		80	130	mA
I_{OS}	Short Circuit Output Current	V_O=0V, V_{CC}=Max (Note 5)	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC}=Max, V_O=0.45V to 2.4V Chip Disabled			+50	μA
					−50	μA
V_{OH}	Output Voltage High	I_{OH}=−2.0 mA				V
		I_{OH}=−6.5 mA	2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S287			DM74S287A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	50		20	30	ns
TEA	TEVQV	Enable Access Time		15	25		15	20	ns
TER	TEXQX	Enable Recovery Time		15	25		15	20	ns
TZX	TEVQX	Output Enable Time		15	25		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	20	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

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TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S387
(256 x 4) 1024-Bit TTL PROM

General Description

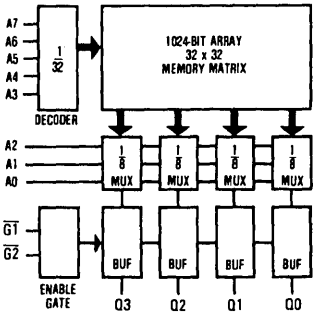
This Schottky memory is organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 30 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



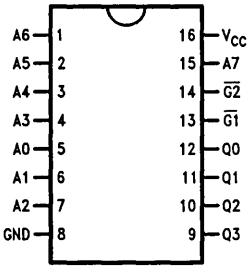
TL/D/9188–1

Pin Names

A0–A7	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

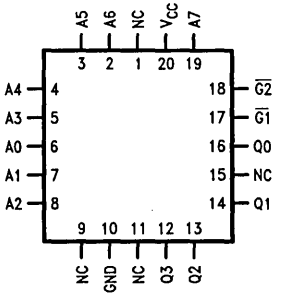


TL/D/9188–2

Top View

Order Number DM74S387J, 387AJ, DM74S387N, 387AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9188–3

Top View

Order Number DM74S387V, 387AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S387AJ	30
DM74S387J	50
DM74S387AN	30
DM74S387N	50
DM74S387AV	30
DM74S387V	50

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to + 7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM74S387			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	Parameter	JEDEC Symbol	DM74S387			DM74S387A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	50		20	30	ns
TEA	Enable Access Time	TEVQV		15	25		15	20	ns
TER	Enable Recovery Time	TEXQX		15	25		15	20	ns
TZX	Output Enable Time	TEVQX		15	25		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	25		15	20	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74LS471
(256 x 8) 2048-Bit TTL PROM

General Description

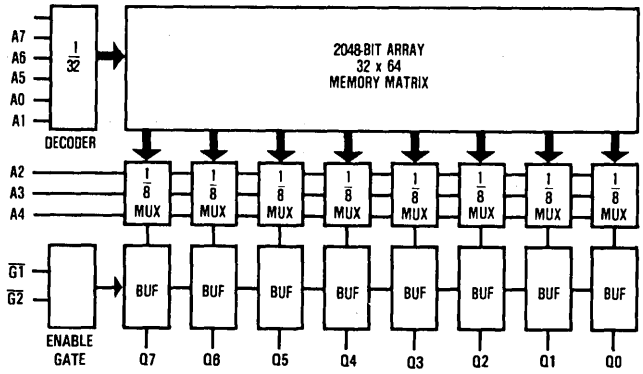
These Schottky memories are organized in the popular 256 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—60 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



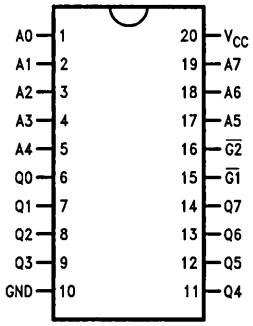
TL/D/9190–1

Pin Names

A0–A7	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

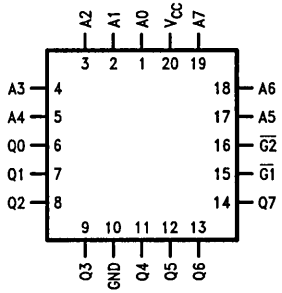


TL/D/9190-2

Top View

Order Number DM74LS471J or DM74LS471N
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9190-3

Top View

Order Number DM74LS471V
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74LS471N	60
DM74LS471J	60
DM74LS471V	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74LS471			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		75	100	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50	μA
					−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA				V
		I_{OH} = − 6.5 mA	2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0v and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM74LS471			Units
			Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60	ns
TEA	TEVQV	Enable Access Time		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30	ns
TZX	TEVQX	Output Enable Time		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S472
(512 x 8) 4096-Bit TTL PROM

General Description

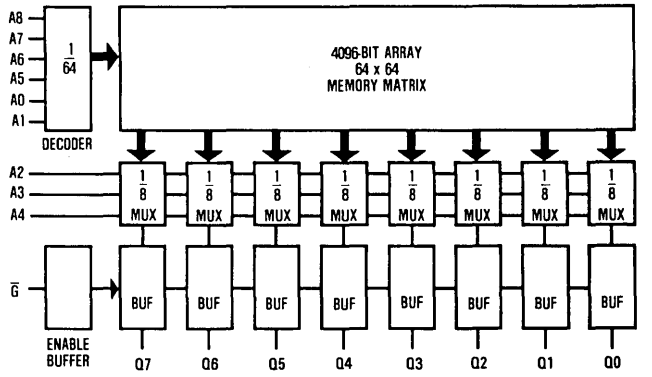
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



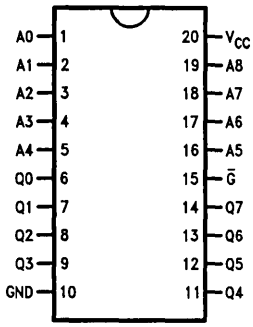
TL/D/9191–1

Pin Names

A0–A8	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

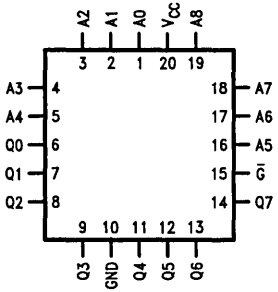


TL/D/9191–2

Top View

Order Number DM74S472J, 472AJ, 472BJ
DM74S472N, 472AN, 472BN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9191–3

Top View

Order Number DM74S472V, 472AV, 472BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S472AN	45
DM74S472BN	35
DM74S472N	60
DM74S472AJ	45
DM74S472BJ	35
DM74S472J	60
DM74S472AV	45
DM74S472BV	35
DM74S472V	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S472			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50	μA
					−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA				V
		I_{OH} = − 6.5 mA	2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S472			DM74S472A			DM74S472B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30		15	25	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S473
(512 x 8) 4096-Bit TTL PROM

General Description

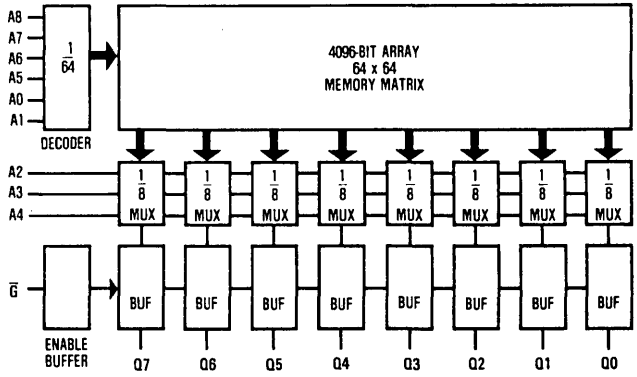
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



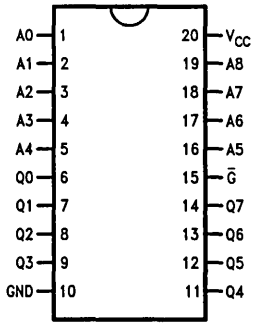
TL/D/9715–1

Pin Names

A0–A8	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

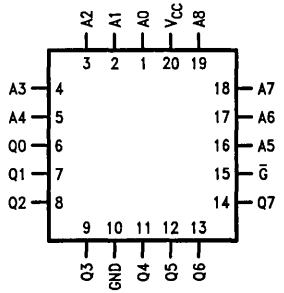


TL/D/9715–2

Top View

Order Number DM74S473J, 473AJ, DM74S473N or 473AN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9715–3

Top View

Order Number DM74S473V or 473AV
See NS Package Number V20A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S473AN	45
DM74S473N	60
DM74S473AJ	45
DM74S473J	60
DM74S473AV	45
DM74S473V	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S473			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP. RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S473			DM74S473A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanuim-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S570
(512 x 4) 2048-Bit TTL PROM

General Description

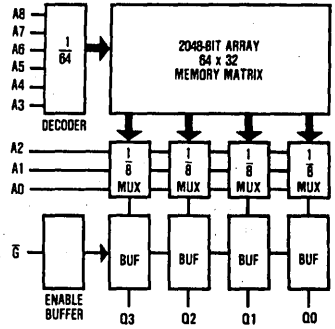
This Schottky memory is organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



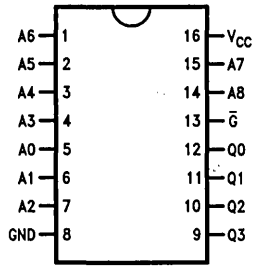
TL/D/9189-1

Pin Names

A0–A8	Addresses
$\overline{G}$	Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

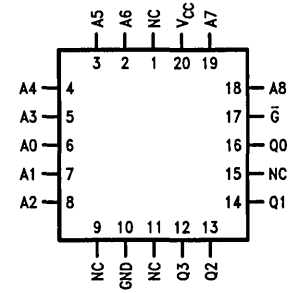


TL/D/9189-2

Top View

Order Number DM74S570J, 570AJ
DM74S570N, 570AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9189-3

Top View

Order Number DM74S570V, 570AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S570AN	45
DM74S570N	55
DM74S570AJ	45
DM74S570J	55
DM74S570AV	45
DM74S570V	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S570			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V, T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded, All Outputs Open		90	130	mA

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S570			DM74S570A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45	ns
TEA	TEVQV	Enable Access Time		20	30		15	25	ns
TER	TEXQX	Enable Recovery Time		20	30		15	25	ns
TZX	TEVQX	Output Enable Time		20	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	30		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S571
(512 x 4) 2048-Bit TTL PROM

General Description

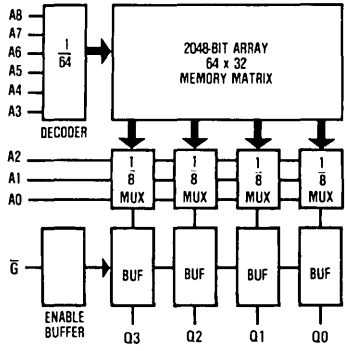
This Schottky memory is organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



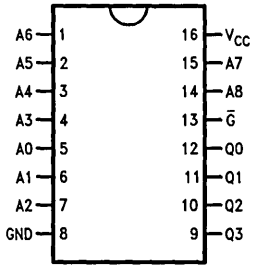
TL/D/9713–1

Pin Names

A0–A8	Address
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

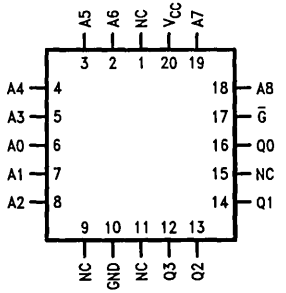


TL/D/9713-2

Top View

Order Number
DM74S571J, 571AJ, 571BJ
DM74S571N, 571AN, 571BN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9713-3

Top View

Order Number
DM74S571V, 571AV, 571BV
See NS Package Number V20A

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S571AN	45
DM74S571BN	35
DM74S571N	55
DM74S571AJ	45
DM74S571BJ	35
DM74S571J	55
DM74S571AV	45
DM74S571BV	35
DM74S571V	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering 10 sec.)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S571			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		90	130	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50	μA
					−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA				V
		I_{OH} = −6.5 mA	2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S571			DM74S571A			DM74S571B			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45		30	35	ns
TEA	TEVQV	Enable Access Time		20	30		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	30		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	30		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	30		15	25		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S572
(1024 x 4) 4096-Bit TTL PROM

General Description

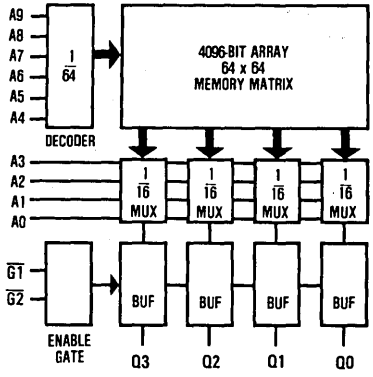
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open collector outputs

Block Diagram



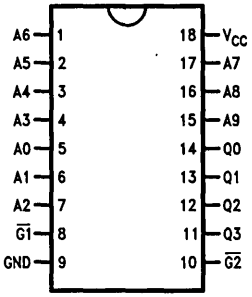
TL/D/9712–1

Pin Names

A0–A9	Addresses
$\overline{G1}$, $\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

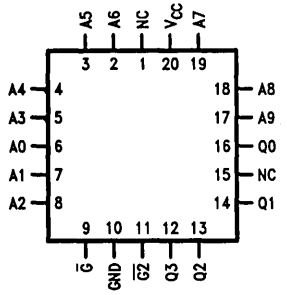


TL/D/9712-2

Top View

Order Number DM74S572J, 572AJ, DM74S572N, 572AN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9712-3

Top View

Order Number DM74S572V, 572AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S572AJ	45
DM74S572J	60
DM74S572AN	45
DM74S572N	60
DM74S572AV	45
DM74S572V	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S572			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameter	DM74S572A			Units
			Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		25	45	ns
T_{EA}	TEVQV	Enable Access Time		15	25	ns
T_{ER}	TEXQX	Enable Recovery Time		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM74S573
(1024 x 4) 4096-Bit TTL PROM

General Description

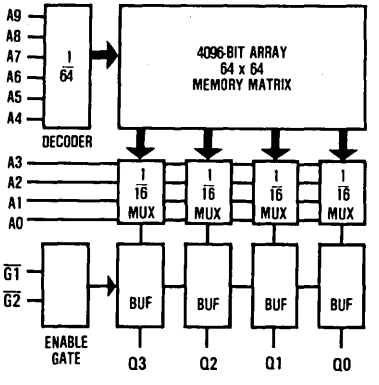
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

Block Diagram



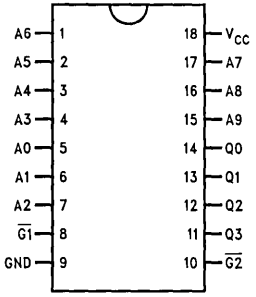
TL/D/9193–1

Pin Names

A0–A9	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

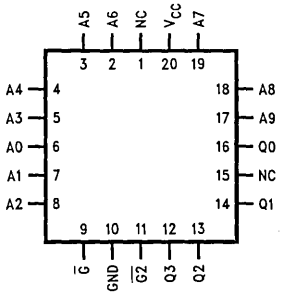


TL/D/9193-2

Top View

Order Number
DM74S573J, 573AJ, 573BJ
DM74S573N, 573AN, 573BN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9193-3

Top View

Order Number
DM74S573V, 573AV, 573BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S573AJ	45
DM74S573BJ	35
DM74S573J	60
DM74S573AN	45
DM74S573BN	35
DM74S573N	60
DM74S573AV	45
DM74S573BV	35
DM74S573V	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) Commercial	4.75	5.25	V
Ambient Temperature (T_A) Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM74S573			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80	V
V_{IH}	High Level Input Voltage		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50	μA
					−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA				V
		I_{OH} = − 6.5 mA	2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S573			DM74S573A			DM74S573B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		20	35		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	35		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	35		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	25		15	25	ns

Functional Description

TESTABILITY

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National Semiconductor

Bipolar PROM Devices in Plastic Leaded Chip Carriers (PLCC)

Introduction of Surface Mount Technology

Recent years have seen rapid advances in microcircuit technology. The integrated circuits of the 1980's are more complex than the circuit boards of the 1960's. It is evident that the next decade will bring demands for packages with higher lead counts and closer lead spacing, both to support the greater system density sought by designers.

National Semiconductor Corporation is committed to surface mount devices, for they provide the most practical solution to these needs. Geared to development of high-complexity semiconductor chips National has placed great emphasis on package development and introducing plastic leaded chip carriers with various number of leads as surface mounted components.

Features of Surface Mount Devices

Surface mount devices have additional features compared to molded Dual-In-Line Packages (DIP):

1. Compact design that saves space during assembly.
2. Mounting on both sides of the substrate.
3. Easier handling and excellent reliability.
4. Automation of the assembly process.
5. Lower board manufacturing costs.
6. Improved operating speed.
7. Increased board density and reduced weight.

Applications

Surface mount devices can be used where substrate size, as well as weight and thickness are limited. The surface mount device can also be used in areas where conventional packages cannot be used. Areas of application include; portable video cassette recorders, video cameras, hand-held computers, personal computers, electronic toys, car electronics, cameras, telephones, and various telecommunication equipment.

Products in PLCC

National Semiconductor has a broad Family of high performance PROMs. All the PAL® and PROM products presently offered in DIP packages will now be available in the PLCC (plastic leaded chip carrier) package including the 15 ns industries fastest PAL.

Advantages of PLCC

1. Permits automated assembly.
2. Lower manufacturing costs.
3. Smaller PLCC size, reduces board density and weight.
4. Lower noise and improved frequency response resulting from shorter circuit paths. Automated assembly ensures accurate component placement which improves reliability and provides more consistent product quality.

Additional Information

National Semiconductor offers a variety of technical briefs covering surface mount topics. These include:

STAR™ Tape-and-Reel Shipping System
Order Number 113635

Getting Started in Surface Mount (Equipment Suppliers)
Order Number 570435

A Basic Guide to Surface Mounting of Electronic Components
Order Number 113615

Reliability Report: Small Outline Packages
Order Number 570430

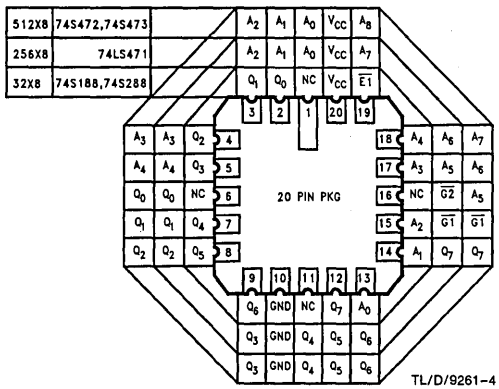
Reliability Report: Plastic Chip Carrier
Order Number 980040

Plastic Chip Carrier Technology
Order Number 113295

PROM

Series-20 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PLCC pins
			STD	A-Series	B-Series			
DM74S188 OC DM74S288 TS	256	32 × 8	35	25	—	110	16	20
DM74S287 TS DM74S387 OC	1K	256 × 4	50	30	—	130	16	
DM74S570 OC DM74S571 TS	2K	512 × 4	55 55	45 45	— 35	130	16	
DM74LS471 TS	2K	256 × 8	60	—	—	100	20	
DM74S572 OC DM74S573 TS	4K	1,024 × 4	60 60	45 45	— 35	140 140	18 18	
DM74S472 TS DM74S473 OC	4K	512 × 8	60 55	45 45	35 —	155 155	20 20	



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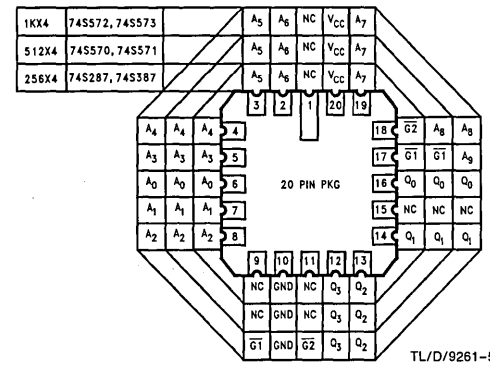

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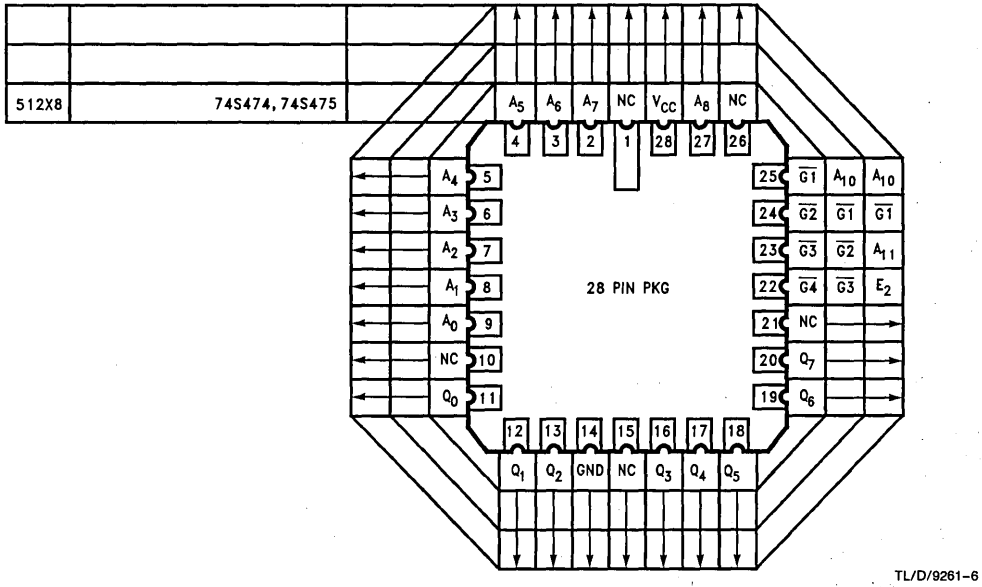
Top View

Series-24 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PLCC pins
			STD	A-Series	B-Series			
DM74S474 TS DM74S475 OC	4K	512 × 8	65	45	35	170	24	

3

Plastic Leaded Chip Carrier



Bipolar PROM Pinout

Programming Support

PROM devices may be programmed with hardware and software readily available in the market. Most programmer manufacturers will offer a PLCC adapter which will fit in existing equipment. For the availability of PLCC adapter please check with your programmer manufacturer.

Programming Equipment

1. Data I/O
2. Structured Design
3. Stag
4. Dig Elec
5. Kontron
6. Prolog
7. Citel

Non-Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more "active low" chip enable inputs.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10.0 V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).
   d) Enable the device by taking the chip enable(s) to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCVH}	Required High V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCVL}	Required Low V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Non-Registered PROM

T_1 = 100 ns Min.

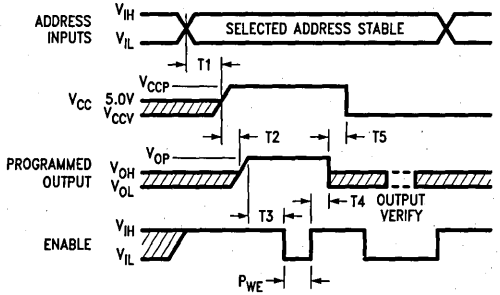
T_2 = 5 μs Min. T2 may be > 0 if V_{CCP} rises at the same rate or faster than (V_{OP})

T_3 = 100 ns Min.

T_4 = 100 ns Min.

T_5 = 100 ns Min.

P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.



NOTE: ENABLE WAVEFORM FOR AN ACTIVE LOW ENABLE. SOME PROMS HAVE MORE THAN ONE CHIP ENABLE. HOLD ALL OTHER ENABLE(S) TO ACTIVE STATE(S).

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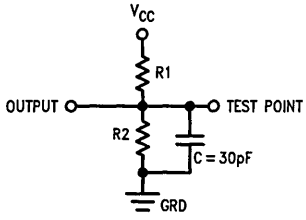
Standard Test Loads

Non-Registered PROMs



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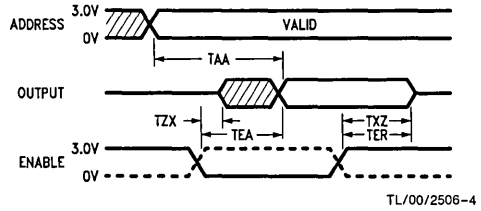
Switching Time Waveforms



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*Device input waveform characteristics are;
Repetition rate = 1 MHz
Source impedance = 50Ω
Rise and Fall times = 2.5 ns max.
(1.0 to 2.0 volt levels)

*TAA is measured with stable enable inputs.

*TEA and TER are measured from the 1.5 volt level on inputs and outputs with all address and enable inputs stable at applicable levels.

*For I_{OL} = 16 mA, R1 = 300Ω and R2 = 600Ω
*for I_{OL} = 12 mA, R1 = 400Ω and R2 = 800Ω.

*"C" includes scope and jig capacitance.

Approved Programmers for NSC PROMs

Manufacturer	System #
DATA I/O	5/17/19/29A
PRO-LOG	M910,M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803
STARPLEX™	

Quality Enhancement Programs For Bipolar Memory

A+ PROGRAM*			B+ PROGRAM		
Test	**Condition**	**Guaranteed LOT AQL 5**	**Test**	**Condition**	**Guaranteed LOT AQL 5**
D.C Parametric and Functionality	25°C	0.05	D.C Parametric and Functionality	25°C	0.05
	Each Temperature Extreme	0.05		Each Temperature Extreme	0.05
A.C. Parametric	25°C	0.4	A.C Parametric	25°C	0.4
Mechanical	Critical	0.01	Mechanical	Critical	0.01
	Major	0.28		Major	0.28
Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4	Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4
	Gross	0.4		Gross	0.4

*Includes 160 hours of burn-in at 125°C.

Section 4

Application Notes

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Protecting Data in Serial EEPROMs

National Semiconductor
Application Brief 15
Paul Lubeck

National offers a broad line of serial interface EEPROMs which share a common set of features:

- Low cost
- Single supply in all modes (+5V ± 10%)
- TTL compatible interface
- MICROWIRE™ compatible interface
- Read-Only mode or read-write mode

This Application Brief will address protecting data in any of National's Serial Interface EEPROMs by using read-only mode.

Whereas EEPROM is non-volatile and does not require V_{CC} to retain data, the problem exists that stored data can be destroyed during power transitions. This is due to either uncontrolled interface signals during power transitions or noise on the power supply lines. There are various hardware design considerations which can help eliminate the problem although the simplest most effective method may be the following programming method.

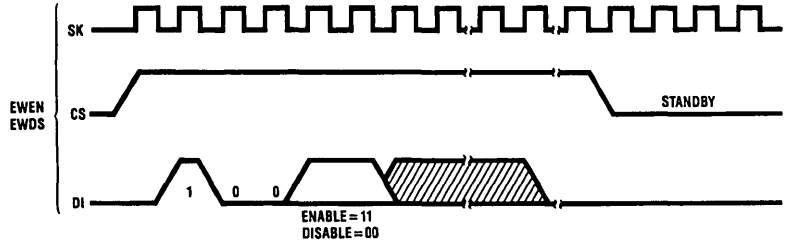
All National Serial EEPROMs, when initially powered up are in the Program Disable Mode*. In this mode, the EEPROM will abort any requested Erase or Write cycles. Prior to Erasing or Writing it is necessary to place the device in the Program Enable Mode†. Following placing the device in the Program Enable Mode, Erase and Write will remain enabled until either executing the Disable instruction or removing V_{CC}. Having V_{CC} unexpectedly removed often results in uncontrolled interface signals which could result in the EEPROM interpreting a programming instruction causing data to be destroyed.

Upon power up the EEPROM will automatically enter the Program Disable Mode. Subsequently the design should incorporate the following to achieve protection of stored data.

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.
2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction to return

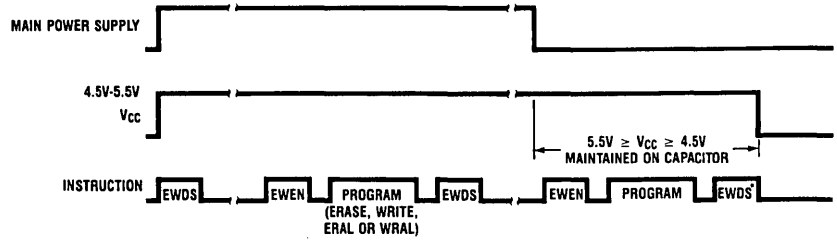
*EWDS or WDS, depending on exact device.

†EWEN or WEN, depending on exact device.



TL/D/7085–1

FIGURE 1. EWEN, EWDS Instruction Timing



TL/D/7085–2

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

the device to the read-only mode and protect the stored data from accidental disturb during subsequent power transients or noise.

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor must be large enough to maintain V_{CC} between 4.5 and 5.5 volts for the total duration of the store operation, INCLUDING the execution of the EWDS instruction immediately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

Electronic Compass Calibration Made Easy with EEPROMs

National Semiconductor
Application Brief 18
Doug Zrebski

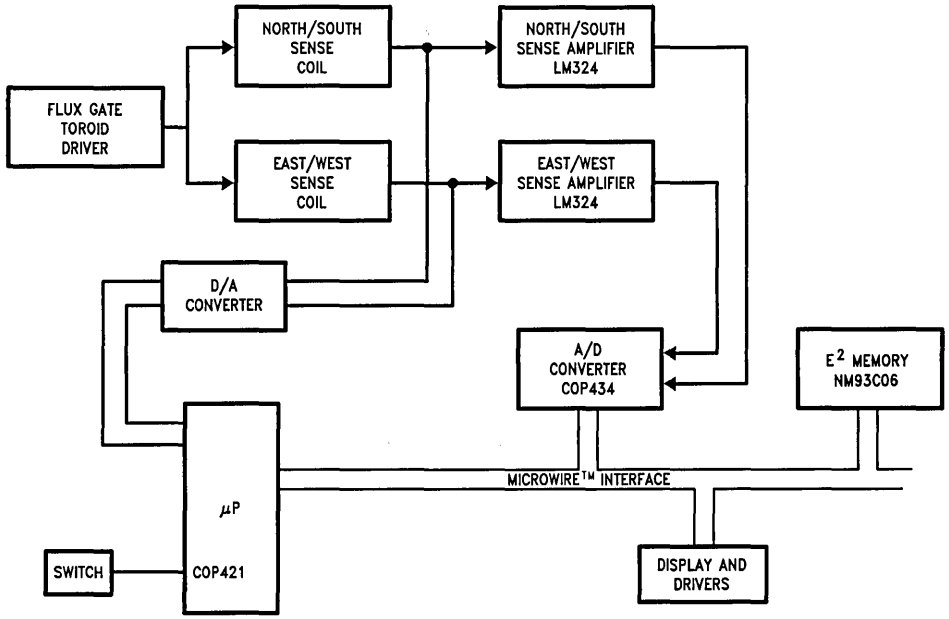
When a compass is first installed in a vehicle, or when new equipment, such as car speakers, are added to a vehicle with a compass, the compass must be compensated for stray magnetic fields. With a magnetic compass, it must be pointed towards magnetic north and then adjusted. This procedure is repeated at all four main points of the compass until the compass is calibrated. This procedure is lengthy and also requires another calibrated compass to point the vehicle in the correct direction.

The block diagram illustrates an electronic compass that, with the aide of an E^2 memory, makes adjusting a compass as easy as pushing a button, and also eliminates the need for another compass. In addition it gives you the ability to adjust for variation between magnetic and true north. This is a major advantage because it is something that even the most expensive magnetic compass cannot do.

The brain of the electronic compass is the COP421 microcontroller. There are two sense coils, one for north/south and one for east/west. The output of each of the sense amplifiers is an analog voltage which is fed into the A to D converter. These voltages are read by the COP421 over the microwire interface. From these voltages, the microcontroller determines the direction and displays the results once again over the microwire interface. To compensate the compass in a new environment the procedure is very simple. Start by pointing the car in any direction and push the switch. The CPU at this time will measure the voltage at the sense amplifiers and store this information in the E^2 memory over the microwire interface. Now the vehicle is turned 180°, and the button is pushed again. The same procedure will be followed internally. The compensation procedures are now complete. During operation the CPU will compensate for stray fields by adding an analog voltage back into the sense amplifiers. This value is stored in E^2 memory and not lost when the power is turned off, but is readjustable if its environment is modified.

Compass variation is the difference between true and magnetic north. This variation differs all over the world and is something that must be taken into consideration when navigating by compass. With the E^2 memory device, a variance can be programmed in for any given location. In California this is approximately 17°, in Michigan approximately 1°. Once again, this cannot be accomplished by a magnetic compass, and would have been impossible to accomplish without an E^2 memory device.

Electronic Compass Block Diagram



TL/D/8613–1

Designing with the NM93C06 A Versatile Simple to Use E^2 PROM

National Semiconductor
Application Note 338
Masood Alavi

This application note outlines various methods of interfacing an NM93C06 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1–6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NM93C06; as well as how serial data outputted from an NM93C06 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NM93C06.

The third part of the application note shows a list of various applications that can use a NM93C06.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

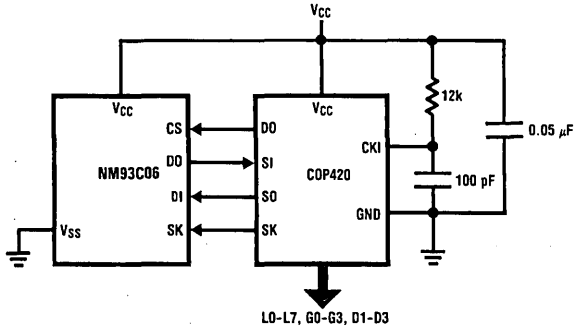
1. Allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. Allow for any number of read cycles.
3. Allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E^2P-ROM, not so in RAMs.)
4. No battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286–1

FIGURE 1. NM93C06—COP420 Interface

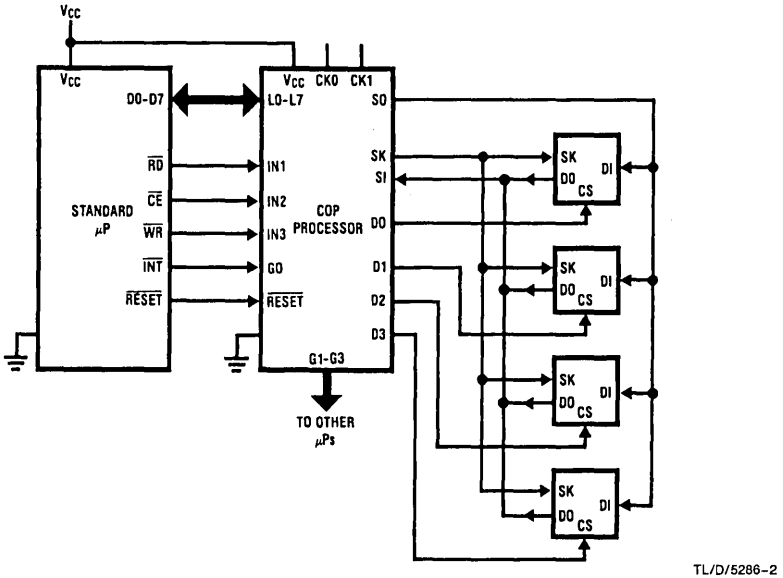
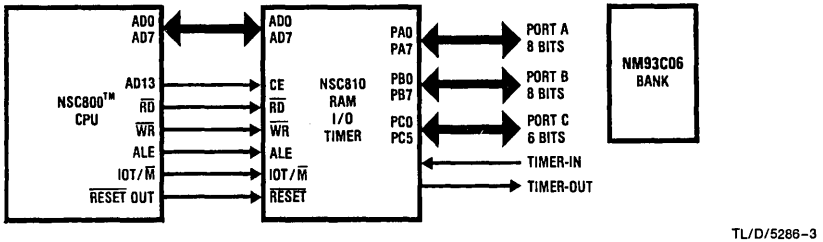


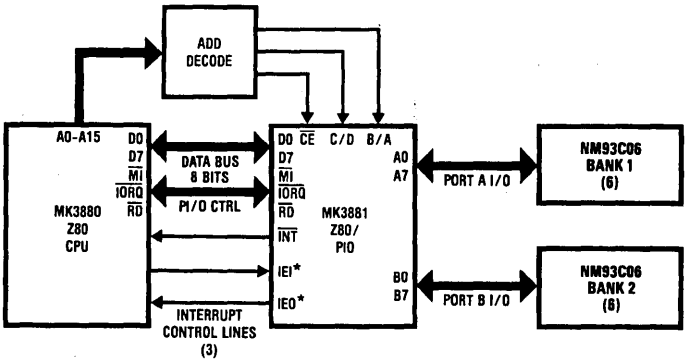
FIGURE 2. NM93CO6—Standard μP Interface Via COP Processor



PA0 → SK
PA1 → DI/DO } Common to all 9306's
PA2–7 → 6CS for 6– 9306's

* SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.
* CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase. SK may be turned off.

FIGURE 3. NSC800™ to NM93C06 Interface (also Valid for 8085/8085A and 8156)

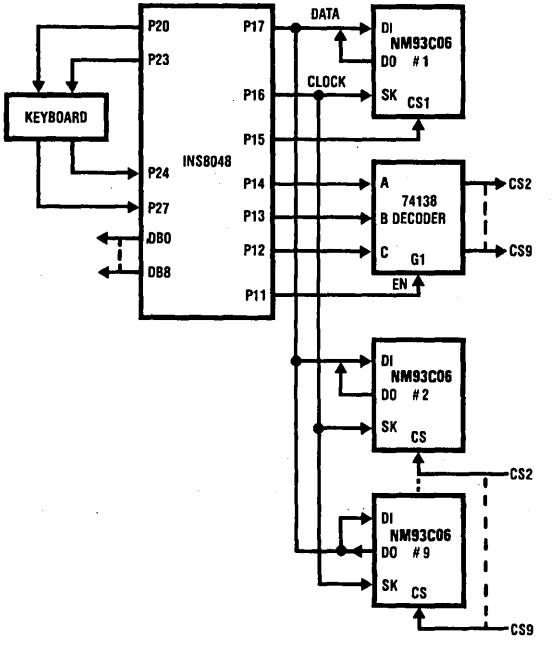


TL/D/5286–4

Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

* Only used if priority interrupt daisy chain is desired
* Identical connection for Port B

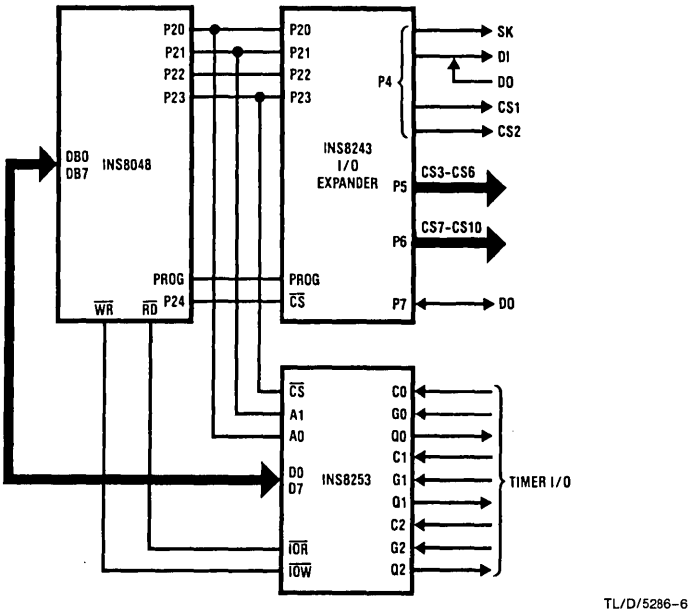
FIGURE 4. Z80—NM93C06 Interface Using Z80-PIO Chip



TL/D/5286–5

* SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NM93C06 frequency range.
* DO may be brought out on a separate port pin if desired.

FIGURE 5. 48 Series μP—NM93C06 Interface

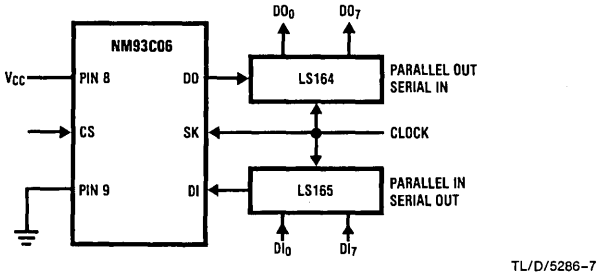


TL/D/5286–6

Expander outputs

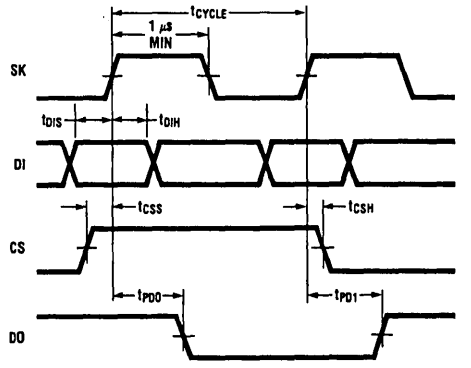
	DI SK	(COMMON)
Port 4	CS1	
	CS2	
Port 5-6	CS3–CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion



TL/D/5286–7

FIGURE 7. Converting Parallel Data into Serial Input for NM93C06



TL/D/5286–8

Min	Max
t_{CYCLE} 0	250 kHz
t_{DIS} 400	ns
t_{D1H} 400	ns
t_{CSS} 200	ns
t_{CSH} 0	ns
t_{PD0}	2 μs
t_{PD1}	2 μs

FIGURE 8. NM93C06 Timing

THE NM93C06A

Extremely simple to interface with any μP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Serial Clock input
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read, TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

*Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

**DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NM93C06

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most μPs this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard μP speeds. Symmetrical duty cycle is irrelevant if SK HI time is ≥ 2 μs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for a minimum of ten years independent of V_{CC}, which may be on or off. Read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E^2PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

INSTRUCTION SET

Instruction	SB	Opcode	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NM93C06 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

The following is a list of various systems that could use a NM93C06

A. Airline terminal
Alarm system
Analog switch network
Auto calibration system
Automobile odometer
Auto engine control
Avionics fire control

B. Bathroom scale
Blood analyzer
Bus interface

C. Cable T.V. tuner
CAD graphics
Calibration device
Calculator—user programmable
Camera system
Code identifier
Communications controller
Computer terminal
Control panel
Crystal oscillator

D. Data acquisition system
Data terminal

E. Electronic circuit breaker
Electronic DIP switch
Electronic potentiometer
Emissions analyzer
Encryption system
Energy management system

F. Flow computer
Frequency synthesizer
Fuel computer

G. Gas analyzer
Gasoline pump

H. Home energy management
Hotel lock

I. Industrial control
Instrumentation

J. Joulemeter

K. Keyboard -softkey

L. Laser machine tool

M. Machine control
Machine process control
Medical imaging
Memory bank selection
Message center control
Mobile telephone
Modem
Motion picture projector

N. Navigation receiver
Network system
Number comparison

O. Oilfield equipment

P. PABX
Patient monitoring
Plasma display driver
Postal scale
Process control
Programmable communications
Protocol converter

Q. Quiescent current meter

R. Radio tuner
Radar dectector
Refinery controller
Repeater
Repertory dialer

S. Secure communications system
Self diagnostic test equipment
Sona-Bouy
Spectral scanner
Spectrum analyzer

T. Telecommunications switching system
Teleconferencing system
Telephone dialing system
T.V. tuner
Terminal
Test equipment
Test system
TouchTone dialers
Traffic signal controller

U. Ultrasound diagnostics
Utility telemetering

V. Video games
Video tape system
Voice/data phone switch

W. Winchester disk controller

X. X-ray machine
Xenon lamp system

Y. YAG—laser controller

Z. Zone/perimeter alarm system

The NM93C46—An Amazing Device

National Semiconductor
Application Note 423
Stacy Deming

Question: What has 8 pins, runs on 5V and can store any one of more than 10^{300} unique bit patterns?

Answer: The NM93C46—a 1024-bit serial EEPROM.

Surprised? It is easy to check:

2^{1024} = number of possible combinations

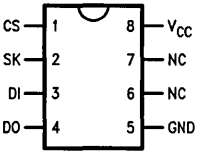
$2^{10} = 10^3$

$2^{1024} \cong (2^{10})^{102} = (10^3)^{102} = 10^{306}$

10^{306} combinations are more than enough for any conceivable security application, serial number, or station I.D. many times over. Although the NM93C46 is a small part both physically and in memory size, its capacity to store unique codes is boundless.

Figure 1 shows the pin assignments and pin names for the NM93C46. Pins 6 and 7 are not connected, leaving only 6 active pins on the device. The DO pin is not active while data is being loaded through the DI pin. DI and DO can be tied together, creating a device that requires a 5-wire interface. This interface may be useful in security applications. The EEPROM could be built into a module that could be used as a "smart key" in electronic security systems. The key would be read whenever it was inserted into a 5-contact keyhole and access would be granted or denied as determined by the stored code. If only 256 bits of the EEPROM were to be used to store the code, this would still provide 10^{77} possible combinations. The remainder of the memory in the key could be used for data collection or to keep a record of where the key had been. It should be noted that ability to write data into the key allows the key to be immediately erased if it is misused.

Dual-In-Line Package



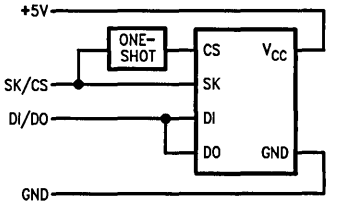
TL/D/8611–1

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Data Input
DO	Data Output
V_{CC}	+5V
GND	Ground
NC	No Connection

FIGURE 1

The 5-contact key is nice, but a 4-contact key is at least 20% better. *Figure 2* shows how the addition of a retriggerable one-shot can achieve this reduction. This circuit puts some timing constraints on the serial clock signal, but these are easily met. The output pulse of the one-shot should remain high for a period that is slightly longer than one serial clock cycle to prevent the NM93C46 from being reset. (The falling edge of CS must occur before the rising edge of the serial clock after the last bit of a write command is transmitted.)

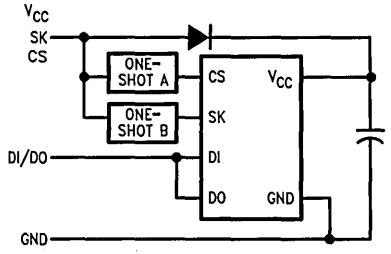


TL/D/8611–2

One-shot is retriggerable MM74HC123

FIGURE 2

A circuit for a 3-contact key is shown in *Figure 3*. A filter capacitor, diode and one-shot have been added. Both one-shots are triggered whenever a pulse to ground occurs on the power supply contact. The capacitor and diode provide power to the NM93C46 and the one-shots during this brief power interruption. An operational amplifier can be used as the power source and can easily generate the required waveform. Both the serial clock and chip select signals are recovered from this waveform.



TL/D/8611–3

One-Shot A—½ MM74HC123

One-Shot B—½ MM74HC123

FIGURE 3

By adding more circuitry to the key, it is possible to achieve a 2-contact interface. A circuit for this interface is shown in *Figure 4*.

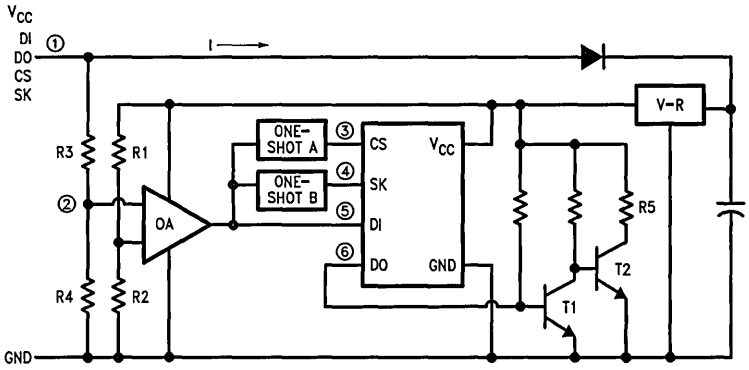
Commands and data are transmitted to the key by superimposing a pulse-width-modulated code on the power supply contact. The voltage swings between 8V and 16V at point 1. A regulated 5V is supplied to the circuits in the key by a local regulator. Resistors R1 and R2 form a divider to create a 3V reference for the operational amplifier. R3 and R4 are used as a divider that converts the 8V to 16V signal at point 1 to a signal at point 2 that swings between 2V and 4V. The output of the operational amplifier now follows the signal at point 1 but swings from 0V to 5V. This signal is used to trigger the one-shots as in the 3-contact circuit, and appears at the DI pin as a pulse-width-modulated signal. Command and data signals may now be entered. Data is read from the key by monitoring the power supply current. When the DO pin is in TRI-STATE® or outputs a one, transistor T2 is turned off. When DO outputs a zero, T2 is turned on and current flows through R5. The value of R5 may be chosen to create whatever current change is needed to detect the state of DO. The current should be tested when the voltage at point 1 is 16V. The resistor in this example will produce a 10 mA change.

Figure 5 shows a typical read sequence for the circuit shown in *Figure 4*.

CONCLUSION

This application note describes a number of circuits that are useful in security and data collection systems. These circuits should be considered only the beginning. It no longer makes sense to install DIP switches to select access codes in garage door openers, cordless and mobile phones, or any other microcontroller-based system. "Smart keys" can be used to gain access to databases and can be invalidated over normal communication lines if they are abused. It boggles the mind to consider what can be done with so many unique codes.

Note: The circuits in this application note feature the NM93C46. The NM93C06 is a pin-compatible part that stores 256 bits. The NM93C46 was used because it has a self-timing write cycle and the NM93C06 does not. Additional circuitry is not required to use the NM93C06, but an additional chip select signal must occur at the CS pin to terminate a write cycle.



TL/D/8611–4

R1 = 20K

R2 = 30K

R3 = 15K

R4 = 5K

One-Shot A = ½ MM74HC123

One-Shot B = ½ MM74HC123

V-R = LM2930Z-5.0

OA = LM358

R5 = 1600Ω

FIGURE 4

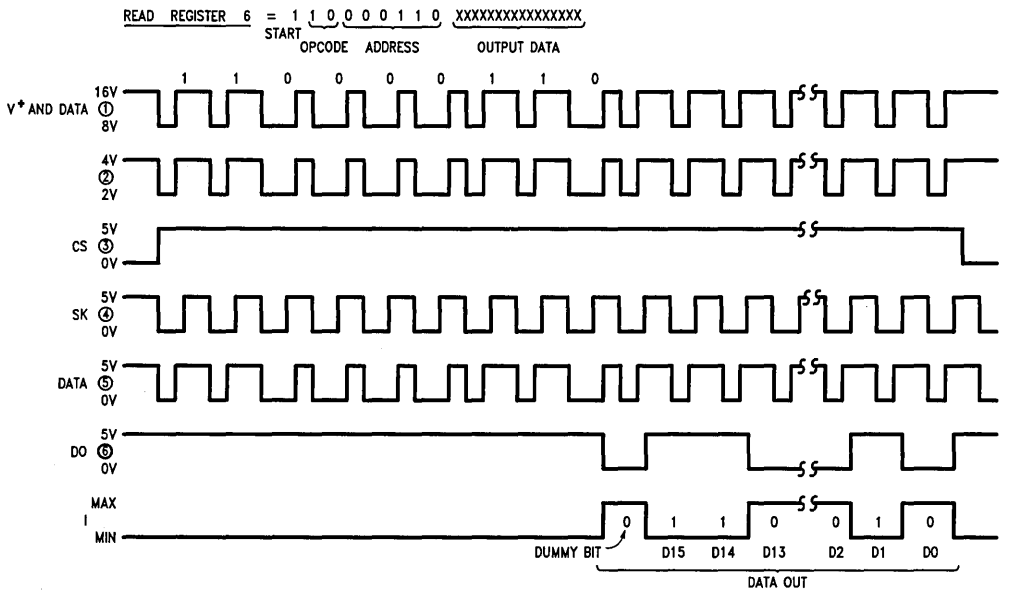

READ REGISTER 6 = 1 1 0 0 0 0 1 1 0 XXXXXXXXXXXXXXX
START
OPCODE
ADDRESS
OUTPUT DATA
1 1 0 0 0 0 1 1 0
V+ AND DATA
16V
8V
4V
2V
CS
5V
0V
SK
DATA
DO
MAX
MIN
0 1 1 0 0 1 0
DUMMY BIT
D15 D14 D13 D2 D1 D0
DATA OUT
TL/D/8611-5

FIGURE 5

Using the NM93CSxx Family

National Semiconductor
Application Note 507

INTRODUCTION

This application note is intended for system designers interested in using the NM93CSxx family of CMOS serial EEPROM devices. These devices are well-suited for applications that call for non-volatile, writeable memory. The NM93CSxx devices offer the additional benefit of selective write-protection by use of an on-chip protect register. This allows the device to perform both read-only memory (ROM) and EEPROM functions on the same chip.

EEPROMs are useful in a wide variety of applications because of their non-volatile, writeable characteristics. The devices can be used for applications that store configuration values, such as feature telephones, station presets on radios, and PC boards with configuration DIP switches and jumpers. Adaptive, closed-loop systems, such as environment controllers and motor controllers, can use EEPROMs to store loop control variables. Data logging is another of the many application areas of EEPROMS.

The NM93CSxx family can support a new set of applications because of their additional capability to perform selective ROM functions. ROM is a requirement when the integrity of data stored in a device must be guaranteed. Applications can make use of this feature while at the same time allocating other locations in the device to operate as EEPROM.

The NM93CSxx family devices exhibit extremely low power consumption due to the low drive requirements of their serial interface and the use of CMOS technology. The serial interface also provides the designer with a flexible interface mechanism allowing the devices to be easily designed into microcontroller and microprocessor systems. In microcontroller systems, or those with a serial bus, the devices can be connected with little or no support logic. The serial interface allows the device to fit in a smaller package, resulting in minimal board space requirements.

TABLE I. NM93CSxx Family

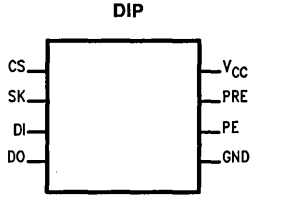
Device	Memory Size
NM93CS06	16 x 16
NM93CS26	32 x 16
NM93CS46	64 x 16
NM93CS56	128 x 16
NM93CS66	256 x 16

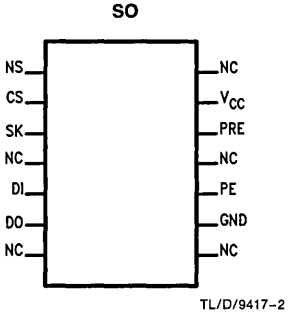
NM93CSxx FAMILY DESCRIPTION

The NM93CSxx family is a set of 5 CMOS serial EEPROM devices with on-chip write-protection logic. The members of the family are differentiated by their memory array size, which ranges from 256 to 4096 bits organized 16 bits wide (see Table I). Because the devices use a serial interface, the pinout for each family member is identical. The devices conform to the MICROWIRE interface and are backwards compatible with previous National serial EEPROM devices (see *Figure 1*).

A set of 10 instructions are provided to control device operation. The general format of the instructions is a start bit (logic 1) followed by opcode, register address and data fields. The register address for the NM93CS06/26/46 is 6 bits, while the register address for the NM93CS56/66 is 8 bits. Data is shifted into the device on the D1 pin, and out on the DO pin following a low to high transition of SK. CS must be high to access the device (see Table 2).

A read operation is performed by issuing the start bit, the appropriate opcode (10), and the desired register address. The device responds by shifting out a dummy bit (logic 0) followed by the data in the selected register. The device will continue to shift data from subsequent registers as long as SK is active (non-volatile shift register mode). Write operations are performed by issuing the start bit, opcode (01), register address, and 16 bits of data. CS must be brought low to initiate the self-timed programming cycle, which includes an automatic erase cycle. CS can then be brought high to monitor DO (low to high transition) for completion of the cycle.





Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial In
DO	Serial Out
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

FIGURE 1. NMC93CSxx Device Pinout

TABLE II. NM93CSxx Instruction Set

Instruction	SB	Op Code	Address	Data	PRE	PR	Comments
READ	1	10	A_X–A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_X–A_0	D15–D0	0	1	Write register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Write all register. Valid only when "protect register" is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in "protect register".
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A_X–A_0		1	1	Programs address into "protect register". Thereafter, memory address < the address in "protect register" are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the "protect register" cannot be altered.

The protect register is used to write protect a segment of registers. The value contained in the protect register designates the first address of the protected segment. All subsequent register locations are write-protected.

USING THE PROTECT REGISTER

The incorporation of the protect register in NM93CSxx devices sets the family apart from other CMOS serial EEPROMs. Including a protect register allows the devices to function as EEPROM and ROM simultaneously. The distribution of EEPROM and ROM in a device is determined by the value in the protect register. The distribution of EEPROM and ROM can be changed in the system by changing the protect register value.

ROM applications typically require that data storage be non-volatile so that no changes will occur when power is turned off and read-only so that changes won't occur under any other circumstances. EEPROMs are non-volatile, but aren't read-only. An EEPROM will function as a ROM if write operations are never attempted or if any attempted write fails.

The protect register is valuable when an application requires a mix of EEPROM and ROM. A NM93CSxx device can be made less susceptible to write problems without using the protect register. The entire device may be made read-only by grounding PE. System software can be implemented to avoid writing to read-only locations and limit when write instructions may be performed by making use of the write enable (WEN) and disable (WDS) instructions. The device would only be susceptible to a write problem if a system failure caused an illegal write or some external source with access to the device abused its write privileges. Use of the protect register under system control would be somewhat safer, but the device would still be subject to the above-mentioned problems. Write access to the protect register must be inhibited for the protected locations to be truly read-only.

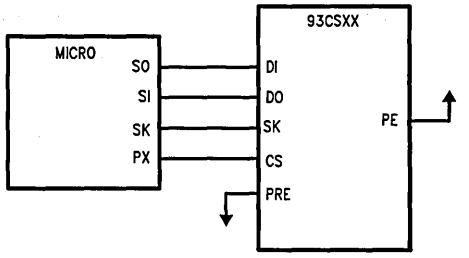


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FIGURE 2a. Protect Register Disabled

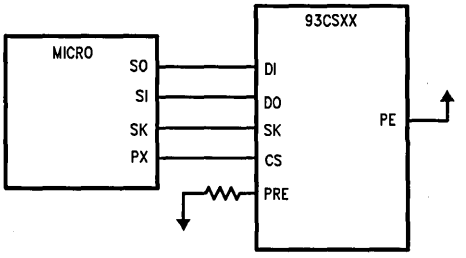

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FIGURE 2b. Protect Register Enabled with Pulldown

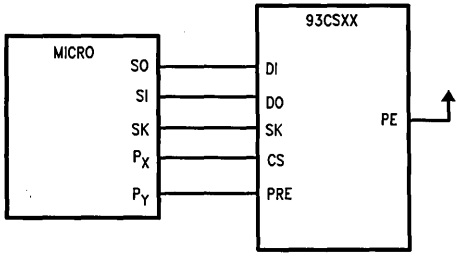

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FIGURE 2c. Protect Register Enabled

ROM devices are most often programmed with data before insertion into a PC board. This approach is applicable to NM93CSxx devices. In a microcontroller system, program code or data could be off-loaded from the internal ROM of the microcontroller into a ROM section in an NM93CSxx device. An EEPROM section could be allocated for any writeable data, such as configuration data values. ROM is desirable in this application because any spurious writes that could corrupt the program will be prevented, a smaller internal microcontroller ROM is possible and if ROM code or data needed alteration, it would be much easier and cheaper to reprogram a NM93CSxx device than the internal ROM of the microcontroller. In manufacturing, the ROM data and the protect register value would be programmed into the device, and the protect register enabled before PC board insertion. The PRE pin would be tied low on the board to prevent write access to the protect register (see *Figure 2a*).

Another application for these devices is in systems that support automated production. Production information, such as date codes and status, would be programmed into the NM93CSxx on a board as it progressed through each step of the production process. Board identification (serial number) and fixed configuration information could also be programmed into the device as a last step. The PRE pin would be pulled low with a resistor to allow production test equipment to drive it high to write data into the device and set the protect register, but prevent any writes to the protected locations during normal operations. The EEPROM section could be used to allow the application to support automated system configuration. Once all boards are placed in the system, any system configuration dependent variables could be programmed (see *Figure 2b*).

In data logging applications, the protect register is programmed as the data is gathered to reduce the likelihood of modification. When the protect register is accessed regularly by the software, PRE must be accorded an interface line, usually a port pin that is controlled by software. The protect register disable (PRDS) instruction must be used upon completion of logging to fully protect the data. PRDS will prevent any further writing to the protect register, even if the device is removed from the board. Extreme care should be exercised when considering use of PRDS. Data should be written into the device from high locations to low to protect the data as it is read in. In addition, the protect register then serves the dual purpose of being a pointer to the last location written, simplifying software and saving a variable location (see *Figure 2c*).

INTERFACING TO THE NM93CSxx FAMILY

COP800 Interface

The COP800 family is a set of 8-bit CMOS microcontrollers. The family members differ by program and data memory, on-chip peripherals, and package size. Some members have on-chip EEPROM for program or data memory. The devices with EEPROM for program memory are only intended for development purposes. All members of the family have an on-chip MICROWIRE™ interface.

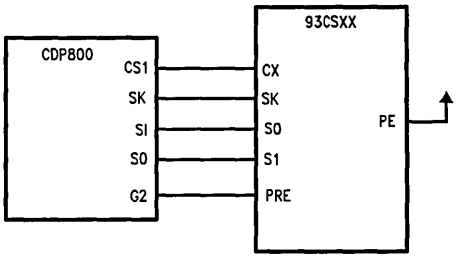

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FIGURE 3. MICROWIRE Interface

The COP800 family provides three options when interfacing to a NM93CSxx device. The interface could be designed by using the COP800 device parallel port pins under software control, on-chip UART if available, or the MICROWIRE interface port. The most attractive option for the interface is the MICROWIRE because NM93CSxx devices connect directly to it.

The MICROWIRE port provides a serial clock (SK), serial input (SI), and serial output (SO). These lines are directly connected to SK, DO and DI of the EEPROM. COP800 parallel port pins can be used for providing CS, PE and PRE. If PE or PRE are static in the application, they can be tied low or high. No other hardware is required for the interface (see *Figure 3*). In a system with multiple devices on the MICROWIRE, additional logic may be required to perform chip selection. If available, parallel port pins could be used for additional chip selects. Otherwise, a PAL device could be designed so that chip selects are set serially preceding any serial device operations.

```
;WREEPROM-WRITE DATA TO EEPROM
;
;THIS ROUTINE WILL WRITE A SPECIFIED NUMBER OF BYTES
;TO THE EEPROM USING THE MICROWIRE INTERFACE. THIS CODE
;ASSUMES THE SHIFT CLOCK RATE IS 1/2 THE XTAL FREQUENCY.
;THE ARGUMENT STRING CONSISTS OF A BYTE COUNT, OPCODE,
;REGISTER ADDRESS, FOLLOWED BY A DATA STREAM.
;
WREEPROM:  LD    A,[B+]   ;COPY BYTE COUNT
           X     A,x'F0   ;
           SBIT  1,x'D4   ;CHIP SELECT
           SBIT  7,x'E9   ;SEND START BIT
           SBIT  2,x'EF   ;
           RBIT  2,x'EF   ;
SLOOP:     LD    A,[B+]   ;SEND DATA BYTES
           X     A,x'E9   ;
           SBIT  2,x'EF   ;
BIT_TST:   IFBIT 2,x'EF   ;STILL BUSY?
           JMP   BIT_TST  ;
           DRSZ  x'F0     ;DONE SENDING?
           JMP   SLOOP    ;
           RBIT  1,x'D4   ;DROP CS
           RET
```

FIGURE 4. COP800 MICROWIRE Write Routine

```
;RDEEPROM-READ DATA FROM EEPROM
;
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE MICROWIRE. THE CODE ASSUMES THAT THE
;SHIFT CLOCK IS PROGRAMMED AT 1/2 THE INSTRUCTION CLOCK RATE.
;THE ARGUMENTS PASSED TO THIS ROUTINE ARE A BYTE COUNT, OPCODE,
;AND REGISTER ADDRESS, POINTED TO BY B.
;THE BYTE COUNT AND DATA READ ARE POINTED AT BY B ON RETURN.
;
RDEEPROM:  LD     A,x'FE      ;SAVE POINTER
           X      A,x'F1      ;
           LD     A,[B+]      ;COPY BYTE COUNT
           X      A,x'F0      ;
           SBIT   1,x'D4      ;CHIP SELECT
           SBIT   7,x'E9      ;SEND START BIT
           SBIT   2,x'EF      ;
           RBIT   2,x'EF      ;
           LD     A,[B]       ;SEND INSTRUCTION
           X      A,x'E9      ;
           SBIT   2,x'EF      ;
TST1:      IFBIT  2,x'EF      ;BUSY?
           JMP    TST1        ;
           SBIT   2,x'EF      ;GET DUMMY BIT?
           RBIT   2,x'EF      ;
RLOOP:     CLRA               ;GET DATA BYTES
           SBIT   2,x'EF      ;
TST2:      IFBIT  2,x'EF      ;BUSY?
           JMP    TST2        ;
           X      A,x'E9      ;
           X      A,[B+]      ;
           DRSZ   x'F0        ;DONE GETTING?
           JMP    RLOOP       ;
           LD     A,x'F1      ;RESTORE POINTER
           X      A,x'FE      ;
           RBIT   1,x'D4      ;DROP CHIP SELECT
           RET
```

FIGURE 5. COP800 MICROWIRE Read Routine

Inside a COP800 device the MICROWIRE hardware consists of an 8-bit shift register (SIO), a control bit (BUSY) in the program status word (PSW), and a control register (CNTRL), BUSY is set by the control program to initiate a shift operation and is automatically reset when eight bits have been shifted. BUSY can be reset by the program for shift operations of less than eight bits. CNTRL is used to set the MICROWIRE mode and rate of SK. SK can be set to a divide by 2, 4, or 8 of the instruction clock rate. The MSEL bit of CNTRL sets the MICROWIRE to Master mode or Slave mode. In Master mode, a device will generate SK and in Slave mode it will receive SK. Master mode is used to interface to an NM93CSxx device.

In addition to initializing the interface, software rountines are required to control data transfers to and from the EEPROM through the MICROWIRE port. The same routines used to read and write to the EEPROM can be used to execute the NM93CSxx instructions, including accessing the protect register. The only extra step required to access the protect register is that PRE must be set high.

A routine must access SIO to perform an NM93CSxx instruction. Since the MICROWIRE shift register is only eight bits wide, multiple accesses are required to complete an instruction. In addition, instructions aren't byte-aligned; routines must align the operation. Instructions can be byte-aligned by sending a single start bit followed by a byte of opcode and address. A start bit can be sent by using the set

bit (SBIT) instruction to set BUSY, followed by the rest bit (RBIT) instruction when SK is being divided by two, or by sending a byte with seven leading zeros as dummy bits and a single one for the start bit. The NMC83CS56/66 devices require two more bits to be sent for alignment because of their larger address space. In this case it is easier to send the byte with leading zeros.

The write routine, WREEPROM, sets CS to select the device, then writes a single start bit, followed by a byte of opcode and address, and two bytes of data. The bytes sent are stored as a string preceeded by a byte-count. The byte count must, obviously, be three for a write. This routine can be used to perform the other write-only NM93CSxx instructions by setting the byte-count and data string appropriately. CS is brought low to initiate the automatic erase/write cycle. The routine doesn't bring CS back high to check for completion of the cycle. This allows the routine to be used to perform the other NM93CSxx instructions and the control program to perform other tasks during the cycle. If the program is unsure of cycle completion, DO should be checked before initiating another instruction (see *Figure 4*).

The read routine, RDEEPROM, sets CS and sends the start bit, opcode and address in the same manner as the write routine. The routine then reads a dummy bit (logic 0) from the EEPROM and the number of bytes of data specified by the byte-count. The dummy bit is read in exactly the same way as a start bit is sent (see *Figure 5*).

HPC Interface

The HPC family is a set of high performance 16-bit microcontrollers. Like the COPS microcontrollers, the HPC devices are MICROWIRE compatible, providing an excellent means of interfacing to NM93CSxx devices. Though, a software controlled interface using parallel port pins could be used, as well as an on-chip UART.

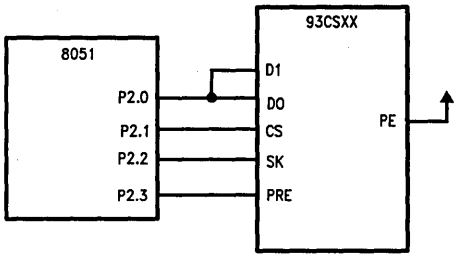

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FIGURE 7. 8051 Interface

```
#define    SET_CS    *_iporta|=0x40     /* set chip select*/
#define    DROP_CS   *_iporta & = 0xFB /* lower chip select*/
#define    SIO       0xD6              /* SIO register location*/
#define    PORTA     0xC8              /* PORT A location*/
#define    IRPD      0xD2              /* IRPD register location*/
#define    NOT_DONE I(*_Irpd & 0x04)   /* DONE flag set if true*/
#define    BFUN      0xF4              /* BFUN register*/
#define    SK                          \
           *_bfun & = 0xBF             \
           *_bfun | = 0x40;
#define    WR_EE (bytes, data)         \
{          int i;                      \
                                       \
           SK;                         \
           for(I=0; I < bytes; I++)\
           {                           \
            *_sio = *data++;           \
            while(NOT_DONE);           \
            *_irpd & = 0xFB;           \
           }                           \
}
/* Global Definitions*/
char       *_sio = SIO;
char       *_iporta = PORTA;
char       *_irpd = IRPD;
char       *_bufn = BFUN;

wr_eeprom(bytes,data)
int        bytes;   /* byte count*/
char       *data;   /* data buffer*/
{
           SET_CS;
           WR_EE;
           DROP_CS;
}

rd_eeprom(bytes, data)
int        bytes;   /* byte count*/
char       *data;   /* buffer pointer*/
{
           SET_CS;
           WR_EE (1, data);
           SK;                         /* get dummy bit*/
           for (i = 0; i < bytes; I ++){
             *data ++ = *_sio;
             while(NOT_DONE);
             *_irpd & = 0xFB;
           }
           DROP_CS;
}
```

FIGURE 6. HPC C Language Interface Routine

```
;
;SNDBYT - SHIFTS 8 BITS OF DATA TO EEPROM
;
;THIS ROUTINE SHIFTS A BYTE POINTED AT BY R0
;ASSUMES CHIP SELECT ALREADY ACTIVE (HIGH)
;
SNDBYT    MOV   B,#8     ;LOAD SHIFT COUNT
          MOV   A,@R0    ;GET BYTE
S_LOOP:   RLC   A        ;SHIFT
          MOV   P2.0,C   ;SEND BIT
          CLR   P2.2     ;SK
          SETB  P2.2     ;
          DJNZ  B,S_LOOP;DONE?
          RET
;
;WREEPROM - WRITE DATA TO EEPROM
;
;THIS ROUTINE WRITES A SPECIFIED NUMBER OF BYTES TO THE
;EEPROM USING SNDBYT UTILITY ROUTINE. THE DATA IS POINTED AT
;BY THE R0 REGISTER AND CONSISTS OF BYTE COUNT, OPCODE/REG ADDR
;AND DATA BYTES. DO IS SET HIGH TO AVOID CONTENTION.
;
WREEPROM: MOV   R2,@R0    ;COPY BYTE COUNT
          INC   R0        ;
          SETB  P2.1      ;CHIP SELECT
          CLR   P2.2      ;START BIT
          SETB  P2.2      ;
WR_LOOP:  LCALL SNDBYT    ;WRITE DATA BYTES
          INC   R0        ;
          DJNZ  R2,WR_LOOP;
          SETB  P2.0      ;DEFAULT DO HIGH
          CLR   P.21      ;DESELECT/PROGRAM
          RET
```

FIGURE 8. 8051 Parallel Port Pin Interface—Write Routines

The MICROWIRE interface provides signals for SK, SI and SO. CS, PE and PRE signals can be provided by using parallel port pins. Port A on the HPC is allocated for general use and is ideal for this function. When used in Master mode, the clock rate for the MICROWIRE is set by programming the appropriate value into the DIVBY register. The 8-bit SIO register is used as a buffer for serial operations.

Unlike the COP800 microcontrollers, the HPC does not use a BUSY bit to control shifting. The DONE flag in the IRPD register is polled to determine completion of a shift operation. A single bit can be transferred by changing the mode of the SK pin back to a general purpose port pin (B.6). This is accomplished by clearing bit six of the port B function register (BFUN). If port B bit six is high, the pin will go high immediately clocking the EEPROM.

```
;RCVBYT - READ A BYTE OF SERIAL DATA
;
;THIS ROUTINE WILL SERIALLY READ 8 BITS OF DATA FROM THE PORT PIN
;AND STORE THE DATA IN THE LOCATION POINTED AT BY R0
;
RCVBYT:    MOV   B,#8       ;LOAD SHIFT COUNT
R_LOOP:    CLR   P2.2       ;SK
           SETB  P2.2       ;
           MOV   C,P2.0     ;GET BIT
           RLC   A          ;SHIFT
           DJNZ  B,R_LOOP   ;DONE?
           MOV   @R0,A      ;STORE DATA
           RET
;RDEEPROM - READ DATA FROM EEPROM
;
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE RCVBYT ROUTINE. INPUT ARGUMENT STRING IS
;A BYTE COUNT, AND OPCODE/REGISTER ADDRESS. ON RETURN, R0 POINTS
;TO A STRING CONTAINING THE BYTE COUNT FOLLOWED BY DATA BYTES
;
RDEEPROM:  MOV   R2,@R0     ;COPY BYTE COUNT
           PUSH  R0         ;SAVE POINTER
           INC   R0         ;
           SETB  P2.1       ;CHIP SELECT
           CLR   P2.2       ;START BIT
           SETB  P2.2       ;
           LCALL SNDBYT     ;SEND INSTRUCTION
           SETB  P2.0       ;DEFAULT DO HIGH
           CLR   P2.2       ;DUMMY BIT
           SETB  P2.2       ;
RD_LOOP    LCALL RCVBYT     ;GET DATA BYTES
           INC   R0         ;
           DJNZ  R2,RD_LOOP;DONE?
           POP   R0         ;RESTORE POINTER
           CLR   P2.1       ;DESELECT
           RET
```

FIGURE 9. 8051 Parallel Port Pin Interface Read Routines

The HPC supports program development in the C language. The software routines to support an HPC interface are similar to those for the COP800, except that they are written in C (see *Figure 6*). The main difference is how the start bit and dummy read bit are handled. Since the HPC supports the C language, core routines are written utilizing macros, eliminating the overhead of an extra level of subroutine calls.

8051 Interface

The 8051 offers two interface alternatives for the NM93CSxx family; the first uses parallel port pins under software control and the second is based on using the on-chip serial port. Both interfaces require a minimum number of device pins and no support logic. The main differences are that the serial port is faster and requires less software.

The first choice for discussion is the use of the port pins. The 8051 has four 8-bit bidirectional I/O ports. The ports are accessed through a special function register. The port registers are bit addressable which facilitates their use in this application. The minimum interface requires the use of only three port pins. A pin for CS, SK, and one connected to both DI and DO (see *Figure 7*). A two wire interface is possible by tying CS active, but this leaves the device in the active (high power) state and prevents the device programming cycle from being executed.

It is not necessary to have separate lines for DI and DO because DO is placed in a high-Z condition during write operations. During a read operation the DI pin is driven to send the instruction to the EEPROM and DO outputs the dummy bit (0) and data. To prevent contention DI has to stop driving a high before DO can output the dummy bit. The 8051 doesn't drive a high, it uses internal pull-ups to obtain a high, so there is no contention problem. This may be a con-

cern in other designs. The DO pin is driven when CS is brought high following a write operation to time completion of programming Contention will occur on the operation following a write if programming completion isn't checked. A dummy check can be used.

When using the port pins, one must consider that some of the port pins have alternate functions. For example, Port 3 pins 0 and 1 are also allocated for the serial port. Similarly, if the program being executed on the 8051 resides in external memory, then Ports 0 and 2 will serve as the system bus during external memory access.

The software support routines are primarily concerned with controlling the flow of data to/from the EEPROM. Because the 8051 is an 8-bit machine, two utility routines, SNDBYT and RCVBYT, are used to shift a byte of data to and from the NM93CSxx.

The write routine, WREEPROM, raises CS to access the device, shifts out a start bit, then calls SNDBYT to shift out the opcode/register address byte, and other data bytes, as specified by the byte-count (see *Figure 8*).

The read routine, RDEEPROM, starts out by raising CS, sending a start bit, and using SNDBYT for the opcode/register address byte. The dummy bit is then shifted from the device and RCVBYT is called to shift in the number of bytes of data specified by the byte-count (see *Figure 9*).

```
;RDEEPROM - READS DATA FROM NMC93CSXX DEVICE
;
;THE ROUTINE READS A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE SERIAL PORT. R0 POINTS TO AN ARGUMENT STRING
;CONTAINING THE BYTE COUNT AND THE OPCODE/REGISTER BYTE
;A STRING IS RETURNED CONTAINING THE BYTE COUNT FOLLOWED BY DATA.

RDEEPROM:
            PUSH   R0        ;SAVE POINTER
            MOV    R2,@R0    ;COPY BYTE COUNT
            INC    R0        ;
            SETB   P2.1      ;CHIP SELECT
            CLR    P3.1      ;SEND START BIT
            SETB   P3.1      ;
            MOV    SBUF      ;SEND INSTRUCTION
            JBC    TI$       ;DONE?
            CLR    TI        ;
            CLR    P3.1      ;GET DUMMY BIT
            SETB   P3.1      ;
            SETB   REN       ;GET DATA BYTES
RLOOP;      JBC    RI,$      ;DONE?
            CLR    RI        ;
            MOV    @R0,SBUF  ;
            INC    R0        ;
            DJNZ   R2,RLOOP  ;
            CLR    REN       ;
            CLR    P2.1      ;DESELECT
            POP    R0        ;RESTORE POINTER
            RET

;WREEPROM - WRITE DATA TO EEPROM
;
;THE ROUTINE WRITES A SPECIFIED NUMBER OF BYTES TO EEPROM
;POINTED AT BY R0. ARGUMENTS INCLUDE BYTE COUNT AND OPCODE/ADDRESS
;
WREEPROM:   MOV    R2,@R0    ;COPY BYTE COUNT
            INC    R0        ;
            SETB   P2.1      ;CHIP SELECT
            SETB   P3.0      ;START BIT
            CLR    P3.1      ;
            SETB   P3.1      ;
SLOOP:      MOV    SBUF,@R0  ;SEND DATA BYTES
            INC    R0        ;
            JBC    TI,$      ;DONE?
            DJNZ   R2,SLOOP  ;
            CLR    P2.1      ;DESELECT
            RET
```

FIGURE 10. 8051 Serial Port Read and Write Routines

8051 INTERFACE—SERIAL PORT

The 8051 serial port operates in one of four modes: 8-bit shift register, 8-bit UART and two different 9 bit UART modes. The 8-bit shift register mode (Mode 0) is preferred because it operates with no protocol, as opposed to the UART modes which send and receive packeted data. When in Mode 0, the 8051 RxD pin is used as a serial in/out pin and the shift clock is provided on the TxD pin. The TxD pin would be connected to SK and RxD would be connected to DI and DO on the NM93CSxx device. CS, PE and PRE would be connected the same way as in the port pin interface.

When using the serial port in Mode 0, the serial port control register (SCON) must be programmed by setting the SM0 and SM1 bits (bits 7 and 6) to 0. The serial clock runs at a fixed rate of $1/_{12}$ of the oscillator frequency. The maximum frequency for the serial clock on NM93CSxx devices is 1 MHz. This means the 8051 can run with an oscillator frequency up to 12 MHz. After every eighth bit is received or transmitted the 8051 hardware will set either the receive interrupt (RI) or transmit interrupt (TI) bit in SCON. These bits may be polled, or used to generate interrupts.

The software routines for the serial port interface are virtually the same as those for the previous example. The only differences are that the 8051 serial port performs the same functions as the SNDBYT and RCVBYT routines. Instead of calling these routines, the REN bit is enabled to initiate reception and the data is read from the serial buffer (SBUF). For writing, the data is written into SBUF to perform the transfer. The routines poll the RI or TI bits. Because data transactions are synchronous, interrupts are not applicable (see *Figure 10*).

8096 INTERFACE

The 8096 is a 16-bit microcontroller. Like other microcontrollers, it interfaces easily to the NM93CSxx devices. The use of parallel port pins or the on-chip serial port provide two interface options.

When implementing the parallel port pin interface, the choice of the port pins used is more critical because more of these pins have alternate functions. If the 8096 must perform external memory accesses, the use of Ports 3 and 4 becomes a problem because these two 8-bit ports make up the address/data bus. Port 0 pins are used for the analog input channels. Port 2 pins have alternate functions such as the serial port. Port 1 pins do not have alternate functions and may be preferred for use.

The 8096 provides an on-chip serial port which may be used for interfacing the NM93CSxx devices. The serial port has 4 modes of operation. The mode of interest for this application is the shift register mode (Mode 0). The 8096 shift register mode serial clock rate is not a fixed rate. It is therefore the responsibility of the support software to program the baud rate appropriately.

INTERFACING NM93CSxx WITH HIGH PERFORMANCE MICROPROCESSORS

High performance microprocessors like the NS32000, iAPX386 and the MC680x0 are usually implemented as central processor in computers and aren't directly involved with peripheral devices. Rather, these machines communicate over a backplane bus. These processors are designed for high speed, parallel data transfers. The NM93CSxx devices could be used with these processors if a serial bus is implemented as part of the backplane bus. Typically, a serial bus would be used for system configuration or diagnostic purposes. Both the VME bus and Multibus II supply serial communication signals that may be used to interface NM93CSxx devices to a high performance processor.

SUMMARY

The NM93CSxx family can be used in a wide variety of applications. The devices provide a non-volatile, writeable memory that requires the least amount of board space, support logic and power. The protect register allows for a flexible mix of RAM and ROM. The previous examples illustrate that the NM93CSxx family easily interfaces to microcontrollers and systems with a serial bus.

```
;RCYBYT - READ UTILITY ROUTINE
;
;THIS ROUTINE WILL READ 8 BITS OF DATA FROM THE SERIAL PORT
;THE DATA IS STORED IN THE LOCATION POINTED AT BY THE DX REGISTER.
;
RCVBYT:    LDB   AH,#8        ;LOAD SHIFT COUNT
BOP_SK:    ANDB  P2,#FBH      ;STROBE SK
           ORB   P2,#04H      ;
           JBS   P2,3,BIT_1   ;READ BIT
           ANDB  AL,#FEH      ;
           SJMP  R_SHIFT      ;
BIT_1:     ORB   AL,#01H      ;
R_SHIFT:   SHLB  AL,1         ;
           DECB  AH           ;DONE?
           JNE   BOP_SK       ;
           LDB   (DX),AL      ;SAVE DATA
           RET

;RDEEPROM - READ DATA FROM EEPROM
;
;SI, SK, CS, SO = P2[3 . . . 0]
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM THE
;EEPROM AND STORE THE DATA. ARGUMENTS SUPPLIED TO THIS ROUTINE
;ARE A BYTE COUNT, OPCODE/REGISTER ADDRESS, AND ADDRESS FOR
;STORING THE DATA.
;
RDEEPROM:  PUSH  DX           ;SAVE POINTER
           LDB   BL,(DX)+     ;COPY BYTE COUNT
           ANDB  P2,#F0H      ;CHIP SELECT,START BIT
           ORB   P2,#03       ;
           ORB   P2,#04       ;
           LCALL SNDBYT       ;SEND INSTRUCTION
           ANDB  P2,#FBH      ;GET DUMMY BIT
           ORB   P2, #04H     ;
RD_LOOP:   LCALL RCVBYT       ;GET DATA BYTES
           INC   DX           ;
           DECB  BL           ;DONE?
           JNE   RD_LOOP      ;
           ANDB  P2,#FDH      ;DESELECT
           POP   DX           ;RESTORE POINTER
           RET
```

FIGURE 11. 8096 Port Pin Interface Read Routines

```
;SNDBYT - WRITE 8 BITS OF DATA TO PORT PIN
;
;THIS ROUTINE WILL WRITE 8 BITS OF DATA TO THE PORT PIN. THE
;DATA BYTE IS POINTED AT BY THE DX REGISTER.
;
SNDBYT:    LDB   AH,#8        ;LOAD SHIFT COUNT
           LDB   AL,(DX)      ;GET DATA BYTE
SLOOP:     JBS   AL,7,BIT_1   ;SEND BIT
           ANDB  P2,#FEH      ;
           SJMP  TOG_SK       ;
BIT1:      ORB   P2,#01H      ;
TOG_SK:    ANDB  P2,#FBH      ;
           ORB   P2,#04H      ;
           SHLB  AL           ;
           DECB  AH           ;DONE?
           JNE   SLOOP
           RET

;WREEPROM - WRITE DATA TO EEPROM
;
;SI, SK, CS, SO = P2[3..0]
;THIS ROUTINE WILL WRITE A SPECIFIED AMOUNT OF BYTES TO THE
;EEPROM. THE DATA TO BE WRITTEN IS POINTED AT BY THE DX REGISTER.
;THE ARGUMENTS INCLUDE THE BYTE COUNT, OPCODE/REGISTER ADDRESS,
;AND 1 OR MORE DATA BYTES.
;
WREEPROM:  LDB   BL,(DX)+     ;COPY BYTE COUNT
           ANDB  P2,#F0H      ;CHIP SELECT, START BIT
           ORB   P2,#03H      ;
           ORB   P2,#04H      ;
WR_LOOP:   LCALL SNDBYT       ;SEND DATA BYTES
           INC   DX           ;
           DECB  BL           ;DONE?
           JNE   WR_LOOP      ;
WR_EXIT:   ANDB  P2#FDH       ;DESELECT/PROGRAM
           RET
```

FIGURE 12. 8096 Parallel Port Pin Interface Write Routines

Using the NM93CS EEPROM Family Features

National Semiconductor
Application Note 716
Paul Lubeck

The NM93CS Family consists of four members as shown in Table I. Each of these members is available in a variety of temperature ranges, operating voltage ranges, and packaging options. These EEPROMs are a superset of the industry standard NM93C Family. The differentiating features of the NM93CS Family are the Sequential Register Read and the Memory Protect Register. The purpose of this application note is to more fully describe these features.

TABLE I. NM93CS Family Members

Part Number	Memory Size	Internal Organization
NM93CS06	256-bit	16 x 16
NM93CS46	1024-bit	64 x 16
NM93CS56	2048-bit	128 x 16
NM93CS66	4096-bit	256 x 16

SEQUENTIAL REGISTER READ

This read mode is entered the same way as the standard word read. First a start bit is transmitted, followed by the op code for a read cycle and then the first address to be read. It is always necessary to define the first address to be read since the address register's state is not guaranteed.

Up until this point, the data out (DO) will remain in TRI-STATE®, but beginning with the same rising edge of the clock (SK) that clocks in address bit A0, the data out will drive a low level. This first bit is always a zero. Starting with the next clock, valid data will appear on the data out pin. The leading zero in the data field will only appear in the first word read in a sequential read sequence, all subsequent data words will be clocked out on the data out pin in an uninterrupted stream. Refer to Figure 1 for the timing sequence.

Any number of data words may be read with a single sequential read instruction. When the top of memory is reached it will automatically wrap around to address 0 and continue in the sequential read mode. Using this feature it would be possible to read the entire memory in an endless loop if desired.

The Memory Protect Register has no effect on Sequential Read. The Sequential Read will cross the write protection boundary and read to the top of the memory and cycle back to address 0 (possibly in the unprotected field) regardless of the Protect Register status.

To terminate a sequential read operation, the host must drop chip select (low). At any time CS is transitioned to a low, the current instruction will be terminated. It is not necessary to observe word boundaries when terminating a read or sequential read operation. It may be terminated at any time without affect on the EEPROM.

MEMORY PROTECT REGISTER

The protect register is a unique method of write protecting the contents of a variable number of memory registers. The basic concept is shown in Figure 2 using the NM93CS66 4096-bit EEPROM. For the other family members everything remains the same except the memory size and the corresponding maximum address that can be set in the protect register. One other difference that needs to be noted is the address length for the NM93CS06 and NM93CS46 is 6 bits and for the NM93CS56 and NM93CS66, 8 bits. The difference in address length produces a corresponding difference in length of the protect register.

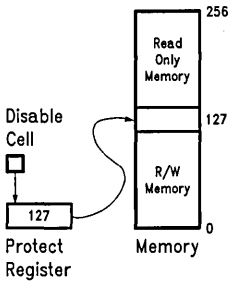

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FIGURE 2. Memory Protect Register

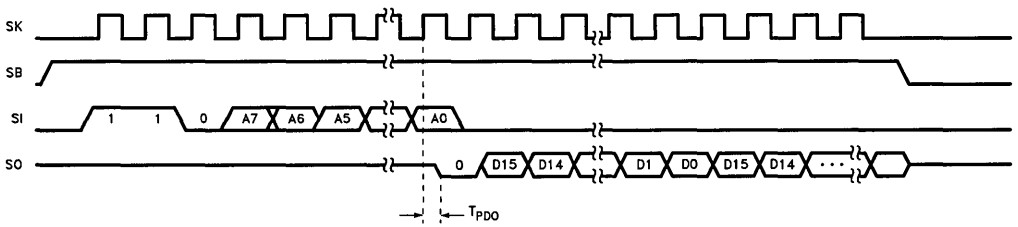

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FIGURE 1. Sequential Read Instruction Sequence

There are two basic elements to the protection scheme, the Protect Register and the Disable Cell. Both the Protect Register and the Disable Cell are implemented in EEPROM latches, therefore do not require the introduction of additional technologies onto the die. The purpose of the Protect Register is to contain the address of the first write protected location in memory. The location in memory defined by the address written into the protect register and all others above that location, to the maximum address in memory are write protected.

The Protect Register is writable from the serial bus in a manner similar to writing a memory register, the only difference being the input PRE (Protect Register Enable) must be high and the instruction immediately preceding the write to the protect register must be a Protect Register Enable (PREN) instruction. By requiring this specific sequence and set of conditions, both hardware and software oriented, the chances of inadvertently changing the contents of the protect register or an unauthorized user changing the data without specific knowledge of the operation of the EEPROM are very remote.

The Disable Cell is a single EEPROM latch that may be set via a Protect Register Disable (PRDS) instruction. Like the Protect Register Write (PRWRITE) instruction, it must be executed with the input PRE high and immediately preceded by a PREN instruction. Once the Disable Cell is written, it cannot be cleared because the PRDS instruction is a one time only instruction. Once the PRDS instruction has been executed, the Protect Register cannot be updated again in the life of the part and the defined portion of memory is permanently protected.

A typical instruction sequence for storing manufacturing and factory calibration information in a NM93CS family part is shown as follows:

Instruction	Description
1.	Power On
2. WEN	Enable all programming instructions.
3. WRITE A(max)	Write maximum address location.
4. WRITE A(max-1)	Write maximum address location -1.
5. WRITE A(max-2)	Write max. address location -2.
:	:
:	:
:	:
6. WRITE A(max-y)	Write maximum address location -y.
7. PREN	Enable programming of Protect Register.
8. PRWRITE (A(max-y))	Write address (max-y) to Protect Register.
9. PREN	Enable programming of the Disable Cell.
10. PRDS	Disable all future programming of the protect register and protected memory.
11. WDS	Disable all programming instructions.

It is not necessary to do steps 9 and 10. The PRDS instruction makes the protection permanent. Without executing the PRDS instruction the option remains to remove the write protection thus allowing changing the data in the formerly protected portion of memory. The following sequence will remove the write protection and clear the contents of the Protect Register:

Instruction	Description
1. WEN	Enable all programming instruction.
2. PREN	Enable programming of the Protect Register.
3. PRCLEAR	Enable writing of all memory locations and clear the Protect Register.
4. WDS	Disable all programming instruction.

In both examples above the final step is a Write Disable (WDS) instruction. This instruction would normally be delayed until all programming is complete, but should be included as a minimal level of data protection for otherwise unprotected memory locations.

Using National's NMC87C257 256K EPROM with On-Chip Latches

National Semiconductor
Application Note 731
Sean Pitonak

INTRODUCTION

The standard EPROM available from most manufacturers limits the on-chip circuitry to just the minimum needed to operate the EPROM and the minimum of user interface handles. Users of standard EPROMs are forced to include latches in their design to interface with most microcontrollers and microprocessors.

Probably one of the most desirable user-interface features is the ability to directly interface the EPROM to a host device that has a multiplexed address and data port. This type of interface is present on many microcontrollers and microprocessors such as the HPC, 80C51 and many of the Intel and Motorola microcontrollers. National is now manufacturing an EPROM that can directly interface with a host device—the NMC87C257.

NATIONAL'S NMC87C257 SOLUTION

The NMC87C257 is pin-compatible with the standard 27C256 (1 Megabit EPROM, organized as 128K x 8 bits), shown in *Figure 1*. In fact, the NMC87C257 can be directly substituted into the many existing 27C256 sockets when used in the unlatched mode. The internal latches are transparent and the Address Latch Enable (ALE) is on a shared pin with V_{PP}. By tying V_{PP} to V_{CC}, the NMC87C257 behaves exactly like the 27C256. The NMC87C257 is available in both quartz-windowed Ceramic DIP and Plastic LCC packages as is the 27C256.

National's latched EPROM is useful because the same ALE used for the 74F373 latch can be tied to the ALE of the NMC87C257, eliminating the need for the 74F373 latch. As shown in *Figure 2*, it is as simple as removing the two octal latches and routing the appropriate bus and control line to the EPROM.

SUMMARY

The NMC87C257 allows the user the combination of familiar functionality, pinout and programmability (due to its compatibility with existing 27C256 EPROMs) and the advantages of saved board space, cost of the octal latches and their insertion and system power consumption. The NMC87C257 gives the system designer the needed flexibility of interfacing directly with microcontrollers and microprocessors that have multiplexed address and data ports.

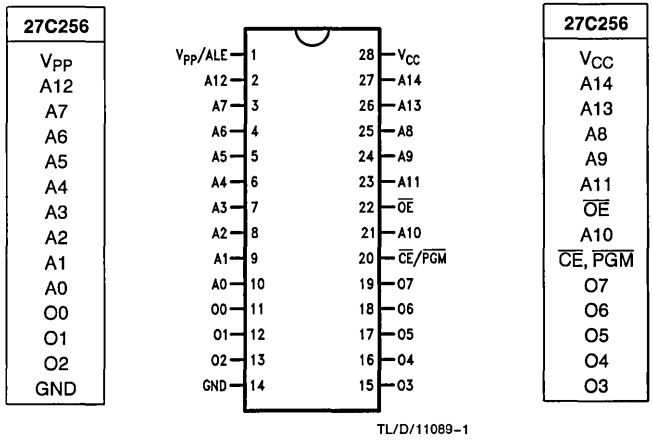

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FIGURE 1. Socket Compatible 27C256 EPROM Pin Configuration is Shown in the Block Adjacent to the NMC87C257 Pins.

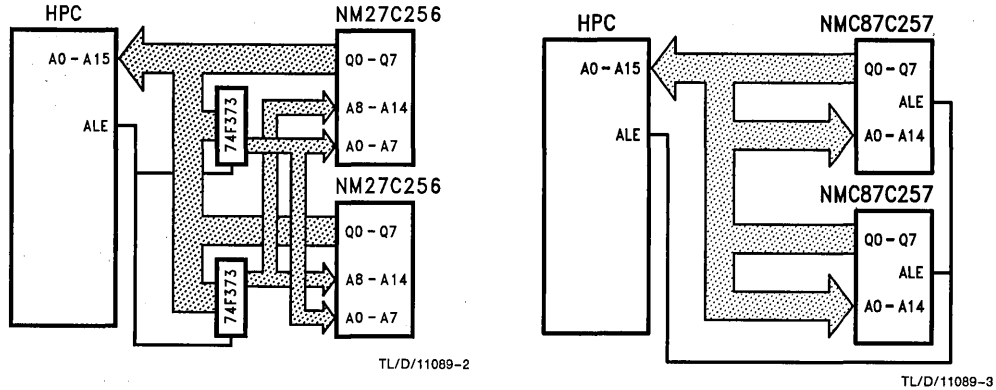

FIGURE 2. A common HPC Microcontroller application using two NM27C256 EPROMs and two 74F373 external latches (left) and the same application using only two NMC87C257 EPROMs with on-chip latches (right).

Understanding National's NM95C12 EEPROM with Programmable Switches

National Semiconductor
Application Note 735
Sean Pitonak

INTRODUCTION

National's NM95C12 is a 1024-bit Serial EEPROM with 8 programmable switches. These outputs can provide logic and analog switch inputs and outputs on a parallel bus, allowing this device to perform functions such as polling via the serial bus, interrupts via the serial bus and converting parallel data onto the serial bus.

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the NM95C12. It consists of a 61-word x 16-bit EEPROM array, a 16-bit Initial Switch Register (ISR), a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and control logic.

Addresses 0–60 of the EEPROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions.

Address 61 is also an EEPROM location, but it is used as the ISR to provide the initial switch configuration information automatically on power-up.

Address 62 is the location of the SCR, which controls the switch logic of the output terminals. This address contains a volatile memory and therefore does not have endurance or programming time limits associated with it, allowing the outputs to be reconfigured an unlimited number of times.

Address 63 contains the SRR. This is a read-only register that reads back the logic levels present on the switch terminals. Only 8-bits of the SRR are used.

The NM95C12 also includes a Sequential Register Read function that allows the user to obtain an endless loop of data by entering the read mode and leaving the CS high.

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals.

Each switch pair can be individually configured to 1 of 14 modes. Therefore both logic and analog switches can be implemented simultaneously.

The logic switch configurations are at standard TTL levels.

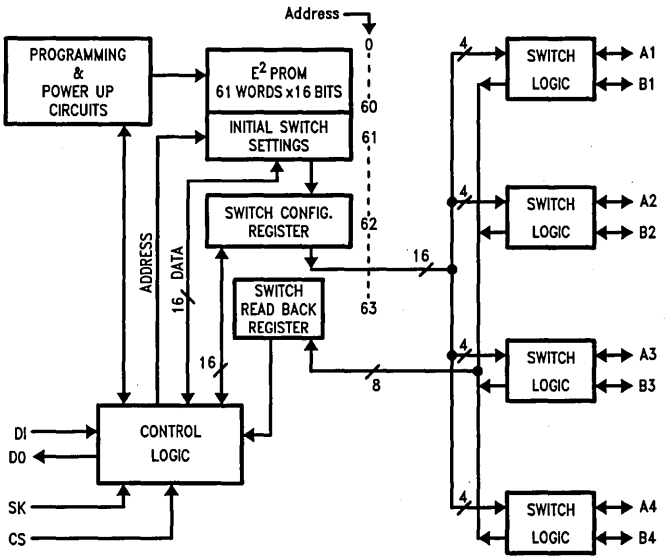

FIGURE 1. NM95C12 Block Diagram

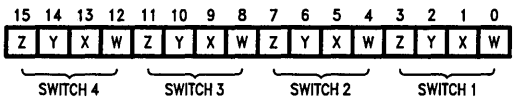

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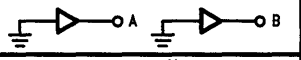
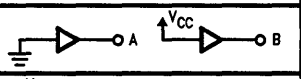
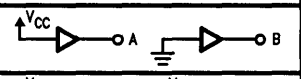
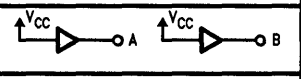
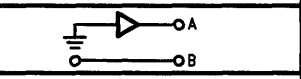
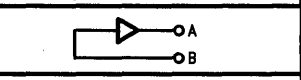
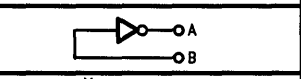
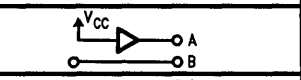
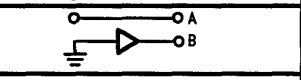
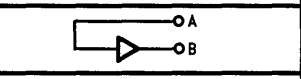
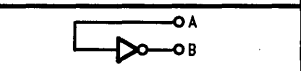
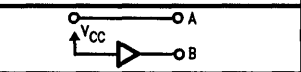
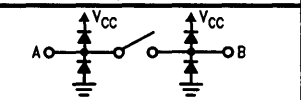
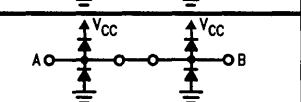
FIGURE 2. Switch Configuration Register (SCR)

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = Tristate
5	0	1	0	1		A = B
6	0	1	1	0		$A = \overline{B}$
7	0	1	1	1		A = 1 , B = Tristate
8	1	0	0	0		A = Tristate , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		$B = \overline{A}$
11	1	0	1	1		A = Tristate , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

For example, in Mode 1, Terminal A would be driving V_{OL} and Terminal B would be driving V_{OH}. In Mode 5, where an input and output structure exists, Terminal A would be driving V_{IL} or V_{IH}. The switches also include a TRI-STATE® mode to represent an open terminal.

Each switch pair can also function as input/output terminals in Modes 5, 6, 9, 10 and 13. Modes 4, 7, 8, 11 and 12 represent the same input/output functions, but with the switch in the "open" configuration.

POWER-UP MODE

When the NM95C12 is powered-up:

1. The data previously stored in the ISR is automatically transferred to the SCR.
2. The SCR controls the switch logic, producing the switch configuration of the terminals A1 through A4 and B1 through B4.

The switch configuration is valid 1 ms after the device power supply reaches 4.5V or greater.

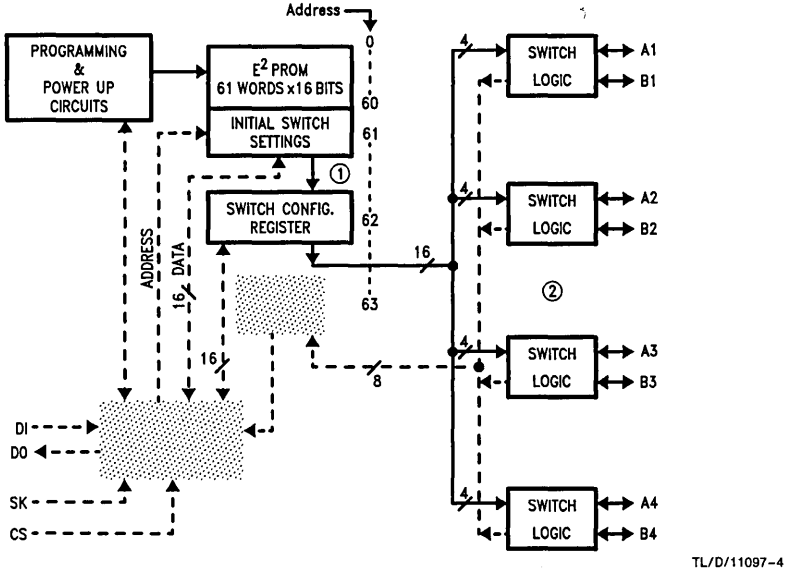


FIGURE 3. Power-Up Mode

UPDATE MODE

To update the information that is contained in the SCR and therefore on the output terminals:

1. The SCR is updated via the serial bus by writing to address 62.
2. The switch logic updates the outputs by selecting the 1 of 14 modes detailed in Table I. The configuration change becomes effective at the terminals after a brief propagation delay (t_{SWPD}), referenced to the falling edge of CS.

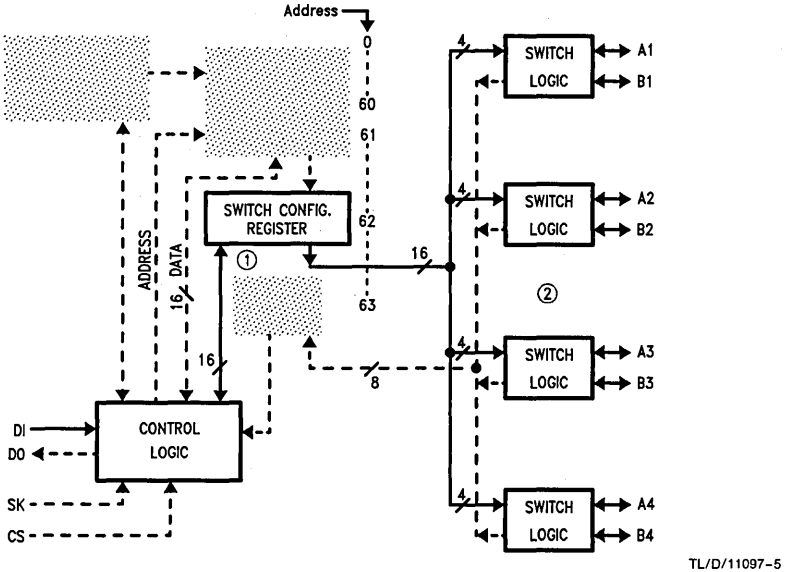


FIGURE 4. Update Mode

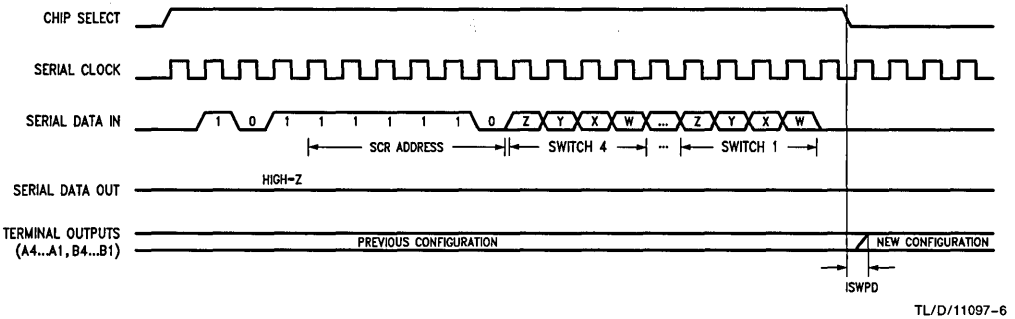


FIGURE 5. SCR Write (Update Mode) Timing Diagram

INPUT MODE

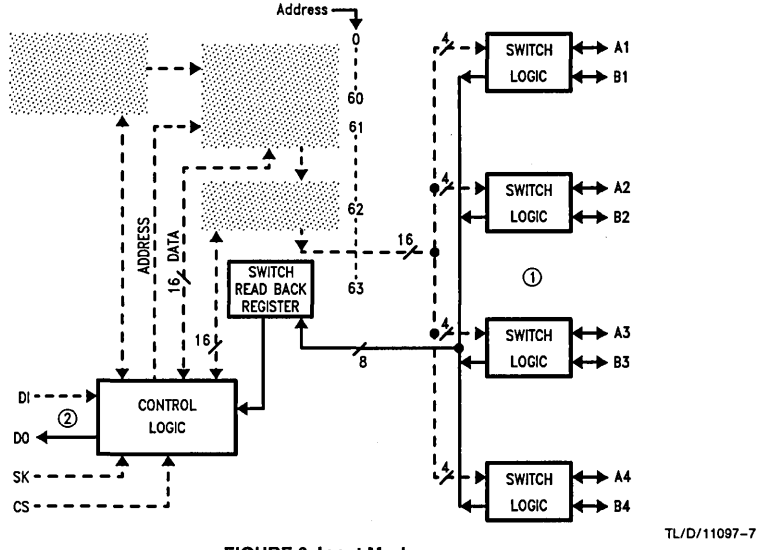
The SRR allows the current logic level present at the switch terminals to be read back on the MICROWIRE™ bus:

1. The states of the output terminals are loaded into the SRR by reading address 63.
2. The control logic allows the 8-bit parallel input to be converted to serial output on the DO pin.

The bit assignments and the conceptual function of the SRR are shown in *Figure 7*. Only bits 15 through 8 are used; Bits 7 through 0 are always read as logical 0.

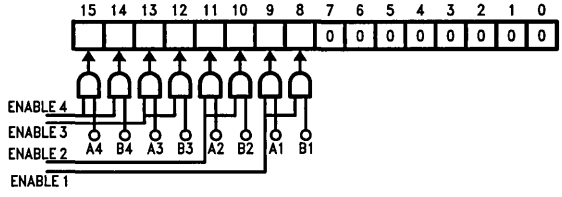
The SRR Read Timing diagram is shown in *Figure 8*. Note that it is valid to terminate any read cycle early, allowing the user to avoid reading Bits 7 through 0 if that is desired. It is also valid to include leading zeros after the CS has gone high and before sending the start bit. Combining leading zeros and terminating the read cycle early may help simplify device control and speed read cycles.

Mode 12, Analog switch open, is valid for SRR input mode. For switch mode 13 (Analog switch closed), the SRR will not report the actual levels present at the terminals due to the analog levels. As a default, bits 15 through 8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the Analog switch mode.



TL/D/11097–7

FIGURE 6. Input Mode



TL/D/11097–8

FIGURE 7. Bit Assignments and Conceptual Function of the Switch Readback Register

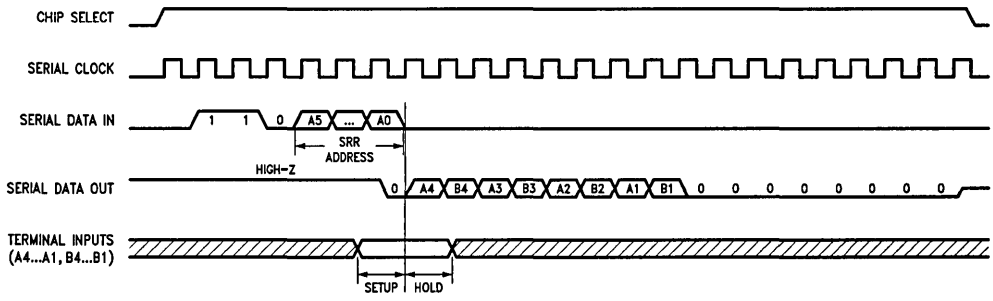


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FIGURE 8. SRR Read (Input Mode) Timing Diagram

SEQUENTIAL REGISTER READ FUNCTION

In a read mode, normally the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the DO pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. In this mode the address count will continue through the ISR, SCR and SRR and then wrap around to Address 0.

During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bit separating the data words.

WRITE CYCLE CONSIDERATIONS

After loading the WRITE instruction and the 16-bit data, the chip enters into a self-timed programming cycle when CS is forced LOW before the next rising edge of the SK clock (refer to *Figure 9*). The timer status is available on the DO pin if the CS input is forced HIGH within 1 ms of starting the programming cycle. LOW on the DO pin indicates that programming is still in progress (BUSY), while HIGH indicates that the device is READY for the next instruction.

If the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

CONCLUSION

National's NM95C12 offers users the standard functionality of a 1024-bit EEPROM and includes 8 programmable terminals that can be used to implement both logic and Analog switch functions simultaneously. These switches can be used, for example, to replace mechanical DIP and SPST switches, as well as allow interrupt polling via the serial bus.

When the device is powered-up, the switch configuration is automatically transferred to the output terminals. The terminals can be updated easily by executing a write cycle. In the input mode, the current logic level at the output terminals is read into the device and output onto the serial bus.

The NM95C12 combines unique and useable features with the simplicity of standard EEPROM functionality.

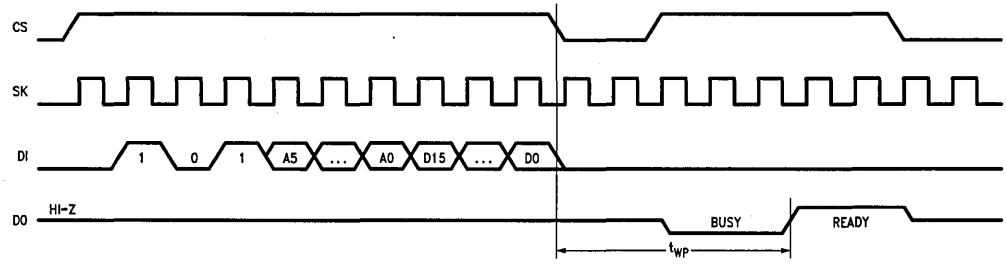

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FIGURE 9. WRITE Timing Diagram

NM95C12 Flexibility in Industrial Control Applications

National Semiconductor
Application Note 755
Sean Long

INTRODUCTION

This application note describes a general purpose industrial controller and details how a NM95C12 can be used to integrate a number of different functions typically found in such a design.

General purpose application examples of the use of the NM95C12 are presented rather than a specific design. Each design idea and software can be incorporated into the designer's required application.

The basic building blocks of an industrial controller (for example, heating, process control, etc.) are a microcontroller, an Analogue to Digital Converter (ADC), an EEPROM, a display (LCD, LED, etc.), I/O interfaces, and power driver/control circuits. The NM95C12 forms the basis of this design performing the non-volatile parameter storage, a low cost ADC, an I/O expander, and providing a simple control interface.

Figure 1 shows the basic block diagram with the shaded parts representing the functions performed by the NM95C12.

This application note will describe the theory of operation behind the design and give detailed software examples to show how to interface a popular microcontroller to the NM95C12.

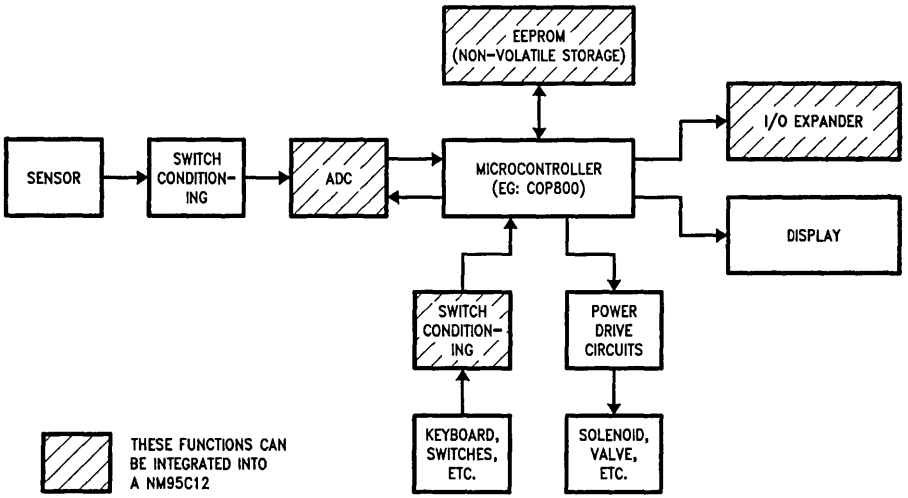

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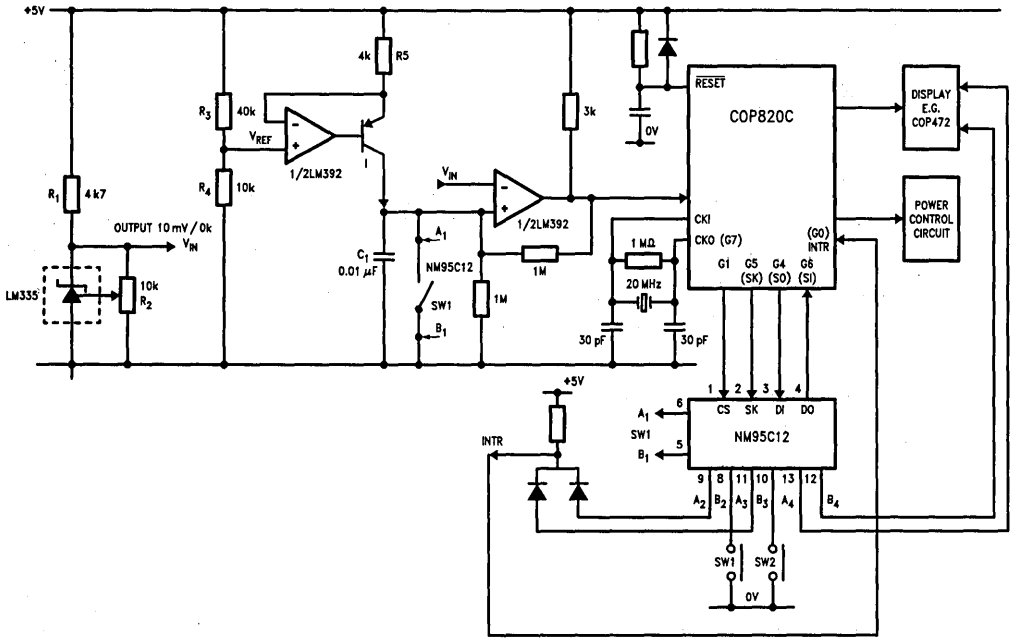
FIGURE 1. Typical Industrial Controller Block Diagram



TL/D/11160–2

COP820/NM95C12 Industrial Controller

THE NM95C12 1024-BIT CMOS EEPROM WITH DIP SWITCHES

The NM95C12 features 1K-bit EEPROM memory with 8 switch logic terminals. These switch logic terminals are individually programmable outputs which may be used as DIP switch positions or as SPST switch positions.

The NM5C12 uses the MICROWIRE™ serial I/O interface which is fully compatible with COPS™ microcontrollers via 4 simple control lines:

SK — Serial Clock
CS — Chip Select
DI — Data In
DO — Data Out

The EPROM array (addresses 0 to 60) is addressed via five instructions:

READ — Read Data from register
WEN — Write enable
WRITE — Writes data to register
WRALL — Writes to all registers
WDS — Disables all programming instructions

This area of memory is used for the normal EEPROM applications such as the storage of user changeable, non-volatile parameters such as time on/off, temperature on/off limits, etc.

CONTROLLING THE SWITCH LOGIC

Address locations 61 to 63 control the switch operation.

Address	Name	Description
61	ISS	Provides the initial switch configuration automatically on power-up. Controlled via a WRITE operation.
62	SCR	The SCR is not an E2 location and hence is volatile. The SCR is loaded automatically from address 61 on power-up. The SCR controls the switch terminals A1–A4 and B1–B4.
63	SRR	The SRR allows the current logic levels of the switch terminals to be read back via the MICROWIRE bus.

THEORY OF OPERATION

The relationship for charge of a capacitor is as follows:

Charge (Q) = Voltage (V) × Capacitance (C)
= Current (I) × Time (T)

Therefore the voltage across the capacitor, V_{CAP}

$V_{CAP} = (I \times T)/C$

Assuming that the current I is a constant source, and the capacitance value C does not vary gives:

V_{CAP} is proportional to T.

Mode of Operation

— initially switch S1 is closed to short out V_{CAP} to measure input voltage V_{IN}

To Measure V_{IN}:

— microcontroller opens S1 and starts internal timer at T1
— V_{CAP} is proportional to time T
— when $V_{CAP} > V_{IN}$ then comparator output V_{COMP} goes high
— microcontroller stops internal timer at T2
— V_{IN} is proportional to time T = T2 − T1
— microcontroller closes S1 ready for next measurement

CURRENT SOURCE/VOLTAGE COMPARATOR FOR ADC

This is based on a LM932 which has an Operational Amplifier and a Voltage Comparator in the same 8-pin package. This device operates from a single +5V supply.

Refer to the National Semiconductor General Purpose Linear Databook for further details of the LM392.

INPUT SENSOR

For this example assume temperature needs to be controlled.

LM335: This is a precision, low-cost, easily calibrated two terminal temperature sensor that behaves like a zener diode with a voltage of +10 mV/degree Kelvin. The initial accuracy is ±1° and can be externally trimmed with a potentiometer connected to the ADJ pin.

Refer to the National Semiconductor Linear Databook 2 for further details of the LM335 Temperature Sensors.

NM95C12 SWITCH LOGIC APPLICATIONS/ CONFIGURATIONS

A_1, B_1—Control the Charge/Discharge of Capacitor for ADC

Switch Configuration:

Analog Switch Open: Mode 12, ZYXW = 110?
(? = don't care)

Analog Switch Closed: Mode 13, ZYXW = 111?

To change the state of the switch terminals A_1, B_1, follow the flowchart in *Figure 3*.

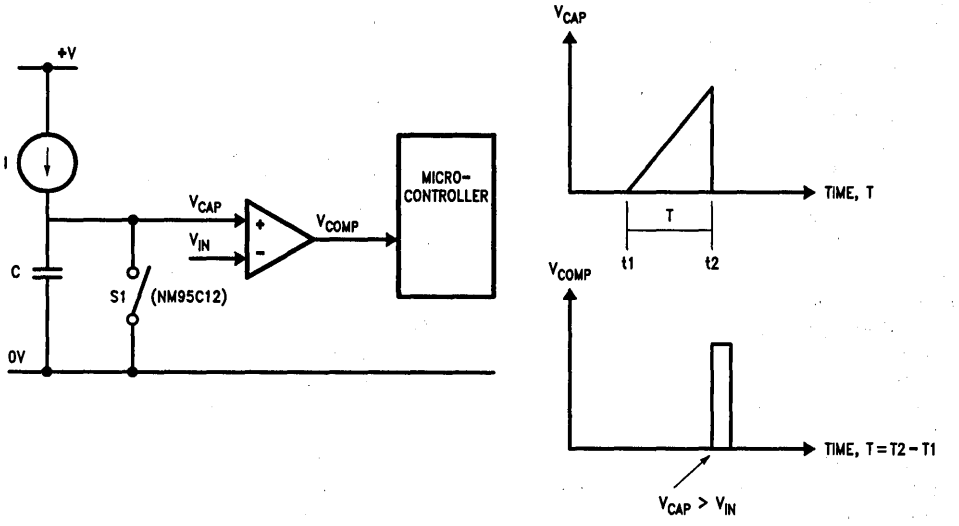


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FIGURE 2. Single Slope Analogue to Digital Converter

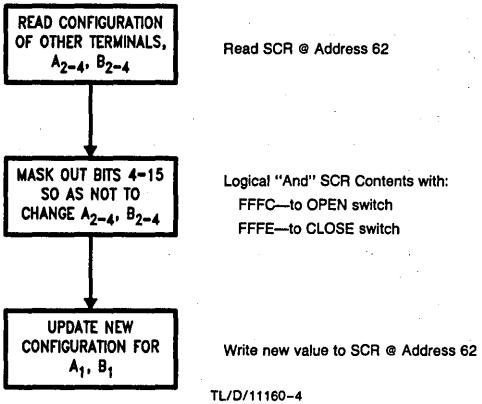

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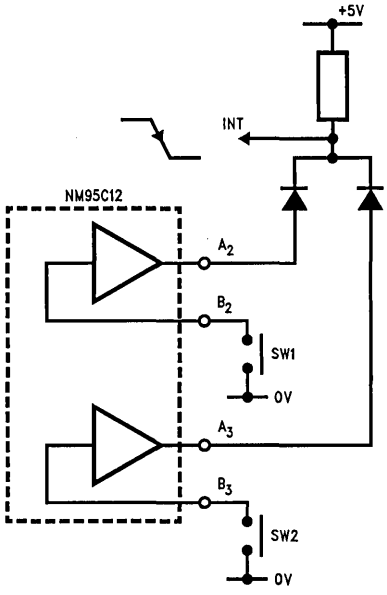
FIGURE 3. Controlling Switch Terminals A1, B1

A_2, B_2 and A_3, B_3 — Switch Debouncing

The switch logic configuration is shown in *Figure 4*. When either of the mechanical switches SW1 or SW2 are pressed, this causes the interrupt line (INT) to be pulled low signalling to the microcontroller that a switch has been pressed. As part of the interrupt service routine the microcontroller can generate a delay to allow time for mechanical switch debouncing, before reading the NM95C12 SRR to determine which mechanical switch was pressed.



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A_2,B_2, A_3,B_3 Configured in mode 5, ZYXW = 0101

FIGURE 4. Switching Conditioning

The advantage of this design is that it saves input pins on the microcontroller and means that the software does not have to perform periodic polling of the inputs to determine the mechanical switch status since the circuit is interrupt driven.

Switch Configuration: both A_2,B_2 and A_3,B_3 will be configured in mode 5; ZYXW = 0101.

To change the state of the switch terminals A_2,B_2 and A_3,B_3 follow the flowchart in *Figure 5*.

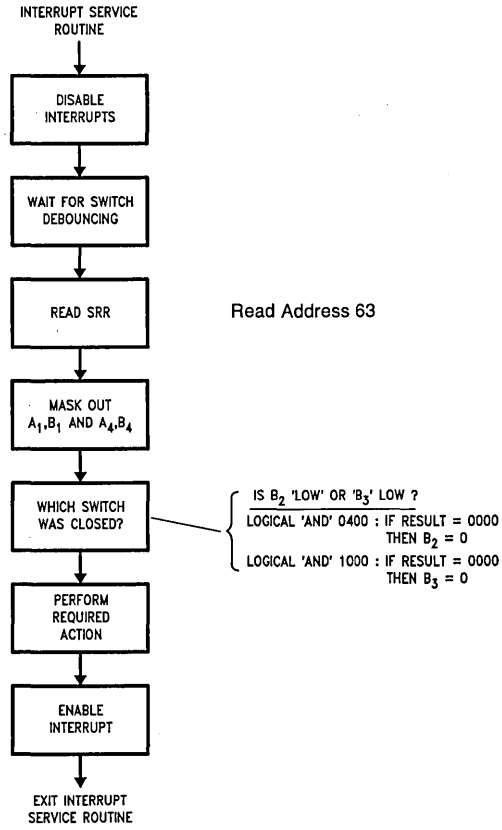

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FIGURE 5. Controlling Switch Terminals A_2,B_2, A_3,B_3

A_4,B_4 Programmable I/O

These two terminals use mode 1 to 4 according to the logic level required on the output. In this example A_4 is used for the Display Chip Select signal and B_4 is used for the Display On/Off control signal.

In order to update and display the contents of the Display then both terminals A_4 and B_4 need to be set to a logic "1" therefore A_4,B_4 are configured in mode 3 with ZYXW = 0011.

To change the state of the switch terminals A_2,B_2 and A_3,B_3 follow the flowchart in *Figure 6*.

SOFTWARE TO INTERFACING THE NM95C12 TO THE COP820 MICROCONTROLLER

This section includes a number of subroutines to interface to a NM95C12 as described in the design example above. There are subroutines to implement each of the basic instructions together with routines for configuring and controlling the switch logic. These subroutines can be used as the basis for a design and be tailored to meet the individual application requirements.

CONCLUSION

The NM95C12 is an extremely versatile and inexpensive device which allows simple interfacing to all popular microcontrollers and microprocessors via a 4-wire serial bus. The complete operation of the NM95C12 can be controlled by a few simple instructions.

The design outlined offers an inexpensive solution for industrial control applications with the key benefits of:

— simple interfacing between microcontroller, EEPROM, "ADC"

— low part count

— fully software controlled and changeable

This has highlighted the flexibility of the NM95C12 and how the switch terminals can be configured for a wide range of applications including: mechanical switch replacement, programmable Address Decoder, programmable I/O expander and a programmable interrupt controller. The NM95C12 offers greater reliability than mechanical switches with the benefits of software control and lower cost.

Plus you still get the 1K-bit EEPROM memory as well!; together with the 8 switch terminals it forms a truly remarkable device.

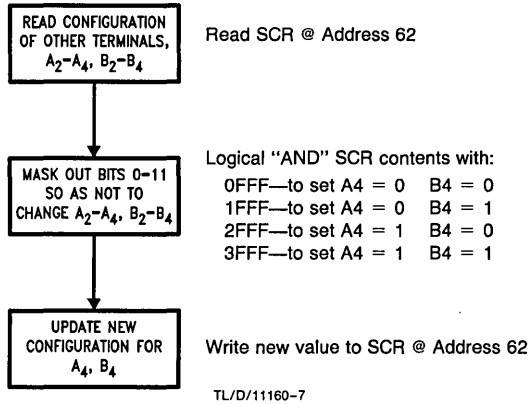

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FIGURE 6. Controlling Switch Terminals A_4,B_4

```
;
; THIS FILE PREDECLARES ITEMS FREQUENTLY USED BY THE
; COP820 PROGRAMMER.
; REGISTER NAMES, CONTROL BITS, ETC. ARE NAMED THE SAME WAY
; AS IN THE DATA-SHEETS.
;
; ************************************************
; * PORT~ , CONFIGURATION- AND CONTROL REGISTERS  *
; ************************************************
      PORTLD   =   0D0          ; PORT L DATA
      PORTLC   =   0D1          ; PORT L CONFIGURATION
      PORTLP   =   0D2          ; PORT L PIN
;
      PORTGD   =   0D4          ; PORT G DATA
      PORTGC   =   0D5          ; PORT G CONFIGURATION
      PORTGP   =   0D6          ; PORT G PIN
      PORTD    =   0DC          ; PORT D
      PORTI    =   0D7          ; PORT I
;
      SIOR     =   0E9          ; SID SHIFT REGISTER
      TMRLO    =   0EA          ; TIMER LOW BYTE
      TMRHI    =   0EB          ; TIMER HIGH BYTE
      TAULO    =   0EC          ; TIMER REGISTER LOW BYTE
      TAUHI    =   0ED          ; TIMER REGISTER HIGH BYTE
;
      CNTROL   =   0EE          ; CONTROL REGISTER
      PSW      =   0EF          ; PSW REGISTER
;             ********************
;             * CONSTANT DECLARE *
;             ********************
;              ---- CNTRL - REGISTER BITS ----

;
      TSEL     =   7
      CSEL     =   6
      TEDG     =   5
      TRUN     =   4
      MSEL     =   3
      IEDG     =   2
      S1       =   1
      S0       =   0
;
;             ---- PSW- REGISTER BITS ----
      HCARRY   =   7
      CARRY    =   6
      TPND     =   5
      ENTI     =   4
      IPND     =   3
      BUSY     =   2
      ENI      =   1
      GIE      =   0

;             I/O - SIGNALS ----
;
      TMRINP   =   3
      INTR     =   0
      TIO      =   3
      SO       =   4
      SK       =   5
      SI       =   6
      CKO      =   7
;
      .CHIP    820
      LD       SP,#02F          ; DEFAULT INITIALIZATION OF SP
```

```
;INCLD COP820.INC
;
; This program provides in the form of subroutines, the ability to enable,
; disable, read and write to the NM95C12 EEPROM with DIP switches.
;
;       ************************************************
;       * PROGRAM VARIABLE MEMORY LOCATION DEFINITIONS  *
;       ************************************************
;
SNDBUF  = 0 ;CONTAINS THE COMMAND BYTE TO BE WRITTEN TO NM95C12
RDATL   = 1 ;LOWER BYTE OF THE NM95C12 REGISTER DATA READ
RDATH   = 2 ;UPPER BYTE OF THE NM95C12 REGISTER DATA READ
WDATL   = 3 ;LOWER BYTE OF THE DATA TO BE WRITTEN TO NM95C12 REGISTER
WDATH   = 4 ;UPPER BYTE OF THE DATA TO BE WRITTEN TO NM95C12 REGISTER
ADDRESS = 5 ;THE LOWER 6-BITS OF THIS LOCATION CONTAIN THE ADDRESS
            ;OF THE NM95C12 REGISTER TO BE READ/WRITTEN
FLAGS   = 6 ;USED FOR SETTING UP FLAGS
            ;
            ; FLAG VALUE        ACTION
            ; ----------        ------
            ;    00             WRITE ENABLE,DISABLE,WRITE ALL
            ;    01             READ CONTENTS OF NM95C12 REGISTER
            ;    03             WRITE TO NM95C12 MEMORY REGISTER
            ;    07             WRITE NM95C12 SCR REGISTER
            ;    OTHERS         ILLEGAL COMBINATION
;
; THE INTERFACE BETWEEN THE COP820C/840C AND THE NM95C12 (1024-BIT EEPROM)
; CONSISTS OF FOUR LINES. THE G1 (CHIP SELECT LINE), G4 (SERIAL OUT SO),
; G5 (SERIAL CLOCK SK) AND G6 (SERIAL IN SI).
;
; ANOTHER PINS USED BY THIS DESIGN IS G0 (INTERRUPT INTR)
;
;
;       ******************
;       * INITIALIZATION *
;       ******************
;
        LD PORTGC,032     ;Setup G1,G4,G5 as outputs
        LD PORTGD,00      ;Initialize G data reg to zero
        LD CNTROL,08      ;Enable MSEL, select MW rate of 2tc
        LD B,fPSW         ;Load B with address of PSW
        LD X,fSIOR        ;Load X with address of Serial I/O Register
;
;
;
;       ********************
;       * WEN INSTRUCTION   *
;       ********************
;
;
; THIS ROUTINE ENABLES PROGRAMMING OF THE NM95C12. PROGRAMMING MUST
; BE PRECEDED ONCE BY A PROGRAMMING ENABLE (WEN).
;
WEN:
        LD  SNDBUF,f030   ; LOAD OP CODE AND 'ADDRESS'
        LD  FLAGS,f0
        JSR INIT
        RET
;
;
;       ********************
;       * WDS INSTRUCTION   *
;       ********************
;
```

```
;
; THIS ROUTINE DISABLES PROGRAMMING OF THE NM95C12.
;
WDS:
        LD  SNDBUF,f0       ; LOAD OP CODE AND 'ADDRESS'
        LD  FLAGS,f0
        JSR INIT
        RET
;
;
;
;       ********************
;       * READ INSTRUCTION *
;       ********************
;
;
; THIS ROUTINE READS THE CONTENTS OF THE NM95C12 REGISTER.
; THE NM95C12 ADDRESS IS SPECIFIED IN THE LOWER 6-BITS OF
; LOCATION "ADDRESS". THE UPPER 2-BITS SHOULD BE SET TO ZERO.
; THE 16-BIT CONTENTS OF THE NM95C12 REGISTER ARE STORED IN
; RDATL AND RDATH.
;
READ:   LD  A,ADRESS     ; LOAD ADDRESS A5-A0 INTO ACCUMULATOR
        OR  A,f080       ; SET OP CODE BITS TO '10'
        X   A,SNDBUF     ; TRANSFER COMMAND BYTE TO SERIAL I/O VARIABLE
        LD  FLAGS,f1
        JSR INIT
        RET
;
;
;
;       *********************
;       * WRITE INSTRUCTION *
;       *********************
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO THE NM95C12 REGISTER WHOSE ADDRESS IS CONTAINED IN THE
; LOWER 6-BITS OF THE LOCATION "ADDRESS". THE UPPER 2-BITS OF
; ADDRESS LOCATION SHOULD BE SET TO ZERO.
;
WRITE:  LD  A,ADRESS      ; LOAD ADDRESS A5-A0 INTO ACCUMULATOR
        OR  A,f040        ; SET OP CODE BITS TO '01'
        X   A,SNDBUF      ; TRANSFER COMMAND BYTE TO SERIAL I/O VARIABLE
        LD  FLAGS,f3
        JSR INIT
        RET
;
;
;
;       *********************
;       * WRALL INSTRUCTION *
;       *********************
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO ALL THE NM95C12 REGISTERS
;
WRALL:  LD  SNDBUF,f040   ; LOAD OP CODE AND ADDRESS'
        LD  FLAGS,f3
        JSR INIT
        RET
;
;
```

```
;       ***********************
;       * WRSCR 'INSTRUCTION' *
;       ***********************
;
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO THE NM95C12 SCR (SWITCH CONTROL REGISTER) WHOSE ADDRESS IS 62 DECIMAL
; WHICH EQUALS f03E HEXADECIMAL. OP CODE = '01'
; A WRITE TO THE SCR DOES NOT REQUIRE A PROGRAMMING CYCLE
;
WRSCR:  LD  SNDBUF,f07E  ; LOAD OP CODE AND ADDRESS
        LD  FLAGS,f7
        JSR INIT
        RET
;
;
;
;       ***********************************
;       * EXECUTE INSTRUCTION SUBROUTINES *
;       ***********************************
;
;
;
; THIS ROUTINE SENDS OUT THE START BIT AND THE COMMAND BYTE.
; IT ALSO DECIPHERS THE CONTENTS OF THE FLAG LOCATION AND TAKES
; A DECISION REGARDING WRITE, WRITE SCR, READ OR RETURN TO THE
; CALLING_ROUTINE.
;
INIT:   SBIT 1,PORTGD    ;SET CHIP SELECT HIGH
        LD SIOR,f001     ;LOAD SIOR WITH START BIT
        SBIT BUSY,[B]    ;SEND OUT THE START BIT
PUNT1:  IFBIT BUSY,[B]
        JP PUNT1
        LD A,SNDBUF
        X  A,[X]         ;LOAD SIOR WITH COMMAND BYTE
        SBIT BUSY,[B]    ;SEND OUT COMMAND BYTE
PUNT2:  IFBIT BUSY,[B]
        JP PUNT2
        IFBIT 0,FLAGS    ;ANY FURTHER PROCESSING?
        JP NOTDON        ;YES
        RBIT 1,PORTGD    ;NO, RESET CS AND RETURN
        RET
;
NOTDON:
        IFBIT 1,FLAGS    ;READ OR WRITE?
        JP WR95C12       ;JUMP TO WRITE ROUTINE
        LD SOIR,f000     ;NO, READ NM95C12
        SBIT BUSY,PSW    ;DUMMY CLOCK TO READ ZERO
        RBIT BUSY,[B]
        SBIT BUSY,[B]
PUNT3:  IFBIT BUSY,[B]
        JP PUNT3
        X   A,[X]
        SBIT BUSY,[B]
        X   A,RDATH
```

```
PUNT4:  IFBIT BUSY,[B]
        JP PUNT4
        LD A,[X]
        X  A,RDATL
        RBIT 1,PORTGD
        RET
;
WR95C12:
        LD  A,WDATH
        X   A,[X]
        SBIT BUSY,[B]
PUNT5:  IFBIT BUSY,[B]
        JP  PUNT5
        LD  A,WDATL
        X   A,[X]
        SBIT BUSY,[B]
PUNT6:  IFBIT BUSY,[B]
        JP  PUNT6         ; FINISHED CLOCKING OUT DATA
        RBIT 1,PORTGD     ; RESET CHIP SELECT
        IFBIT 2, FLAGS    ; WRITE/WRALL OR WRSCR?
        RET               ; WRSCR , NO PROGRAMMING TIME SO RETURN
        SBIT 1,PORTGD     ; SET CHIP SELECT TO ALLOW TO POLL DO FOR BUSY/READY
POLL:   IFBIT SI,PORTGP   ; IS NM95C12 DO = SI LOW?
        JP ENDTWP         ; DO HAS GONE HIGH, SO END PROGRAMMING CYCLE
        JP POLL           ; DO IS STILL LOW, SO KEEP POLLING
;
ENDTWP;
        BIT 1, FLAGS      ; RESET CHIP SELECT
        RET
;
        .END
```

Using the NM95C12 to Solve Common Manufacturing Problems

National Semiconductor
Application Note 756
Kent Brooten

INTRODUCTION

This application note describes how the NM95C12 E^2P-ROM + Dip Switches is utilized to reduce manufacturing costs and increase reliability.

PROBLEM

The application described herein is a factory programmable power supply. The existing system *(Figure 1)* requires one of three different power supplies, depending on the options installed in the final unit. The design engineer has presented two solutions:

1. Three different assemblies, one for each output configuration, or,
2. One assembly with a dip switch (or jumpers) to select the configuration.

The manufacturing engineer would prefer to have one assembly that would satisfy all three needs. Dip switches are undesirable because they are difficult to flow solder when on the PCB (and later clean the PCB) as well as posing a threat to the final system should an untrained technician choose to change a switch setting (thus altering the output voltage). Jumpers are undesirable since they require hand soldering—an additional step.

The manufacturing engineer would prefer to have one final test program—not three.

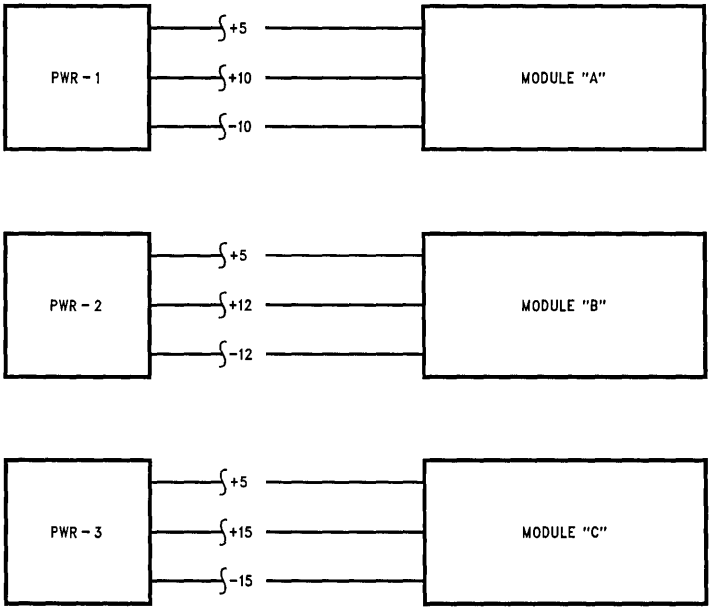
THE SOLUTION

The NM95C12 provides the solution. It enables the power supply module to be configured for any of the three output voltages. There only needs to be one assembly. No dip switches or jumpers are used. The Automatic Test Equipment (ATE) used at final test can check all three configurations. The test program can set the final configuration as well as assign a serial number and date of manufacture which is stored in the EEPROM.

THE DESIGN

The power supply is designed using an LM2577 switching regulator ("the Simple Switcher") in the flyback mode *(Figure 2)*. The resistor divider R_1/R_2 set the output voltages V_{OUT1} and V_{OUT2}. All three output voltages can be set by merely selecting which combination of R_1/R_2 is connected to the feedback pin of the switching regulator. When the switches in the NM95C12 are configured for the analog switch mode, they can be used to connect the appropriate switch to the feedback pin of the Simple Switcher™.

The manufacturing group need only produce one assembly which is electronically configured either at final test or during final assembly. An increase in manufacturing efficiency results.



TL/D/11161-1

FIGURE 1. Modules A, B, C Each Require Slightly Different Power Supply Modules

During final test, the ATE can check each switch position by sending serial commands via the serial μWIRE interface of the NM95C12. The serial number and date of manufacture can be stored at this time. Output configuration can be selected at final test or the power supply modules can be stored and the output voltage programmed at a later time.

Note that there is no microcontroller necessary in the system. While the NM95C12 is typically utilized in a μController based system, it can also be used in non-μController applications. The ATE provides programming and control of the NM95C12 and connects to pads on the PCB via a bed-of-nails test fixture. Alternatively, the Clock, Data IN, Data OUT and Chip Select lines can be routed to fingers on an edge connector.

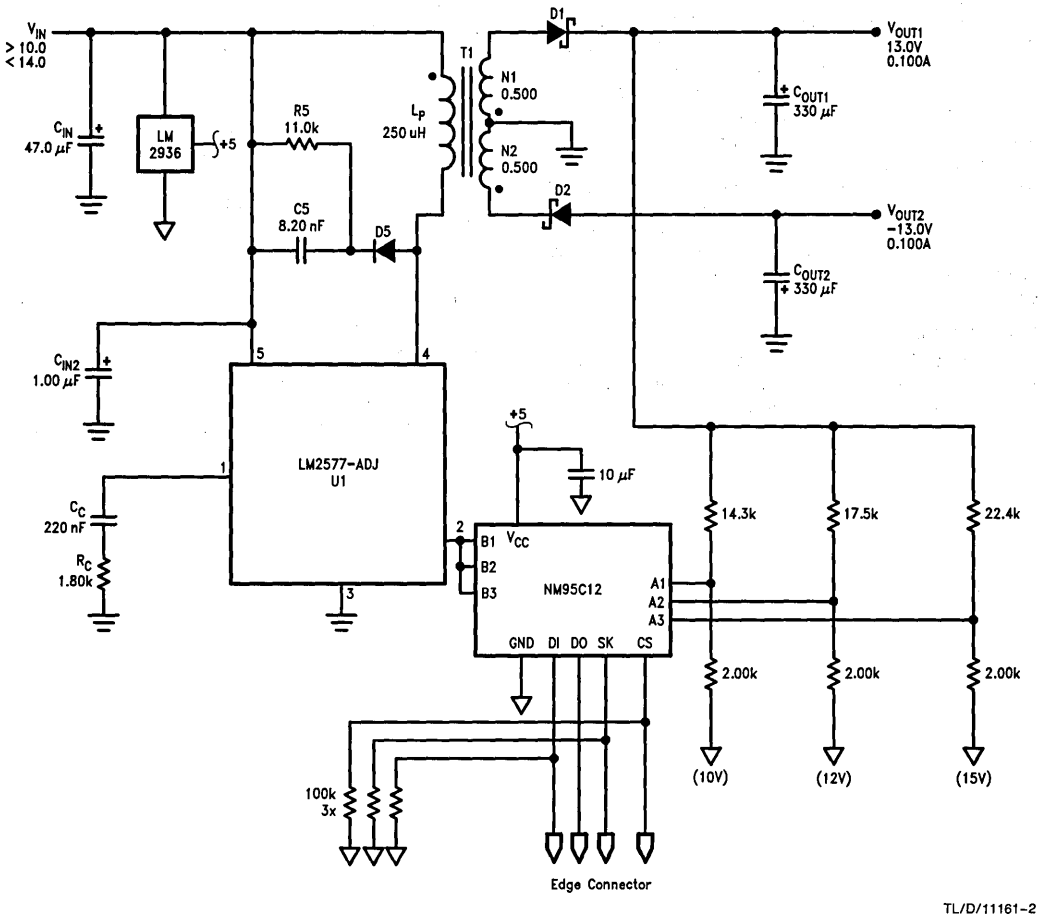
PROGRAMMING

The programming example is written in the popular Z80 assembly language. An NSC800 is used for this example. Flow charts are shown for each module.

SUMMARY

The NM95C12 is used in this application to replace a dip switch. The user benefits in many ways:

1. Increased efficiency by manufacturing 1 large lot of sub-assemblies rather than 3 smaller ones,
2. Ease of manufacturing since neither mechanical dip switches have to be treated with extra care nor jumpers specially installed,
3. Only 1 sub-assembly needs to be inventoried, cutting costs,
4. Increased reliability because mechanical devices are not used,
5. Increased efficiency at final test since only 1 test program can check all three configurations,
6. Inventory costs are reduced because 1 assembly will satisfy any of 3 different functions, and
7. A history of the module can be stored in the EEPROM portion of the device including serial number, date of manufacture, date of last repair, etc.



TL/D/11161–2

FIGURE 2

```
;
;       THIS PROGRAMMING EXAMPLE IS A SAMPLE
;       THAT COULD BE USED TO PROGRAM THE NM95C12
;
;       IT IS WRITTEN IN Z80 ASSEMBLY LANGUAGE FOR THE NSC800



;
;       EQUATES:
;
READ    EQU     80H             ;READ COMMAND
WEN     EQU     00H+30H         ;WRITE ENABLE COMMAND
WRITE   EQU     40H             ;WRITE COMMAND
WRALL   EQU     00H+10H         ;WRITE ENTIRE MEMORY
WDS     EQU     00H             ;WRITE DISABLE
;
MODE0   EQU     0H              ;A=0,B=0
MODE1   EQU     1H              ;A=0,B=1
MODE2   EQU     2H              ;A=1,B=0
MODE3   EQU     3H              ;A=1,B=1
MODE4   EQU     4H              ;A=0,B=TS
MODE5   EQU     5H              ;A=B
MODE6   EQU     6H              ;A=B'
MODE7   EQU     7H              ;A=1,B=TS
MODE8   EQU     8H              ;A=TS,B=0
MODE9   EQU     9H              ;B=A
MODE10  EQU     0AH             ;B=A'
MODE11  EQU     0BH             ;A=TS,B=1
MODE12  EQU     0CH             ;ANALOG SWITCH OPEN
MODE13  EQU     0DH             ;ANALOG SWITCH CLOSED
;
OPEN    EQU     MODE12          ;
CLOSED  EQU     MODE13          ;
;
;       MASKS USED TO OPEN AND CLOSE SWITCHES
;
AB1CLO  EQU     0000FH          ;SWITCH 1 CLOSED
AB2CLO  EQU     000F0H          ;SWITCH 2 CLOSED
AB3CLO  EQU     00F00H          ;SWITCH 3 CLOSED
AB4CLO  EQU     0F000H          ;SWITCH 4 CLOSED
AB1OPN  EQU     0000CH          ;SWITCH 1 OPEN
AB2OPN  EQU     000C0H          ;SWITCH 2 OPEN
AB3OPN  EQU     00C00H          ;SWITCH 3 OPEN
AB4OPN  EQU     0C000H          ;SWITCH 4 OPEN
AB1MSK  EQU     0FFF0H          ;MASK
AB2MSK  EQU     0FF0FH          ;
AB3MSK  EQU     0F0FFH          ;
AB4MSK  EQU     00FFFH          ;
;
;       EEPROM MEMORY LOCATIONS
;
ENABLE  EQU     0               ;LOC 0,BIT 0=1 IF WR ENABLE
;                               ;           =0 IF WR DISABLED
SN      EQU     1               ;SERIAL NUMBER STORAGE
DATE    EQU     32              ;DATE STORED (DP8570 FORMAT)
PUSCR   EQU     61              ;SCR LOADED FROM HERE ON POWER UP
SCR     EQU     62              ;SWITCH CONFIGURATION REGISTER
SRR     EQU     63              ;SWITCH READ BACK REGISTER (READ ONLY)
```

TL/D/11161–3

```
EEPORT: EQU     00H             ;I/O ADDRESS OF PARALLEL PORT
EE:     EQU     EEPORT          ;SHORTHAND


;       THE PARALLEL PORT IS CONFIGURED AS:
;
;               BIT 0 = DATA OUT     OUTPUT
;               BIT 1 = CLOCK        OUTPUT
;               BIT 2 = CHIP SELECT  OUTPUT
;               BIT 3 = N/U
;               BIT 4 = N/U
;               BIT 5 = N/U
;               BIT 6 = N/U
;               BIT 7 = DATA IN      INPUT
;
;       FOR THIS PROGRAMMING EXAMPLE:
;
;               H  = EEPROM OPCODE
;               L  = EEPROM ADDRESS
;               DE = 16 BIT DATA
;               B  = SHIFT COUNTER
;               C  = PORT DATA STORAGE
;               A  =

        ORG     1000H
;
;
;       MAIN PROGRAM
;
;       THIS SAMPLE PROGRAM SETS SWITCH 1 CLOSED, ALL OTHERS OPEN
;
MAIN:
        LD      H,WEN           ;ENABLE CODE FOR NM95C12
        CALL    WRCMD           ;SEND COMMAND
        LD      DE,AB1CLO+AB2OPN+AB3OPN+AB4OPN
                                ;SWITCH 1 CLOSED
                                ;SWITCH 2 OPEN
                                ;SWITCH 3 OPEN
                                ;SWITCH 4 OPEN
        LD      H,WRITE         ;EEPROM OPCODE
        LD      L,SCR           ;ADDRESS TO WRITE TO
        CALL    WRDATA          ;WR TO SWITCH CONFIGURATION REGISTER
        LD      H,WRITE         ;OPCODE
        LD       L,PUSCR                ;ADDRESS
        CALL    WRDATA          ;WR TO POWER UP SCR
        LD      H,WDS           ;WRITE DISABLE
        CALL    WRCMD           ;DISABLE FURTHER WRITING
        HALT                    ;END OF THIS EXAMPLE
```

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```
;
;       WRITE COMMAND SUBROUTINE
;
;       USE FOR "WEN" AND "WDS" COMMANDS
;
;       WRITES COMMAND TO EEPROM
;       EXPECTS COMMAND TO BE IN H REG
;       EXPECTS ADDRESS TO BE IN L REG
;
WRCMD:
        CALL    PRECK           ;SET CS, CHECK FOR BUSY
        CALL    SHIFT8          ;SEND COMMAND
        CALL    CSLOW           ;SET CS INACTIVE
        RET                     ;DONE
;
;       WRITE DATA SUBROUTINE
;
;       USE FOR "WRITE" AND "WRALL" COMMANDS
;
;       WRITES COMMAND AND DATA TO EEPROM
;       EXPECTS COMMAND TO BE IN H REG
;       EXPECTS ADDRESS TO BE IN L REG
;       EXPECTS DATA    TO BE IN D&E REG
;       ASSUMES EEPROM IS WRITE ENABLED
;
WRDATA:
        CALL    PRECK           ;PRELIMINARY CKS
        CALL    SHIFT8          ;SEND COMMAND
        CALL    SHIFT16         ;SEND DATA
        CALL    CSLOW           ;SET CS INACTIVE
        RET
;
;       THIS ROUTINE DOES A PRECHECK OF THE EEPROM STATUS
;
;       IT SETS CS ACTIVE
;       WAITS AT LEAST 500 NS
;       LOOPS TILL NOT BUSY
;       LEAVES CS ACTIVE, DATA OUT LOW
;       IT EXPECTS PORT DATA IN C REG
;
PRECK:
        PUSH    AF              ;SAVE
        LD      A,C             ;GET PORT DATA
        AND     0FDH            ;MASK CLK & DATA LOW
        OR      4               ;SET CS ACTIVE
        LD      C,A             ;SAVE
        OUT     (EE),A          ;WRITE TO PORT
PRECK1:
        IN      A,(EE)          ;READ PORT
        AND     80H             ;ACC = 0 IF BUSY
        JP      Z,PRECK1        ;LOOP UNTILL NOT BUSY
        POP     AF              ;RESTORE
        RET                     ;ELSE DONE
```

TL/D/11161–5

```
;
;       THIS ROUTINE SHIFTS OUT 8 BITS OF COMMAND (+ START BIT)
;
;       IT WRITES TO A PARALLEL PORT WHOSE OUTPUTS ARE CONFIGURED AS:
;
;       BIT 0 = DATA
;       BIT 1 = CLOCK
;       BIT 2 = CHIP SELECT (ACTIVE HI)
;
;       IT ASSUMES CS IS ACTIVE
;       IT SENDS A START BIT (LOW TO HI TRANSITION)
;       THEN IT SENDS DATA MSB FIRST
;       IT EXPECTS PORT DATA IN C REG
;       IT DESTROYS H,L,B
;
SHIFT8:
        PUSH    AF              ;SAVE
        CALL    STRTBT          ;SEND START BIT
        LD      B,7             ;LOOP COUNTER
        LD      A,L             ;ADDRESS
        OR      H               ;COMBINE WITH OPCODE
        LD      L,A             ;SAVE IN L
SNDBIT:
        LD      A,C             ;GET PORT CONTENTS
        AND     0FDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     L               ;CK MSB OF DATA
        JP      NC,SH8LP        ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH8LP:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     0FDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBIT       ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT 8 BITS
;
        POP     AF              ;RESTORE
        RET                     ;
```

TL/D/11161–6

```
;
;       THIS ROUTINE SHIFTS OUT 16 BITS OF DATA
;
;       IT WRITES TO A PARALLEL PORT WHOSE OUTPUTS ARE CONFIGURED AS:
;
;       BIT 0 = DATA
;       BIT 1 = CLOCK
;       BIT 2 = CHIP SELECT (ACTIVE HI)
;
;       IT ASSUMES CS IS ACTIVE
;       <DE> HOLDS DATA TO BE SENT (MSB FIRST)
;
SHIFT16:
        PUSH     AF
        PUSH    DE              ;
        LD      B,7             ;LOOP COUNTER
SNDBT:
        LD      A,C             ;GET PORT CONTENTS
        AND     0FDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     D               ;CK MSB OF FIRST BYTE OF DATA
        JP      NC,SH16LP       ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH16LP:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     0FDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBT        ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT FIRST 8 BITS
;
        LD      B,7             ;LOOP COUNTER
SNDBT1:
        LD      A,C             ;GET PORT CONTENTS
        AND     0FDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     E               ;CK MSB OF SECOND BYTE OF DATA
        JP      NC,SH16LP1      ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH16LP1:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     0FDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBT1       ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT ALL 16 BITS
;
        POP     DE              ;
        POP     AF              ;RESTORE
        RET                     ;
```

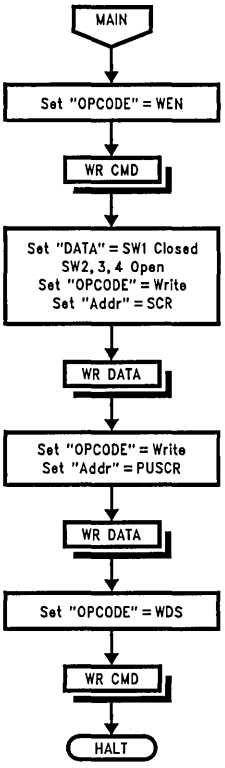
TL/D/11161–7

```
;
;       SEND A START BIT
;
STRTBT:
        PUSH    AF              ;SAVE ACC
        LD      A,C             ;GET PORT CONTENTS
        AND     OFCH            ;MASK CLK & DATA LOW
        OUT     (EE),A          ;SEND IT
        OR      1               ;DATA = 1
        OUT     (EE),A          ;SET UP DATA
        OR      2               ;CLK = 1
        OUT     (EE),A          ;SEND
        AND     OFDH            ;CLK = 0
        OUT     (EE),A          ;SEND
        LD      C,A             ;SAVE NEW CONTENTS IN C
        POP     AF              ;RESTORE ACC
        RET                     ;
;
;       SET CS LOW (INACTIVE)
;
;       ALTERS C REG
;
CSLOW:
        PUSH    AF              ;SAVE
        LD      A,C             ;GET PORT DATA
        AND     OF8H            ;SET CS LOW (AND DATA AND CLK)
        LD      C,A             ;SAVE
        OUT     (EE),A          ;WRITE TO PORT
        POP     AF              ;RESTORE
        RET                     ;DONE


        END
```

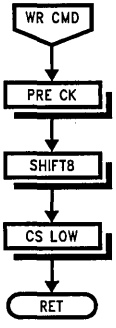
TL/D/11161–8

Main Loop

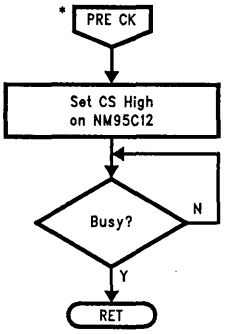


TL/D/11161–9

Write Command to NM95C12

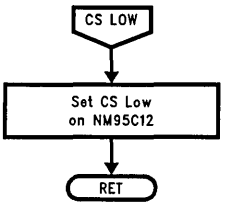


TL/D/11161–10



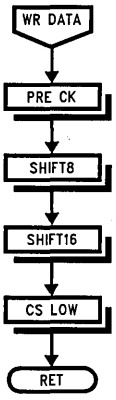
TL/D/11161–11

*Pre-check of NM95C12 sets CS active. Returns when NM95C12 not busy.



TL/D/11161–12

Write Data (16 Bits) to NM95C12



CS Active
Wait Till Not Busy

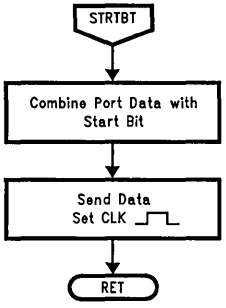
Send OPCODE + ADDRESS

Send Data

CS Inactive

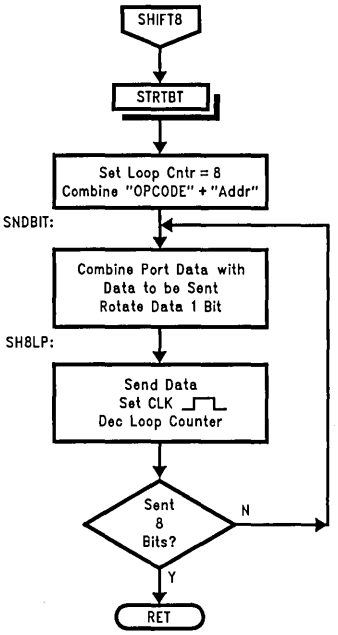
TL/D/11161–13

Send Start Bit to NM95C12



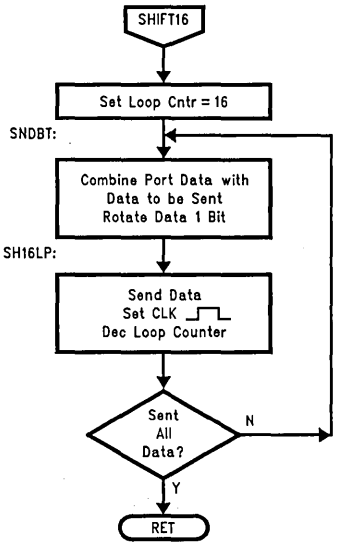
TL/D/11161–14

Shifts 8 Bits into the NM95C12 via the Data IN Pin



TL/D/11161–15

Shift 16 Bits of Data to NM95C12



TL/D/11161–16

Using National's MICROWIRE™ EEPROM

National Semiconductor
Application Note 758
Paul Lubeck

National Semiconductor manufactures a wide range of low density serial EEPROMs that use the MICROWIRE interface as a means of communication. Although all of these devices use the MICROWIRE interface, there are slight variations in interfacing due to differences in memory sizes, features, and technology used to implement the device. Additionally, the MICROWIRE interface does not specifically define any protocol, it only defines a basic set of signal lines to interconnect two or more devices. Due to these reasons, additional information is necessary to fully understand how to best interface to National's family of MICROWIRE EEPROM.

The goal of this application guide is to cover a diversity of information in regard to basic timing, interfacing options, and functionality of different EEPROMs. I will use an outline approach, so the appropriate heading can be located easily. Each section attempts to be stand alone so the information can be easily extracted. The outline appears below:

OUTLINE

1.0 Description of EEPROM Families
- 1.1 CMOS EEPROM
  - 1.1.1 NM93C Family
  - 1.1.2 NM93CS Family
  - 1.1.3 Variations

2.0 HARDWARE CONNECTIONS
- 2.1. INTERFACE PIN DESCRIPTIONS
  - 2.1.1 Chip Select
  - 2.1.2 Serial Clock
  - 2.1.3 Data-In (DI)
  - 2.1.4 Data-Out (DO)
  - 2.1.5 Program Enable (PE)
  - 2.1.6 Protect Register Enable (PRE)
  - 2.1.7 Organization (ORG)
  - 2.1.8 Status (RDY/BUSY)
- 2.2. FOUR WIRE BUS
- 2.3. THREE WIRE BUS

3.0 TIMING CONSIDERATIONS
- 3.1 BUS TIMING
- 3.2 INSTRUCTION SEQUENCE DESCRIPTIONS
  - 3.2.1 Read Cycle
  - 3.2.2 Sequential Read
  - 3.2.3 Erase and Erase All
  - 3.2.4 Write and Write All
  - 3.2.5 Program Enable and Program Disable
  - 3.2.6 Protect Register Read
  - 3.2.7 Protect Register Enable
  - 3.2.8 Protect Register Disable
  - 3.2.9 Protect Register Clear
  - 3.2.10 Protect Register Write
- 3.3. INTERFACING SOLUTIONS

4.0 CONCLUSION

1.0 Description of EEPROM Families

1.1 CMOS EEPROM

National builds a range of MICROWIRE CMOS EEPROMs in memory sizes ranging from 256-bit to 4906-bit. The NM93C family is the base family and the NM93CS is a similar family with additional features, there are also other devices with slight variations on the interface. All these devices are available with certain "standard" options such as operating temperature ranges and operating voltage ranges, packaging options and test options. These options being fairly standard variations for semiconductor devices, will not be addressed beyond this. The purpose of this article is to address basic functionality and interfacing, including various tricks to simplify or modify the interface.

1.2 NM93C Family

The NM93C family of EEPROM is available in 256-, 1024-, 2048-, and 4096-bit sizes. All of these are internally organized in 16-bit words, therefore all data transactions deal with 16 bits. This family of EEPROMs has 7 instructions that deal with read, write, and a basic level of data protection. The instructions are listed in Table I. It is important to note that there is a basic difference in length of the instruction between the NM93C06 or NM93C46 and the NM93C56 or NM93C66. This is due to the larger devices needing additional address bits.

The NM93C family of EEPROM, like all of National's serial EEPROMs have a basic level of write protection that can be turned on or off by the use of the ERASE/WRITE DISABLE (EWDS) and ERASE/WRITE ENABLE (EWEN) instructions. Although there are two erase instructions included in the NM93C family, these are included only for compatibility with older EEPROMs that require erase before write. These EEPROMs don't require erase before write and it is recommended that in application the erase not be used as this adversely affects endurance.

1.3 NM93CS Family

The NM93CS EEPROMs are identical to the NM93C family in memory sizes and organization. Making them different, they have two additional functions, sequential read and user configurable write protection, and don't have either of the erase functions, ERASE and ERASE-ALL as they are not needed. Like all of the CMOS EEPROMs, these have self timed programming cycles and operate from a single external supply of either 4.5V to 5.5V or 2.0V to 5.5V. In these devices it is necessary to eliminate the erase cycles from the code as they may adversely affect the performance of the device.

As these have additional functions, the instruction set includes a total of 10 instructions, 3 that operate on the memory array, 2 that deal with the basic write protection and 5 that deal with the user configurable write protection. Refer

to the NM93CS instruction set table (Table II) for definitions of these instructions. As with the NM93C family, there is a basic difference in instruction length depending on memory size.

To further increase data security in these EEPROMs there are also two additional input signals defined, Program Enable (PE) and Protect Register Enable (PRE). These signals are on pins that are unused on the NM93C family providing upward compatibility to the NM93CS devices.

TABLE I. NM93C Family Instruction Set Table

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7/A5–A0		Reads data stored in memory.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

TABLE II. NM93CS Family Instruction Set Table

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Program address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

1.1.3 Variations

There are two variations on the standard implementation of the Microwire bus. Both variations can be viewed as enhancements. The first enhancement is a Organization (ORG) input that allows the user to select the internal configuration of the memory as either 8 bits wide or 16 bits wide. When the input is high or unconnected, the device is configured as 16 bits wide, when the ORG input is at a low level, the memory is configured as 8 bits wide, but twice as deep. The feature is present on both the NM93C46A and the NM59C11.

The second variation is the STATUS output. This is the Busy/Ready polling to indicate programming status. All other devices have this feature on the Data-Out (DO) output, the NM59C11 alone has status available as a separate output and not on the Data-Out output. This can simplify interfacing to a bidirectional data bus.

2.0 Hardware Connection

2.1 INTERFACE PIN DESCRIPTIONS

In this section, each possible input or output will be described followed by the most popular variations of bus connections. Not all devices have all of the described I/Os. The I/Os are available according to Table III, I/O Functionality.

2.1.1 CHIP SELECT (CS)

Chip Select is used to differentiate between various devices on the same Microwire bus. In the case of EEPROM it cannot be tied high even if it is the only device on the bus as it performs several additional functions. As it applies to any of the Microwire EEPROMs, the rising edge resets the internal circuitry of the device, a function necessary prior to initiating any new cycle. As shown in the functional block diagram *(Figure 1)* chip select also gates the data input and clock input, thus disabling these functions.

During the course of clocking in the start bit, op-code address and data-in or data-out, chip select must be held high continuously, otherwise the internal circuits will be reset and the cycle will have to be started again with a new start bit.

During programming cycles chip select initiates the internal programming cycle. The falling edge of chip select will start the internal programming cycle when a programming op-code has been entered (Erase, Write, Erase All, Write All) and then, in conjunction with Data-Out (DO), will indicate if programming is complete (except the NMOS NMC9306). If programming is complete, Data-Out will drive high, if incomplete it will drive low. In the case of the NMC9306, the user must provide the programming time and in this case chip select must be held low for a minimum of 10 ms, then brought high and clocked to end the programming cycle.

Several additional notes in regard to chip select:

If a programming cycle is partially clocked in and then chip select dropped, the EEPROM may enter into a programming mode. This is determined by how many bits have been clocked in when chip select is dropped. If the start bit, op-code, and all of the address has been clocked in, a programming cycle will be initiated with no or partial data. If less than a complete address has been clocked in, the programming cycle will not be initiated. Refer to *Figure 2*, reference line 1.

In the case of the NM59C11, a programming cycle will not be entered unless a full data field has been clocked in. A full data field may be either 8 or 16 bits depending on the logic level present at the ORG input. A programming cycle will be entered at reference line 2 in *Figure 2* for the NM59C11.

Chip select hold time at the end of a cycle is referenced to the last rising edge of clock (SK). The hold time from the rising edge is the same as the minimum SK high time for the particular device. This is stated in the datasheets as 0 ns hold time from the falling edge of SK which assumes that SK high time is always minimum. In this case SK can be left in the high state or taken low at a later time. Internally chip select gates SK, therefore SK is not critical.

TABLE III. I/O Functionality by Device

	CS	SK	DI	DO	PE	PRE	ORG	STAT
NM93C Family	X	X	X	X				
NM93CS Family	X	X	X	X	X	X		
NM93C46A	X	X	X	X			X	
NM59C11	X	X	X	X			X	X

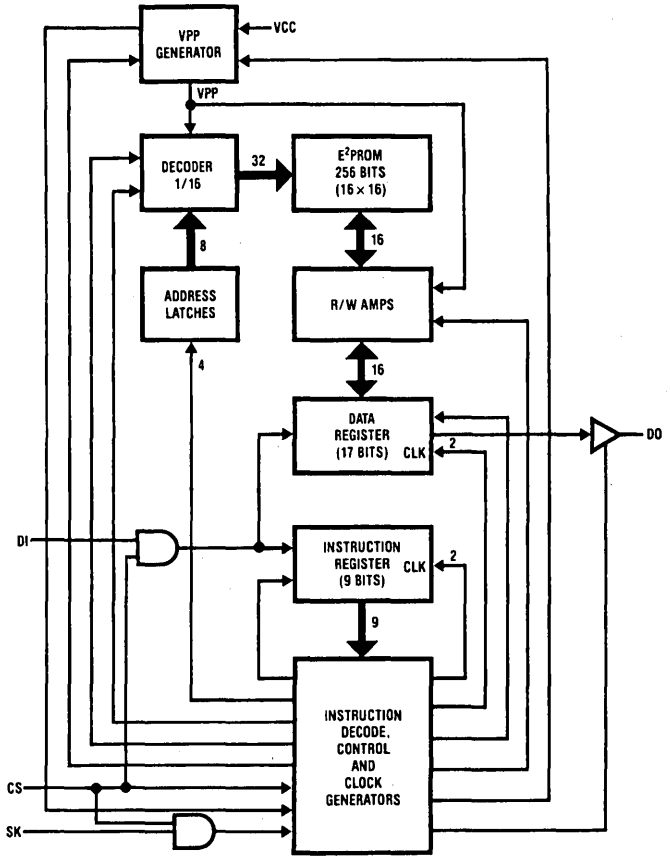


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FIGURE 1. Block Diagram

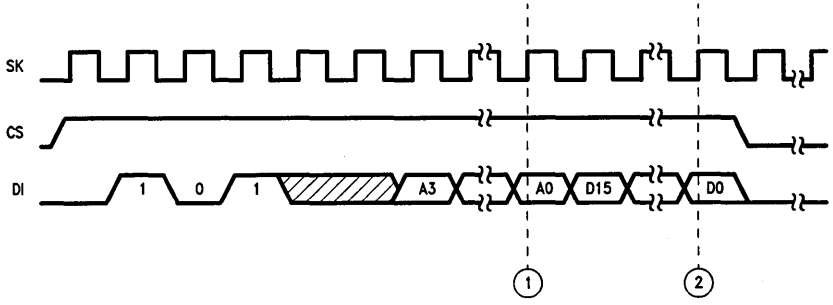

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FIGURE 2. Programming Cycle Point of No Return

2.1.2 SERIAL CLOCK (SK)

The clock input is used to clock all data, address, op-code, and start bits into or out of the EEPROMs. SK clocks both input and output on the rising edge only, the falling edge has no effect on the devices. The only function it is not necessary for is the Busy/Ready Polling which is an asynchronous function.

Since SK is gated by ship select, it is a "Don't Care" any time chip select is low. It is also don't care prior to a start bit being clocked in and during Busy/Ready Polling. During these conditions Data-In (DI) must be held at a low level, otherwise a start bit will be interpreted.

If it is desirable to insert additional clock cycles during a instruction sequence for the purpose of byte aligning the data, there are several places in the data stream they may be inserted as described below:

— On any instruction, zeros can be clocked into the DI input before the start bit. Any number of clock cycles may be added if Data-In (DI) is held at zero. The first 1 clocked in will be interpreted as the start bit. This requires special precautions if a bidirectional data bus is used (Data-In tied to Data-Out) as the Busy/Ready Polling will interfere with the Data-In if it is not cleared out at the end of each programming cycle. See Section 2.3, THREE WIRE BUS, for more information.

— During a Read instruction, it is allowable to continue to clock the device after the 16 bits of data has been clocked out. In the case of the NM93CS family this will cause the memory to increment to the next register and present its contents on the Data-Out pin. In the case of all other devices, whatever was present on the Data-In pin will become present on the Data-Out pin (Fall thru). Refer to *Figure 1,* Block Diagram.

— During a Write or Write-All, additional clock cycles may be added after address A0 and before the valid data. The EEPROM will write into the memory the most recent 16 bits, or in the case of the NM93C46A, the most recent 8 bits or 16 bits depending on the status of the ORG input. Adding additional clocks after the valid data will cause the data to be misaligned. In the case of the NM59C11, the device counts the data bits clocked in and automatically enters the programming mode when it receives a full data field, therefore bits cannot be inserted between A0 and valid data.

— During the EWEN, Erase, Erase All, EWDS, WEN, WDS cycles, it is not necessary to clock in a data field, although it is mandatory to clock in a complete address field, even if the addresses are "Don't Care". Additional clocks can be added after the address field.

2.1.3 DATA-IN (DI)

The Data-In input receives the Start-Bit, Address, and input data in a serial stream, each bit clocked in on the rising edge of SK. DI is gated by the chip select to provide a high degree of noise immunity. As shown in the block diagram, Data-In is routed to both the instruction shift register and the data shift register. When the start bit is clocked into the last bit of the instruction register, the clock is switched to the data register to receive input data and clock data out simultaneous. The Data-Out remains in high impedance unless a read cycle or Busy/Ready status is being done. The safest state is to keep the Data-In pin in a low level as a start bit is a high level.

2.1.4 DATA-OUT (DO)

The Data-Out (DO) output sends read data onto the microwire bus and is clocked out on the rising edge of SK. It also carries the programming status after a programming cycle which is an asynchronous function that does not require the clock. At all other times the Data-Out is in the high impedance state. During a Read cycle, the Data-Out output begins to drive actively after the last address bit (A0) is clocked in. During the Busy/Ready polling it begins to drive active after chip select is raised to a high level.

During the Busy/Ready Polling, the Data-Out output drives low while the device is still in the internal programming cycle. After the EEPROM has completed the internal programming cycle, the Data-Out pin will drive high when chip select is high. Subsequently, if chip select is brought high again, Data-Out will again drive high indicating it has completed the programming cycle. To clear the Busy/Ready Polling it is necessary to raise chip select and clock in a start bit. Once the start bit is clocked in, Data-Out will return to the high impedance state. It is not necessary to continue with a cycle after this start bit has been clocked in, although it is permissible to start a new cycle with this start bit. This clearing of the Busy/Ready status may be necessary if a bidirectional data bus is used (Data-In tied to Data-Out) as the Data-Out output will interfere with the new data being presented on the Data-In input.

2.1.5 PROGRAM ENABLE (PE)

The program enable (PE) input will enable all programming cycles when it is held at a high level during the duration of a programming cycle. Conversely, it will disable all programming, including programming of the protect register, while it is held low. This input has no affect on any other cycle, so it may be permanently tied high or low, or may be used in an active mode. This input is available on the NM93CS family only.

2.1.6 PROTECT REGISTER ENABLE (PRE)

The protect register enable (PRE) input is used to switch between memory operations and protect register operations since the same op-codes are used for both. With the PRE input high, the op-codes define operations in the protect register, with the PRE input low, the op-codes define operations in the memory. This pin may be tied high or low, or used in the active mode. This input is available on the NM93CS family only.

2.1.7 ORGANIZATION (ORG)

The Organization input (ORG) is used to control the internal organization of the memory. The two selectable organizations are 16-bit words and 8-bit words. Simply by holding the ORG pin at a high level, 16-bit words are selected, by holding the input at a low level 8-bit words are selected. When in the 8-bit mode, one additional address bit is required in the instruction sequence since the depth of the memory is doubled. This input is available only on certain device types, refer to the individual datasheets.

2.1.8 STATUS (RDY/BUSY)

The status output indicates the programming cycle status after a programming cycle. When the device is in the programming mode and therefore cannot accept any other cycles, this pin will be low. After completion of the cycle the STATUS pin will be driven high. When this function is present, the Busy/Ready Polling is not available on the Data-Out

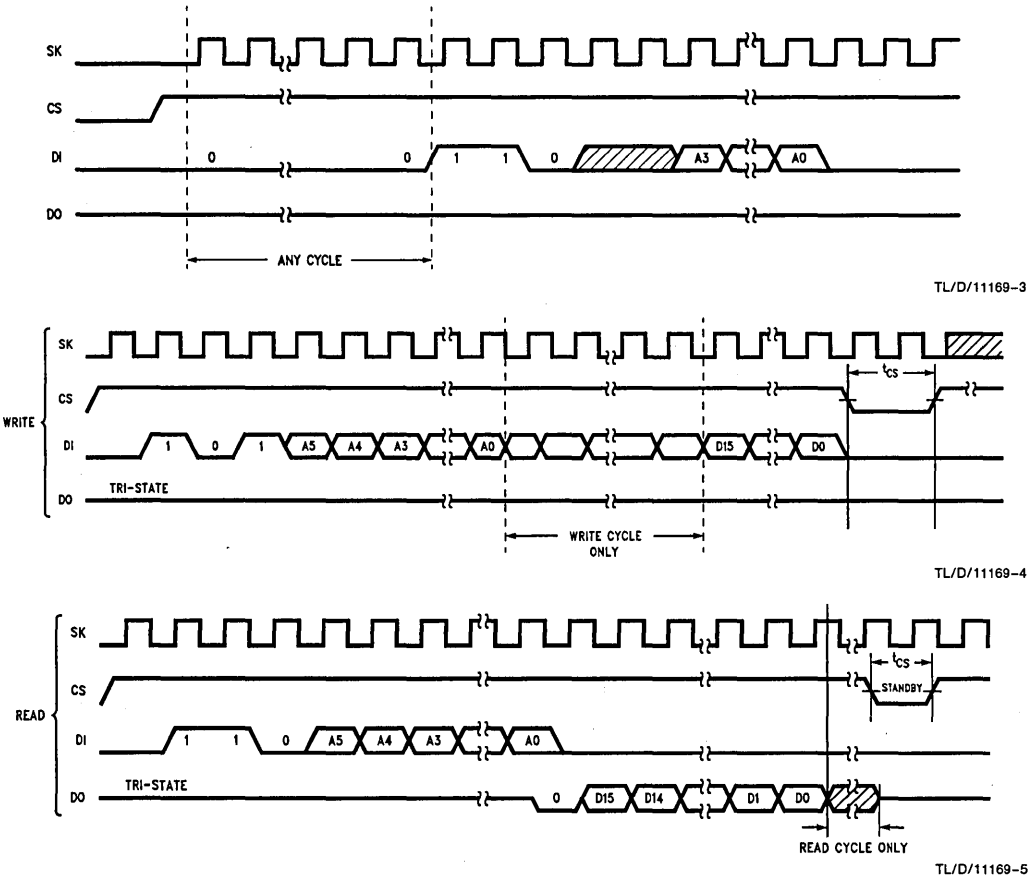

FIGURE 3. Possible Locations for Additional SK Cycles

output. In some systems, particularly those using a bi-directional data bus, this can simplify interfacing by eliminating the possible contention between the Ready indication and the incoming data from the host device. This output is available only on certain device types, refer to the individual datasheets.

2.2 FOUR WIRE BUS

The 4 wire bus is the simplest interconnection between the EEPROM and the host device. In most cases the only signals necessary to provide are clock, chip select, Data-In and Data-Out as shown in *Figure 5.* The PRE, PE, ORG, and STATUS pins are not shown as they are variations on this and the 3 wire bus connection. Multiple devices can be connected to the microwire bus, the only limitations being loading and available chip select means. In some systems it is necessary to have a bi-directional data line as described below in 3 wire bus.

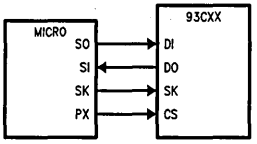

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FIGURE 5. Four Wire Connection

2.3 THREE WIRE BUS

The 3 wire bus operates in the same mode as the 4 wire bus with the exception that the Data-In and Data-Out pins on the EEPROM are tied together. When using this connection, there are two precautions that need to be observed.

— When Data-In is tied to Data-Out, there is a possible conflict between address A0 in the instruction sequence and the dummy bit. This only occurs during a READ cycle. This is not harmful to the device and the internal circuitry of the EEPROM guarantees that the device will function properly under this condition. To decrease the noise created by the condition, a resistor may be placed in the locations indicated in *Figure 6.* The timing diagram in *Figure 7* shows the bus conflict.

— The second possible area of conflict occurs when the Busy/Ready status is on the Data-Out output. Since the device will continue to indicate a Ready status indefinitely after a programming cycle (until a start-bit is clocked in), this can conflict with the beginning of the next cycle if leading zeros are clocked in (See *Figure 7*). The solution is to either use a separate cycle to clear the Ready bit or to eliminate any leading zeros from the instruction sequence. If the Busy/Ready Polling is not used in the application, the easiest solution is to use the NM59C11 that does not have the polling on Data-Out but has it on a separate output.

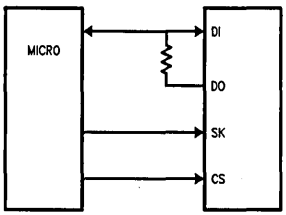

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FIGURE 6. Three Wire Connection Showing Optional Resistor

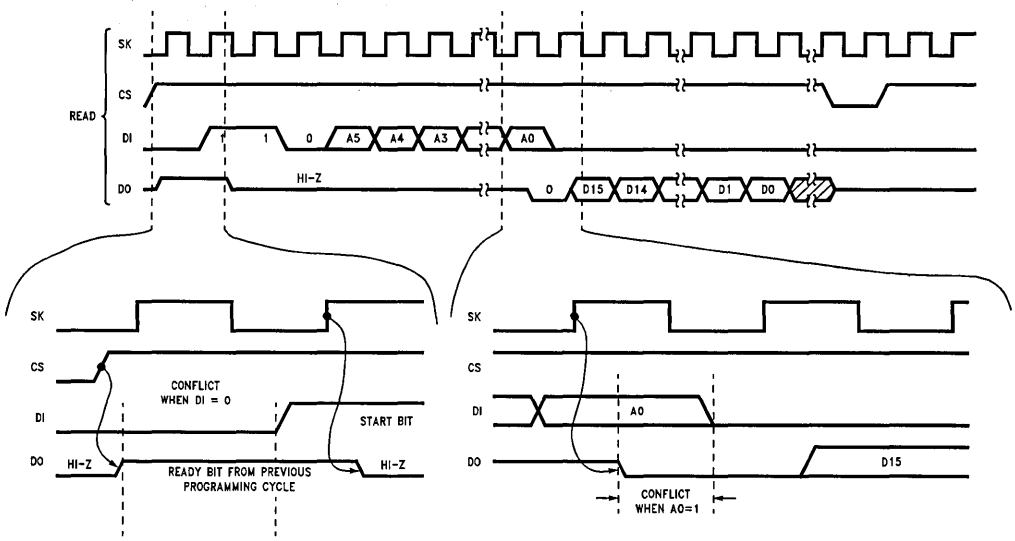

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FIGURE 7. Three Wire Connection Bus Conflict Areas

3.0 Timing Considerations

The following information describing the Microwire bus timing must be used in conjunction with the datasheet as it is an expansion and clarification of the datasheet. First, the basic timings with respect to the clock (SK) will be described, followed by instruction sequence timing, and finally, specific information in each instruction sequence.

3.1. BUS TIMING

The synchronous data timing shown in *Figure 8* is similar to that shown in the various datasheets. There is one significant modification to the timing specification though, the chip select (CS) hold time is referenced to the rising edge of the clock rather than the falling edge. With this modification, the hold time specification must be changed to be the same as the minimum clock (SK) high time. Other significant points are:

— The only active edge of the clock is the rising edge.

— The only time the clock is necessary is when clocking data into or out of the EEPROM. It is not necessary during Busy/Ready Polling.

— The clock may be left in either the high state or low state between cycles. It is safer to leave the clock in the low state.

— When chip select (CS) is high, clock (SK) is a critical signal. With the exceptions noted in Section 2.1.2 tilted SERIAL CLOCK (SK), no additional clock cycles or noise that crosses the V_{IH} or V_{IL} thresholds can be tolerated.

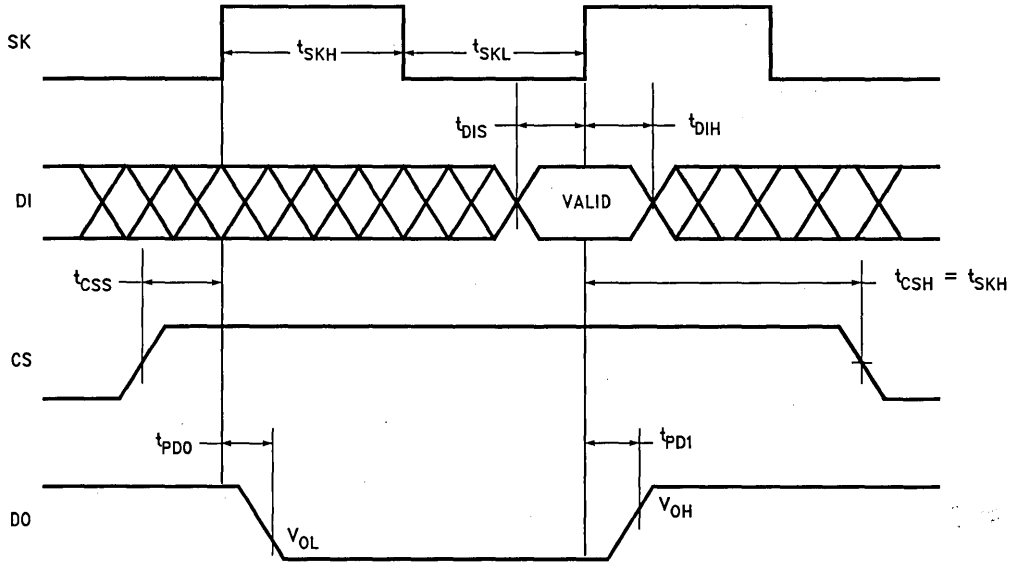

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FIGURE 8. Synchronous Timing

3.2 INSTRUCTION SEQUENCE DESCRIPTIONS

3.2.1 READ CYCLE

The READ cycle requires the host to raise chip select (CS) and then clock in thru the Data-In (DI) pin a start-bit, op-code, and address. Following clocking in the last address bit, the Data-Out (DO) output comes out of the high impedance state and drives a low level on the output. This is referred to as the dummy bit and is a good indication that a READ mode has been successfully entered if difficulty is encountered during initial debug of a system. The dummy bit is clocked out of the EEPROM on the same rising edge of SK that clocks in the last address bit, A0. This is shown in *Figure 9.*

3.2.2 SEQUENTIAL READ

Sequential read is a read mode available only on the NM93CS family. It is entered by entering a READ cycle and clocking out the first 16-bit word. After reading the first 16-bit word if chip select (CS) is kept high, address A + 1 may be clocked out followed by address A + 2 and so on. When the maximum address is reached, the memory continues in the sequential read mode at address 0. In this manner, the host may operate the memory in a continuous loop read. When initiating a SEQUENTIAL READ, the first data word is proceeded by a dummy bit as in a standard READ, although the dummy bit is supressed in all subsequent data words as shown in *Figure 9.*

3.2.3 ERASE AND ERASE ALL

The ERASE cycles return the contents of the EEPROM to a clear state which is read as 1's. It is not necessary for any of the CMOS EEPROM described in this article, and is included in the NM93C family, NM93C46A, and NM59C11 only for compatibility with older devices that require erasing. It is recommended that the erase cycles be eliminated from the instructions to simplify the code, speed up writing and to improve the endurance obtained in the application. These modes are entered by clocking in a start-bit, op-code, and address. It is not necessary to clock in the data field as it is assumed to be all 1's. It is necessary to clock in the address, even in the case of ERASE-ALL where it is "don't care" in all except the first two bits of the address field which is used as additional op-code bits. After the full address field has been clocked in, chip select must be returned to a low level in initiate the erase cycle. In all devices, except the NMC9306, programming completion can be determined by Polling as shown in *Figure 4,* or a simple 10 ms timeout will guarantee programming is complete if polling is not used.

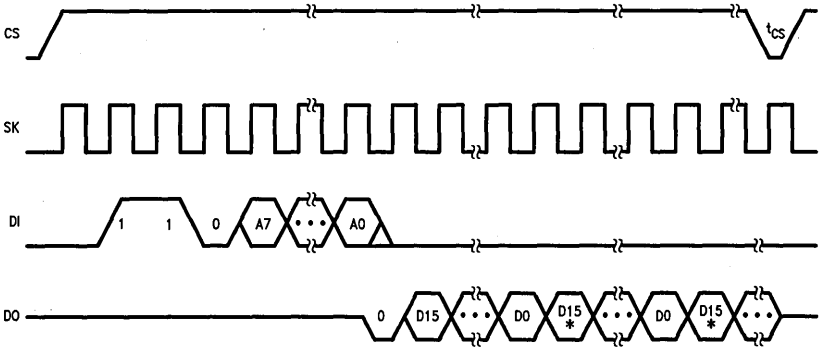


FIGURE 9. Sequential Read Sequence

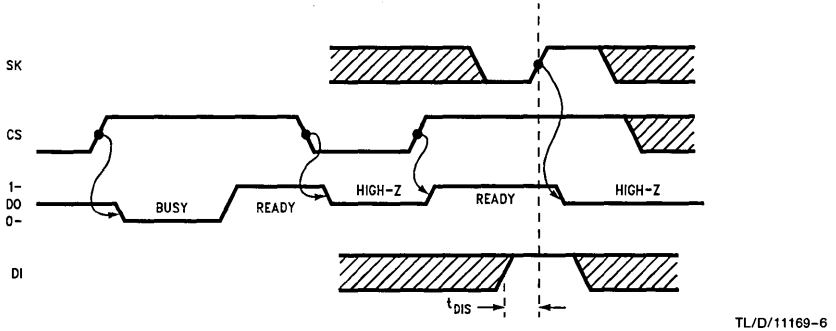


FIGURE 4. Busy/Ready Polling Sequence

3.2.4 WRITE AND WRITE ALL

The Write and Write All cycles will write a specified data word into the specified address, or in the case of Write All, the same data pattern will be written into all locations. In all devices a new data pattern may be directly written over an existing data pattern without erasing the first data pattern. The write mode is entered by clocking in a start-bit, op-code, address, and data. The full address field must be clocked in for the Write All even though it is don't care in all but the first 2 bits. It is also necessary to clock in a full data field to assure correct alignment of data. The write cycle will be initiated after 8- or 16-bit have been clocked into the device in some of the devices and in other devices after chip select is brought low regardless of how many data bits have been clocked in. Refer to the specific datasheets to determine which method is used.

3.2.5 PROGRAM ENABLE AND PROGRAM DISABLE

Program enable and program disable are the instructions that enable or disable writing and, where included, erasing. The instruction name varies depending on the specific device but includes EWEN, EWDS, WEN, and WDS. These instructions enable or disable the entire memory array with a single instruction. All devices power up in the disable mode and once placed in the enabled mode remain enabled until a disable instruction is performed or V_{CC} is cycled. These instructions provide the most basic level of data protection. Although since most lost data is the result of the host device becoming uncontrolled and performing the "Program Subroutine" it may be helpful to structure the software such that the enable command is not included in the "Program Subroutine" but is in a separate subroutine. If a greater degree of data security is needed, a NM93CS family device is recommended, or other more elaborate schemes involving redundant data storage and polling.

3.2.6 PROTECT REGISTER READ

The protect register read (PRREAD) command is the same as a word read command except the input PRE must be held at a high level and the address is don't care. In spite of the address being don't care, the entire address field must be clocked in. On the Data-Out pin the contents of the protect register will be clocked out MSB first descending to LSB.

3.2.7 PROTECT REGISTER ENABLE

Similar to the programming enable instructions described above, the PREN instruction is necessary to perform any programming instruction the affects the Protect Register. Unlike the enable instructions described above, a PREN must immediately proceed each programming instruction that involves the protect register. The Protect Register programming instructions are PRCLEAR, PRWRITE, and PRDS.

3.2.8 PROTECT REGISTER DISABLE

The protect register disable instruction permanently disables any further programming instructions to the protect register. Therefore it can only be performed once in the lifetime of a NM93CS device. The purpose of it is to permanently configure a portion of the EEPROM as true ROM and a portion as Read/Write EEPROM. Great caution should be exercised prior to executing this instruction as there is no second chance. It is performed by sending a start-bit, op-code and an address field of all 0's while both the PRE and PE inputs are at a high level. This instruction must be immediately proceeded by a PREN instruction.

3.2.9 PROTECT REGISTER CLEAR

The protect register clear instruction will clear the contents of the Protect Register making the entire contents of the EEPROM alterable only if the PRDS instruction has not previously been executed. This is done by clocking in a start-bit, op-code, and address field of all ones. This instruction must be immediately proceeded by PREN instruction and requires that both PRE and PE inputs be held at a high level.

3.2.10 PROTECT REGISTER WRITE

The Protect Register write command (PRWRITE) allows the host to write the protect register with the address where the memory is to be segmented into ROM and EEPROM. The defined address is the first ROM address and the ROM field then continues to the top of memory. To execute this command a start-bit, op-code, and address must be clocked in, the address field containing the memory address that defines the ROM/EEPROM boundary. The PRE and PE inputs must be held at a high level.

3.3 INTERFACING SOLUTIONS

When interfacing serial microwire EEPROMs to microcontrollers there is an apparent conflict that occurs when selecting clock polarity and phase. This can be easily overcome in most situations, although when using some microcontrollers that do not allow selection of either clock polarity or clock phase, the only solution may be to resort to bit set and bit reset instructions to interface to the EEPROM rather than use of the serial interface provided on the microcontroller.

In the instance where there is a dedicated serial interface provided, the conflict typically occurs as follows. *Figure 10* demonstrates an EEPROM READ as this involves data being transferred from the micro to the EEPROM (Start bit, op-code, and address) and data transferred from the EEPROM to the micro (address contents). The conflict occurs in this example when the micros clock sets data up on the falling edge of SK and expects the EEPROM to accept it on the rising edge, but then expects the EEPROM to do the same when it sends data back to the micro.

1. The micro sets up a data bit. A propagation delay after the falling edge the data bit is valid at the EEPROM DI pin.
2. The EEPROM uses the rising edge of SK to clock the data bit into its internal register.
3. When the data direction changes the EEPROM sets the data up starting at the rising edge of SK.
4. The micro attempts to clock the data bit in that was set up on clock edge 3.

This example will work if the micro requires 20 ns or less data hold time after edge 4. If greater than 20 ns is required, an alternate strategy is needed.

1a. The micro sets up the data bit on the rising edge and a propagation delay later it is valid at the EEPROM.

2a. The EEPROM clocks the data into its internal register. The EEPROM requires only 10 ns data hold time, which can normally be guaranteed.

3a. The EEPROM sets the Data-Out up on the rising edge.

4a. The micro clocks the data into it's internal registers on the falling edge of the clock and a minimum data setup and hold time is guaranteed for the micro based on the minimum high and low time of the SK clock used in the application.

It should be noted that in the second example, CS (chip select) is asserted when SK is low. If this cannot be done, the DI input should be low when CS is asserted. If both DI and SK are high when CS is asserted the EEPROM will recognize this as a rising edge of SK. To accommodate this in a design, it is allowable to clock in any number of logic zeros prior to the start bit.

4.0 Conclusion

The serial EEPROM offered by National all share a common structure. Separating them are various features that give benefit to various applications such as the need for a bi-directional data bus or need for one byte word width. There are a number of "tricks" that may simplify interfacing to these which can easily be understood with the help of a functional block diagram. Given this information the overall job of using a serial interface EEPROM will be simpler.

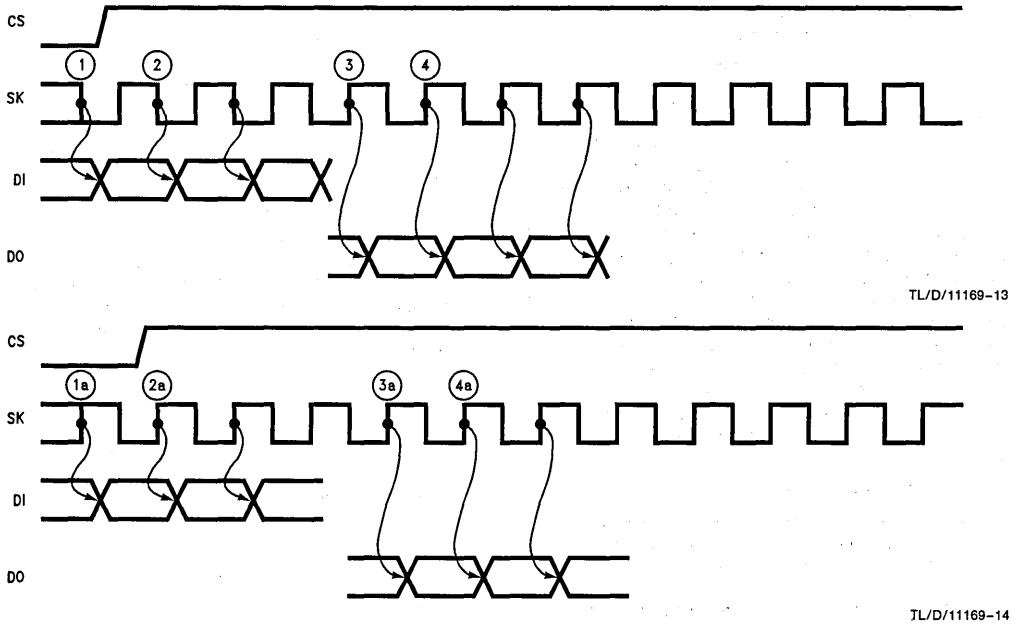


FIGURE 10

Using the NM95C12 CMOS EEPROM with Programmable Switches for Analog Applications

National Semiconductor
Application Note 765
Alfred P. Neves

INTRODUCTION

National's NM95C12 EEPROM programmable switch occupies a unique niche in the switch marketplace. Consisting of a 1024-bit serial input EEPROM with 8 programmable switches, the output can provide either an analog switch or TTL compatible logic functions.

The combination of switch performance and the flexibility offered in the ability to software reconfigure the switching function makes the NM95C12 an excellent device for analog systems requiring switching or multiplexing. Often calibration sequences or multiplexing functions have either required using several IC's or manually shorting and opening printed circuit board connections, until the availability of the NM95C12.

However, the limited analog range of the NM95C12 makes it difficult to use for general analog functions. In order to capitalize on the full capabilities of programmable switches, it is important to understand the appropriate design techniques in level shifting, increasing the output drive capability, and increasing the output signal range. The focus of this application note is to summarize general circuits that perform this function, and thereafter provide a practical transducer measurement system example. The discussion will be solely devoted to extending the use of the NM95C12's switches function, and not on the actual software programming or operation of the IC.

GENERAL DESCRIPTION

A detailed description of the overall operation of the NM95C12 can be found in AN-735, "Understanding National's NM95C12 EEPROM with Programmable Switches", or the NM95C12 data sheet. However, for the sake of completeness, the NM95C12 consists of a 61-word x 16-bit EEPROM array, a 16-bit Initial Switch Register, a 16-bit Switch Configuration Register, a 16-bit Switch Readback Register, four identical blocks of switch logic, programming and power-up circuits and control logic. Essentially, the NM95C12 programmable switch can be easily configured, and reconfigured, for applications including both analog and digital switching functions. 60 internal addresses are available to reconfigure the switch settings on the fly. Upon power-up the Initial Switch Register, address 61, provides a defined set-up state. This operational feature is extremely valuable since it provides an established initial condition for the system.

SWITCH DETAILS

Each switch pair can be configured for either logic functions, or as an analog switch. Functional block details relating control of the switches to the input control logic can be found in Table I of the NM95C12 data sheet. Basically, the logic switch configurations are at standard TTL levels. Also, the analog switch configurations can be looked at as standard MUX switches. Since this note specifically focuses on extending the operating voltage range of the analog switches, the emphasis will be on the analog switches. *Figure 1* summarizes the salient operating features of the switch pairs.

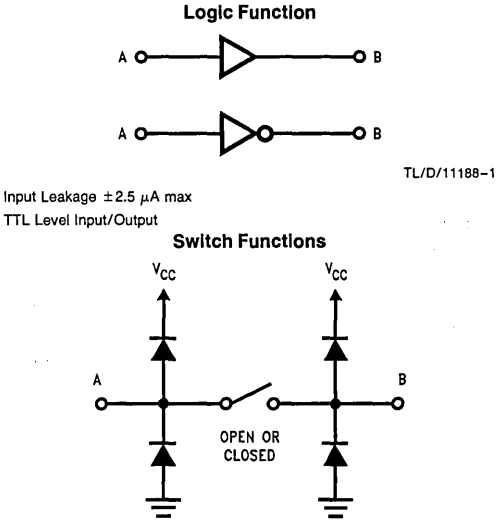
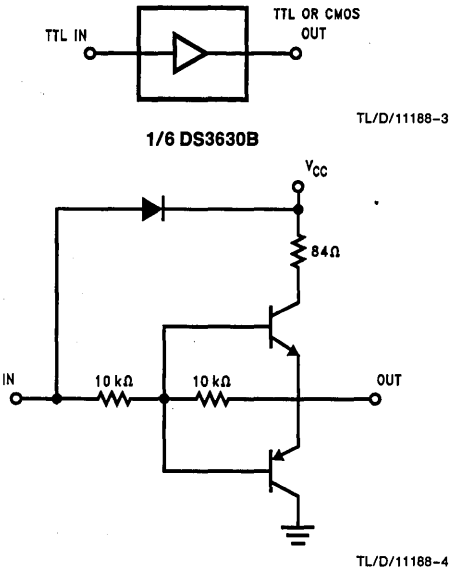


FIGURE 1. The NM95C12 can be Programmed to Configure either Logic Function or an Analog Switch

LEVEL SHIFTING AND EXTENDING THE SWITCHES RANGE

In considering level switching and enhancement of the voltage range for the NM95C12, it is logical to examine some simple level translations that can be solved with commercially available IC's. Examples of simple translation circuits includes the DS1630B Hex CMOS Compatible Buffer shown in *Figure 2*. Where simple translation of TTL output signals to higher levels of output voltage is required (such as CMOS compatible signals), used at the output of logic configured NM95C12 switch, the DS1630B represents a simple solution.



Equivalent Circuit

FIGURE 2. The DS1630B/DS3630B Is a Hex CMOS Buffer Amplifier. It Features Low Power Consumption, and an Output Voltage that can go to 16V (V_{CC}).

An example of a voltage translation is the DS8800 Dual Voltage Level Translator which can be found in *Figure 3*. Custom control of output swing can be established over a 31V range by setting V3, and V2 to the appropriate values. Additional information can be found in the DS8800 data sheet.

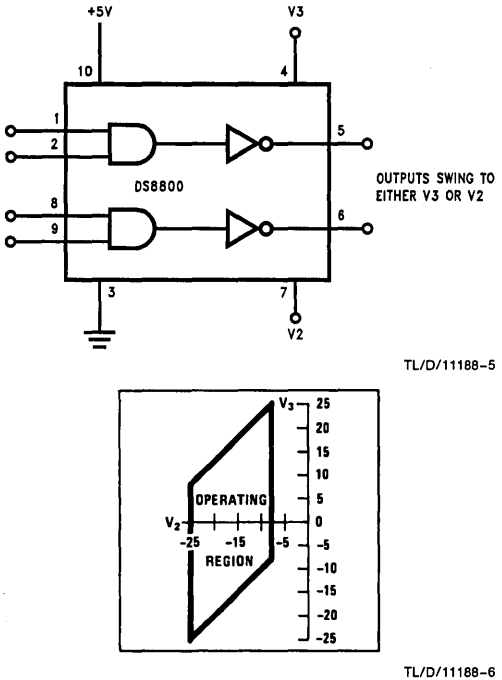


FIGURE 3. The DS8800 Is a Dual Voltage Translator that Is useful for Programming MOS Type Memory, Establishing Bias Voltages, and Driving Transducers. Output Swing Is Limited to 31V.

Figures 4 through *10* illustrate some useful translation circuits that use discrete components to achieve higher output drive than typical monolithic IC's. The circuit in *Figure 4* is similar in functionality to the DS8800. However, wider output swings (limited to BVCeo of the output transistor), and larger sink/source current ability is achieved.

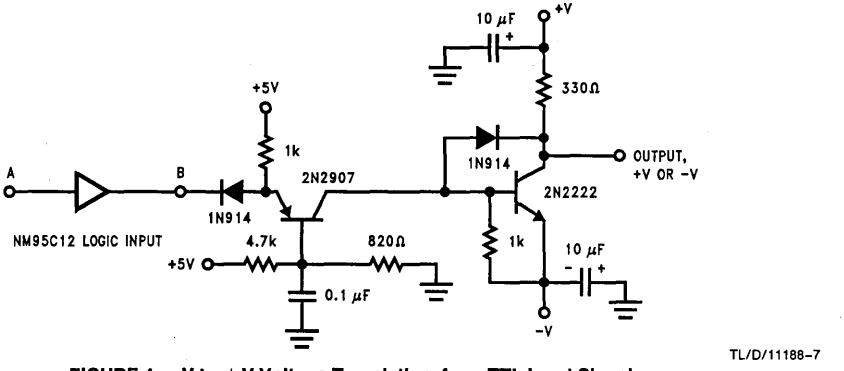


FIGURE 4. −V to +V Voltage Translation, from TTL Input Signal

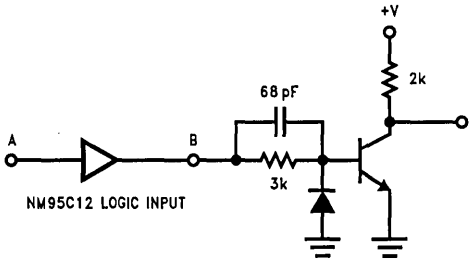


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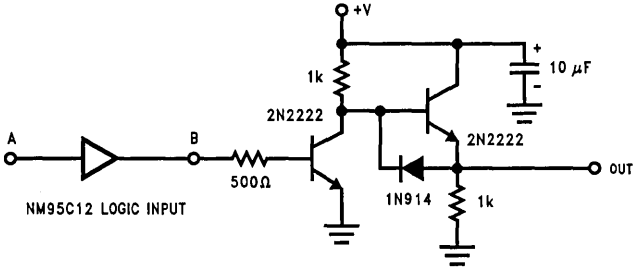
FIGURE 5. A Simple 0 → +V (+V Typically Is 3V → +18V) Level Translation Stage. $I_{SOURCE} > I_{SINK}$



$I_{SINK} > I_{SOURCE}$

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FIGURE 6. High Output Current Sink Level Translation Stage—Excellent for Transducer Bridge Drive

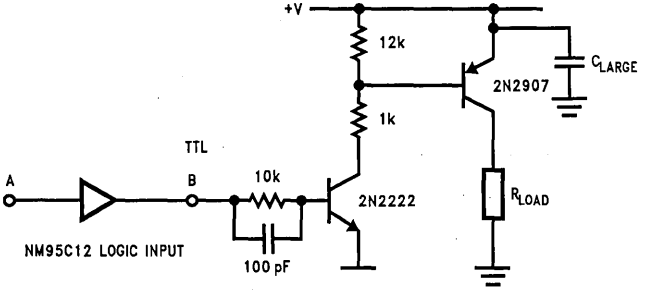

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FIGURE 7. A Simple 0V → +V Switch, from TTL Input

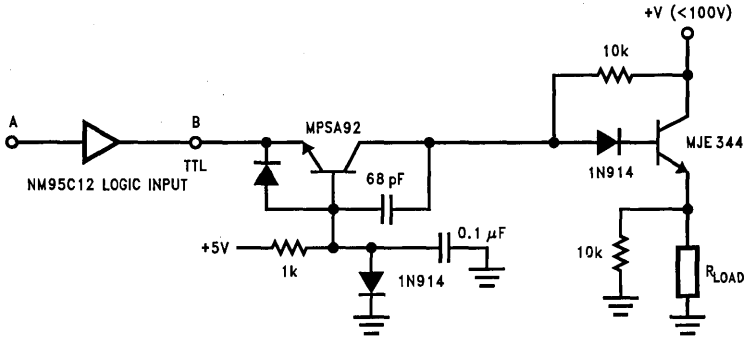

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FIGURE 8. 0V to High Voltage Translation Circuit, from TTL Input

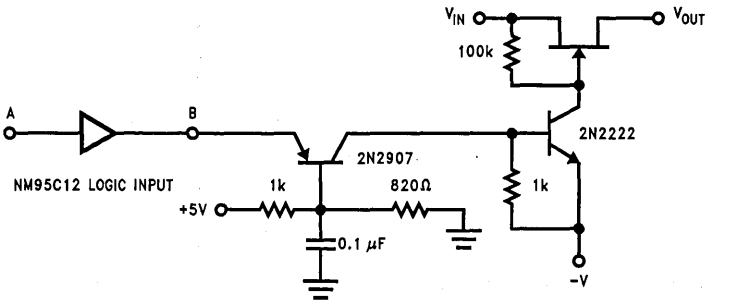

FIGURE 9. Control of FET Switch

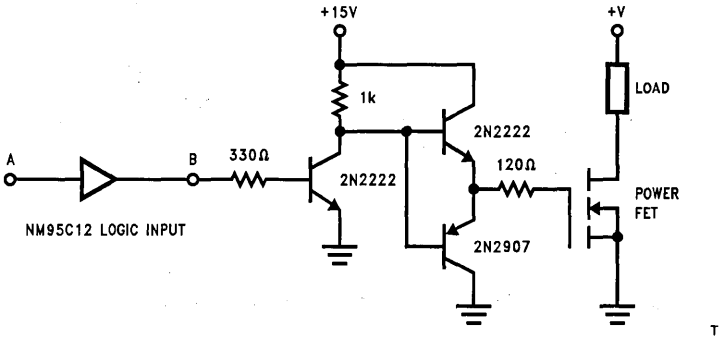

FIGURE 10. TTL Control of Power FET

TWO PRACTICAL EXAMPLES

Bridge circuits play a dominant role in many measurement applications. Typically, providing a trimmed, calibrated output response is usually the goal of a bridge transducer signal processing system. Often this requires calibration, switching for it's operation, and adjustments for operating conditions related to available supply voltage. The NM95C12 provides a software reconfigurable analog system, where manual shorting and opening circuit board traces is not required for either altering the operation of the system, or performing calibration.

Figure 9 shows how the NM95C12 can be used to control a transducer measurement system. By shifting through the 61-word sequence of the NM95C12 operation of the bridge—pulsing or exciting the bridge, sampling with the LF398, and strobing the A/D converter can be performed with the switches, which are configured in the TTL output mode.

Figure 10 illustrates the inherent flexibility in using the NM95C12 for controlling analog applications. One NM95C12 is used as a switch to directly control both the excitation voltage output level and enable to the bridge, provide TTL control signals for nulling the bridge-amplifier offset voltage, and strobe the LF398 sample/hold. Complete control of the transducer measurement system can now be controlled by the reconfigurable memory contents of the NM95C12.

A stable LM185-2.5 reference is used to generate an accurate 2.5V voltage. The 1K, 0.001 μF, 20K circuit provides a soft-start to the transducer bridge. This prevents potential damage to metal-foil type 350 bridge transducers. SW1 must be programmed to either enable or disable the bridge drive. A single-supply, low-power dual op-amp is used to drive Q1 which provides the appropriate bridge drive. Reliability is enhanced by including a 100 mA short circuit current limit.

The circuit is compatible with positive supply voltages extending from +5V to +15V. SW2 can be enabled to alter the output voltage range of the bridge drive. SW3 and SW4, in combination with the LF11333 can be programmed to provide a short to the instrumentation amplifier to null the amplifiers offset.

Since the output range of the NM95C12 switch is limited to a diode drop from the +5V supply line, a LF13333 multiplexer is used to provide switching the bridge output voltage, which will probably exceed this limited voltage range.

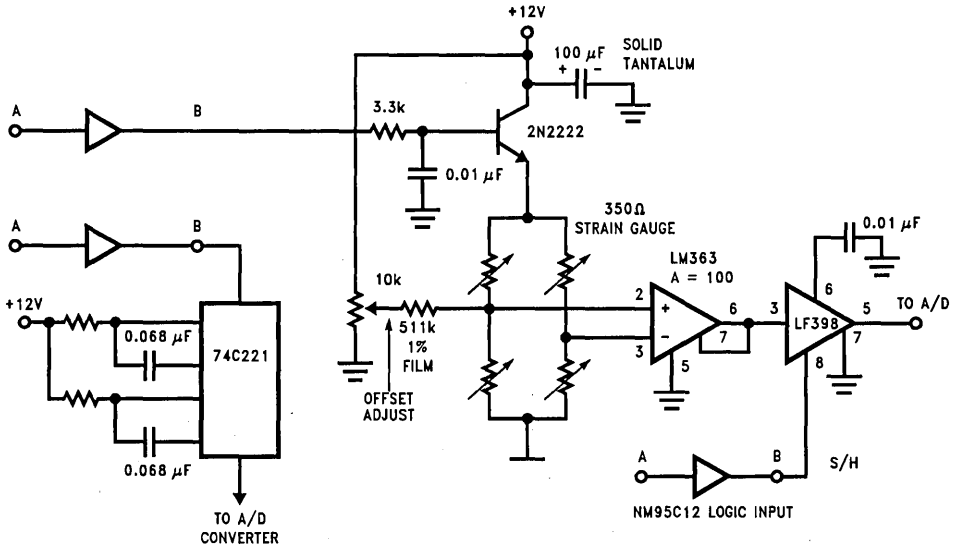

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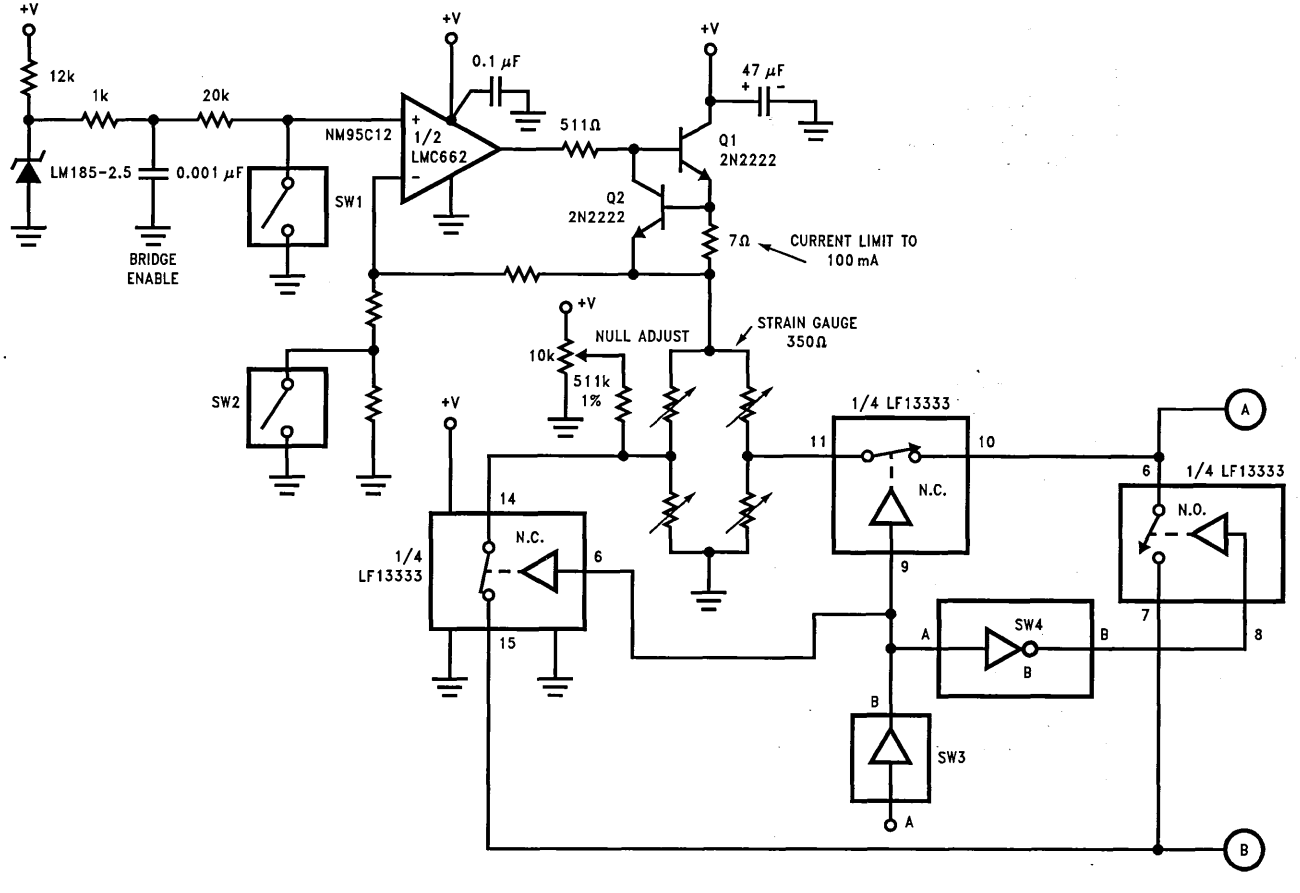
FIGURE 11. Using the NM95C12 in the TTL Output Switch Mode to Control Transducer Bridge Operation



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SWX are Internal Switches to the NM95C12

FIGURE 12. Transducer Measurement System

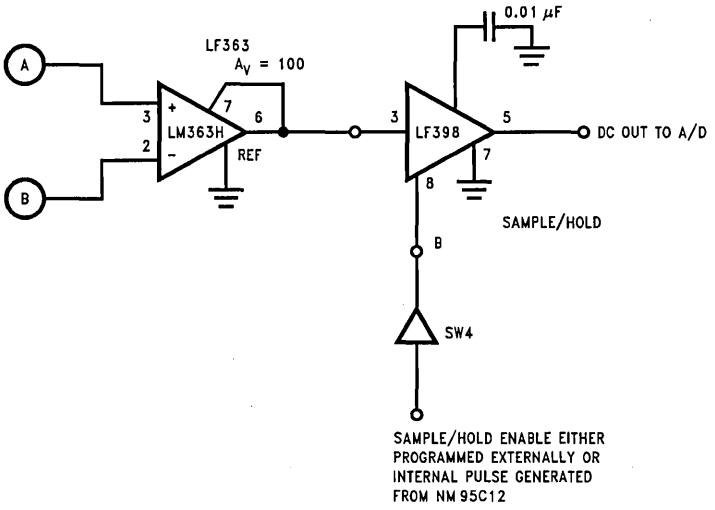

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FIGURE 12. Transducer Measurement System (Continued)

Using the NM95C12 in a Stand Alone Metering Device

National Semiconductor
Application Note 766
Chris Siegl

ABSTRACT

This application gives a detailed description of the use of the NM95C12 in electronic metering key applications where it is desirable to have a status display without having the key connected to any device. By using the NM95C12 such functionality can be obtained without using a microcontroller in the key. This can have significant cost, size and power impact.

INTRODUCTION

Metering keys are becoming quite common now for use on copying machines in large corporations for departmental accounting purposes as well as in the flood of neighborhood copy centers and resource facilities shared by a number of businesses. The simplest implementation of such a device is a simple mechanical counter with an advance solenoid—as each copy is made a pulse advances the counter. This approach suffers a number of drawbacks including low reliability, easy to tamper with, bulky and unable to itemize between different uses or equipment. These types of devices are no longer just used for copying machines—fax machine usage, word processor usage, plotters, and laser printers are now becoming part of the shared resources of a corporation or among a number of businesses as well as such services being incorporated into the neighborhood copy center. While the mechanical counter could still be used in such applications where the device under use could increment the counter at different rates depending on the type of usage, a different counter could be used for each service; generating an itemized receipt for the user becomes very cumbersome.

By using a non-volatile memory in the key device an itemized list can be kept of the services used. The value of the services used could also be tracked and the key terminated when a certain limit is reached. The key device could function like a debit card where the user gets a certain amount of credit stored in his card—when it is all used up he must go back for more at which point a cash register or other device with a printer and a receptacle for the key device would print an itemized list of usage and optionally erase the memory and store a new credit amount. The disadvantage of this approach when compared to the mechanical counter is the lack of an indication of the remaining credit or usage to the user. One way to solve this problem is to include a display on the device being used to display the current credit information. This has the disadvantage that the user must have the key device plugged into a service device to find his credit status. Another approach is to include a microcontroller in the key device along with a display, a battery and a switch to activate the display. If the battery fails, information in the key is lost. By using serial E²PROM memory devices such as the NM9306, NM93Cxx or NM93CSxx families solves the information retention problem when the battery fails, but we still need the microcontroller if the key device is to have an active display without connection to another device.

Enter the NM95C12 serial E²PROM with eight programmable outputs which are set to their stored values on power up. This device is not only non-volatile, but is small, inexpensive, simple to use and does not require a microcontroller in the key device.

THE NM95C12

The NM95C12 is a 1024-bit, CMOS E²PROM with 8 programmable outputs. The 1024 bits of memory are divided into 60 registers of 16 bits each and each register can be individually accessed. Registers 61–63 are dedicated to storing the programmable output settings. Each output may be programmed to provide either a HIGH or a LOW output level or these outputs may also be programmed to form four individual pairs of SPST switches. In this application we will only be programming these pins as HIGH or LOW outputs but there are many other applications where a SPST switch or switches would be useful.

Other features of the NM95C12 include a very low operating current (less than 4 mA), software write protection, self timed write cycle (erase cycles not necessary) with an endurance of over 40,000 writes per register and at least 10 year data retention.

Interfacing to the NM95C12 is done through the on-board MICROWIRE™ port; this port consists of four signal lines: a serial clock (SK), serial data input (SI), serial data output (SO), and chip select (CS). MICROWIRE is supported in hardware in the COP400, COP800 and HPC™ microcontroller families. MICROWIRE can also be easily implemented on most microncontrollers and microprocessors in software. The TP3064 and TP3065 implement a MICROWIRE hardware interface to various standard microprocessors.

DISPLAY INTERFACE

The NM95C12 has 8 programmable outputs. The switch configuration register (SCR) controls these outputs in pairs, four bits per pair. Table I shows the different switch configurations possible for each pair. In this application we are only interested in modes 0, 1, 2 and 3. Because the NM95C12 has a much greater current sinking capability than sourcing we will configure our LED displays with their cathodes to the output port. A LOW output results in a lit LED. *Figure 1* shows a bar graph display being driven by the NM95C12. A single resistor SIP can be used to limit the current to the LEDs. The configuration register looks like *Figure 2* with a, b, c . . . h representing the LED segments. To light a particular segment the appropriate bit in the SCR register must be set to 0. This register is set to the contents of the word stored in the E²PROM's location 61 at power-up. The SCR register itself is located at address 62 and can be written to directly without affecting the E²PROM location 61 and the new contents of the SCR register will be lost on power-down. At the next power-up the contents of location 61 will again be stored in the SCR.

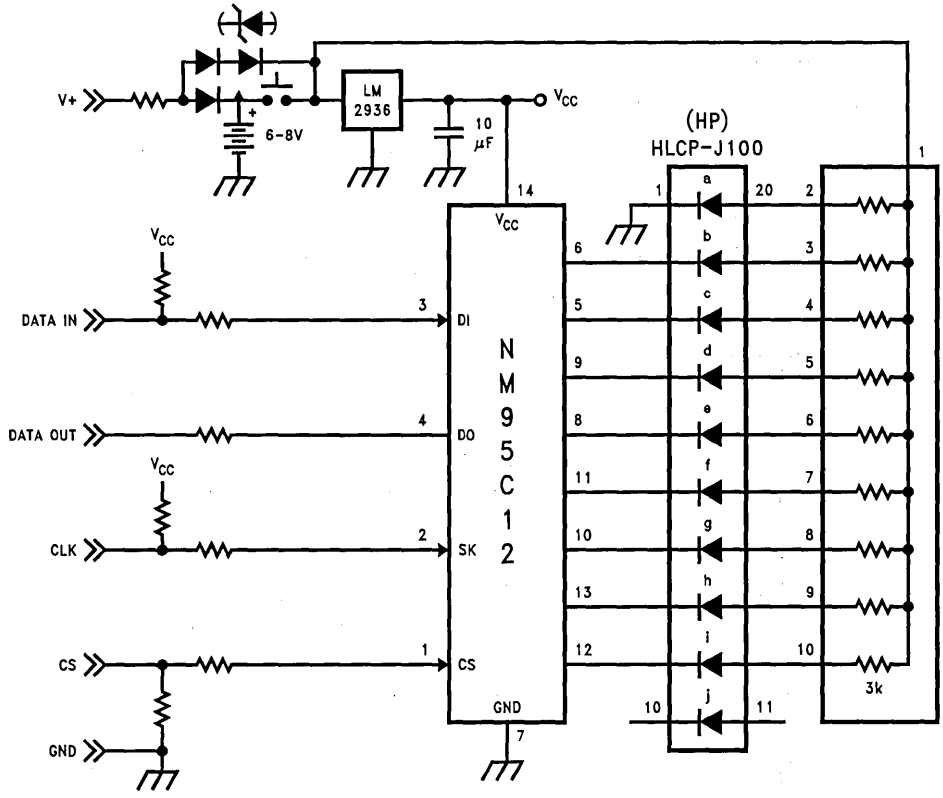


FIGURE 1

Switch Configuration Register (SCR)

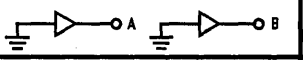
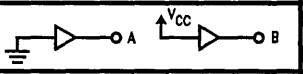
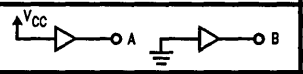
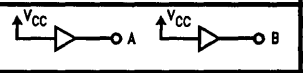
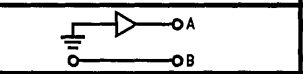
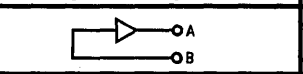
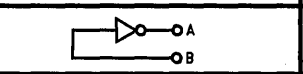
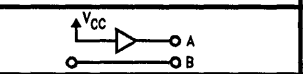
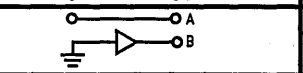
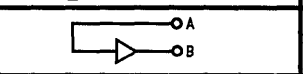
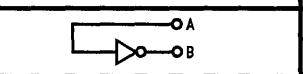
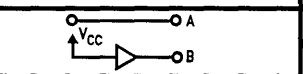
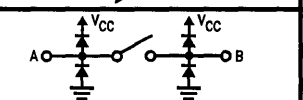
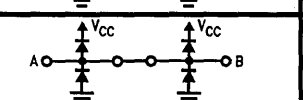
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z	Y	X	W	Z	Y	X	W	Z	Y	X	W	Z	Y	X	W
		Switch 4				Switch 3				Switch 2				Switch 1	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	a	b	0	0	c	d	0	0	e	f	0	0	g	h

FIGURE 2. SCR Configured to Drive Bar Graph (a 0 in a, b . . . h turns on appropriate segment)

The circuit in *Figure 1* uses some tricks to maximize the battery life. The LM2936 (low dropout; ultra-low quiescent current 5V regulator) was used to regulate the battery voltage down to 5V for the NM95C12. By bypassing the regulator for the +V connection to the resistor SIP the current through the regulator only feeds the NM95C12 which in its quiescent state (with all inputs at CMOS logic levels) is <50 μA the dropout voltage of the LM2936 is <0.1V. To have the LEDs operate correctly it is important to keep the battery voltage under 8V to 9V otherwise the LEDs which should be off will get turned on through the protection diodes (see modes 12 and 13 of Table I) not to mention the increase in current discharging the battery. Another approach would be to power the LEDs from the regulated +5V. Now the thing to watch out for is the current limit of the LM2936; exceeding 65 mA could force the regulator to go into current limit.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		$A = \overline{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		$B = \overline{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

All the circuits in this application note use very low current Hewlett Packard displays (they are specified for operation at 1 mA per segment) to maximize battery life. Other displays at higher currents can be used but care must be exercised not to exceed the current capabilities of the LM2936 as well as the power dissipation capabilities of the NM95C12 especially if the surface mount package is used at higher temperatures. Another side effect of higher currents in the LEDs is the V_{OL} specification is 0.4V at an I_{OL} of 2.1 mA but will rise with higher I_{OL}s (typically stays well under 1V at 10 mA).

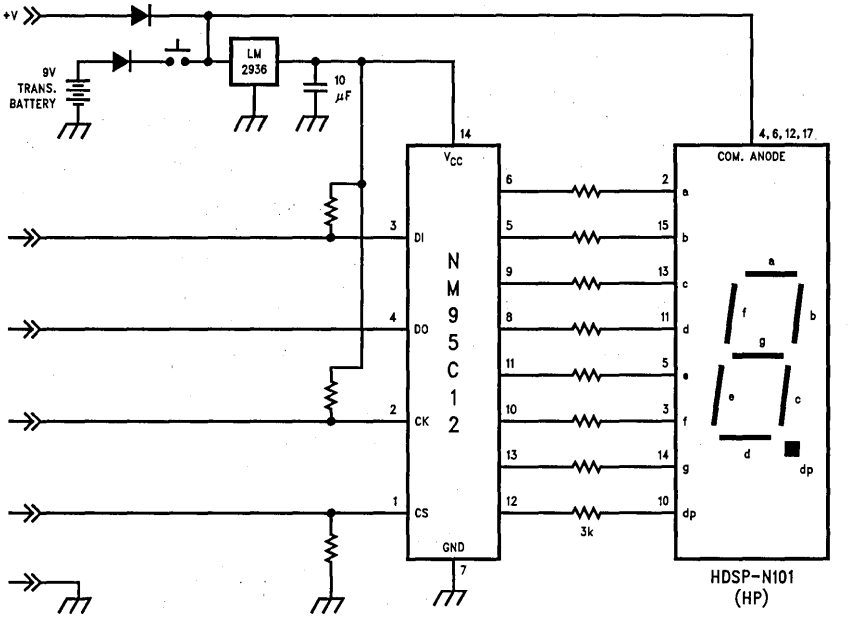
Instead of using a bar graph individual LEDs could be used in much the same manner. The length of bar graph lit or number of LEDs lit would show the amount of credit remaining. Another approach would be to use a 7 segment display. *Figure 3* shows such a circuit. The button is pressed when the user wishes to see the display. There is a diode bypass of the push button switch so the display is active while the key is plugged into the device under use. The user can monitor his remaining credit while operating the device. The battery is being charged whenever the key is plugged into a device. If the battery should ever go too low to operate, the user just plugs the key into a device for a while to recharge—the contents of the E²PROM are not lost. The rechargeable battery could be replaced with a 9V transistor battery (typical voltage on these is 7V to 8V) which will give operating life of multiple months if checked only intermittently. No data would be lost during battery changes. *Figure 3* shows how the key would be configured using the transistor battery. Table II shows the bit combinations for the SCR register to generate the digits 0 to 9. Notice with the 7 segment display we no longer can use a resistor SIP because segment LEDs are all tied to a common cathode. Resistors in this configuration are available in DIPs as well as SOIC.

Applications desiring two digits (credit can now be displayed as percent remaining) can be implemented with two MM74HC4511 display decoder/drivers as shown in *Figure 4*. The MM74HC4511s have a quiescent current of $<80\ \mu A$ maximizing battery life and are available both in DIP as well as SOIC packages. The MM74HC4511 has a maximum supply voltage of 6V so it should be operated from +5V regulated supply as shown in *Figure 5*. Table III shows how the BCD (binary coded decimal) data is configured in the SCR register to display the two digits.

TABLE II

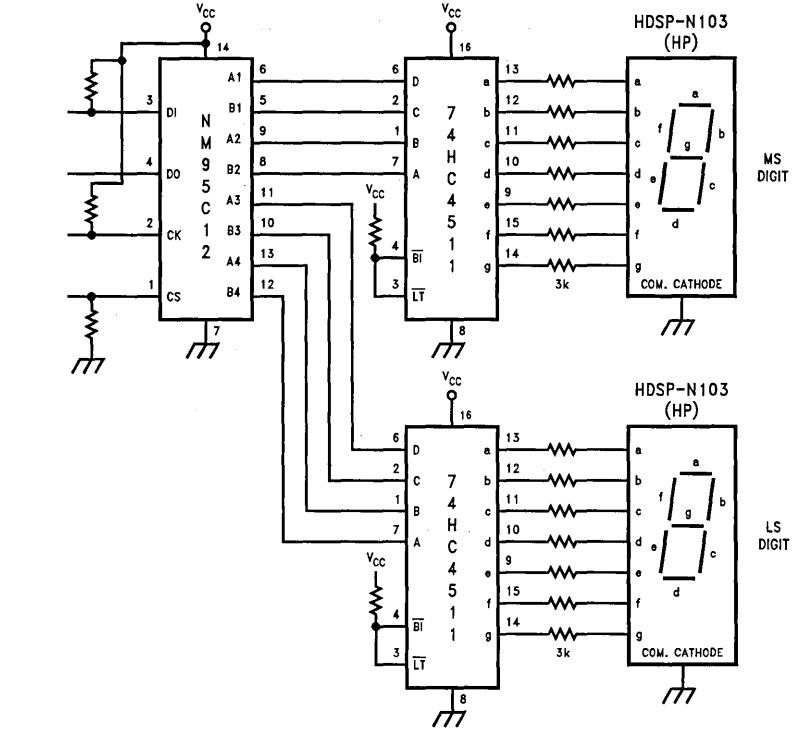
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	a	b	0	0	c	d	0	0	e	f	0	0	g	dp	
0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0
0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	1	0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	0	3
0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	4
0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	5
0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0	6
0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	7
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	8
0	0	1	1	0	0	1	0	0	0	0	1	0	0	1	0	9

TL/D/11189–3



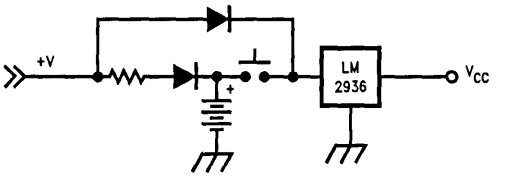
TL/D/11189-2

FIGURE 3



TL/D/11189-4

FIGURE 4



TL/D/11189–5

FIGURE 5

TABLE III

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	D	C	0	0	B	A	0	0	D	C	0	0	B	A	
MS DIGIT								LS DIGIT								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	01
0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	43
0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	95

TL/D/11189–6

If there is a need to display the number 100 as well, this can be accomplished with the addition of just one quad NOR gate as shown in *Figure 6*. Here we get a little tricky. By adding some gating to the two most significant bits of the most significant digit a coding can be worked out that gives a zero code to the most significant digit driver at the same time as driving through another gate the hundreds digit. *Figure 7* shows the logic along with a table of the states. If the 2 most significant bits of the most significant digit are inverted before going to the SCR register the right numbers will be displayed. To display 100 the SRC is loaded with all zeros. Table IV shows some example numbers.

MODULE INTERFACE

The metering device or key must connect to the service device through some type of connector. The simplest approach is to bring out the MICROWIRE port through a connector to a processor or microcontroller in the service device. The MICROWIRE port consists of four signal lines; a serial clock (SK), serial data input (SI), serial data output (SO), and the chip select (CS). When CS is LOW the chip is powered down into standby mode (outputs A1 through A4 and outputs B1 through B4 are still driven even while in standby) and accesses on the MICROWIRE port are disabled. So while the metering device is unplugged from the service device we want this signal low, therefor this signal has a pull down resistor. To begin an access to the NM95C12 the CS is first set high by the service device then a high start bit is on DI and clocked into the NM95C12 by a low to high transition on SK (see *Figure 8*) the start bit is then followed by opcode and address (see Table V) with SK low to high transitions for each bit. In the case of a read instruction, subsequent toggling of the SK line causes the addressed data to be shifted out on DO. Data should not be sampled on DO on the low to high transition of SK as this is when the bit is shifted out. On write operations they must be preceded by the write enable instruction (WEN). In the write instruction (WRITE) the data follows right after the address. (see *Figure 9*).

The MICROWIRE interface is supported in hardware on the COP400, COP800 and HPC microcontroller families. MICROWIRE can also be easily implemented on most microcontrollers and processors in software. Application Note AN-507 "Using the NMC93CSxx family" covers the details of how to communicate with these types of serial memory devices from various microcontrollers. The TP3464 and TP3465 implement a MICROWIRE hardware interface to various standard microprocessors.

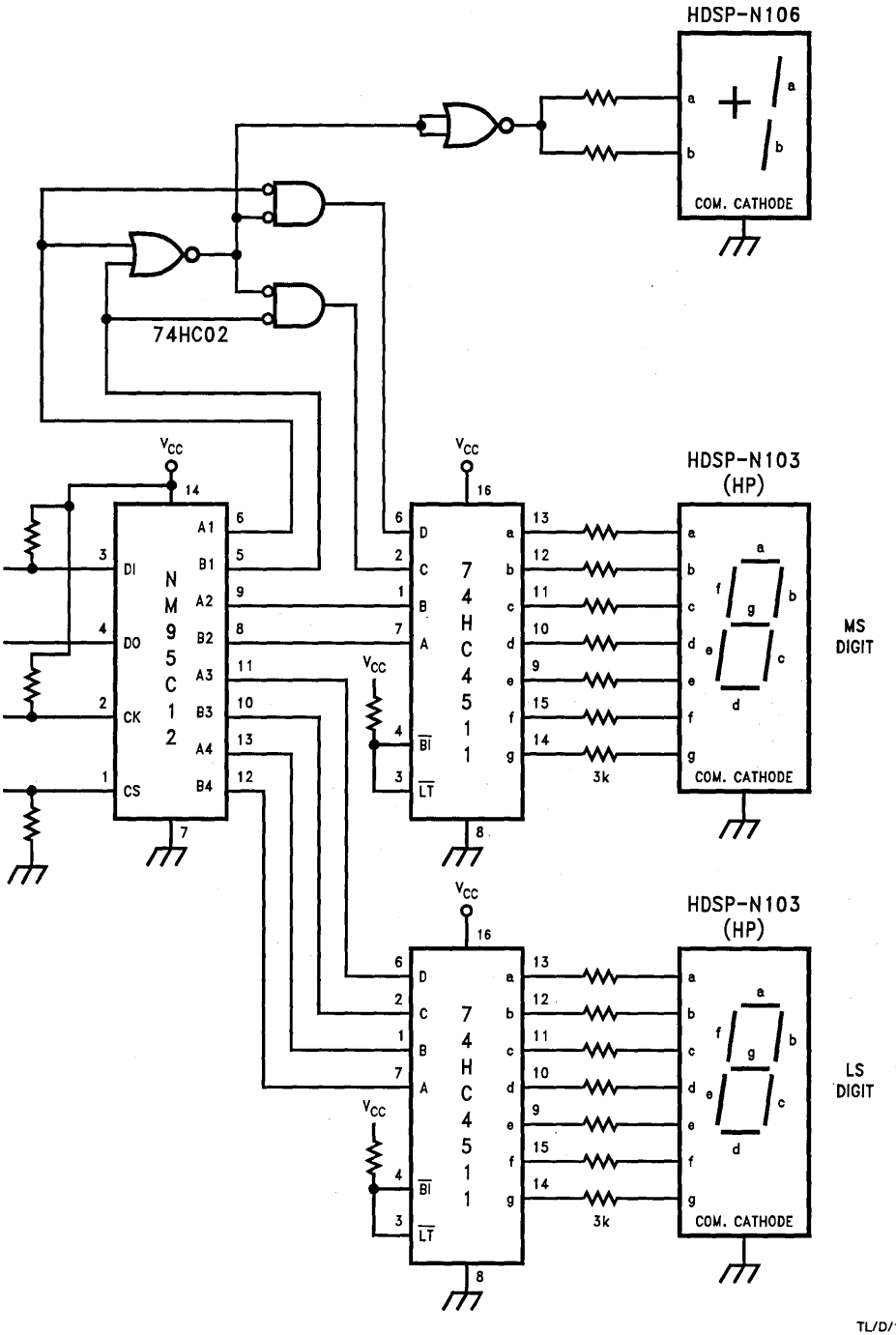
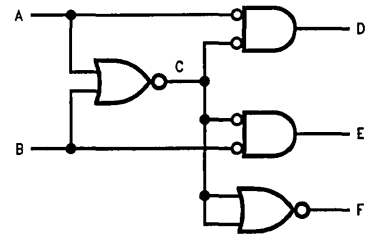

HDSP-N106
COM. CATHODE
74HC02
V_{CC}
NM95C12
DI
DO
CK
CS
A1
B1
A2
B2
A3
B3
A4
B4
74HC4511
BI
LT
HDSP-N103
(HP)
3k
MS
DIGIT
LS
DIGIT
TL/D/11189-7

FIGURE 6

If there is a need to minimize the number of contacts in the connector from the metering device to the service device, Application Note AN-423 "The NMC9346—An Amazing Device" gives the details to implementing power and MICROWIRE signals over just two connections.

CONCLUSION

This application note describes a number of approaches to metering devices from the very simple to the complex. If more E²PROM is required it is available in the NM93Cxx family in 8-pin DIPs and SOIC in various sizes. With the features of very low power, small size, and low cost as well as the simplicity of interface to most processors and controllers already part of the panel interface of most server devices, the implementation of this type of product is very easy.



TL/D/11189–8

A	B	C	D	E	F
0	0	1	0	0	0
1	0	0	0	1	1
0	1	0	1	0	1
1	1	0	0	0	1

FIGURE 7

TABLE IV

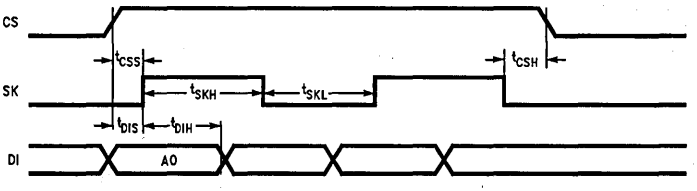
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	$\overline{D}$	$\overline{C}$	0	0	B	A	0	0	D	C	0	0	B	A	
MS DIGIT								LS DIGIT								
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	00
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	01
•																
•																
•																
0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	89
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	100

TL/D/11189–13

TABLE V. NMC95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, starting at specified address
WEN	1	00	11XXXX		Write enable must precede all programming modes
WRITE	1	01	A5–A0	D15–D0	Writes register
WRALL	1	00	01XXXX	D15–D0	Writes all registers
WDS	1	00	00XXXX		Disables all programming instructions

Synchronous Data Timing



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Instruction Sequence

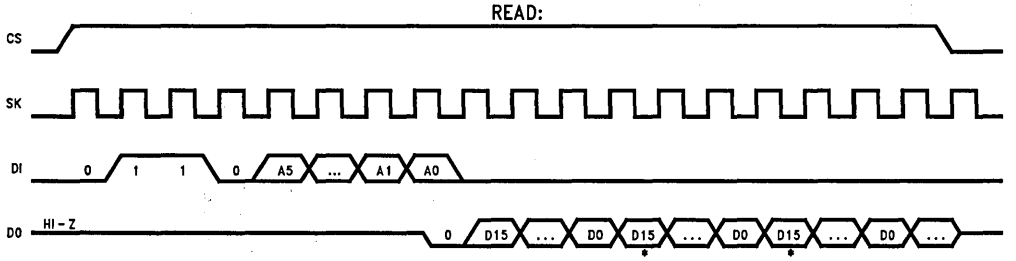

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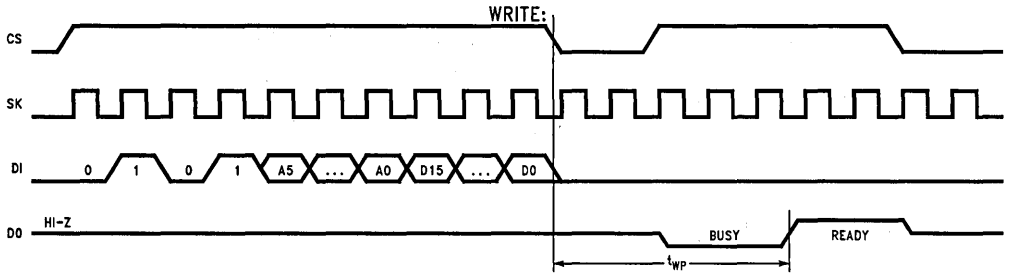
FIGURE 8



TL/D/11189–12

FIGURE 9

NM95C12 Memory Mapping Solution for PC® Applications

National Semiconductor
Application Note 767
Christian Plourde

INTRODUCTION

The design of an adapter card for a PC requires some knowledge of the different mechanisms used by the PC to access or exchange data with the adapter card.

The complexity of the mechanism used depends upon the level of functionality one wishes to implement on his design. At the low-end, the PC will access the adapter card as a simple I/O location, where for the more sophisticated cards, a BIOS will be incorporated onto the adapter card which may also use memory, I/O, interrupts and DMA channels from the PC.

This note discusses how to use the NM95C12 as a low cost solution for the implementation of high-end features on a general purpose adapter card for a PC.

1.0 OVERVIEW OF THE PC AND THE ADAPTER CARDS

In order to fully understand the possibilities offered by using an NM95C12 at the interface level between the PC and its adapter card, let's review the characteristics of that interface.

1.1 The PC has a certain amount of memory available for adapter cards. Both the location and space occupied by this memory vary depending on the type of PC (XT, AT). The XT reserves memory locations for 8-bit data transfers onto the adapter cards. The AT reserves the same locations for 8-bit data transfers but also reserves additional space for 16-bit data transfers.

1.2 The same mechanism applies to the I/O locations on the PC that are reserved for accesses onto an adapter card. A certain amount of I/O addresses will allow the PC to perform 8-bit data transfers with the adapter card on an XT system and some more locations will additionally be made available for 16-bit data transfers with the adapter card on an AT system.

1.3 Any adapter card you install into a PC is allowed to request interrupt service from the main PC card. An XT system offers the adapter card 6 interrupt lines where an AT system offers an additional 5 lines. (Not all of these lines are directly available for the adapter cards since some of them will be used by other cards on the PC.)

1.4 Finally, some DMA channels on the PC main board can be used by the adapter card through proper handling of DMA REQUEST and DMA ACKNOWLEDGE lines available on the PC connector. As for the other mechanisms, 8-bit DMA data transfers are allowed on an XT system where both 8- and 16-bit DMA data transfers are allowed on an AT-based system.

2.0 POSITIONING THE ADAPTER CARD

Any designer which intends to use one or more of the data transfer paths described above is aware that his card will have to carry the ability to be mapped into the available areas on the system, since other cards already installed into the PC probably make use of a part of the space reserved for the adapter cards.

2.1 If the adapter card contains memory accessible from the PC main board, up to two different levels of mapping may take place depending on the size of the memory. For a small memory size (let's say 8K or less), the entire area will be linearly accessible from the PC but its location will have to be mappable at different places into the range reserved for the adapter cards, thus ensuring that it will not interfere with any other cards using parts of this range. For larger memory, a second level of mapping is required, partitioning the memory into software selectable windows of 2K, 4K, 8K, etc. which location will still be mappable into available areas as described above (see *Figure 1*).

2.2 The same procedure applies to I/O locations on the adapter card. Any peripheral address has to have the possibility to be accessed at different selectable locations into the I/O address range reserved for adapter cards, thus ensuring that there won't be any address conflict with peripherals from other cards already installed into the system.

2.3 If the adapter card has the ability to request interrupt service from the PC main board, it also has to have the possibility to select the interrupt line it will use among those not being used by other adapter cards.

2.4 Finally, as for the interrupt lines, an adapter card using DMA channels must be able to select channels not used by other adapter cards.

3.0 TWO ISSUES: POSITIONING AND INITIALIZING

The most widely used way of implementing all of the above options is to install jumpers on the adapter card which setting will allow the end user to position its card into the available areas (see *Figure 2*). Even though this method has some disadvantages, like the fact that the user has to open the PC and remove the adapter card each time he has to modify the setting and the fact that a description of the settings allowed has to be carried along with the adapter card, it remains one of the cheaper and most easy to implement methods of positioning an adapter card into a PC.

Let's now consider some other interesting features that could be implemented on an adapter card. Once the application software is loaded from a diskette usually provided with the card, it may be possible to initialize and then to configure the card. For example, if the card is a data communication product, its on-board peripherals first have to be properly initialized and then the overall configuration of the link has to be defined (the parity and stop bits, the baud rate and such parameters as flow control, echoing, DCE or DTE arrangement, split clocking, etc. for either asynchronous or synchronous data transmission). Once all these parameters have been defined, the card should be operational as long as the power feeds the system.

An interesting step further in functionality would then be the implementation of some non-volatile data storage area on board into which the actual initialization and configuration of the adapter would be stored and referred to at any subsequent call of the application software following a power-up.

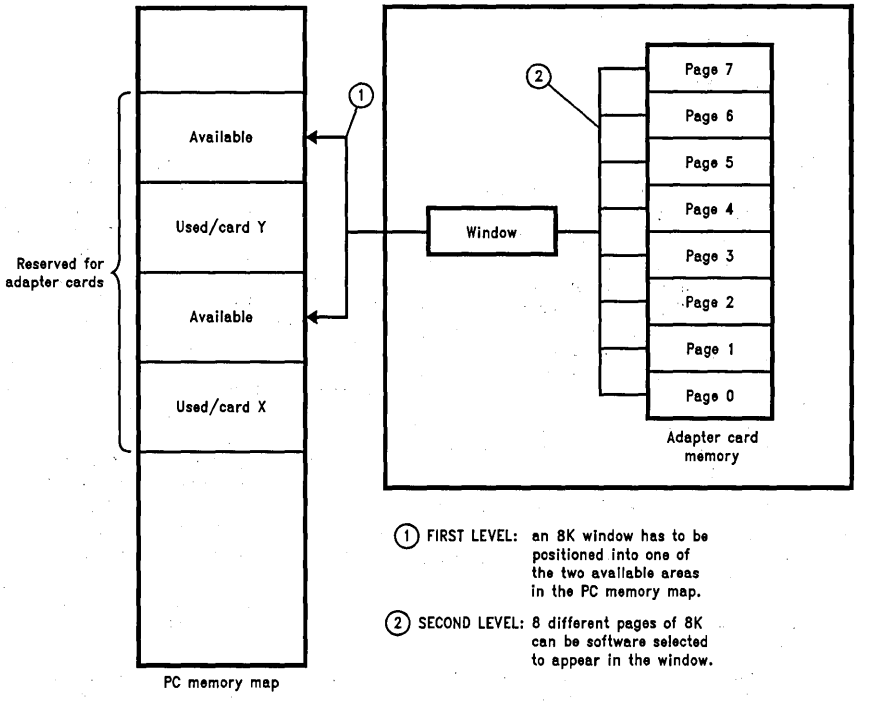


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FIGURE 1. Partitioning of 64K of Memory through an 8k Window Positioned into One of Two Available Areas in the PC Memory Map

If a BIOS is installed on the adapter card, the user could even be prompted to verify and modify (if required) the configuration of the card right away at power-up, since the BIOS signatures are scanned and given control after the usual diagnostics executions, graphic card, floppy and hard-disk recognition.

4.0 USE OF AN NM95C12 ADDS POWERFUL FEATURES TO YOUR ADAPTER CARD

The proposed application is to provide the PC with the possibility to access an NM95C12 located on the adapter card. The BIOS on the adapter card would instruct the PC to verify the status of a configuration flag stored in the NM95C12. If the status indicates that the card hasn't been initialized and configured yet, the user will be requested to accomplish these tasks prior to any further operation of the adapter card. Once the initialization has been properly loaded and saved, the BIOS, at any subsequent power-up, will simply instruct the user of the current configuration and ask if any modification is required.

The initialization portion of the card would make use of both the non-volatile memory and the dip switch's replacement features on the NM95C12. The positioning of the memory, the selection of the I/O addresses range and the interrupt lines or DMA channels (if required) would be set using the dip switch's replacement according to the user selection at first initialization. The other bytes or words used to initialize the peripherals on the adapter card would be stored in the NM95C12. All the configuration parameters related to the software operation of the card would also be saved into the NM95C12.

It is understood that such a solution does not eliminate all the jumpers or dip switches' on the adapter card. The location of the BIOS implemented on the card and the I/O address used to access the NM95C12 both have to be determined and set prior to the installation of the card into the PC. There is no easy way, if any, to work around such restrictions.

The circuit on *Figure 3* shows a simple way to implement an interface to the PC that will allow the user to position an 8K window of memory into one of eight possible locations in the adapter card's reserved area. He will have the possibility to select one of eight possible ranges of addresses for the I/O address of the peripherals on board and he will also be able to select one of four interrupt lines available on the PC connector. The memory on the adapter card consists of 32K of RAM divided into four pages of 8K. The selection of the page is performed through a write operation of 2 bits in a register whose I/O location has been determined by the setting of the NM95C12.

At power-up, before the system has been initialized, the PC must have the possibility to access at least the BIOS on the adapter card (ROM BIOS on *Figure 3*). LK1 on *Figure 3* allows eight different locations for that BIOS in the PC memory range reserved for that purpose. Since that BIOS will verify the configuration byte or word into the NM95C12, the I/O addresses of the circuit that accesses the NM95C12 also have to be selected prior to the installation of the adapter card into the PC. This is done via LK2 on *Figure 3*.

The circuit that allows the accesses to the NMC9512 is very simple. A sequence of writes to a latch (Itch A on *Figure 3*)

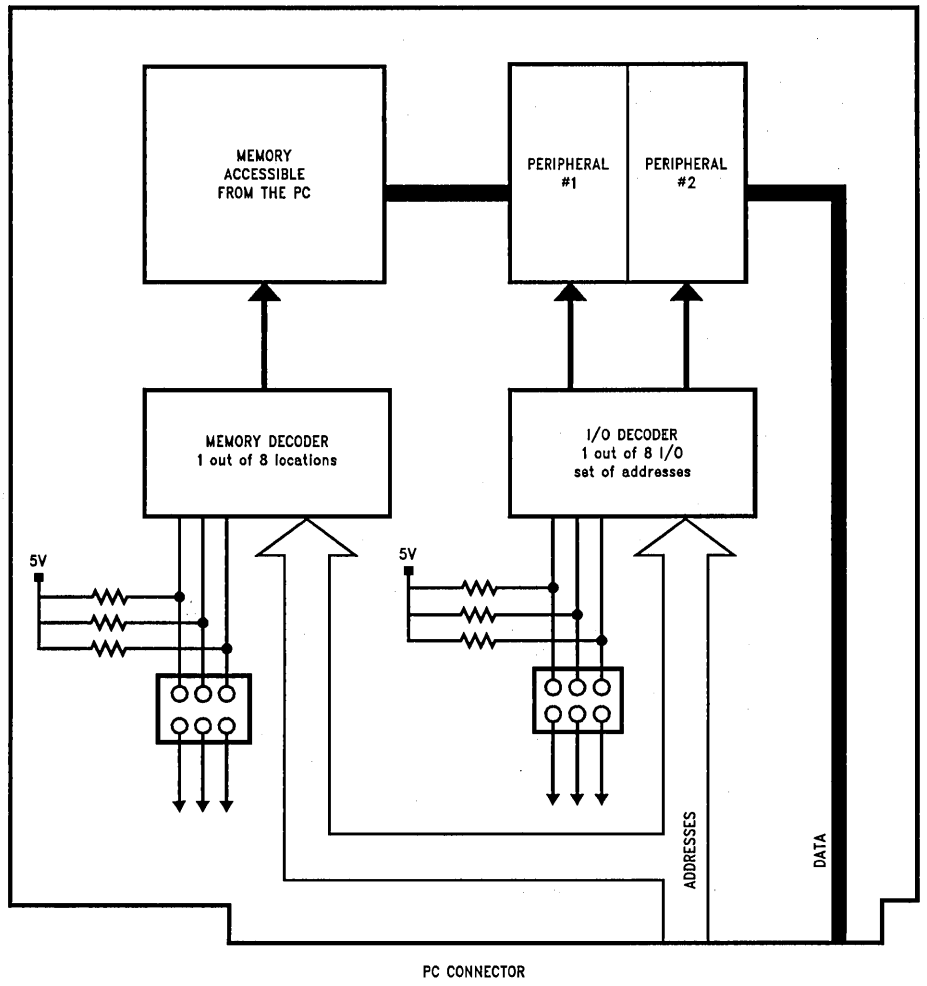

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FIGURE 2. Using Jumpers (or Dip Switches) to Position Both Memory and I/O Addresses on an Adapter Card

enables CS on the NM95C12, presents the data to be written to pin DI and latches this data into the NM95C12 by toggling the pin SK. The same principle applies to the read operation except that the bit output at pin DO of the NM95C12 is sent to the PC via a buffer (buff A on *Figure 3*).

The clock of latch A, the enable of buff A and the select and output enable of the ROM BIOS are all controlled by control A on *Figure 3* which may be a GAL.

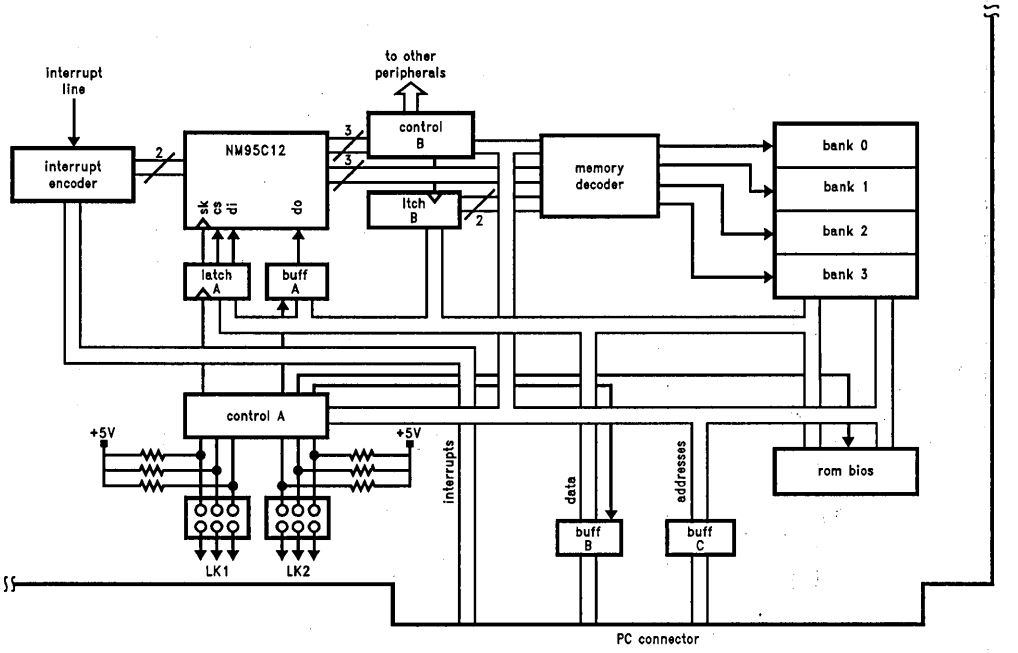
The user is then allowed to position and configure its card. On the example of *Figure 3*, three lines of the NM95C12 are connected to the memory decoder. The status of these lines will position a window of 8K of RAM into one of eight possible locations in the PC memory area reserved for adapter cards. Three other lines of the NM95C12, connected to control B on *Figure 3*, will allow the same possibility for the I/O address of the peripherals on the adapter card. One of these peripherals is latch B into which the PC is now allowed to write two bits whose value will select one of the four pages of RAM to appear on the 8K window positioned by the first three lines of the NM95C12.

Finally, the two remaining lines of the NM95C12 are connected to the interrupt encoder on *Figure 3*, thus allowing the user to determine which interrupt line, out of four possible lines, he will select for his application.

Additional precautions should be added by the designer to ensure that a non-initialized card will not interfere with existing cards already plugged into the PC. A latch which status at power-up disables the interrupt encoder, the I/O and memory decoders, for example, could be reset by the PC once the proper configuration has been loaded or confirmed by the BIOS.

CONCLUSION

The implementation of similar features on a PC adapter card without the use of a NM95C12 would still require an EEPROM-like type of device in addition to some non-volatile latch mechanism. For such an application, the NM95C12 represents a simpler, cost-effective solution.



TL/D/11190–3

FIGURE 3. A Powerful Use of the NM95C12 for a PC Interface

Integrated Manufacturing Control—NM95C12

National Semiconductor
Application Note 789
Jan Ladiges

INTRODUCTION

Manufacturing methods and testing techniques have become increasingly automated over the past few years. Of current interest are techniques which allow automated access to manufacturing information which, in turn, is used to tailor test and set up for individual manufactured assemblies. This note explores the application of the latest generation of memory devices to manufacturing control situations and integrating access schemes for test, in system programming and manufacturing control.

WHAT INFORMATION?

The first question raised in manufacturing control applications is what information needs to be accessable. In most cases information like serial number, date of manufacture, and revision number need to be written once during initial manufacture. Ideally, this information should be secure (i.e., read only). As a product passes through test additional data may be recorded such as calibration constants or configuration data. If an assembly should fail, the type of failure and number of recurrences may be recorded at the repair depot to determine, for example, if this assembly should be scrapped.

All of this data does not require a large memory device. National Semiconductor's family of serial access E²PROMs are ideal candidates because of low cost, small footprint and ease of access.

SECURITY

The issue of data security is addressed by the 93CSXX family of devices. In these units a portion (or all) of the memory area may be set up to appear as ROM (once desired data has been loaded into the device). The amount of ROM vs PROM is determined by a value in the protection register which delimits the portion of the device that is write protected. For details refer to AN-507 — Using the 93CSXX MICROWIRE™ family.

Some of the synchronous bus devices (24CXX I²C family) have write protection of the upper half of the memory space by bringing a control line (WP) high.

ACCESS

In the most basic form of automated manufacturing control, an E²PROM is simply added to a circuit assembly as an isolated block. There may be no electrical connection between the memory and any portion of the circuit assembly. A means of accessing the pins of the memory device must be considered. This may involve adding extra contacts to a card edge, creating a separate pin-type connector area or simply providing BON (Bed Of Nails) access. The latter may prove impractical with the increased use of surface mount.

A more promising and efficient use of board resource can be realized if the memory device shares I/O pins and power supply with the host assembly. The number of access points required for varying applications schemes ranges from 2 (for synchbus with no security) to 5 (for microwire with full security).

To take maximum advantage of the E²PROM it is often desirable to allow access both externally (like the isolated case) and internally by the system resident on the circuit assembly.

An example of shared functionality is given in *Figure 1* which allows the resident system to flag a fault condition. The unique feature of this is the fault flag will be valid even if system power is cycled on and off or the board removed from the system. The visible flag (an LED) allows a technician to quickly identify a problem board. Additional information (i.e., a fault code) can be written into the E²PROM as well. The module, when returned for repair, contains all the traditional manufacturing information as well as the fault code.

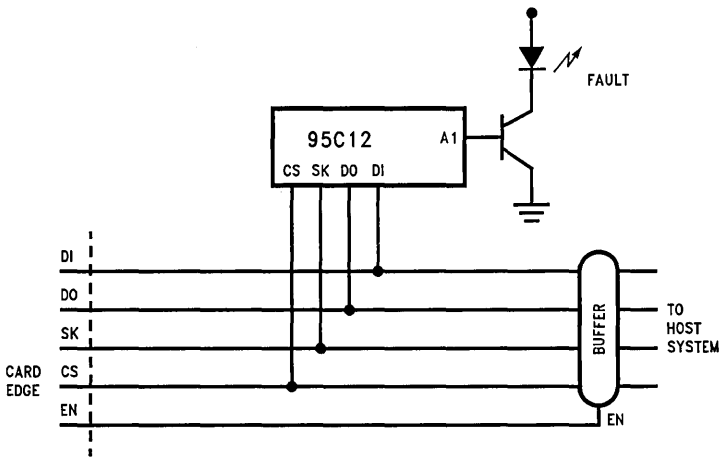


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FIGURE 1. Shared Access with Non-Volatile Fault Flag

INTEGRATION WITH OTHER FUNCTIONS

The trend towards more electronics in smaller packages has led to the acceptance of surface mount technology. Traditional test access methods (BON) has become impractical at present density levels and virtually impossible when SMD's are mounted on both sides of the board.

To facilitate surface mount board testing, electronic rather than mechanical techniques have evolved. The solution often consists of boundary scan and some form of built in self test (BIST).

JTAG (Joint Test Action Group), sponsored by the IEEE P1149-1 Working Group, has defined a boundary scan standard which has become widely endorsed. This JTAG standard specifies that each conforming IC have a Test Access Port (TAP) which allows devices to be connected in series and minimizes interconnect overhead *(Figure 2)*. The boundary scan register (double buffered) gives access to the device pins for testing. The rest of the structure provides an instruction decode, a bypass function and any product specific requirements through additional registers (shown in dashed lines).

Surveying current programmable logic trends, GAL type devices are extremely popular to replace small blocks of random logic. One disadvantage is that traditionally each different "pattern" would have to be programmed, tested and identified prior to being installed on the assembly. With SMT versions of these devices, handling alone poses a significant inconvenience.

The concept of programming devices after they have been installed (ISP — In System Programming) is beginning to attract interest.

What do these test and ISP techniques have in common with manufacturing control? — serial board access.

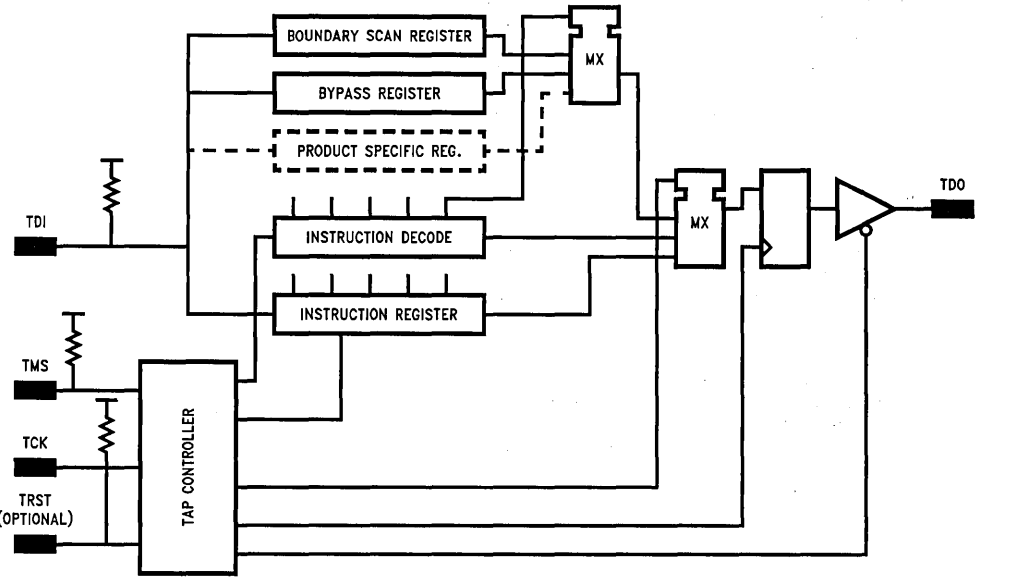

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FIGURE 2. JTAG Test Access Port

Let's consider a typical high density PCB assembly *(Figure 3)*. This assembly requires boundary scan testing, uses ISP GALS and implements a serial E²PROM for manufacturing control data.

All 3 functions require a serial access scheme. If each is considered independently, a considerable number of pins would have to be dedicated to these functions (at least 12 connection points). One common bus and a common protocol to access management information, provide test access, and perform incircuit PLD programming would be ideal.

AN EXAMPLE COMMON ACCESS SYSTEM

The circuit of *Figure 3* uses a COP 822 microcontroller to create a JTAG to MICROWIRE converter with added support for an ISP PLD loop and an E²PROM with security for manufacturing control. The combined test, manufacturing data and PLD programming requires only 5 access pins.

Because JTAG test access often requires high speed, this system has been broken down as two JTAG loops (hence two TMS pins), one high speed dedicted to the test loop and a slower speed loop dedicated to E²PROM and PLD access through the COP 822. The speed of this JTAG loop is limited by COP processing speed in translation to MICROWIRE.

This approach represents a solution for common access using devices available today. As standards take hold (like JTAG) then non-volatile memories and ISP PLD's may appear supporting a **standard** serial protocol and further reducing the overheads in a common access scheme.

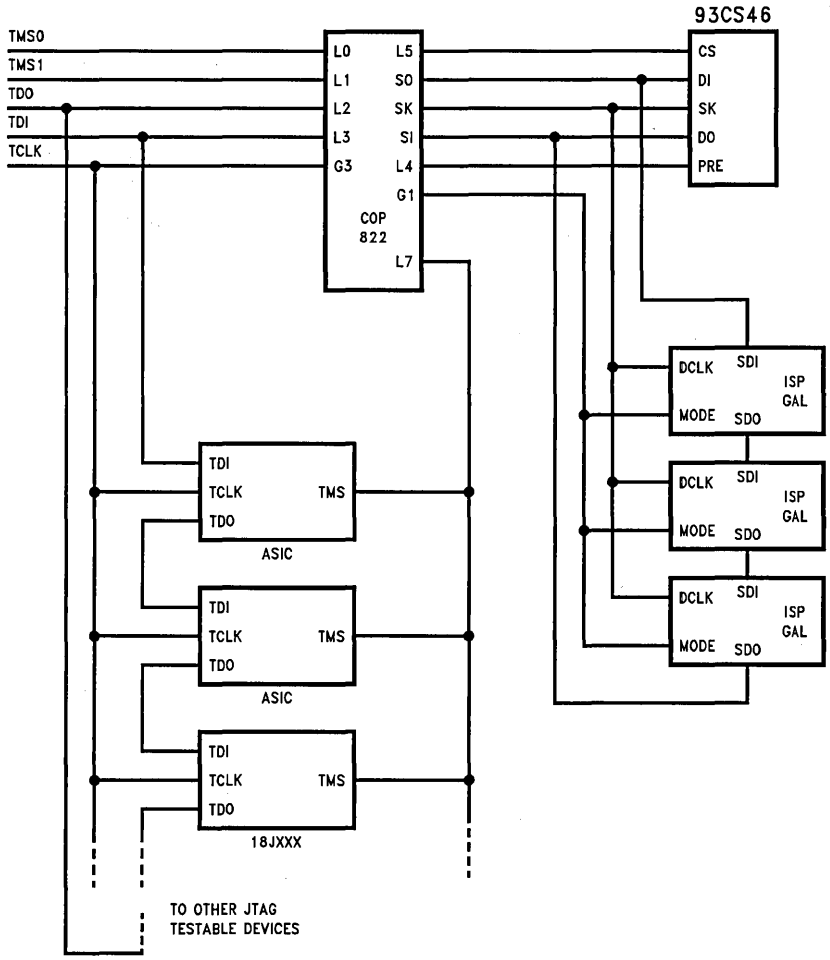

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FIGURE 3. Common JTAG Access for Test, ISP, and Manufacturing Control

NM95C12 EEPROM Controls Amplifier Gain

National Semiconductor
Application Note 790
Harry W. Lewis

BACKGROUND

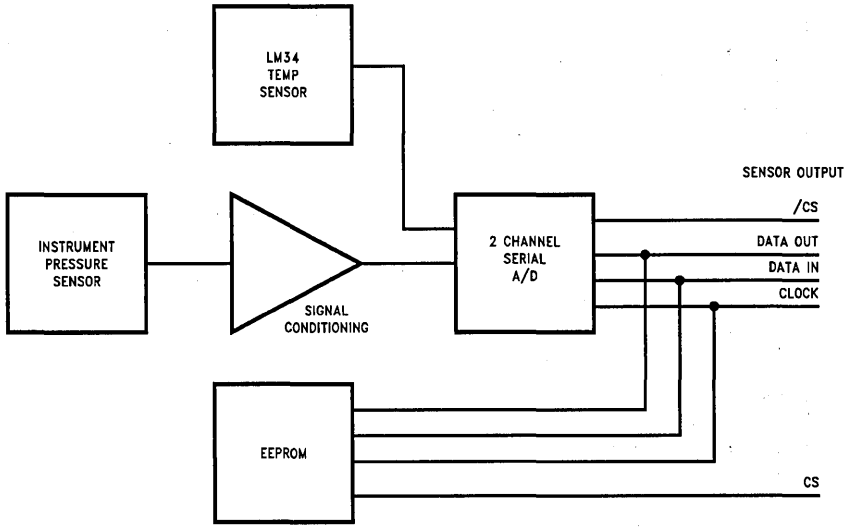
Electrically Erasable PROM or EEPROM finds wide application in analog data acquisition. When using sensors, some possibilities include storing calibration constants (gain, nonlinearities, temperature effects and offset), the engineering units of measurements, and even keeping serial numbers. In *Figure 1* for example, after an A/D converter converts the analog sensor output, the processor can use correction factors from the EEPROM to get a final value. By keeping these corrections with the sensor assembly, one can effectively get a more accurate sensor.

There are several ways to achieve a wide input range when required. One way is to use an A/D with more bits than needed and then use the extra bits for ranging. In other words, if 8 bits are needed for the output by using a 10-bit converter a full scale resolution of 8 bits is still provided even if the input range is only ¼ of the converter range. This can get expensive quickly since the price of accurate A/Ds goes up substantially with the number of bits! Even so, with advances in audio parts of 16 to 18 bits, this could be viable in some instances.

A more common way to cover wide range inputs is to scale the incoming levels to close to the maximum rated input range of the A/D. If the input range is 0 $\rightarrow$ 0.2V and the converter is rated 0 $\rightarrow$ 5V, a gain of 25 in front of the A/D will give the full resolution over the reduced range. Additionally, the input range can be offset from zero. While many A/Ds have range and offset options, there are limits if the accuracy is to be kept. A circuit to use both scaling and offset is *Figure 2*. The gain and offset are mostly determined by the reference and the resistor ratios.

$$V(A/D) = V_{IN}(1 + R3 * (R1 + R2)/(R1 * R2)) - V_{REF} * R3/R1$$

Common metal film resistors are widely sourced and have good temperature coefficients. Type RN55 T-2 are rated at ±50 ppm/°C. The difficulty comes with their resistance specification of ±1%. Since most gain stages require at least 2 resistors to determine gain, the system accuracy is already reduced to, at best, 2%. Multiple stages and other error sources compound the problem. Some 10-bit serial A/Ds have 0.1% accuracy! Even the lowly 8-bit converter can be ½%. For the circuit in *Figure 2*, EEPROM is a very handy way to store the calibration of the low cost resistors to get more of the full accuracy capability of the A/D. Even when not using a sensor, EEPROM can be useful for calibrating a scaling and offset circuit. This is especially true now that low cost A/D converters have gotten so accurate.



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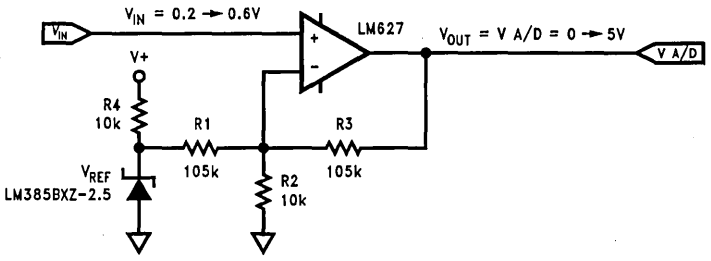
Full Scale (5V) = 4720 PSI
Zero (0V) = −83 PSI
Temp Coefficient = +0.2 PSI/°F
Serial # = 184625
Last Rev = F

FIGURE 1. Sensor with Digital Output and Correction Factors



$$V_{OUT} = V\,A/D = V_{IN}\left(1 + \frac{R3\,(R1 + R2)}{(R1 * R2)}\right) - \frac{R3}{R1}V_{REF}$$

$$= 12.5 * V_{IN} - 2.5V$$

FIGURE 2. Scaling and Offset Circuit

DON'T BE A DIP

For storing data, EEPROM can generally beat DIP switches. However, there were some other things that DIP switches could do better. One case was having external access to logic levels without needing an additional port chip. Another area was switching analog voltages. To replace an analog DIP switch, a designer often had to add an output port and a separate CMOS or other switch to do the actual switching. The NMC95C12 1024-bit CMOS EEPROM with DIP switches attacks both these areas. When first glancing at the data sheet, the title "EEPROM with DIP switches" can conjure up visions of the data being stored in 1024 tiny levers on top of the package! Of course that is not the case, see *Figure 3* for the real block diagram. Actually the part has 61 words of 16 bits of EEPROM for general use. That totals 976 bits. The DIP switches referenced in the title are 8 pins with switch logic to allow several different modes of operation as controlled by the switch configuration register. There is a nonvolatile Initial Switch Setting Register of 16 bits. And, finally, a Switch Readback Register allows the pins to be used as a digital input port. Processor interface is by a serial MICROWIRE™ port.

THE BIG SWITCH

Switches are the main difference between the NM95C12 and other EEPROMs. They can be thought of as four independent switches each having two pins, A and B. Each switch has four control bits labeled W, X, Y and Z to set it to one of its 14 modes. Table I shows all the modes. The Switch Configuration Register (SCR *Figure 4*) is 16 bits long to hold all four bits of each of the four switches. It is not made from EEPROM cells so it can be written faster and there is no wearout mechanism. Being volatile, the SCR is reloaded at each powerup from the EEPROM Initial Switch Setting Register.

WHERE DID THE PARALLEL PORT COME FROM?

Switch modes 0–3 allow the 2 pins to be digital outputs. When bits Y and Z are set to 0, A = X and B = W. Other modes allow A and/or B to be TRI-STATE® for use as digital inputs or I/O. *Figure 5* shows the switches being used for general input and output, to set gain controls, and to drive analog multiplexers. In *Figure 5*, the port of U4 selects the input channel of the A/D via the multiplexer U3. Input channel 7 has a selectable gain preamplifier (U1) whose gain is controlled by U2 selecting the proper feedback tap. The resistor values for R1, R2, R3 and R4 are standard 1% values. Ideally the values would be 48K, 12K, 3K and 1K. Although they are not quite correct for the gains desired, calibration values stored in the EEPROM can correct for this while fixing the other errors. One thing to keep in mind when selecting the standard values, make sure the A/D stays in its active range during the whole range of expected signal input. If the A/D needed to exceed the maximum count, the error generated is not correctable. This implies making the gains on the low side.

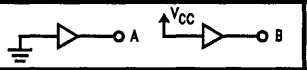
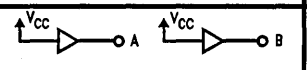
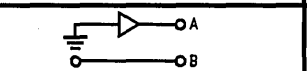
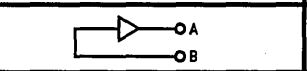
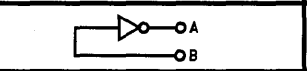
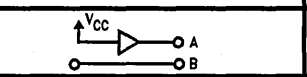
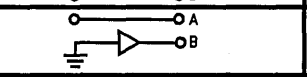
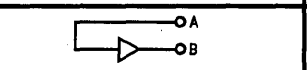
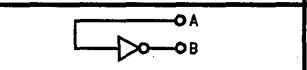
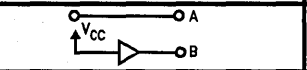
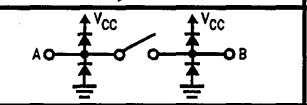
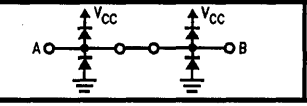
MODES 12 AND 13?

Mode 12 is an open (10+ MΩ) between pins A and B. Mode 13 is an ANALOG short (200Ω or less) between the same pins. In *Figure 6*, analog switches give variable gains and do analog multiplexing. Switches 1 and 2 select the input to the A/D. Switches 3 and 4 control gain. Although the pins used for a closed analog switch can not be read as an input, the input function of the Switch Readback Register will still work for the other pins, so mixed analog and digital operation is possible. Of course, errors in the amplifier gains will be corrected by storing calibration constants in the EEPROM section of the part.

FINALLY!

The NM95C12 can accomplish what a DIP switch used to do without the extra parts. You have external access to logic levels and you can even switch analog voltages. All without needing additional port or multiplexer chips.

Table I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\overline{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\overline{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

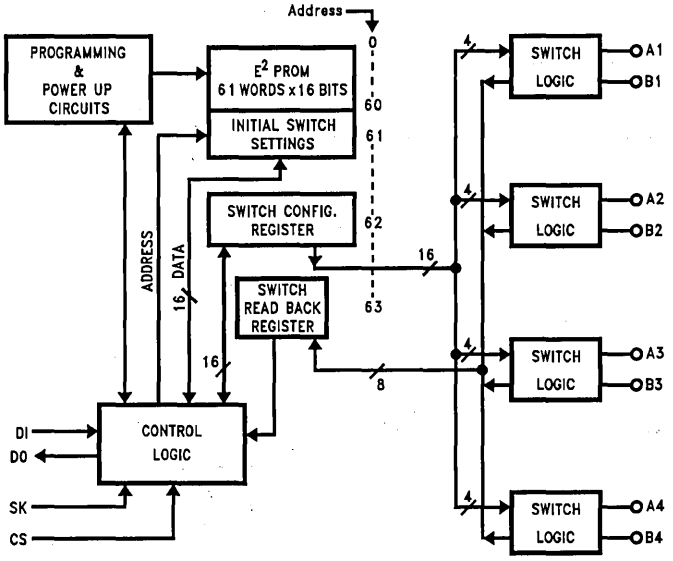

FIGURE 3. Block Diagram

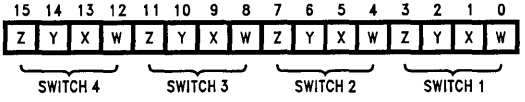

FIGURE 4. Switch Configuration Register (SCR)

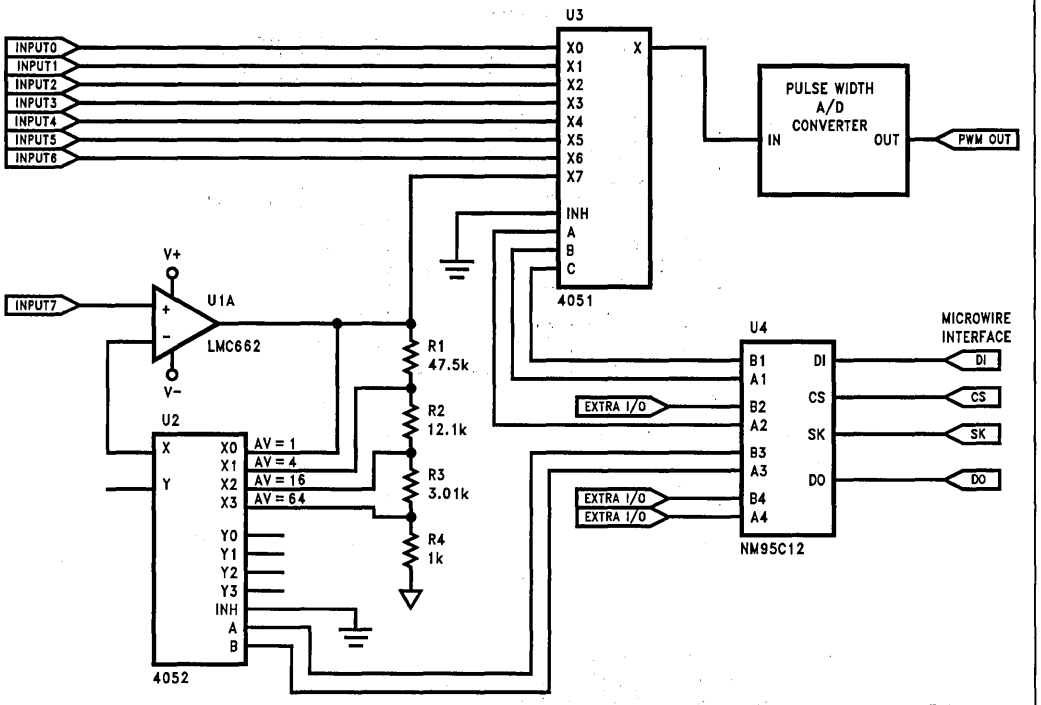

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FIGURE 5. Using NM95C12 Switches as Digital I/O

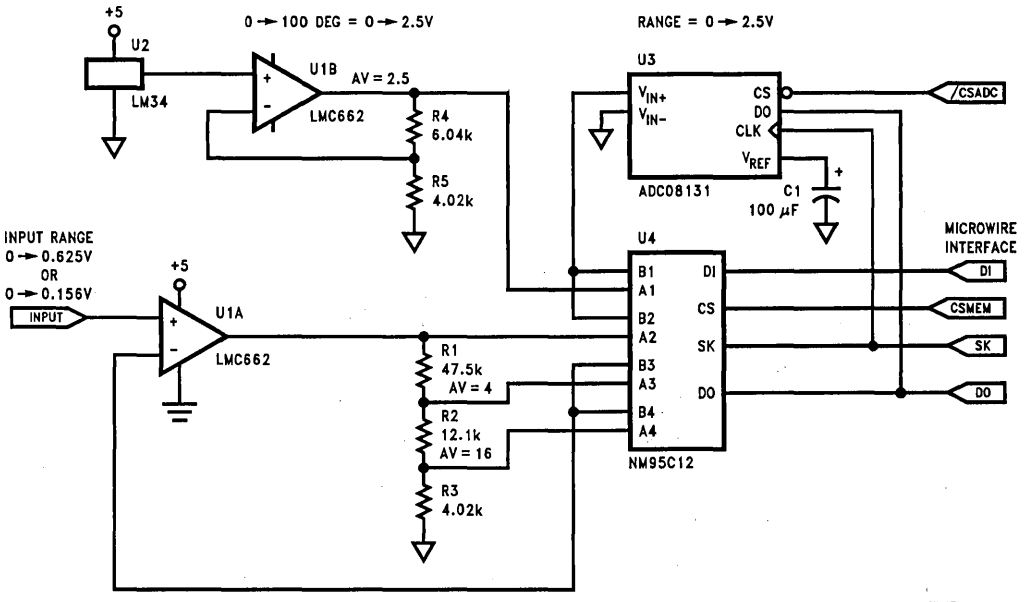

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FIGURE 6. Using NM95C12 Switches as Analog Switches

Stand Alone Control of MICROWIRE™ Peripherals Using the NMC87C257

National Semiconductor
Application Note 791
Charlie Mitchell

INTENT

This note describes the implementation and use of a standard memory element in the realization of state machine control for the purpose of generating serial data. The applications shown here employ serial data streams to control and program peripheral devices which would otherwise require CPU support for use.

The benefit to the user of the demonstrated techniques is the low cost, low effort, implementation of tasks normally allocated to more sophisticated and more engineering intensive methods. These solutions expand the range of systems and applications in which a variety of National Semiconductor's MICROWIRE devices may be used.

MICROWIRE

The MICROWIRE standard is an interface technique first developed at National in the 1970's in an effort to reduce the component pin count (and hence package size and cost) required for the interfacing of microcontrollers to peripheral components. Over the ensuing years a wide variety of devices employing this interface technique have been introduced to the market. They include display drivers, analog to digital converters, phase lock loop frequency synthesizers, memories and complex analog devices. A full list of all but the most recent devices using the MICROWIRE interface can be found in the *Master Selection Guide.*

A MICROWIRE connection is a straight forward serial hookup consisting of data and clock. Generally, input and output data are presented on separate lines. The clock to data relationship resembles that of a TTL or CMOS 7400 series shift register with the positive edge of the clock performing the active transfer of data into and out of the device. Care must be taken to examine the data sheet for a device under consideration as there may be deviations from this general description. A more complete description of this interface method is available in National Semiconductor Application Note 452 by Abdul Aleaf.

STATE SEQUENCERS

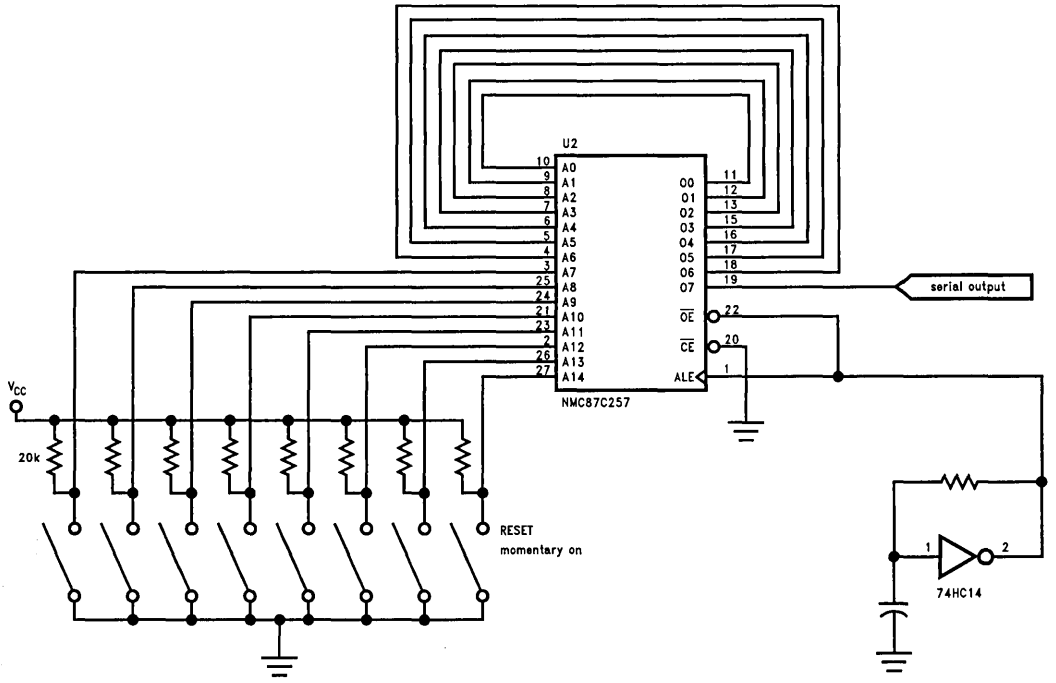
State machines or sequencers in their simplest form consist of a current state memory element and a next state determination network. Upon a clock edge the next state information is converted and held as a new current state while a fresh next state logical determination takes place. One way of implementing this state sequencer is by utilizing a register or latch as the memory element and a Read Only Memory to supply the logic function for the next state. Because a ROM is a "rectangular" or complete logic array (i.e., for every input combination there exists a unique output), this next state logic is a lookup table.

THE NMC87C257 UV ERASABLE CMOS PROM WITH LATCHES

The NMC87C257 is a device first conceived to reduce the chip count in microprocessor systems which had a multiplexed address/data bus. As such, the latches required to capture the address while return data occupied the bus were put on board the device. Intended for this microprocessor application, the NMC87C257 does not have the speed of some of the bipolar "logic" PROMs (nor the power dissipation), but it's large memory array would be exceedingly expensive in a bipolar device. The 32k x 8 memory means that in a state machine application fifteen inputs can define over 32,000 states, represented in eight output pins.

GENERATING A SERIAL OUTPUT WORD FROM THE NMC87C257 BASED STATE MACHINE

Figure 1 depicts a state machine capable of generating 128 different 128-bit serial data streams. DIP switches 0–7 select the specific data stream program. Seven bits of output data are fed back to inputs to define the next state in the serial data sequence. Bit 08 is the serial data output. A CMOS oscillator generates the clock. It is important to note that the clock drives both the ALE (Address Latch Enable) and $\overline{OE}$ (Output Enable) inputs. ALE is the signal which activates the "open" state of the input latch, as such, unlike an edge triggered register, the outputs follow the inputs until its (ALE's) fall. To avoid a high speed feedback phenomenon while the latches are open it is necessary to break the feedback loop and "freeze" the data at the desired output/input state. This is accomplished by disabling the TRI-STATE® outputs. As long as the outputs are loaded only by the high impedance inputs of the CMOS device, the next state information will be transferred into the latches. Resistive or bipolar logic loads should not be attached to lines operating in this manner.



Note: Refer to AN 140 for R & C values.

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FIGURE 1. State Machine for Serial Word Generation

TABLE I. PROM Addresses and Data

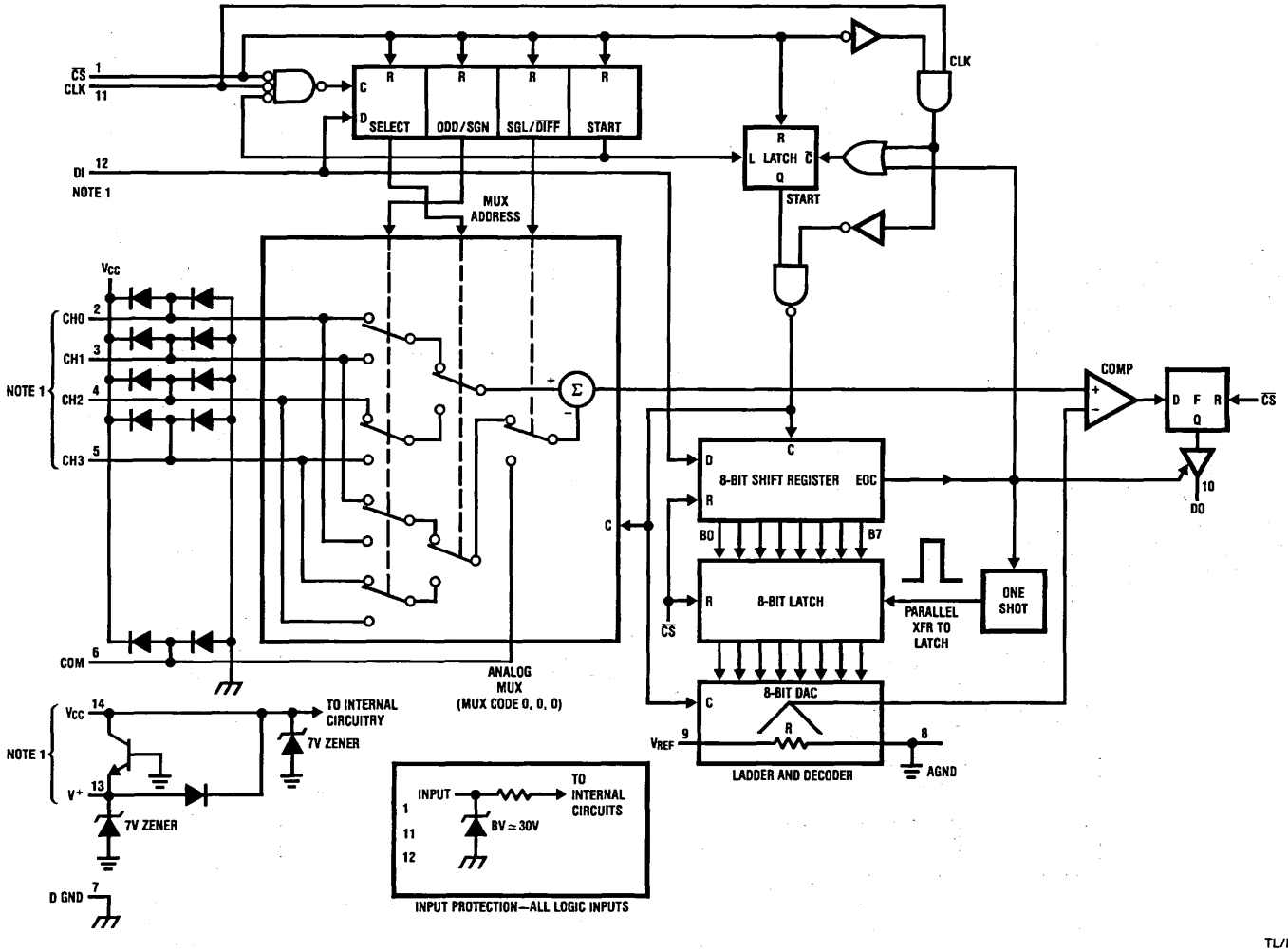
Address	Data (7 Bits)	Serial Output	Comments
nn 7F	00	0	Startup Address Generates 1st Word
nn 00	01	1	
nn 01	02	1	
nn 02	B4	0	
nn B4	03	1	
•			
•			
•			
•			
nn 7E	7E	0	Loop to Self - Stop

Table I shows an example of the PROM code which generates the serial output. The address includes a leading byte "nn" which will determine which of the bit streams will be selected. Notice that the 7-bit data is in fact the next state information reflected in the next address.

APPLICATIONS FOR A SERIAL WORD GENERATOR USING THE NMC87C257

A Power Supply Sequencer

The ADC0854 is a comparator circuit with a MICROWIRE controlled four input multiplexer and a settable 8-bit reference divider which drives the second compare input. A block diagram is depicted in *Figure 2.*



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Note 1: For ADC0852; D1 is input directly to the D input of ODD/SIGN, select: is forced to a "1", A_{GND} and COM are internally tied to D_{GND}, only V_{CC} is brought out, V_{REF} is internally tied to V_{CC}, only CH2 and CH3 are brought out.

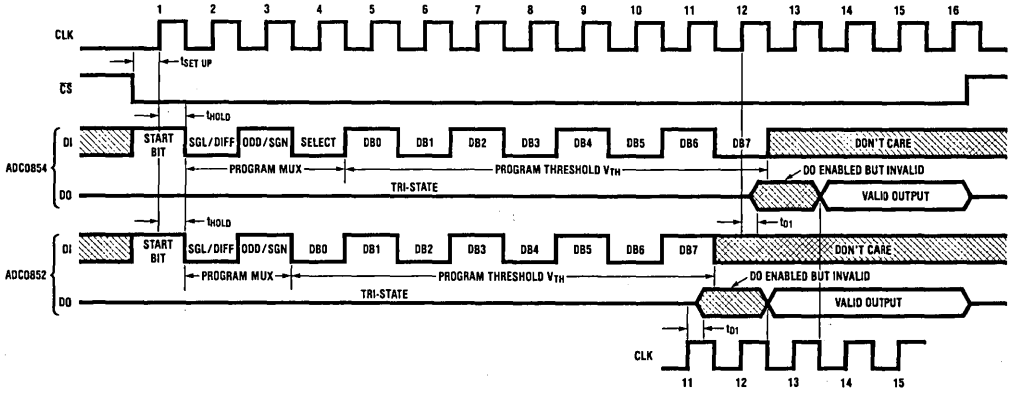
FIGURE 2. ADC0854 Detailed Block Diagram

Many voltage regulators feature an on-off input. Couple these linear components along with the serial word generator and a sophisticated power supply sequencer can be built.

The ADC0854 requires a 12-bit serial word to provide setup information. A start bit is required, which is followed by one bit to select four single ended or two differential inputs. A two bit channel selection and the eight bit reference data byte complete the serial word. It is depicted in *Figure 3.*

Referencing the simplified schematic in *Figure 4,* analog input signals are presented to the multiple inputs of the comparator from the voltage sources, in this case Simple Switcher™ Regulators are used.

The serial word is presented to the ADC0854 is generated from the sequence shown in *Figure 5A.* The Chip Select input which acts to latch the data word into the comparator is generated by a diode AND gate from the four output/input lines controlling the count. All diodes depicted in the schematic are in a single FSA2619P 16-pin dual-in-line package. An MM74C14 hex Schmitt trigger circuit provides the necessary clock wave form and an MM74C244 contributes buffering for the diode gates.



Note: Valid Output can change only on Falling Edge of CLK.

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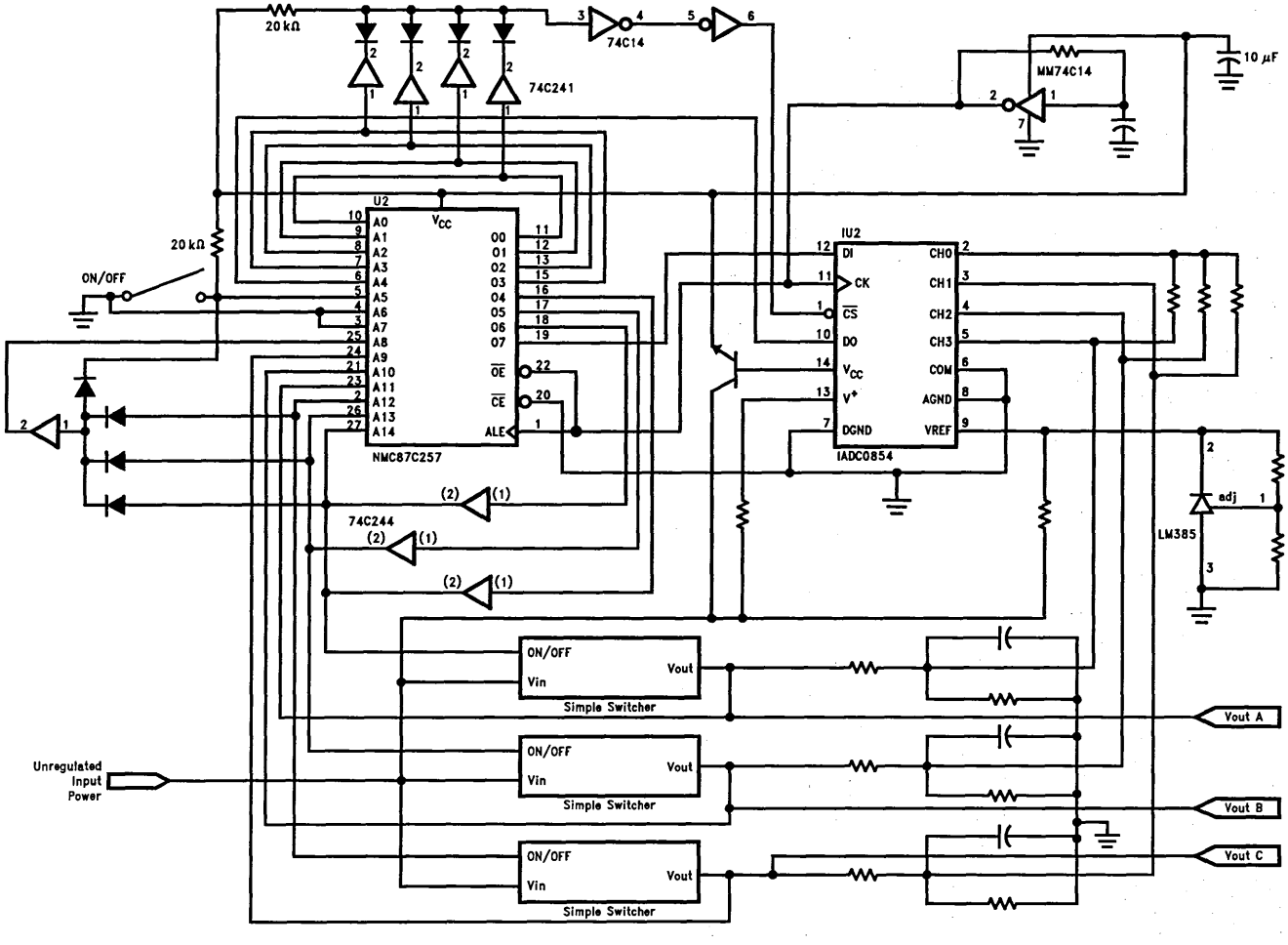
FIGURE 3. ADC0854 Clock, Control Data and Output Data Relationships



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Note: Refer to AN 140 for R & C values.

Note: As resistive and capacitive values in this circuit will vary with application, consult the datasheets of the associated devices for component selection.

FIGURE 4. Partial Schematic of Power Supply Sequencer

Each regulator output is sequentially selected by the PROM generated MICROWIRE and tested for compliance to a voltage level also set via the MICROWIRE. When Voltage A reaches its terminal value, the sequencer delays for a defined period while voltage settles as determined here by the RC network at the comparator input and then raises the control voltage to the regulator B ON/OFF input and, after monitoring that regulator's voltage rise, continues to regulator C. A stable and fixed reference is supplied for the comparisons by an LM385.

A similar control procedure allows an orderly shutdown. During operation the controller monitors the sum of the three supply voltages. A drop from the proper sum will commence the controlled shutdown. These procedures are delineated by the state diagram in *Figure 5b.* In order to differentiate the state defining the condition of the voltages when powering up and the state produced when shutting down a "history circuit" consisting of four diodes and a capacitor records the "all supplies on" condition. The ON/OFF switch must be recycled for the system to power up once again.

A Zener diode regulated output is provided from the ADC0854 permitting the PROM and the Schmitt Trigger oscillator to be powered from the primary source.

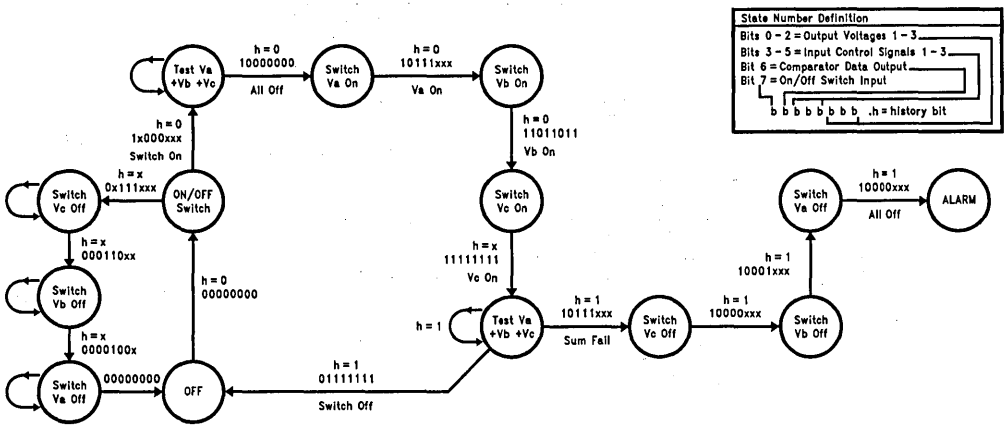
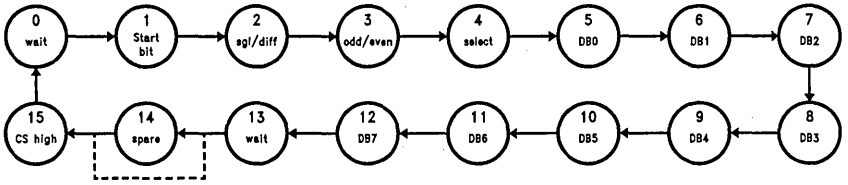


Figure 4A



TL/D/11274–5

FIGURE 5. State Diagram for Power Supply Sequencer

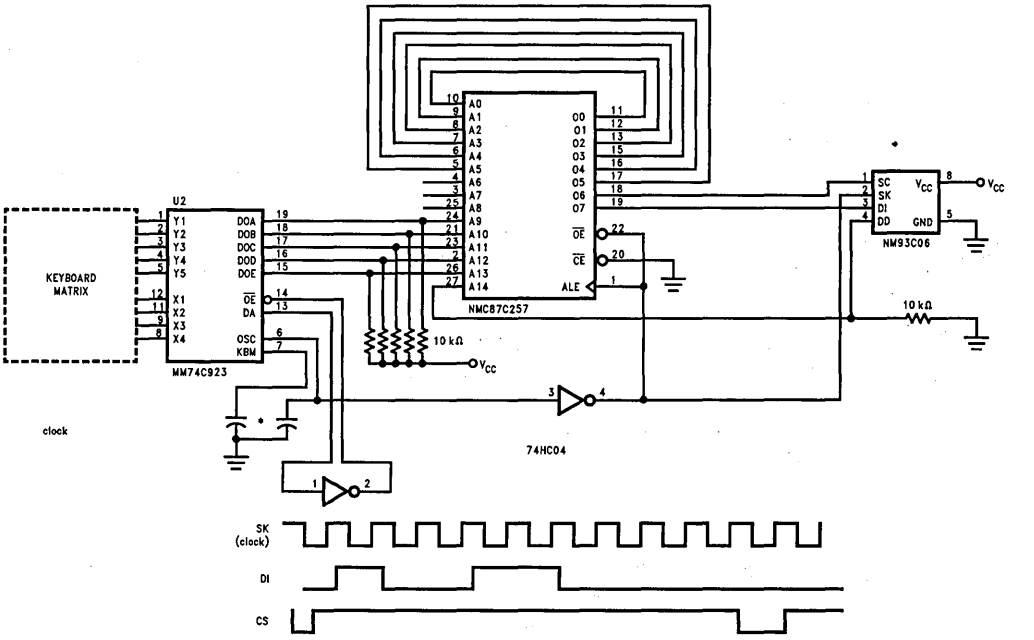
PRODUCTION LINE PROGRAMMING OF MICROWIRE EEPROMS

EEPROMs are frequently programmed prior to board insertion on the production line. This programming may reflect the revision level of the system software and the engineering change level of the printed circuit board.

In this case an NM93C06 256-bit device has been selected. In a production line situation it is desirable to write a segment of memory with the parameters described above.

In order to perform this task the memory must receive a series of MICROWIRE commands. Each of the commands is itself a state ordered sequence. The command sequences first enable the write capability, write 16 bits of information to the specified address and then turn off the write enable. Table II lists the inputs and outputs of the NMC87C257 for a sequence to write a sixteen bit word.

The logic diagram in *Figure 6* depicts a circuit which includes keypad entry capability such that an operator can select up to 20 different such commands.



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*Consult MM74C923 datasheet for component values appropriate to the specific application.

FIGURE 6. Logic Diagram for EEPROM Programmer

TABLE II. PROM Listing for EEPROM Programming

Address (Hex)	00–04 (Hex)	EN	74HC173 (Hex)	CS	DI	DO	Comments
000	01	0	0	0	0	X	
001	02	0	0	1	0	X	Start Erase/Write Enable
002	03	0	0	1	1	X	Start Bit
003	04	0	0	1	0	X	Opcode
004	05	0	0	1	0	X	
005	06	0	0	1	1	X	
006	07	0	0	1	1	X	
007	08	0	0	1	0	X	
008	09	0	0	1	0	X	
009	0A	0	0	1	0	X	
00A	0B	0	0	1	0	X	
00B	0C	0	0	1	0	X	
00C	0D	0	0	1	0	X	
00D	0E	0	0	0	0	X	End Erase/Write Enable
00E	0F	0	0	0	0	X	
00F	10	0	0	1	0	X	Start Write of Data
010	11	0	0	1	1	X	
011	12	0	0	1	0	X	
012	13	0	0	1	1	X	
013	14	0	0	1	a	X	Address Entry
014	15	0	0	1	a	X	
015	16	0	0	1	a	X	
016	17	0	0	1	a	X	
017	18	0	0	1	a	X	
018	19	0	0	1	a	X	
019	1A	0	0	1	a	X	
01A	1A	0	0	1	a	X	
01A	1A	0	0	1	d	X	Data Input
01A	1B	0	0	1	d	X	
01B	1F	1	0	1	d	X	
01F	00	0	F	1	d	X	
020	01	0	F	1	d	X	
021	02	0	F	1	d	X	
022	03	0	F	1	d	X	
023	04	0	F	1	d	X	
024	05	0	F	1	d	X	
025	06	0	F	1	d	X	
026	07	0	F	1	d	X	
027	08	0	F	1	d	X	
028	09	0	F	1	d	X	
029	0A	0	F	1	d	X	
02A	0B	0	F	1	d	X	
02B	0C	0	F	1	d	0	End of Cycle
02C	0D	0	F	0	0	0	Wait for Data Out to
02D	0E	0	F	1	0	0	Go High
02E	0F	0	F	1	1	1	
02F	10	0	F	0	0	X	
030	11	0	F	1	0	X	Start of Erase/Write
031	12	0	F	1	1	X	Disable Cycle
032	13	0	F	1	0	X	
033	14	0	F	1	0	X	
034	15	0	F	1	0	X	
035	16	0	F	1	0	X	
036	17	0	F	1	0	X	
037	18	0	F	0	0	X	End of EWDS Command
038	19	0	F	0	0	X	

FILTER PARAMETER CONTROL

The LMC835 provides the complete resistor and switch set to implement a stereo 7 band equalizer or a mono 14 band system. While control of this device is usually provided from a microcontroller there are instances where that expense and effort are not necessary to achieve a complex filtering function.

To program the LMC835 one of fourteen frequency bands must be selected and the gain for that band entered. This band gain setting requires a minimum of 18 states. All fourteen bands must be preset and various control states must be implemented. Because of the large number of states involved in setting each of the fourteen bands a wider word is needed than can be implemented in a single PROM. There are several methods of dealing with this, however the most straight forward (for purposes of illustration) is to employ two PROMs.

The MICROWIRE interface used with the LMC835 differs slightly from those implemented above in that it uses a strobe to transfer data from the internal shift register to the latch for the addressed switch matrix. This permits the reprogramming of individual bands without the necessity of rewriting the entire machine state.

A complete logic diagram for the word generator is shown in *Figure 7*. The schematics for the implementation of the linear portions of the circuit can be obtained by referencing the LMC835 datasheet. A template for the PROM listing is also shown in *Figure 8*.

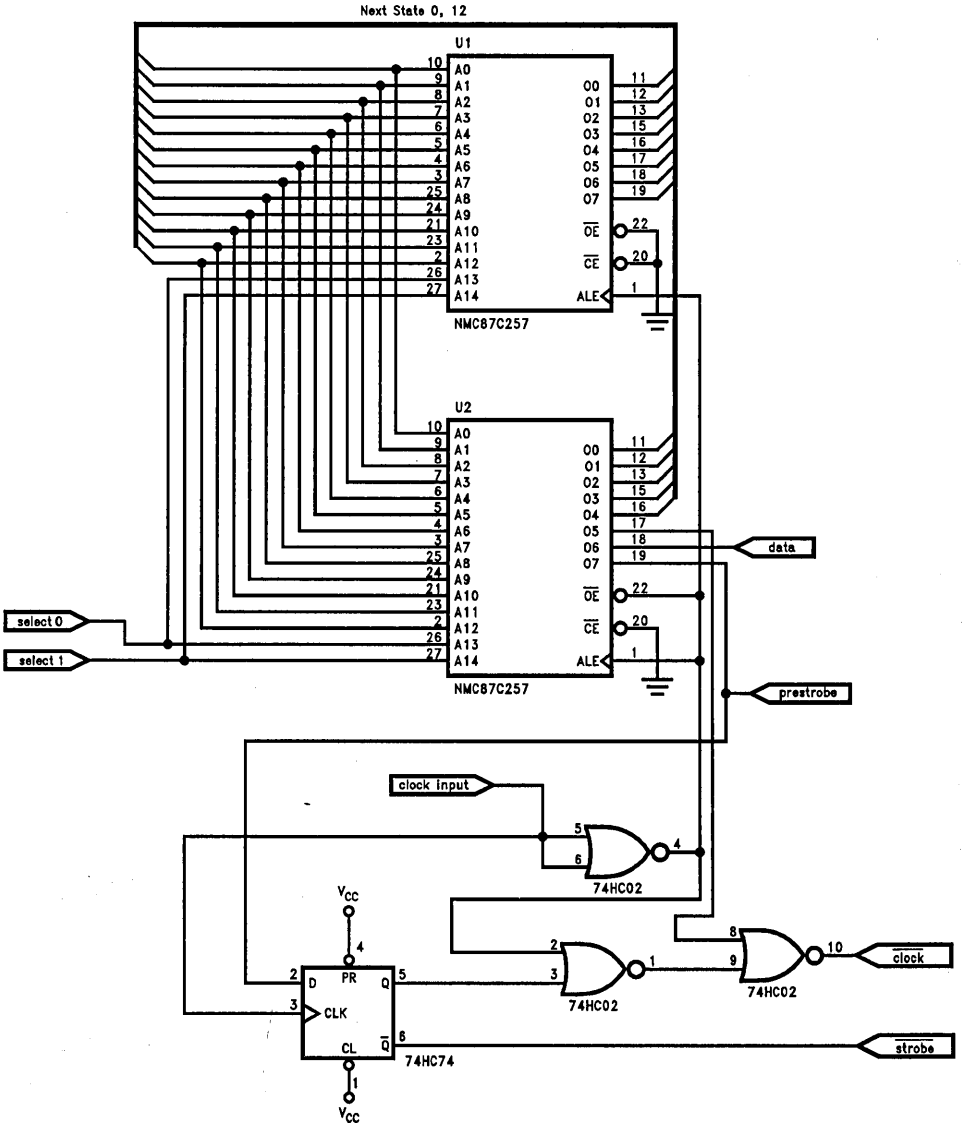

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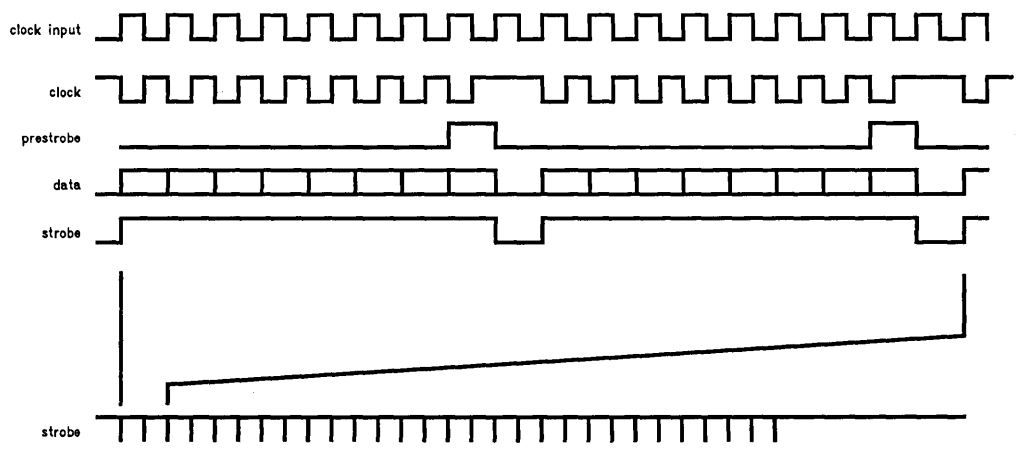
FIGURE 7. Logic Diagram for Equalizer Controller



Data / Prestrobe / Address																			
00	1	b	24	1	b	48	1	b	6C	1	b	90	1	b	B4	1	b	D8	1	b
01	1	b	25	1	b	49	1	b	6D	1	b	91	1	b	B5	1	b	D9	1	b
02	1	b	26	1	b	4A	1	b	6E	1	b	92	1	b	B6	1	b	DA	1	b
03	1	b	27	1	b	4B	1	b	6F	1	b	93	1	b	B7	1	b	DB	1	b
04	1	R	28	1	R	4C	1	R	70	1	R	94	1	R	B8	1	R	DC	1	R
05	1	R	29	1	R	4D	1	R	71	1	R	95	1	R	B9	1	R	DD	1	R
06	1	X	2A	1	X	4E	1	X	72	1	X	96	1	X	BA	1	X	DE	1	X
07	0	H	2B	0	H	4F	0	H	73	0	H	97	0	H	BB	0	H	DF	0	H
08	1	0	2C	1	0	50	1	0	74	1	0	98	1	0	BC	1	0	E0	1	0
09	1	g	2D	1	g	51	1	g	75	1	g	99	1	g	BD	1	g	E1	1	g
0A	1	g	2E	1	g	52	1	g	76	1	g	9A	1	g	BE	1	g	E2	1	g
0B	1	g	2F	1	g	53	1	g	77	1	g	9B	1	g	BF	1	g	E3	1	g
0C	1	g	30	1	g	54	1	g	78	1	g	9C	1	g	C0	1	g	E4	1	g
0D	1	g	31	1	g	55	1	g	79	1	g	9D	1	g	C1	1	g	E5	1	g
0E	1	g	32	1	g	56	1	g	7A	1	g	9E	1	g	C2	1	g	E6	1	g
0F	1	B	33	1	B	57	1	B	7B	1	B	9F	1	B	C3	1	B	E7	1	B
10	0	L	34	0	L	58	0	L	7C	0	L	A0	0	L	C4	0	L	E8	0	L
11	1	0	35	1	0	59	1	0	7D	1	0	A1	1	0	C5	1	0	E9	1	0
12	1	b	36	1	b	5A	1	b	7E	1	b	A2	1	b	C6	1	b	EA	1	b
13	1	b	37	1	b	5B	1	b	7F	1	b	A3	1	b	C7	1	b	EB	1	b
14	1	b	38	1	b	5C	1	b	80	1	b	A4	1	b	C8	1	b	EC	1	b
15	1	b	39	1	b	5D	1	b	81	1	b	A5	1	b	C9	1	b	ED	1	b
16	1	R	3A	1	R	5E	1	R	82	1	R	A6	1	R	CA	1	R	EE	1	R
17	1	R	3B	1	R	5F	1	R	83	1	R	A7	1	R	CB	1	R	EF	1	R
18	1	X	3C	1	X	60	1	X	84	1	X	A8	1	X	CC	1	X	F0	1	X
19	0	H	3D	0	H	61	0	H	85	0	H	A9	0	H	CD	0	H	F1	0	H
1A	1	0	3E	1	0	62	1	0	86	1	0	AA	1	0	CE	1	0	F2	1	0
1B	1	g	3F	1	g	63	1	g	87	1	g	AB	1	g	CF	1	g	F3	1	g
1C	1	g	40	1	g	64	1	g	88	1	g	AC	1	g	D0	1	g	F4	1	g
1D	1	g	41	1	g	65	1	g	89	1	g	AD	1	g	D1	1	g	F5	1	g
1E	1	g	42	1	g	66	1	g	8A	1	g	AE	1	g	D2	1	g	F6	1	g
1F	1	g	43	1	g	67	1	g	8B	1	g	AF	1	g	D3	1	g	F7	1	g
20	1	g	44	1	g	68	1	g	8C	1	g	B0	1	g	D4	1	g	F8	1	g
21	1	B	45	1	B	69	1	B	8D	1	B	B1	1	B	D5	1	B	F9	1	B
22	0	L	46	0	L	6A	0	L	8E	0	L	B2	0	L	D6	0	L	FA	0	L
23	1	0	47	1	0	6B	1	0	8F	1	0	B3	1	0	D7	1	0	FB	0	0

band selection bits
range, Ch, B
range, Ch, A
don't care
DATA I
gain selection bits
boost/cut
DATA II
NEXT ADDR = 00

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FIGURE 8. Template for PROM Program for Filter Controller

SUMMARY

The use of the NMC87C257 CMOS PROM with latches has been shown to be an effective element in the implementation of several MICROWIRE interfaces. This use allows the designer to implement systems with devices necessitating a MICROWIRE interface without the use of a microcontroller or microprocessor.

In constructing or adapting any of the circuits described in this note the reader is advised to obtain copies of the National Semiconductor data sheets for the components included and to review their operation for applicability to their system requirements.

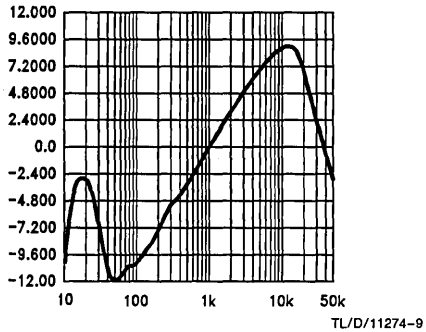


FIGURE A1. A Ramp Transfer Characteristic. Refer to Table A1 for program inputs.

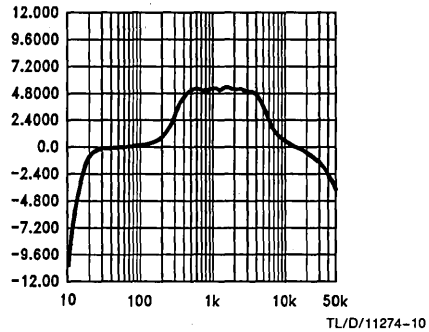


FIGURE A2. Vocal Presence Filter. Refer to Table A2 for program inputs.

TABLE A1. Program Inputs for Ramp Transfer Characteristic

Frequency (Hz)	Level (dB)
40	−7
63	−6
100	−5
160	−4
250	−3
400	−2
630	−1
1k	0
1.6k	+1
2.5k	+2
4k	+3
6.3k	+4
10k	+5
16k	+6

TABLE A2. Program Inputs for Vocal Presence Filter

Frequency (Hz)	Level (dB)
40	0 Subsonic Filter
63	0
100	0
160	0
250	0
400	+3
630	+3
1k	+3
1.6k	+3
2.5k	+3
4k	+3
6.3k	0 Supersonic Filter
10k	0
16k	0

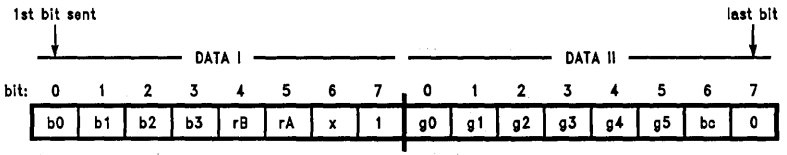
Figures A1 and *A2* are gain vs. frequency plots of specimen filters realized using the logic of *Figure 7* and PROM code generated with SM835.c.

```
/*************************************************************
*                                                            *
* File: SM835.C                                              *
* Author: Bob Moses, Rane Corporation, Mukilteo, WA          *
* Revision: 18 June 1991                                     *
* Compiler: Borland TurboC                                   *
*                                                            *
* Description: Generates Intel Hex file for NMC87C257 based  *
*              LMC835 state machine loader.                  *
*                                                            *
* File Input:  void                                          *
* File Output: SML835.HEX                                    *
*                                                            *
*************************************************************/

#include "stdio.h"

/*------------*/
/* Data Types */
/*------------*/

struct LMC835_RECORD
{
    int chAbands[7];   /* gains for chan A bands */
    int chArng;        /* chan A range */
    int chBbands[7];   /* gains for chan B bands */
    int chBrng;        /* chan B range */
};

/*--------------------*/
/* Function Prototypes*/
/*--------------------*/

void say_howdy(void);
void get_parameters(struct LMC835_RECORD *eq);
void compile_state_mach(struct LMC835_RECORD *eq, unsigned int states[]);
void output_data(unsigned int states[]);
void wr_ihex_data_rec(FILE *outfile, unsigned int addr, unsigned char recsize,
                      unsigned char data[]);

/*-------------*/
/* Main Program */
/*-------------*/

main()
{
    /* declare one LMC835 equalizer */
    struct LMC835_RECORD eql;
```

```
    /* 14 bands * 2 blocks/band * 9 states/block + final state = 253 states */
    unsigned int states[253];

    say_howdy();
    get_parameters(&eql);
    compile_state_mach(&eql,states);
    output_data(states);
}

/*------------*/
/* Functions  */
/*------------*/

void say_howdy(void)
{
    clrscr();
    fprintf(stdout,"\nSM835 - NMC87C257 LM835 State Machine Loader.");
    fprintf(stdout,"\n\nThis Program accepts parameters for an LMC835-based");
    fprintf(stdout,"\nequalizer and generates an Intel Hex file ( SML835.HEX )");
    fprintf(stdout,"\nfor the NMC87C257 State Machine Loader. This file can be");
    fprintf(stdout,"\nloaded into most EPROM programmers and split-programmed");
    fprintf(stdout,"\n(even and odd bytes) into two EPROMs.");
    fprintf(stdout,"\n\nThe LMC835 graphic equalizer consists of two channels");
    fprintf(stdout,"\n(chan A & chan B), each channel has 7 bands. The range of");
    fprintf(stdout,"\neach band is selectable for ± 12 dB in 1 dB steps, or");
    fprintf(stdout,"\n± 6 dB in 1/2 dB steps.\n");
}

void get_parameters(struct LMC835_RECORD *eq)
{
    unsigned int i,currng;
    int tempint;
    char chan;
    float tempfloat;

    /* get range for chan A */
    fprintf(stdout,"\nPlease enter range of chan A (0 = ±12dB, 1 = ±6dB): ");
    fscanf(stdin,"%d",&tempint);
    eq->chArng = tempint&0x0001;

    /* get range for chan B */
    fprintf(stdout,"Please enter range of chan B (0 = ±12dB, 1 = ±6dB): ");
    fscanf(stdin,"%d",&tempint);
    eq->chBrng = tempint&0x0001;
```

```
    /* get EQ bands */
    for(i = 0,chan = 'A',currng = 12-6*(eq->chArng);i < 14;)
    {
        /* if start of chan B, modify chan flag and chan range variables */
        if(i == 7)
        {
            chan = 'B';
            currng = 12-6*(eq->chBrng);
        }
        /* get a band value */
        fprintf(stdout,"Gain of chan %c band #%d? ",chan,(i%7)+1);
        fscanf(stdin,"%g",&tempfloat);

        /* scale for range */
        if(currng == 6) tempint = (int)(tempfloat*2.0);
        else tempint = (int)tempfloat;

        /* check limits */
        if((tempint > 12) || (tempint < -12))
        {
            fprintf(stderr,"...err! value must be between -%d and +%d\n",currng,currng);
            continue;
        }
        /* save band */
        if(chan == 'A') eq->chAbands[i] = tempint;
        else eq->chBbands[i-7] = tempint;
        i++; /* band counter */
    }
}
void compile_state_mach(struct LMC835_RECORD *eq, unsigned int states[])
{
```

LMC835 CONTROL CODES



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/*

State Machine:

State Current	State Next	Data	Outputs Prestrobe	Outputs CLK Enable
0	1	Chan A, band 1, DATA I b0	0	0
1	2	Chan A, band 1, DATA I b1	0	0
2	3	Chan A, band 1, DATA I b2	0	0
3	4	Chan A, band 1, DATA I b3	0	0
4	5	Chan A, band 1, DATA I rB	0	0
5	6	Chan A, band 1, DATA I rA	0	0
6	7	Chan A, band 1, DATA I x	0	0
7	8	Chan A, band 1, DATA I 1	1	0
8	9	rest for strobe	0	0
9	9	Chan A, band 1, DATA II g0	0	0
10	11	Chan A, band 1, DATA II g1	0	0
11	12	Chan A, band 1, DATA II g2	0	0
12	13	Chan A, band 1, DATA II g3	0	0
13	14	Chan A, band 1, DATA II g4	0	0
14	15	Chan A, band 1, DATA II g5	0	0
15	16	Chan A, band 1, DATA II bc	0	0
16	17	Chan A, band 1, DATA II 0	1	0
17	18	rest for strobe	0	0
18	19	Chan A, band 2, DATA I b0	0	0
:	:	:	:	:
34	35	Chan A, band 2, DATA II 0	1	0
35	36	rest for strobe	0	0
:	:	:	:	:
124	125	Chan A, band 7, DATA II 0	1	0
125	126	rest for strobe	0	0
126	127	Chan B, band 1, DATA I b0	0	0
:	:	:	:	:
250	251	Chan B, band 7, DATA II 0	1	0
251	252	rest for strobe	0	0
252	252	0	0	1

NMC87C257 pin connections:

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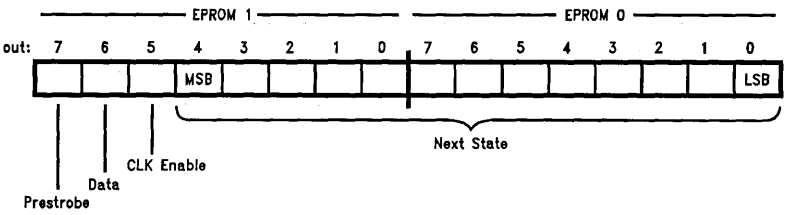

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/*

```
    unsigned int band,substate,stateimg,curstate;
    unsigned char LMC835GainCodeTable[] = {0x2F,0x2D,0x29,0x01,0x16,0x2A,
                                           0x12,0x02,0x04,0x08,0x10,0x20,
                                           0x00,
                                           0x20,0x10,0x08,0x04,0x02,0x12,
                                           0x2A,0x16,0x01,0x29,0x2D,0x2F};

    /*--------*/
    /* chan A */
    /*--------*/

    for(band = 0,curstate = 0;band < 7;band++)
    {
        for(substate = 0;substate < 18;substate++)
        {
            /* next state = current state +1 */
            stateimg = (curstate+1)&0x1FFF;

            /* CLK Enable */
            stateimg &= 0xDFFF;

            /* Prestrobe */
            if((substate == 7)||(substate == 16)) stateimg += 0x8000;

            /* Data */
            switch(substate)
            {
                case 0: /* DATA I b0 */
                    stateimg += (((band+1)&0x0001)<<14);
                    break;
                case 1: /* DATA I b1 */
                    stateimg += (((band+1)&0x0002)<<13);
                    break;
                case 2: /* DATA I b2 */
                    stateimg += (((band+1)%0x0004)<<12);
                    break;
                case 3: /* DATA I b3 */
                    stateimg += (((band+1)%0x0008)<<11);
                    break;
                case 4: /* DATA I rB */
                    stateimg += (((eq->chBrng)&0x0001)<<14);
                    break;
                case 5: /* DATA I rA */
                    stateimg += (((eq->chArng)&0x0001)<<14);
                    break;
                case 6: /* DATA I don't care */
                    break;
                case 7: /* DATA I 1 */
                    stateimg += 0x4000;
                    break;
*/
```

```
            case 8: /* rest for strobe */
                break;
            case 9: /* DATA II g0 */
                stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0001)<<14);
                break;
            case 10: /* DATA II g1 */
                stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0002)<<13);
                break;
            case 11: /* DATA II g0 */
                stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0004)<<12);
                break;
            case 12: /* DATA II g3 */
                stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0008)<<11);
                break;
            case 13: /* DATA II g4 */
                stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0010)<<10);
                break;
            case 14: /* DATA II g5 */
                stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0020)<<9);
                break;
            case 15: /* DATA II bc ( 0 = cut, 1 = boost) */
                if(eq->chAbands[band] < 0) stateimg &= 0xBFFF;
                else stateimg += 0x4000;
                break;
            case 16: /* DATA II 0 */
                stateimg &= 0xBFFF;
                break;
            case 17: /* rest for strobe */
                break;
        } /* switch... */

        /* write this state to states array */
        states[curstate++] = stateimg;

    } /* for(substate... */
} /* for(band... */

/*--------*/
/* chan B */
/*--------*/

for(band = 7;band < 14;band++)
{
    for(substate = 0;substate < 18;substate++)
    {
        /* next state = current state +1 */
        stateimg = (curstate+1)&0x1FFF;

        /* CLK Enable */
        stateimg &= 0xDFFF;
```

```
/* Prestrobe */
if((substate == 7)||(substate == 16)) stateimg += 0x8000;

/* Data */
switch(substate)
{
    case 0: /* DATA I b0 */
        stateimg += (((band+1)&0x0001)<<14);
        break;
    case 1: /* DATA I b1 */
        stateimg += (((band+1)&0x0002)<<13);
        break;
    case 2: /* DATA I b2 */
        stateimg += (((band+1)&0x0004)<<12);
        break;
    case 3: /* DATA I b3 */
        stateimg += (((band+1)&0x0008)<<11);
        break;
    case 4: /* DATA I rB */
        stateimg += (((eq->chBrng)&0x0001)<<14);
        break;
    case 5: /* DATA I rA */
        stateimg += (((eq->chArng)&0x0001)<<14);
        break;
    case 6: /* DATA I don't care */
        break;
    case 7: /* DATA I 1 */
        stateimg += 0x4000;
        break;
    case 8: /* rest for strobe */
        break;
    case 9: /* DATA II g0 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0001)<<14);
        break;
    case 10: /* DATA II g1 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0002)<<13);
        break;
    case 11: /* DATA II g2 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0004)<<12);
        break;
    case 12: /* DATA II g3 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0008)<<11);
        break;
    case 13: /* DATA II g4 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0010)<<10);
        break;
```

```
                case 14: /* DATA II g5 */
stateimg +=((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0020)<<9);
                    break;
                case 15: /* DATA II bc ( 0 = cut, 1 = boost) */
                    if(eq->chBbands[band-7] < 0) stateimg &= 0xBFFF;
                    else stateimg += 0x4000;
                    break;
                case 16: /* DATA II 0 */
                    stateimg &= 0xBFFF;
                    break;
                case 17: /* rest for strobe */
                    break;
            } /* switch... */

            /* write this state to states array */
            states[curstate++] = stateimg;

        } /* for(substate... */
    } /* for(band... */

    /* final state: "jump 0" with clock disabled */
    states[252] = 252+0x2000;
}

void output_data(unsigned int states[])
{
    unsigned int i,addr,bitmask;
    unsigned char csum,data[16];
    FILE *outfile;

    /* open output file */
    if((outfile = fopen("sml835.hex","w")) == NULL )
    {
        fprintf(stderr,"can't open file SML835.HEX");
        exit(0);
    }

    /* write states to stdout */
    /*------------------------*/
    for(i = 0;i < 253;i++)
{
        if(i == 252) fprintf(stdout,"\n\nFinal state...");
        else if (!(i&18)) fprintf(stdout,"\n\nBand %d...",(i/18)+1);
        fprintf(stdout,"\nState %d: ",i);

        /* write each state as a binary image  */
        for(bitmask = 0;bitmask < 16;bitmask++)
        {
            if((states[i]<<bitmask)&0x8000) fprintf(stdout,"1");
            else fprintf(stdout,"0");
        }
    }
```

```
    /* write states to Intel Hex file */
    /*-------------------------------*/
    fprintf(stdout,"\n\nWriting Intex Hex file: SML835.HEX...\n");

    /* write first 252 states */
    for(addr = 0;addr < 252;addr += 8)
    {
        /* copy 8 states (16 bytes) to temp data buffer */
        for(i = 0;i < 16;i += 2)
        {
            data[i] = (char)(states[addr+(i/2)]&0x00FF);
            data[i+1] = (char)((states[addr+(i/2)]>>8)*0x00FF);
        }

        /* write data to Intex Hex record */
        wr_ihex_data_rec(outfile,addr*2,16,data);
    }

    /* write last state */
    data[0] = (char)(states[252]&0x00FF);
    data[1] = (char)((states[252]>>8)&0x00FF);
    wr_ihex_data_rec(outfile,252*2,2,data);

    /* EOF record */
    fprintf(outfile,"\n:00000001FF");

    /* close file */
    fclose(outfile);
}

void wr_ihex_data_rec(FILE *outfile, unsigned int addr, unsigned char recsize, unsigned char
data[])
{
    unsigned int i;
    unsigned char csum;

    /* record mark, record length, record address, and record type fields */
    fprintf(outfile,"\n:%2.2X%4.4X00",recsize,addr);
    csum = recsize + (char))addr&0x00FF) + (char)((addr>>8)&0x00FF);

    /* data field */
    for(i = 0;i < recsize;i++)
    {
        fprintf(outfile,"%2.2X",data[i]);
        csum += data[i];
    }

    /* checksum field */
    csum &= 0x00FF;
    csum *= -1;
    fprintf(outfile,"%2.2X",csum);
}
```

BIBLIOGRAPHY

NMC87C257 — CMOS PROM with Address Latches

ADC0854 — Multiplexed Comparator with 8-bit Reference Divider

FSA2619 — Monolithic Diode Array

MM74C14 — Hex CMOS Schmitt Trigger

NM93C06 — 256-bit Electrically Erasable Programmable Memory

MM74C923 — 20 Key Encoder

LMC35 — Digital Controlled Graphic Equalizer

AN-452 — MICROWIRE Serial Interface

AN-140 — CMOS Schmift Trigger

Appendix

ACKNOWLEDGEMENTS

The author would like to express his gratitude to the engineering staff at Rane Corporation in Mukilteo, Washington for providing expert assistance and breadboarding of the LMC835 application and to Bob Moses for contributing a C program (see Appendix) to generate the ROM map.

NM95C12 Applications in a PC-AT® Ethernet® Adapter

National Semiconductor
Application Note 792
Sean Long

INTRODUCTION

This application describes a typical Ethernet adapter card designed to be plugged into a PC-AT expansion slot. The board is designed around the National Semiconductor DP83932 SONIC™ Network Controller device. This application note will detail the system design and focus on the functions performed by the NM95C12 EEPROM.

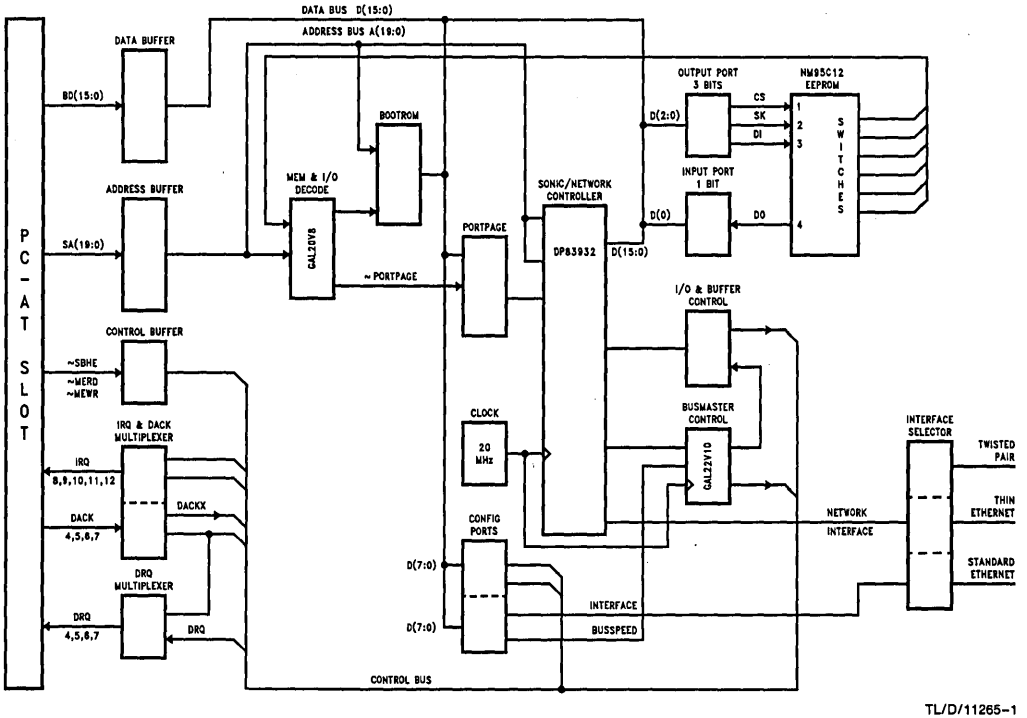
This application note assumes that the reader is familiar with the PC-AT architecture, the DP83932 device, the NM95C12 EEPROM and designing with GAL® Programmable Logic Devices (PLDs).

SYSTEM DESCRIPTION

The network controller card has been designed to meet the following specifications:

- Designed around high performance 32-bit DP83932 Ethernet Controller
- 16-Bit bus master operation to give higher performance
- Fully software configurable (no jumpers or mechanical DIP switches)
- Extensive test and configuration capabilities
- Supports different media interfaces
- Bootrom option

The system block diagram is shown in *Figure 1*.



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*Denotes an active low signal.

FIGURE 1. System Block Diagram

FUNCTIONAL DESCRIPTION OF THE BOARD

The system contains the following logical functions:

1. Network controller (DP83932)
2. Cable interfaces
3. Busmaster interface logic, including data and address buffers
4. EPROM option for remote boot loader

This system uses both the EEPROM locations and the switch logic terminals of the NM95C12 to perform various functions within the system as detailed below.

FUNCTIONAL DESCRIPTION OF NM95C12 EEPROM

Use of the Switches:

The switch terminals of the NM95C12 EEPROM are used as part of the memory map address decoding and the I/O map decoding circuitry, feeding as inputs to a GAL20V8 which performs the address decoding logic from the system address inputs.

The NM95C12 switches control:

1. The base I/O address of the network controller board.
2. The base memory address of the bootrom EPROM option on the board.

ADDRESS DECODING

The address decoding is controlled by a GAL20V8 PLD (refer to the 1990 National Semiconductor PLD Databook and Design Guide for further information) as shown in *Figure 2*.

The inputs to the GAL20V8 are the system address lines, the memory and I/O control signals, and the switch terminals from the NM95C12. The outputs from the GAL20V8 are the various chip select signals for the memory and I/O ports. The system address bus transmits the current address value and the M/~IO signal determines if a memory or I/O cycle is in progress.

Address lines A0–A19 allow up to 1 Meg (0–FFFFF) of memory to be addressed, while address lines A0–A15 allow up to 64K (0-FFFF) of I/O ports to be addressed. If the control signal M/~IO is logical "1" (high) then the processor is performing a memory cycle and if the M/~IO signal is logical "0" then an I/O cycle is in operation.

For a PC-AT various memory and I/O locations are reserved for standard functions such as system memory and I/O (refer to PC-AT documentation to determine which memory and I/O locations are free for add-in boards).

The switch outputs from the NM95C12 are connected as inputs to the GAL address decode logic and are used to determine the base memory and I/O locations for the add-in card. *Figure 2* shows the typical use of a GAL for address decoding.

The advantage of using a PLD for the address decoding is that it is an easy way to implement different address decode functions by logic equations. The logic equations can be implemented with a standard PLD design compiler such as OPAL™ from National Semiconductor or a third party software package such as ABEL™ from Data I/O. The PLD compiler will take the logic equations and convert them into the GAL fuse map which can be used for programming on a wide range of device programmers. A typical set of logic equations using National Semiconductors OPAL software package is shown in *Figure 3*.

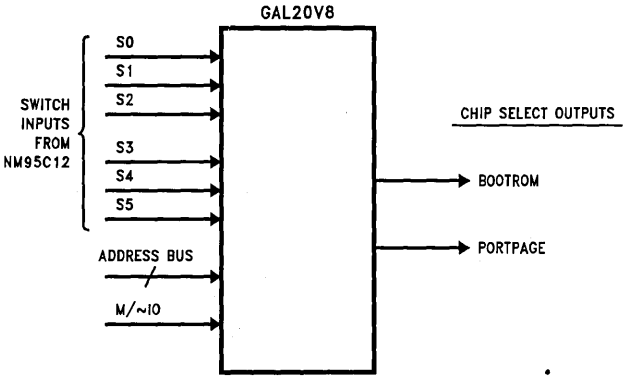

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FIGURE 2. Address Decoding

```
BEGIN HEADER
TITLE    Address decoding for PC AT Ethernet adapter card
PATTERN  Addr_Dec
REVISION Rev 0
AUTHOR   Dave Engineer
COMPANY  National Semiconductor
DATE     June 1991
Everything in the header command is copied directly into the JEDEC map as a comment field for
easy documentation
END HEADER

BEGIN DEFINITIONS
device G20V8;                                  { specify the device used }
inputs s0, s1, s2, s3, s4, s5;                 { define the inputs }
inputs m_~io, a0, a1, a2, a3, a4, a5;
outputs(com) bootroom, portpage;               {define the outputs}
{ OPAL will perform automatic pin assignment }
set ioselect=[s2,s1,s0], memselect=[s5,s4,s3]; { define the switch sets }
set address=[a5,a4,a3,a2,a1,a0];
END DEFINITIONS

BEGIN EQUATIONS
{ " / " = logical NOT function (i.e. logical 0)
  " & " = logical AND function
  " + " = logical OR function }
{ if m_~io is logical 0, then decode switch set s2, s1, s0 and address lines for the various
base I/O locations.
  Refer to PC-AT system I/O address map before selecting free I/O ports, the decodes shown are
  for example only - change for specific applications as required. }
bootrom = /m_~io & ( (ioselect == 0) & (address == ↑h00)
                   + (ioselect == 1) & (address == ↑h01)
                   + (ioselect == 2) & (address == ↑h02)
                   + (ioselect == 3) & (address == ↑h03)
                   + (ioselect == 4) & (address == ↑h04)
                   + (ioselect == 5) & (address == ↑h05)
                   + (ioselect == 6) & (address == ↑h06));
{ if m_~io is logical 1, then decode switch set s5, s4, s3 and address line for the various
base memory locations.
  Refer to PC-AT system I/O address map before selecting free Memory locations, the decodes
  shown are for example purposes only - change for specific applications as required. }
portpage = m_~io & ( (memselect == 0) & (address == ↑h18)
                   + (memselect == 1) & (address == ↑h20)
                   + (memselect == 2) & (address == ↑h28)
                   + (memselect == 3) & (address == ↑h30)
                   + (memselect == 4) & (address == ↑h38);
END EQUATIONS
```

FIGURE 3. GAL® Logic Equations

USE OF THE NM95C12 EEPROM LOCATIONS

1. Three locations are used to store the ethernet address of the card.
2. One location is used to store the interrupt number and the DMA channel of the board.
3. One location is used to store the busmaster speed setting of the card.
4. Two locations are used to store information about the production flow of the board e.g.; the version number of the out-going inspection, and serialization program which stores a unique ethernet address in the EEPROM.
5. There are also some EEPROM locations used to enable some special features in the network driver such as protocol, DMA priority, etc.

Figure 4 below shows the memory usage of the NM95C12.

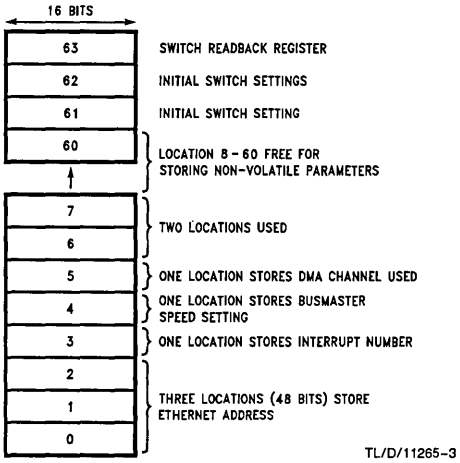

FIGURE 4. Memory Locations Used in NM95C12

FUNCTIONAL DESCRIPTION OF THE SOFTWARE

The driver for the card can be supplied in two ways:

1. As a driver which is loaded from the disk.

2. As a bootrom which is located at the card.

The driver determines the base I/O address of the card. This is done by scanning the possible I/O map where the card can be located (seven possible locations) and testing if the NM95C12 EEPROM can be found.

The EEPROM is found if, after an address is shifted in the EEPROM, the DO output from the NM95C12 has become logical "zero". Then the CS pin will be disabled and there will be a check if the DO output pin will become high (this pin is pulled up with a 47K resistor).

When the software finds the base address of the card, it reads the locations which contain the DMA and IRQ number to use and programs these values into the corresponding output latches. These latches will enable and/or multiplex the corresponding DMA (DACKx, DRQx) and INT (IRQx) to the busmaster logic and interrupt logic.

The same operation is done for the busmaster speed, one location in the EEPROM determines the active low and high time for busmaster cycles, the output of this latch will go to the busmaster state machine (implemented in a GAL22V10).

The ethernet address will be read by the driver and copied to a private location in the driver data area for use with the network software.

The bootrom can be located at five locations in memory (controlled by the NM95C12 switch logic) and can be disabled if required.

CONCLUSION

This application has shown the many advantages of the NM95C12 EEPROM with DIP Switches. In this example the NM95C12 replaces the functions typically performed by a Bipolar PROM (store ethernet address), mechanical DIP switches/jumpers (select options), and general read/write logic (software testing of the hardware configuration). The use of the switch terminals as part of the address decode logic makes the address decode function more flexible and allows for software control.

The easy interfacing to the NM95C12 (just four pins) and the simple, but powerful instruction set allows the NM95C12 to give the system designer:

- Greater flexibility
- Fully software controllable and testable
- Greater reliability (no mechanical switches or jumpers)
- Reduced component count
- Lower component cost

Using an EEPROM— I²C Interface NM24C02/03/04/05/08/09/16/17

National Semiconductor
Application Note 794
N. Brian Underwood

INTRODUCTION

National Semiconductor's NM24C EEPROMs are designed to interface with Inter-Integrated Circuit (I²C) buses and hardware. NSC's electrically erasable programmable read only memories (EEPROMs) offer valuable security features (write protection), two write modes, three read modes and a wide variety of memory sizes. Applications for the I²C bus and NM24C memories are included in SANs (small-area networks), stereos, televisions, automobiles and other scaled-down systems that don't require tremendous speeds but instead cost efficiency and design simplicity.

I²C BACKGROUND

The I²C bus configuration is an amalgam of microcontrollers and peripheral controllers. By definition: a device that transmits signals onto the I²C bus is the "transmitter" and a device that receives signals is the "receiver"; a device that controls signal transfers on the line in addition to controlling the clock frequency is the "master" and a device that is controlled by the master is the "slave". The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. It is possible to combine several masters, in addition to several slaves, onto an I²C bus to form a multimaster system. If more than one master simultaneously tries to control the line, an arbitration procedure decides which master gets priority. The maximum number of devices connected to the bus is dictated by the maximum allowable capacitance on the lines, 400 pF, and the protocol's addressing limit of 16k; typical device capacitance is 10 pF. Up to eight E²PROMs can be connected to an I²C bus, depending on the size of the memory device implemented.

Simplicity of the I²C system is primarily due to the bidirectional 2-wire design, a serial data line (SDA) and serial clock line (SKL), and to the protocol format. Because of the efficient 2-wire configuration used by the I²C interface compared to that of the MICROWIRE™ and SPI interface, reduced board space and pin count allows the designer to have more creative flexibility while reducing interconnecting cost.

OPERATING NATIONAL SEMICONDUCTOR'S NM24Cs

The NM24C E²PROMs require only six simple operating codes for transmitting or receiving bits of information over the 2-wire I²C bus. These fields are explained in greater detail below and briefly described hereafter: a start bit, a 7-bit slave address, a read/write bit which defines whether the slave is a transmitter or receiver, an acknowledge bit, message bits divided into 8-bit segments and a stop bit.

For efficient and faster serial communication between devices, the NM24C Family features page write and sequential read.

The NM24C03/C05/C09/C17 Family offers a security feature in addition to standard features found in the NM24C02/C04/C08/C16 Family. The security feature is beneficial in that it allows Read Only Memory (ROM) to be implemented in the upper half of the memory to prevent any future programming in that particular chip section; the remaining memory that has not been write protected can still be programmed. The security feature in the NM24C03/C05/C09/C17 Family does not require immediate implementation when the device is interfaced to the I²C bus, which gives the designer the option to choose this feature at a later date. Table I displays the following parameters: memory content, write protect and the maximum number of individual I²C E²PROMs allowed on an I²C bus at one time if the total line capacitance is kept below 400 pF.

Code used to interface the NM24Cs with National Semiconductor's COP8 Microcontroller Family is listed in a latter section of this application note for further information to the reader.

TABLE I

Part No.	Number of 256x8 Page Blocks	Write Protect Feature	Max. Parts
NM24C02	1	No	8
NM24C03	1	Yes	8
NM24C04	2	No	4
NM24C05	2	Yes	4
NM24C08	4	No	2
NM24C09	4	Yes	2
NM24C16	8	No	1
NM24C17	8	Yes	1

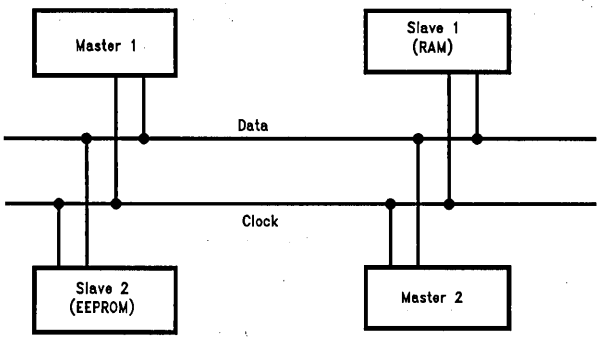

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FIGURE 1. I²C-Bus Configurations

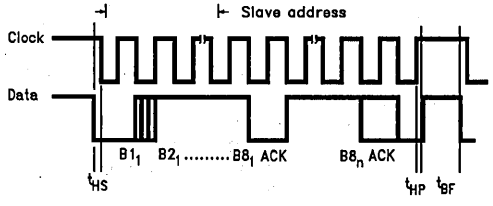

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FIGURE 2. I²C Bus Timing

Start Condition

— Clock and Data line high (Bus free)

— Change Data line from high to low

— After $t_{HS(Min)}$ = 4 μs the master supplies the clock

Acknowledge

— Transmitting device releases the Data line

— The receiving device pulls the Data line low during the ACK-clock if there is no error

— If there is no ACK, the master will generate a Stop Condition to abort the transfer

Stop Condition

— Clock line goes high

— After $t_{HP(Min)}$ = 4.7 μs the Data lines go high

— The master maintains the Data and Clock line high

— Next Start Condition after $t_{FB(Min)}$ = 4.7 μs is possible

START/STOP CONDITIONS

If both the data and clock lines are HIGH, the bus is not busy. To attain control of the bus, a start condition is needed from a master; and to release the lines, a stop condition is required.

Start Condition: HIGH-to-LOW transition of the data line while the clock line is in a HIGH state.

Stop Condition: LOW-to-HIGH transition of the data line while the clock line is in a HIGH state.

The master always generates the start and stop conditions. After the start condition the bus is in the busy state. The bus becomes free after the stop condition.

DATA BIT TRANSFER

After a start condition "S" one databit is transferred during each clock pulse. The data must be stable during the HIGH-period of the clock. The data line can only change when the clock line is at a LOW level.

Normally each data transfer is done with 8 data bits and 1 acknowledge bit (byte format with acknowledge).

ACKNOWLEDGE

Each data transfer needs to be acknowledged. The master generates the acknowledge clock pulse. The transmitter releases the data line (SDA = HIGH) during the acknowledge clock pulse. If there was no error detected, the receiver will pull down the SDA-line during the HIGH period of the acknowledge clock pulse.

If a slave receiver is not able to acknowledge, the slave will keep the SDA line HIGH and the master can then generate a STOP condition to abort the transfer.

If a master receiver keeps the SDA line HIGH, during the acknowledge clock pulse the master signals the end of data transmission and the slave transmitter release the data line to allow the master to generate a STOP-condition.

ARBITRATION

Only in multimaster systems.

If more than one device are potential masters and more than one desires access to the bus, an arbitration procedure takes place: if a master transmits a HIGH level and another master transmits a LOW level, the master with the LOW level will get the bus and the other master will release the bus; and the clock line switches immediately to the slave receiver mode. This arbitration could carry on through many bits (address bits and data bits are used for arbitration).

FORMATS

There are three data transfer formats supported:

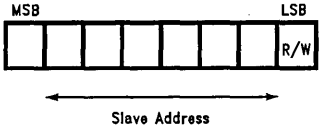
— Master transmitter writes to slave receiver; no direction change

— Master reads immediately after sending the address byte

— Combined format with multiple read or write tranfers.

ADDRESSING

The 7-bit address of an I²C device and the direction of the following data is coded in the first byte after the start condition:



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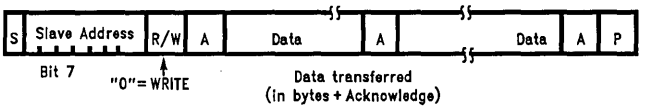
A "0" on the least significant bit indicates that the master will write information to the selected Slave address device; a "1" indicates that the master will read data from the slave.

Some slave addresses are reserved for future use. These are all addresses with the bit combinations 1111XXX and 0000XXX. The address 00000000 is used for a general call address, for example, to initialize all I²C devices (refer to I²C bus specification for detailed information).

Master Transmits to Slave, No Directon Change



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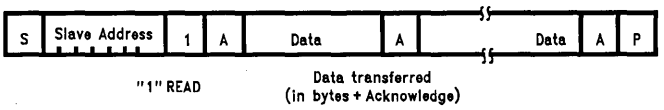
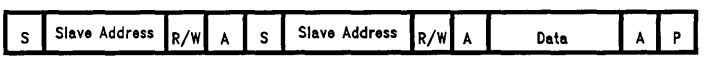
Master Reads Slave Immediately after First Byte



TL/D/11268–5

The master becomes a master receiver after first ACK

Combined Formats



TL/D/11268–6

n bytes Data + ACK n bytes Data + ACK

S = Start Condition A = Acknowledge P = Stop Condition

FIGURE 3. I²C-Bus Transfer Formats

TIMING

The master can generate a maximum clock frequency of 100 KHz. The minimum LOW period is defined as 4.7 μs; the minimum HIGH period width is 4 μs; the maximum rise time on SDA and SCL is 1 μs; and the maximum fall time on SDA and SCL is 300 ns.

Figure 4 shows the detailed timing requirements.

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	100	kHz
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
t_{HD}; STA	Hold Time Start Condition. After this Period the First Clock Pulse is Generated	4.0		μs
t_{LOW}	The LOW Period of the Clock	4.7		μs
t_{SU}; STA	Setup Time for Start Condition (Only Relevant for a Repeated Start Condition)	4.7		μs
t_{HD}; DAT	Data in Hold Time	5 0*		μs μs
t_{SU}; DAT	Setup Time Data	250		ns
t_r	Rise Time of Both SDA and SCL Lines		1	μs
t_f	Fall time of Both SDA and SCL Lines		300	ns
t_{SU}; STO	Setup Time for Stop Condition	4.7		μs

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

FIGURE 4. I²C-Bus Timing Requirements

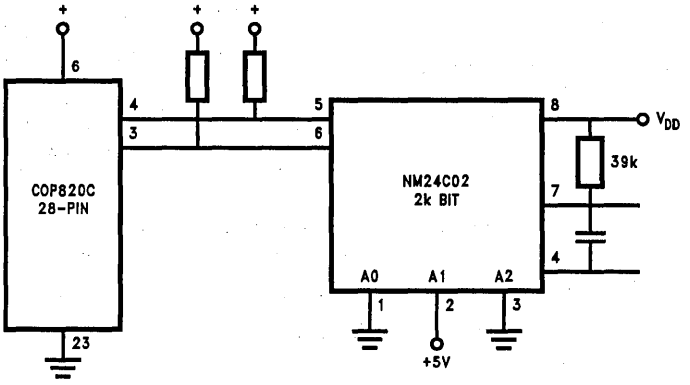


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FIGURE 5. I²C Bus EEPROM/μController Configuration Used for Sample Code

SOFTWARE TASKS

I. Write fixed values to E2PROM cells

II. Read values back from E2PROM and save in RAM locations from COP

Note: I²C Bus Modes Used:

Master Transmitter $\overset{SDA}{SCL}\rightarrow$ Slave Receiver

Master Receiver $\overset{SDA}{SCL}\rightarrow$ Slave Receiver

REMARKS

— The I²C bus, 2-wire serial interface generally requires a pull-up resistor on the SDA line and the SCL line, depending on whether TTL or CMOS hardware interfacing exists.

— I²C bus compatible μC's or peripherals have OPEN DRAIN outputs at SDA and SCL.

— COP800 does not have OPEN DRAIN outputs, but the "bus requirements" can be met by switching SDA and SCL connections into TRI-STATE® for the following cases:

The bus is not accessed

A slave has to send an acknowledge bit.

— MICROWIRE can not be used for I²C bus operations.

— Current sink capability on SDA and SCL must be 3 mA to maintain "Low Level" (an I²C bus spec.).

```
.TITLE IIC - EEPROM  ROUTINES'
.INCLD COP800.INC
.CHIP 840
.LIST X '21

          * * *TASK RELATED RAM - DECLARE* * *

EEADR                                          = 002      ;ADDRESS OF EEPROM
EEWRD                                          = 003      ;WORD ADDRESS EEPR.
EEDAT1                                         = 004      ;DATA TO EECELL
EEDAT2                                         = 005      ;SECOND BYTE
FLAG                                           = 010      ;FLAG–WORD
EEREAD                                         = 012      ;READ–DATA FROM EE
                                               = 013      ;SECOND BYTE
                                               = 014      ; THIRD BYTE
                                               = 015      ;FOURTH BYTE
BITCO                                          = 0F0      ;COUNTER FOR BITSHFT

INIT:
    LD SP,                                     #06F
    LD B,                                      PORTLD     ; INIT LS, L3 FOR EE-
    LD  [B+],                                  #00C       ;OPERATIONS
    LD [B],                                    #00C
    LD B,                                      #EEDAT2    ; INIT RAMS
    LD  [B-],                                  #034       ;FIXEED VALUES FOR
    LD  [B-],                                  #012       ; EEWRITE (2 BYTES)
    LD  [B-],                                  #0A0       ; MIRROR OF #05
    LD [B]                                     #025       ; MIRROR OF "A5"

        ;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
        ; EXAMPLE: IF ADDRESS BYTES IS    "1010 010X THEN    *
        ; STORE:                          "X010 0101         *
        ; INTO RAM (X=0/1; WRITE/READ)                       *
        ;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

    LD PSW,                                    #00        ;LOAD PSW
    LD CNTRL,                                  #00        ;AND CNTRL REG.
    LD FLAG,                                   #0
    .FORM

            ;  * * * * * * * * * * * * * * * * * * * * * * * * * * *
            ;  * * * *   DO WRITE TO EE-PROM   * * * *
            ;  * * * * * * * * * * * * * * * * * * * * * * * * * * *

          ; (2 BYTE SUCCESSIVE WRITE)

    SBIT 0,                                    FLAG       ;SET FLAG FOR WRITE
    LD B,                                      PORTLD     ;POINT LPORT DAT REG.
                                                          ;TO MODIFY "SDA, SCL"
    RBIT 2 [B],                                           ;PREPARE FOR START
    JSR STACON                                            ;CONDITION.
    JSR WAIT                                              ;AFTER WRITE TO EE.
                                                          ; WAIT FOR > THAT 40
```

TL/D/11268–8

```
                ************************
                ; ** DO THE START CONDITION **
                ; ** AND SHIFT OUT ADRESS - **
                ; ** BYTE AND WORD-ADRESS **
                ************************

STACON:
    RBIT 3,                          PORTLD      ;FINISH START COND.
    LD B,                            #EEADR      ;PREPARE TO CLOCK
                                                 ;OUT ADDRESS.
LOPA:
    LD BITCO,                        #0 0 8      ;DO SETS OF 8 BITS

LOPA 1:
    IFBIT 0, [B]                                 ;SWITCH SDA BEFORE
    JP ONE,                                      ;SCL
    RBIT 2,                          PORTLD      ; SET BIT LEVLE "0"
    JP CLK

ONE:
    SBIT 2,                          PORTLD      ; SET BIT LEVEL "1"
    JP CLK                                       ;ENSURE SAME BIT
                                                 ;LENGTH

CLK:
    SBIT 3,                          PORTLD      ;DO CLOCK PULSE
    NOP
    NOP
    RBIT 3,                          PORTLD      ;ENSURE> 4USEC
    RBIT 2,                          PORTLD      ;SWITCH ALSO SDA LOW
    .FORM

    LD A, [B]                                    ;ROTATE BYTE ONE
    RRC A,                                       ;BIT POS. RIGHT
    X A, [B]                                     ;AND SAVE
    DRSZ BITCO                                   ;CHECK IF 8 BITS
    JP LOPA1,                                    ;SHIFTED
    LD A, [B+],                                  ;DECREMENT 8
    IFBIT 1,                         FLAG        ;CHECK IF READ
    JMP,                             GETDAT      ;3RD BYTE IS NEXT?
                                                 ;IF SO, THEN READ.
    JSR ACK,                                     ;GET ACKNOWLEDGED
                                                 ;WHEN 8 BITS ARE
                                                 ;SHIFTED.
    IFBIT 0,                         FLAG        ;CHECK IF READ
    JP CEC1,                                     ;OR WRITE OPERATION.
    IFBNE                            #0 4        ;ON READ (HERE)
    JMP LOPA,                                    ;IF NOT 2 BYTES YET
    RET                                          ;AFTER EE-ADDRESS AND
                                                 ;WORD ADDRESS ARE SHFT.

CEC1:
    IFBNE,                           #0 6        ;1ST AND 2ND DATA-
    JMP LOPA,                                    ; BYTE (3RD + 4TH)
```

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```
                                                    ;NSEC TO PROPERLY
                                                    ;ERASE WRITE.

LD B,                                   #EEDAT2     ;INIT RAMS
LD  [B-],                               #078        ;ANOTHER 2 BYTES
LD  [B-],                               #056        ;OF FIXED DATA
LD  [B-],                               #0E0        ;MIRROR OF #07
LD [B],                                 #025        ;MIRROR OF "A5"
LD B,                                   PORTLD      ;POINT LPORT DAT REG.
                ;TO MODIFY "SDA, SCL"
RBIT 2, [B],                                        ;PREPARE FOR START
JSR STACON,                                         ;CONDITION.
JSR WAIT,                                           ;AFTER WRITE TO EE.
                                                    ;WAIT FOR > THAN 40
                                                    ;MSEC TO PROPERLY
                                                    ;ERASE WRITE.

.FORM

        ; ******************************
        ; **** DO READ FROM EE-PROM ****
        ; ******************************

            (READ 4 SUCCESSIVE BYTES)
RBIT 0                                  FLAG        ;INDICATE READ
LD B,                                   #EEWRD      ;INIT RAMS
LD  [B-],                               #0A0        ;MIRROR OF #05
LD [B],                                 #025        ;MIRROR OF "A5"

        ; ******************************
        ; ** FIRST 2 BYTES SAME AS IF WRITE **
        ; ******************************

                                (IN TERMS OF TRNSMIT)
LD B,                                   #PRTLD      ;PREPARE
RBIT 2 [B]                                          ;FOR
JSR STACON,                                         ;START COND.
                                                    ;AND SHIFT 1ST
                                                    ;2 BYTES.
SBIT 2,                                 PORTLD      ;PREPARE FOR
NOP,                                                ;ANOTHER START-
NOP,                                                ;CONDITION,
SBIT 3,                                 PORTLD      ;SDA HIGH FIRST.
SBIT 1,                                 FLAG        ;INDICATE THAT
                                                    ;3RD BYTE IS NEXT
LD B,                                   #EEWRD      ;INIT RAMS
LD  [B-],                               #0A0        ;MIRROR OF #05
LD [B],                                 #0A5        ;MIRROR OF "A5"
                                                    ;PERFORM ANOTHER
RBIT 2, [B],                            PORTLD      ;START
JSR STACON
RBIT 1,                                 FLAG
JMP INIT                                            ;CLOSE THE LOOP WHEN
.FORM                                               ;FINISHED
```

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```
STP:
    SBIT 3,                          PORTLD      ; ESTABLISH STOP-
    NOP,                                         ; CONDITION
    SBIT 2,                          PORTLD
    RET,
    .FORM

        ********************************
        ;* *  GET 8BIT OF DATA FROM EE-PROM * *
        ********************************

GETDAT:
    JSR ACK,                                     ; GET ACKNOWLEDGMENT
    LD B,                            #EEREAD     ; POINT FIRST READ RAM
    JP                               GETDT1      ; AND READ IN

GETDAT:
    JSR ACK,                                     ; ACKNOWLEDGMENT TO EE-
                                                 ; PROM WHEN 8 BITS
                                                 ; ARE SHIFTED IN.

GETDAT1:
    LD BITCO,                        #0 0 8      ; INIT BIT COUNTER
    RBIT 2,                          PORTLC      ; BEFORE READING, PUT
    RBIT 2,                          PORTLD      ; 'SDA' INTO HIGH-Z.

LOPB:
    SBIT 3,                          PORTLD      ; DO CLOCK HIGH
    RBIT 7, [B]                                  ; READ IN EEDATA
    IFBIT 2,                         PORTLD      ; IN SETS OF 8 BITS
    SBIT 7, [B]
    RBIT 3,                          PORTLD      ; DO CLOCK LOW
    DRSZ BITCO,                                  ; CHECK IF 8 BITS
    JP SHFT                                      ; ARE SHIFTED
    LD A, [B+],                                  ; INCREMENT B
    IFBNE                            #0 6        ; CHECK IF 4 BYTES
    JMP GETDT,                                   ; ARE SHIFTED IN?
    SBIT 2,                          PORTLC      ; PUT L2=0
    JMP STP                                      ; WHEN TRUE, DO STOP
                                                 ; CONDITION AND
                                                 ; RETURN

    .FORM

SHFT:
    LD A, [B],                                   ; ROTATE BITS ONE
    RRC A                                        ; POSITION RIGHT
    X A, [B]
    JP LOPB

        ************************************
        ; * * SIMPLE ROUTING TO DO 40 MSEC DELAY * *
        ************************************
```

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```
WAIT:
    LD 0F1                  #0.20       ;SIMPLE WAIT LOOP

LOPD:
                                        ;TO PRODUCE>40MSEC
    LD 0F2,                 #OFF        ;TIMEOUT

LOPC:
                                        ;TO PROPERLY PROGRAM
    DRSZ 0F2,                           ;EEPROM. TIME REQUIRED
    JP LOPC,                            ;TO ERASE/WRITE
    DRSZ0F1,                            ;THE EEPART.
    JP LOPD
    RET

ACK1:
    SBIT 2,                 PORTLC      ;INDICATE TO EE-PROM
    JP ACLK,                            ;(PUT DATA LINE LOW)

ACK:
    RBIT 2,                 PORTLC      ;PUT DATA-LINE HI-Z

ACLK:
                                        ;AND GET ACKNOWLEDGE
    SBIT 3,                 PORTLD      ;8 BITS ARE SHIFTED,
    NOP                                 ;DO A DUMMY CLOCK
    NOP
    NOP
    RBIT 3,                 PORTLD      ;(FOR ACKNOWLEDGE)

    SBIT 2,                 PORTLC
    RET
    .END
```

TL/D/11268–13

Section 5

Quality and Reliability

Section 5 Contents

EPROM and EEPROM Reliability Information 5-3

National Semiconductor

EPROM and EEPROM Reliability Information

Reliability testing of National Semiconductor's EPROMs and EEPROMs has been on the basis of accept on zero, reject on one. Sampling has typically been on the basis of 77 units. Since the qualification for hermetic and plastic devices is somewhat different, they are separated into two sections below.

HERMETIC DEVICES (EPROMs)

Typical packages for EPROMs are the Cer-DIP and Ceramic Leadless Chip Carrier, CLCC. Both meet industry standard hermeticity tests and are monitored as part of the assembly process. The following 3 principal tests are used for qualification of a new device or revision of an existing qualified device:

1. The Operating Life test is at 150°C with V_{CC} at specification maximum—which in most cases is 5.5V. Release is given after 3 lots have completed 500 hours.

Note: The 3 lots are from 3 distinct wafer fabrication and assembly lots. This helps verify the reliability and reproducibility of the device. The stress is continued for at least 1,000 hours to insure the long term performance of NSC EPROMs. The devices are typically programmed to a checkerboard type pattern.

2. The Static Bake test is at 250°C with no power applied. The purpose of this test is to insure the pattern remains correct for many years in customer applications. Acceptance of the pattern is done after 168 hours with no sample failure on 3 separate wafer and assembly lots. The most common pattern utilized is checkerboard, although variations are used depending on the final test flow. Our goal is to verify that no loss of pattern or pattern sensitivity has occurred. The testing is continued beyond 168 hours to determine performance margin and initial durability. The devices are tested for total electrical performance with emphasis on any charge change characteristic.
3. The Temperature Cycling test is done from −65°C to +150°C for 1,000 cycles. The devices are checked for electrical performance. Any degradation is considered a defect. Again, 3 wafer lots are sampled.

PLASTIC DEVICES (EPROMs and EEPROMs)

In addition to the Operating Life, Storage Life, and Temperature Cycling tests mentioned above, Autoclave and Temperature Humidity Bias testing (85:85) are also done.

1. The Operating Life is identical to that of the hermetic testing described above, i.e., 150°C for EPROMs and 1000 hours at 125°C for EEPROMs.
2. Static Bake does not exceed 150°C for both EPROMs and EEPROMs since the plastic molding compounds cannot withstand higher temperatures for an extended period of time. To partially compensate for this, the stress is extended to 1,000 hours at or below 150°C. Again, the pattern is usually checkerboard.
3. The Temperature Cycling is identical to that of the hermetic testing (−65°C to +150°C for 1,000 cycles).
4. Temperature Humidity Bias testing is done at 85°C and 85% relative humidity. The part is programmed and biased in a non-functioning mode with only DC power applied, at 5.5V. The power application is chosen to minimize power consumption to avoid heating the part and to maximize internal fields. The stress is continued for 1,000 hours. Any shift beyond datasheet limits is considered a failure. Any electrical failure prevents qualification.
5. Autoclave is also done on patterned devices. Any shift in electrical characteristics beyond datasheet limits is considered a failure. 168 hours for EPROMs and 500 hours for EEPROMs are minimum duration times. This stress is normally continued beyond 168 hours for both EPROMs and EEPROMs to determine device margins.

EPROM AND EEPROM RELIABILITY AUDITS

Quarterly audits are conducted to make certain there are no changes in the reliability of the product going to customers. The accept criteria is zero for these audits.

Graphs of the 168 and 1000 hour test data are forwarded to corporate management each month to verify that the EPROMs and EEPROMs meet expected standards.

WAFER LEVEL RELIABILITY

In addition to the classic reliability described above, National Semiconductor has a program in place that monitors performance of the dielectrics, metal and poly layers. This program is termed WLR (Wafer Level Reliability), and its purpose is to insure that the layers are processed correctly and perform at their designed values. Examples of dielectric reliability are Q_{bd} (charge to break down), step coverage, and pinhole testing. Examples of metal testing include step coverage, thickness, and hillock control.

EPROM Qualification/Audit Criteria

QUALIFICATION CRITERIA

Test	Conditions		Duration	Accept
Operating Life	V_{CC}: Temperature:	5.5V +125°C	1,000 Hours	0
Temperature/Humidity Bias	V_{CC}: Temperature: Humidity:	5.5V +85°C 85% RH	1,000 Hours	0
Temperature Cycle	−65°C ⟷ +150°C		1,000 Cycles	0
Autoclave (Unbiased)	Temperature: Pressure:	121°C 15 PSIG	168 Hours	0
High Temperature Storage Life	Plastic Temperature:	150°C	1,000 Hours	0
High Temperature Storage Life	Ceramic Temperature:	250°C	168 Hours	0
Electrostatic Discharge (ESD)	Voltage:	±2000V		

EPROM PERIODIC AUDIT CRITERIA

Test	Conditions		Duration	Accept
Operating Life	V_{CC}: Temperature:	5.5V +125°C	1,000 Hours	0
Temperature/Humidity Bias	V_{CC}: Temperature: Humidity:	5.5V +85°C 85% RH	1,000 Hours	0
Temperature Cycle (Unbiased)	−65°C ⟷ +150°C		1,000 Cycles	0
Autoclave (Unbiased)	Temperature: Pressure:	+121°C 15 PSIG	168 Hours	0

EEPROM Qualification/Audit Criteria

QUALIFICATION CRITERIA

Test	Conditions	Duration	Accept
Operating Life Dynamic Burn-In	V_{CC}: 5.5V Temperature: +125°C	1,000 Hours	0
Temperature/Humidity Bias	V_{CC}: 5.5V Temperature: +85°C Humidity: 85% RH	1,000 Hours	0
Temperature Cycle (Unbiased)	−65°C ⟷ +150°C	1,000 Cycles	0
Autoclave (Unbiased)	Temperature: 121°C Pressure: 15 PSIG	500 Hours	0
High Temperature Storage Life	Temperature: 150°C	1,000 Hours	0
Electrostatic Discharge (ESD)	Voltage: ±2000V		

EEPROM PERIODIC AUDIT CRITERIA

Test	Conditions	Duration	Accept
Operating Life (Dynamic Burn-In)	V_{CC}: 6.0V Temperature: +125°C	1,000 Hours	0
Temperature/Humidity Bias	V_{CC}: 5.5V Temperature: +85°C Humidity: 85% RH	1,000 Hours	0
Temperature Cycle (Unbiased)	−40°C ⟷ +150°C	1,000 Cycles	0
Temperature Cycle (Unbiased)	−65°C ⟷ +150°C	1,000 Cycles	0
Autoclave (Unbiased)	Temperature: +121°C Pressure: 15 PSIG	500 Hours	0

Note: Except for MIL-AERO parts, all EEPROMs are shipped in plastic packages.

Section 6

Physical Dimensions

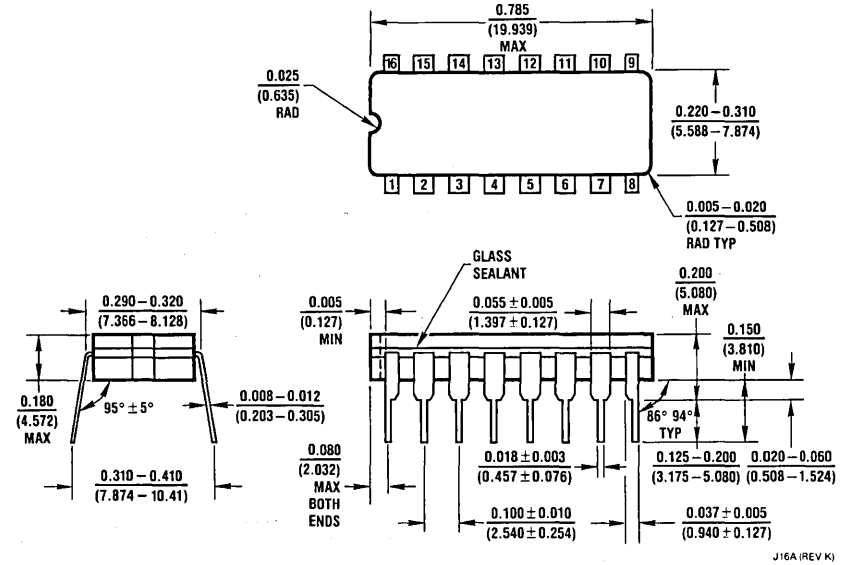
Section 6 Contents

Physical Dimensions 6-3
Bookshelf
Distributors

National Semiconductor

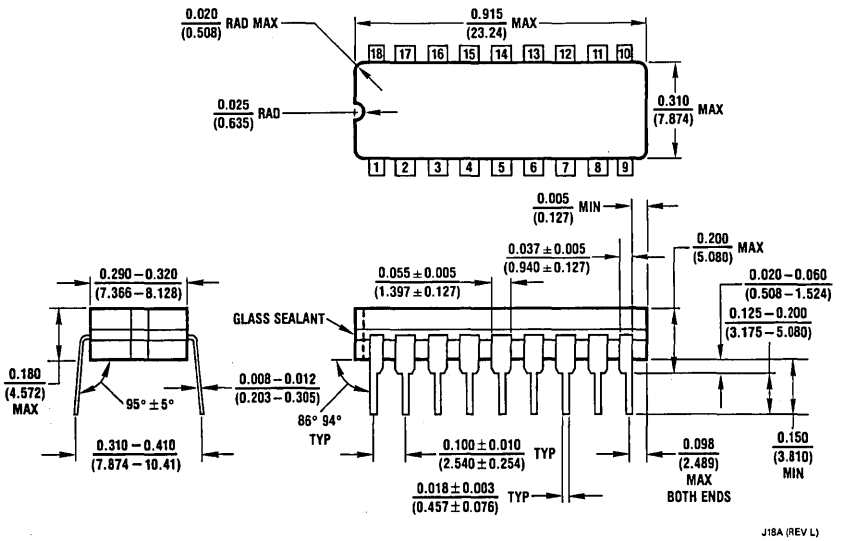
All dimensions are in inches (millimeters)

16 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



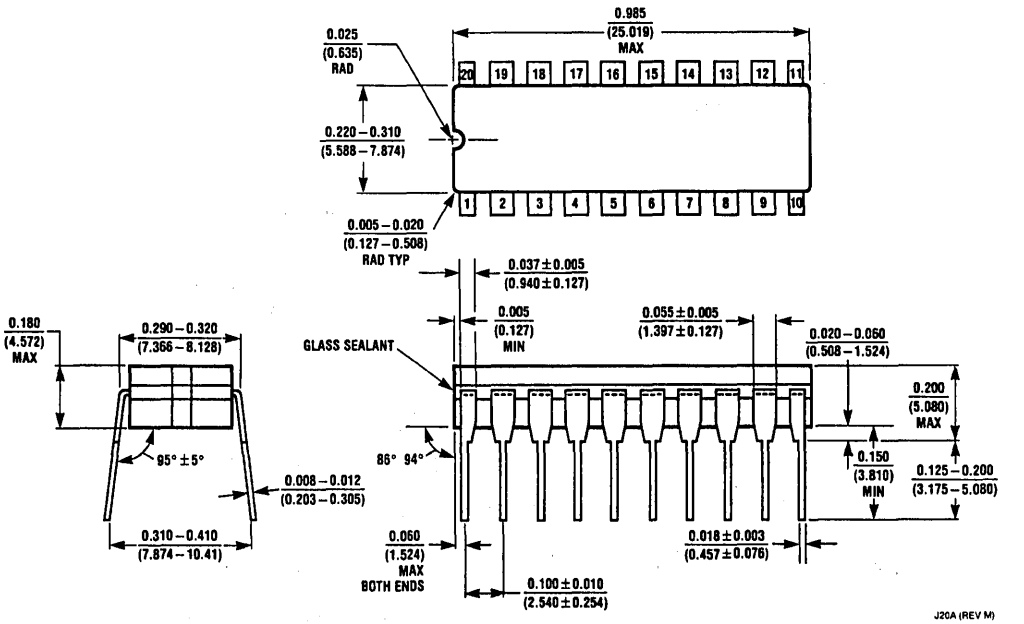
J16A (REV K)

18 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J18A



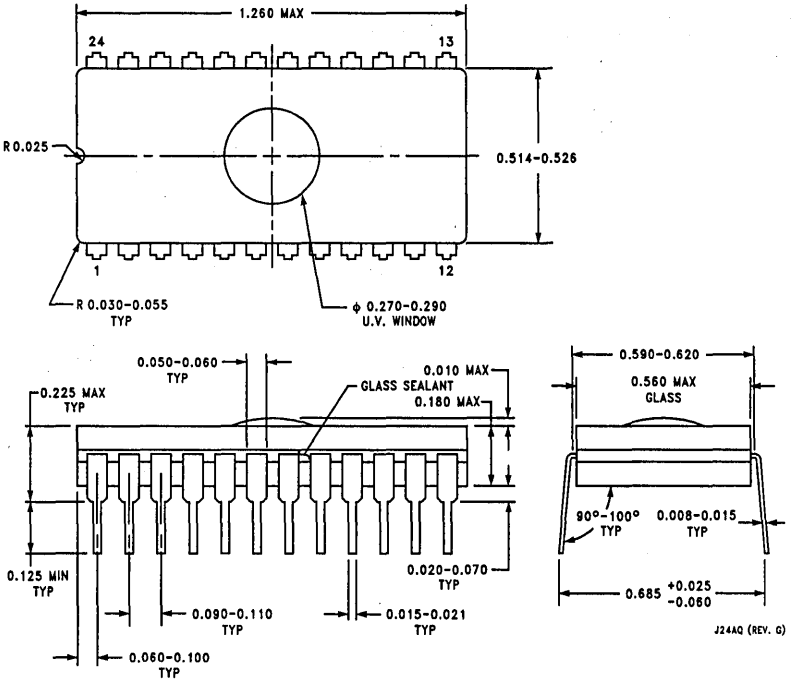
J18A (REV L)

20 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J20A



J20A (REV M)

24 Lead EPROM Ceramic Dual-In-Line Package (JQ) (Small Window)
NS Package Number J24AQ



J24AQ (REV. G)

28 Lead EPROM Ceramic Dual-In-Line Package (JQ) (Small Window)
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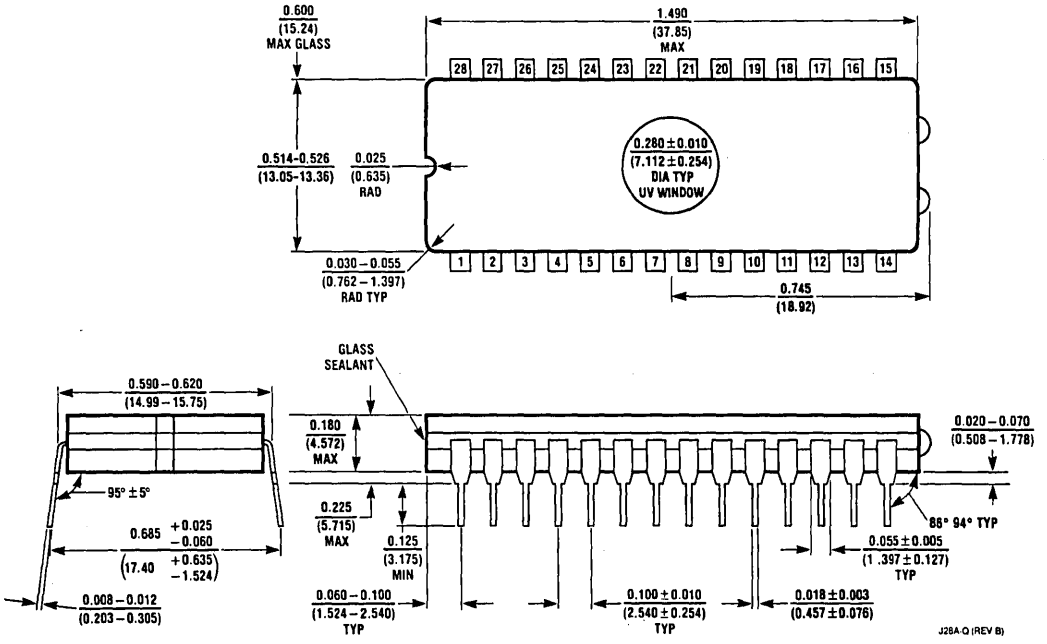
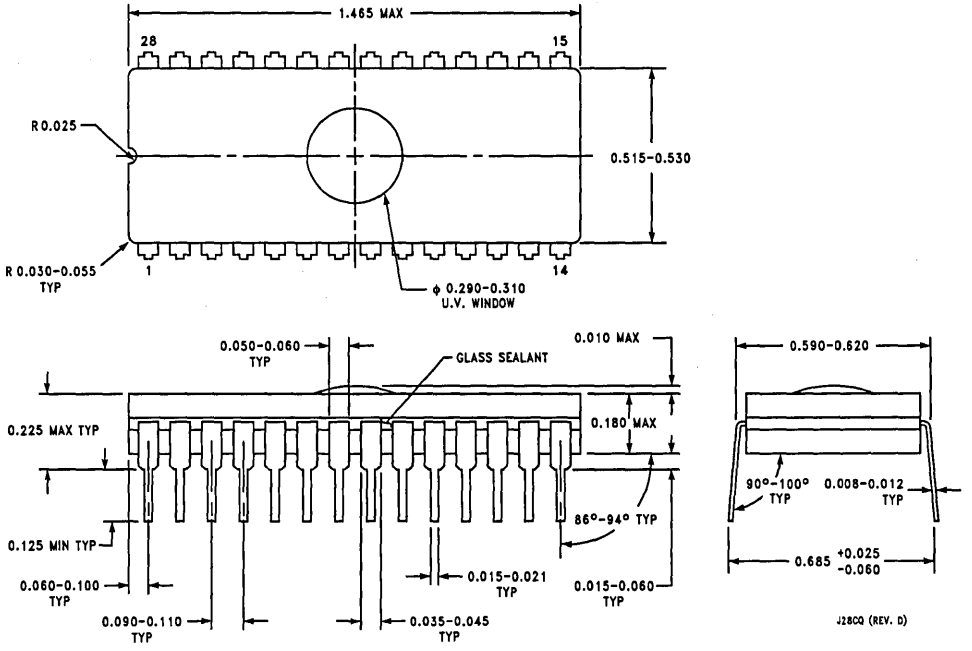


28 Lead EPROM Ceramic Dual-In-Line Package (JQ) (Medium Window)
NS Package Number J28CQ



32 Lead EPROM Ceramic Dual-In-Line Package (JQ)
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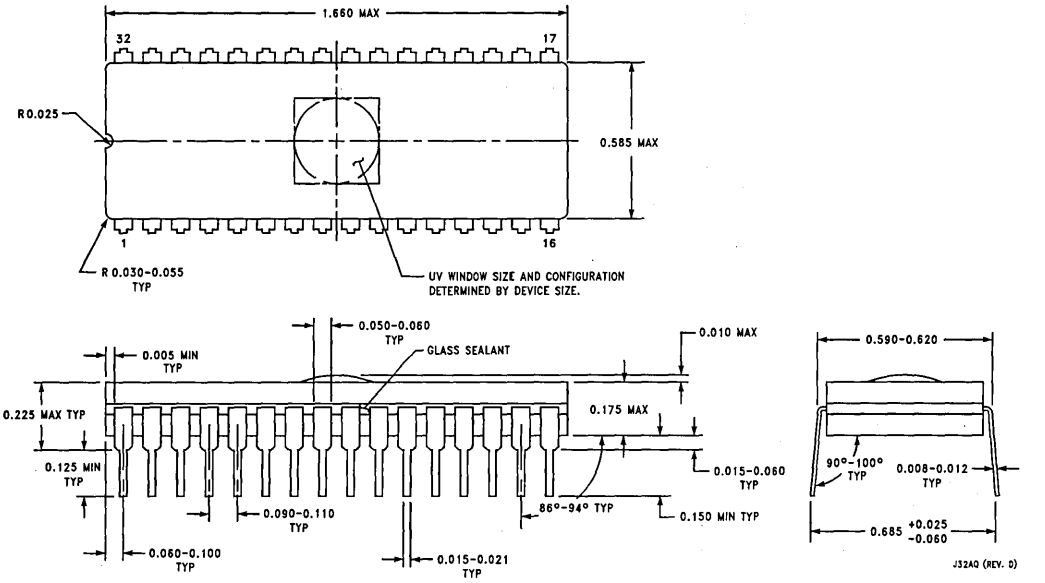

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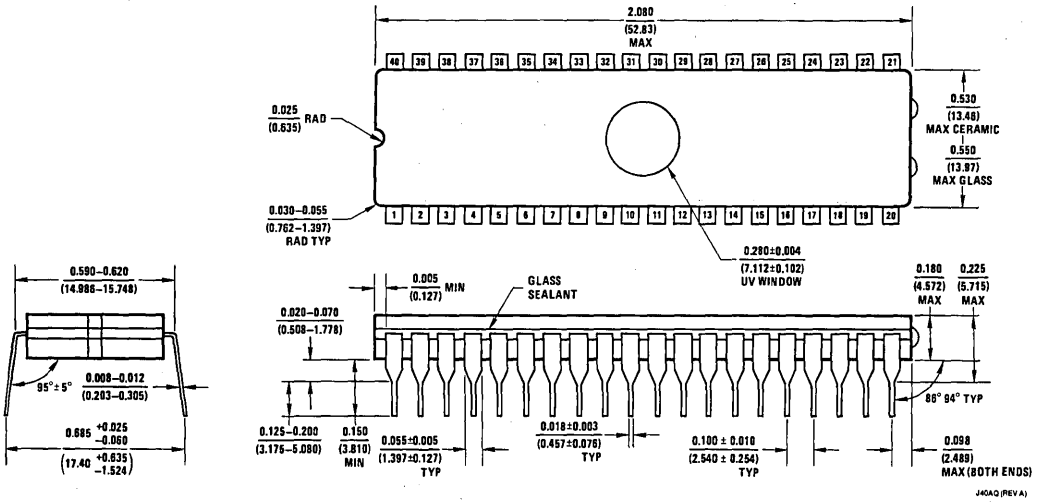
NS Package Number J40AQ



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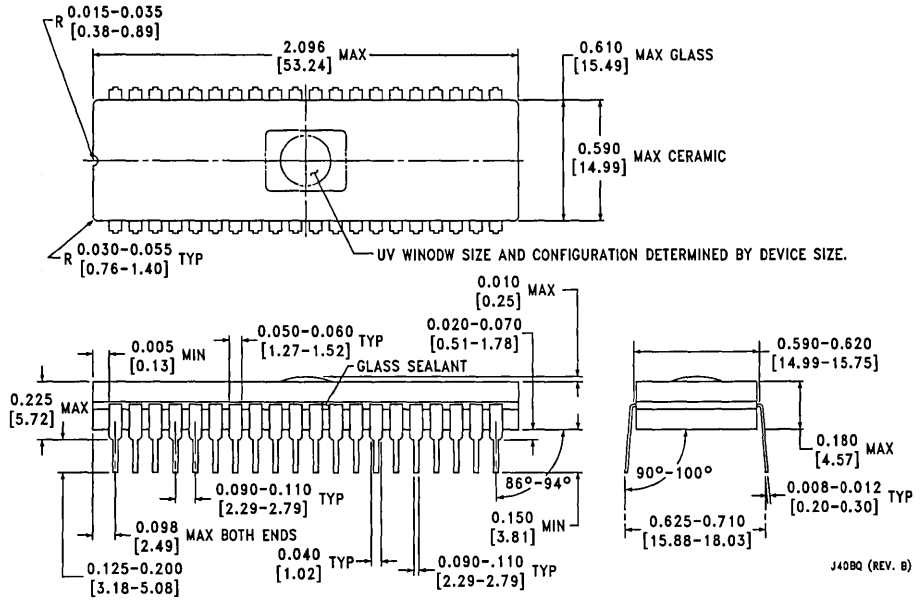
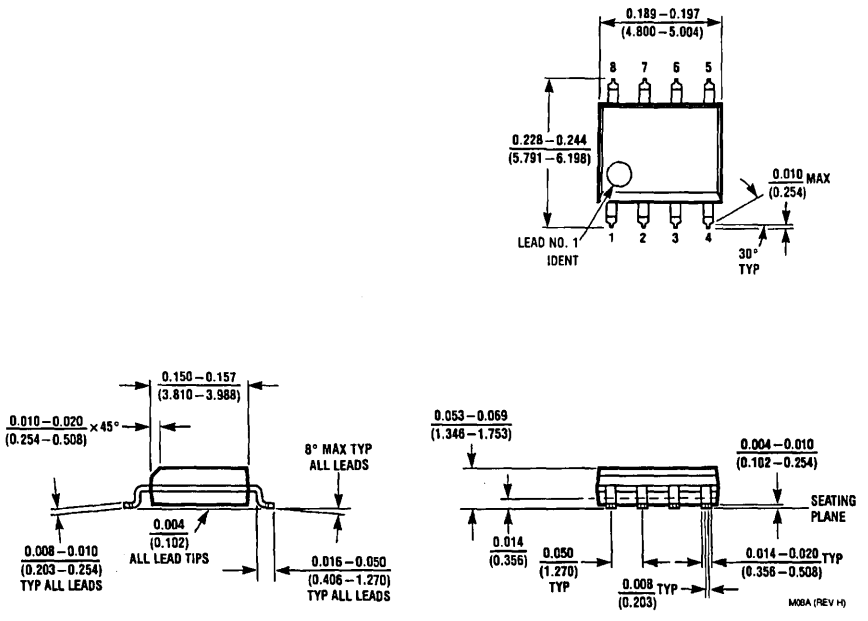
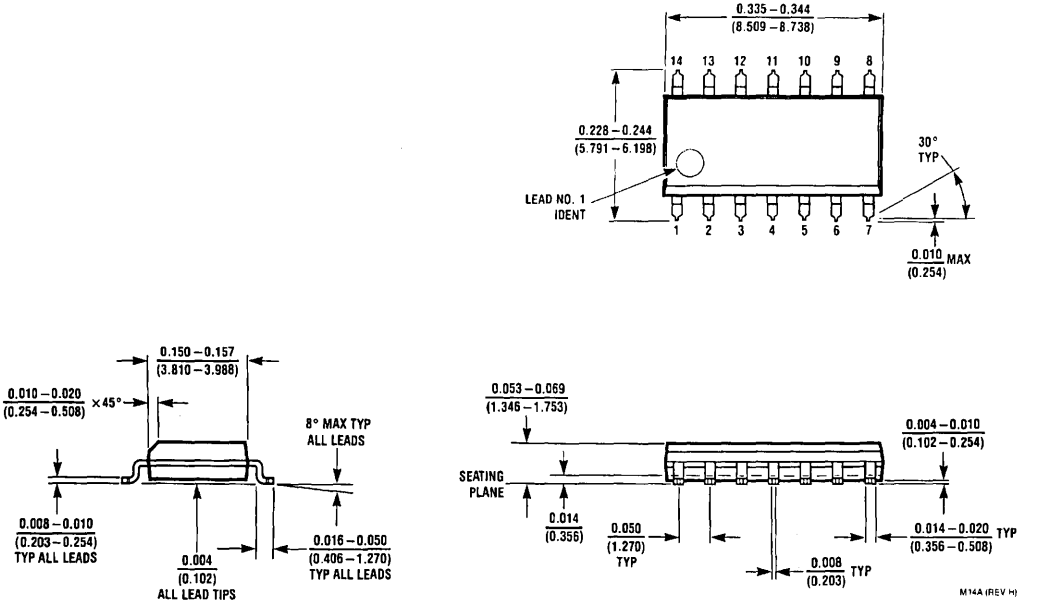
NS Package Number J40BQ



8 Lead (0.150" Wide) Molded Small Outline Package (M)
NS Package Number M08A



14 Lead (0.150" Wide) Molded Small Outline Package (M)
NS Package Number M14A



14 Lead (0.300" Wide) Molded Small Outline Package (M)
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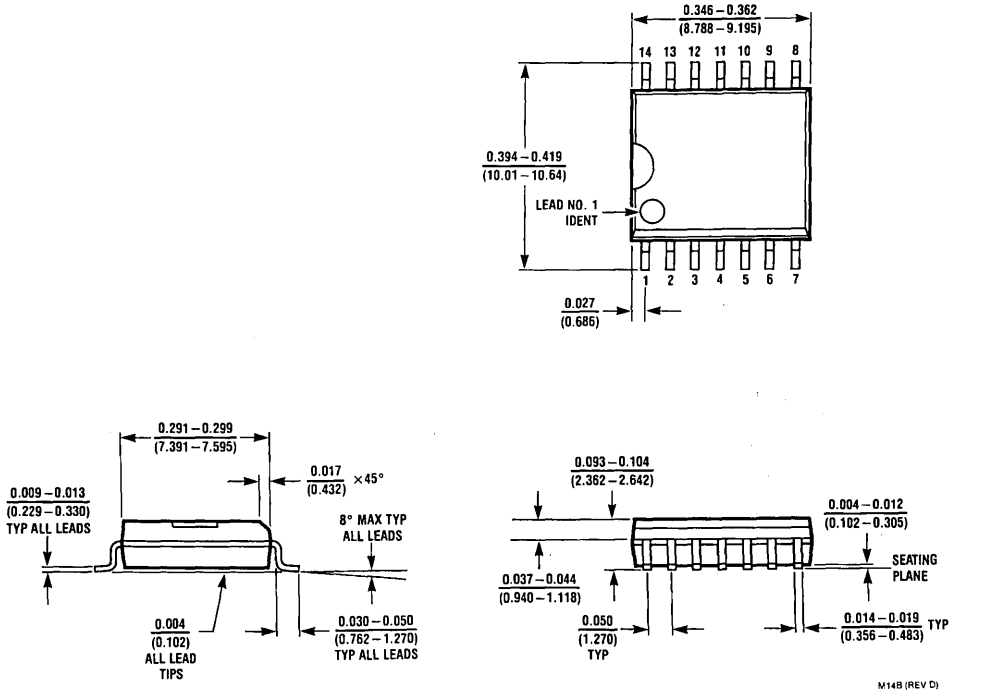
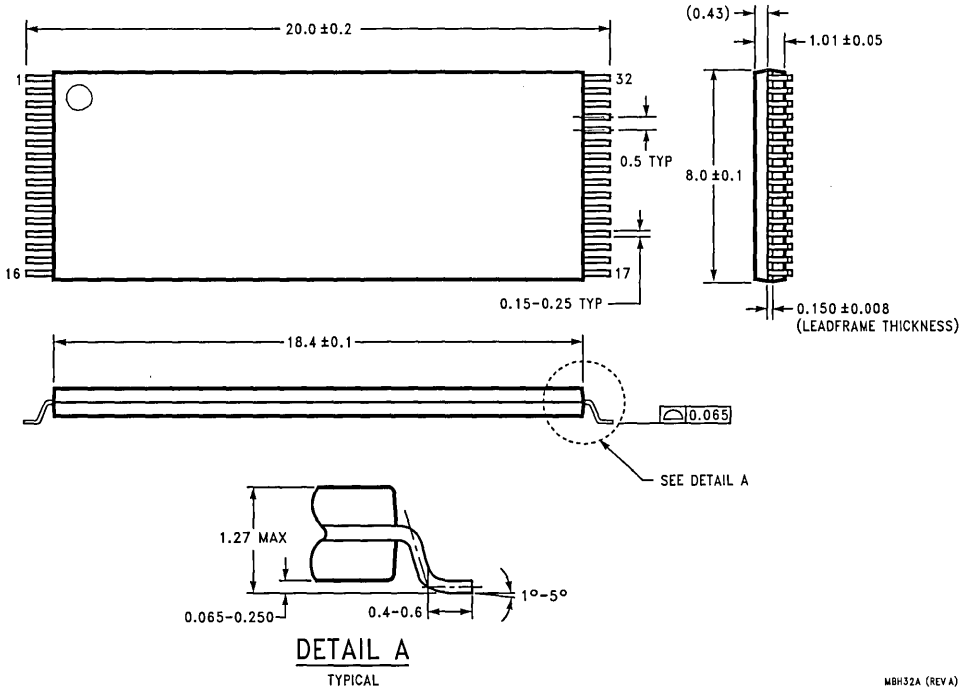
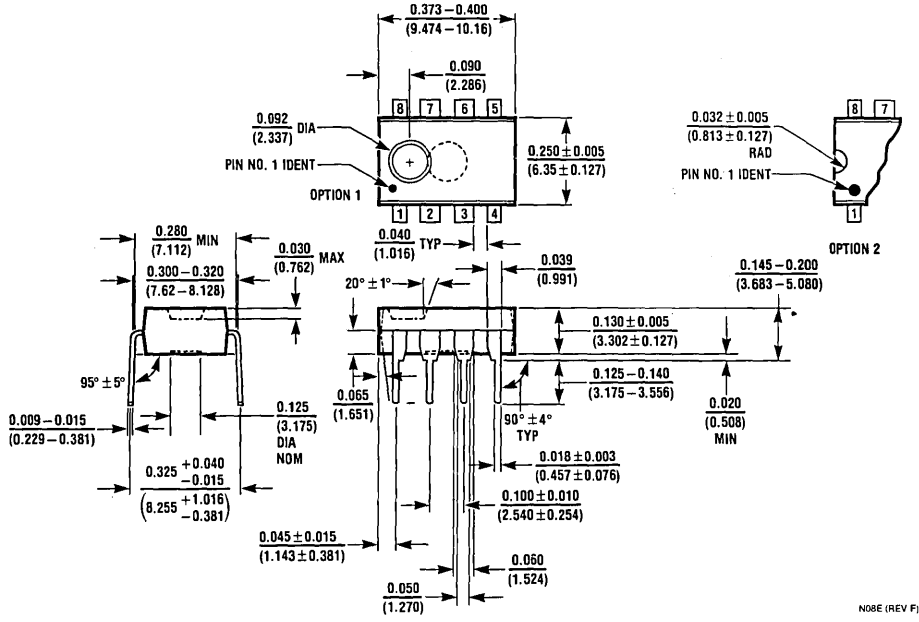


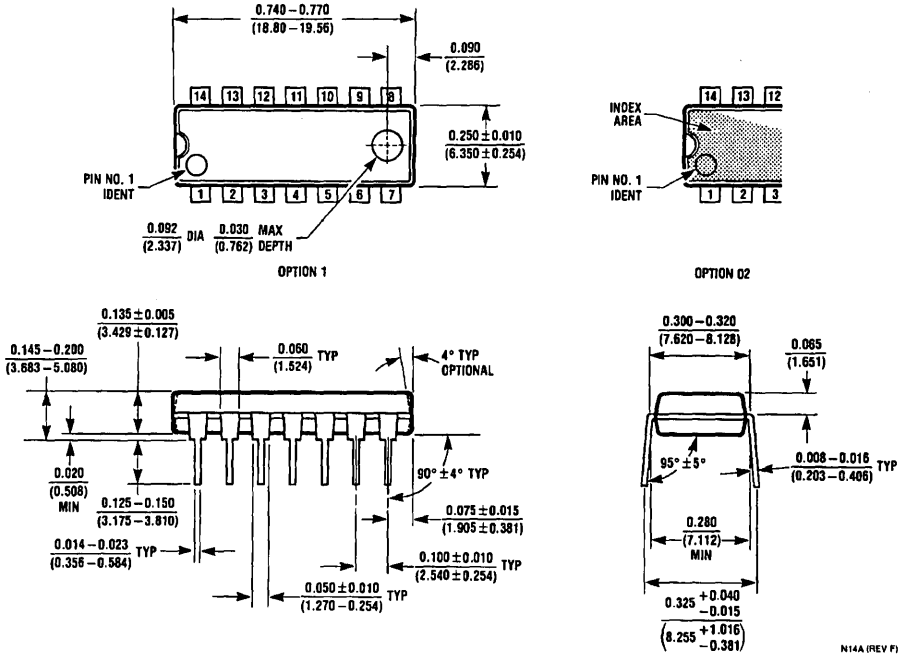
32 Lead TSOP, EIAJ Type I (M)
NS Package Number MBH32A



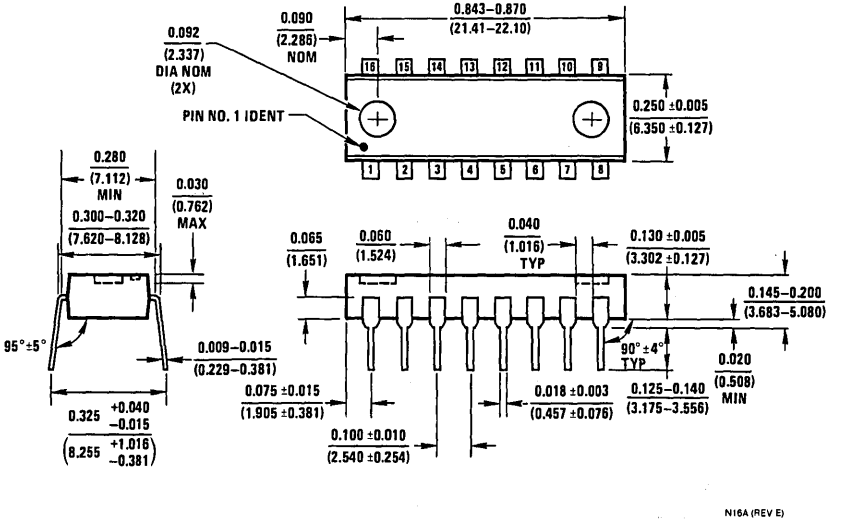
8 Lead Molded Dual-In-Line Package (N)
NS Package Number N08E



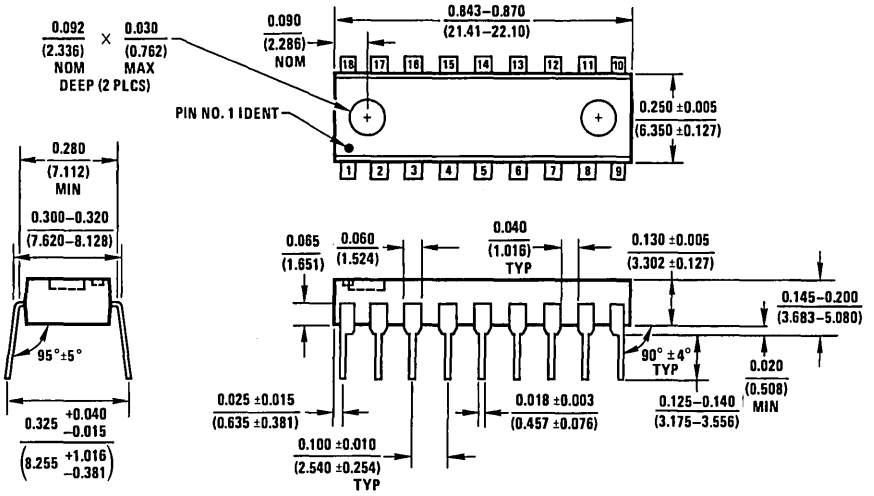
14 Lead Molded Dual-In-Line Package (N)
NS Package Number N14A



16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16A

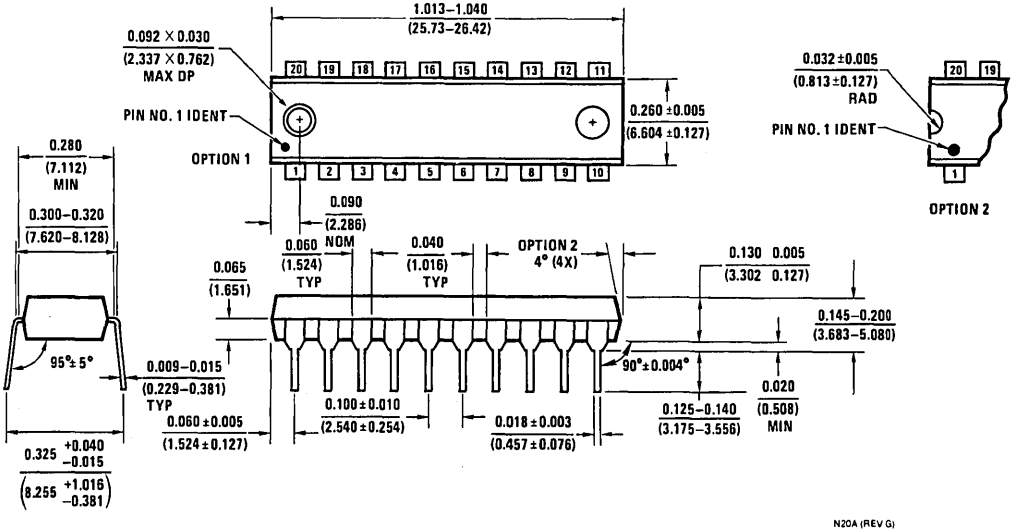


18 Lead Molded Dual-In-Line Package (N)
NS Package Number N18A



N18A (REV E)

20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20A



N20A (REV G)

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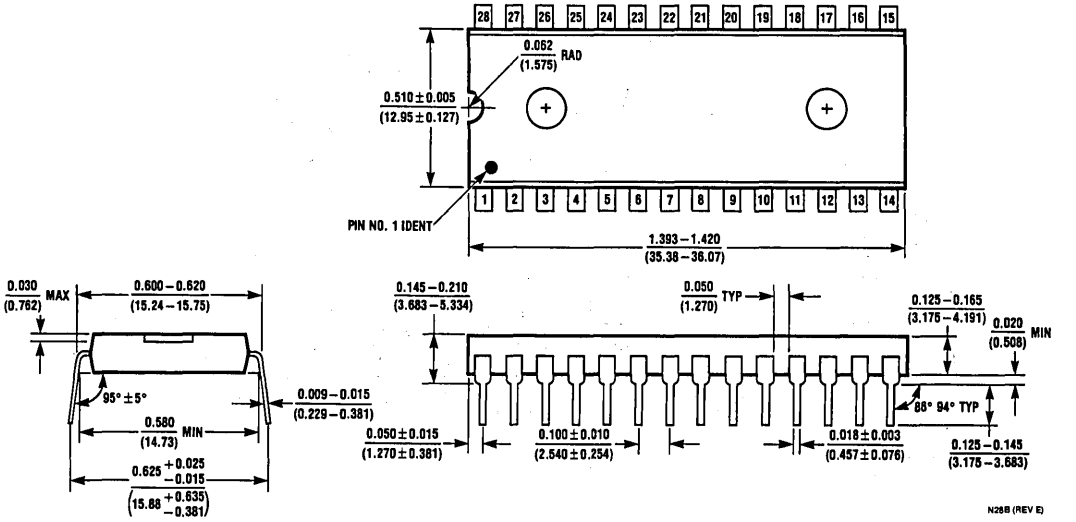
NS Package Number N28B



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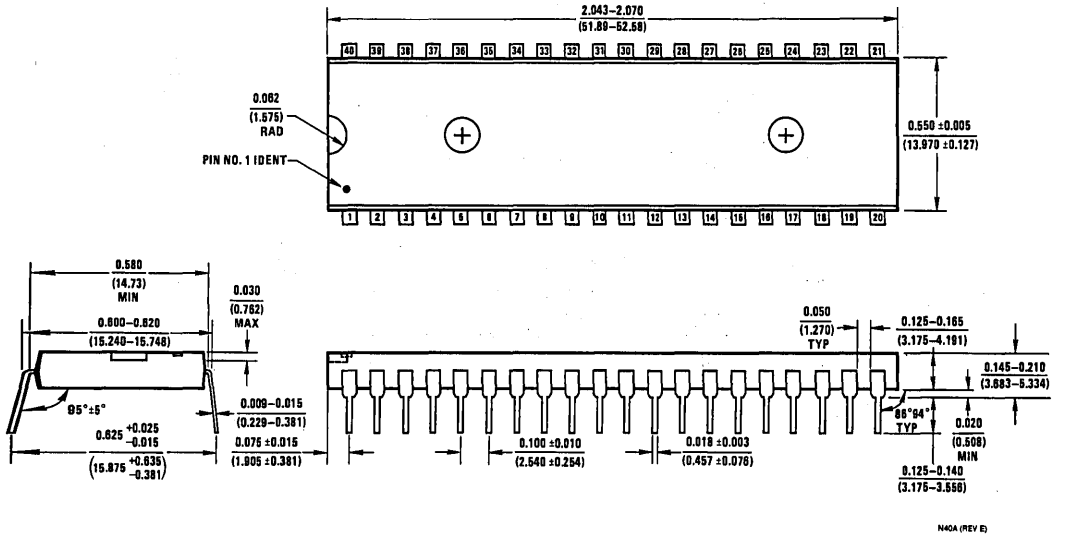

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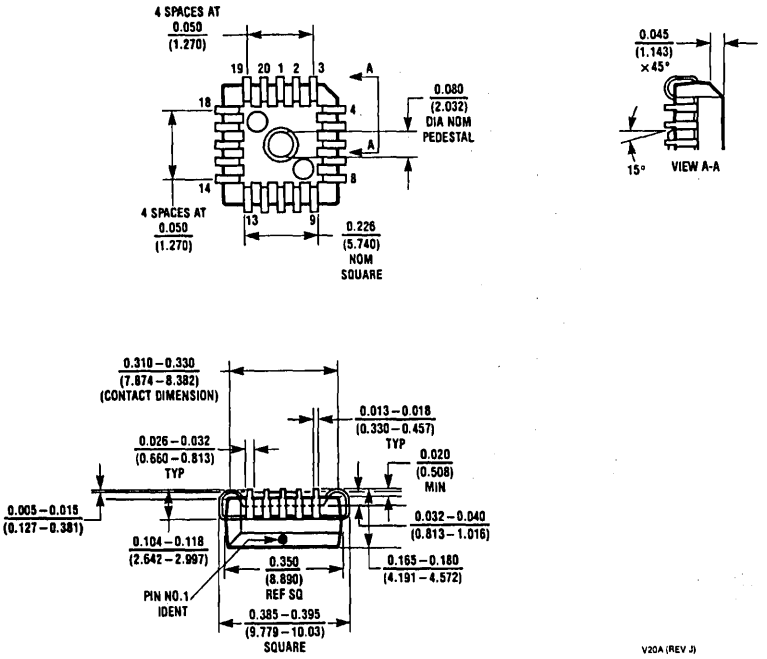

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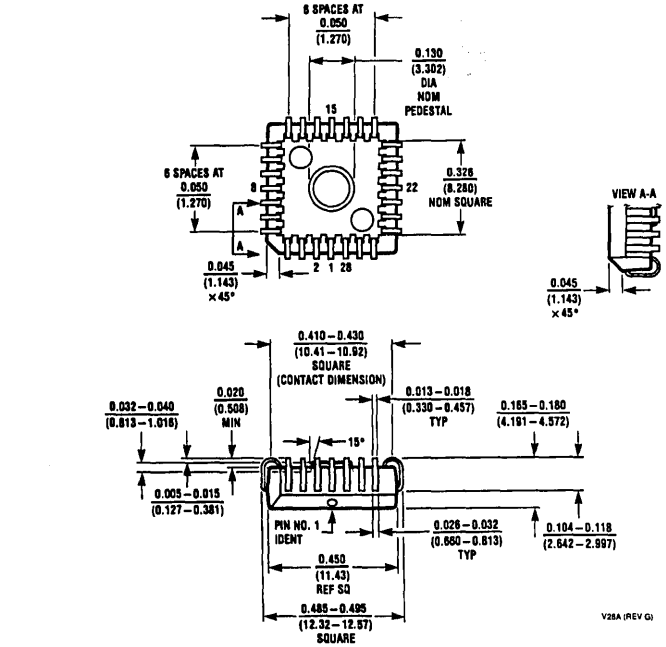

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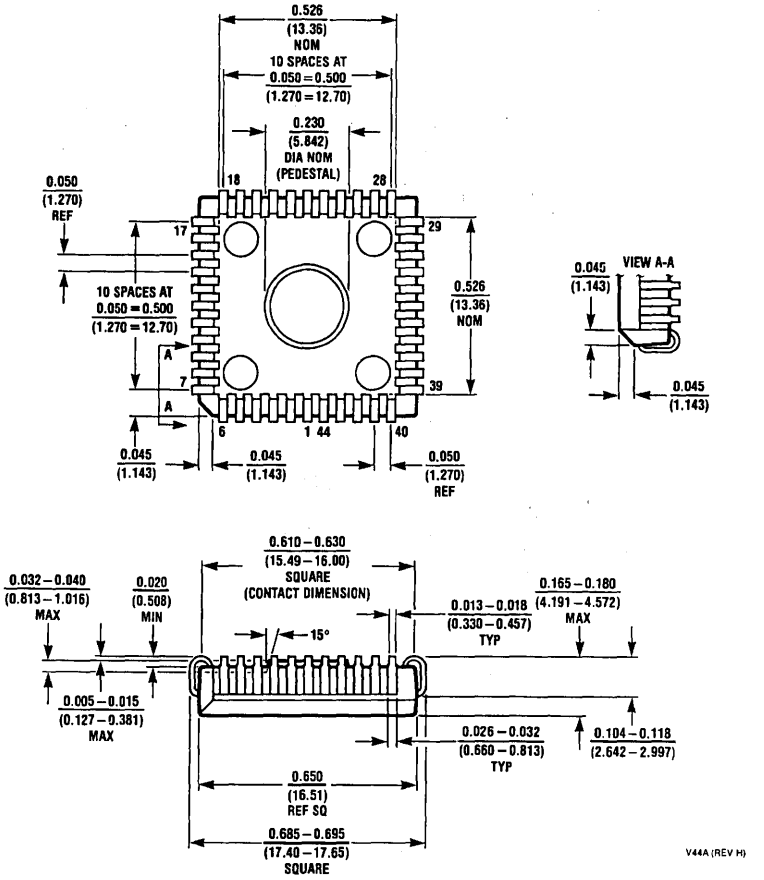

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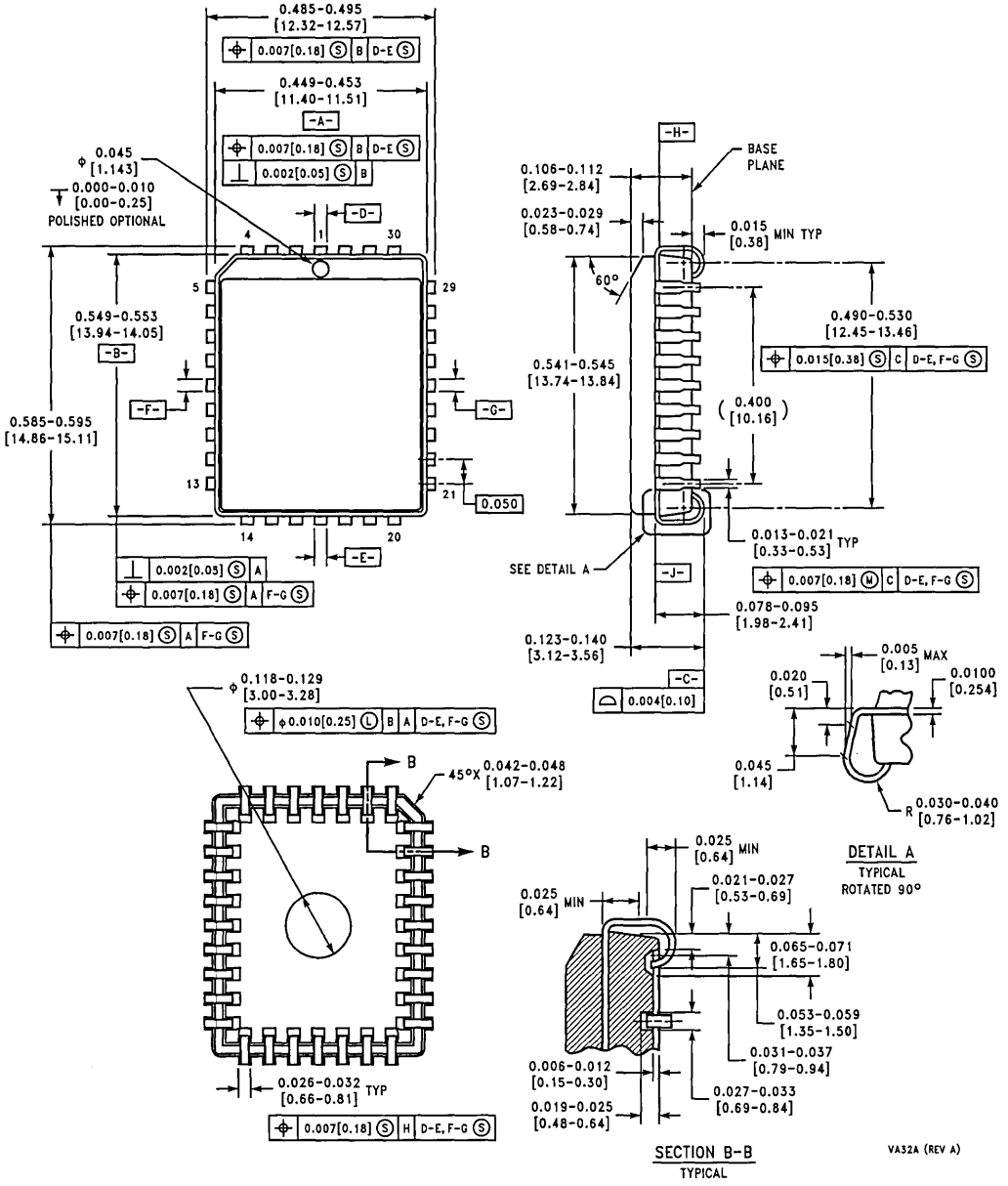

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