A 48 MB/S DISK DRIVE DATA SEPARATOR

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Abstract

A high speed data separator/endec has been developed. The 48 Mb/s serial data is converted to a parallel 8 bit byte for NRZ data transfer at a 6 MHz clock rate.

Introduction

Recent work in the disk drive industry has been paced by the increasing levels of integration in the data channel. A key factor in this advance has been the continuing improvement in IC performance characteristics for these applications. Present development work is moving towards data rates in excess of 25 Mb/s. Besides the speed increases, these data rate ranges impose tighter requirements on the accuracy of such parameters as read data window positioning and write data precompensation. Additionally, many disk drive controller interfaces are based on technologies that begin to develop limitations at clock rates above 25 MHz.

Therefore work was undertaken to develop an integrated circuit that would address these issues. A 48 Mb/s data rate was selected as the target performance level for the data channel. For systems utilizing a 1,7 RLL encoding scheme, this translates to a 72 MHz encoded data rate. In order to relax the requirements on the controller interface, an 8 bit serial to parallel conversion function was also included on the IC. As a result, the controller can operate on a full byte of data during each clock cycle, while running with a reasonable 6 MHz clock. A challenge imposed by this interface is the requirement to maintain correct timing relationships as operating modes are switched. Also of concern is the presence of additional noise generated by the many TTL output drivers. This includes the 8 bit data port, a parity bit, and two generated clock signals. Therefore, another objective was to create a data synchronization function that could maintain its performance characteristics within this environment.

The Design

The architecture shown in the Figure 1 block diagram was used to implement this design. In the read mode, the circuit performs data synchronization, sync field search and detect, and data decoding. For soft sector applications, an address mark detect function is also available.

While the device is in idle mode, the PLL is kept locked to the reference clock. When a read operation is initiated, the PLL is switched over to the incoming read data. Once lock is achieved, a search is started to find the correct bit sequence to synchronize the decoder to the read data. After this is achieved, the decoded NRZ data is generated.

The data synchronization includes the capability to adjust the symmetry of the data window. This feature can be used during system testing to evaluate the window margin of the read channel. This design provides 3 digital control bits to allow 7 steps of window shifting in either an early or late direction. An optional external resistor can be added to adjust the magnitude of each step. This analog adjustment capability allows points between the digital shift steps to be monitored. This combination of window symmetry adjustments allows detailed recording of the decode error rate as a function of window size. Since the minimum unit shift can be scaled by the external resistor, this function also can be used during normal read operation to cancel any systematic data channel skew.

In order to allow the decoded serial NRZ data to be converted to a byte format, circuitry is included that allows a sync byte

to be loaded into a reference register. Before the initial read operation, the sync byte is loaded into this register. As the data is being decoded, it is compared to the sync byte. When a match is found, it defines the byte boundary in the serial data stream. At that time, the byte clock (RCLK) is in an arbitrary phase relationship to the byte data. Therefore, when the sync byte is found, the timing logic in the clock generator also initiates a synchronization sequence. This sequence realigns the RCLK to the data byte boundary. The operation proceeds in a manner that prevents any short duration glitch pulses from appearing at the RCLK output. NRZ data then appears at the byte output. A parity bit is generated for each output byte.

In write mode, the circuit converts NRZ data into a 1,7 RLL format. When a write sequence is initiated, the internal timing is first synchronized to the write clock for the NRZ input byte. The data is then converted from parallel to serial form. After the data is encoded, write precompensation is performed. This design has 2 digital control bits to allow 3 steps of write precompensation adjustment in either an early or late direction. The magnitude of each step of the precompensation is set by an external reference resistor. The precompensated write data signal is then used to clock a toggle flip-flop, whose output is sent off the chip as WD. Each transition of WD represents a write data bit position.

Testability

As an aid to device analysis, a test mode was included in the design. When the device is in this mode, the PLL is disabled. This allows the VCO to be directly controlled for measurement of the center frequency and dynamic range. A read operation in test mode is directly controlled by the reference clock. By synchronizing RD to the reference clock, the read decode and the serial to parallel conversion logic can be examined independent of the PLL. Additionally, the decoded serial NRZ data is accessible at the WD output pins.

As an aid to evaluating write mode operation, the write data output flip-flop is kept reset in test mode. Therefore, the WD output is in a known low state upon exit from the test mode.

Experimental Results

The device was implemented with an oxide-isolated bipolar process. Evaluation of initial prototypes indicate nominal operation in excess of the targeted 48 Mb/s NRZ data rate. In read mode the data window centering accuracy is approximately ±0.5ns. The decode window symmetry is controllable down to a minimum step of less than 1ns. As shown in Figure 2, window shifts up to 21% can be set. In write mode, the write data precompensation can be adjusted to step sizes below 1ns. Figure 3 shows the 1x, 2x, and 3x shifts over a range of external precompensation resistor settings.

Conclusions

This design provides a means for operating a disk drive data channel at a 48 Mb/s data rate while allowing a much slower 6 MHz controller to interface with it. The circuitry includes additional functions that are important for such a high data rate application. The window symmetry control function allows accurate evaluation of the read channel decode window margin. The write precompensation feature allows accurate positioning of the encoded data on the media.

References

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[2] C. D. Mee and E. D. Daniel, *Magnetic Recording, Volume II,* McGraw-Hill, 1988.

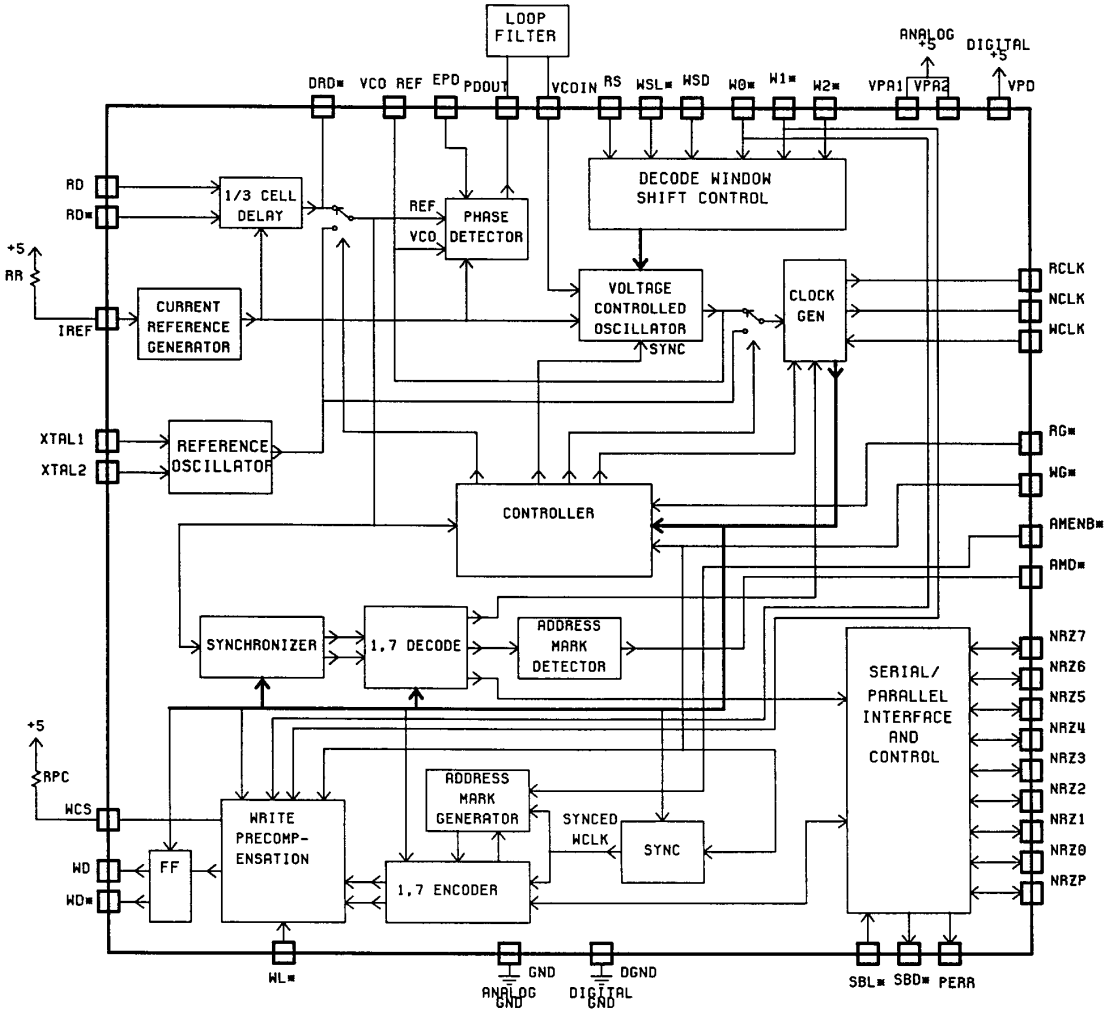

Figure 1 Block Diagram

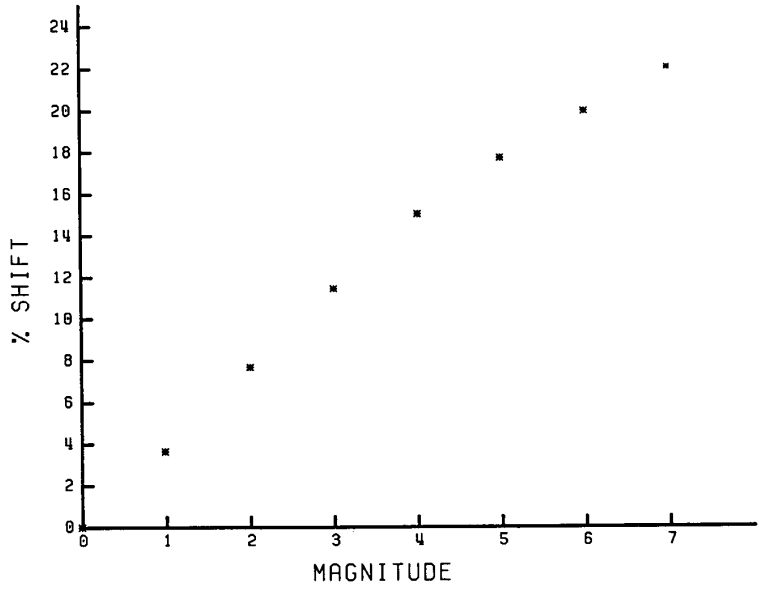

Figure 2 Window Shift

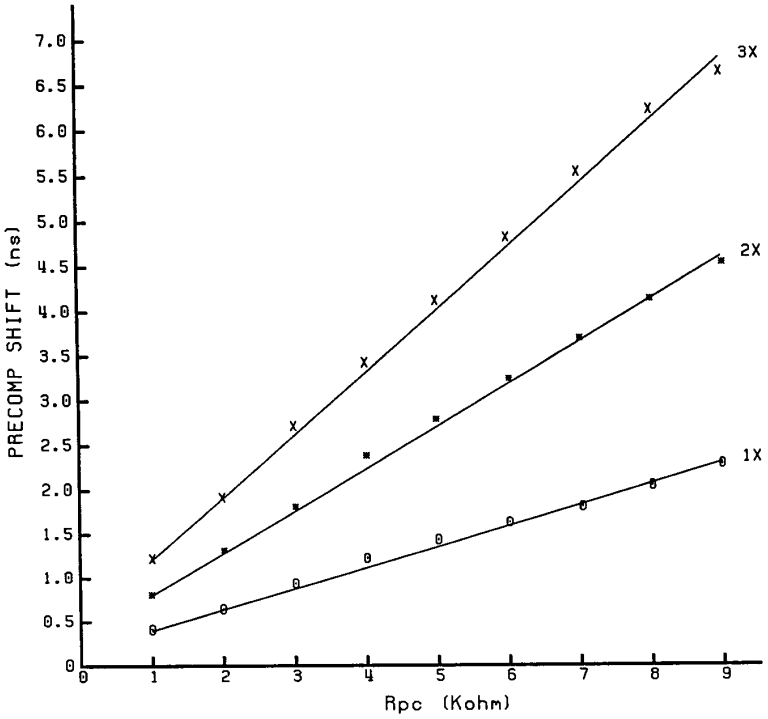

Figure 3 Write Precompensation Shift